EXPERIMENT #9 TIMING CIRCUITS USING TIMER IC 555

I OBJECTIVE

The objective of this experiment is to familiarize the student with timing applications such as monostable and astable multivibrators.

II COMPONENTS AND INSTRUMENTATION

The focus will be on the timer IC 555 which is an 8-pin IC (Fig. 9.1). For power supply, you will use +5 V. As well, you need some resistors and capacitors. Note that it is important to bypass each power supply directly on your prototyping board, using a parallel combination of a 100μF tantalum or electrolyte capacitors and or 0.1 μF low inductance ceramic capacitor. For measurement, you will use a two channel oscilloscope.

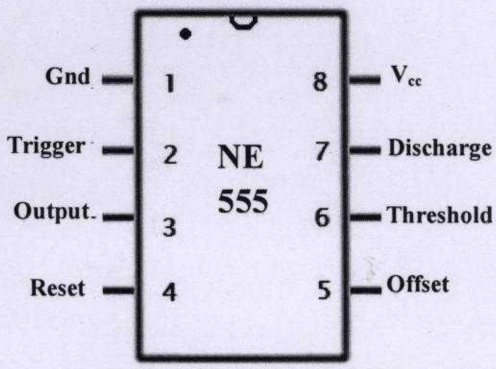


Fig. 9.1 Pin diagram of IC 555

III BRIEF THEORY

The IC 555 timer must be one of the most useful ICs ever made and it is used in many projects. With just a few external components it can be used to build many circuits and not all of them involve timing! The NE555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the monostable mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered or reset (on falling edge) and the output structure can source or sink up to 200mA.

3.1 The monostable multivibrator circuit (shown in Fig.9.2) produces a single output pulse when triggered. The duration of the pulse is called the **time period** (T) and this is determined by resistor R_1 and capacitor C_1. The time period is given by

$$T = 1.1 \times R_1 \times C_1$$

where T is the time period in seconds (s), R_1 is the resistance in ohms (Ω) and C_1 is the capacitance in farads (F). *The maximum reliable time period is about 10 minutes.* Fig.9.3 shows the typical waveforms of the trigger, the output voltage and the capacitor voltage.

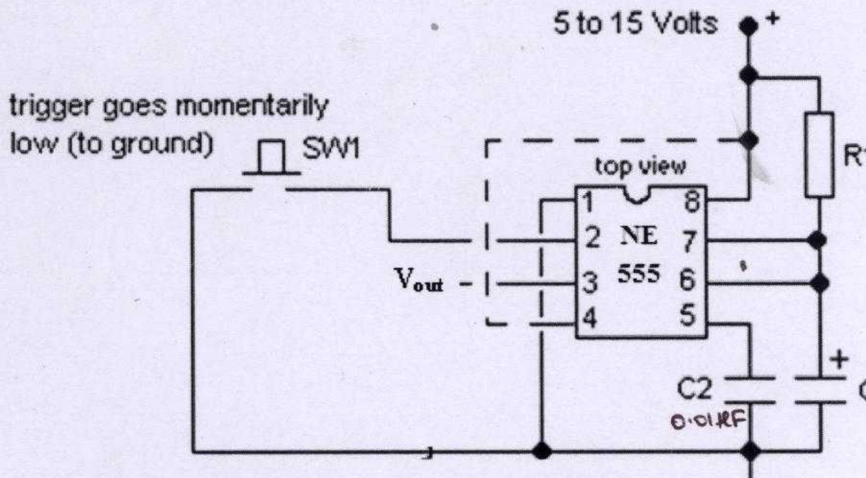


Fig.9.2 Monostable operation with IC 555

3.2 An astable multivibrator circuit (shown in Fig.9.4) produces a 'rectangular wave'. This is a digital waveform with sharp transitions between low (0V) and high ($+V_{cc}$). The high (ON) and low (OFF) durations are given by

$T_{on} = 0.7 \times (R_1 + R_2) \times C_1$ and

$T_{off} = 0.7 \times R_2 \times C_1$

The time period (T) of the square wave is the time for one complete cycle.

$T = 0.7 \times (R_1 + 2R_2) \times C_1$

where T is the time period in seconds (s), R_1 is the resistance in ohms (Ω), R_2 is the resistance in ohms (Ω) and C_1 is the capacitance in farads (F).

Duty cycle: The duty cycle of an astable circuit is the proportion of the complete cycle for which the output is high. It is usually expressed as a percentage.

Percentage duty cycle $\delta = (T_{on}/T) X100$

Fig.9.5 shows the typical waveforms of the output voltage and the capacitor voltage.

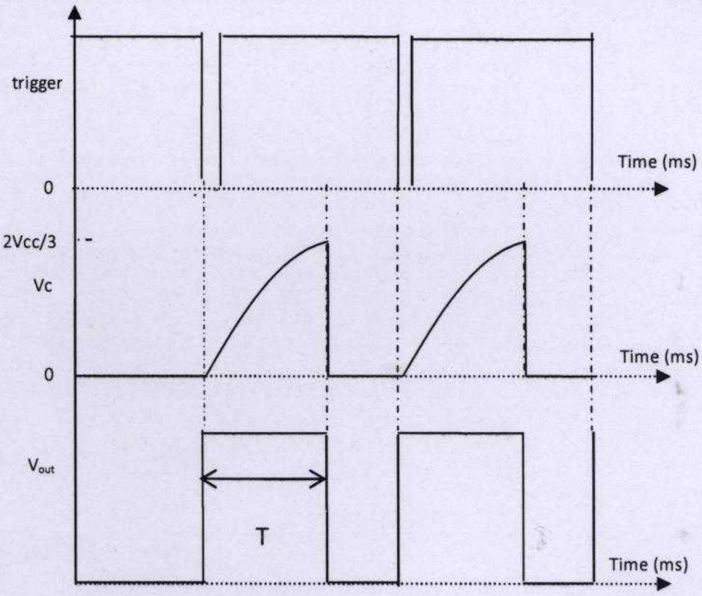


Fig. 9.3 Typical waveforms for monostable operation with IC 555

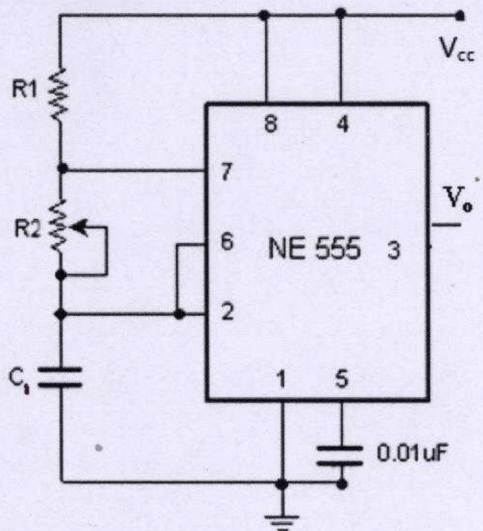


Fig. 9.4 Astable mode of operation using IC555

Hints for design:

- **Choose C_1 first** (there are relatively few values available).
- **Choose R_1** and **R_2** to give the timing intervals. These resistors should be in the range 1k Ω to 1M Ω. Use a fixed resistor of at least 1kΩ in series if R_1 is variable (this is not required for R_2 if it is variable).

IV PREPARATION

(Answers may be given on the reverse side.)

1. Design a circuit using IC555 to produce a rectangular output with T_{on} of 0.95ms at a frequency of 1kHz.
2. With the output from the circuit in previous question as the trigger signal, design a circuit using IC555 to produce a monostable output with a pulse width of 0.1ms. Is it true or false that this output is monostable but will appear as a 1kHz clock?

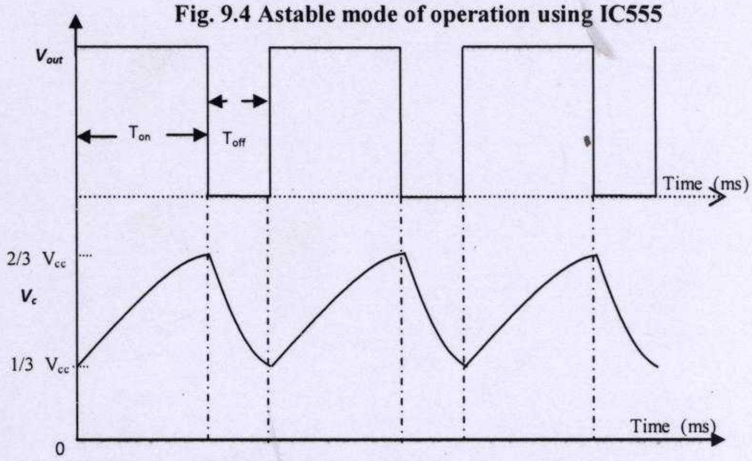


Fig. 9.5 Waveforms for astable operation with IC 555

3. It is necessary that the trigger signal in the monostable mode is normally high and should be low for a very short time. Why is this so? What is the consequence otherwise?
4. The Fig.9.6 shows divide by 3 operation using IC 555 in monostable mode. Can you suggest how this is possible?
5. It is possible to generate a square waveform in astable mode with IC555, by using a diode. Can you suggest where this diode should be connected? Should there be any other changes in the circuit? In the design values?

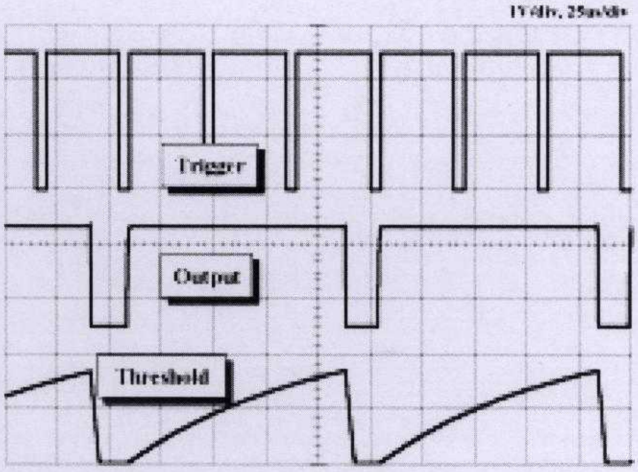


Fig.9.6 Divide by three operation using IC555 as a monoshot

V EXPLORATIONS

5.1

5.11 **Design:** Suggest a circuit to generate a clock signal of time period 'T_m' with T_{onm} specified as below.
T_m= 3msec ; T_{onm}= 2msec (suffix m for monostable). You may use two numbers of IC555, one in astable mode to generate the trigger signal for the other in monostable mode. The trigger signal should have a duty cycle close to unity (90 to 95%) with a suitable frequency. Assume the power supply to be 5V. Compute the resistor and capacitor values (R_{1m}, C_{1m}, R_{1a}, R_{2a} and C_{1a}) for your set up (suffix a for astable).

i) Monostable :

$$T_{onm} = 2\times10^{-3}\,s = 1.1\,R_1'C_1'$$

let $\boxed{C_1' = 0.01\mu F}$

$\therefore$ $\boxed{R_1' = 181.82\ k\Omega}$

ii) Astable :

$$T_m = T_{ON} + T_{OF} = 3ms.$$

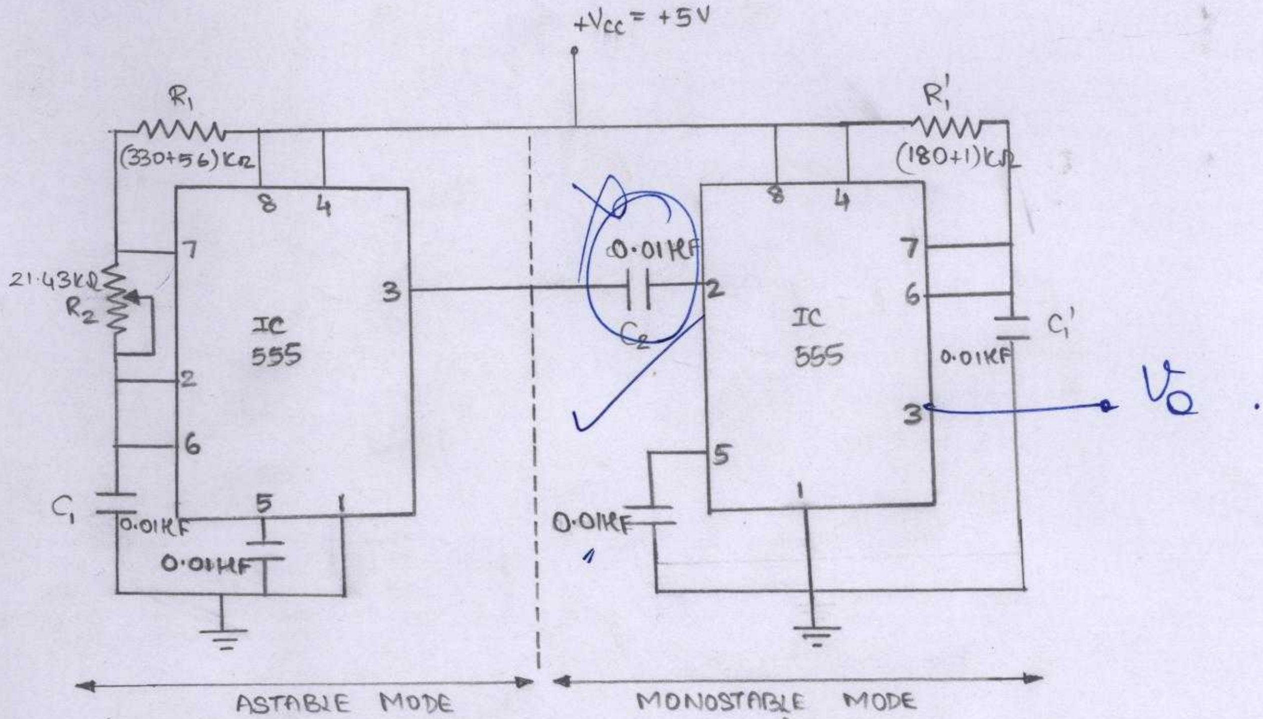
$$\delta = 0.95 = \frac{T_{ON}}{T_m} \Rightarrow \left.\begin{array}{l} T_{ON} = 2.85\ ms \\ T_{OFF} = 0.15\ ms \end{array}\right\} \text{Assume } C_1 = 0.01\mu F$$

$$0.15\times10^{-3} = 0.7\times R_2\,(0.01\times10^{-6})$$

$\boxed{R_2 = 21.43\ k\Omega}$

$$\boxed{R_1 = \frac{2.85\times10^{-3}}{0.7\times0.01\mu F} - 21.43\times10^3} = \boxed{385.71\ k\Omega}$$

5.2 **Draw a neat** circuit diagram with complete detail for your design.



5.3 **Procedure:**

1. Make the connections as per the approved circuit diagram. With the connections approved, switch on the power supply.
2. Firstly verify the working of the astable circuit without connecting its output to the (trigger pin of) monostable circuit.
3. Observe the waveforms of capacitor voltage (V_{ca}) and output voltage (V_{outa}) of astable.
4. Note the timings T_{ona} and T_{offa} and compare with the calculated values. Adjust the setting of any potentiometer to get the required output pulse width.
5. Switch off the supply and connect the output of astable as the trigger input to the monostable circuit.
6. Observe the waveforms of capacitor voltage (V_{cm}) and output voltage (V_{outm}) of monostable circuit.
7. Verify the synchronization of the output of astable and the monostable circuits.
8. Note the timings T_{onm} and T_{offm} and compare with the calculated values.
9. Measure (using LCR bridge) and note the values of resistors and capacitors used.

Table 9.1 Design and measured data							
Astable circuit					Monostable circuit		
T_{ona} (cal)	T_{offa} (cal)	C_{1a}	R_{1a}	R_{2a}	T_{onm} (cal)	R_{1m}	C_{1m}
2.85ms	0.15ms	0.01μF	385.71kΩ	21.43kΩ	2 ms	181.82kΩ	0.01μF
Revised design (rounding to standard resistor values)							
T_{ona} (cal)	T_{offa} (cal)	C_{1a}	R_{1a}	R_{2a}	T_{onm} (cal)	R_{1m}	C_{1m}
2.852ms	0.148ms	0.01μF	386kΩ	21.4kΩ	1.99ms	181kΩ	0.01μF
Actually used (measured)							
T_{ona}	T_{offa}	C_{1a}	R_{1a}	R_{2a}	T_{onm}	R_{1m}	C_{1m}
2.8ms	0.2ms	0.0108μF	383.4kΩ	21.388kΩ	2.1ms	178.4kΩ	0.0108μF

Compute the % error in T_{onm} (based on the measured values of components)

Tonm (measured) = 2.1 ms

Tonm (rounding to standard values) = 1.99ms

$$\% \text{ error} = \frac{2.1 - 1.99}{1.99} \times 100$$

$$= 5.527\%$$

5.3 Plot the observed waveforms of capacitor voltage (V_{ca}), the output voltage (V_{outa}) of the astable, the capacitor voltage (V_{cm}) and the output voltage (V_{outm}) of the monostable on the **same** time frame.

VI. INFERENCE/CONCLUSIONS

i) Thus the 555 Timer is used in astable mode to generate a normally HIGH trigger signal, with a 95% duty cycle

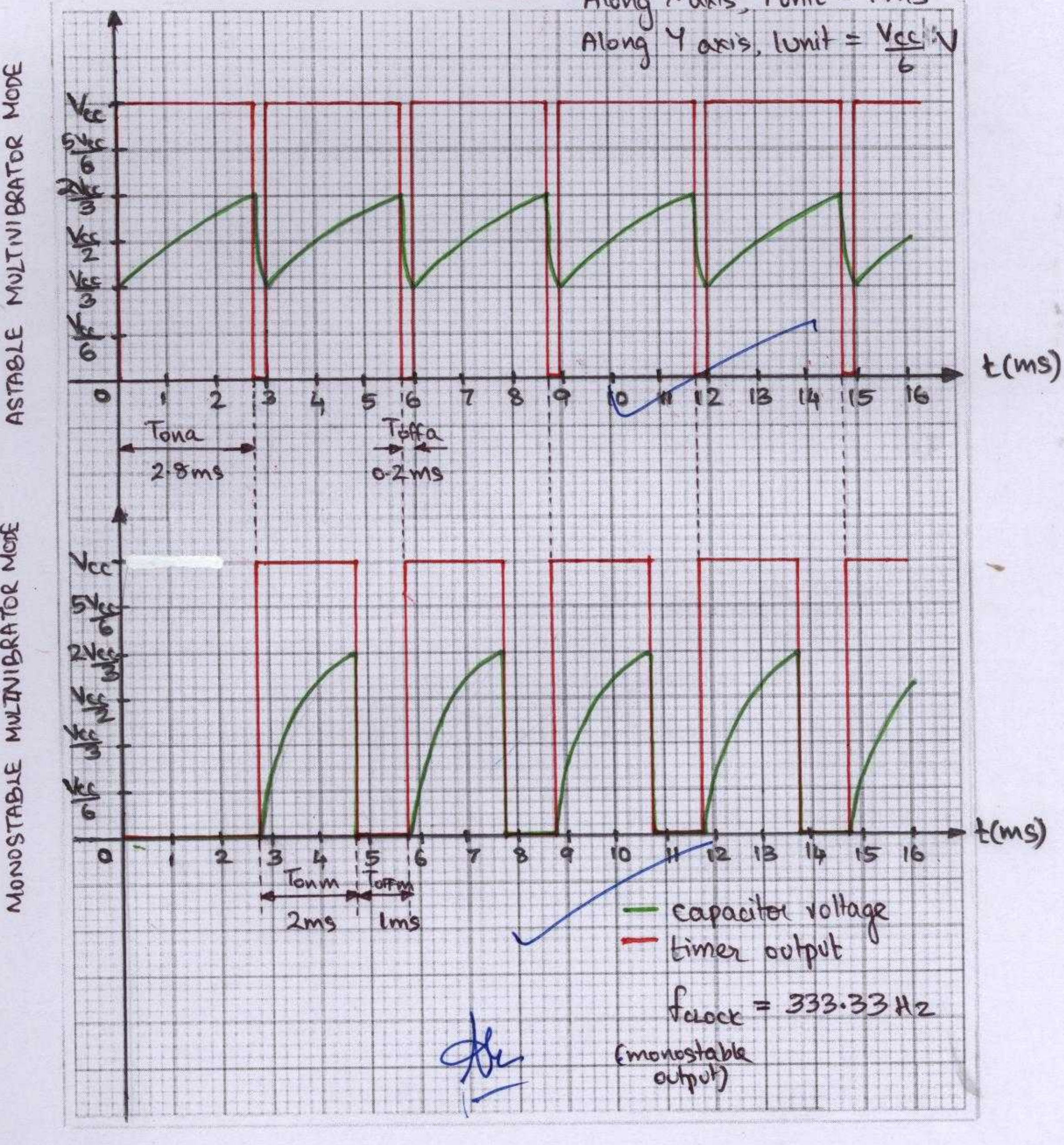
ii) This 90–95% duty cycle is necessary to avoid un-determinable state.

iii) The capacitor charging time in monostable circuit should be lesser than the on-time of the astable output, to get exact frequency

iv) Otherwise, a divide-by-two or divide by 'n' operation would be achieved.

Integrated Circuits Lab		
	Credit	Maximum Marks
Preparation	4.5	5
Experimentation	9 1/2	10
Reporting	5.	5
Total Marks		20

SCALE
Along X axis, 1 unit = 1 ms
Along Y axis, 1 unit = $\frac{V_{cc}}{6}$ V



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EXPERIMENT - 9 PREPARATION

1) $T_{on} = 0.95 ms$

$f = 1 KHz$

$T = 1 ms.$

$T_{off} = 0.05 ms$

Using an astable circuit,

$T_{on} = 0.7 (R_1 + R_2) C_1$

$T_{off} = 0.7 R_2 C_1$

(ie) $0.95 \times 10^{-3} = 0.7 R_1 C_1 + 0.05 \times 10^{-3}$

Let $C_1 = 0.1 \mu F$

$\therefore R_1 = 12.857 k\Omega$

$R_2 = 714.28 \Omega$

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2) Pulse width, $T = 1.1 R_1 C_1$

$0.1 \times 10^{-3} = 1.1 R_1 (0.1 \times 10^{-6})$

$R_1 = 909.1 \Omega \simeq 0.91 k\Omega.$

The output of this monostable multivibrator would have a frequency of 1KHz, as it switches HIGH only at the falling edge of the trigger. Thus it is synchronized with the trigger of 1KHz frequency.

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4) A monostable multivibrator would not get triggered during the time the capacitor gets charged until $\frac{2V_{cc}}{3}$. Thus, any falling edges of the trigger would prove unsuccessful in switching the state of its output during this timing cycle.

- Thus, the pulse width, $T = 1.1 R_1 C_1$ should be slightly larger than twice the input trigger time period, less than thrice the trigger period
- Thus the state of monostable multivibrator changes only in the falling edge of 3rd trigger cycle.
- This would act as a divide by three operation

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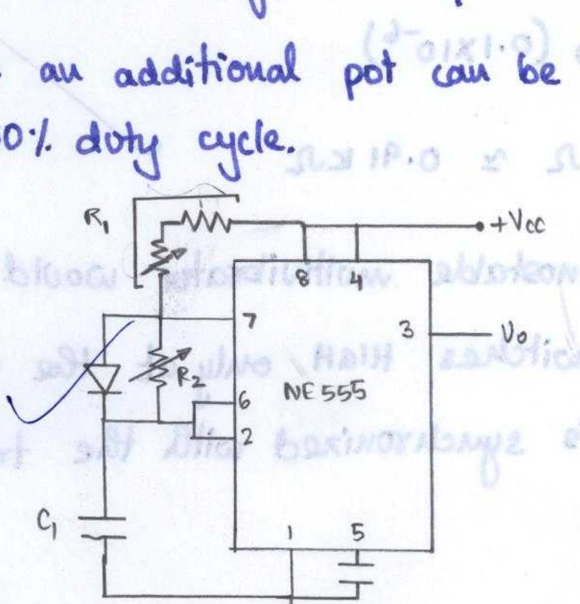
5) The diode can be connected across R_2. Thus during charging, R_2 would be bypassed and $T_{ON} = 0.7 R_1 C_1$. During discharging, $T_{off} = 0.7 R_2 C_1$. Now to get a square wave, $T_{ON} = T_{OFF}$.

Thus an additional pot can be added to R_1, to get a 50% duty cycle.



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3) The trigger signal in monostable mode, when HIGH, keeps the oscilla in stable state. At the falling edge of the trigger, the output toggles. This falling edge should be for a very short duration to prevent undeterminable output state. If the negative period (off time of trigg prevails for a longer time, the 'S' and 'R' of the flip flops might be HIGH. This state is not desired.