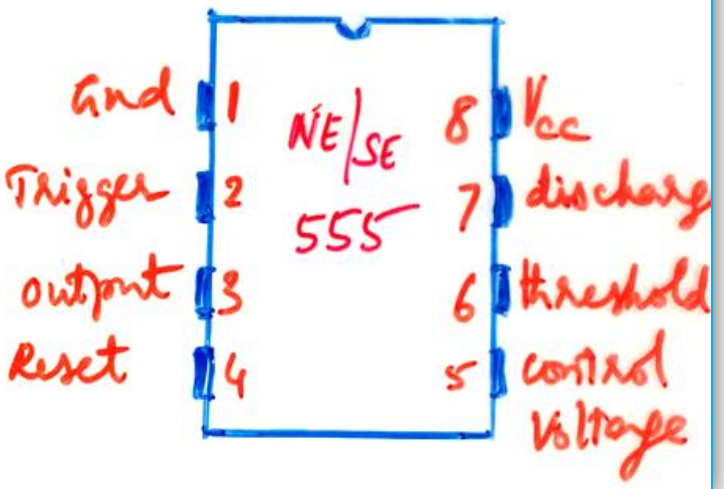
TIMER IC 555

- Timing from MS to hours
- astable & monostable modes
- TTL compatible
- adjustable duty cycle

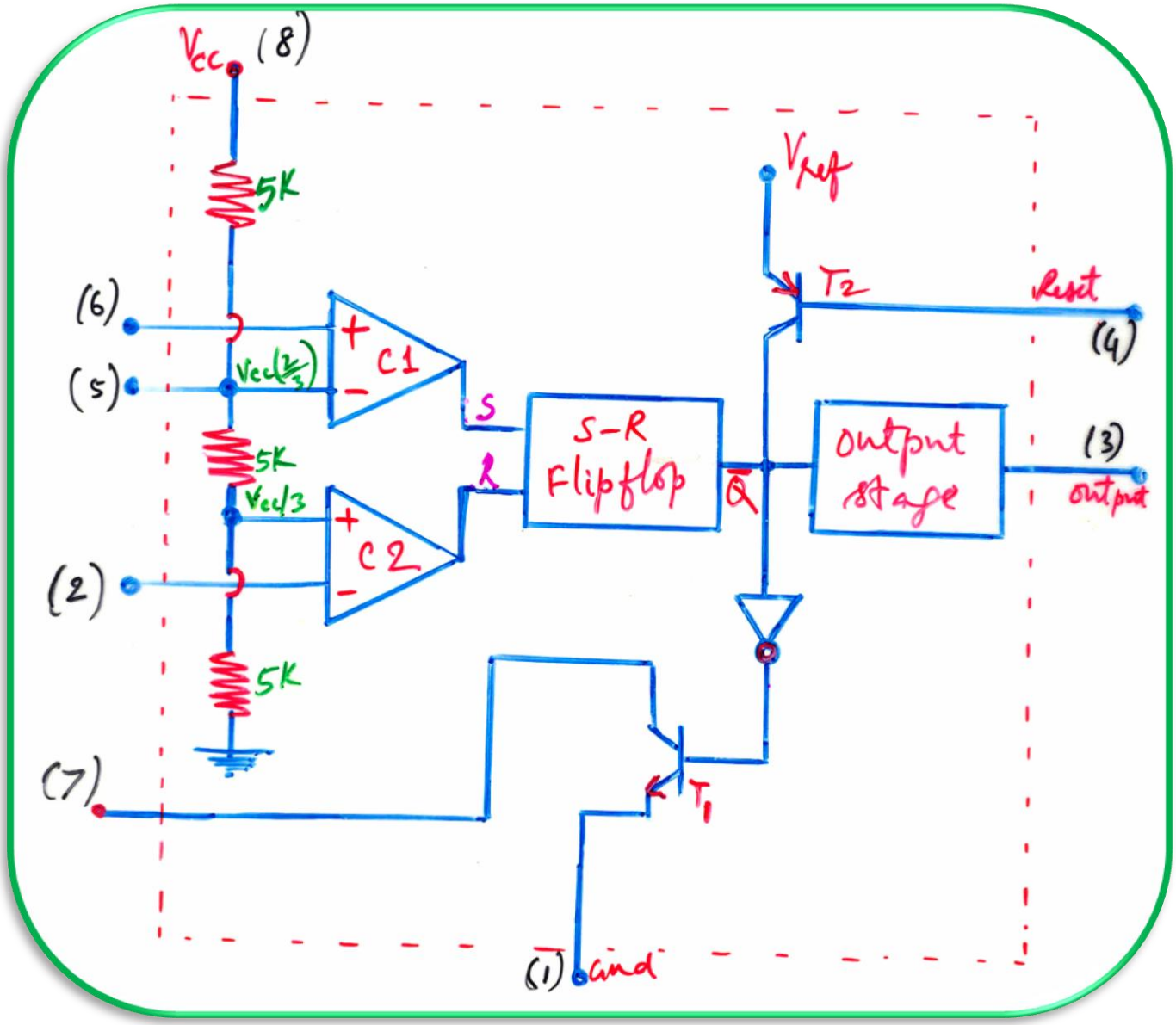


Salient features of timer IC 555

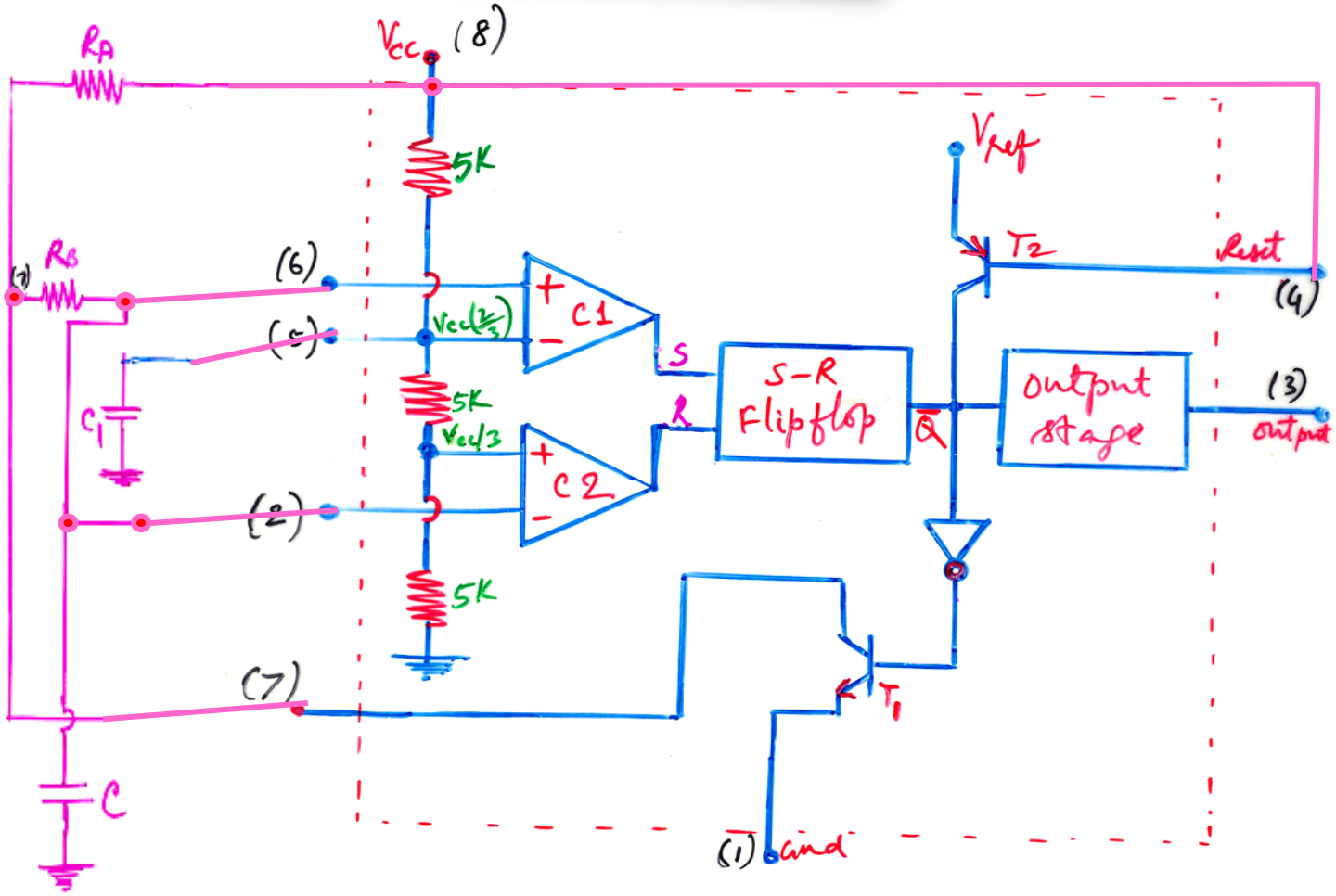
- Output can be taken either between 3 & 1 (pins) or between 8 and 3 (complementary output).
- can sink about 200 mA.
- Max frequency greater than 500 KHz
- Timing from μs to hours
- adjustable duty cycle
- TTL compatible

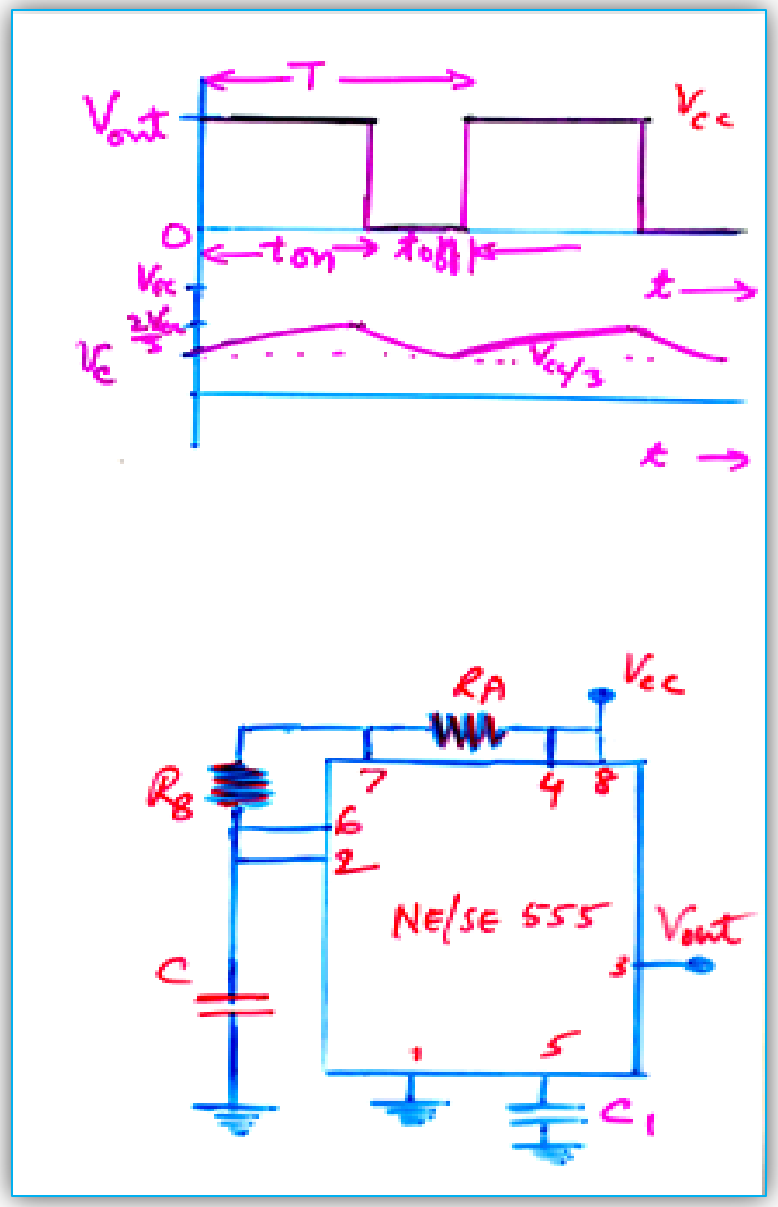
Applications:

- Precision timing, pulse generation, sequential timing, time delay generation, pulse width modulation, pulse position modulation, missing pulse detector

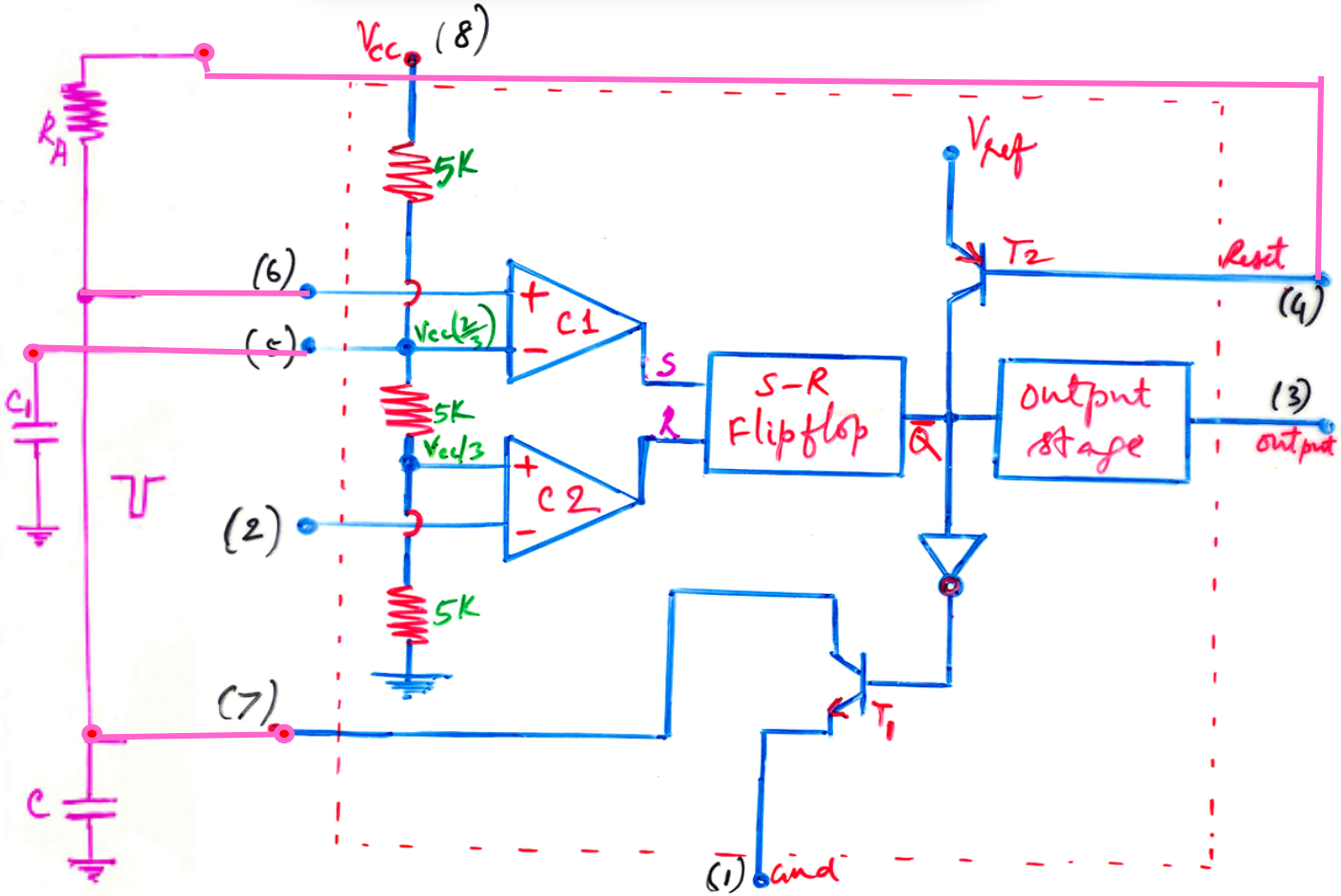

Vcc
(8)
5K
(6)
(5)
Vcc(2/3)
C1
5K
Vcc/3
C2
(2)
5K
(7)
S
R
S-R
Flipflop
Q
Vref
T2
Reset
(4)
output
stage
(3)
output
T1
(1)
gnd

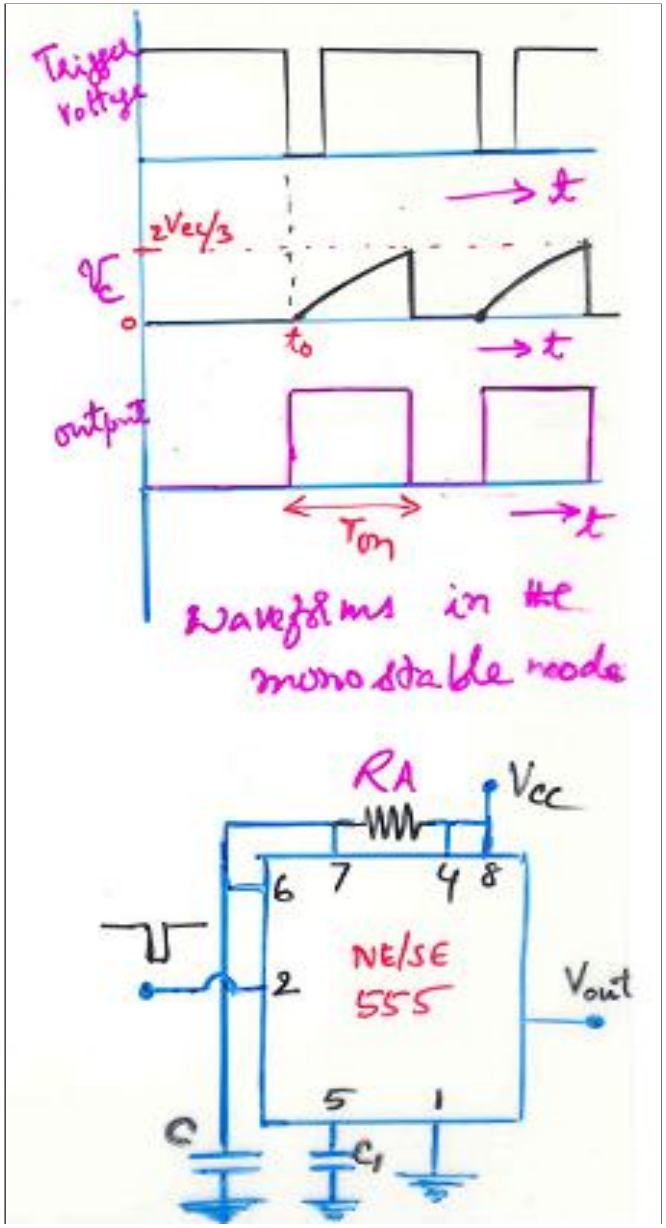
Astable mode of IC 555




T
V_{out}
V_{cc}
0
t_{on}
t_{off}
t
V_c
t
R_A
V_{cc}
R_B
7
4
8
6
2
NE/SE 555
V_{out}
3
C
1
5
C_1

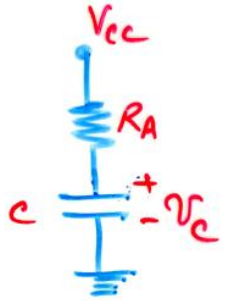
MONOSTABLE MODE OF 555 IC




Trigger voltage
t
2Vcc/3
V_c
0
t_0
t
output
T_{on}
t
Waveforms in the monostable mode
RA
Vcc
6
7
4
8
NE/SE 555
2
Vout
5
1
C
C_1

Analysis

Monostable mode:



At $t = 0$ s, $V_c(0) = 0$ and 'c' starts to charge via R_A towards V_{cc}. ∴ we can write

$$V_c(t) = V_{cc}\left(1 - e^{-\frac{t}{R_A C}}\right)$$

When $t = T_{on}$, $V_c(T_{on}) = \frac{2}{3}V_{cc}$.

ie, $$\frac{2}{3}V_{cc} = V_{cc}\left(1 - e^{-T_{on}/R_A C}\right)$$

or $$e^{-\frac{T_{on}}{R_A C}} = \left(1 - \frac{2}{3}\right) = \frac{1}{3}$$

or $$\ln(3) = \frac{T_{on}}{R_A C}$$

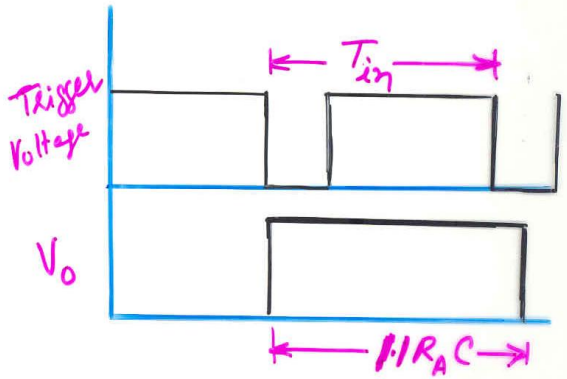
$$\Rightarrow T_{on} = \ln(3)\, R_A C$$

$$\boxed{T_{on} = 1.1\, R_A C}$$ on pulse time

Applications :

Monostable mode:

a) Frequency divider



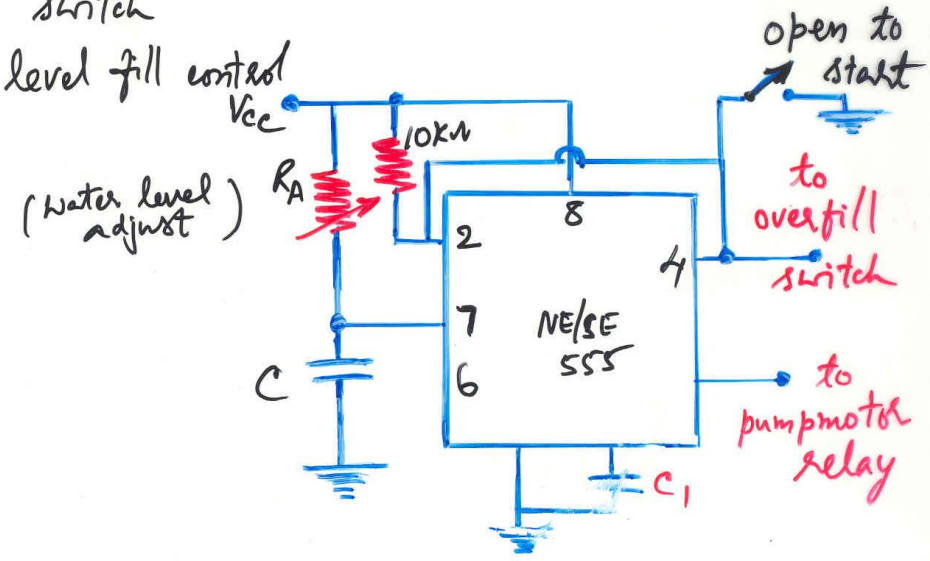
For a $\div 3$ operation,

$1.1R_AC > 2T_{in}$ and $< 3T_{in}$.

b) pulse stretcher (for visual or audio indication)

c) Touch switch

d) Water level fill control



2. Successive approximation ADC.

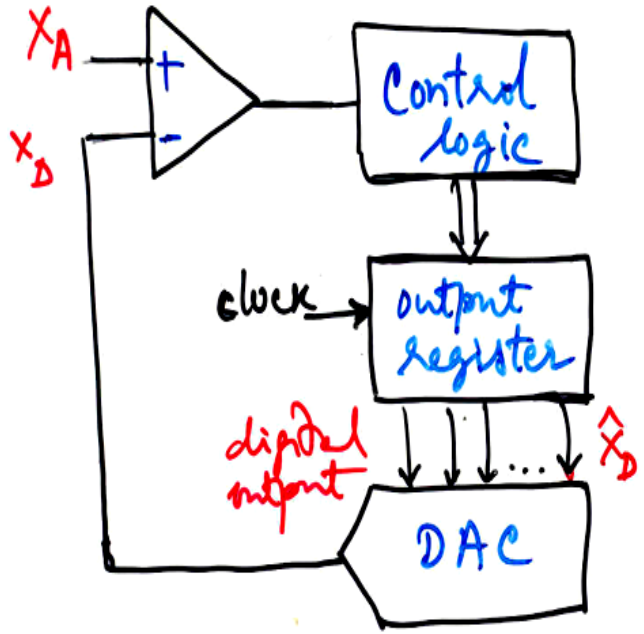


Fig 2. Block diagram of successive approximation ADC

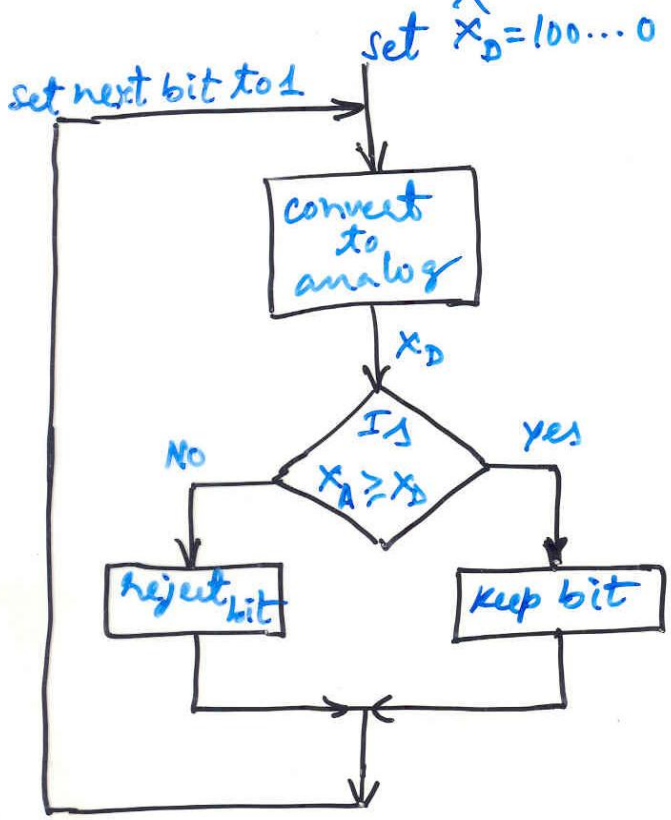
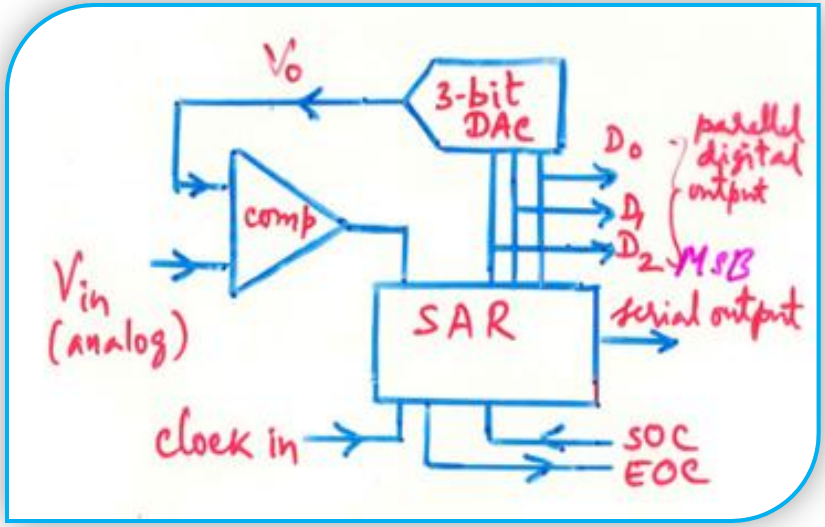


Fig 3. Flow chart for successive approximation ADC

→ No. of comparisons = n (constant)

where n = no. of bits in the ADC.



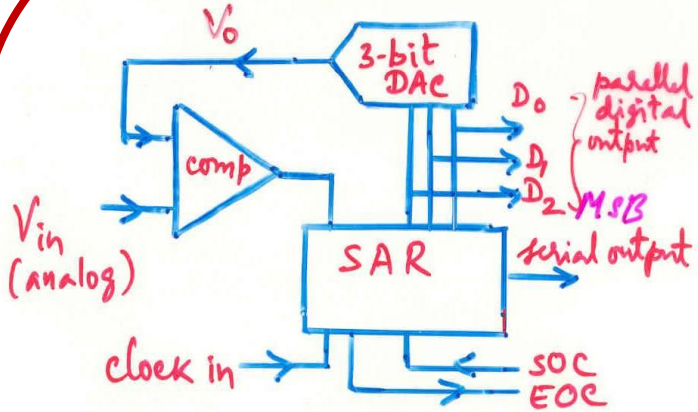
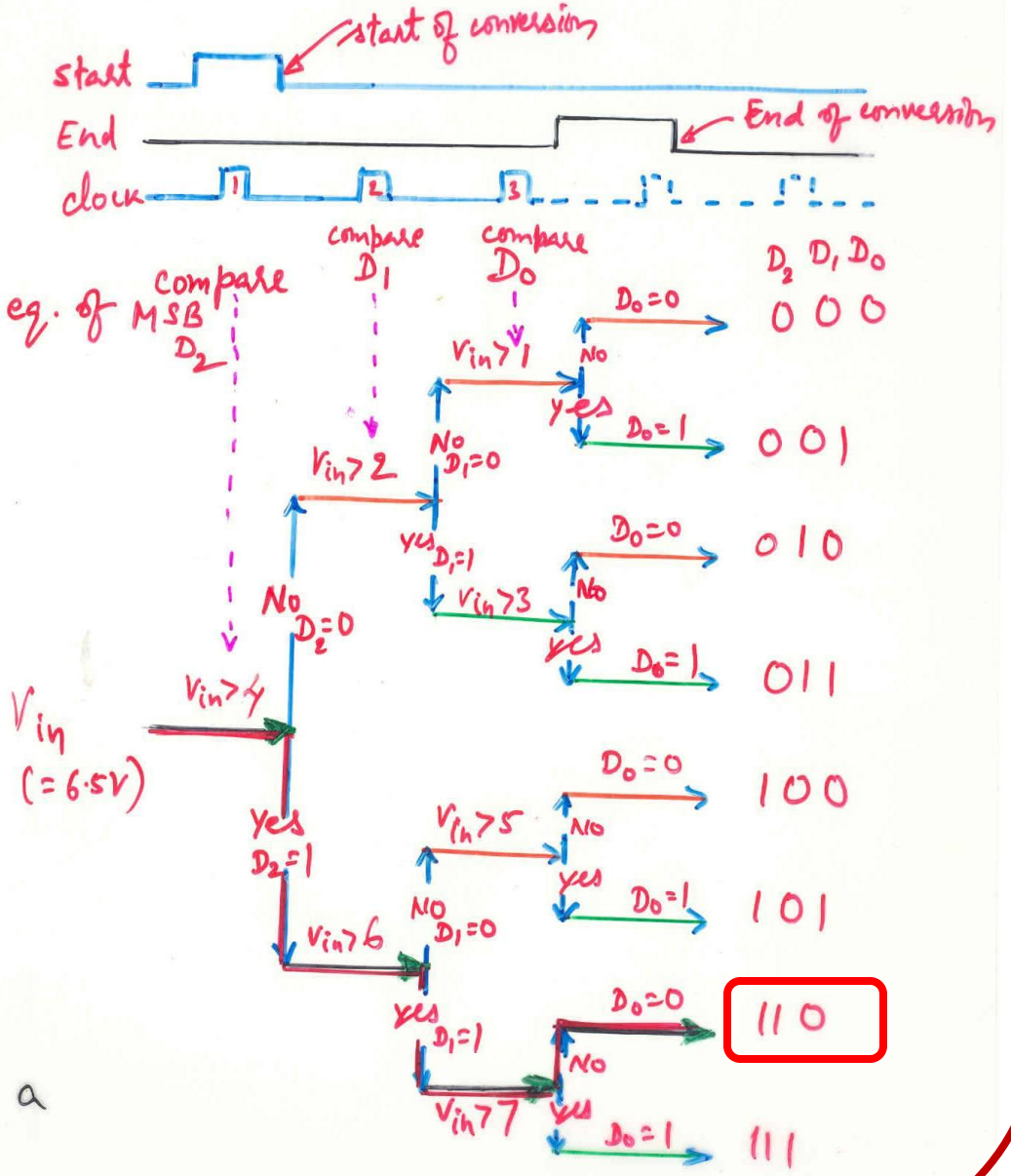


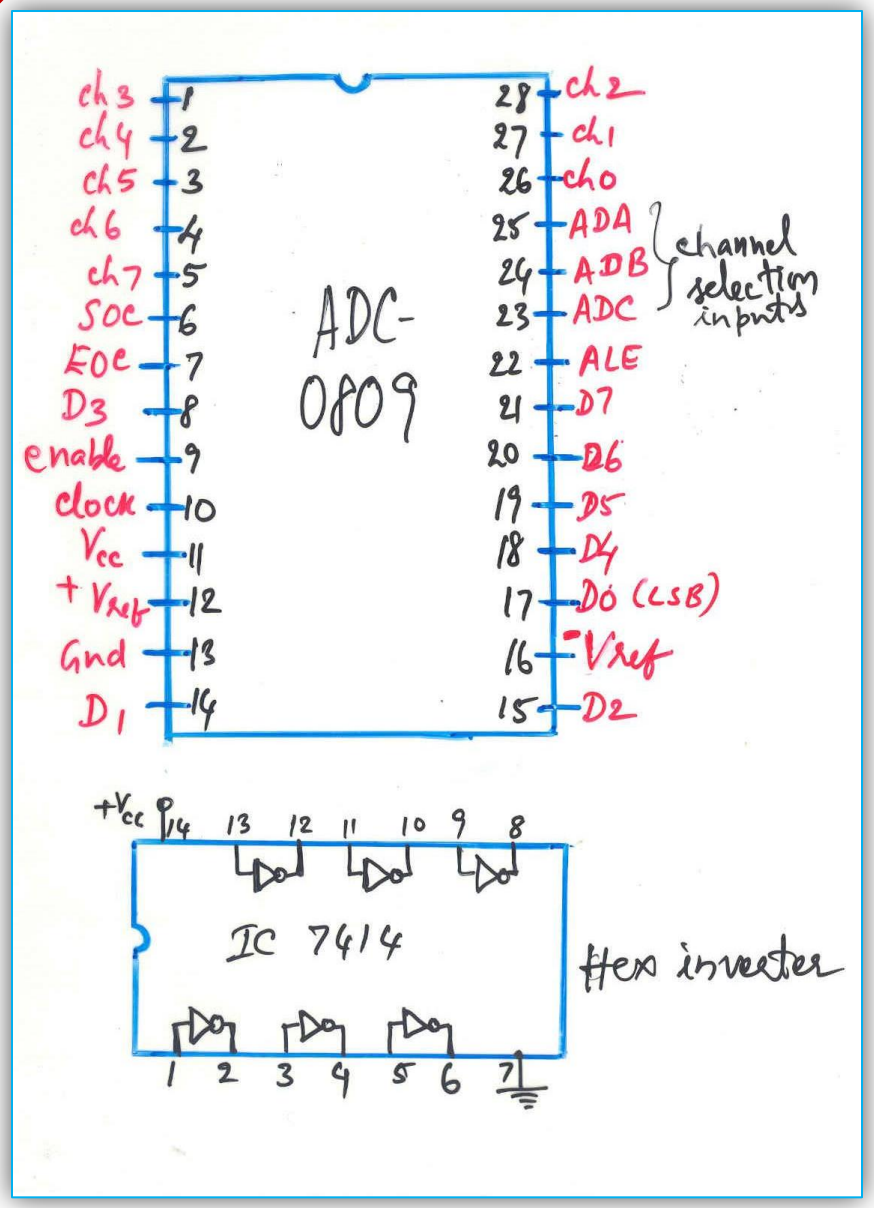
fig. 3-bit successive approximation ADC

Let 1 LSB weight = 1V

& V_{in} (analog) = 6.5V



Sequence of events in a 3-bit SA ADC

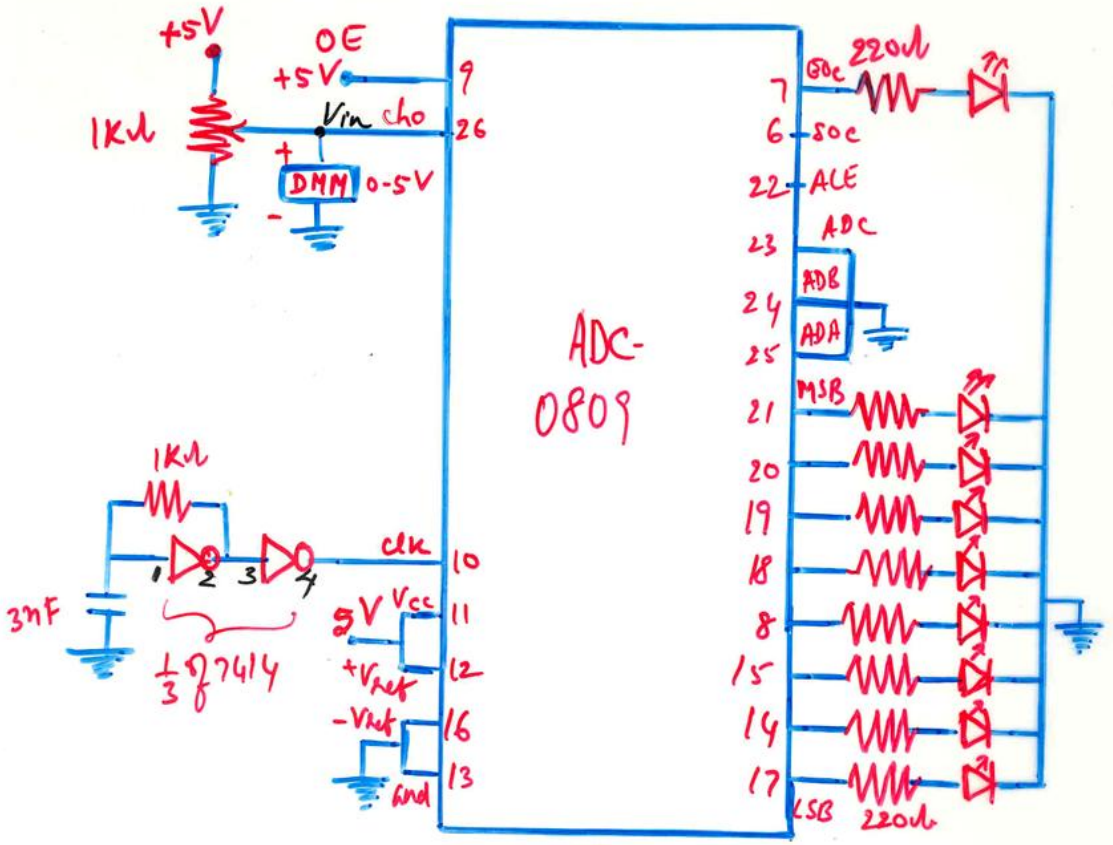


$$V_{out} = \frac{x}{255} \times {}^{+}V_{ref}$$ where

x = decimal count

$= D_0 2^0 + D_1 2^1 + \ldots + D_7 2^7$

where $D_0 - D_7$ are binary numbers



SOC : Start of conversion
EOC : End
ALE : Address Latch Enable
OE : Output Enable

f_c = 640 KHz (typically)

Conversion time : 100 μs (typically)

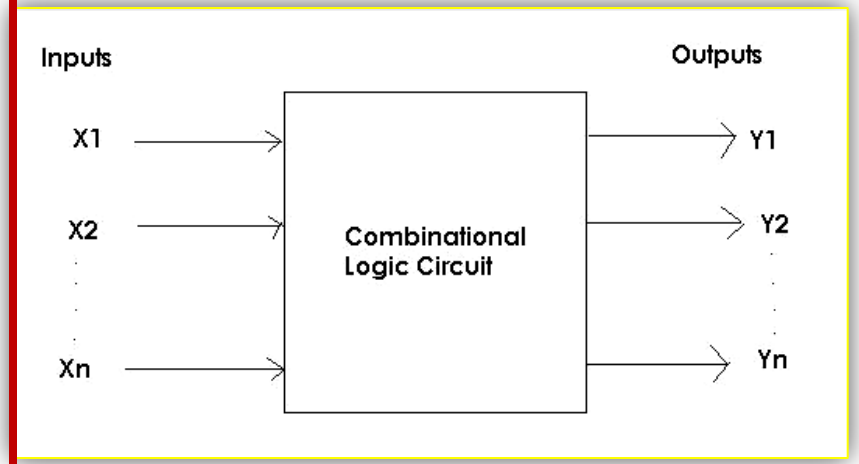
Selected channel	Address line		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

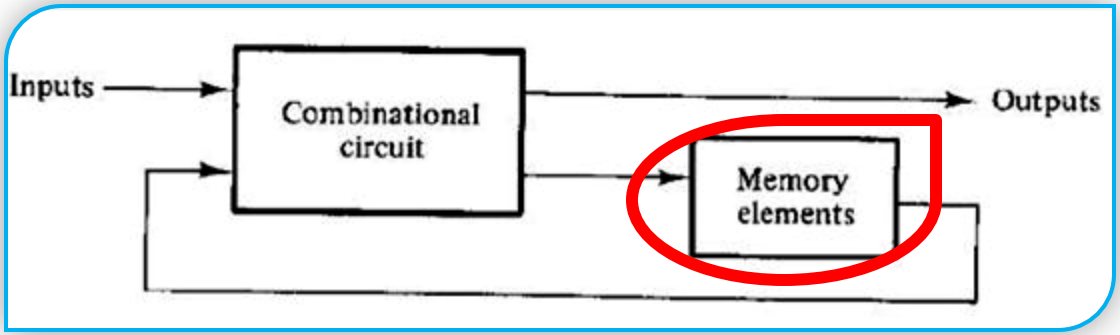
procedure for conversion

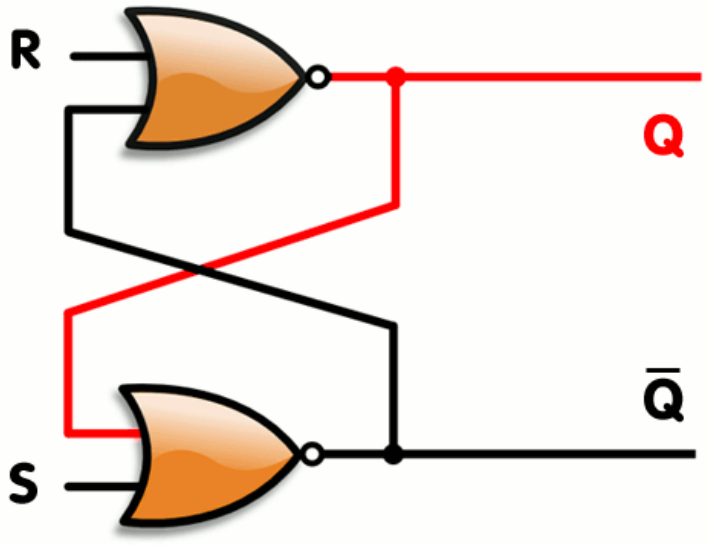
1. set ALE pin HIGH
2. set SOC HIGH and then LOW.
3. set ALE LOW.
4. EOC LED indicates the end of conversion process.

Basically the logic circuits are divided into

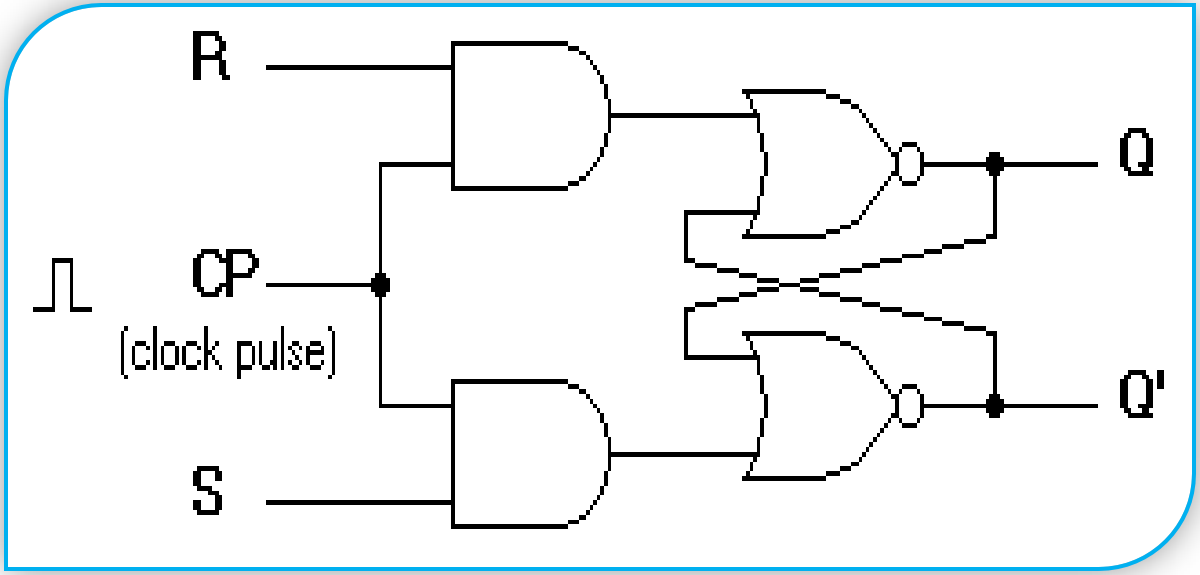
- Combinational logic circuits
- Sequential logic circuits

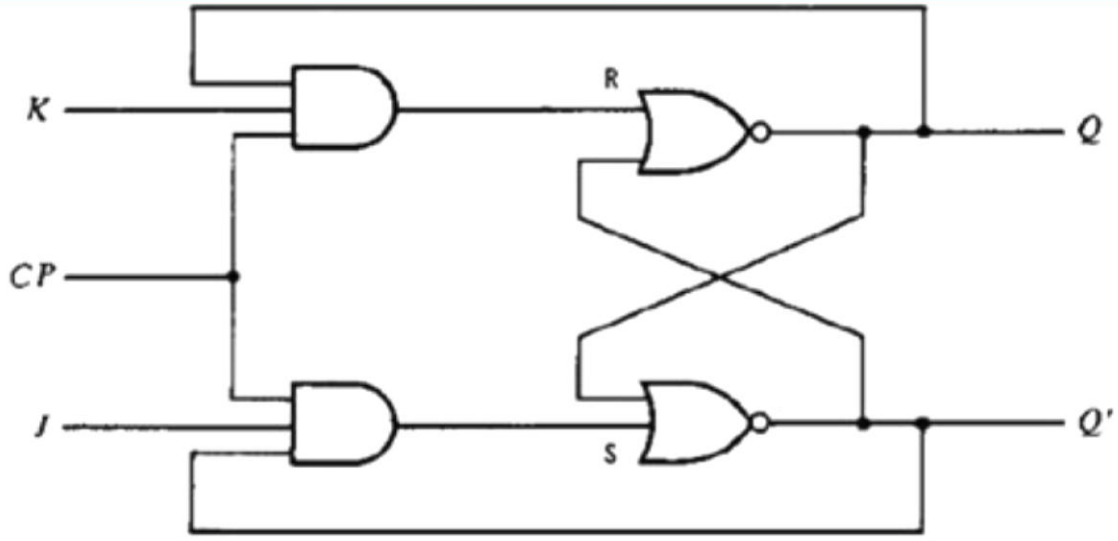






S	R	Q_{N+1}	Q_N
0	0	Q_N	Q_N
0	1	0	1
1	0	1	0
1	1	Not Used	

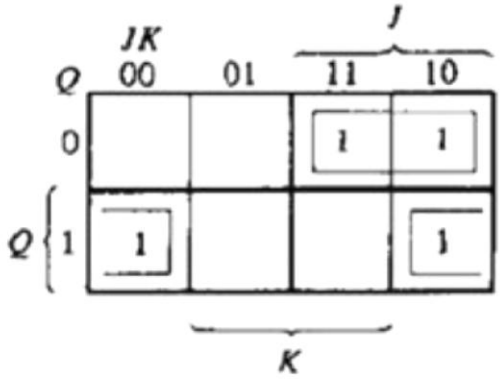




(a) Logic diagram

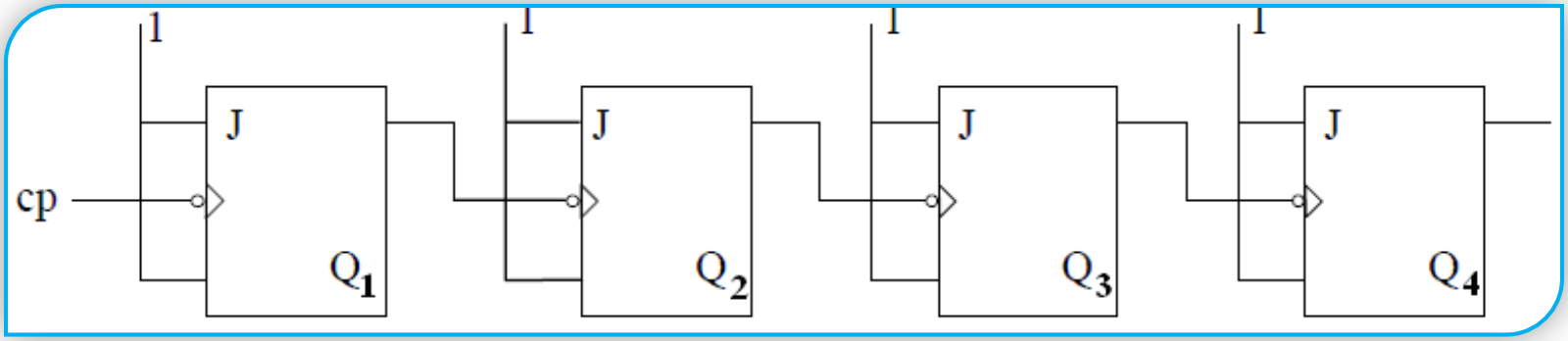
Q	J	K	Q(t + 1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

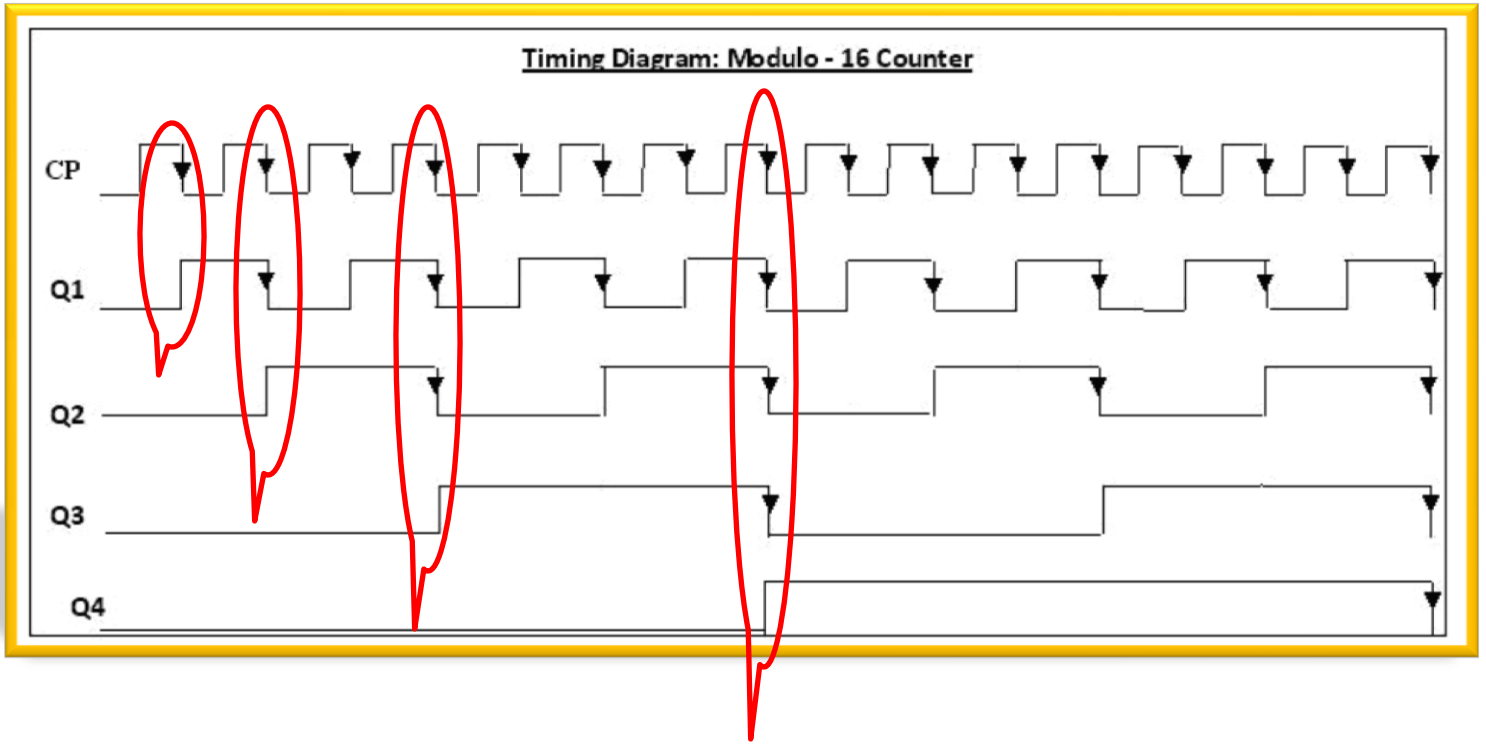
(b) Characteristic table



$Q(t+1) = JQ' + K'Q$

(c) Characteristic equation


1
J
cp
Q1
Q2
Q3
Q4


Timing Diagram: Modulo - 16 Counter
CP
Q1
Q2
Q3
Q4