EXPERIMENT #6 **COUNTERS**

I OBJECTIVES

The overall objective of this experiment is to familiarize students to design, build and test simple asynchronous counters using the TTL digital ICs.

II COMPONENTS AND INSTRUMENTATION

Student's concentration should be on the TTL gates and flip flops. As well, you need a variety of resistors and LED's. For measurement, use a two channel oscilloscope with probes and a waveform generator. List of commonly available digital ICs and internal circuits are given at the end. The pin diagram and internal circuit of IC 7476 which is dual J-K flip-flop, is given below.

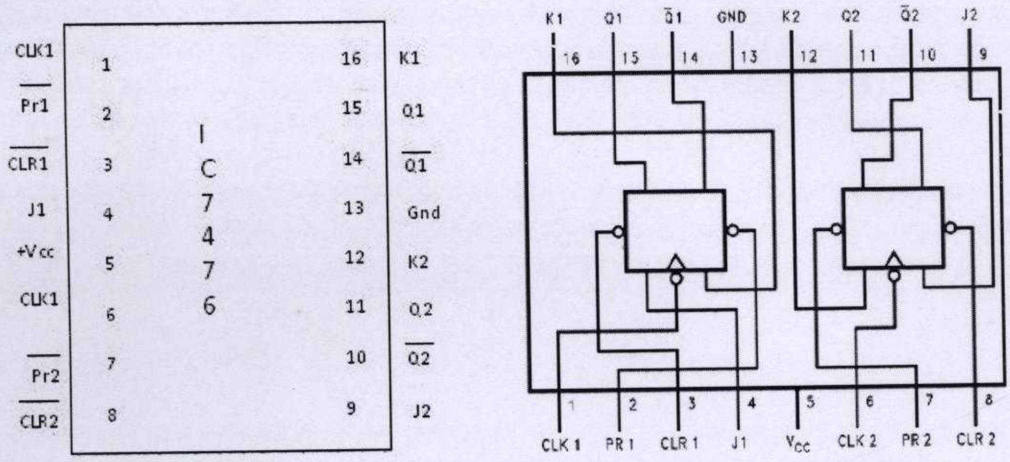


Fig. 6.1 Pin diagram and internal diagram of IC 7476 (dual J-K flip-flop)

III PREPARATION

P3.1 Connect the D input of the logic circuit shown in Fig. 6.2 to the pulse generator and set it at 1kHz. Connect the enable input (node E) to a logic high (+5V) through a 1k Ω resistor. Observe the output; obtain the data for the Truth-table 6.1.

Then change the enable input to logic low. Leave the enable low and place a momentary short to ground first on Q and then on Q'. What happens to the output?

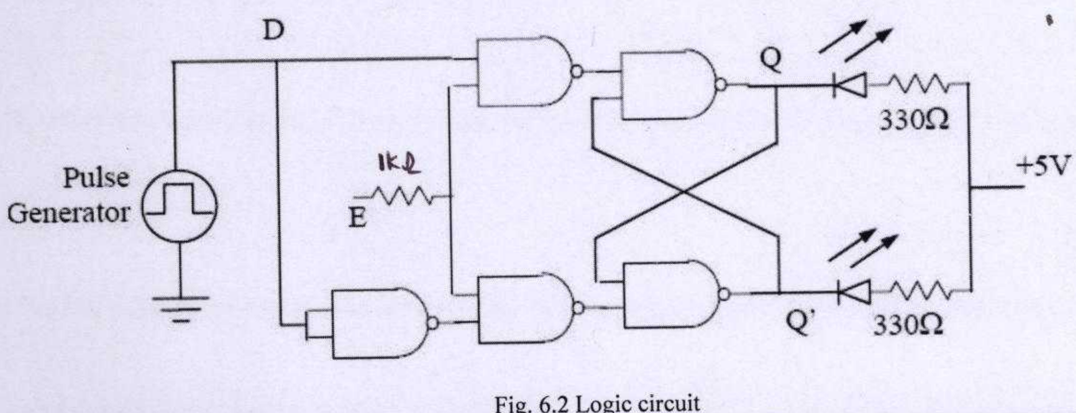


Fig. 6.2 Logic circuit

Table 6.1 Truth-table for Fig. 6.2

D	Q	Q'
0	0	1
1	1	0

→ LED Q glows

→ LED $\bar{Q}$ glows

When the enable (E) input is pulled down to logic low, then the present states of Q & $\bar{Q}$ are maintained.

i) when Q – grounded → LED Q glows, $\bar{Q}$ doesnt glow

ii) when $\bar{Q}$ – grounded → LED $\bar{Q}$ glows, Q doesn't glow.

P3.2 - Asynchronous counters (optional question)

Asynchronous counters are a series of flip-flops each clocked by the previous state, one after the other. Since all the stages of the counter are not clocked together, a ripple effect propagates as various flip-flops are clocked. For this reason they are called ripple counters. The modulus of a counter is the number of different output states the counter may take (i.e. mod 4 means the counter has four output states).

In the pre-lab construct a 4-bit asynchronous counter shown in Fig.6.3. (It is also called binary ripple counter). Use four generic JK flip-flops. Connect four Binary Probes to Q outputs. Connect all R and S inputs to Logic 1 and connect a switch to the CP (clock pulse) input.

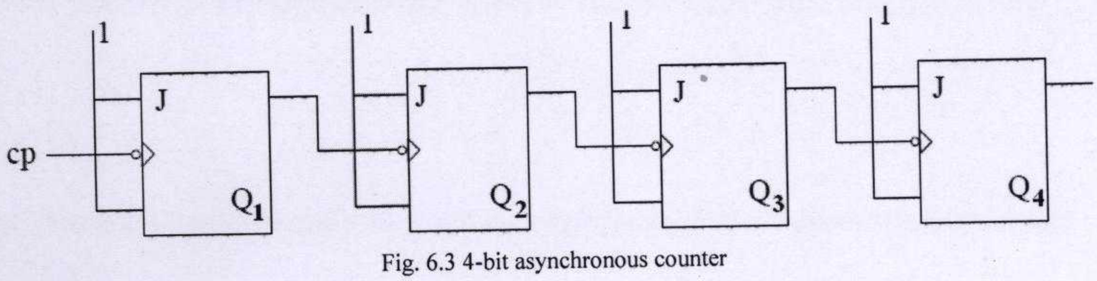


Fig. 6.3 4-bit asynchronous counter

Simulate the circuit using PSPICE or SEQUEL software and check that the output is as anticipated and print the waveforms and bring them to the lab.

IV EXPLORATIONS

E4.1

Use two 7476 ICs to implement the design of asynchronous counter to count up to 15 (as shown in Fig. 6.4). Connect the Q outputs of flip-flops to LEDs and connect all clear (CLR) and preset (PR) inputs to logic high.

Clock pulse - square wave with offset
(0 to 5V)

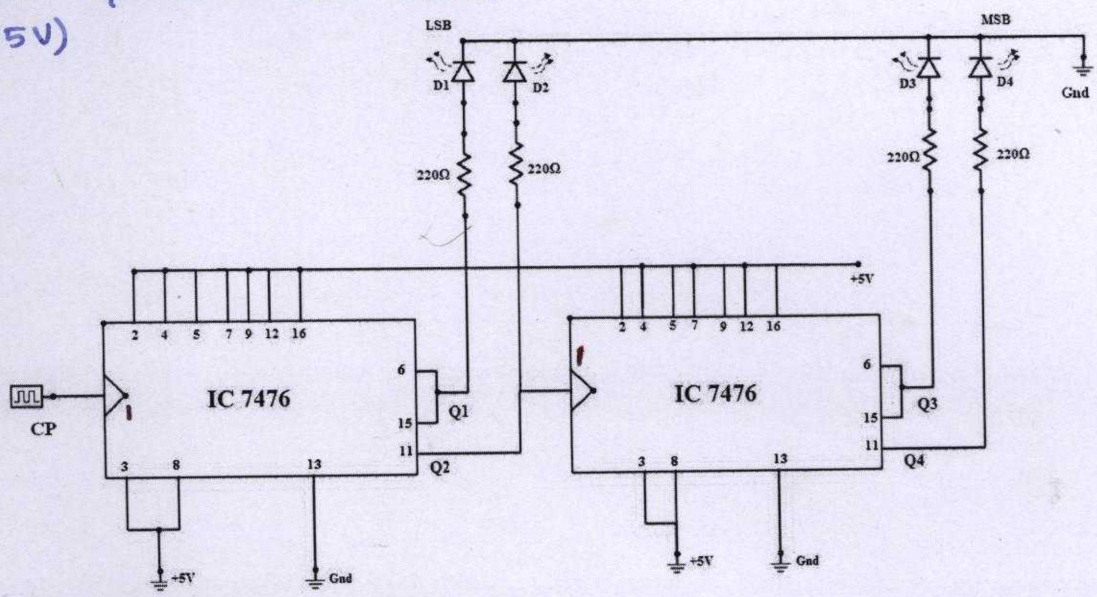


Fig. 6.4 Asynchronous counter using two 7476 ICs

Write down the count sequence in Table 6.2. Identify this count sequence (up or down). Comment on what happens at output after the 16th pulse at CP input. Timing sequence of input and output signals is shown in Fig.6.5.

Table 6.2 Count Sequence for the 4-bit ripple counter

Clock stage	Q_4	Q_3	Q_2	Q_1
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1
11	1	0	1	0
12	1	0	1	1
13	1	1	0	0
14	1	1	0	1
15	1	1	1	0
16	1	1	1	1

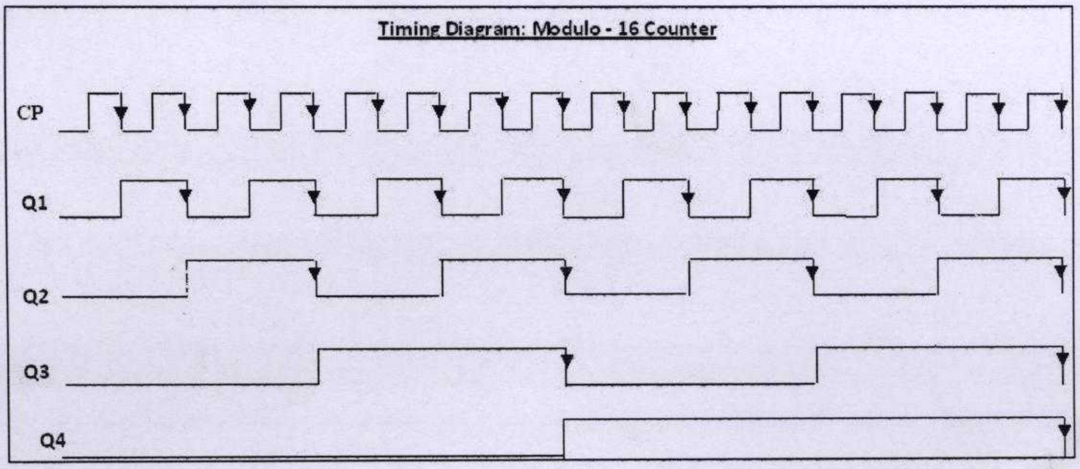
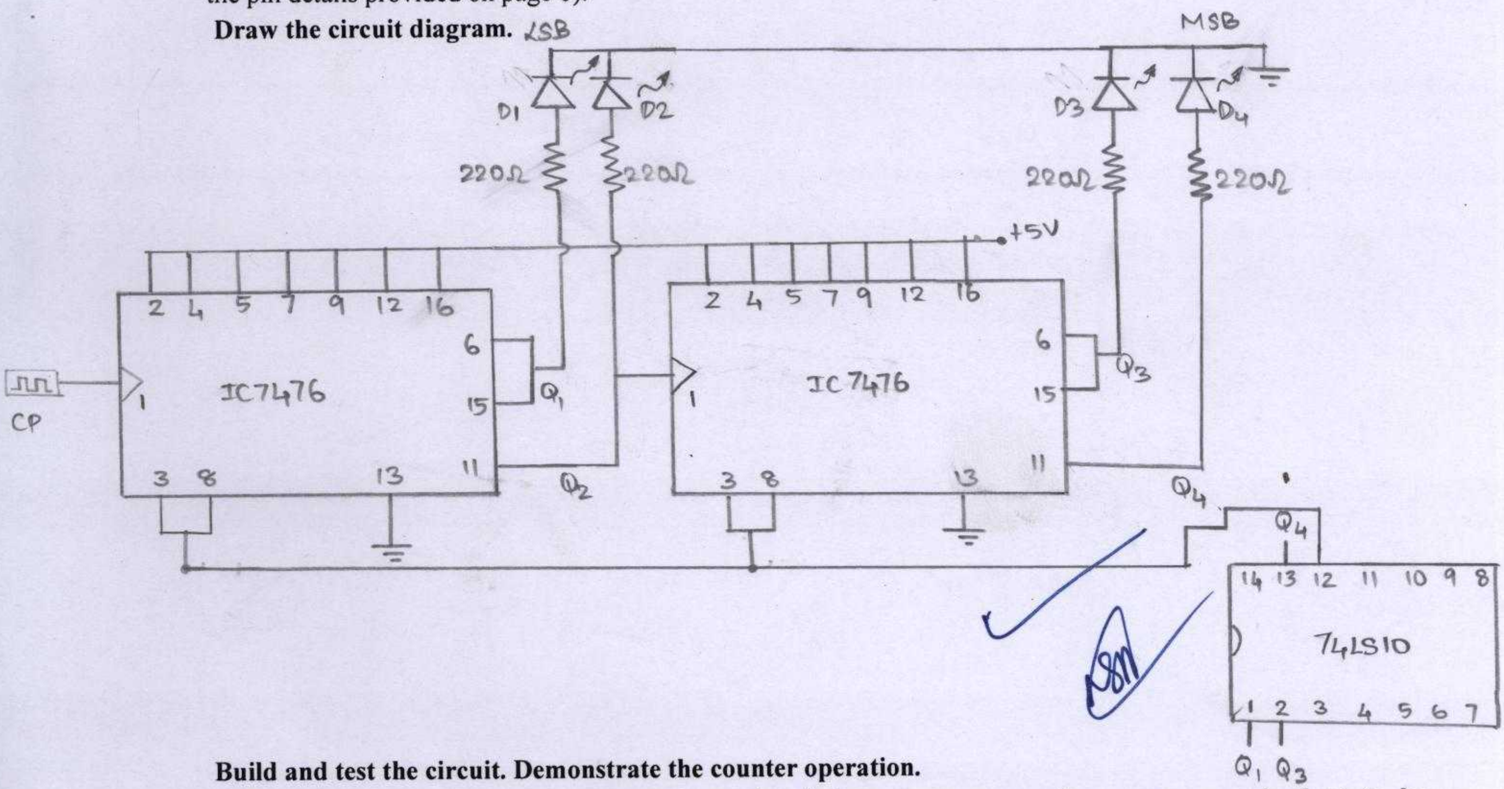


Fig.6.5 Timing sequence of input and output signals

E4.2 Mod-N counter

Design an asynchronous counter that goes through the count sequence ____13____.
How many flip-flops do you need? You may use any other gates for initiating 'Clear' operation. (choose from the pin details provided on page 6).

Draw the circuit diagram.



Build and test the circuit. Demonstrate the counter operation.
Tabulate the counting sequence and draw the timing sequence waveforms on a graph sheet to be submitted in report.

Table 6.3 Count Sequence for the 4-bit ripple counter

Clock stage	Q_4	Q_3	Q_2	Q_1
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1
11	1	0	1	0
12	1	0	1	1
13	1	1	0	0
14	0	0	0	0
15	0	0	0	1
16	0	0	1	0

- A ripple counter is built using a series of J-K flip flops, with the clock of each flip flop being fed by its preceding output.
- Any MOD-N counter can be implemented using the Mod-16 circuit, by using suitable combinations of NAND gates to reset the device at required intervals.
- Since each flip flop acts as a frequency divider, the use of two IC (7476) with 4 J-K flip flops would measure upto $2^4 = 16$ counts or clock cycles.

Integrated Circuits Lab	Credit	Maximum Marks
Preparation	4½	5
Experimentation	9½	10
Reporting	5	5
Total Marks	19	20

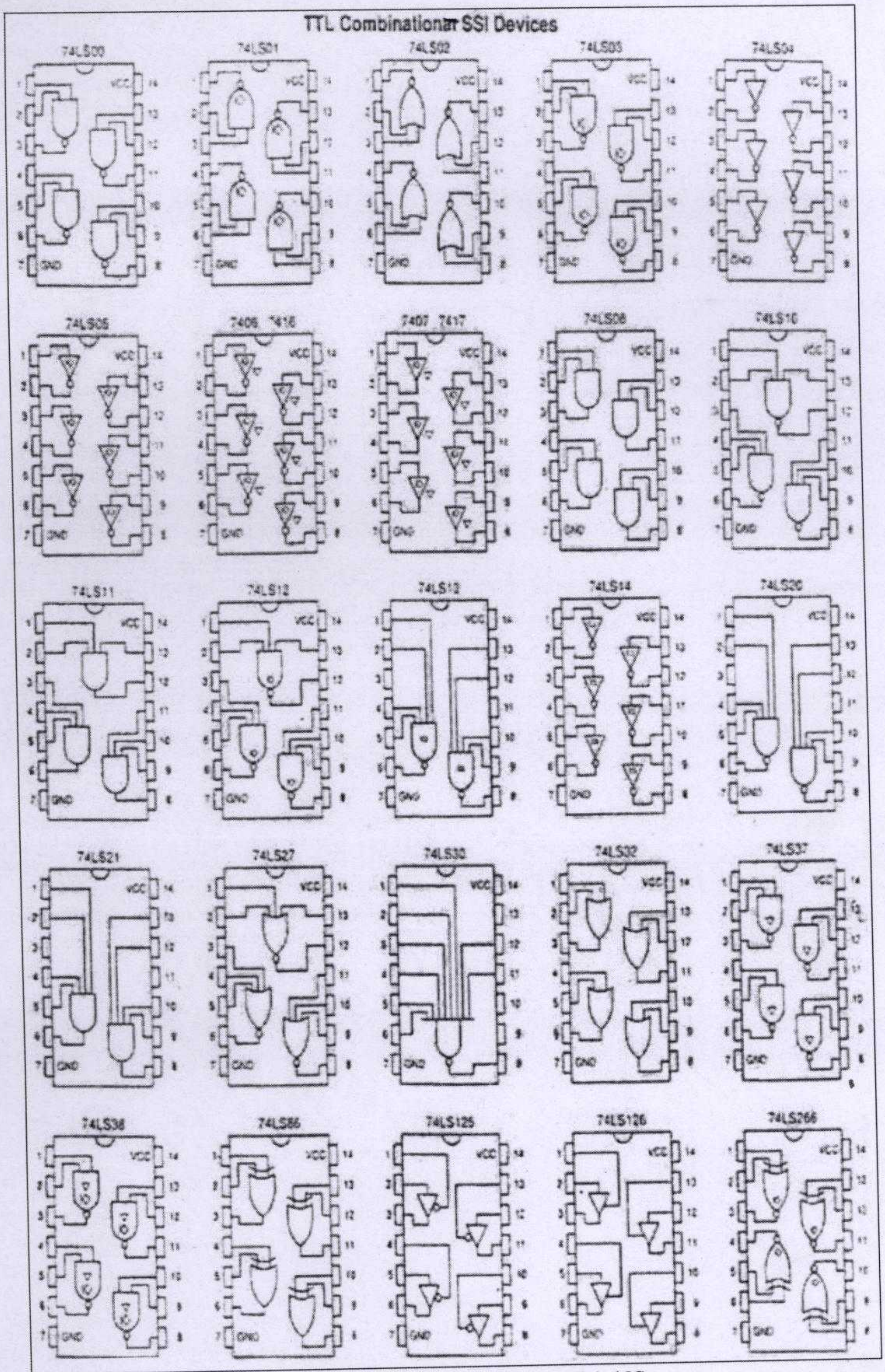


Fig.6.6 Pin details of common digital ICs

TIMING DIAGRAM - MODULO-13 COUNTER