

**Department of Electrical and
Electronics Engineering**



**National Institute of
Technology, Tiruchirappalli**

Microprocessors & Microcontrollers Lab Report

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(107108103)**

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- Dr. Moonlight S

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STD.: EEE SEC.: III YEAR - VI SEMESTER

ROLL No.: 107108103



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Average : $(19.86/20)$

DATE : 18.01.2011

ADDITION ON TWO 8-BIT NUMBERS

EXP. NO: 1a

USING THE 8085 MICROPROCESSOR

AIM:

To evaluate the sum of two 8-bit numbers using the 8085 microprocessor.

APPARATUS REQUIRED:

8085 microprocessor trainer kit

PROGRAM : (ASSEMBLY CODE)

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENT
8200H	21 4082	START:	LXI H, 8240H	; Load register pair immediate
8203H	7E		MOV A, M	; A \leftarrow (HL)
8204H	23		INX H	; Increment register pair
8205H	86		ADD M	; A \leftarrow A + (HL)
8206H	32 5082		STA 8250H	; Store accumulator direct
8209H	D2 1182		JNC HERE	; Jump on no carry.
820CH	3E 01		MVI A, 01H	; Move immediate
820EH	32 5182		STA 8251H	; Store accumulator direct
8211H	76	HERE:	HLT	; Halt

Input :

ADDRESS	DATA
8240H	A1 H
8241H	19 H

Verified -

Output :

ADDRESS	DATA
8250H	BA
8251H	00

(SUM)

(CARRY)

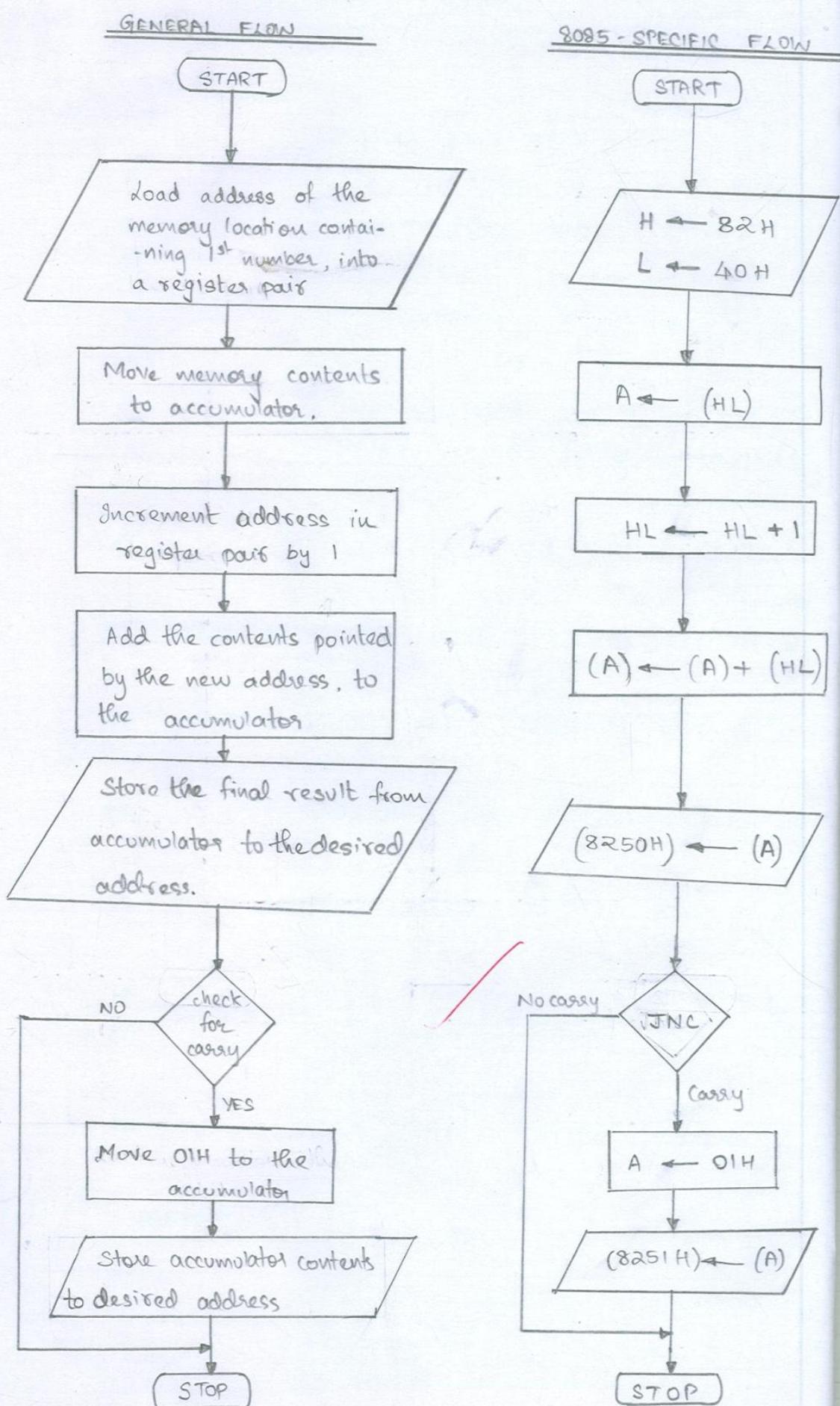
RESULT :

Hence the sum of the given two 8-bit numbers has been verified.

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 1011

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FLOWCHART:



DATE : 18.01.2011

EXP.-NO : 1b

SUBTRACTION OF TWO 8-BIT NUMBERSUSING THE 8085 MICROPROCESSOR

(3)

AIM :

To evaluate the difference of two 8-bit numbers using the 8085 microprocessor.

APPARATUS REQUIRED:

8085 microprocessor trainer kit

ASSEMBLY CODE :

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENT
8200H	21 40 82	START:	LXI H, 8240H	; Load register pair immediate
8203H	7E		MOV A, M	; A \leftarrow (HL)
8204H	23		INX H	; Increment register pair
8205H	96		SUB M	; A \leftarrow A - (HL)
8206H	32 50 82		STA 8250H	; Store accumulator direct
8209H	D2 11 82		JNC HERE	; Jump on no carry
820CH	3E 01		MVI A, 01H	; Move immediate
820EH	32 51 82		STA 8251H	; Store accumulator direct
8211H	76	HERE:	HLT	; Halt

Input :

ADDRESS	DATA
8240H	12H
8241H	ABH

Output :

ADDRESS	DATA
8250H	67
8251H	01

RESULT :

Hence two numbers are subtracted and the result is

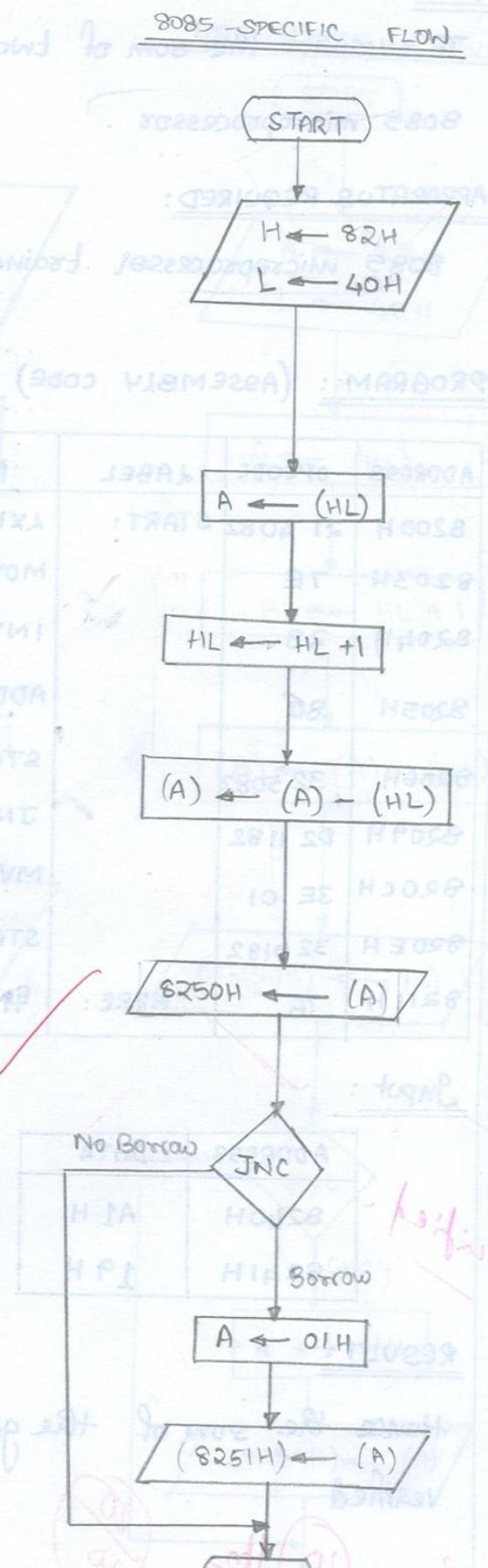
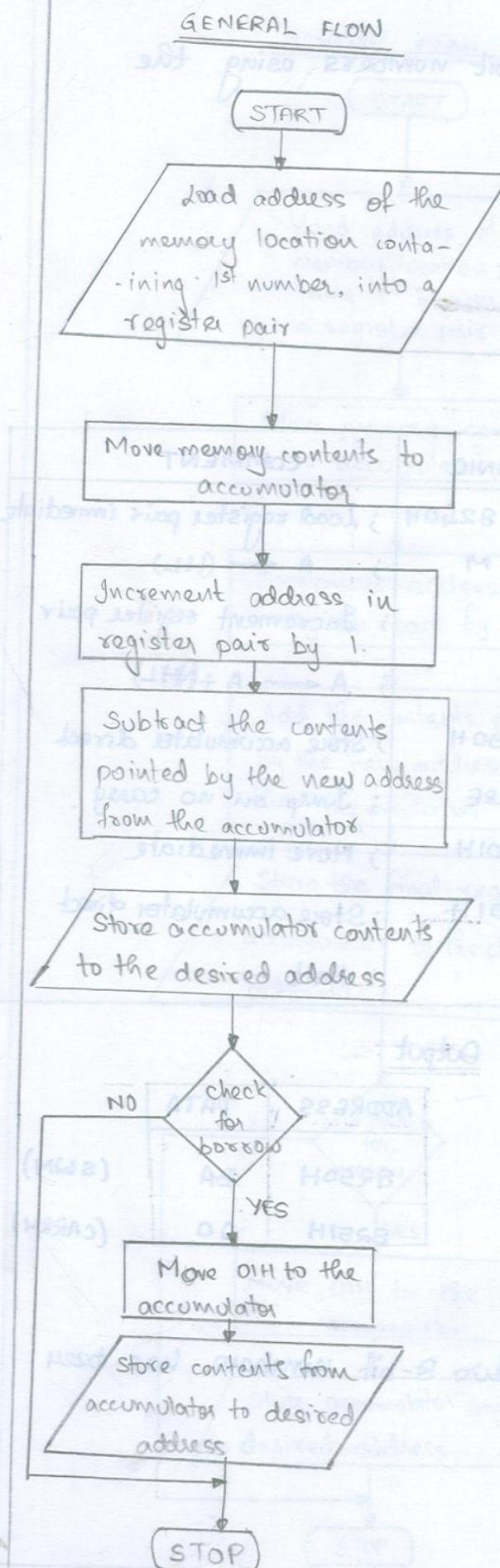
stored in 2's complement representation with a borrow indicator

Viva: 10
16
18
111
18

20
22

1m

FLOWCHART:



DATE: 25.01.2011

MULTIPLICATION OF TWO 8-BIT NUMBERS

EXP.NO. 1C

USING THE 8085 MICROPROCESSOR

(5)

AIM:

To evaluate the product of two 8-bit numbers using the 8085 microprocessor.

APPARATUS REQUIRED:

8085 microprocessor trainer kit.

ASSEMBLY CODE:

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENT
8200H	21 50 82	START:	LXI H, 8250H	; load HL pair immediate
8203H	AF		XRA A	; EX-OR A with A
8204H	46		MOV B, M	; B \leftarrow (M)
8205H	23		INX H	; HL \leftarrow HL+1
8206H	56		MOV D, M	; D \leftarrow (M)
8207H	0E 00		MVI C, 00H	; C \leftarrow 00H
8209H	80	L1:	ADD B	; A \leftarrow A+B
820AH	D2 0E 82		JNC L2	; jump on no carry
820DH	0C		INR C	; C \leftarrow C+1
820EH	15	L2:	DCR D	; D \leftarrow D-1
820FH	C2 09 82		JNZ L1	; jump on non zero
8212H	23		INX H	; HL \leftarrow HL+1
8213H	77		MOV M, A	; M \leftarrow A
8214H	23		INX H	; HL \leftarrow HL+1
8215H	71		MOV M, C	; M \leftarrow C
8216H	76		HLT	; Halt

Input:

ADDRESS	DATA
8250H	11
8251H	AF

Output:

ADDRESS	DATA
8252H	9F
8253H	0B

(product)
(carry)

seenopal

RESULT:

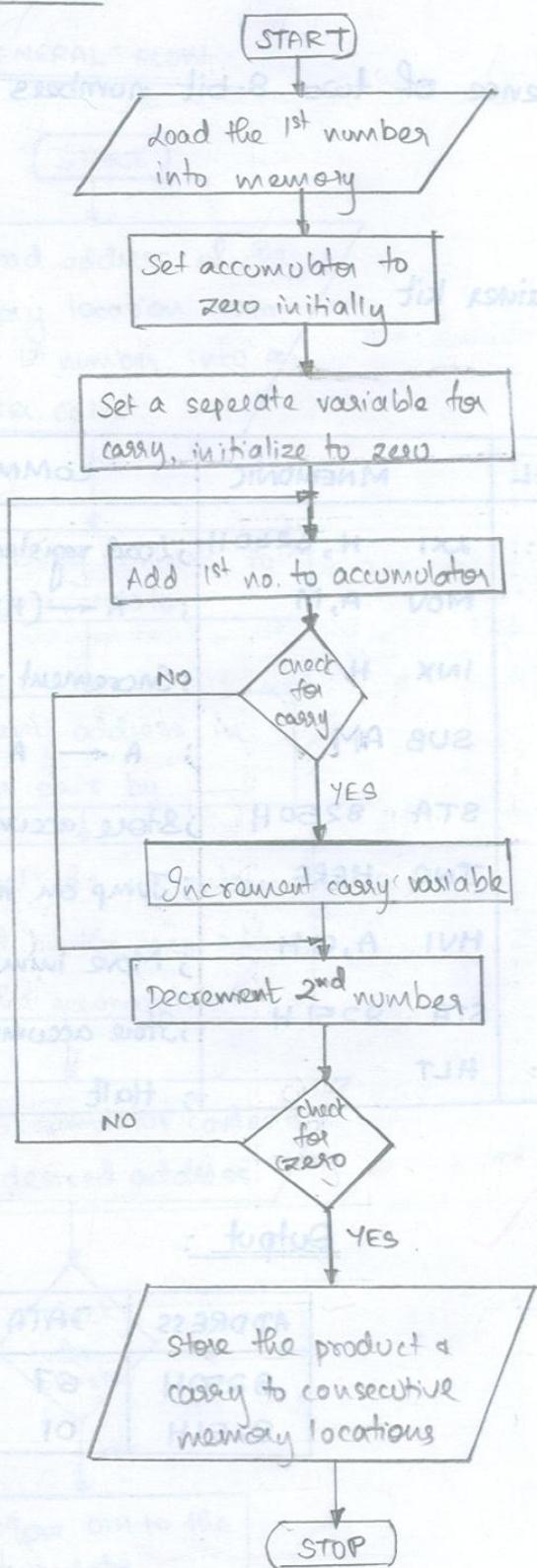
Hence the product of two 8-bit numbers is evaluated and the result is stored in the consecutive memory addresses.

25/1/2011

25/1/2011

25/1/2011

FLOW CHART:



AIM :

To evaluate the quotient and remainder upon dividing one number (8-bit) by another.

APPARATUS REQUIRED:

8085 microprocessor trainer kit.

ASSEMBLY CODE :

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENT
8200H	21 50 82	START:	LXI H, 8250H	; load HL pair immediate
8203H	7E		MOV A,M	; A ← (M)
8204H	23		INX H	; H ← HL+1
8205H	46		MOV B,M	; B ← (M)
8206H	OE 00		MVI C,00H	; C ← 00H
8208H	B8	L1:	CMP B	; compare A with B
8209H	DA 1182		JC L2	; jump on carry
820EH	90		SUB B	; A ← A-B
820DH	0C		INR C	; C ← C+1
820EH	C3 0882		JMP L1	; jump unconditional
8211H	23	L2:	INX H	; HL ← HL+1
8212H	71		MOV M,C	; M ← C
8213H	23		INX H	; HL ← HL+1
8214H	77		MOV M,A	; M ← A
8215H	76		HLT	; halt

Input :

ADDRESS	DATA
8250H	80
8251H	05

Output :

ADDRESS	DATA	
8252H	19	(quotient)
8253H	03	(remainder)

RESULT :

Hence the two numbers are divided and quotient and remainder are stored in consecutive memory locations

19
03

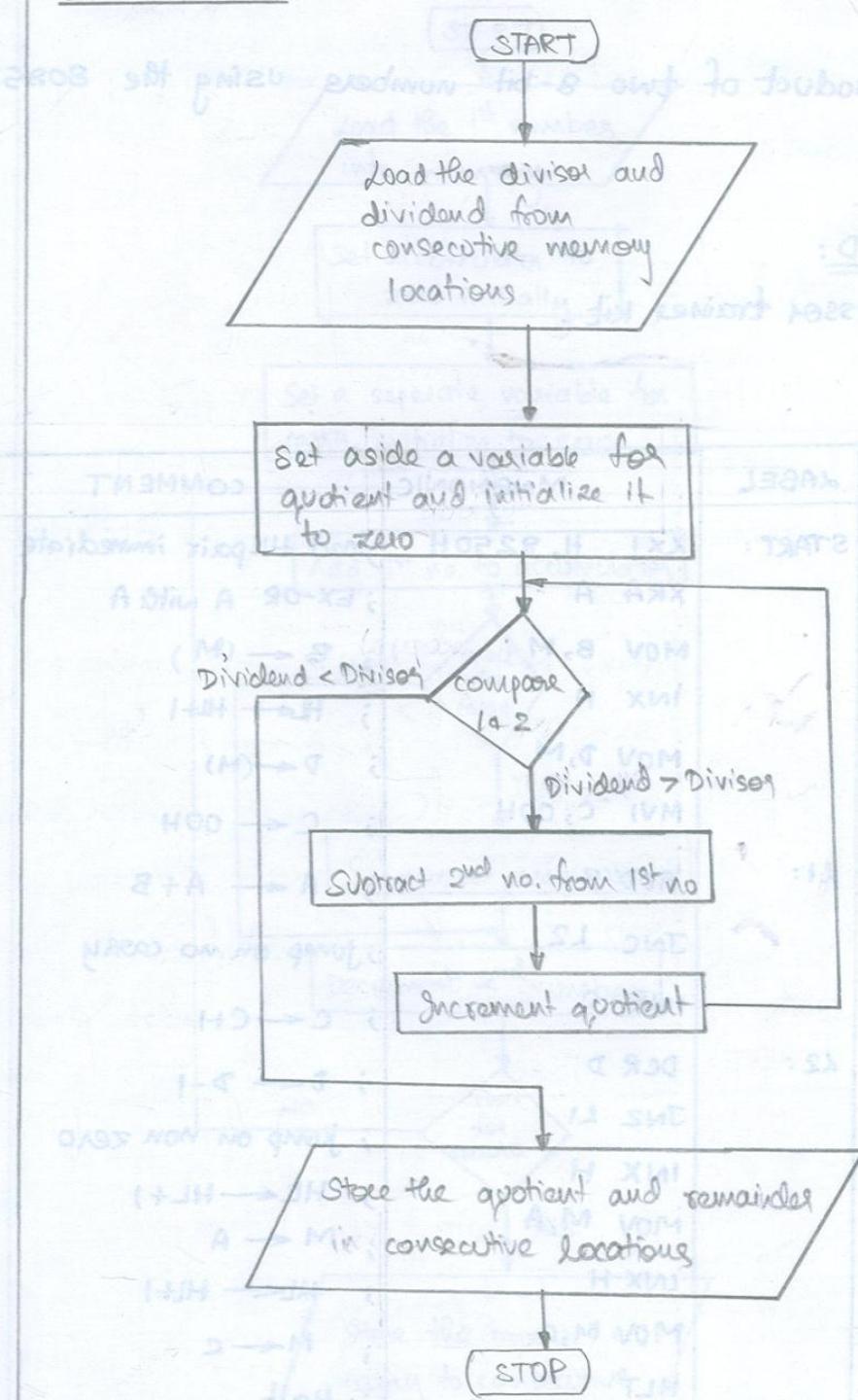


Vm

Verified
25/1/11

19
03

FLOWCHART:



EX-NO. 2A

AIM:

To evaluate the sum of two 16-bit numbers using the 8085 microprocessors

APPARATUS REQUIRED:

8085 microprocessor trainer kit

ASSEMBLY CODE :

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENTS
8200H	21 50 82	START:	LXI H, 8250H	; load HL pair immediate
8203H	46		MOV B, M	; B \leftarrow (M) [Higher order byte of data]
8204H	23		INX H	; HL \leftarrow HL + 1
8205H	7E		MOV A, M	; A \leftarrow (M) [lower order byte of data]
8206H	23		INX H	; HL \leftarrow HL + 1
8207H	56		MOV D, M	; D \leftarrow (M) [Higher Order byte of data]
8208H	23		INX H	; HL \leftarrow HL + 1
8209H	5E		MOV E, M	; E \leftarrow (M) [lower order byte of data]
820AH	DE 00		MVI C, 00H	; C \leftarrow 00H
820CH	83		ADD E	; A \leftarrow A + E
820DH	23		INX H	; HL \leftarrow HL + 1
820EH	77		MOV M, A	; M \leftarrow A
820FH	78		MOV A, B	; A \leftarrow B
8210H	8A		ADC D	; A \leftarrow A + D + CY
8211H	D2 15 82		JNC LI	; jump on no carry
8214H	0C		INR C	; C \leftarrow C + 1
8215H	23	LI:	INX H	; HL \leftarrow HL + 1
8216H	77		MOV M, A	; M \leftarrow A
8217H	23		INX H	; HL \leftarrow HL + 1
8218H	71		MOV M, C	; M \leftarrow C
8219H	76		HLT	; Halt

15
15

1/2 0/1 Input :

ADDRESS	DATA
8250H	F9
8251H	EF
8252H	D8
8253H	6B

Verified
1/2 0/1

Output :

ADDRESS	DATA	
8254H	5A	(lower order)
8255H	D2	(higher order)
8256H	01	(carry)

20
20

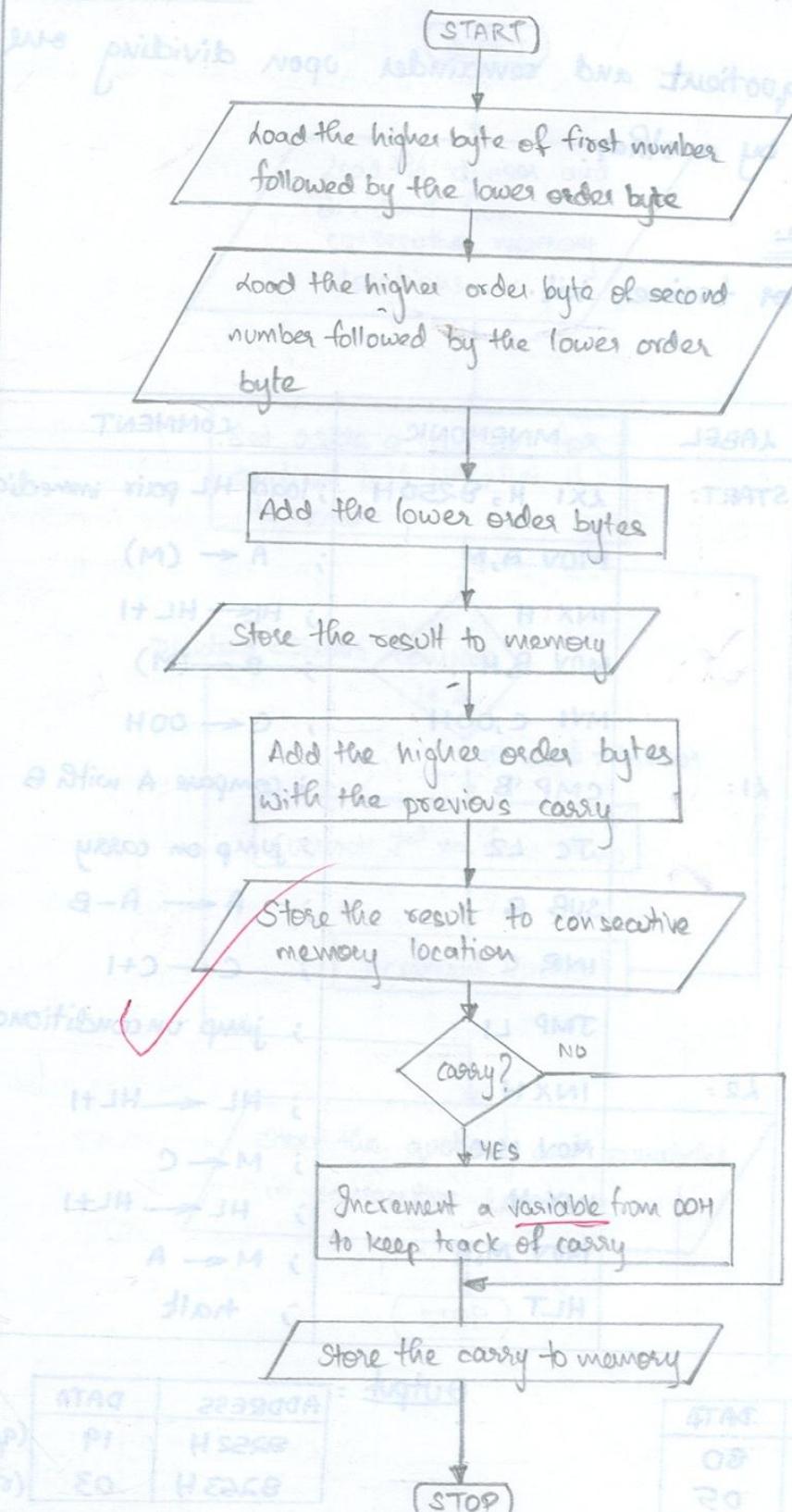
RESULT :

Thus the sum of two given 16 bit numbers has been evaluated

and the result is stored along with the carry.

1/2 0/1
0/1

FLOWCHART:



DATE: 01.02.2011

SUBTRACTION OF TWO 16-BIT NUMBERS

(11)

EX-N0. 2b

USING THE 8085 MICROPROCESSOR

AIM :

To evaluate the difference of two 16 bit numbers using the 8085 microprocessor.

APPARATUS REQUIRED :

8085 microprocessor trainer kit

ASSEMBLY CODE :

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENTS
8200H	21 50 82	START:	LDI H, 8250H	; load HL pair immediate
8203H	46		MOV B, M	; B \leftarrow (M)
8204H	23		INX H	; HL \leftarrow HL + 1
8205H	7E		MOV A, M	; A \leftarrow (M)
8206H	23		INX H	; HL \leftarrow HL + 1
8207H	56		MOV D, M	; D \leftarrow (M)
8208H	23		INX H	; HL \leftarrow HL + 1
8209H	5E		MOV E, M	; E \leftarrow (M)
820AH	0E 00		MVI C, 00H	; C \leftarrow 00H
820CH	93		SUB E	; A \leftarrow A - E
820DH	23		INX H	; HL \leftarrow HL + 1
820EH	77		MOV M, A	; M \leftarrow A
820FH	78		MOV A, B	; A \leftarrow B
8210H	9A		SBB D	; A \leftarrow A - D - Borrow
8211H	D2 1582		JNC L1	; jump on no carry
8214H	0C		INR C	; C \leftarrow C + 1
8215H	23	L1:	INX H	; HL \leftarrow HL + 1
8216H	77		MOV M, A	; M \leftarrow A
8217H	23		INX H	; HL \leftarrow HL + 1
8218H	71		MOV N, C	; M \leftarrow C
8219H	76		HLT	; Halt

Input :

ADDRESS	DATA
8250H	DB
8251H	6B
8252H	E7
8253H	8A

15
15
Verified
Jan 01/02

Output :

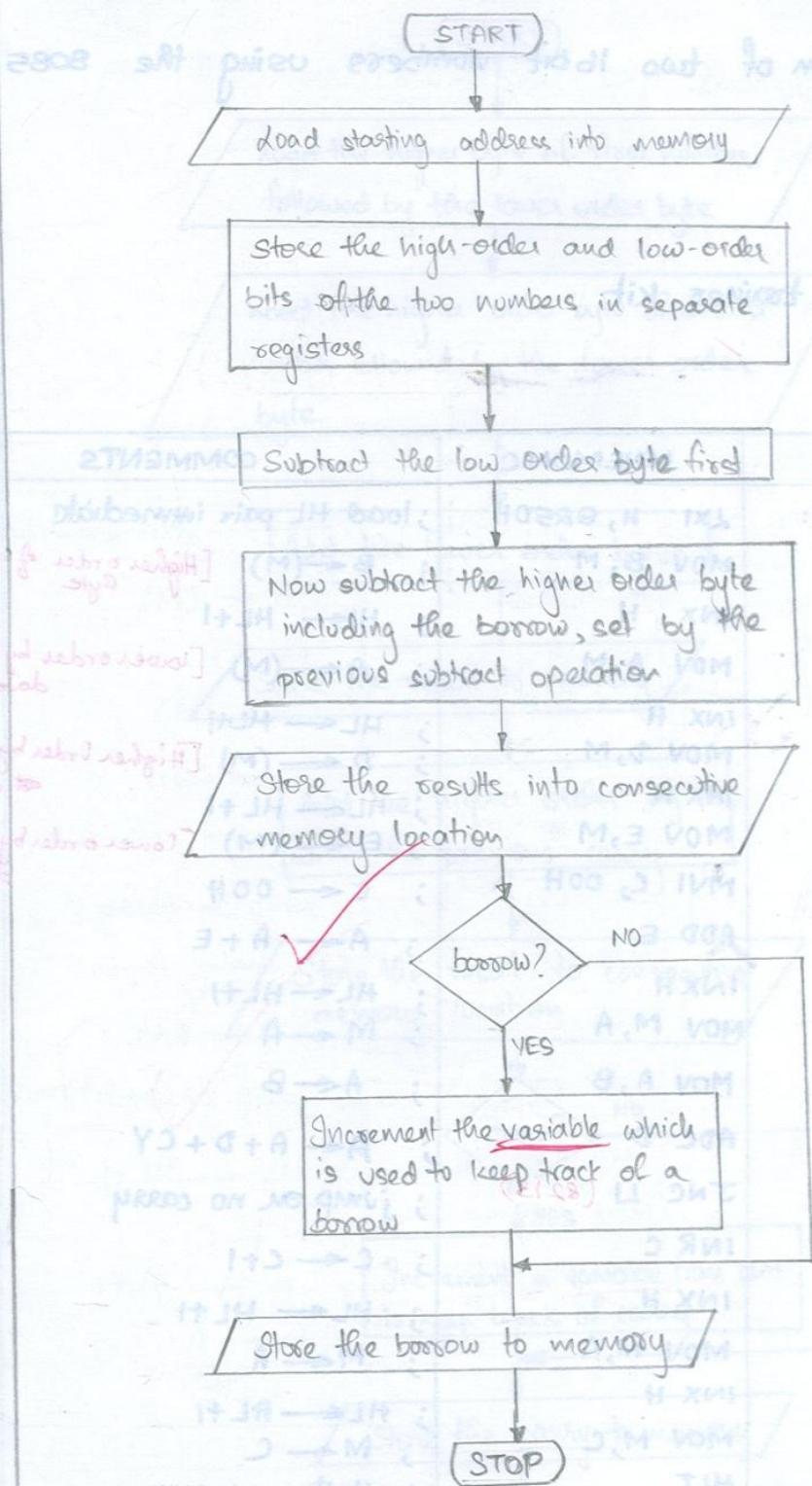
ADDRESS	DATA	
8254H	E1	(lower, older)
8255H	F0	(higher, older)
8256H	01	(borrow)

RESULT :

Thus the difference of two 16 bit numbers is calculated and the result is stored in its 2's complement representation.

15
15
15
of 20

FLOWCHART:



AT&R	ADDRESS	DATA
A0	8552H	8552H
B2	8525H	8525H
10	8525H	8525H

AT&R	ADDRESS	DATA
A7	8552H	8552H
B3	8525H	8525H
18	8525H	8525H
2E	8525H	8525H

EX-NO.3

OPCODE LABEL MNEMONIC COMMENT

AIM :

To evaluate the sum of two BCD numbers using the 8085 microprocessor.

APPARATUS REQUIRED:

8085 microprocessor trainer kit.

ASSEMBLY CODE :

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENTS
8200H	16 00	START:	MVI D,00H	; D ← 00H
8202H	1E 00		MVI E,00H	; E ← 00H
8204H	21 A0 82		XLH H,820AH	; HL ← 820AH
8207H	7E		MOV A,M	; A ← (M)
8208H	E6 0F		ANI OFH	; and immediate with A
8209H	4F		MOV C,A	; C ← A
820BH	23		INX H	; HL ← HL + 1
820CH	7E		MOV A,M	; A ← (M)
820DH	E6 0F		ANI OFH	; and immediate with A
820FH	81		ADD C	; A ← A + C
8210H	FF 0A		CPI OA H	; compare immediate with A
8212H	DA 17 82		JCL L1	; jump on carry
8215H	1E 01		MVI E,01H INRE	; E ← 01H
8217H	7E	L1:	MOV A,M	; A ← (M)
8218H	2B		DCX H	; HL ← HL - 1
8219H	86		ADD M	; A ← A + M
821AH	47		MOV B,A	; B ← A
821BH	D2 33 82		JNC L2	; jump on no carry
821EH	16 01		MVI D,01H INRD	; D ← (01)H
8220H	7B		MOV A,E	; A ← E
8221H	3D		DCR A	; A ← A - 1
8222H	C2 22C82		JNZ L4	; jump on nonzero
8225H	78		MOV A,B	; A ← B
8226H	C6 66		ADI 66H	; A ← A + (66)H
8228H	47		MOV B,A	; B ← A
8229H	C3 5082		JMP A3	; jump
822CH	78	L4:	MOV A,B	; A ← B

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENT
822DH	C6 60		ADI 60H	; A \leftarrow A + (60) _H
822FH	47		MOV B,A	; B \leftarrow A
8230H	C3 5082		JMP L3	; unconditional jump
8233H	7B	L2:	MOV A,E	; A \leftarrow E
8234H	3D		DCR A	; A \leftarrow A - 1
8235H	C2 4082		JNZ L5	; jump on non zero
8238H	78		MOV A,B	; A \leftarrow B
8239H	C6 06		ADI 06H	; A \leftarrow A + (06) _H
823BH	D2 3F82		JNC NC1	; jump on no carry
823EH	14		INR D	; D \leftarrow D + 1
823FH	47	NC1:	MOV B,A	; B \leftarrow A
8240H	78	L5 :	MOV A,B	; A \leftarrow B
8241H	E6 F0		ANI FOH	; A \leftarrow A \wedge (FO) _H
8243H	FE AO		CPI AOH	; compare immediate with Acc.
8245H	DA 5082		JC L3	; jump on carry.
8248H	78		MOV A,B	; A \leftarrow B
8249H	C6 60		ADI 60H	; A \leftarrow A + (60) _H
824BH	D2 4F82		JNC NC2	; jump on no carry
824EH	14		INR D	; D \leftarrow D + 1
824FH	47	NC2:	MOV B,A	; B \leftarrow A
8250H	23	L3 :	INX H	; HL \leftarrow HL + 1
8251H	23		INX H	; HL \leftarrow HL + 1
8252H	70		MOV M,B	; M \leftarrow B
8253H	23		INX H	; HL \leftarrow HL + 1
8254H	72		MOV M,D	; M \leftarrow D
8255H	76		HLT	; halt

Input

ADDRESS	DATA
82A0H	93
82A1H	97

Output

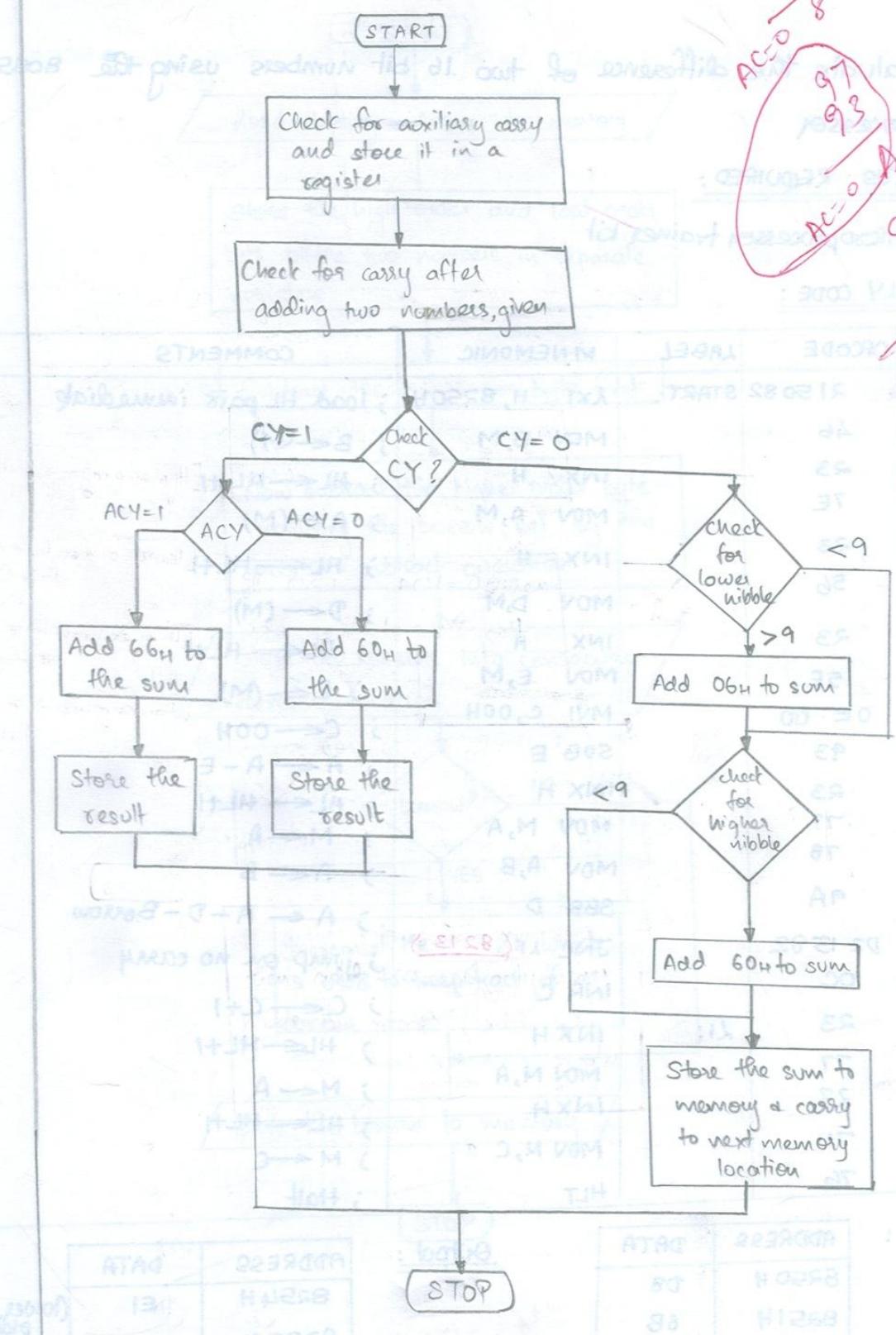
ADDRESS	DATA
82A2H	90
82A3H	01

(carry)

RESULT:19
10

Thus the sum of two BCD numbers is evaluated using the 8085 microprocessor.

FLOWCHART



97
91

8

DAP

AC=0
97
93
AC=0
99
99

Add if zone
0901

2

Xc

AT&F (value)	DATA (value)	ADDRESS (value)	DATA (value)
13F	07	H2258	H2258
07			
10		H3258	H3258

AT&F (value)	DATA (value)	ADDRESS (value)	DATA (value)
F0	8	H2258	H2258
8			
T3		H3258	H3258
A8		H3258	H3258

DATE: 15.02.2011 LARGEST AND SMALLEST NUMBER IN AN ARRAY

EX-NO.4

USING 8085 MICROPROCESSOR

AIM:

To find the largest and smallest number from an array of numbers, of known size.

COMPONENTS REQUIRED:

8085 microprocessor trainer kit.

ASSEMBLY CODE:

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENTS
8200H	A1 50 82	START:	LDI H, 8250H	; load H = L ⁱⁿ direct immediate
8203H	4E		MOV C,M	; C ← (M) [no. of elements, N]
8204H	23		INX H	; HL ← HL + 1
8205H	56		MOV D,M	; D ← (M) [max of N]
8206H	5E		MOV E,M	; E ← (M) [min of N]
8207H	23		INX H	; HL ← HL + 1
8208H	0D		DCR C	; C ← C - 1
8209H	7A	LOOP:	MOV A,D	; A ← D
820AH	BE		CMP M	; compare A with (M)
820BH	D2 0F 82		JNC L1	; jump on no carry
820EH	56		MOV D,M	; D ← (M)
820FH	7B	L1:	MOV A,E	; A ← E
8210H	BE		CMP M	; compare A with (M)
8211H	DA 1582		JC L2	; jump on carry
8214H	5E		MOV E,M	; E ← (M)
8215H	23	L2:	INX H	; HL ← HL + 1
8216H	0D		DCR C	; C ← C - 1
8217H	C2 09 82		JNZ LOOP	; jump on non zero
821AH	7A		MOV A,D	; A ← D
821BH	32 60 82		STA 8260H	; store accumulated direct
821EH	7B		MOV A,E	; A ← E
821FH	32 61 82		STA 8261H	; store accumulated direct
8222H	76		HLT	; halt

INPUT :

ADDRESS	DATA
8250 H	0A
8251 H	02
8252 H	09
8253 H	05
8254 H	07
8255 H	0C
8256 H	A0
8257 H	BC
8258 H	00
8259 H	CD
825AH	11

O/P

verified

152w01

152w01

OUTPUT: 9AH00H

ADDRESS	DATA	Comments
8260 H	CD	(largest)
8261 H	00	(smallest)

RESULT :

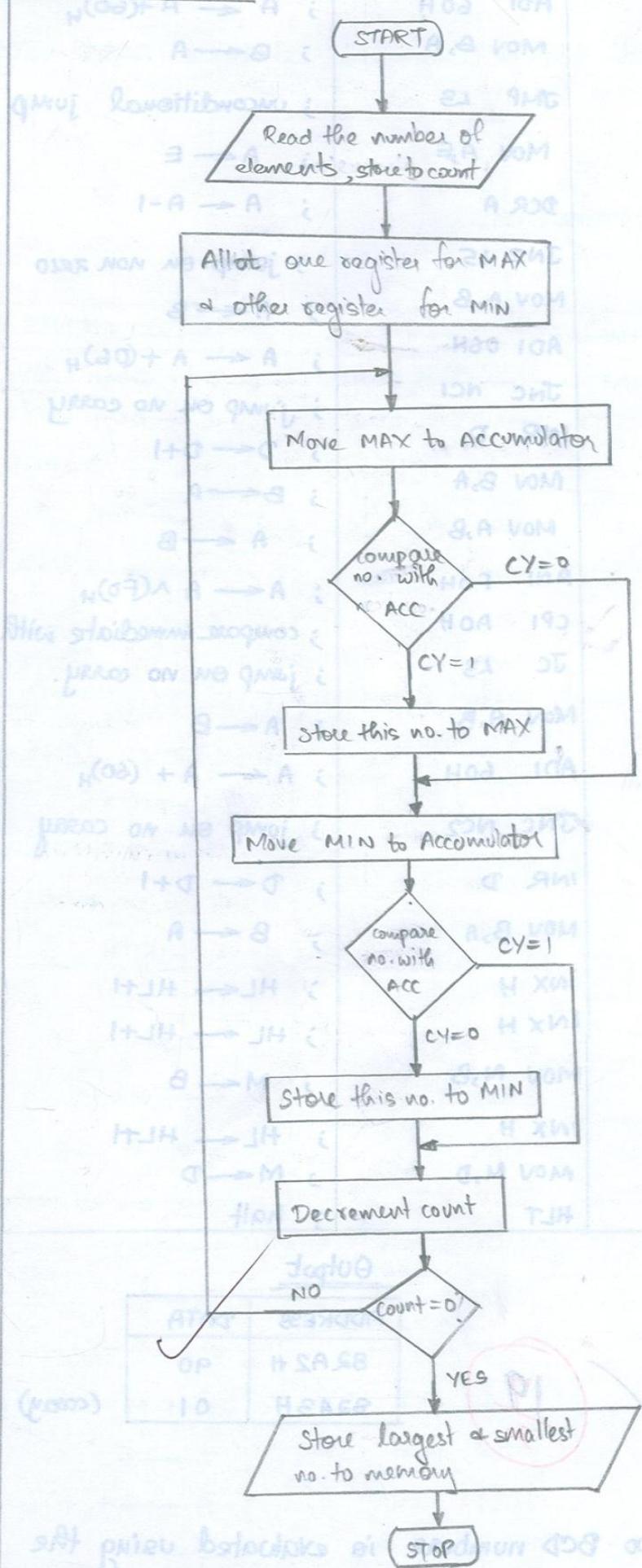
20
20

Hence, from the given N numbers, largest and smallest are found and stored to consecutive memory locations

152w01

8215 H	CB 04 92	LDAX B	load B with 92H
8216 H	CD	STAX D	store D
8217 H	22 65 82	JNZ A	jump on zero
8218 H	01 50 82	LDAX B	load B with 82H
8219 H	DA	STAX D	store D
8220 H	6F	JNZ A	jump on non-zero
8221 H	03	LDAX B	load B with 03H
8222 H	3D	STAX D	store D
8223 H	C2 21 82	JNZ A	jump on non-zero
8224 H	11 61 82	LDAX B	load B with 82H
8225 H	0B	STAX D	store D
8226 H	12	JNZ A	jump on zero

FLOWCHART:



DATE: 28-02-2011

SORTING IN ASCENDING AND DESCENDING ORDER

EX-N6-5

AIM:

To sort given array of N numbers using descending & ascending scheme.

COMPONENTS REQUIRED:

8085 microprocessor trainer kit.

ASSEMBLY CODE:

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENTS
8200H	21 50 82	START:	LXI H, 8250H	; load HL pair immediate
8203H	4E		MOV C, M	; count, C \leftarrow (M)
8204H	0D		DCR C	; C \leftarrow C-1
8205H	51	REP:	MOV D, C	; D \leftarrow C
8206H	31 51 82		LXI SP, 8251H	; load SP immediate
8209H	E1	LOOP:	POP H	; L \leftarrow (SP), SP \leftarrow SP+1, H \leftarrow SP
820AH	7D		MOV A, L	; A \leftarrow L
820BH	BC		CMP H	; compare A with H
820CH	DA 1282		JC NEXT	; jump on carry
820FH	44		MOV B, H	; B \leftarrow H }
8210H	65		MOV H, L	; H \leftarrow L } swap
8211H	68		MOV L, B	; L \leftarrow B }
8212H	E5	NEXT:	PUSH H	; (SP \leftarrow L, SP \leftarrow SP-1, SP \leftarrow SP+1) (SP \leftarrow H)
8213H	33		INX SP	
8214H	15		DCR D	; D \leftarrow D-1
8215H	C2 09 82		JNZ LOOP	; jump on non zero
8218H	0D		DCR C	; C \leftarrow C-1
8219H	C2 05 82		JNZ REP	; jump on non zero
821CH	01 50 82		LXI B, 8250H	; load BC pair immediate
821FH	0A		LDAX B	; load A with (BC)
8220H	6F		MOV L, A	; L \leftarrow A
8221H	D3	L1:	INX B	; BC \leftarrow BC+1
8222H	3D		DCR A	; A \leftarrow A-1
8223H	C2 21 82		JNZ LP	; jump on non zero
8226H	11 61 82		LXI D, 8261H	; load DE pair immediate
8229H	0A	L2:	LDAX B	; load A with (BL)
822AH	12		STAX D	; store A to (DE)

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENTS
822BH	0B		DCX B	; BC \leftarrow BC-1
822CH	13		INX D	; DE \leftarrow DE+1
822DH	2D		DCR L	; L \leftarrow L-1
822EH	C2 29 82		JNZ L2	; jump on non zero
8231H	76		HLT	; halt

B6R
28/2/14

18
18

INPUT

ADDRESS	DATA (H)
8250H	06
8251H	05
8252H	03
8253H	01
8254H	09
8255H	00
8256H	07

RESULT:

OUTPUT

ADDRESS	DATA (H)
8251H	00
8252H	01
8253H	03
8254H	05
8255H	07
8256H	09
8261H	09
8262H	07
8263H	05
8264H	03
8265H	01
8266H	00

ascending
order

descending
order

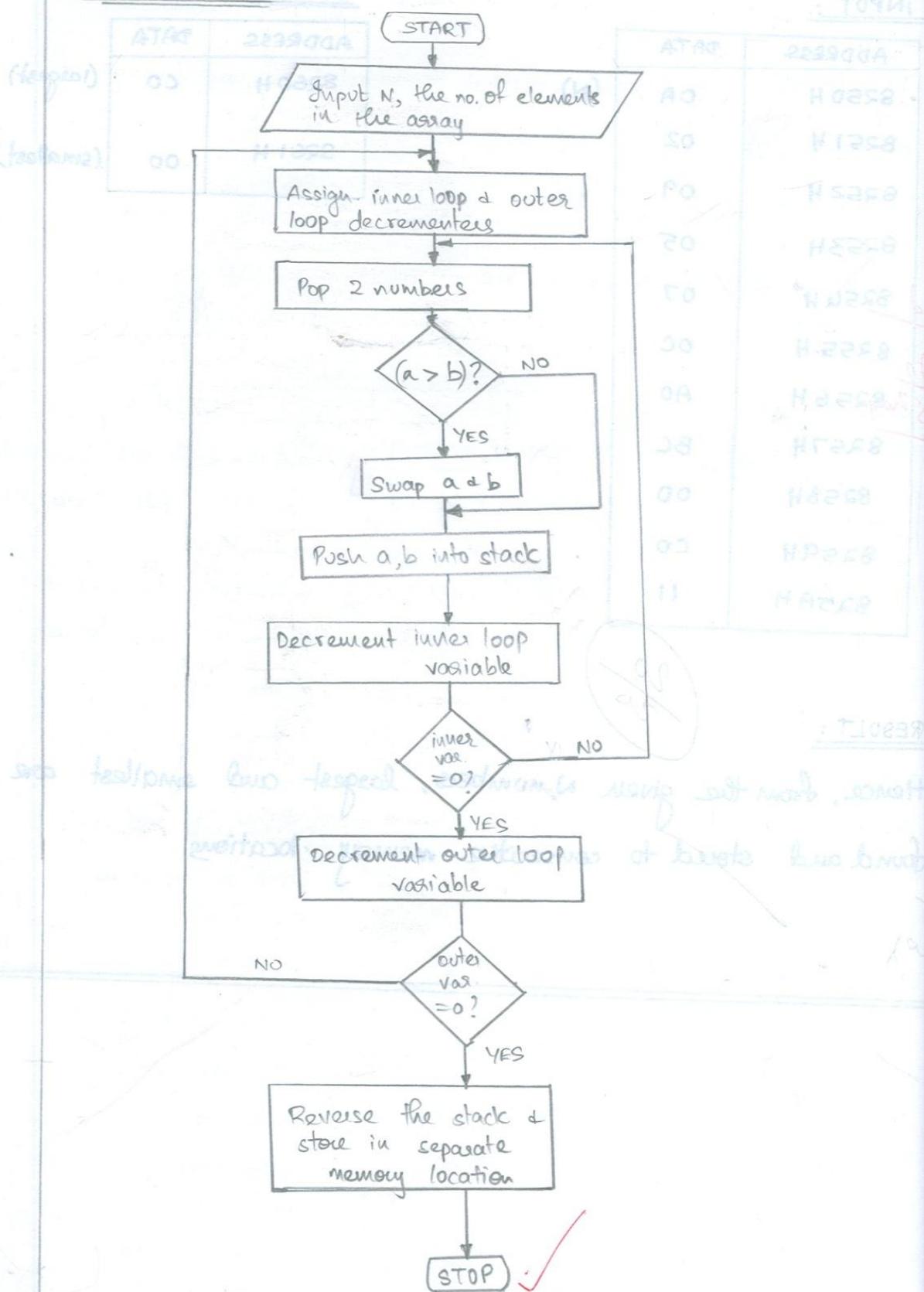
RESULT:

Hence the N numbers have been sorted in ascending and descending order and stored to the memory. Bubble sort algorithm is used.

18
18

Hence a square wave is generated by a 8085 microprocessor using its 8085 microprocessor.

FLOWCHART



AIM:

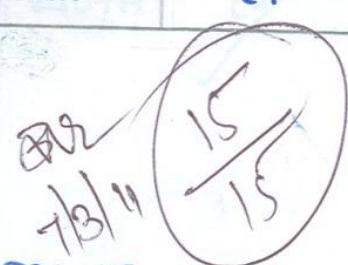
To generate a square wave (rectangular wave) of given frequency and duty cycle using the 8085 microprocessor.

COMPONENTS REQUIRED:

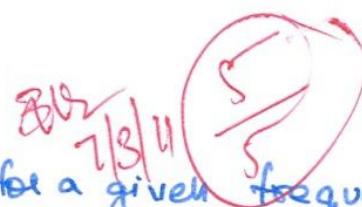
8085 microprocessor trainer kit, CRO / DSO

ASSEMBLY CODE:

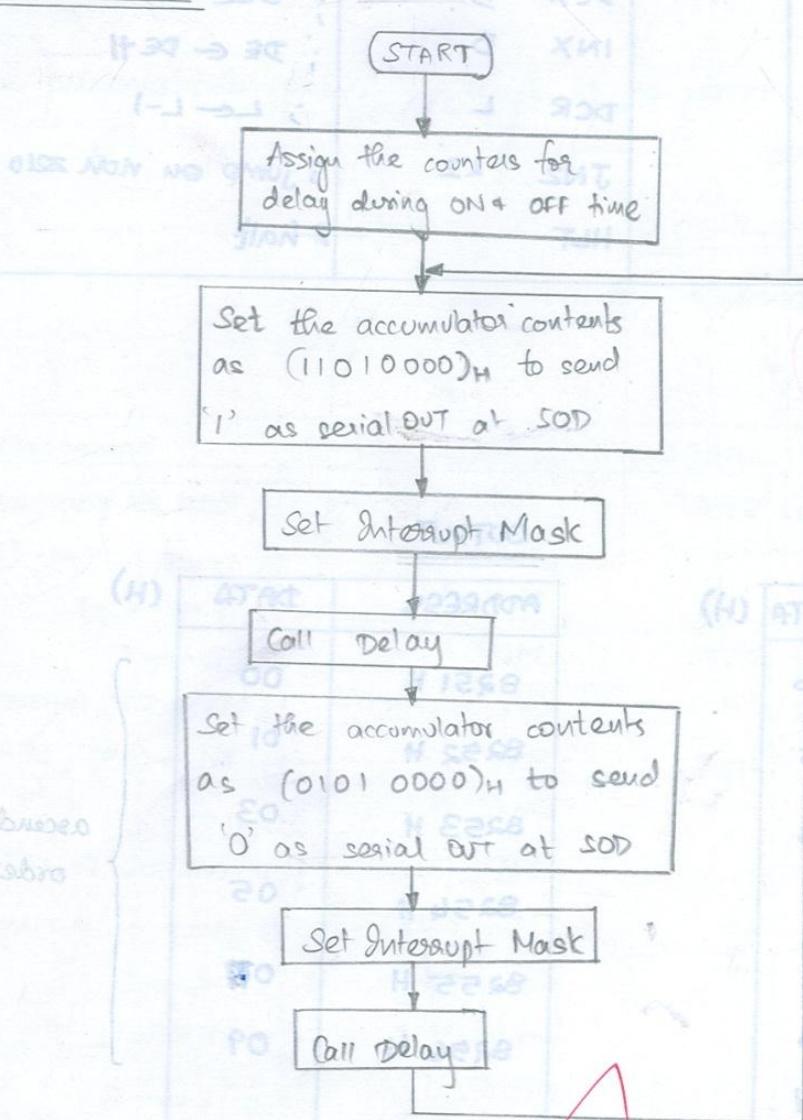
ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENTS
8200H	R1 FF FF	START:	LXI H, FFFFH	; On time
8203H	11 FF FF		LXI D, FFFFH	, Off time
8206H	3E D0	REPEAT:	MVI A, D0H	; A ← (D0) _H
8208H	30		SIM	; state set interrupt mask
8209H	CD 18 82		CALL DELAY	; call DELAY subroutine
820CH	EB		XCHG	
820DH	3E 50		MVI A, 50H	; exchange H ↔ D L ↔ E
820FH	30		SIM	; A ← (50) _H
8210H	CD 18 82		CALL DELAY	; set interrupt mask
8213H	EB		XCHG	; call DELAY subroutine
8214H	C3 06 82		JMP REPEAT	; exchange H ↔ D L ↔ E
8217H	76		HLT	; jump unconditional
8218H	44	DELAY: →	MOV B, H	; halt
8219H	4D		MOV C, L	; B ← H
821AH	0B	L1:	DCX B	; C ← L
821BH	79		MOV A, C	; (BC) ← (EC) - 1
821CH	B0		ORA B	; A ← C
821DH	C2 1A 82		JNZ L1	; OR A with B
8220H	C9		RET	; jump on non-zero
				; return

RESULT:

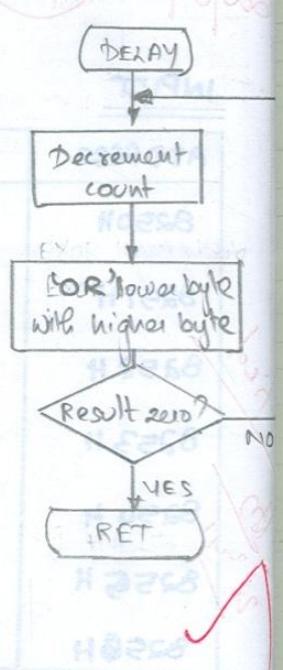
Hence a square wave is generated for a given frequency using the 8085 microprocessor.



FLOW CHART:



Delay subroutine



problems
sabre

No. of T-states in loop = 24

Clock frequency = 2 MHz

∴

$$T_{on} = (65536) \times (24) \times \frac{1}{2 \times 10^6} = 0.786 \text{ s}$$

~~$$T_{off} = (65536) \times (24) \times \frac{1}{2 \times 10^6} = 0.786 \text{ s}$$~~

$$\text{Duty cycle} = \frac{T_{on}}{T_{on} + T_{off}} = 50\%$$

$$T_{total} = 1.5728 \text{ s}$$

$$f = 0.636 \text{ Hz}$$

CRO output :

$$f = 0.616 \text{ Hz}$$

~~$$T = 1.624 \text{ s}$$~~

$$T_{on} = 0.812 \text{ s}$$

$$T_{off} = 0.812 \text{ s}$$

DATE : 15-03-2011

STEPPER MOTOR CONTROL USING 8085

EX NO. 7

MICROPROCESSORAIM :

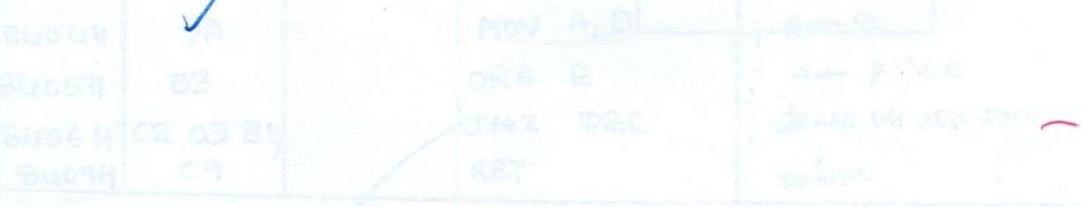
To control the operation of a stepper motor using the 8085 microprocessor and operate in full step and half step mode.

APPARATUS REQUIRED :

8085 microprocessor trainer kit, Stepper motor board, 8255 (PPI)

ASSEMBLY CODE : (1) FULL STEP MODE

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENTS
8200H	3E 82	MAIN:	MVI A, 82H	; A \leftarrow (82)H
8202H	D3 A3		OUT 0A3H	; write in CWR
8204H	3E 09	REPEAT:	MVI A, 09H	; A \leftarrow (09)H
8206H	D3 A0		OUT 0A0H	; write to port A
8208H	CD 00 84		CALL DELAY	; call delay routine
820BH	3E 05		MVI A, 05H	; A \leftarrow (05)H
820DH	D3 A0		OUT 0A0H	; write to port A
820FH	CD 00 84		CALL DELAY	; call delay routine
8212H	3E 06		MVI A, 06H	; A \leftarrow (06)H
8214H	D3 A0		OUT 0A0H	; write to port A
8216H	CD 00 84		CALL DELAY	; call delay routine
8219H	3E 0A		MVI A, 0AH	; A \leftarrow (0AH)
821BH	D3 A0		OUT 0A0H	; write to port A
821DH	CD 00 84		CALL DELAY	; call delay routine
8220H	C3 D4 82		JMP REPEAT	; jump
8400H	11 FF10	DELAY:	LXI D, 10FFH	; DE \leftarrow (10FF)H
8403H	1B	DEC:	DCX D	; DE \leftarrow DE - 1
8404H	7A		MOV A,D	; A \leftarrow D
8405H	B3		DRA E	; OR 'A' with 'E'
8406H	C2 03 84		JNZ DEC	; jump on non-zero
8409H	C9		RET	; return.

RESULT:

Hence the operation & control of a stepper motor is achieved in both full step and half step mode using the 8085 microprocessor.

② Half Step mode :

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENT :
8200H	3E 82	MAIN:	MVI A, 82H	; A ← (82)H
8202H	D3 A3		OUT 0A3H	; write in CWR
8204H	3E 09	REPEAT:	MVI A, 07H	; A ← (07)H
8206H	D3 A0		OUT 0AOH	; write to port A
8208H	CD 0084		CALL DELAY	; call delay routine
820BH	3E 06		MVI A, 06H	; A ← (06)H
820DH	D3 A0		OUT 0AOH	; write to port A
820FH	CD 0084		CALL DELAY	; call delay routine
8212H	3E 0E		MVI A, 0EH	; A ← (0E)H
8214H	D3 A0		OUT 0AOH	; write to port A
8216H	CD 0084	NEXT:	CALL DELAY	; call delay routine
8219H	3E 0A		MVI A, 0AH	; A ← (0A)H
821BH	D3 A0		OUT 0AOH	; write to port A
821DH	CD 0084		CALL DELAY	; call delay routine
8220H	3E 0B		MVI A, 0BH	; A ← (0B)H
8222H	D3 A0		OUT 0AOH	; write to port A
8224H	CD 0084		CALL DELAY	; call delay routine
8227H	3E 09		MVI A, 09H	; A ← (09)H
8229H	D3 A0		OUT 0AOH	; write to port A
822BH	CD 0084		CALL DELAY	; call delay routine
822EH	3E 0D	REP:	MVI A, 0DH	; A ← (0D)H
8230H	D3 A0		OUT 0AOH	; write to port A
8232H	CD 0084		CALL DELAY	; call delay routine
8235H	3E 05		MVI A, 05H	; A ← (05)H
8237H	D3 A0		OUT 0AOH	; write to port A
8239H	CD 0084		CALL DELAY	; call delay routine
823CH	C3 0482		JMP REPEAT	; jump
8400H	11 FF00	DELAY:	LXI D, 0FFFH	; DE ← 0FFFH
8403H	1B	DEC:	DCX D	; DE ← DE-1
8404H	7A		MOV A, D	; A ← D
8405H	B3		ORA E	; A ← A ∨ E
8406H	C2 0384	DELAY	JNZ DEC	; jump on non-zero
8409H	C9		RET	; return

RESULT:

Hence the operation & control of a stepper motor is achieved in both full step and half step mode using the 8085 microprocessor.

Initialization :

8255

Port A - $(0A0)_H$

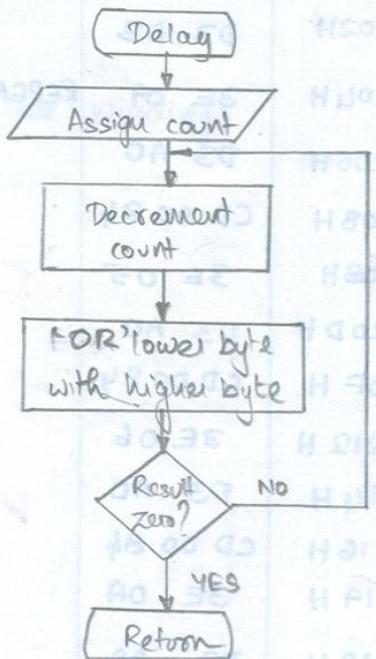
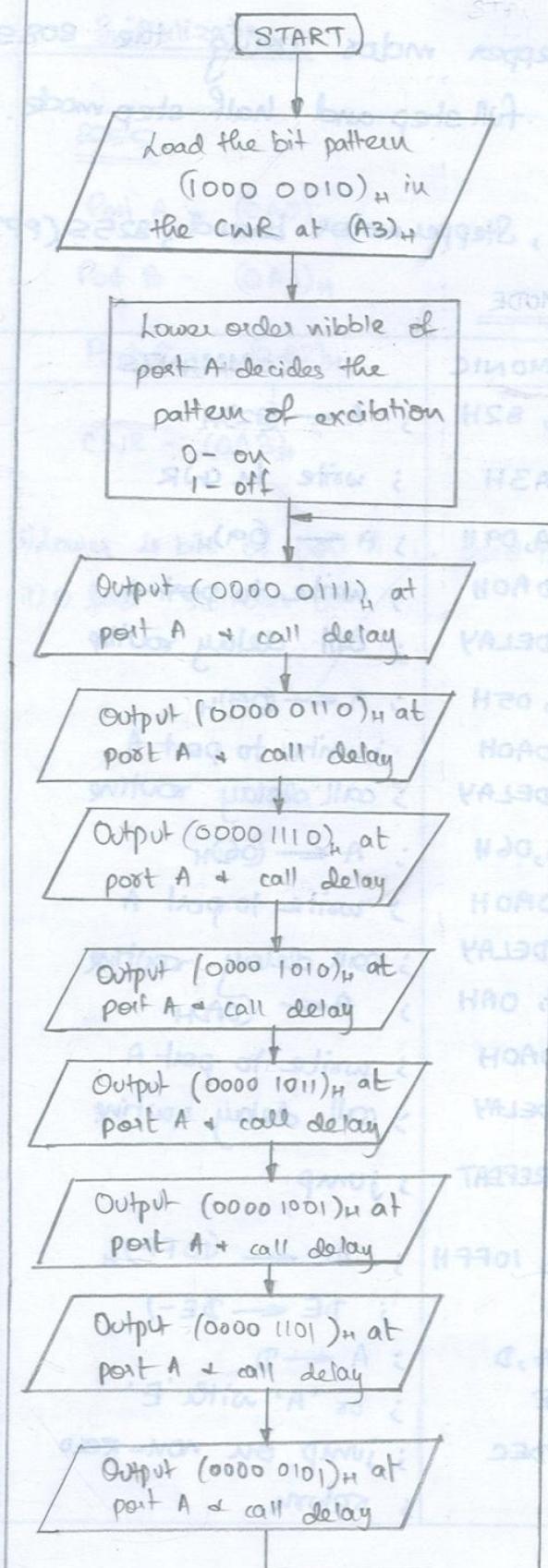
Port B - $(0A1)_H$

Port C - $(0A2)_H$

CWR - $(0A3)_H$

- i) lower 4 bits of port A is used to switch on the windings
- ii) O level switches on

FLOWCHART



AIM:

To interface the ADC and verify its operation with the help of the 8085 microprocessor trainer kit.

APPARATUS REQUIRED:

8085 microprocessors trainer kit, ADC board, 8255 (PP1)

ASSEMBLY CODE :

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENTS
8200H	3E 98		MVI A, 98H	; A $\leftarrow (98)_H$ PA - I/O PCl - O/I P
8202H	D3 A3		OUT A3H	; write in the CWR
8204H	3E 01	NEXT:	MVI A, 01H	; A $\leftarrow (01)_H$ (channel address) $\hookrightarrow PC_0$
8206H	D3 A2	SUCCESS	OUT A2H	; write to port C
8208H	3E 03	FAILURE	MVI A, 03H	; A $\leftarrow (03)_H$ (ALE-High) $\hookrightarrow PC_1$
820AH	D3 A2		OUT A2H	; write to port C
820CH	3E 07		MVI A, 07H	; A $\leftarrow (07)_H$ (start of convert)
820EH	D3 A2		OUT A2H	; write to port C $\hookrightarrow PC_2$
8210H	3E 01		MVI A, 01H	; A $\leftarrow (01)_H$ (ALE-0) $\hookrightarrow SOC-0$
8212H	D3 A2		OUT A2H	; write to port C
8214H	3E 64		MVI A, 64H	; A $\leftarrow (64)_H$ }
8216H	3D	REP:	DCR A	; A $\leftarrow (A-1)$ } Delay
8217H	C2 16 82		JNZ REP	; jump on non zero
821AH	DB A2	L1:	IN A2H	; read port C
821CH	E6 10		ANI 10H	; A $\leftarrow A \wedge (10)_H$ (check EOC) $\hookrightarrow PC_4$
821EH	CA 1A 82		JZ L1	; jump on zero
8221H	3E 08		MVI A, 08H	; A $\leftarrow 68_H$ } set output enable
8223H	D3 A2		OUT A2H	; write to port C } using $\hookrightarrow PC_3$
8225H	DB A0		IN A0H	; read port for ADC data
8227H	D3 A8	for LED	OUT A8H	; write ^(8 bits) to LED at PA
8229H	CD 0084	delay	CALL DELAY	; call delay
822CH	C3 04 82	return	JMP NEXT	; jump
8400H	11 FF FF	DELAY:	LXI D, FFFFH	; load DE pair immediate
8403H	1B	L2:	DCX D	; DE $\leftarrow DE-1$
8404H	7A		MOV A, D	; A $\leftarrow D$
8405H	B3		ORA E	; A $\leftarrow A \vee E$
8406H	C2 D3 84		JNZ L2	; jump on non zero
8409H	C9		RET	; return

OBSERVATION :

Max ilp = 4.85V

Calculated analog ilp	Observed analog ilp	Calculated digital ilp	Observed digital ilp
-	4.32 V	11100011	11100100
4.336 V	-	11100100	11100101
-	2.9612 V	10011100	10011100
2.967 V	-	10011100	10011101

RESULT:

Verified
Program
1/04

- (10) The ADC was successfully interfaced with the 8085 microprocessor trainer kit and its operation was verified.
- (20) ~~The ADC was successfully interfaced with the 8085 microprocessor trainer kit and its operation was verified.~~

8400H : 00 0000 11
 8401H : 00
 8402H : 00
 8403H : 00
 8404H : 10
 8405H : 74
 8406H : B3
 8407H : C2 09 00
 8408H : , 00
 8409H : C2 02 00
 840AH : C9

CONCLUSION:

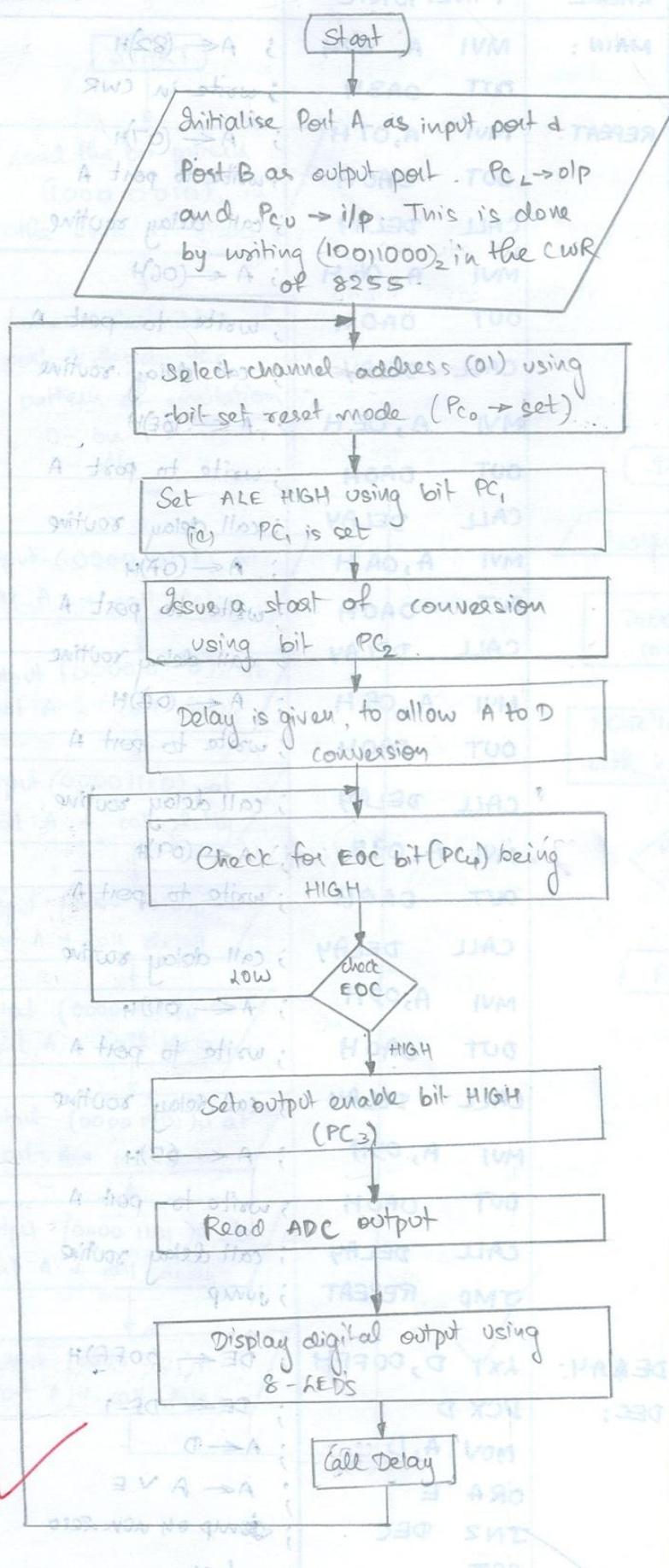
Sawtooth wave - 0.1 peak - 2V

Time period - 15ms

REPORT:

Hence the operation of a DAC was verified by interfacing it with the 8085 microprocessor trainer kit.

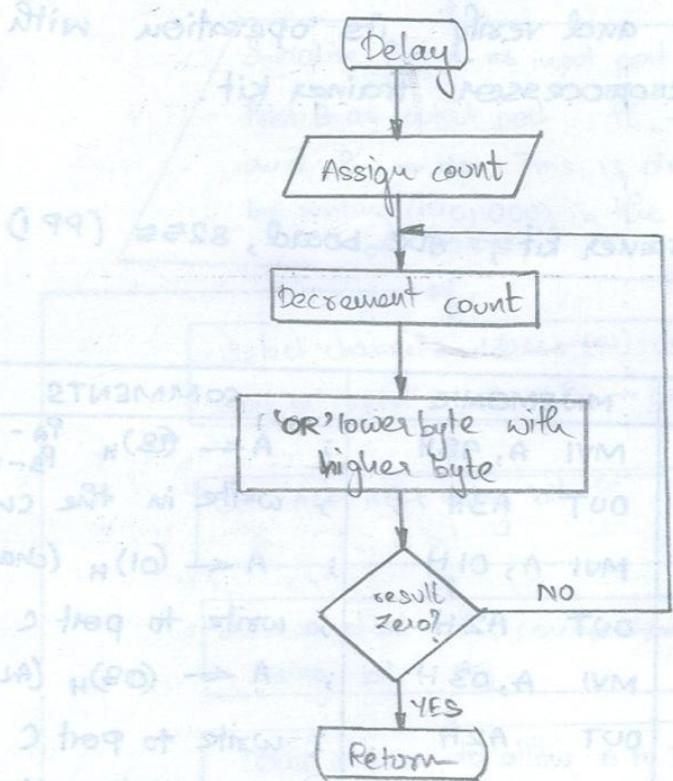
FLOWCHART:



Delay : → next page

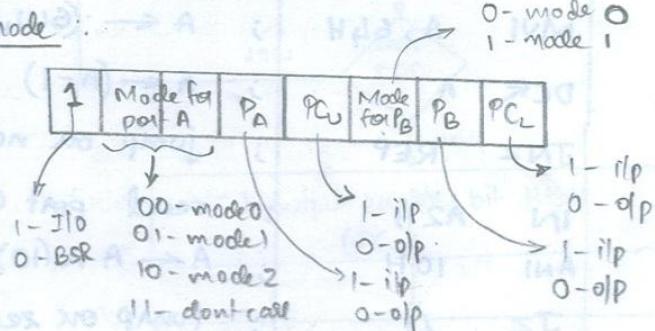
ni Basishas er solon rogesete o 3 lajco = weitoro set aat te dherogen set aat te dherogen
recessor set privz about gate float bne gate lA + slot 19

FLOWCHART for DELAY SUBROUTINE

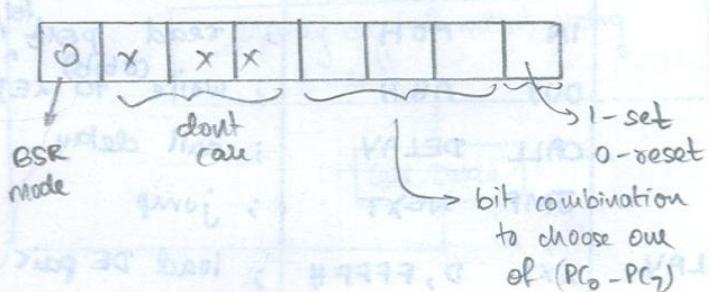


Control word of 8255

I/O mode:



BSR mode:



AIM:

To interface the DAC and verify its operation with the help of the 8085 microprocessor trainer kit.

APPARATUS REQUIRED:

8085 microprocessor trainer kit, DAC board, 8255 (PPI)

ASSEMBLY CODE:

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENTS
8200H	3E 98	MAIN:	MVI A, 98H	; A \leftarrow (98)H PA \rightarrow i/P PB \rightarrow o/P PW _{IP}
8202H	D3 A3		OUT A3H	; write in the CWR
8204H	D6 00		MVI B, 00H	; B \leftarrow (60) _H
8206H	78	NEXT:	MOV A,B	; A \leftarrow B
8207H	D3 A1		OUT A1H	; write in port B
8209H	04		INR B	; B \leftarrow B + 1
820AH	CD 00 84		CALL DELAY	; call delay
820DH	C3 06 82		JMP NEXT	; jump
8400H	OE 02	DELAY:	MVI C, 02H	; C \leftarrow (62) _H
8402H	11 FFFF	L2:	AXI D, FFFFH	; DE \leftarrow (FFFF) _H
8405H	00	L1:	NOP	; no-operation
8406H	00		NOP	
8407H	00		NOP	
8408H	1B		DCX D	; DF \leftarrow DE - 1
8409H	7A		MOV A,D	; A \leftarrow D
840AH	B3		DRA E	; A \leftarrow AVE
840BH	C2 05 84		JNZ L1	; jump on non zero
840EH	0D		DCR C	; C \leftarrow C - 1
840FH	C2 02 84		JNZ L2	; jump on non zero
8412H	C9		RET	; return

OBSERVATION:

Saw-tooth wave : - V_o (peak-peak) = 4V

Time period = 15ms.

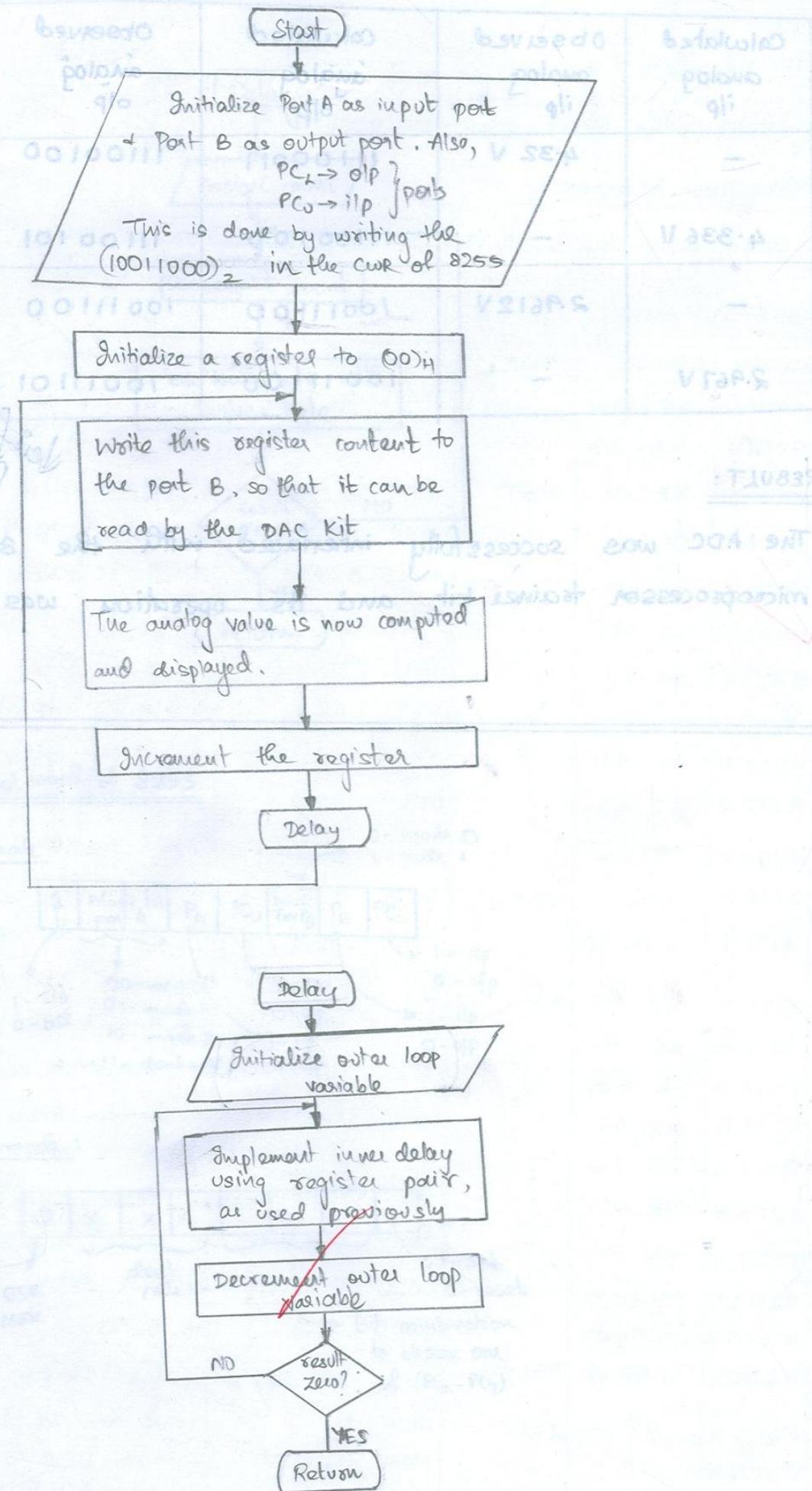
Verified
Oscilloscope
Not

RESULT:

Hence the operation of a DAC was verified by interfacing it with the 8085 microprocessor trainer kit.

20/20
12/11

FLOWCHART



END. 9

USING - 8085 MICROPROCESSORAIM:

To control traffic lights for 2 modes, with both vehicle control + pedestrian control, using the 8085 microprocessor.

APPARATUS REQUIRED :

8085 microprocessor trainer kit, traffic light LED board, 8255 (PPI).

ASSEMBLY CODE :

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENT
8200H	3E 81	START:	MVI A, 81H	; PA=0lp, PB=0lp, PC ₁ =1lp
8202H	D3 A3		OUT A3H	; write in CWR
8204H	06 02		MVI B, 02H	; Day/Night pattern check
8206H	DB A2		IN A2H	; read Port C (bit PC ₁)
8208H	A0		ANA B	
8209 H	C2 00 83		JNZ NIGHT	; if PC ₁ =1, jump to NIGHT
820CH	C3 0F82		JMP DAY	; if PC ₁ =0, jump to DAY.
820FH	3E 00	DAY:	MVI A, 00H	; turn off all LEDs
8211H	D3 A0		OUT A0H	; in north-south
8213H	D3 A1		OUT A1H	; in east-west
8215H	3E 14		MVI A, 14H	Turn green at north
8217H	D3 A0		OUT A0H	red at the rest.
8219H	3E 11		MVI A, 11H	Thus N-S } allowed
821BH	D3 A1		OUT A1H	N-W } N-E }
821DH	OE 07		MVI C, 07H	
821FH	CD 00 84	L1:	CALL DELAY	
8222H	OD		DCR C	
8223H	C2 1F82		JNZ L1	
8226H	3E 12		MVI A, 12H	turn yellow at north
8228H	D3 A0		OUT A0H	}
822AH	OE 02		MVI C, 02H	for some time
822CH	CD 00 84	L2:	CALL DELAY	
822FH	OD		DCR C	
8230H	C2 2C82		JNZ L2	

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENT
8233H	3E 44		MVI A, 44H	
8235H	D3 A0		OUT A0H	
8237H	3E 99		MVI A, 99H	
8239H	D3 A1		OUT A1H	
823BH	0E 07		MVI C, 07H	
823DH	CD 00 84	L3:	CALL DELAY	
8240H	OD		DCR C	
8241H	C2 3D 82		JNZ L3	
8244H	3E 42		MVI A, 42H	
8246H	D3 A0		OUT A0H	
8248H	0E 02		MVI C, 02H	
824AH	CD 00 84	L4:	CALL DELAY	
824DH	OD		DCR C	
824EH	C2 4A 82		JNZ L4	
8251H	3E 41		MVI A, 41H	
8253H	D3 A0		OUT A0H	
8255H	3E 11		MVI A, 11H	
8257H	D3 A1		OUT A1H	
8259H	0E 07		MVI C, 07H	
825BH	CD 00 84	L5:	CALL DELAY	
825EH	OD		DCR C	
825FH	C2 5B 82		JNZ L5	
8262H	3E 21		MVI A, 21H	
8264H	D3 A0		OUT A0H	
8266H	0E 02		MVI C, 02H	
8268H	CD 00 84	L6:	CALL DELAY	
826BH	OD		DCR C	
826CH	C2 68 82		JNZ L6	
826FH	3E 11		MVI A, 11H	
8271H	D3 A0		OUT A0H	
8273H	3E 14		MVI A, 14H	
8275H	D3 A1		OUT A1H	
8277H	0E 07		MVI C, 07H	
8279H	CD 00 84	L7:	CALL DELAY	
827CH	OD		DCR C	
827DH	C2 79 82		JNZ L7	

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENT
8280H	3E 12		MVI A, 12H	
8282H	D3 A1		OUT A1H	{ Turn yellow on all east for some time
8284H	DE 02		MVI C, 02H	
8286H	CD 0084	L8:	CALL DELAY	
8289H	OD		DCR C	
828AH	C2 8682		JNZ L8	
828DH	3E 99		MVI A, 99H	
828FH	D3 A0		OUT A0H	
8291H	3E 44		MVI A, 44H	{ turn green at east & west for E-W + W-E traffic + turn pedestrian on at south + north.
8293H	D3 A1		OUT A1H	
8295H	DE 07		MVI C, 07H	
8297H	CD 0084	L9:	CALL DELAY	
829AH	OD		DCR C	
829BH	C2 9782		JNZ L9	
829EH	3E 42		MVI A, 42H	{ turn yellow at east for some time
82A0H	D3 A1		OUT A1H	
82A2H	DE 02		MVI C, 02H	
82A4H	CD 0084	L10:	CALL DELAY	
82A7H	OD		DCR C	
82A8H	C2 A482		JNZ L10	
82ABH	3E 11		MVI A, 11H	
82ADH	D3 A0		OUT A0H	
82AFH	3E A1		MVI A, 41H	{ turn green at west + red at the rest to get W-S W-N W-E
82B1H	D3 A1		OUT A1H	
82B3H	DE 07		MVI C, 07H	
82B5H	CD 0084	L11:	CALL DELAY	
82B8H	OD		DCR C	
82B9H	C2 B582		JNZ L11	
82BCH	3E 21		MVI A, 21H	{ turn on yellow at west for some time
82BEH	D3 A1		OUT A1H	
82COH	DE 02		MVI C, 02H	
82C2H	CD 0084	L12:	CALL DELAY	
82C5H	OD		DCR C	
82C6H	C2 C282		JNZ L12	
82C9H	C3 0082		JMP START	; repeat

ADDRESS	OPCODE	LABEL	MNEMONIC	COMMENT
8300H	3E 22	NIGHT:	MVI A,22H	; make yellow lamps on
8302H	D3 A0		OUT A0H	; in north south
8304H	D3 A1		OUT A1H	; in east west
8306H	CD 0084		CALL DELAY	
8309H	3E 00		MVI A,00H	; make yellow lamps off
830BH	D3 A0		OUT A0H	; in north south
830DH	D3 A1		OUT A1H	; in east west
830FH	CD 0084		CALL DELAY	
8312H	C3 0082		JMP START	
8400H	11 FFFF	DELAY:	LXI D,FFFFH	; load count
8403H	1B	DEC:	DCX D	; decrement
8404H	7A		MOV A,D	↓
8405H	B3		ORA E	↓ .OR lower + higher byte
8406H	C2 0384		JNZ DEC	↓
8409H	C9		RET	; return

RESULT:

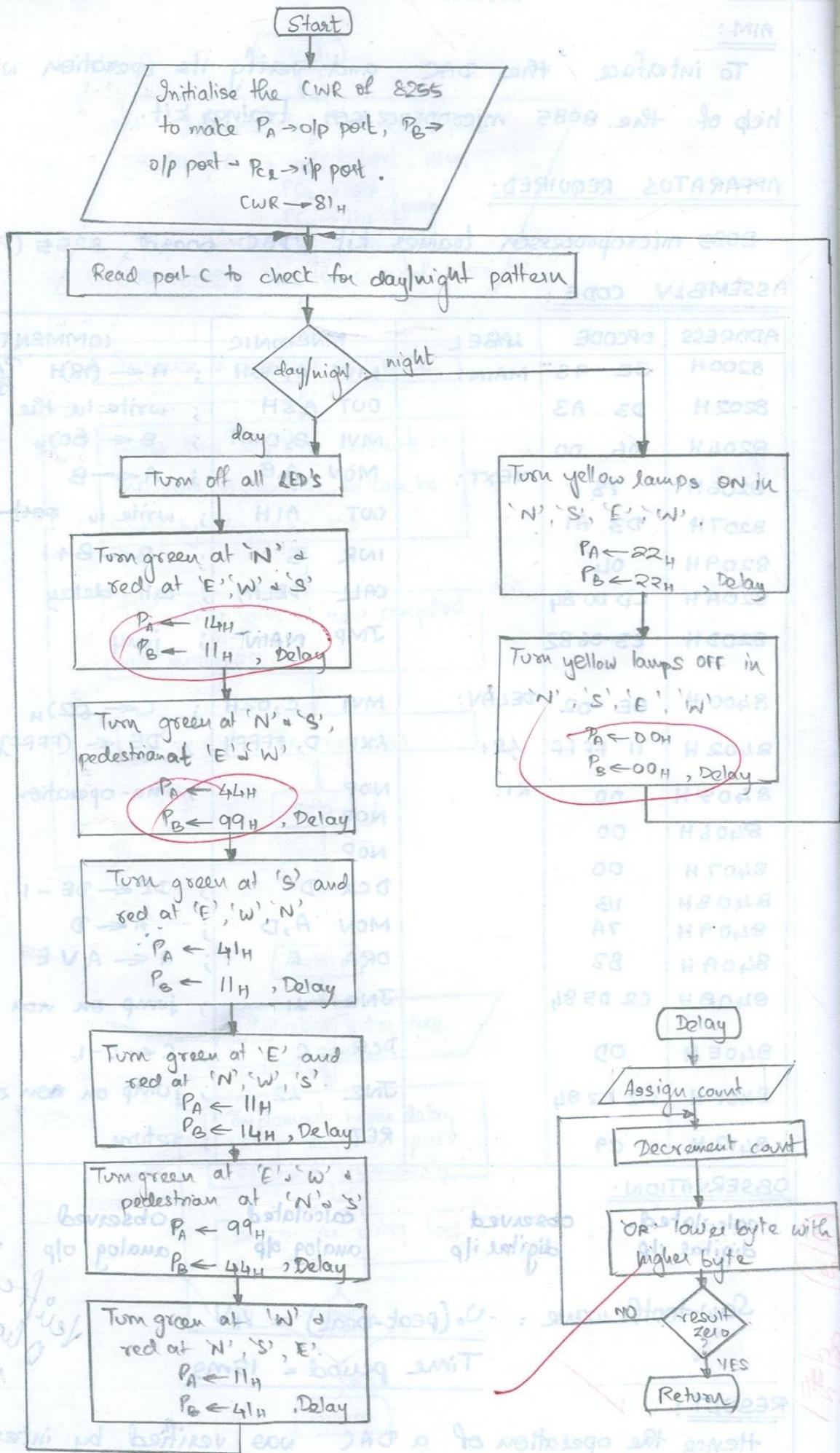
Hence the traffic light control is implemented in both vehicle + pedestrian mode using the 8085 microprocessor.

Test
7/4/14

10/10
19/4/14

9/10

FLOWCHART:

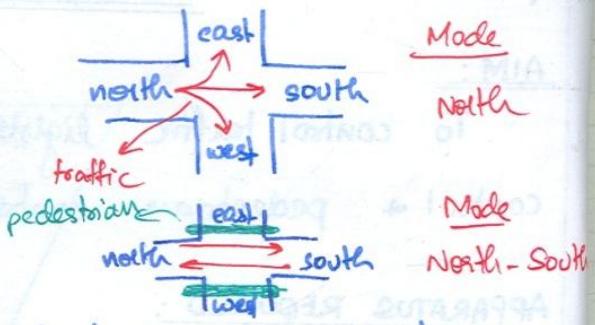


Port A → AOH

Port B → A1 H

Port C → A2 H

CWR → A3 H



North

PA₀-R

PA₁-Y

PA₂-G

PA₃ - Pedestrian PA₇ - Pedestrian

South

PA₄ - R

PA₅ - Y

PA₆ - G

PA₃ - Pedestrian PA₇ - Pedestrian

East

PB₀ - R

PB₁ - Y

PB₂ - G

PB₃ - Pedestrian

West

PB₄ - R

PB₅ - Y

PB₆ - G

PB₇ - Pedestrian

Ordering of modes

- North
- North - South
- South
- East
- East - West
- West.