EXPERIMENT #8 ANALOG TO DIGITAL CONVERSION

I OBJECTIVES

The objective of this experiment is to familiarize the student with the basic principles of analog to digital conversion. The aspects of converting a uni-polar analog signal to a 8-bit digital signal are explored. The emphasis will be on the Successive Approximation technique based conversion.

II COMPONENTS AND INSTRUMENTATION

The focus will be on the ADC0809 which is a 8-bit Successive Approximation type ADC. For power, you will use +5 V. As well, you need some resistors, capacitors and a few LEDs. Also a hex inverter IC (SN7414) for generating the clock signal. Note that it is important to bypass the power supplies directly on your prototyping board, using, for each supply, a parallel combination of a 100μF tantalum or electrolyte capacitors and or 0.1 μF low inductance ceramic capacitor. For measurement, you will use a bench multimeter.

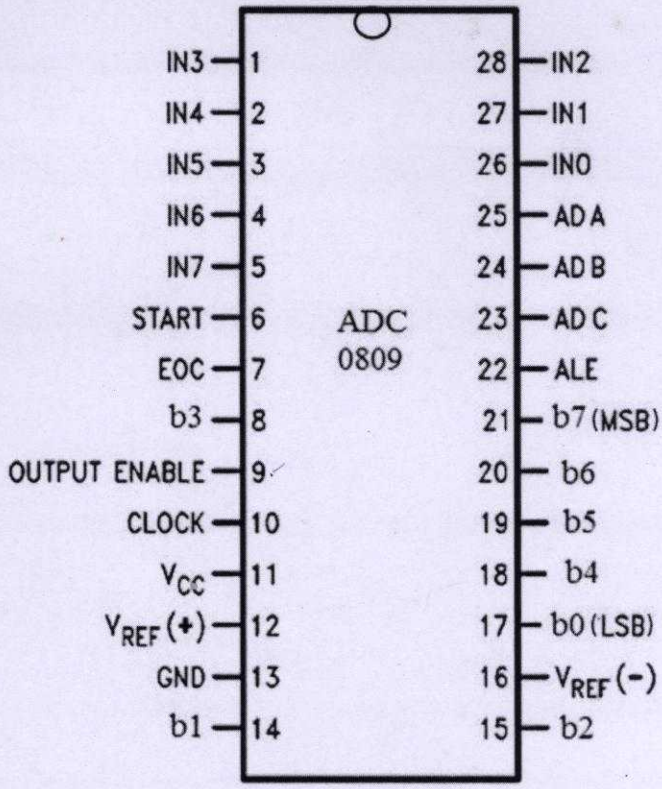


Fig.8.1 Pin diagram of ADC 0809
(refer to data sheets for more details)

III BRIEF THEORY

To convert an analog signal to digital form (i.e. to represent an analog voltage of 2.83623V using a binary number such as 101) we must know both the maximum possible range of the input signal (from 0V to a maximum, traditionally called V_{ref}) and the number of bits that will be used to represent it (called N). Dividing a 0-4V range into 4 distinct levels gives four 1V steps: these are 0, 1, 2, and 3V (NOT 4V). So, in summary, if you power your A/D converter with 0 and V_{ref} volts, you can get out of it anything from 0V to just 1 step less than V_{ref}, which mathematically is 0V to $V_{ref}(2^N - 1)$.

The following general formula converts an analog input voltage V_{analog} to a digital output V_{out} (decimal equivalent of N-bit binary input with scaling):

$$Vout = \frac{B}{2^N} V_{ref} \quad (8.1)$$ where 'B' is the decimal equivalent of the N-bit binary output. That is

$$B = \sum_{i=0}^{N-1} b_i 2^i$$

Fig.8.2 shows the transfer characteristics which is also known as the stair-case waveform of a 3-bit ADC. This is extended to 256 steps in a 8-bit ADC such as ADC0809. The operation of ADC-0809 is based on 'Successive Approximation' principle using (8.1).

The digital output voltage can be computed as

$$V_{out} = \frac{V_{ref}}{256}\left[\sum_{i=0}^{7} b_i 2^i\right]$$

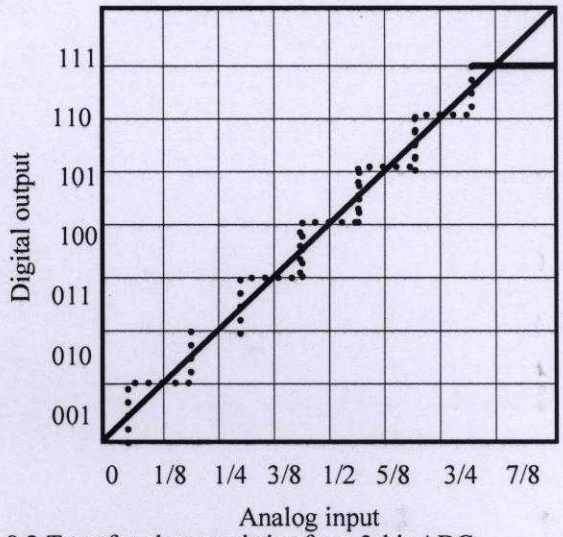


Fig. 8.2 Transfer characteristics for a 3-bit ADC

The resolution of an ADC is the smallest change in the analog signal that can be processed by the ADC. It is given by

Resolution = $1/2^N$ *pu*.

IV PREPARATION

1. An 8-bit ADC outputs all 1's when the input voltage is 5.1V. Calculate the resolution. Find the output voltage for an input of a)1 V b) 2.50 V c) 3.40V d) 4.68 V

2. An ADC converts a given positive analog signal into a digital signal. The reference voltage is 5 V. The least measurable voltage is not greater than 0.0048828 V. What is the number of bits at output?

3. What is the purpose of a clock input signal in the experiment using ADC-0809?

4. Specify the required voltages at AD A, AD B and AD C for selecting input channel 3 in ADC0809. (refer to data sheets)

V EXPLORATIONS

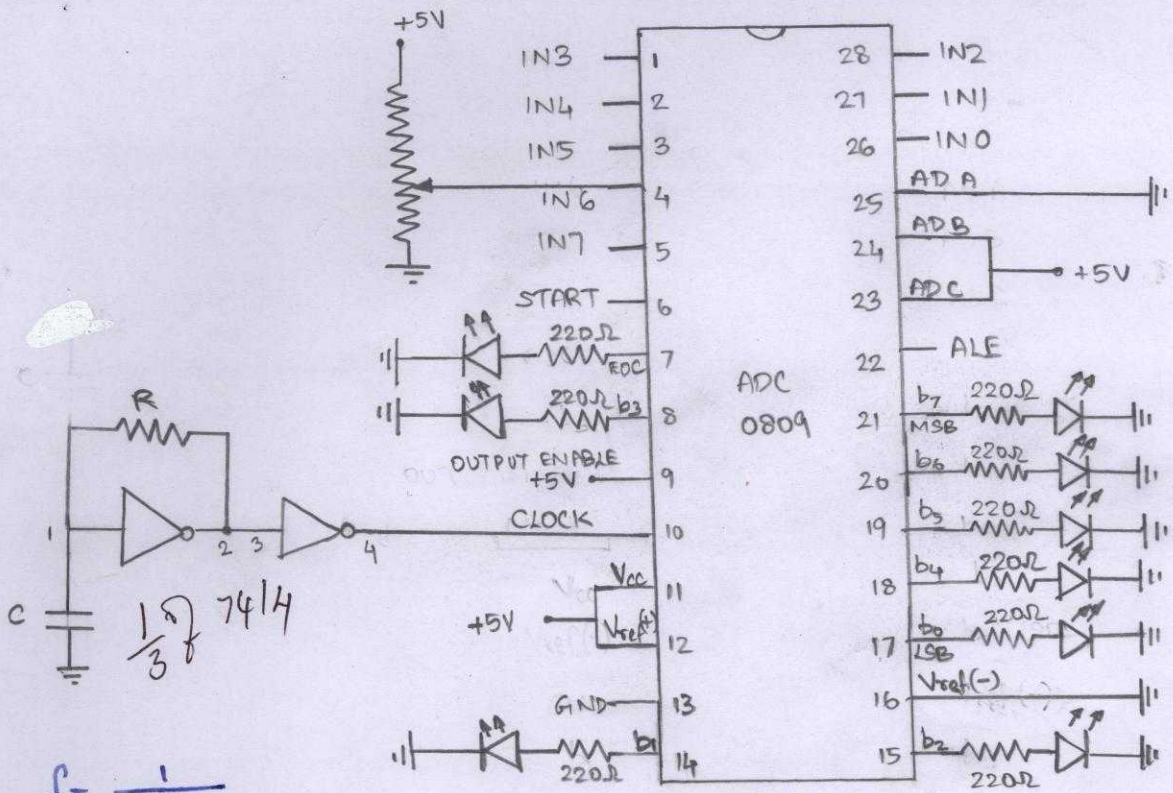
5.1

5.11 Design: Configure the voltage levels at AD A, AD B and AD C for selecting input channel
6 in your set up using ADC0809. Use Vref= +5V. Indicate how the channel is selected.

f= 55KHz

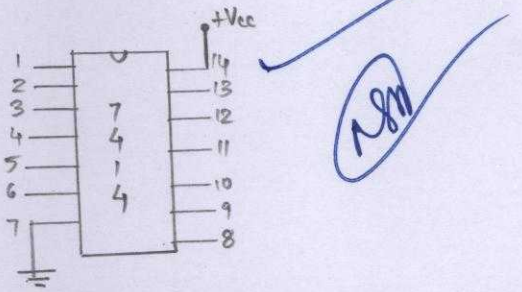
C= 0.01KF

5.12 Draw a neat circuit diagram with all details for your ADC circuit.(Include details of input channel selection, clock frequency).



$f = \frac{1}{2.2RC}$

$R = 289.37\ \Omega$



$f = 55\text{KHz}$

$C = 0.01\ \text{RF}$

Input channel = IN6

∴ ADA = LOW
ADB = HIGH
ADC = HIGH.

ALE - address latch enable

5.2 Procedure:

1. Make the connections as shown in the circuit diagram.
2. Set the analog signal input at the minimum level.
3. Set the **ALE** pin to logical high.
4. Set the **SOC** pin to logical high momentarily and then connect back to ground.
5. Set the **ALE** pin to back to logical low. The **EOC** should now be seen (indicated by the glow of the EOC LED).
6. Record the state of the output bits (logical high or low , indicated by the corresponding LED glowing or otherwise). Compute the equivalent analog output voltage.
7. Repeat the above steps (2-6) for different values of analog inputs (from 0 V to 5 V) and fill in the rest of the Table 8.1.

S.No.	Analog input V	Digital output (logical '0' or '1')								Decimal count (B)	V_{out} (measured) V	% error
1		b7	b6	b5	b4	b3	b2	b1	b0			
2	0	0	0	0	0	0	0	0	0	0	0	0
3	0.522	0	0	0	1	1	0	1	1	27	0.5273	-1.015
4	1.02	0	0	1	1	0	1	0	0	52	1.0156	0.4313
5	1.502	0	1	0	0	1	1	0	1	77	1.5039	-0.126
6	2.02	0	1	1	0	0	1	1	1	103	2.0117	0.411
7	2.60	1	0	0	0	0	1	0	1	133	2.5976	0.092
8	2.83	1	0	0	1	0	0	0	0	144	2.8125	0.618
9	3.02	1	0	0	1	1	0	1	0	154	3.0078	0.4039
10	3.15	1	0	1	0	0	0	0	0	160	3.125	0.7936
11	3.31	1	0	1	0	1	0	0	0	168	3.2813	0.867
12	3.71	1	0	1	1	1	1	0	1	189	3.6914	0.5013
13	4.12	1	1	0	1	0	0	0	1	209	4.082	0.9223
14	4.516	1	1	1	0	0	1	1	0	230	4.492	0.5314
15	4.8276	1	1	1	1	0	1	0	1	245	4.785	0.8824
16	5.012	1	1	1	1	1	1	1	1	255	4.9804	0.6305

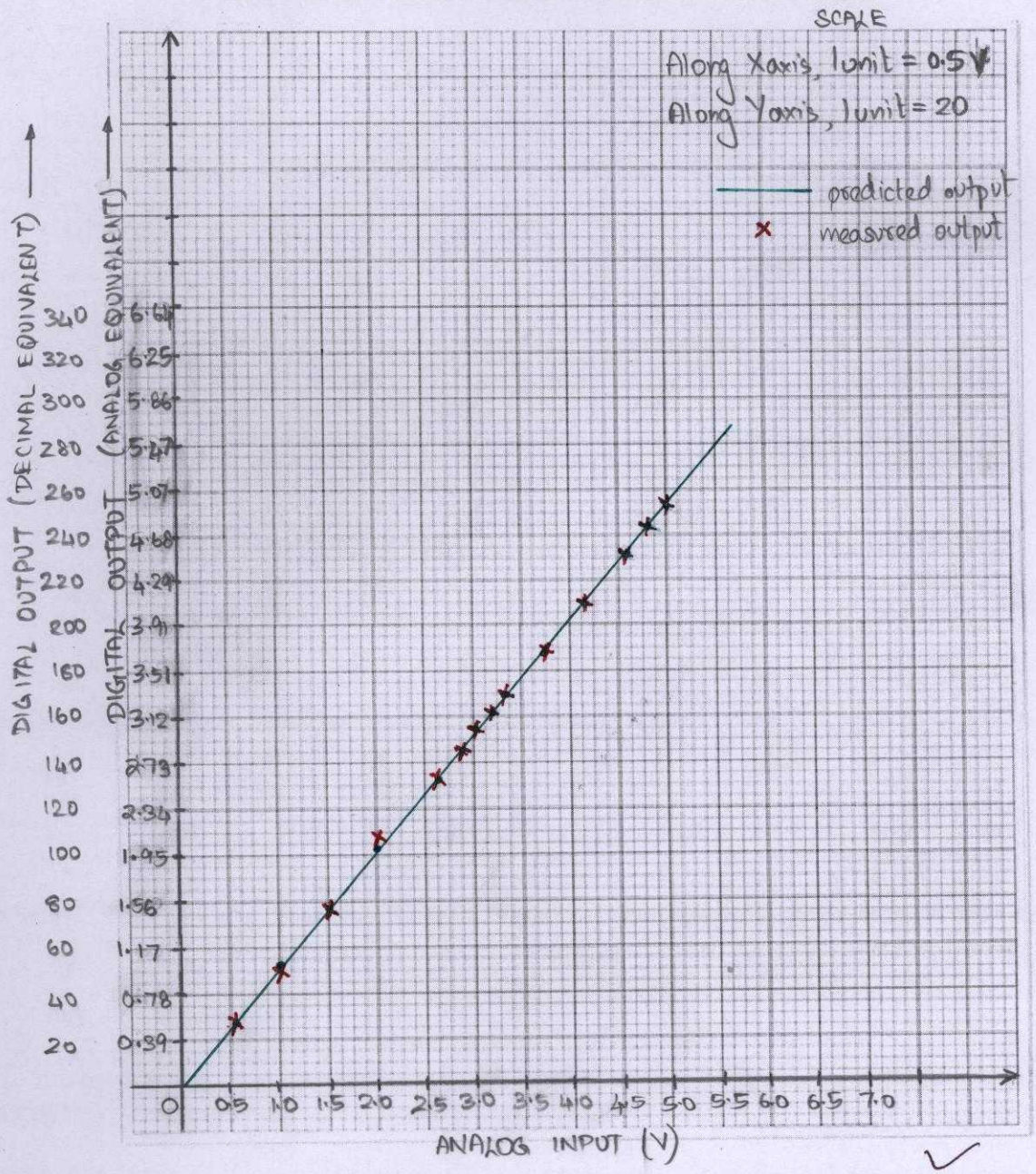
5.3 Plot the transfer characteristics for the ADC0809 using both predicted (continuous line) and your measured data (markers).

VI. INFERENCE/CONCLUSIONS

- The use of an ADC to convert a uni-polar analog signal to a 8-bit digital signal is explored.
- The ADC used was of Successive Approximation Type.
- The clock to this ADC is given using the oscillator operation of two inverters, where the on-time & off-time depend on the R-C charging and discharging times.
- The error in the digital output measured and computed is found to be less than 1% for any input between 0V and Vref. The reason is that the resolution of an 8-bit ADC is high enough.
- The % error can further be reduced by increasing the no. of bits or resolution.

Integrated Circuits Lab		
	Credit	Maximum Marks
Preparation	3 1/2	5
Experimentation	9 1/2	10
Reporting	5	5
Total Marks	18	20

TRANSFER CHARACTERISTICS OF ADC 0809



1.) Resolution = $\frac{1}{2^N}$ p.u

N = 8

∴ resolution = $\frac{1}{2^8}$

= 3.90625×10^{-3} p.u.

$V_{out} = \frac{8}{2^N} V_{ref}$

$5.1 = \frac{255}{256} V_{ref}$

$\boxed{V_{ref} = 5.12V}$

a) $V_{out} = \frac{V_{ref}}{256} \left[\sum_{i=0}^{7} b_i 2^i\right]$

$1 = \frac{5.12}{256} \left[\sum_{i=0}^{7} b_i 2^i\right]$

∴ Digital output : 0011 0010

b) $2.5 = \frac{5.12}{256} \left[\sum_{i=0}^{7} b_i 2^i\right]$

∴ Digital output : 0111 1101

c) $3.4 = \frac{5.12}{256} \left[\sum_{i=0}^{7} b_i 2^i\right]$

∴ Digital output : 1010 1010

d) $4.68 = \frac{5.12}{256} \left[\sum_{i=0}^{7} b_i 2^i\right]$

∴ Digital output : 1110 1010

2) The least measurable voltage would yield a digital output of '1'.

$V_{ref} = 5V$

$V_{out} = 0.0048828\ V$

$$V_{out} = \frac{V_{ref}}{2^N}\ [1]$$

$$2^N = \frac{5}{0.0048828}$$

$$\boxed{N = 10}$$

---

3) All analog to digital conversions require some time in which sampling of the analog waveform is done, and at the sampling rate, the digital output is obtained.

- The clock to the ADC decides the sampling frequency.
- If unclocked, then even before the digital equivalent of an analog input is found, the analog input would have already changed.
- Thus the sample + hold circuit has to be synchronized with the clock pulse to the ADC.

---

4) To select input channel 3 in ADC0809:

AD A : HIGH
AD B : HIGH
AD C : LOW
