**Project 2**

**To implement the simulator for an out-of-order version of the simulator for the APEX ISA.**

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Description

1. The simulated processor makes use of register renaming with three function units, a centralized issue queue, a LSQ, a ROB and a unified register file (URF).
2. The processor uses register renaming with an IQ, ROB and LSQ. A unified register file is used, along with a front-end rename table and a back-end RAT. The issue queue entry holds literal operands and all register operand values in addition to all other relevant information that is needed.

Contributions

1. Discussed the theories and logic behind the code.
2. Once that was done we jotted down points of how to go about with the implementation.
3. Shrey implemented Issue queue and rename table.
4. Aditya implemented LSQ and ROB.
5. Once completed we tested the code on remote.cs.binghamton.edu. tested the test cases sent.