VERILOG AND ITS LEXICAL RULES

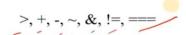
2.4. Identifiers:

- User defined words for variables, function names, module names, block names and instance names
- Begins with a letter or underscore
- Never begins with a number and \$
- Identifiers are case-sensitive in Verilog

2.5. Operators:

- Operators are one, two or sometimes three characters
- Used to performs operations on variables

Example 2.5:



2.6. Verilog Keywords:

- Verilog Language Specific words
- They can not be used as Verilog identifiers

assign, always, case, while, wire, reg, and, or, module, begin, input, output, inout, posedge, negedge

Module #02: Lexical Tokens

```
module myDesign(a_i, b_i, ctrl_i, clk_i, result_o);
                                    input a i;
Verilog Keyword
                                    input b i;
                                                                                                   identifier
                                    input clk i;
                                    input [1:0] ctrl_i;
                                                                                                   Single line comment
                                    output result_o;
                                    reg result o; // Registered Output
  whitespace
                                /* A small ALU operations, based on the ctrl i signal
                                   values */
                                  always @(posedge clk i)
                                                                                                    Multi line comment
                                    begin
                                                                                                     operator
                                      case(ctrl i)
                                         2'b00 : result o \le a i \& b i;
                                         2'b01 : result \ o \le a \ i + 1'b1;
                                         2'b10 : result \ o \le a \ i \mid b \ i;
                                         2'b11 : result \ o \le a \ i * b \ i;
                                                                                                      Number
                                        default : result_o \le a_i;
                                      endcase
                                    end
                                endmodule VLSI Excellence - Gyan Chand Dhaka
22-09-2022
```

https://www.vlsisystemdesign.com/paper-7-top-down-transaction-level-design-with-tl-verilog/ →

