VERILOG AND ITS LEXICAL RULES

2.4. Identifiers :

- User defined words for variables, function names, module names, block names and instance names
- Begins with a letter or underscore
- Never begins with a number and $
- Identifiers are case-sensitive in Verilog

2.5. Operators:

- Operators are one, two or sometimes three characters
- Used to performs operations on variables

Example 2.5:

>, +, -, ~, &, !=, ===

2.6. Verilog Keywords:

- Verilog Language Specific words
- They can not be used as Verilog identifiers

assign, always, case, while, wire, reg, and, or, module, begin, input, output, inout, posedge, negedge

Module #02 : Lexical Tokens

```
module myDesign(a_i, b_i, ctrl_i, clk_i, result_o);
  input a_i;
  input b_i;
  input clk_i;
  input [1:0] ctrl_i;
  output result_o;
  reg result_o; // Registered Output
/* A small ALU operations, based on the ctrl_i signal
   values */
  always @(posedge clk_i)
    begin
      case(ctrl_i)
          2'b00 : result_o <= a_i & b_i;
          2'b01 : result_o <= a_i + 1'b1;
          2'b10 : result_o <= a_i | b_i;
          2'b11 : result_o <= a_i * b_i;
        default : result_o <= a_i;
      endcase
    end
endmodule
```

Verilog Keyword

whitespace

identifier

Single line comment

Multi line comment

operator

Number

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