

# Low-Power 22nm CMOS Operational Amplifier

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**Abstract**—In this report, we design and simulate a low-power CMOS operational amplifier using 22nm technology, suitable for portable electronic systems such as tablets, smartphones, and MP3 players. Specifically, we target an op-amp with  $<1.5\text{mW}$  DC power consumption, a  $+1.0\text{V}$  single power supply with a common-mode voltage of  $V_{CM} = 0.5\text{V}$ , an open-loop differential gain  $>1,500$ , up/down settling times  $<7.0\text{ns}$ , and PSRR+ and CMRR noise rejection  $>40\text{dB}$ . To achieve these goals, we first extract transistor parameters such as transconductance, intrinsic gain, saturation voltage, and transit frequency for different channel length transistors. Using the extracted parameters, we develop a hand-calculated model to guide the design of a two-stage differential-to-single-ended operational amplifier. Finally, we verify that the proposed design meets the specifications through SPICE simulation.

**Index Terms**—Operational Amplifier, Low-Power Op-Amp, Intel 22nm CMOS Process

## I. INTRODUCTION

Operational amplifiers (op-amps) are fundamental components in the design of complex analog circuits, including Analog-to-Digital and Digital-to-Analog Converters. Recently, low-power operational amplifiers have gained importance in portable electronic systems such as tablets, smartphones, and MP3 players. Additionally, low-power op-amps are increasingly researched for use in mixed-signal circuits since: (1) The supply voltage continuously decreases with a scaling CMOS technology [1], [2]; (2) The power consumption of mixed-signal ICs are often dominated by analog components [3], [4].

In this paper, we present the design of a low-power operational amplifier using a 22nm CMOS process. The supply voltage ( $V_{DD}$ ) is set to  $+1.0\text{V}$ , with a common-mode voltage ( $V_{CM}$ ) of  $0.5\text{V}$ . The design targets the following minimum specifications:

- **DC Power Consumption:**  $<1.5\text{mW}$ .
- **DC Small Signal Differential Gain ( $A_{vd}$ ):**  $>1,500$  (measured in open-loop with a load capacitance of  $C_L = 0.5 \text{ pF}$ ).
- **Phase Margin:**  $>60^\circ$  with a  $1 \text{ pF}$  load at a feedback factor  $f = 0.5$  (corresponding to a gain-of-2 crossover).
- **Output Swing:** Within  $0.2\text{V}$  of both  $V_{DD} = 1.0\text{V}$  and  $\text{AGND} = 0.0\text{V}$  (measured in open-loop and defined as the maximum output range where the incremental gain  $v_o/v_{id} > 500$ ).
- **PSRR+ and CMRR:**  $>40\text{dB}$  from DC to 10 MHz with an input common-mode voltage of  $V_{IC} = 0.5\text{V}$ .

- **Thermal Noise:**  $<250\mu V_{rms}$  integrated from 1MHz to 500MHz (output-referred, using the configuration in Fig. 1).
- **Maximum Settling Time:**  $<7.0\text{ns}$  (both rise and fall) to within 0.5% of the output step size ( $0.2\text{V}$ ) for a square wave input with  $V_{IL} = 0.4\text{V}$ ,  $V_{IH} = 0.6\text{V}$ , and an input transition time of 10 ps.

This design is optimized to balance low power consumption, stability, and performance, making it suitable for modern low-voltage applications. The following sections provide further details on the circuit schematic, hand analysis, and simulation results.

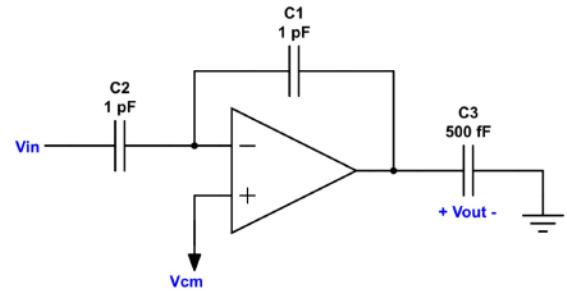


Fig. 1: Testbench Configuration with Feedback  $\beta = \frac{1}{2}$ .

## II. PARAMETER EXTRACTION

As shown in Fig. 2, we first extract the approximate p- and n-channel transistor characteristics using Cadence Simulation. Note that the actual small-signal parameters change over the DC operating point sweep. We ignore such variances for hand calculations since our goal is to predict the circuit functionality within an order of magnitude error from the SPICE simulation. Therefore, second-order changes in small-signal parameters are not considered during the analysis.

Additionally, we approximate that the transistor current scales linearly with its width ( $W$ ), meaning  $I_D/W$  remains constant since the transistor is very wide ( $W \gg L$ ). To simplify our testbench, we use a fixed-width transistor ( $W = 1 \mu\text{m}$ ) and scale linearly for different widths.

The  $g_m$  vs.  $I_D$  measurements are shown in Fig. 2a and 2d. We use a fixed  $|V_{DS}| = 600 \text{ mV}$  to ensure transistors operate in the saturation region, then sweep  $V_{gs}$  to measure the current and transconductance. To measure the intrinsic gain  $g_m r_o$ , we assess the common-source amplifier gain with an ideal DC current source connected to the drain. The intrinsic

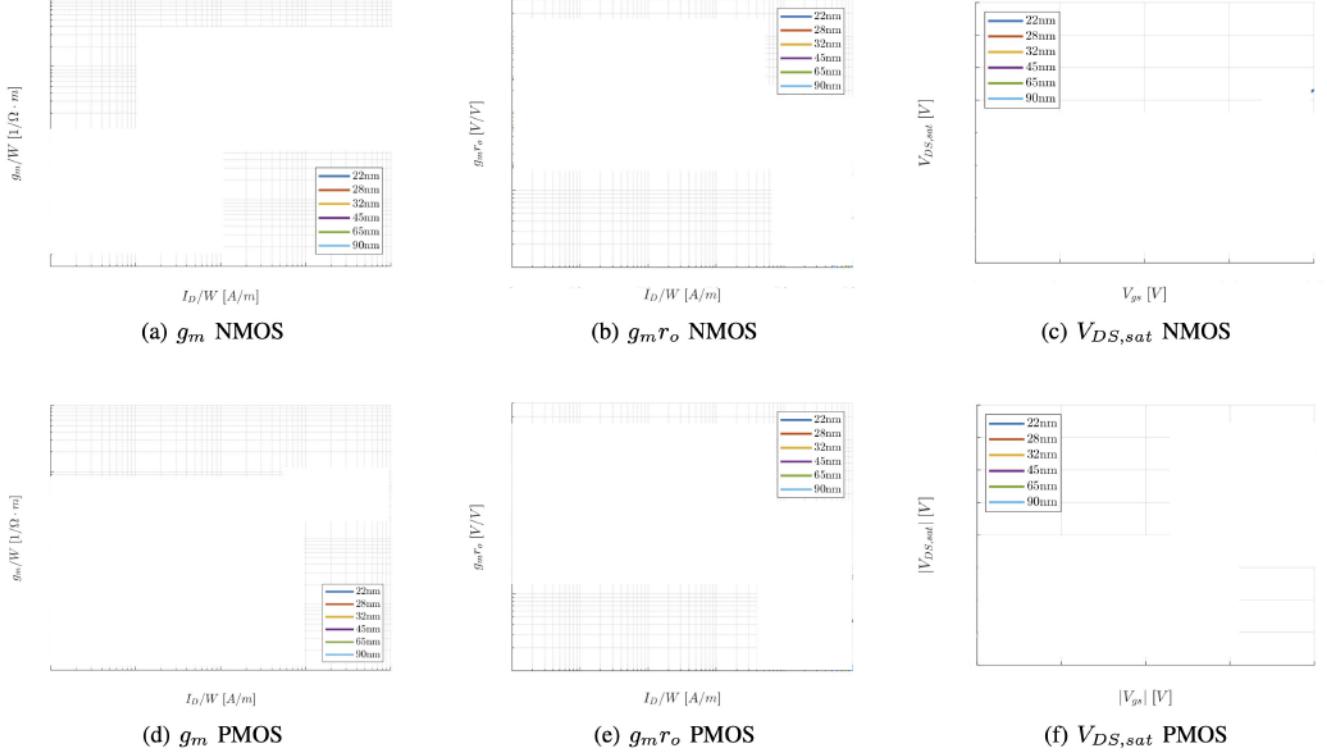


Fig. 2: Extracted Transistor Characteristics.

gain remains constant in weak inversion and declines as the transistor approaches strong inversion. This behavior is opposite to that of the transconductance  $g_m$ , which increases as the device moves closer to strong inversion. Consequently, we aim to operate transistors midway between their weak and strong inversion regions to achieve both high gain and speed.

Operating transistors in weak inversion is also advantageous for voltage headroom. As shown in Fig. 2c and 2f, the overdrive voltage  $V_{DS,sat}$  is lower in weak inversion. Since transistors must remain in saturation, a sufficient overdrive voltage is necessary for every  $|V_{DS}|$ , which can significantly reduce the voltage swing, especially given the low supply voltage of  $V_{DD} = 1V$ .

Finally, we measure the channel-length modulation parameter  $\lambda$  over a wide range of drain currents:  $I_D/W = 50, 100, 200 [A/m]$ . For  $L = 90 nm$  devices,  $\lambda$  remains approximately constant regardless of drain current, with  $\lambda_n \approx \boxed{\times} [1/V]$  for NMOS and  $\lambda_p \approx \boxed{\times} [1/V]$  for PMOS transistors.

### III. CIRCUIT DESIGN AND ANALYSIS

#### A. Circuit Schematic

Fig.3 shows the circuit schematic of the proposed two-stage differential-input, single-ended operational amplifier. The circuit is mainly divided into four parts: the current source, the first and second stage amplifiers, and the gate biasing circuitry. The transistor widths are shown in Tab.I, with values normalized to  $W_0 = 66 \mu m$ . We use  $L = 90 nm$  transistors,

a  $1.24 k\Omega$  resistor for the current source, and  $C_C = 1.2 pF$  and  $R_Z = 150 \Omega$  for pole splitting.

All bias currents are generated using diode-connected transistors (M6 and M6N) and a resistor (R1) serving as a simple current source. As discussed in Section V, the output current of this circuitry is heavily dependent on the supply voltage, leading to reduced PSRR. The current source output is mirrored by transistor M7 to power the first-stage actively-loaded cascode amplifier.

For biasing, the input transistors (M1 and M2) are set by the common-mode input voltage,  $V_{CM} = 0.5V$ . The load transistors (M3 and M4) utilize negative feedback on their tied gates to stabilize the gate voltage. The gate voltages of the cascode transistors (M1B, M2B, M3B, and M4B) are set using a separate biasing circuit. Finally, we use common-source configuration for 2nd-stage amplifier (M5 & M8) with  $R_Z$  and  $C_C$  for pole splitting and eliminating a Right Half Plane (RHP) zero.

#### B. Hand Analysis

1) *Thermal Noise Estimation:* We derive the thermal noise of our op-amp design to determine the compensation capacitance  $C_C$ . Specifically, shot noise  $i^2 = 2qI_D\Delta f$  represents the device in weak inversion, where it depends on carriers jumping the potential barriers to create a diffusion current. We only consider the input-referred voltage noise, ignoring current noise since the source impedance  $R_s \ll 1/[\omega(C_{GS} + C_{GD})]$ .

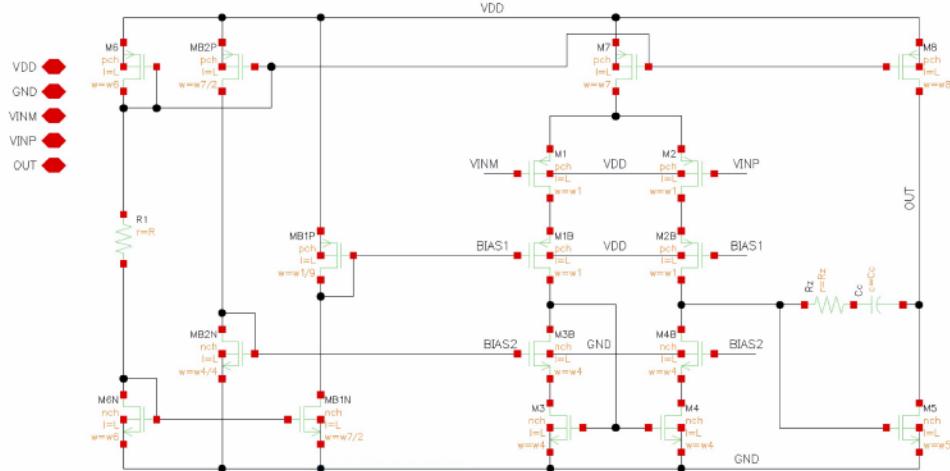


Fig. 3: Circuit Schematic.

TABLE I: Transistor Width (1 a.u. =  $66\mu m$ )

Name	W [a.u.]	Name	W [a.u.]
M1/1B	1	MB1P	1/9
M2/2B	1	MB1N	1
M3/3B	1	MB2P	1
M4/4B	1	MB2N	1/4
M5	4	MB6/6N	1/3
M8	4	M7	2

The input shot noise for a MOS transistor is:

$$\overline{i_d^2} = \frac{\overline{i_d^2}}{g_m^2} = \frac{2qI_D}{g_m^2} = \frac{2nk_BT}{g_m}. \quad (1)$$

We can substitute the total input-referred noise  $\overline{v_{iT}^2}$  as the sum of the noise from transistors in Fig. 3. Compared to the second stage, the first-stage transistors with higher voltage gain will dominate the noise. Specifically, the transistors in the cascode amplifier's signal path (M1/M1B, M2/M2B, M3/M3B, M4/M4B) with high transconductance contribute significantly to the noise. Assuming the noise sources are independent, we derive the total input-referred noise using:

$$\overline{i_o^2} = g_{m1}^2 \overline{v_{iT}^2} = \sum g_{mj}^2 \overline{v_{eq,j}^2}, \quad (2)$$

for  $j \in [1, 1B, 2, 2B, 3, 3B, 4, 4B]$ . Thus the spectral noise profile of 2-stage cascode op-amp is:

$$S_i(f) = \frac{\overline{v_{iT}^2}}{\Delta f} = 8nk_BT \left( \frac{1}{g_{m1}} + \left( \frac{g_{m3}}{g_{m1}} \right)^2 \frac{1}{g_{m3}} \right) \approx \frac{16nk_BT}{g_{m1}}. \quad (3)$$

We measure the output-referred noise using the configuration in Fig. 1 with a feedback factor  $\beta = 0.5$ . Since the op-amp's open-loop transfer function can be approximated as  $A(f) = \frac{f_1}{jf}$ , the total output-referred noise is calculated as:

$$\overline{v_{therm}^2} = \int_0^\infty \frac{S_i(f)}{(1 + (f_1\beta/f)^2)} df = \frac{mB}{4\beta} \frac{k_BT}{C_C} < (250\mu V)^2, \quad (4)$$

with a  $m \approx 4$  factor for noise contribution from other devices (including the contribution from Equation 3) and  $B = 4n \approx 6$ . Equation (4) leads to  $C_C > 0.80 \text{ pF}$ . During the design process, this approximate value was used as an initial reference, which resulted in using  $C_C = 1.2 \text{ pF}$ .

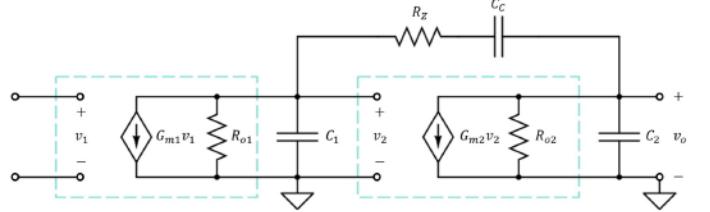


Fig. 4: Op-amp AC Equivalent Circuit.

2) *Bandwidth and Phase Margin:* We model our op-amp using the small-signal equivalent circuit shown in Fig. 4 to estimate its functionality. In the schematic, the op-amp is divided into the first and second-stage amplifiers, with parasitic capacitances  $C_1$  &  $C_2$ , compensation capacitor  $C_C$ , and resistor  $R_Z$ . To meet the gain-of-2 bandwidth  $w_2 > 50MHz$ , we get:

$$\omega_1 = \frac{g_{m1}}{C_C} = \frac{w_2}{\beta} > 2(2\pi \cdot 50MHz) \Rightarrow g_{m1} > 0.754[mV], \quad (5)$$

To satisfy the phase margin  $\Phi > 60^\circ$ , the crossover frequency  $w_c$  should approximately be half the op-amp's second pole  $|p_2|$ , and therefore:

$$\omega_1 = \frac{g_{m1}}{C_C} < \frac{|p_2|}{2} = \frac{g_{m5}}{2C_2} \Rightarrow C_C > \frac{2g_{m1}}{g_{m5}} C_2. \quad (6)$$

3) *Right Half-Plane (RHP) Zero Cancellation:* The compensation capacitor  $C_C$  creates a RHP zero  $z$ , which can degrade the phase margin at high frequency. The nulling

TABLE II: Simulation Result

Category	Requirement	SPICE Simulation
$P_{DC}$	< 1.5mW	1.18mW
$A_{vd}$	>1,500	59,000
Phase Margin $\Phi$	> 60°	75°
Output Swing	> 600mV	935mV
PSRR+ (10MHz)	> 40dB	33.5dB
CMRR (10MHz)	> 40dB	46.8dB
Thermal Noise	< 250μV	230.1μV
Settling Time (up/down)	7.0/7.0ns	5.52/6.99ns

resistor  $R_Z$  is connected in series to eliminate the RHP zero by:

$$z = \frac{1}{C_C(|G_{m2}|^{-1} - R_Z)} < 0 \Rightarrow R_Z > \frac{1}{|G_{m2}|} \approx 134\Omega. \quad (7)$$

During SPICE simulation, we use a slightly larger  $R_Z = 150\Omega$  to create a LHP zero which improves the phase margin.

4) DC Small Signal Differential Gain: With a drain current density  $I_D/W = 1.60$  [A/m], we estimate the transconductance and intrinsic gain of transistors using Fig. 2a & 2d:

$$\frac{g_m}{W} \approx \boxed{\text{NMOS}}, \boxed{\text{PMOS}} [\text{U}/\text{m}], \quad (8)$$

$$g_m r_o \approx \boxed{\text{NMOS}}, \boxed{\text{PMOS}} [\text{V}/\text{V}]. \quad (9)$$

The transconductance of the amplifier stages are determined by input transistors:  $G_{m1} = g_{m1} \approx \boxed{\text{NMOS}} [\text{mU}]$ ,  $G_{m2} = g_{m5} \approx \boxed{\text{PMOS}} [\text{mU}]$ . The output resistances are calculated using cascode & common-source amplifier equation:

$$R_{o1} = (g_{m1} r_{o1}^2) \parallel (g_{m3} r_{o3}^2) \approx \boxed{\text{MΩ}}, \quad (10)$$

$$R_{o2} = r_{o5} \parallel r_{o8} \approx \boxed{\text{kΩ}}. \quad (11)$$

Therefore, the total gain is estimated as:

$$A_{vd} = (G_{m1} R_{o1}) \cdot (G_{m2} R_{o2}) \approx 2.0 \times 10^5 [\text{V}/\text{V}] = 106 [\text{dB}]. \quad (12)$$

#### IV. SIMULATION AND RESULTS

The SPICE simulation results and minimum design requirements are summarized in Tab.II. The open-loop frequency response is shown in Fig.5. The simulated DC small-signal gain is 9.7 dB lower than the hand analysis result, primarily because the first-stage gain was overestimated due to the idealized approximation of the cascode output resistance.

Fig. 6 depicts the DC output voltage corresponding to the differential input  $V_{in,diff}$ . Defining the valid operating region as the range where the DC small-signal gain is greater than 500, the condition is satisfied within  $-83.8 \mu\text{V} < v_{id} < 59.9 \mu\text{V}$ , resulting in an output voltage range of [36.7 mV, 971.7 mV]. Consequently, the maximum output voltage swing is 935 mV.

The common-mode and power-supply rejection ratios are shown in Fig. 7. At a 10 MHz input frequency, the CMRR

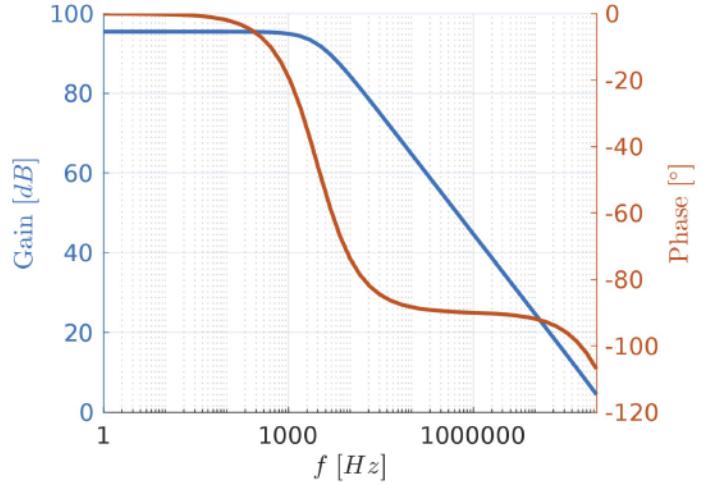


Fig. 5: Op-amp Open-loop Frequency Response (Gain and Phase).

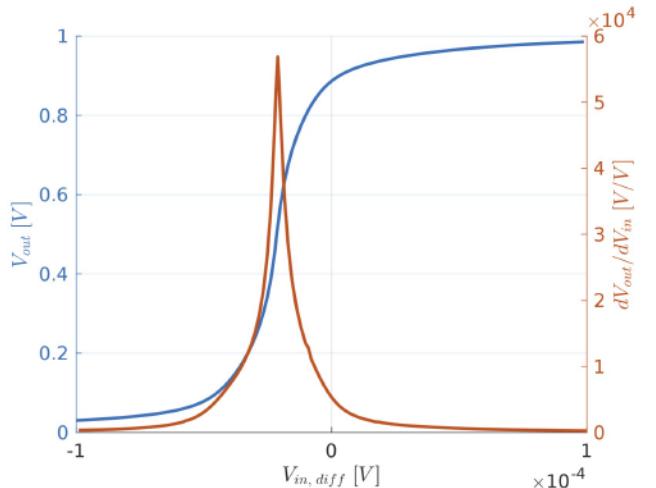


Fig. 6:  $V_{out}$  vs.  $V_{in, diff}$  Response.

is 46.7 dB, and the PSRR+ is 34.5 dB. However, the power-supply rejection does not meet the design specification. This is because the current source is implemented using a simple series of diode-connected transistors and a resistor, causing the current output to scale linearly with the supply voltage. Since all circuit biasing depends on the current source, its high sensitivity to supply voltage results in a significant reduction in PSRR+.

Finally, the settling time of the op-amp under a 200 mV voltage step up/down is shown in Fig. 8. Although a phase margin of  $> 65^\circ$  theoretically ensures a stable step response, the actual settling time is limited by the slew rate, given by  $SR = \min(I_{D7}/C_C, I_{D8}/(C_C + C_2))$ . Therefore, to enhance the settling time, we consider increasing  $g_{m5}$ ,  $I_{D5}$ , and  $I_{D7}$  at the cost of increased power consumption.

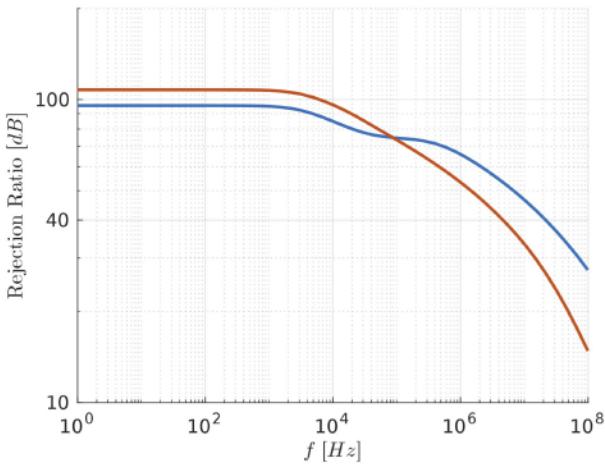


Fig. 7: Common Mode and Power Supply Rejection Ratio.

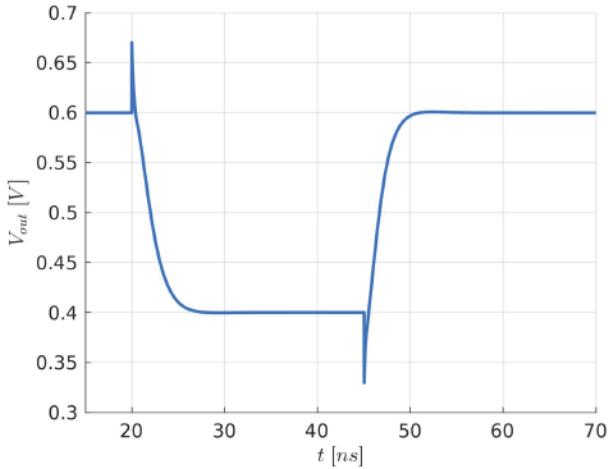


Fig. 8: Op-amp  $\beta = \frac{1}{2}$  Negative Feedback Step Response. Settling time defined as minimum time for the output to stabilize within  $\pm 0.5\%$  of the voltage jump.

## V. CONCLUSION

In this paper, we designed a low-power operational amplifier using a 22nm CMOS process. Through SPICE simulations, we evaluated key performance metrics, including small-signal gain, output voltage swing, common-mode rejection ratio (CMRR), power-supply rejection ratio (PSRR+), and settling time. While the design met most specifications, the PSRR+ fell short due to the limitations of the simple current source implementation. Additionally, the actual small-signal gain was lower than predicted by hand analysis, primarily due to the idealized assumptions in the cascode output resistance estimation.

To improve performance, future work could focus on enhancing the current source with higher stability for better power supply rejection ration. In addition, transistor sizing could be further optimized by using different  $W/L$  ratio. Specifically, instead of driving every transistor with the same

current density ( $I_D/W$ ), a broader design space could be explored by using different current densities to each transistor. For instance, increasing the transconductance of M1 relative to M3 ( $g_{m1} > g_{m3}$ ) could effectively reduce thermal noise, as described in Equation (3). Despite these limitations, this work demonstrates the low-power op-amp design with high gain and stability for mixed-signal applications.

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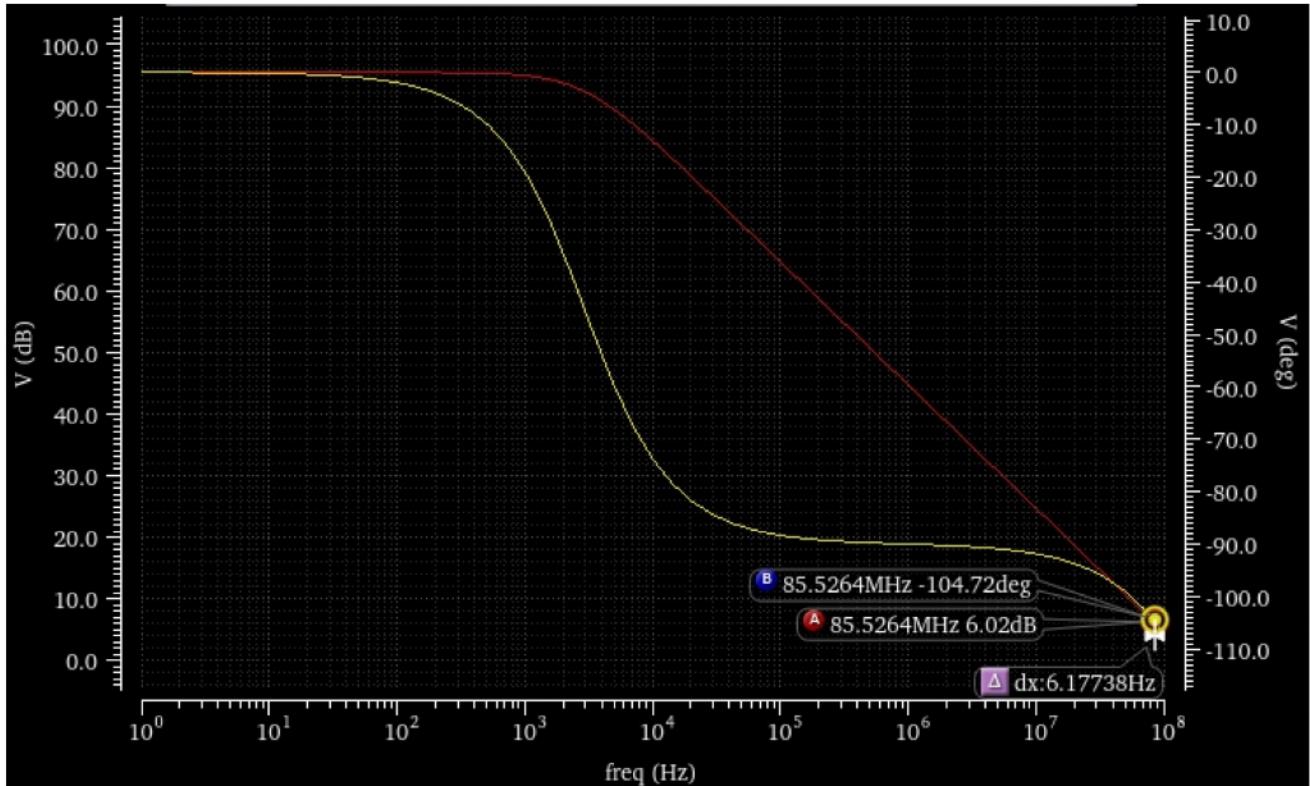


Fig. 9: Open-Loop Gain and Phase.

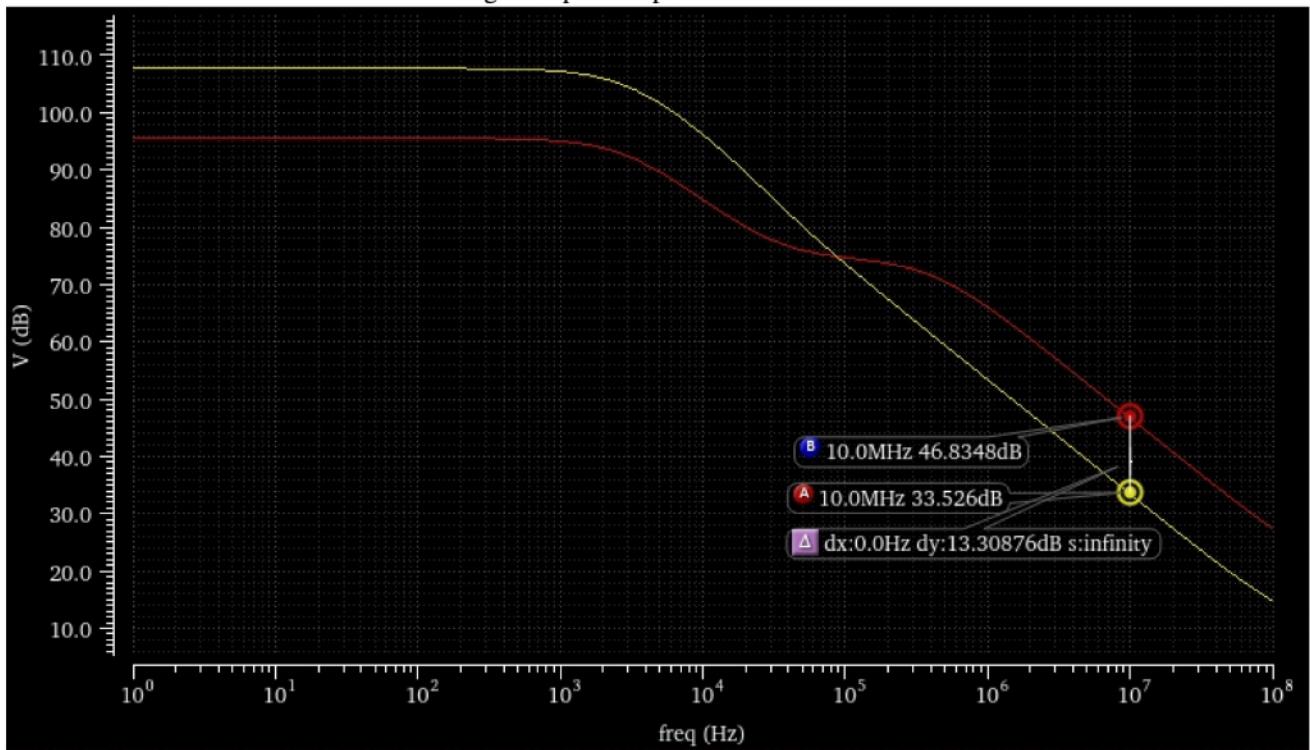


Fig. 10: Rejection Ratio.

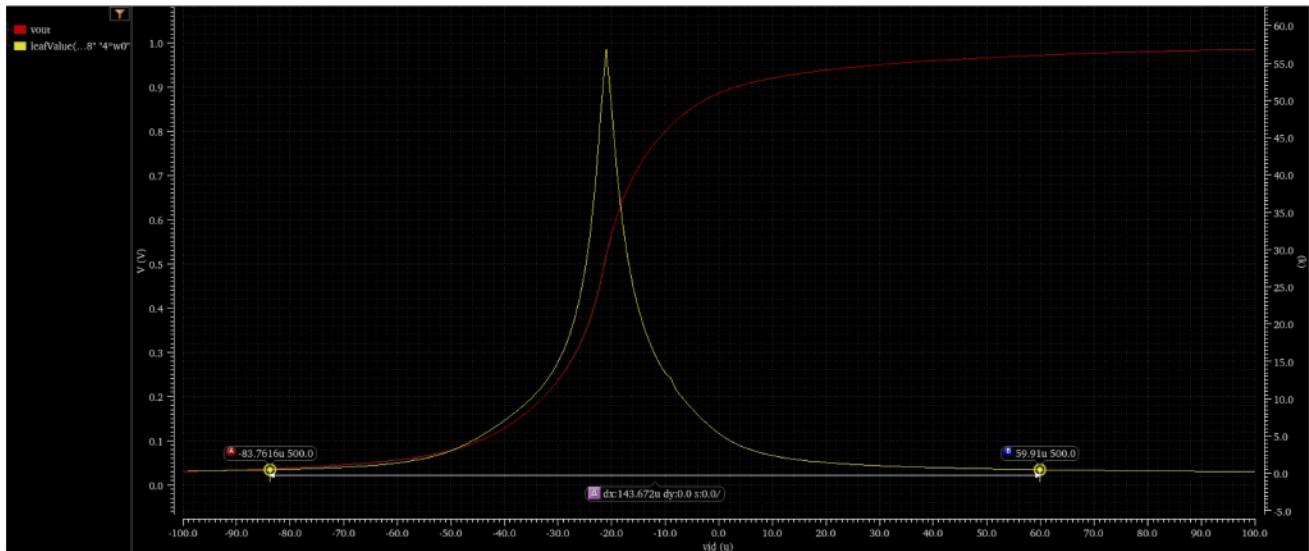


Fig. 11: Differential Input Range for Gain  $> 500$ .

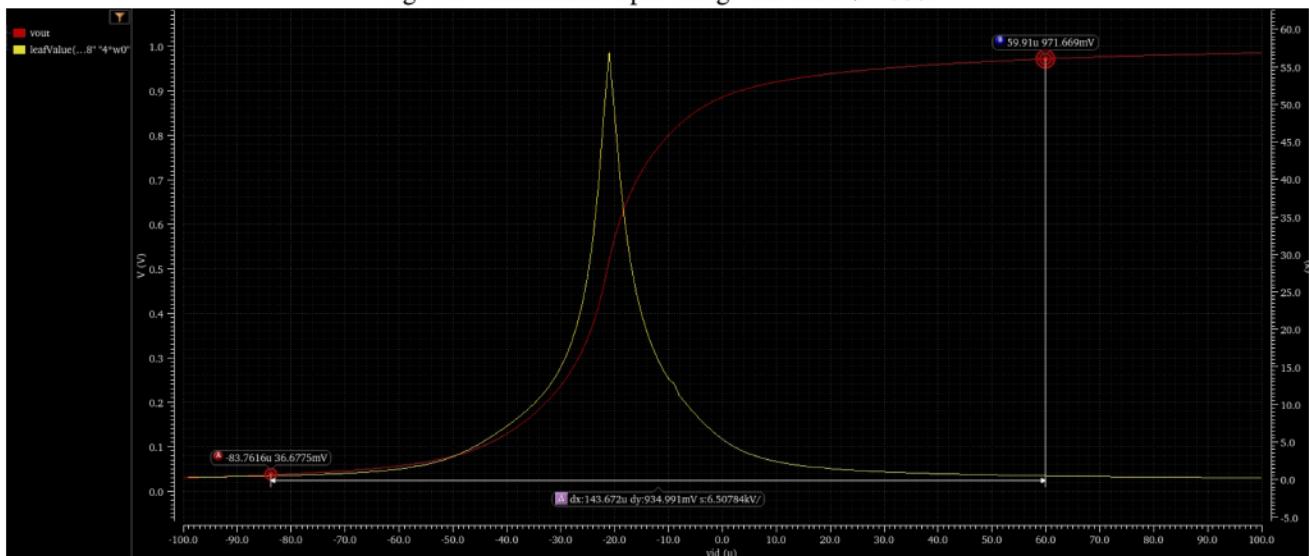


Fig. 12: Output .

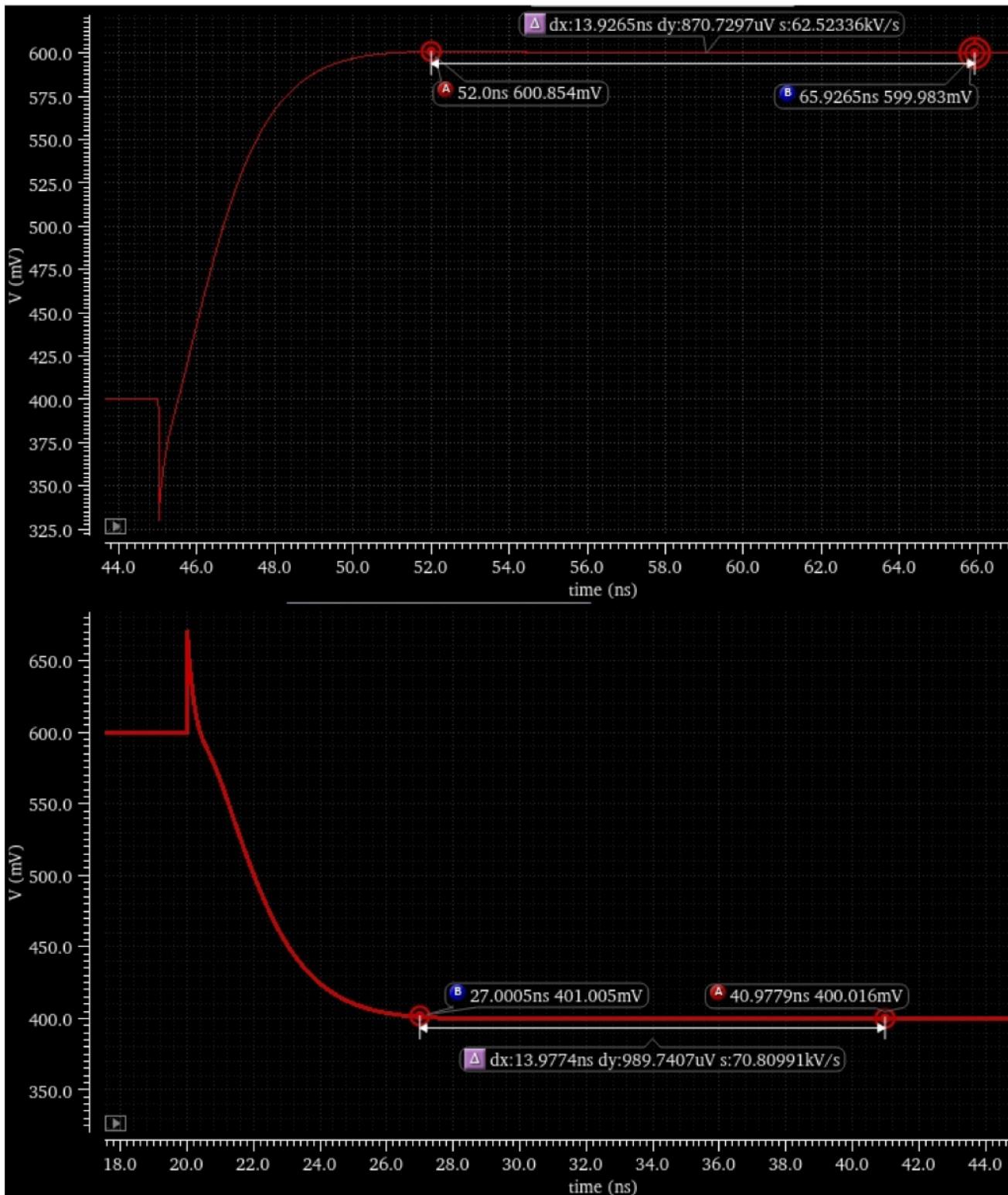


Fig. 13: Step-Response Rise/Fall Settling Time.