

Unit-5

## Microprocessor - II

Q. Write and explain instruction set in 8086 micro processor

Ans: Instruction set in 8086 microprocessor

- (i) Data Copy / Transfer Instruction
- (ii) Arithmetic / Logical Instruction,
- (iii) Branch Instruction.
- (iv) Loop Instruction.
- (v) Machine Control Instruction.
- (vi) Shift / Rotate Instruction.
- (vii) Flag Manipulation Instruction.
- (viii) String Instruction.

The 8086/8088 instructions are categorized into the following main types. This section explains the function of each of the instructions with suitable examples wherever necessary.

(i) Data Copy / Transfer Instructions:

This type of instructions are used to transfer data from source operand to destination operand. All the store, move, load, exchange, input and output instructions belong to this category.

(ii) Arithmetic and Logical Instructions:

All the instructions performing arithmetic, logical, increment, decrement, compare and scan instructions belong to this category.



### (iii) Branch Instructions:-

These instructions transfer control of execution to the specified address. All the call, jump, interrupt and return instructions belong to this class.

### (iv) Loop Instructions:-

If these instructions have REP prefix with CX used as count register, they can be used to implement unconditional and conditional loops.

The LOOP, LOOPNZ and LOOPZ instructions belong to this category. These are useful to implement different loop structures.

### (v) Machine Control Instructions:-

These instructions control the machine status. NOP, HLT, WAIT and LOCK instructions belong to this class.

### (vi) Flag Manipulation Instructions:-

All the instructions which directly affect the flag register, come under this group of instructions. Instructions like CLD, STD, CLI, STI, etc. belong to this category of instructions.

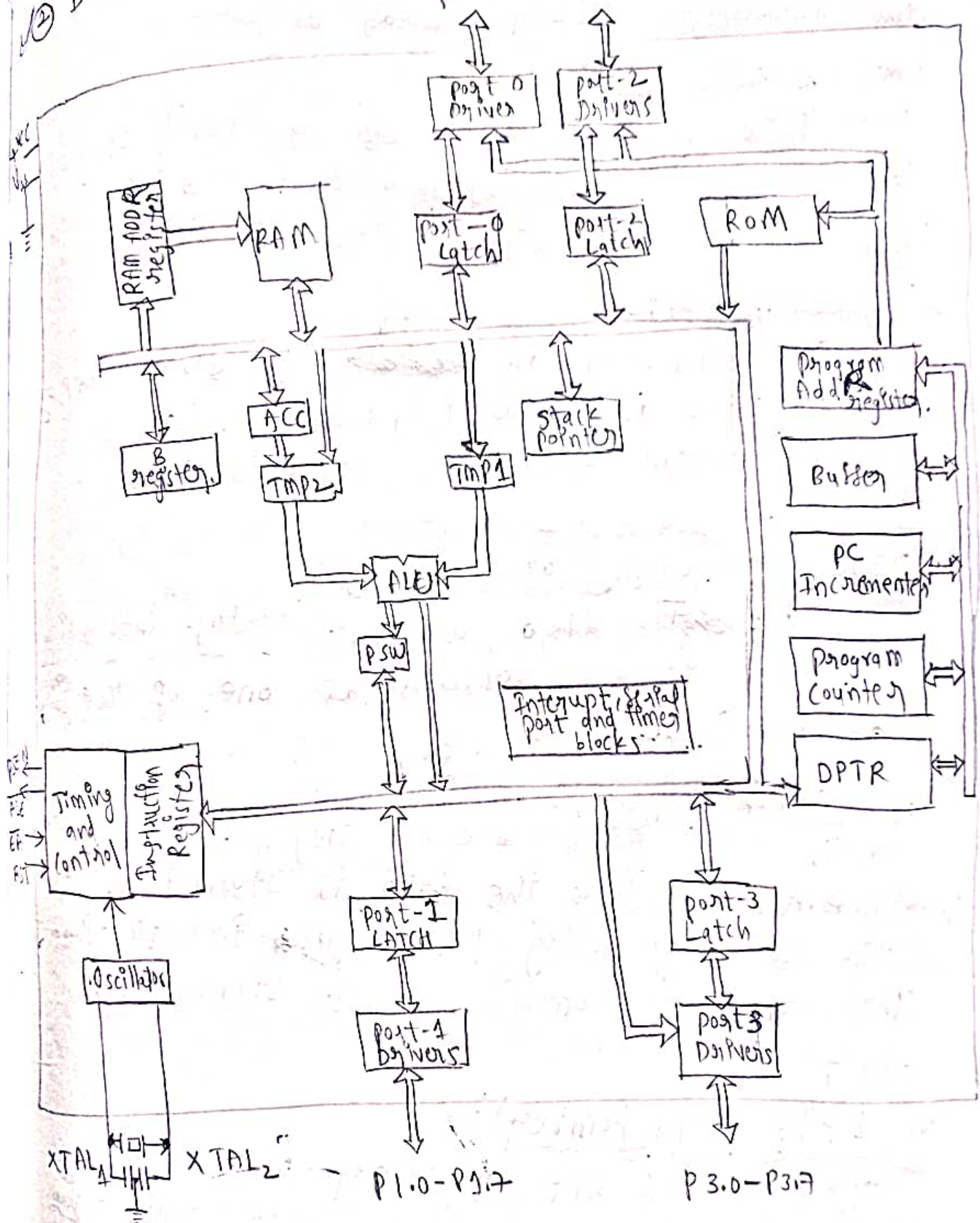
### (vii) Shift and Rotate Instructions:-

These instructions involve the bitwise shifting (or rotation either direction) with or without a count in CX.

### (viii) String Instructions:-

These instructions involve various string manipulation operations like load, move, scan, compare, store, etc. These instructions are only to be operated upon the strings.

② Draw and explain 8051 micro controller ?





The internal architecture of 8051 is representing the functional description as follows

(i) ACC (Accumulator):-

This may be acts as operand register either implicit, <sup>or</sup> specified in the instructions. This is on chip special function register.

(ii) B. Register:-

This register is <sup>used</sup> ~~not used~~ to store one of the operands for multiply and division instruction and considered as special function register.

(iii) PSW (Program Status) Word:-

The <sup>set</sup> ~~reg~~ of flags contains the status information and is ~~not~~ considered as one of the special function registers.

(iv) Stack Pointer:-

This is 8-bit ~~wide~~ register is incremented before the data is stored on to the stack using push/pop instructions. This register contain 8-bit stack top address.

(v) DPTR (Data Pointer):-

This is 16 bit register contains a higher byte DPH and lower byte DPL of a 16 bit external data RAM address.

(vi) Port '0' to 3 Latches and Drivers:  
These 4 latches and drivers pairs are allotted to each of the 4 on chip IO ports. These latches have been allotted addresses in the special function register, using the allotted addresses. The user can communicate and identified as  $P_0, P_1, P_2, P_3$  and  $P_3$ .

(vii) Serial Data Bytes:  
This consisting of (a) Transmit Buffer: which is necessary a parallel in serial out (PISO) register. (b) Receive Buffer: This is a serial in parallel out register. (SIPD)

(viii) Timer Registers:  
The two 16-bit registers can be accessed as their lower and upper bytes  $TL0, TH0$  for register '0'.  
Similarly  $TL1$  and  $TH1$  represents lower and higher bytes of timing register '1'.

(ix) Control Registers:  
The special function registers IP, IE, TMOD, T-COM, S-COM and P-COM contain control and status information for interrupts/.

Timers / Counters



### (X) Timing and Control Unit

This derives all the necessary timing and control signals required for the internal operation of the circuit. It also derives control signals required for controlling the external system bus.

### (Xi) Oscillator:-

The circuit generates the basic timing clock signals for the operation of the circuit using the crystal oscillator.

### Instruction Register:-

This register decodes the opcode of an instruction to be executed and gives information to the timing and control unit to generate necessary signals for the execution of the instruction.

### EPROM and program address Register:-

This provides on-chip EPROM and mechanism to internally address it.

### RAM and RAM address register:-

This block provides internal 128-bytes RAM and a mechanism to address it internally.

### ALU:-

The Arithmetic and Logic Unit performs 8-bit arithmetic and logical operations over the operands held by the temporary registers (temp-1 and temp-2). But user can not access these temporary registers.

## SFR Register Bank:-

SFR = Special Function Register.

This is a set of SFRs, which can be addressed using their respective addresses, which lie in the range 80H to FFH.

Finally the interrupt, serial port and timer units control and perform their specific functions under the control of timing and control unit.

Write 8051 Instruction set supports addressing modes.

- Ex: (i) Direct Addressing Mode  
(ii) Indirect Addressing Mode  
(iii) Register Addressing Mode  
(iv) Register Specific Addressing Mode  
(v) Immediate Addressing Mode  
(vi) Indexed Addressing Mode
- $DIR^2 I^2$

### Direct Addressing Mode:-

In this the operands are specified using the 8-bit address field in the instruction format only. Internal data RAM and SFRs can directly address.

Ex: MOV R<sub>0</sub>, 89H.

Here 89H is address of a special function register.  
T-mode



#### 4 Indirect Addressing Mode:-

In this mode of addressing the 8-bit address of an operand is stored in a register and the 8-bit address is present in a register. This specified in the instruction the register  $R_0$  and  $R_1$  of the selected bank of register (or SP) can be used as the address registers. For storing the 8-bit address. The address register for 16-bit address can only be data pointer (DPTR).

~~Register~~ Ex: `ADD A, @R0`

#### Register Addressing Mode:-

In this addressing mode operands are stored in the registers  $R_0 - R_7$  of the selected register bank one of these 8-registers  $R_0$  to  $R_7$  is specified in the instruction using 3-bit specification field of the opcode format.

Ex: `ADD A, R3` or `MOV A, R3`.

#### Register Specific Instruction Addressing Mode:-

In this type of instructions the operand is implicitly specified using one of the registers.

Ex: `RLA` (ROL).

This instruction rotates accumulator content left.

#### Immediate Addressing Mode:-

In this an immediate data that is a constant is specified in the instruction after the opcode byte. Ex: `MOV A, #100H`



## Indexed Addressing Mode:-

Only program memory accessed using this addressing mode. This addressing mode is used in 8051 for look up table manipulations.

Program counter and DPTR are allowed 16-bit storage registers. These point to the base of lookup table and the accumulator register contents a code to be converted using look up table.

Ex: `MOV CA, @A+DPTR`

`JMP @A+DPTR`

4) Describe instruction set of 8051

- Sol: (i) Data Copy Instruction (as Data Transfer Instruction)  
(ii) Arithmetic Instruction  
(iii) Logical Instruction  
(iv) Branch Instruction  
(v) Bit Processing Instruction

## Data Copy Instruction:-

Data transfer instructions move the content of one register to another. The register content of which is moved remains unchanged. If they have suffix 'X'.

`MOV X` The data is exchanged with external memory.

Ex: `MOV A, Rn`

`MOV A, @Ri`

`MOV @DPTR, A`

MOV @DPTR, A

This indicates accumulator to external RAM 16-bit address.

### Arithmetic Instructions:

This performs several basic operations such as addition, subtraction, division, multiplication etc.

After execution of this instructions the result is stored in the first operand.

Ex: ADD A, R<sub>1</sub>

The result of addition  $A + R_1$  will be stored in the accumulator.

Ex: ADD A, #DATA

INCA .

INC R<sub>n</sub>

### Logical Instructions:

These performs logic operations upon corresponding bits of two registers - AND, OR, X-OR. etc. on logic instructions. After execution the result is stored in the first operand.

Ex: ORL A, @R<sub>i</sub>.

① XRL A, R<sub>n</sub>.  $\Rightarrow$  X-OR register to accumulator performed by this instruction

### Branch Instruction:-

In this branch instruction

$\rightarrow$  Unconditional jump:-

Upon the execution of a jump to a new location from where the program



continuous execution is executed.

### a) Conditional Jump:-

This is a jump to a new program location is executed only if a specified condition is met. Otherwise the program normally proceeds with the next instruction.

Ex: A call address 11.

[<sup>↓</sup>Absolute subroutine call] [Long subroutine call]

L call address 16

NOP (No operation).

### Bit processing Instruction:-

Similar to logic instructions bit oriented instructions perform logic operations. The difference is that these are performed upon single bit.

Ex: CLRC (Clear carry flag)

SETBC (Sets <sup>the</sup> carry flag)

CPLC. (Compliment the carry flag).

### 8051 IO ports and memory organization:-

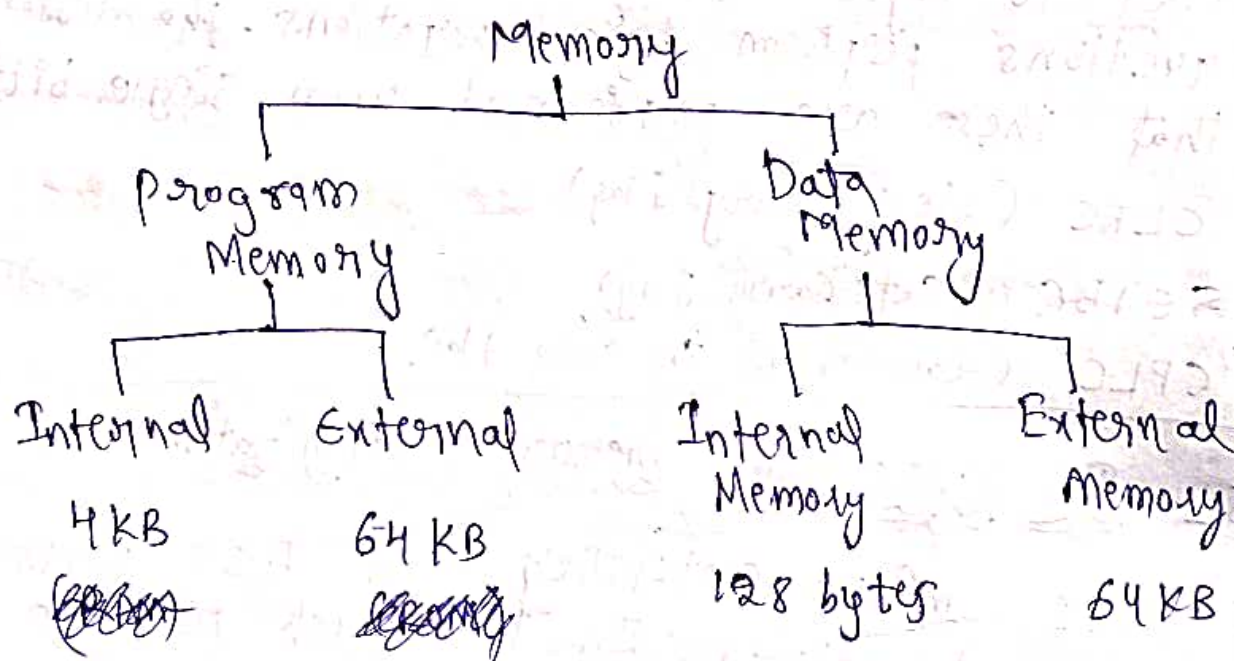
The 8051 micro controller has 4 IO ports drivers and latches. In this each port is of 8-bit and this is configured as input and output ports. By this there is 32 input/output pins allowed to the micro controller to be connected with the peripheral devices. The pin can be configured as "one" for input and "zero" for o/p.

as the logic state.

### Memory Organization:-

The memory is organized logically into program memory and data memory separately. The technique of organizing program and data memory with separate physical addresses is called Harvard Architecture.

The program memory is read only type, the data memory is organized as read/write memory again program and data memories can be within the chip or outside.



Intel 8051 has 128 bytes of RAM, 4KB of ROM within the chip.

The address bus of 8051 is 16 bits wide. So, it can access  $2^{16} = 64 \text{ KB}$  of memory in program and in data.



A user can configure program memory 4 KB, 60 KB inside and outside respectively in the chip. Internal data memory accessed with 8-bit address and external data memory with 16-bit address. So, the maximum data memory that can be connected to the 8051 system is 64 KB.

### Procedures and Macros:

Procedure and Macros are two concepts in assembly language programming.

#### Macro:

Macro is a set of instructions and small (less than 10). The programmer can use it any where in the program by its name and used multiple times whenever required with the help of macro. These are not follow call-return method. Assembly directive MACRO is used to define macro, ENDM used after completion.

#### Procedures:

This is also like macro but they are used for largest set of instructions. Macro is useful for small set of instructions, which performs a specific task. Procedure contain procedure body which contains set of instructions and RET statements. Which denotes return statement. Procedure follow CALL-RETURN method.

Execution time of procedure is high compare to macro. Assembly directive is PROC for starting, ENDP for ending used.

### Assembly Directive:-

An assembler is a program to convert an assembly language program into equivalent machine code modules which may be further converted to executable code.

Hints are given to the assembler using some pre-defined alphabetical strings called assembly directives. These help the assembler to correctly understand the assembly language programs to prepare the code.

### DB - Define Byte:-

This reserves byte of memory locations in the memory.

Ex: RANK DB 01 02 03

MESSAGE DB "Good Morning".

### DW - Define Word:-

This reserves 16-bits instead of bytes.

Words DW 1 2 3 4

### DQ - Define Quadword:-

Reserves 4 words.



DT-Define Tenbytes :-

ASSUME logical segment name.

ASSUME CS : CODE

ASSUME DS : DATA

ENDP :-

End of procedure.

END S :-

End of segment.

---

## Ex 1.9

① Solve for  $x$

(i)  $(1256)_8 = (x)_2$

Sol  $\therefore = (\underline{001010101110})_2$

$\therefore (1256)_8 = (686)_{10} //$

(ii)  $(19.125)_{10} = (x)_8$

Sol  $\therefore \begin{array}{r} 8 \overline{) 19} -3 \\ \underline{2} \end{array}$   
 $(23)_8$

$\begin{array}{r} 0.125 \times 8 \\ \hline 1.000 \rightarrow 1 \\ 0.000 \times 8 \\ \hline 0 \rightarrow 0 \end{array}$

$\therefore (19.125)_{10} = (23.10)_8 //$

(iii)  $(AC.2)_{16} = (x)_8$

Sol  $\therefore (1010 \ 1100 . 0010)_{16}$   
 $= (010 \ 101 \ 100 . 001 \ 000)_8$   
 $= (254.10)_8$

(iv)  $(10011.11)_2 = (x)_{16}$

Sol  $\therefore (0001 \ 0011 . 1100)_2$   
 $= (13.C)_{16}$

② Each of the following arithmetic operation is correct at least one number system. Determine the possible bases of the numbers in each operation.



$$(i) 1234 + 5432 = 6666$$

$$\text{Sol} \quad (1234)_{10} + (5432)_{10} = (6666)_{10}$$

$$(ii) \sqrt{41} = 5$$

$$\text{Sol} \quad \sqrt{41} = 5$$

$$b^1 \quad b^0 \quad b^0$$

$$\sqrt{4(b) + 1(b^0)} = 5b^0$$

S.O.B.S.

$$(\sqrt{4b+1})^2 = (5)^2 \Rightarrow 4b+1=25$$

$$4b=24$$

$$\boxed{b=6} //$$

$$\therefore (\sqrt{41})_6 = (\sqrt{25})_{10} = 5 //$$

$$(iii) \frac{302}{20} = 12.1$$

$$\text{Sol} \quad \frac{3b^2 + 0(b) + 2(b^0)}{2b + 0(b^0)} = \frac{1(b) + 2(b^0)}{b} + \frac{1 \times b^{-1}}{1}$$

$$\frac{3b^2 + 2}{2b} = b + 2 + \frac{1}{b}$$

$$\frac{3b^2 + 2}{2b} = \frac{b^2 + 2b + 1}{1}$$

$$2b^2 + 4b + 2 = 3b^2 + 2$$

$$3b^2 - 2b^2 - 4b = 0$$

$$b^2 = 4b$$

$$\boxed{b=4} //$$

(90)  $23 + 44 + 14 + 32 = 223$

Sol  $2b + 3 + 4b + 4 + b + 4 + 3b + 2 = 2b^2 + 2b + 3$

$10b + 13 = 2b^2 + 2b + 3$

$2b^2 - 10b + 2b - 13 + 3 = 0$

$2b^2 - 8b - 10 = 0$

$b^2 - 4b - 5 = 0$

$b = 5, -1 \Rightarrow b = 5 //$

(3) If  $(789)_{16} + (473)_8 = (x)_4$

Sol & given  $(789)_{16} + (473)_8 = (x)_4$

$(1929)_{10} + (315)_{10} = (2244)_{10}$

$\therefore x = (2244)_{10} = (203010)_4$

$$\begin{array}{r} 4 \overline{) 2244} \\ 4 \overline{) 561} \\ 4 \overline{) 140} \\ 4 \overline{) 353} \\ 4 \overline{) 872} \end{array}$$

BCD Addition:- (on (8421)).

$184 + 576$

$$\begin{array}{r} 1 \quad 8 \quad 4 \\ 5 \quad 7 \quad 6 \\ \hline 7 \quad 6 \quad 0 \\ \hline 0111 \quad 0110 \quad 0000 \end{array}$$

$$\begin{array}{r} \Rightarrow \begin{array}{ccc} 0001 & 1000 & 0100 \\ 0101 & 0111 & 0110 \\ \hline 0110 & 1111 & 0101 \end{array} \end{array}$$

$\nearrow$  Incorrect BCD

Incorrect BCD results & 9 को संशोधित करने के लिए 6 add करना पड़ेगा.

$$\begin{array}{r} 0110 \quad 1111 \quad 0100 \\ 0110 \quad 0110 \\ \hline 0111 \quad 0110 \quad 0000 \end{array}$$

$6 = 0110$

$\leftarrow$  Correct BCD result



Q Write 4 different binary codes in a table for the decimal digits.

Decimal digit	BCD 8421	2421	Excess-3 Code	84-2-1
0	0000	0000	0011	0000
1	0001	0001	0100	0111
2	0010	0010	0101	0110
3	0011	0011	0110	0101
4	0100	0100	0111	0100
5	0101	0101	1000	1011
6	0110	0110	1001	1010
7	0111	0111	1010	1001
8	1000	1110	1011	1000
9	1001	1111	1100	1111
Six unused combinations	1010	1000	1101	0001
	1011	1001	1110	0010
	1100	1010	1111	0011
	1101	1011	0001	1100
	1110	1100	0010	1101
	1111	1101	0000	1110

② Explain weighted code and self complementing property with example.

Weighted Code

In this each bit pattern is assigned a weighting factor in such a way that each digit can be evaluated by adding the weights

of all the ones in the coded information.  
Ex: BCD code and 2421 code.

### Self Complementing

The property that the 9's complement of decimal number is obtained directly by changing 1's to 0's and 0's to 1's.

i.e., by complementing each bit.

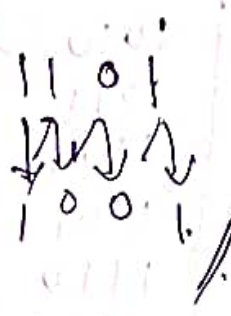
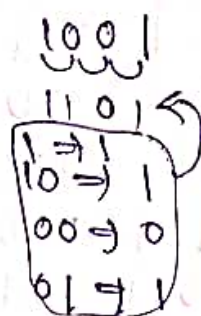
Ex: 2421 code and excess-3 code  
(are self complementing code).

6  $\rightarrow$  1001  
9's  $\rightarrow$  0110  $\rightarrow$  1's

### Gray Code

X-OR

x	y	z
0	0	0
0	1	1
1	0	1
1	1	0



The code which exhibits only a single bit change from one code number to the next is known as gray code.

i.e., each gray code number differs from the preceding number by a single bit.



2) Convert binary number to a gray code.

1001101

Sol 1 0 0 1 1 0 1  $\leftarrow$  binary

1 1 0 1 0 1 1  $\leftarrow$  gray code.

(i) Convert graycode to binary number.

Sol 1 1 0 1 0 1 1  $\leftarrow$  gray code

1 0 0 1 1 0 1  $\leftarrow$  binary.

4) Simplify the boolean function

(i)  $F(w, x, y, z) = \sum (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$ .

Sol

w \ x	00	01	11	10
00	1	1		1
01	1	1		
11	1	1		1
10	1	1		

w \ x y z

0000

0001

0100

0101

1100

1101

1000

1001

w \ x y z

0010

0110

0000

0100

$\overline{w} \overline{z}$

$x \overline{z}$

w \ x y z

0100

1100

0110

1110

$x \overline{z}$

$\overline{w} \overline{z}$

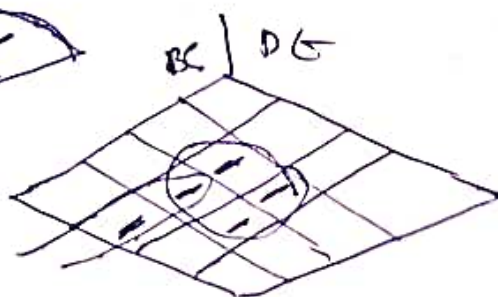
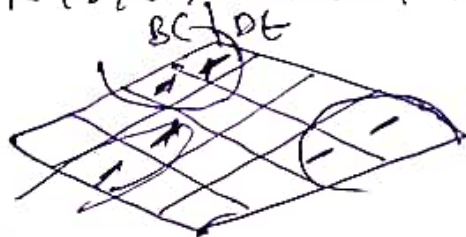
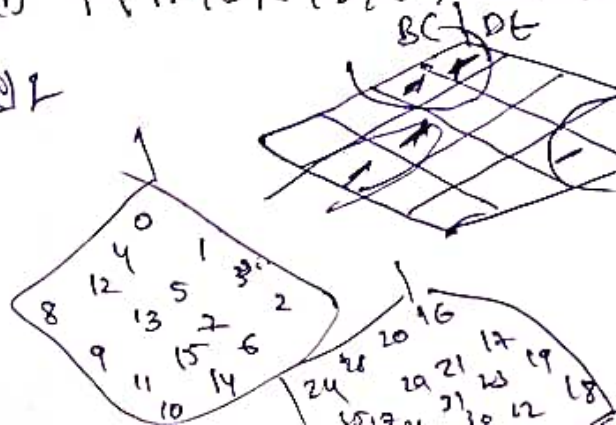
$x \overline{z}$

$\overline{y}$

$$\therefore F(w, x, y, z) = \overline{y} + \overline{w} \overline{z} + x \overline{z} \quad (\text{or } y' + w'z' + xz')$$

(ii)  $F(A, B, C, D, E) = \sum (0, 2, 4, 6, 9, 13, 21, 23, 25, 29, 31)$ .

Sol



$$= A'(B'e') + ACE + (A+A') \cdot BD'e //$$

$$= A'B'e' + ACE + BD'e //$$

6.0.00

$$\begin{array}{r} 0.10 \\ 0.01 \\ 0.10 \\ 0.01 \\ \hline 0.22 \end{array}$$

$$\begin{array}{r} 0.00 \\ 0.10 \\ 0.00 \\ 0.10 \\ 0.00 \\ 0.00 \\ 0.00 \\ 0.00 \\ \hline 0.20 \end{array}$$

0.10	0.00	0.00
0.01	0.10	0.00
0.10	0.00	0.00
0.01	0.10	0.00
0.00	0.00	0.00
0.00	0.00	0.00
0.00	0.00	0.00
0.00	0.00	0.00

$$\frac{1}{2}K = \frac{1}{2}W + \frac{1}{2}C = \frac{1}{2}A + \frac{1}{2}W + \frac{1}{2}P = \frac{1}{2}(A+W+P)$$

$$\frac{1}{2}(A+W+P) = \frac{1}{2}(A+W+P) = \frac{1}{2}(A+W+P)$$

$$\frac{1}{2}(A+W+P) = \frac{1}{2}(A+W+P) = \frac{1}{2}(A+W+P)$$