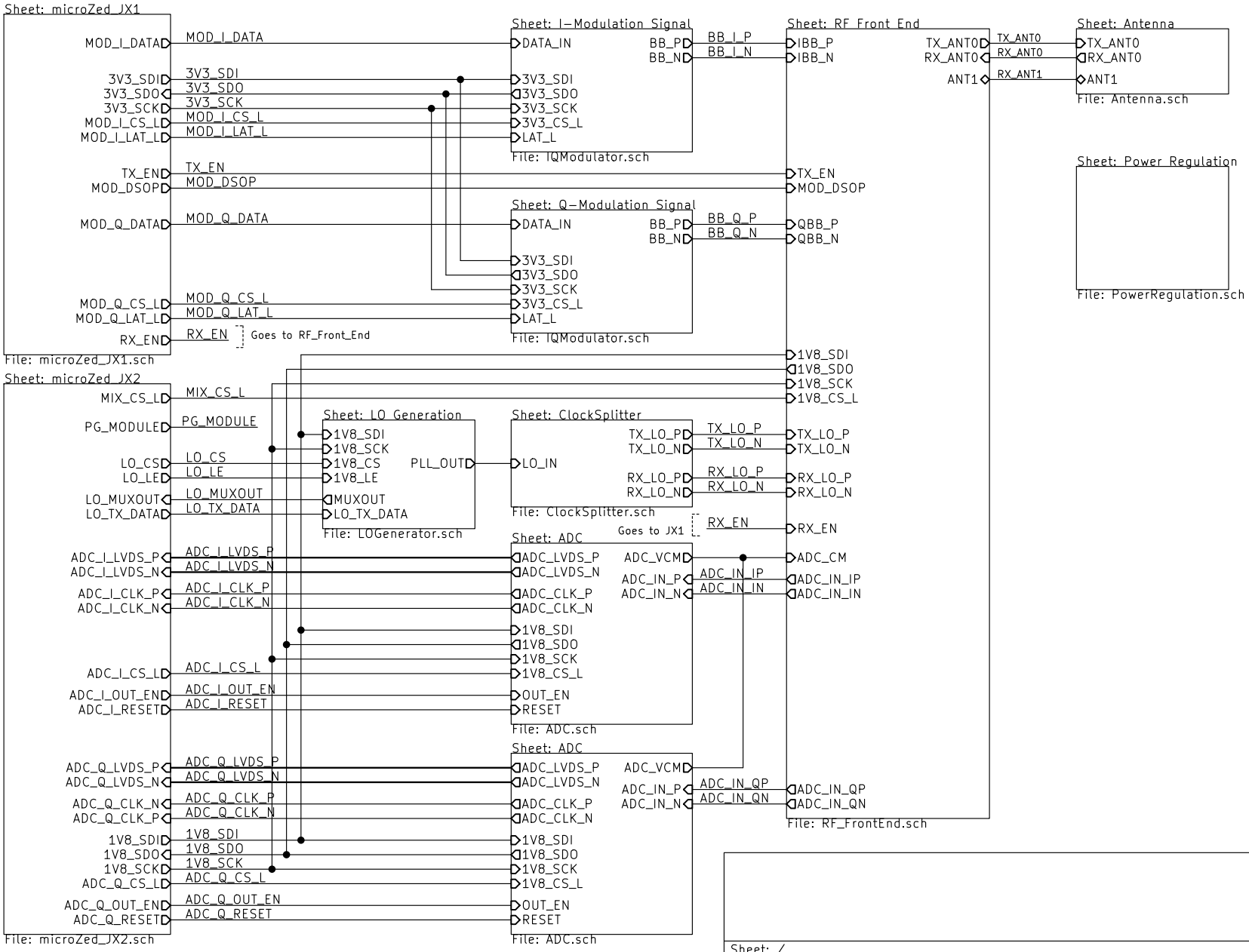
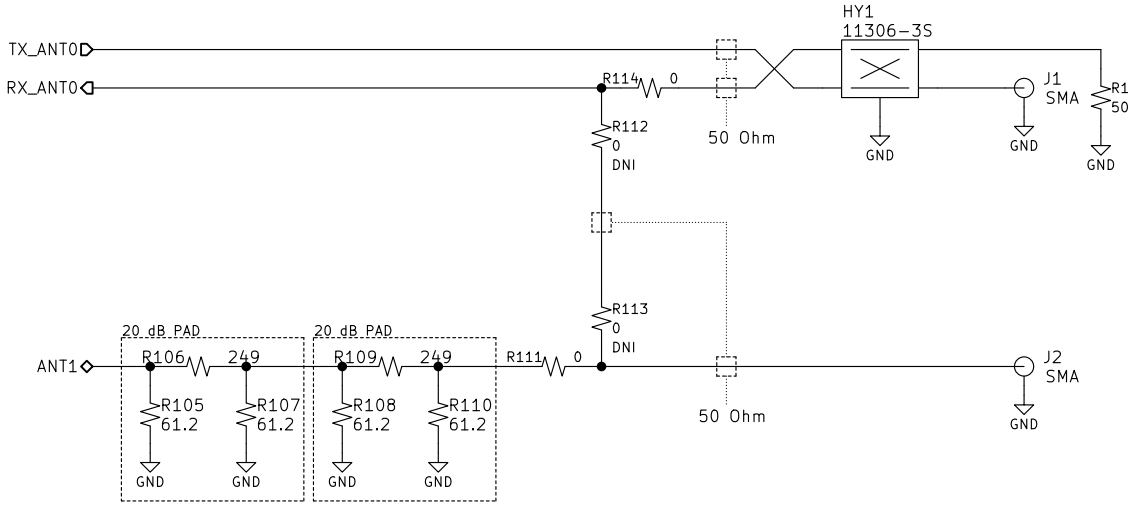

Sheet: microZed_JX1
MOD_I_DATA
3V3_SDI
3V3_SDO
3V3_SCK
MOD_I_CS_L
MOD_I_LAT_L
TX_EN
MOD_DSOP
MOD_Q_DATA
MOD_Q_CS_L
MOD_Q_LAT_L
RX_EN
Goes to RF_Front_End
File: microZed_JX1.sch
Sheet: I-Modulation Signal
DATA_IN
3V3_SDI
3V3_SDO
3V3_SCK
3V3_CS_L
LAT_L
BB_P
BB_N
BB_I_P
BB_I_N
File: IQModulator.sch
Sheet: Q-Modulation Signal
DATA_IN
3V3_SDI
3V3_SDO
3V3_SCK
3V3_CS_L
LAT_L
BB_P
BB_N
BB_Q_P
BB_Q_N
File: IQModulator.sch
Sheet: RF Front End
IBB_P
IBB_N
QBB_P
QBB_N
TX_EN
MOD_DSOP
1V8_SDI
1V8_SDO
1V8_SCK
1V8_CS_L
TX_LO_P
TX_LO_N
RX_LO_P
RX_LO_N
RX_EN
ADC_CM
ADC_IN_IP
ADC_IN_IN
ADC_IN_QP
ADC_IN_QN
TX_ANT0
RX_ANT0
ANT1
File: RF_FrontEnd.sch
Sheet: Antenna
TX_ANT0
RX_ANT0
ANT1
File: Antenna.sch
Sheet: Power Regulation
File: PowerRegulation.sch
Sheet: microZed_JX2
MIX_CS_L
PG_MODULE
LO_CS
LO_LE
LO_MUXOUT
LO_TX_DATA
ADC_I_LVDS_P
ADC_I_LVDS_N
ADC_I_CLK_P
ADC_I_CLK_N
ADC_I_CS_L
ADC_I_OUT_EN
ADC_I_RESET
ADC_Q_LVDS_P
ADC_Q_LVDS_N
ADC_Q_CLK_N
ADC_Q_CLK_P
1V8_SDI
1V8_SDO
1V8_SCK
ADC_Q_CS_L
ADC_Q_OUT_EN
ADC_Q_RESET
File: microZed_JX2.sch
Sheet: LO Generation
1V8_SDI
1V8_SCK
1V8_CS
1V8_LE
MUXOUT
LO_TX_DATA
PLL_OUT
File: LOGenerator.sch
Sheet: ClockSplitter
LO_IN
TX_LO_P
TX_LO_N
RX_LO_P
RX_LO_N
File: ClockSplitter.sch
Goes to JX1
Sheet: ADC
ADC_LVDS_P
ADC_LVDS_N
ADC_CLK_P
ADC_CLK_N
1V8_SDI
1V8_SDO
1V8_SCK
1V8_CS_L
OUT_EN
RESET
ADC_VCM
ADC_IN_P
ADC_IN_N
File: ADC.sch
Sheet: ADC
ADC_LVDS_P
ADC_LVDS_N
ADC_CLK_P
ADC_CLK_N
1V8_SDI
1V8_SDO
1V8_SCK
1V8_CS_L
OUT_EN
RESET
ADC_VCM
ADC_IN_P
ADC_IN_N
File: ADC.sch
Sheet: /
File: PulseRadar_3GHz.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.5)-3
Id: 1/17

To Do:
1. Add limiter to RX_ANT0



Sheet: /Antenna/
File: Antenna.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 2/17

Power Consumption

Rails	Voltage (V)	Current (mA)
AVDD	1.8	7.5 – 10.0
3V3	3.3	33.5 – 49.0
5V	5.0	29.3

Spurious Emissions

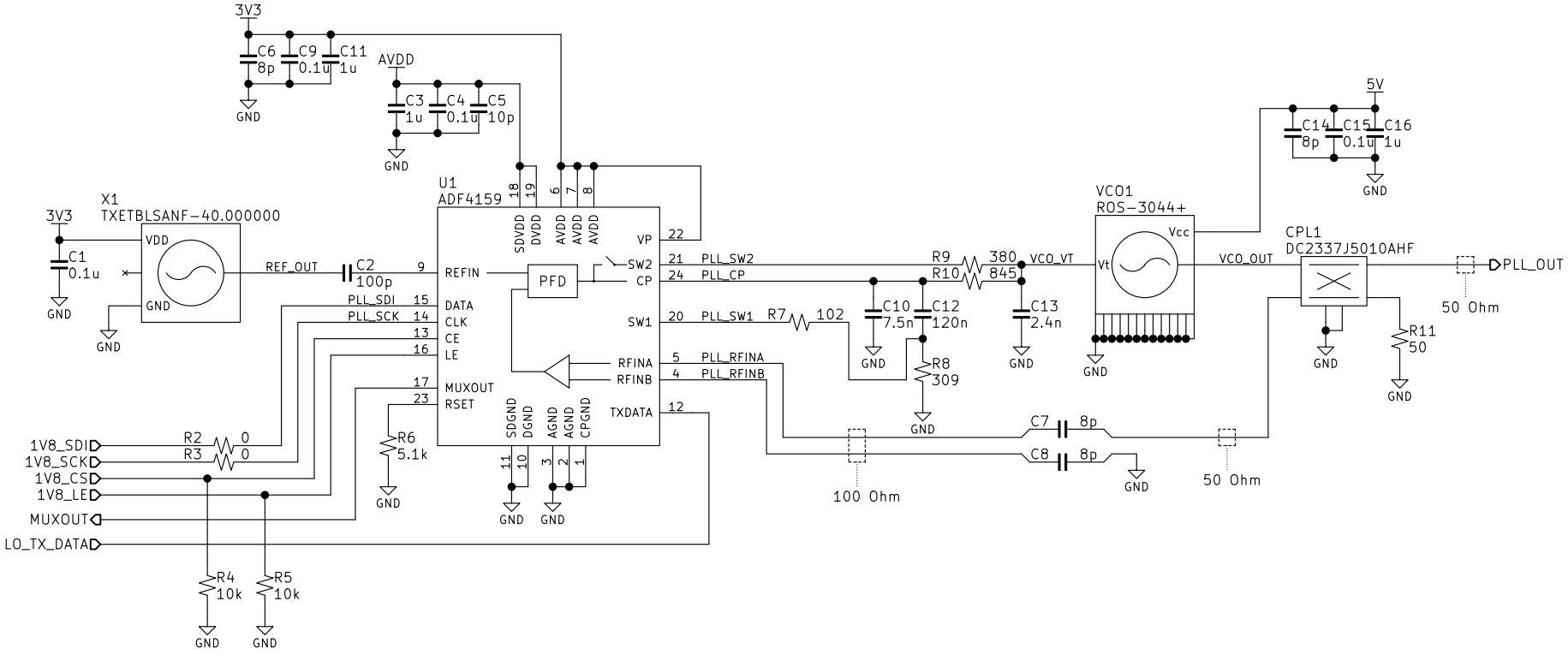
Harmonic	Rel. Power
1st	−28.7 dBc
2nd	−33.3 dBc
3rd	−56.4 dBc

Phase Noise

Offset	Spectral Density
100 Hz	−90 dBc
1 kHz	−100 dBc
10 kHz	−95 dBc
100 kHz	−110 dBc
1 MHz	−135 dBc

Power Output

6.9−7.8 dBm



Digital Lock Detect Triggers at 10 % Frequency Tolerance

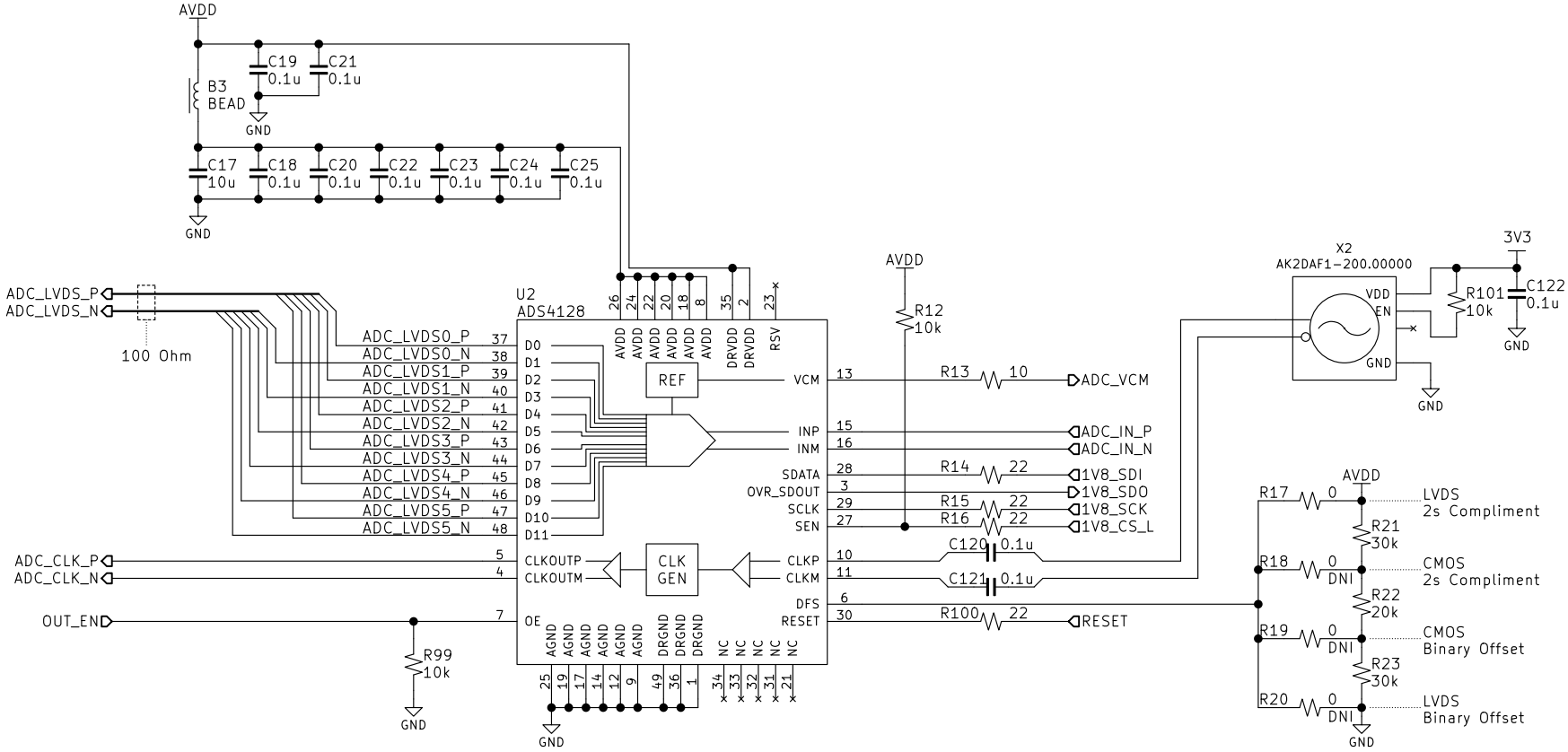
Sheet: /LO Generation/
File: LOGenerator.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)−3		Id: 3/17

Power Consumption

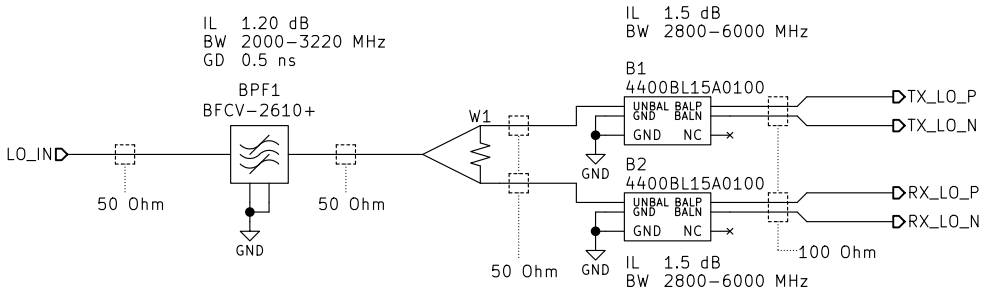
Rails	Voltage (V)	Current (mA)
AVDD	1.8	140–185
3V3	3.3	10–15
5V	5.0	N/A



Sheet: /ADC/
File: ADC.sch

Title:

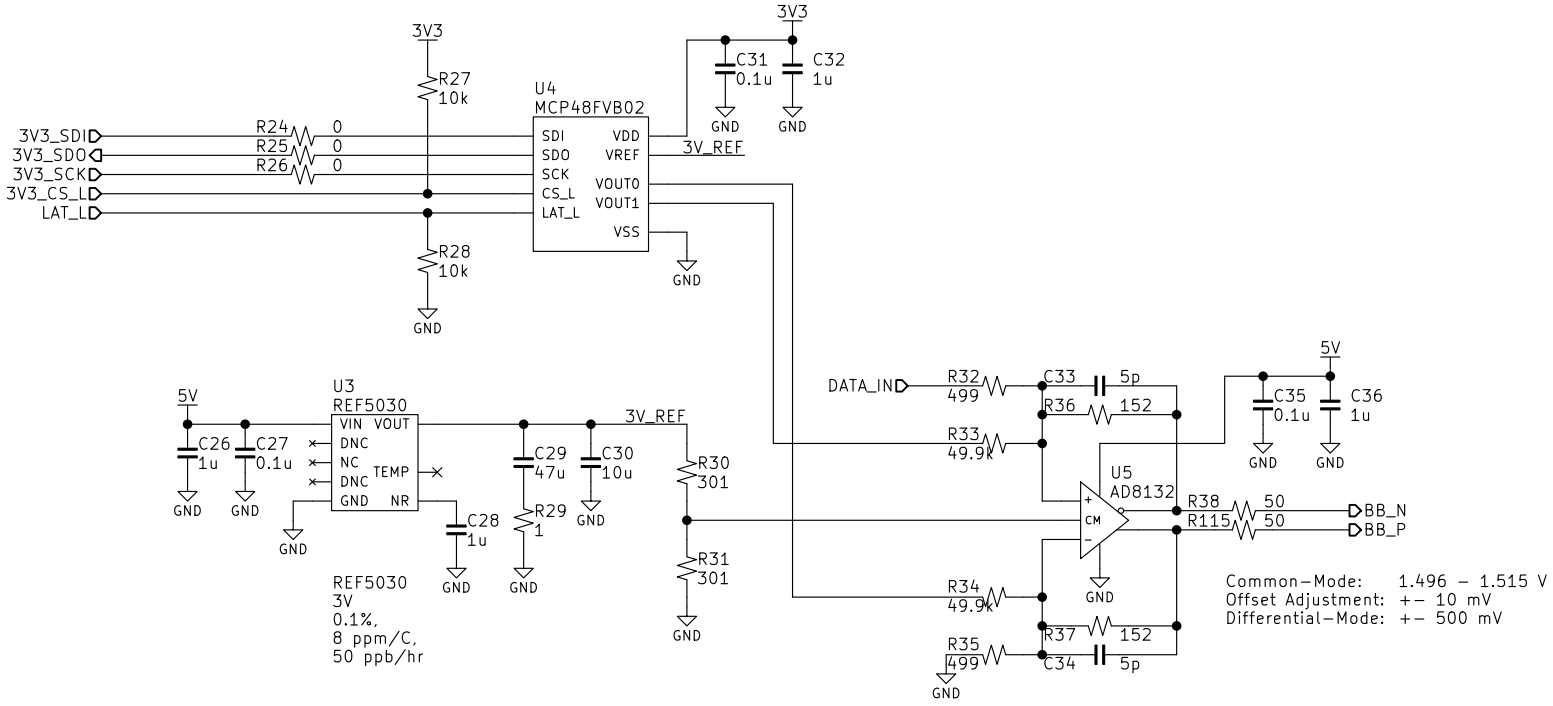
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 4/17



Sheet: /ClockSplitter/ File: ClockSplitter.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)–3		Id: 5/17

Power Consumption

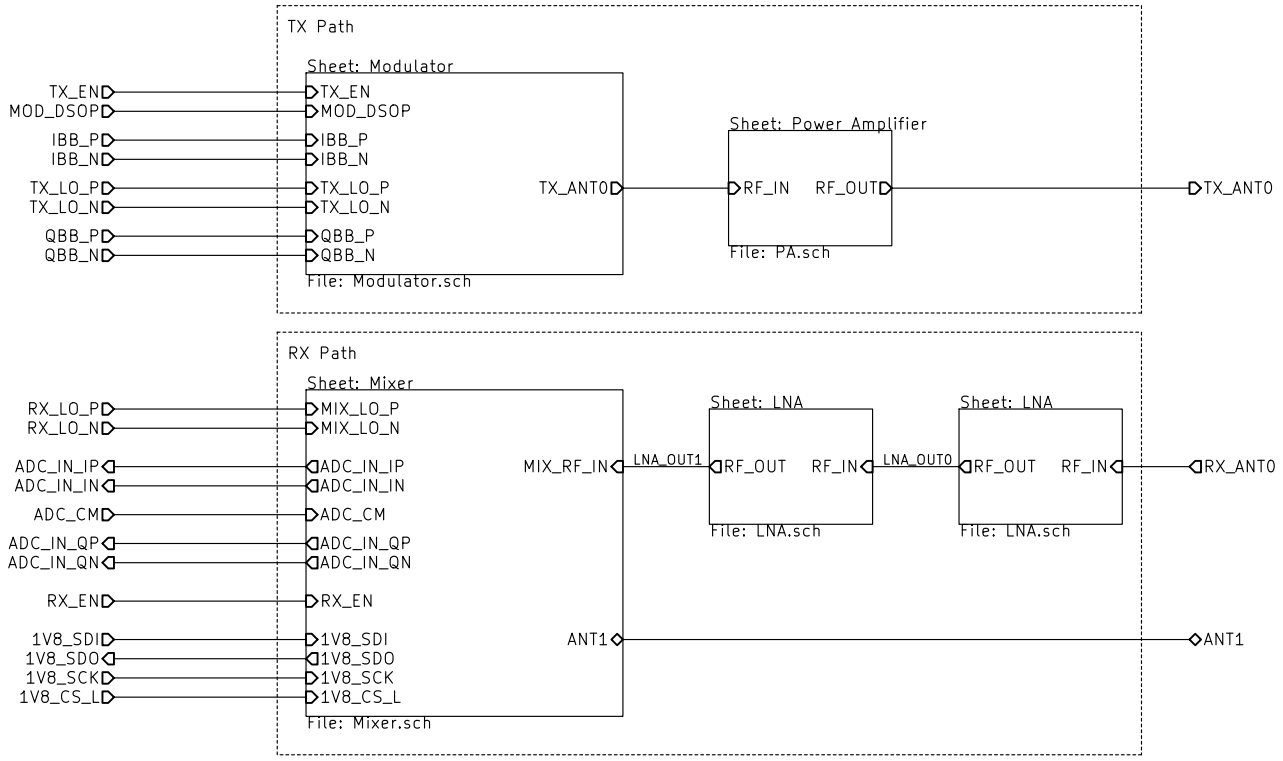
Rails	Voltage (V)	Current (mA)
AVDD	1.8	N/A
3V3	3.3	0.51–1.85
5V	5.0	10.7–13.7



Sheet: /Q–Modulation Signal/
File: IQModulator.sch

Title:

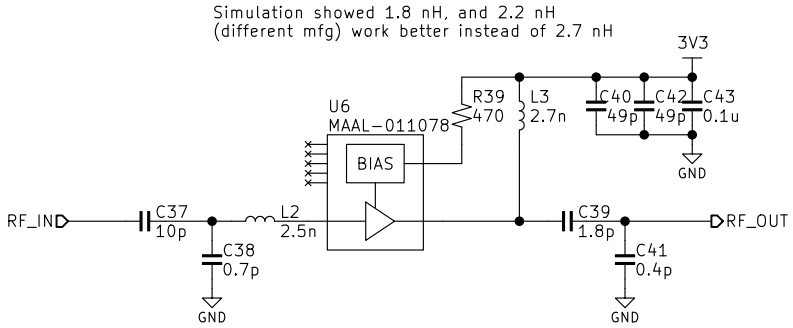
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)–3		Id: 6/17



Sheet: /RF Front End/ File: RF_FrontEnd.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 7/17

Power Consumption

Rails	Voltage (V)	Current (mA)
AVDD	1.8	N/A
3V3	3.3	43–53
5V	5.0	N/A



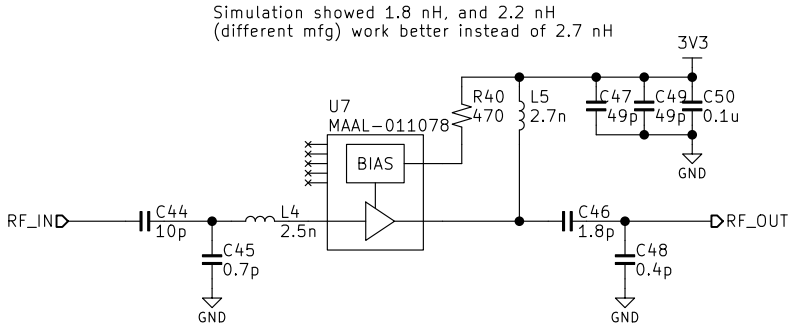
Sheet: /RF Front End/LNA/
File: LNA.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 8/17

Power Consumption

Rails	Voltage (V)	Current (mA)
AVDD	1.8	N/A
3V3	3.3	43–53
5V	5.0	N/A



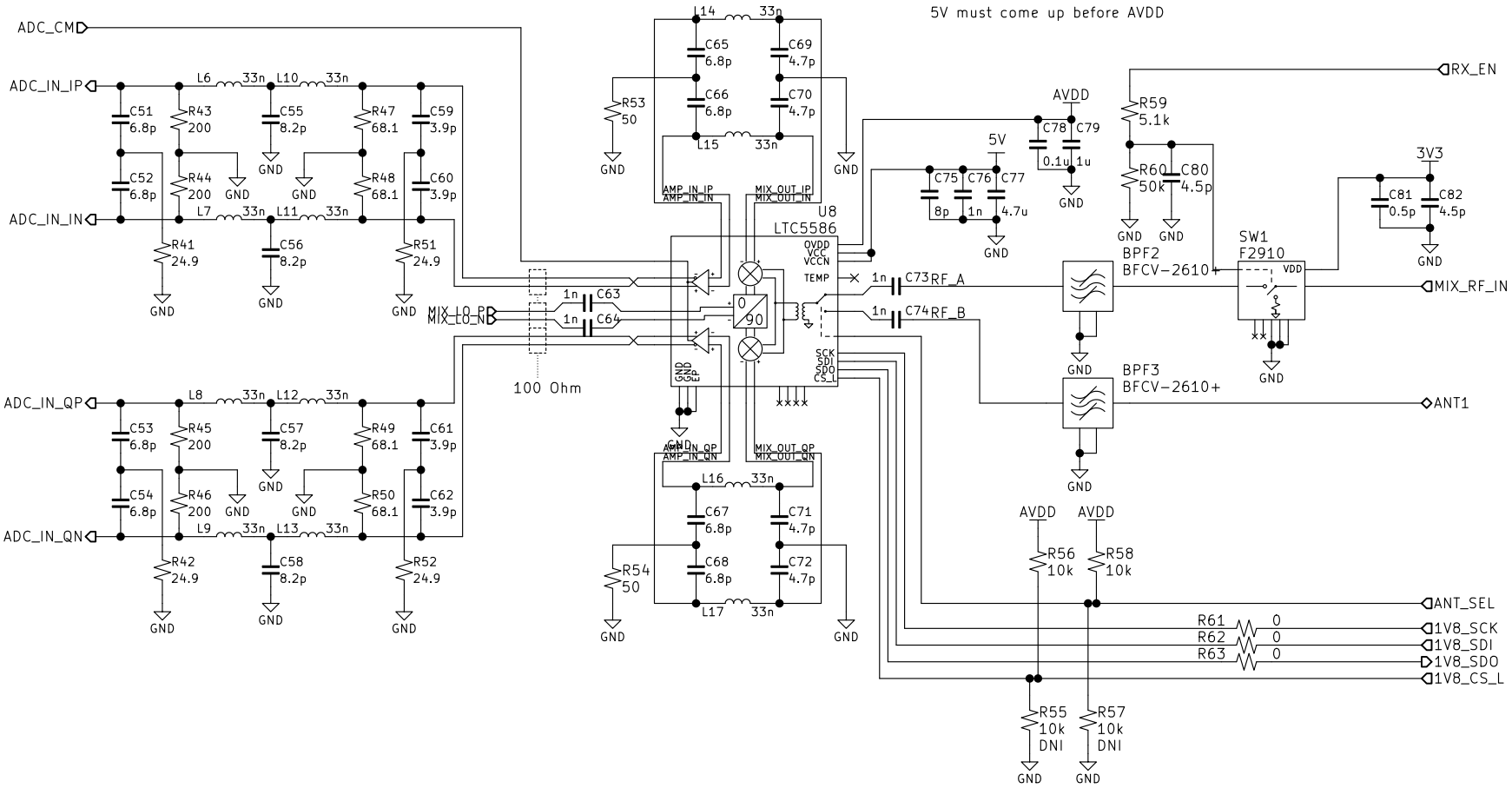
Sheet: /RF Front End/LNA/
File: LNA.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 9/17

Power Consumption

Rails	Voltage (V)	Current (mA)
AVDD	1.8	< 1
3V3	3.3	N/A
5V	5.0	430–470



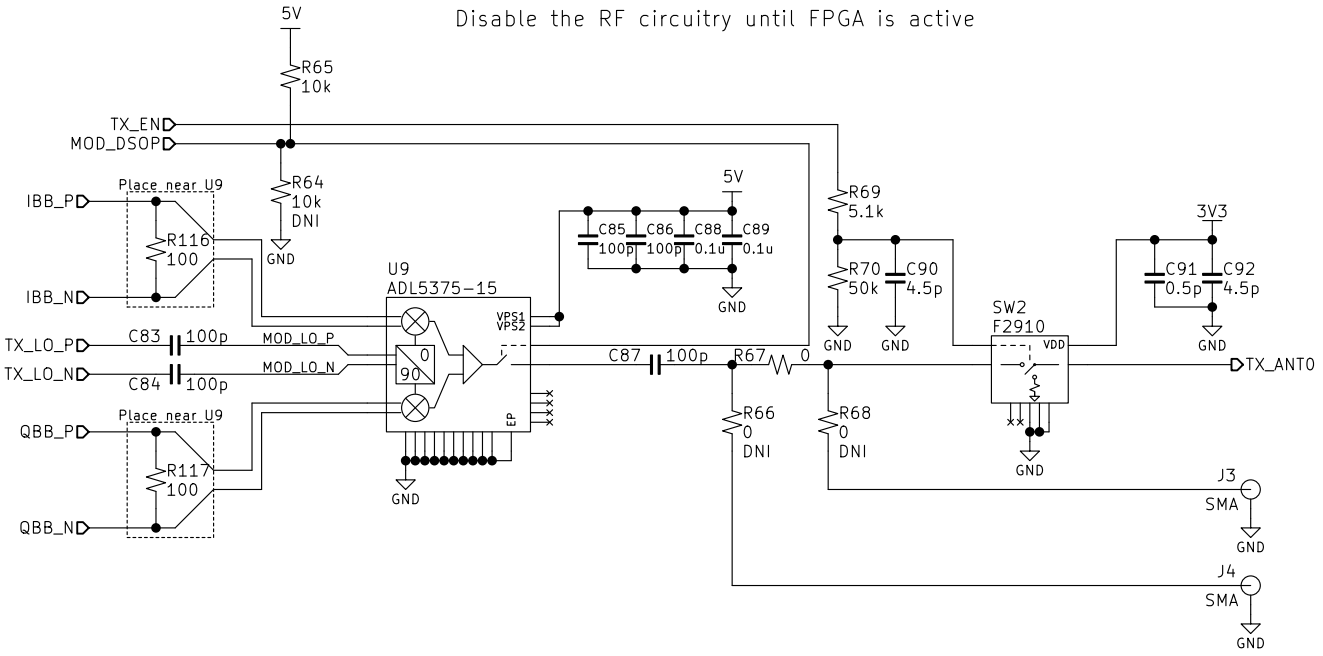
Sheet: /RF Front End/Mixer/
File: Mixer.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 10/17

Power Consumption

Rails	Voltage (V)	Current (mA)
AVDD	1.8	N/A
3V3	3.3	N/A
5V	5.0	127–203



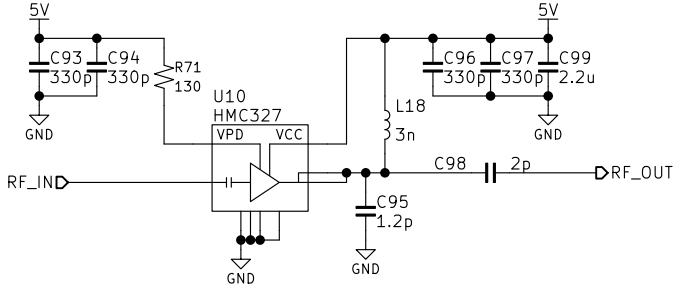
Sheet: /RF Front End/Modulator/ File: Modulator.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 11/17

Power Consumption

Rails	Voltage (V)	Current (mA)
AVDD	1.8	N/A
3V3	3.3	N/A
5V	5.0	257

RF Performance – Datasheet

Gain	21.2 dB
Psat	30 dBm
OIP3	39 dBm
NF	6 dB



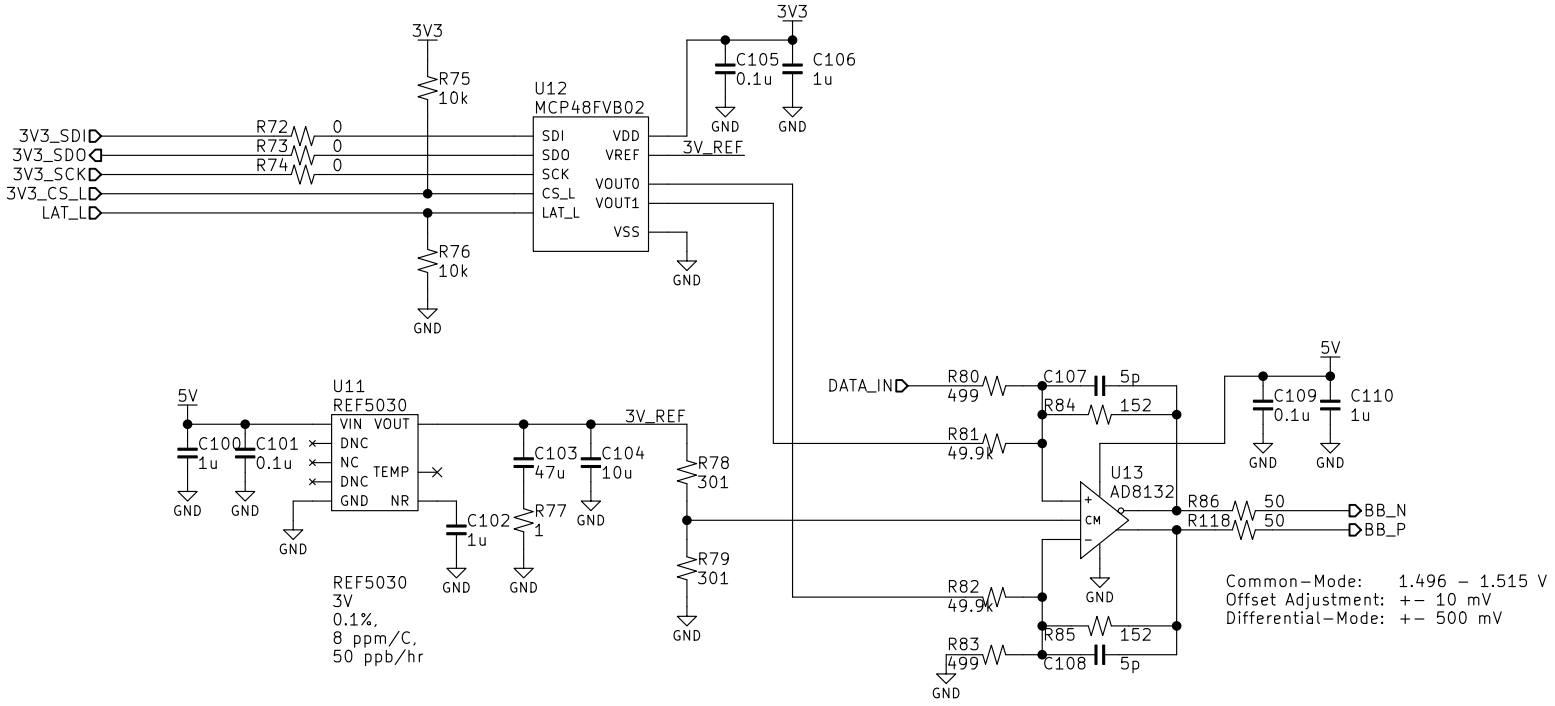
Sheet: /RF Front End/Power Amplifier/
File: PA.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 12/17

Power Consumption

Rails	Voltage (V)	Current (mA)
AVDD	1.8	N/A
3V3	3.3	0.51–1.85
5V	5.0	10.7–13.7

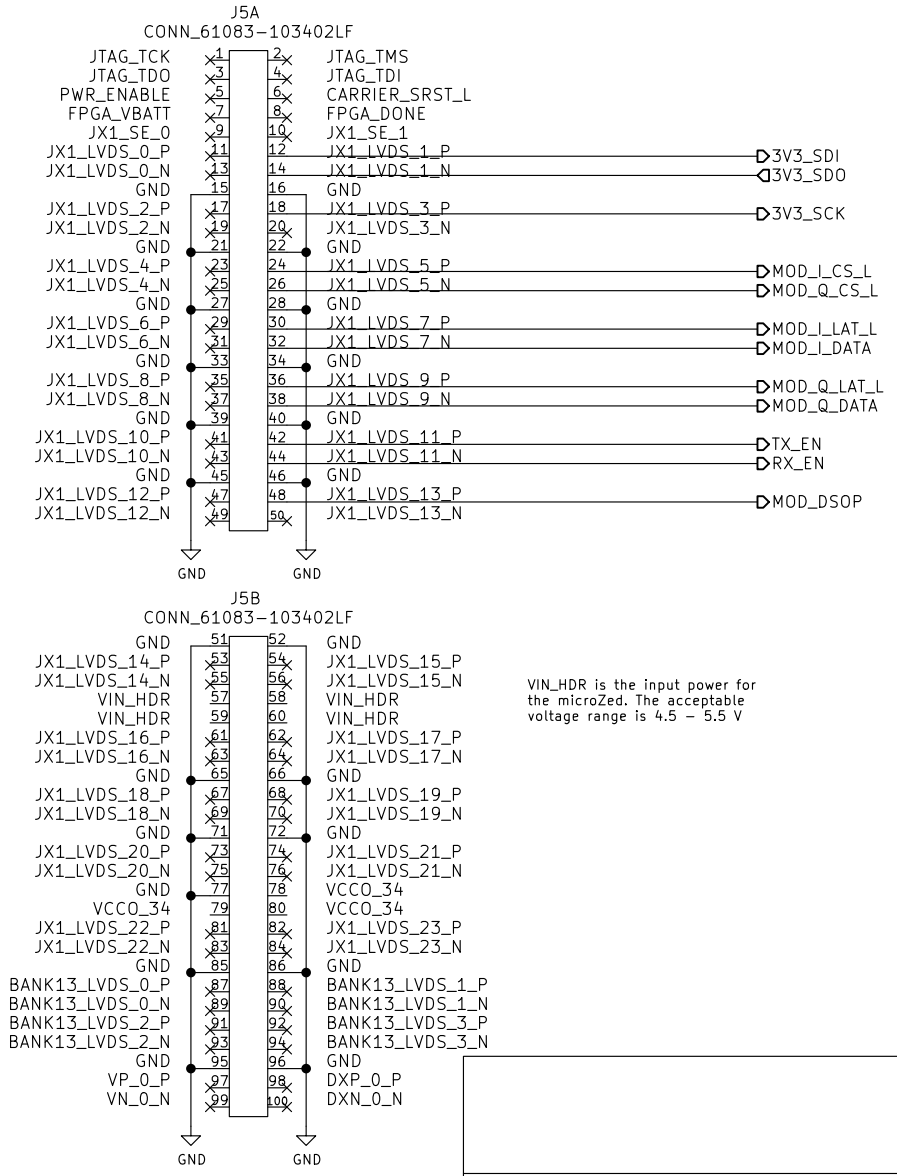


Sheet: /I–Modulation Signal/
File: IQModulator.sch

Title:

Size: A4 | Date: | **Rev:**

KiCad E.D.A. kicad (5.1.5)–3 | Id: 13/17



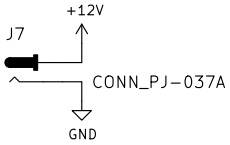
Sheet: /microZed_JX1/
File: microZed_JX1.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 14/17

Power Consumption

Rails	Voltage (V)	Current (mA)
AVDD	1.8	288.5–381
3V3	3.3	140.5–188.7
5V	5.0	864.7–986.7



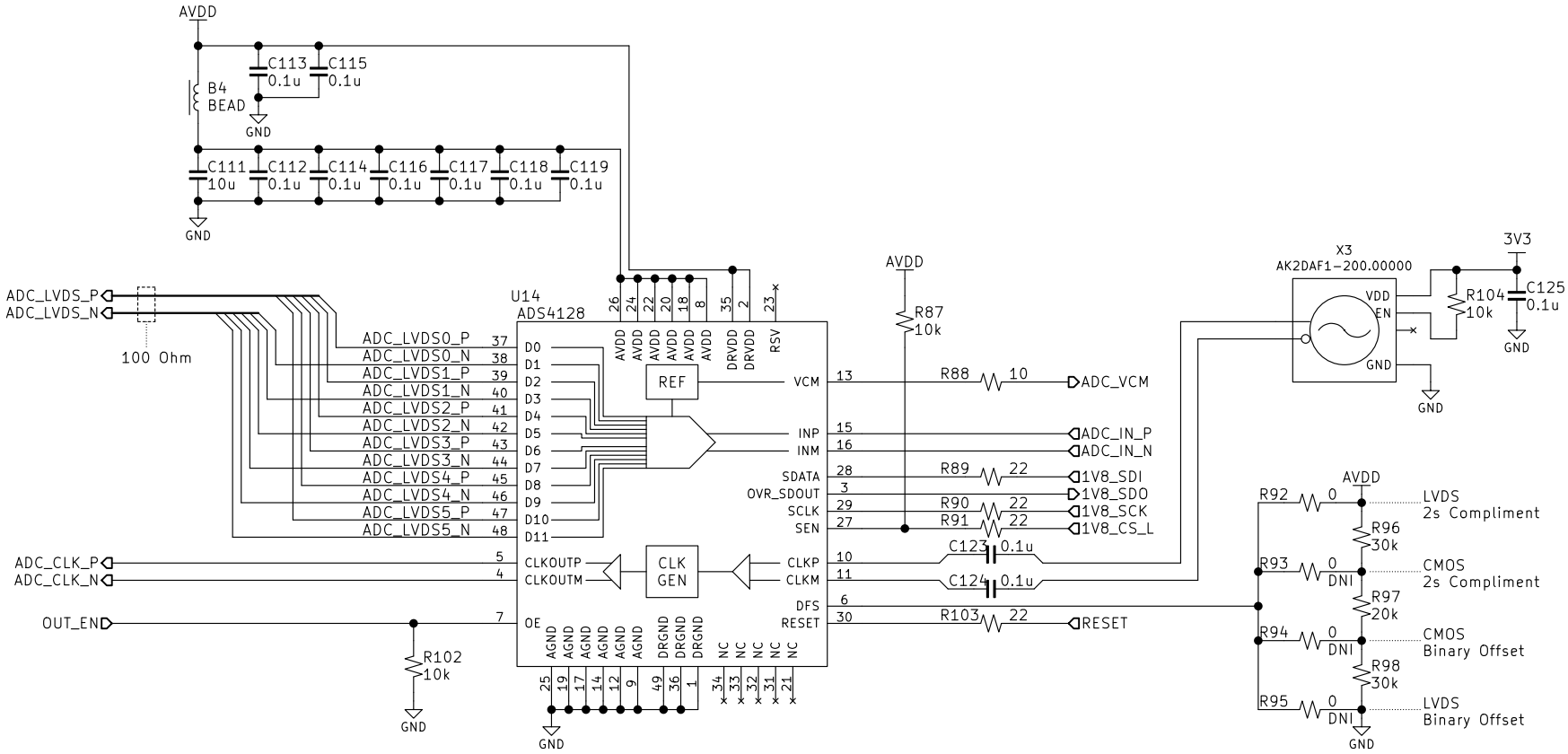
Sheet: /Power Regulation/
File: PowerRegulation.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 15/17

Power Consumption

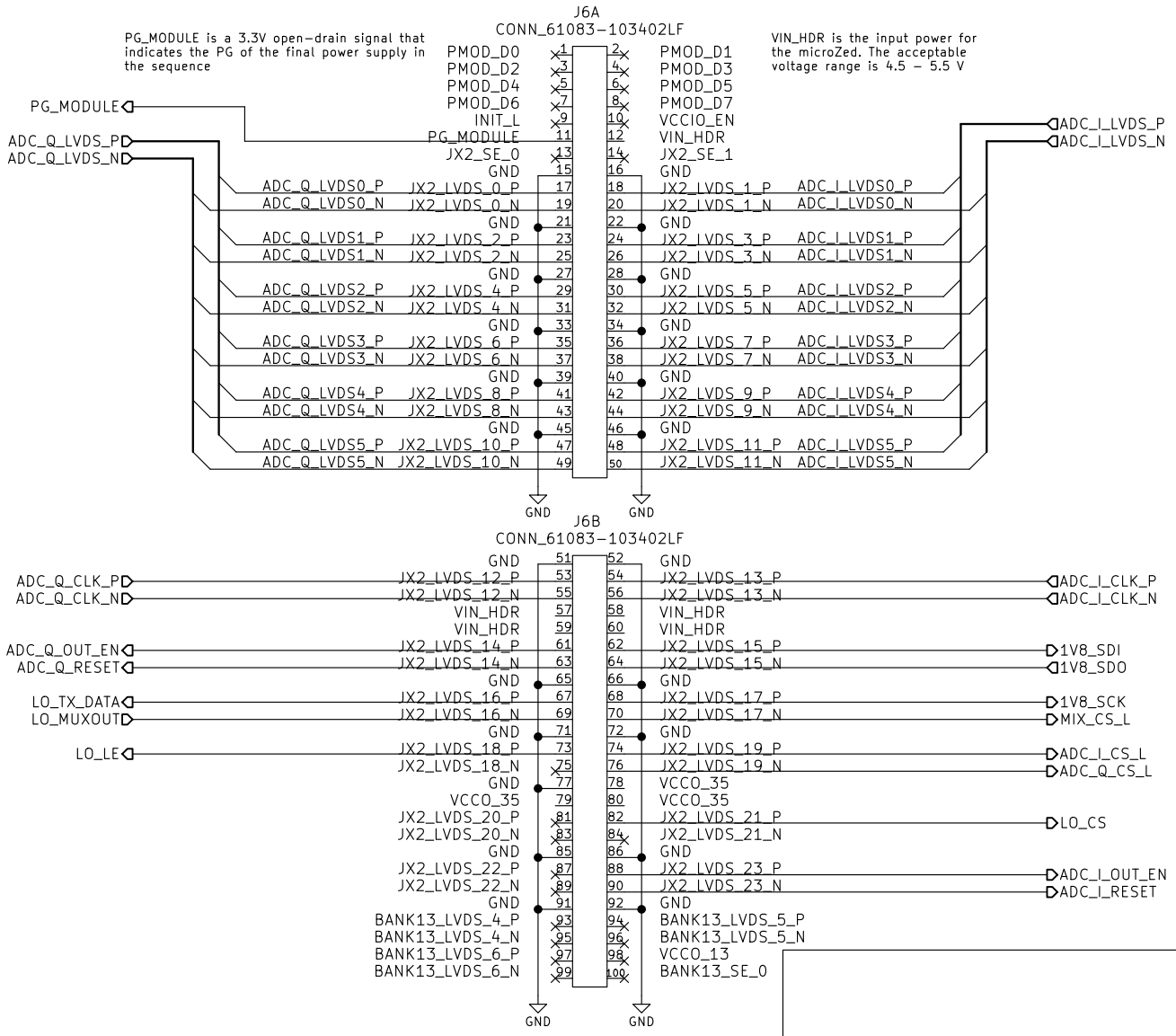
Rails	Voltage (V)	Current (mA)
AVDD	1.8	140–185
3V3	3.3	10–15
5V	5.0	N/A



Sheet: /ADC/
File: ADC.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.5)-3		Id: 16/17


J6A
CONN_61083-103402LF
PG_MODULE is a 3.3V open-drain signal that indicates the PG of the final power supply in the sequence
VIN_HDR is the input power for the microZed. The acceptable voltage range is 4.5 – 5.5 V
PG_MODULE
ADC_Q_LVDS_P
ADC_Q_LVDS_N
PMOD_D0
PMOD_D1
PMOD_D2
PMOD_D3
PMOD_D4
PMOD_D5
PMOD_D6
PMOD_D7
INIT_L
VCCIO_EN
PG_MODULE
VIN_HDR
JX2_SE_0
JX2_SE_1
GND
ADC_Q_LVDS0_P
JX2_LVDS_0_P
JX2_LVDS_1_P
ADC_I_LVDS0_P
ADC_Q_LVDS0_N
JX2_LVDS_0_N
JX2_LVDS_1_N
ADC_I_LVDS0_N
ADC_Q_LVDS1_P
JX2_LVDS_2_P
JX2_LVDS_3_P
ADC_I_LVDS1_P
ADC_Q_LVDS1_N
JX2_LVDS_2_N
JX2_LVDS_3_N
ADC_I_LVDS1_N
ADC_Q_LVDS2_P
JX2_LVDS_4_P
JX2_LVDS_5_P
ADC_I_LVDS2_P
ADC_Q_LVDS2_N
JX2_LVDS_4_N
JX2_LVDS_5_N
ADC_I_LVDS2_N
ADC_Q_LVDS3_P
JX2_LVDS_6_P
JX2_LVDS_7_P
ADC_I_LVDS3_P
ADC_Q_LVDS3_N
JX2_LVDS_6_N
JX2_LVDS_7_N
ADC_I_LVDS3_N
ADC_Q_LVDS4_P
JX2_LVDS_8_P
JX2_LVDS_9_P
ADC_I_LVDS4_P
ADC_Q_LVDS4_N
JX2_LVDS_8_N
JX2_LVDS_9_N
ADC_I_LVDS4_N
ADC_Q_LVDS5_P
JX2_LVDS_10_P
JX2_LVDS_11_P
ADC_I_LVDS5_P
ADC_Q_LVDS5_N
JX2_LVDS_10_N
JX2_LVDS_11_N
ADC_I_LVDS5_N
ADC_I_LVDS_P
ADC_I_LVDS_N
GND
GND
J6B
CONN_61083-103402LF
ADC_Q_CLK_P
ADC_Q_CLK_N
JX2_LVDS_12_P
JX2_LVDS_12_N
JX2_LVDS_13_P
JX2_LVDS_13_N
ADC_I_CLK_P
ADC_I_CLK_N
VIN_HDR
VIN_HDR
ADC_Q_OUT_EN
ADC_Q_RESET
JX2_LVDS_14_P
JX2_LVDS_14_N
JX2_LVDS_15_P
JX2_LVDS_15_N
1V8_SDI
1V8_SDO
LO_TX_DATA
LO_MUXOUT
JX2_LVDS_16_P
JX2_LVDS_16_N
JX2_LVDS_17_P
JX2_LVDS_17_N
1V8_SCK
MIX_CS_L
LO_LE
JX2_LVDS_18_P
JX2_LVDS_18_N
JX2_LVDS_19_P
JX2_LVDS_19_N
ADC_I_CS_L
ADC_Q_CS_L
VCCO_35
VCCO_35
JX2_LVDS_20_P
JX2_LVDS_20_N
JX2_LVDS_21_P
JX2_LVDS_21_N
LO_CS
JX2_LVDS_22_P
JX2_LVDS_22_N
JX2_LVDS_23_P
JX2_LVDS_23_N
ADC_I_OUT_EN
ADC_I_RESET
BANK13_LVDS_4_P
BANK13_LVDS_4_N
BANK13_LVDS_6_P
BANK13_LVDS_6_N
BANK13_LVDS_5_P
BANK13_LVDS_5_N
VCCO_13
BANK13_SE_0
Sheet: /microZed_JX2/
File: microZed_JX2.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.5)-3
Id: 17/17