# Initial Architecture



To remove the effects of the reflected and leaked LO signal from the RX path the two phase shifts, related to , and should be configured to match . To accomplish this a phase shifter is placed in the LO path to match the leakage phase shift. Once reduced to an acceptable level a second phase shifter can be added to the antenna to match the reflected phase shift.

A low pass filter must be added to remove the additional harmonics from the mixing and the leakage of the mixer.

## Path Characteristics

### Minimum Distance

The minimum distance is determined by the minimum detectable time difference between when a pulse is sent and when it is received. The receiver will not be able to distinguish between sent and received pulse if the pulse is returned during the pulse width.

|  |  |  |
| --- | --- | --- |
| Pulse Width (ns) | Sampling Rate (MSps) | Minimum Distance (m) |
| 10 | 200 | 2.25 |
| 15 | 200 | 3.00 |
| 20 | 200 | 3.75 |
| 25 | 200 | 4.50 |

### Maximum Distance

The maximum distance is determined by the minimum detectable signal. With the design requirement that the minimum detectable signal be -90 dBm the maximum distance can be achieved using the radar range equation.

### Minimum / Maximum Distance Tradeoff

There exists a tradeoff between the maximum and minimum detectable distances. As discussed in the previous sections to reduce the minimum detectable distance the pulse width needs to be minimized. In doing so the bandwidth of the system increases which increases the amount of noise in the system and inevitably reducing the maximum detectable range.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Pulse Width (ns) | Sampling Rate (MSps) | Bandwidth (MHz) | Min. Distance (m) | Max. Distance (m) | Max. / Min. |
| 10 | 200 | 100 | 2.25 | 56 | 25 |
| 15 | 200 | 67 | 3.00 | 62 | 21 |
| 20 | 200 | 50 | 3.75 | 67 | 18 |
| 25 | 200 | 40 | 4.50 | 70 | 16 |

### Maximum Power

The maximum returned power is achieved when an object is at the minimum detectable distance

## High Level Spectral Growth Analysis

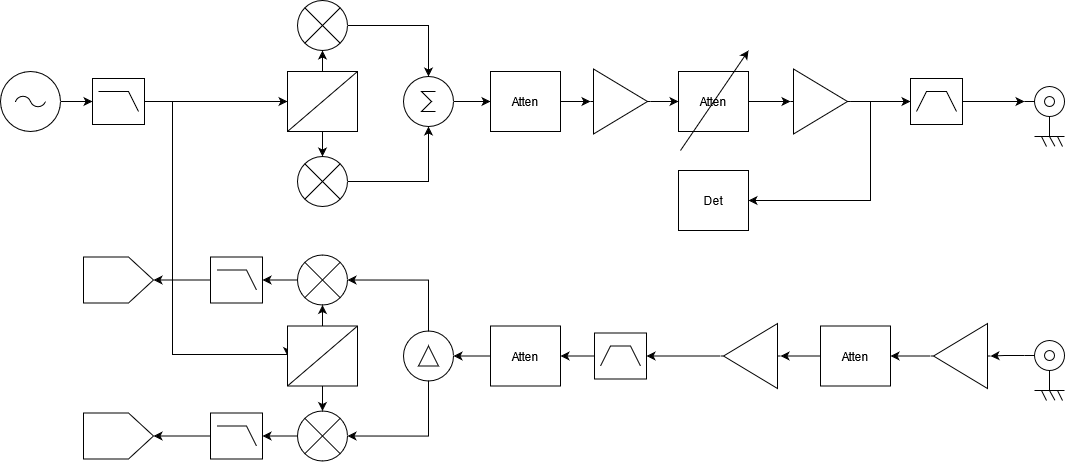


# Architecture



## Component Selection

# Design



## TX Chain

### Oscillator / PLL (ADF4159)

#### Reference Clock (TXETBLSANF-40.000000)

The reference input to the ADF4159 PLL chip is a CMOS input with 100 kOhm input impedance. This pin can be driven with TTL, CMOS or AC-coupled. It must be driven with a bias of 0.9V and -5 to +9 dBm. The bias level can be achieved with an ac-coupling capacitor.

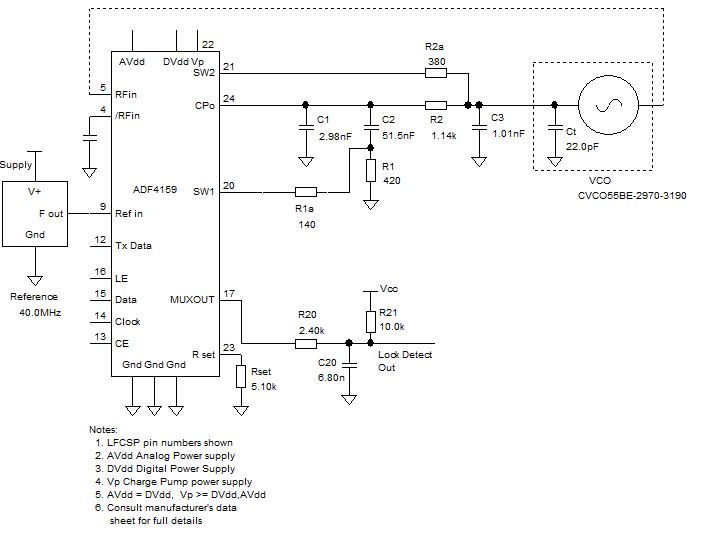
The TXETBLSANF-40.000000 oscillator outputs 0.8 Vpp into a 10 kOhm load which is 2 dBm into a 50 ohm load. The TCXO oscillator has a 2 ppm start-up tolerance and is insensitive to frequency pushing.

#### Voltage Controlled Oscillator (ROS-3044+)

The selected VCO must cover the desired frequency of 3 GHz and the tuning range must cover the charge pump output levels to guarantee a lock at 3 GHz.

#### Loop Filter

To ease the design of the loop filter and interconnectivity Analog Device’s ADIsimPLL is used for synthesizing the parameters.



The software did not have the intended VCO for the design; however, the parameters of CVCO55BE-2970-3190 are similar to the desired VCO.

#### Simulations





### Vector Modulator (ADL5375-05/-15)

#### I/Q Baseband Signaling (AD8132)

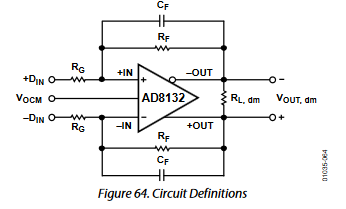
Each of the four baseband pins should be driven with 500 mVpp with a common-mode of 500 mV resulting in 1 Vpp swing on each differential baseband input. The output common-mode voltage of AD8132 defaults to half the supply point but there is a pin for providing an external reference for the common-mode voltage.

The output common-mode voltage can be as low as 0.3V above the negative supply and 2V below the positive supply. If the input of the amplifier is 3.3V CMOS logic then the gain should be 1/3.3 to give a differential output of 1 Vpp.

Since the minimum pulse width will be 10 ns it is necessary that the amplifier is capable of transitioning from 0 V to 1 V in under 1 ns (slew rate > ). The amplifier must also have a bandwidth high enough to cover the bandwidth of the pulse signal (bandwidth > ).

The AD8132 is selected as it satisfies the two criteria above with a 3 dB bandwidth of 350 MHz and slew rate of .

To avoid gain peaking due to wire-bond and pin inductance it is recommended by the manufacturer to add a small value capacitor across the feedback resistor. The value of this capacitor needs to be tuned without optimization.



#### Carrier Feedthrough Nulling (DAC)

The datasheet of ADL5375 specifies that carrier feedthrough can be reduced by applying a small differential offset to the common-mode voltage at the baseband inputs. The recommended tuning range is given to be ±10 mV for each input. This adjustment can be accomplished using a DAC connected to the single-ended to differential amplifier via a summing node.

Let R1 >> R2, RF

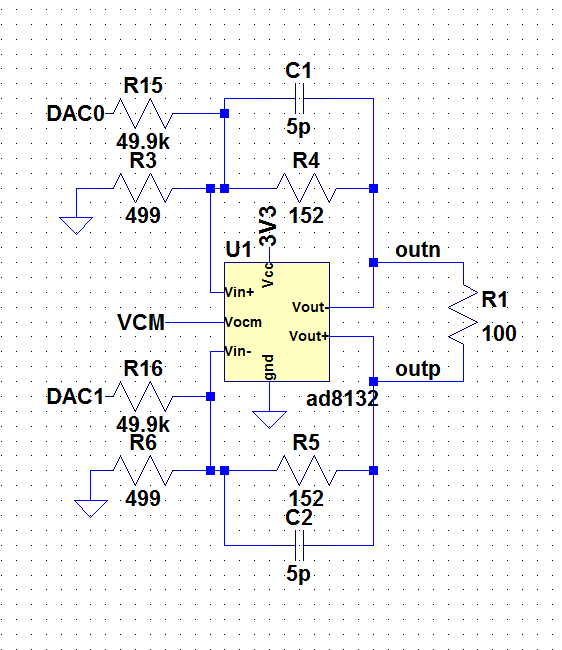


Figure 1: Simulation model of the baseband circuit setup for offset measurement



Figure 2: Output differential off set voltage with DAC1 held at 0V



Figure 3: Pulse output without carrier nulling

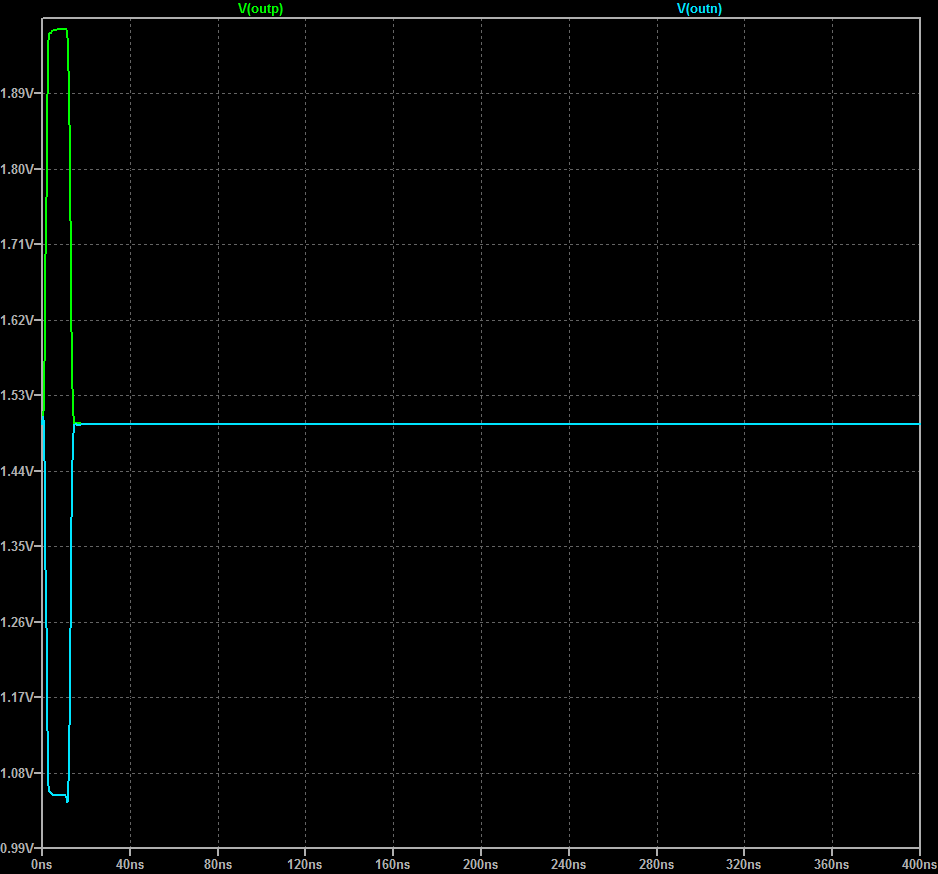


Figure 4: Pulse output with carrier nulling

#### Common-Mode Voltage

This design is intended to operate properly over a wide temperature range so it is important to use voltage reference and resistor array to produce the common-mode voltage. This will improve the stability of the temperature-related performance degradation.

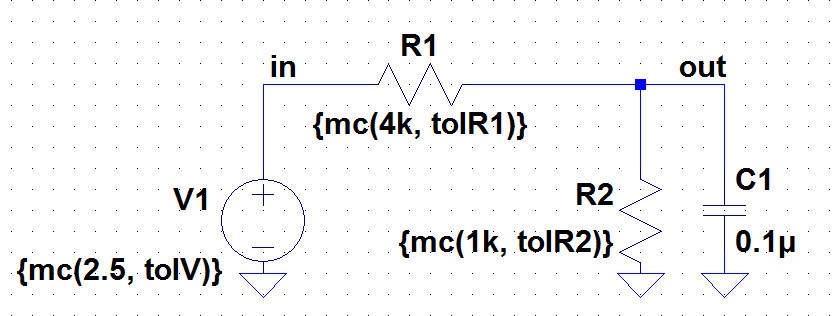


Figure 5: LTSpice simulation of Common-Mode Voltage Input

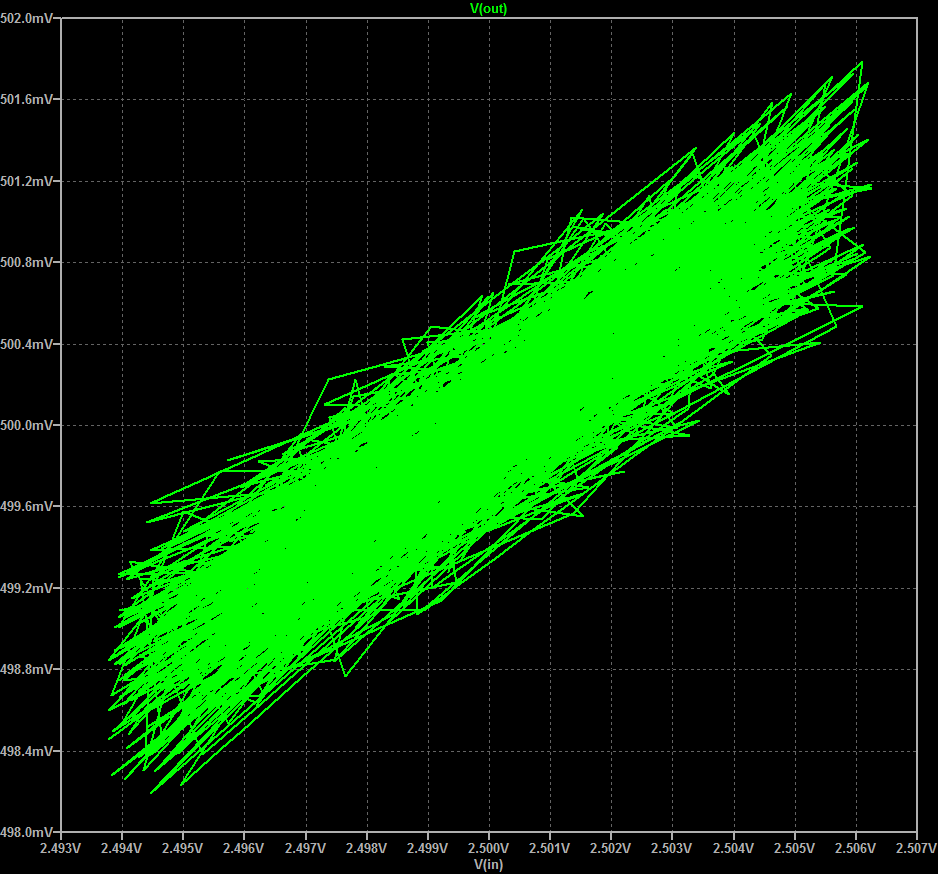
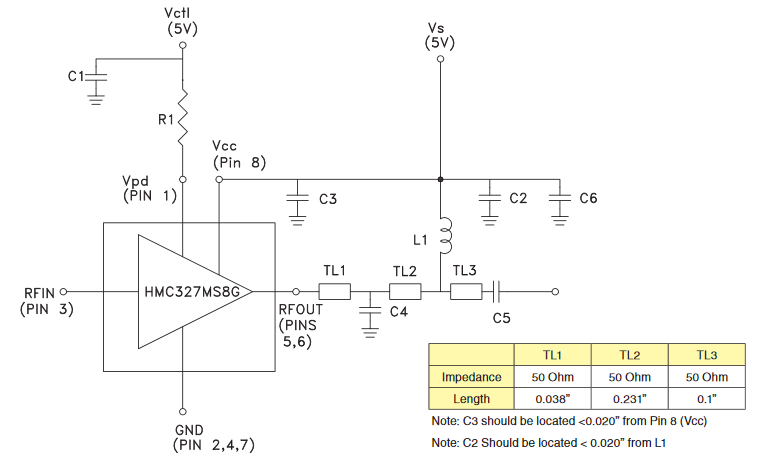


Figure 6: Monte-Carlo Simulation of the Common-Mode Input Voltage

### Power Amplifier (HMC327)

The HMC327MS8G(E) is a high efficiency GaAs InGaP Heterojunction Bipolar Transistor (HBT) MMIC power amplifier which operates between 3 and 4 GHz. The amplifier is packaged in a low cost, surface mount 8 leaded package with an exposed base for improved RF and thermal performance. With a minimum of external components, the amplifier provides 21 dB of gain, +30 dBm of saturated power at 45% PAE from a single +5V supply. Power down capability is available to conserve current consumption when the amplifier is not in use.



## RX Chain

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Bits | Ref. (V) | Min Power (dBm) | Max Power (dBm) | Min Gain (dB) | Max Gain (dB) |
| 8 | 1.8 | -33 | 15 | 27 | 57 |
| 10 | 1.8 | -45 | 15 | 15 | 45 |
| 12 | 1.8 | -57 | 15 | 3 | 33 |
| 14 | 1.8 | -69 | 15 | -9 | 21 |

### Downconverter (ADL5350 / GRF7001 / ADL5801)

### Vector Demodulator (ADL5380)

### Low Noise Amplifier (QPL9057 / GRF2051)

### Analog-to-Digital Converter (ADS4128)

#### Acquisition Range

The signal that is expected at the input of the ADC is an amplified version of the Minimum / Maximum Power. The ADC must have a dynamic range large enough to support the full power range expected at the output of the receiver block.

The following table lists the minimum input power detectable with an ideal ADC and a given voltage reference.

|  |  |  |  |
| --- | --- | --- | --- |
| Bits | Reference (V) | Resolution (mV) | Power (dBm) |
| 8 | 1.8 | 7.03 | -33 |
| 10 | 1.8 | 1.76 | -45 |
| 12 | 1.8 | 0.439 | -57 |
| 14 | 1.8 | 0.110 | -69 |

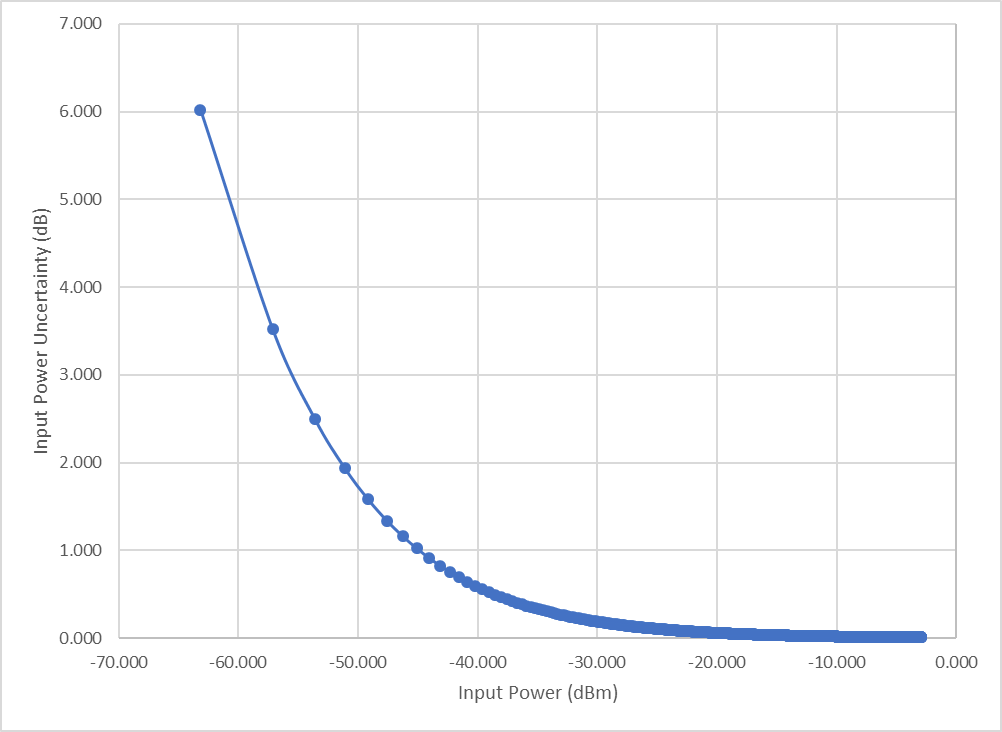
This table ignores any temperature drifting and aging effects that might cause the effective number of bits (ENOB) to be reduced. When the input power is near the LSB each increment has an uncertainty of about 6 dB. This is far too large for our application so to mitigate this the design must ensure that the signal power seen at the ADC input is 10 dB larger than the LSB.

Table 1: Ideal 12-bit ADC with 1.8 V Reference

|  |  |  |  |
| --- | --- | --- | --- |
| N | Input (mV) | Power (dBm) | (dB) |
| 1 | 0.44 | -57.14 | 6.02 |
| 2 | 0.88 | -51.12 | 3.52 |
| 3 | 1.32 | -47.60 | 2.50 |
| 4 | 1.76 | -45.10 | 1.94 |
| 5 | 2.20 | -43.16 | 1.58 |
| 6 | 2.64 | -41.58 | 1.34 |
| 7 | 3.08 | -40.24 | 1.16 |
| 8 | 3.52 | -39.08 | 1.02 |
| 9 | 3.96 | -38.06 | 0.92 |
| 10 | 4.39 | -37.14 | 0.83 |

|  |  |  |  |
| --- | --- | --- | --- |
| Bits | Reference (V) | (dB) | Minimum Input Power (dBm) |
| 8 | 1.8 | 0.5 | -8 |
| 10 | 1.8 | 0.5 | -20 |
| 12 | 1.8 | 0.5 | -32 |
| 14 | 1.8 | 0.5 | -44 |

This table shows that to have an input power measurement uncertainty less than 0.5 dB the input power must be greater than the calculated minimum power. Since the expected dynamic range is -65 dBm – (-90 dBm) = 25 dB and given that most devices saturate somewhere at or near 0 dBm the only options available to us is to use 12 bit or 14 bit ADC.



To ensure that the resolution error is less than 0.5 dB the input power to the ADC should be greater than -35 dBm. The system gain should be enough to bring the minimum input of -90 dBm to our minimum ADC level of -35 dBm. This puts the system gain at 55 dB. The maximum input power is -65 dBm which means the maximum level at the ADC input will be -10 dBm.

#### Sampling Rate

In order to achieve a range resolution of less than 5 m using the pulse radar technique the pulse generated must be lower than 30 ns. This pulse width can be considered as the half-period of a periodic modulation meaning that the fundamental frequency is approximately 16.7 MHz.

The Nyquist criteria dictates that the sampling rate must be twice as large as the highest frequency content. Since the pulse is rectangular the spectrum will contain only odd harmonics. To preserve the first six harmonics a filter would have to be designed at 100 MHz which places the minimum sampling rate at 200 MSps.

In order to reduce the range resolution to 2 m the sampling rate needs to be increased to 500 MSps and the cutoff frequency of the filter will need to be increased to 250 MHz.

Therefore, the sampling rate needs to be 200 – 500 MSps.

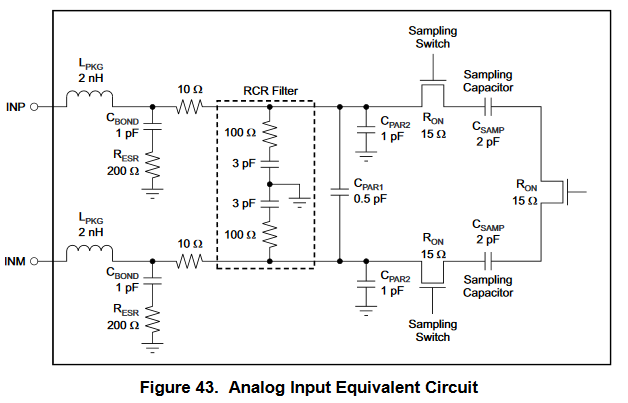
The transmit signal will not be a continuous waveform. Instead it will be a periodically pulsed 3 GHz signal.

Let the bandwidth be the first point where the Fourier coefficient becomes 0. This point accounts for 90% of the signal energy.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Pulse Width (ns) | Duty Cycle | n | Bandwidth (MHz) | Min. Distance (m) |
| 10 | 0.0250 | 80 | 200 | 2.25 |
| 15 | 0.0375 | 54 | 135 | 3.00 |
| 20 | 0.0500 | 40 | 100 | 3.75 |
| 25 | 0.0625 | 32 | 80 | 4.50 |
| 30 | 0.0750 | 27 | 67 | 5.25 |
| 35 | 0.0875 | 23 | 57 | 6.00 |
| 40 | 0.1000 | 20 | 50 | 6.75 |

#### Analog Input

The analog input consists of a switched-capacitor-based, differential, sample-and-hold architecture. This differential topology results in very good ac performance even for high input frequencies at high sampling rates. The INP and INM pins must be externally biased around a common-mode voltage of 0.95V, available on the VCM pin. For a full-scale differential input, each input INP and INM pin must swing symmetrically between (VCM+ 0.5 V) and (VCM– 0.5 V), resulting in a 2-VPP differential input swing. The input sampling circuit has a high 3-dB bandwidth that extends up to 550 MHz (measured from the input pins to the sampled voltage). Figure43 shows an equivalent circuit for the analog input.

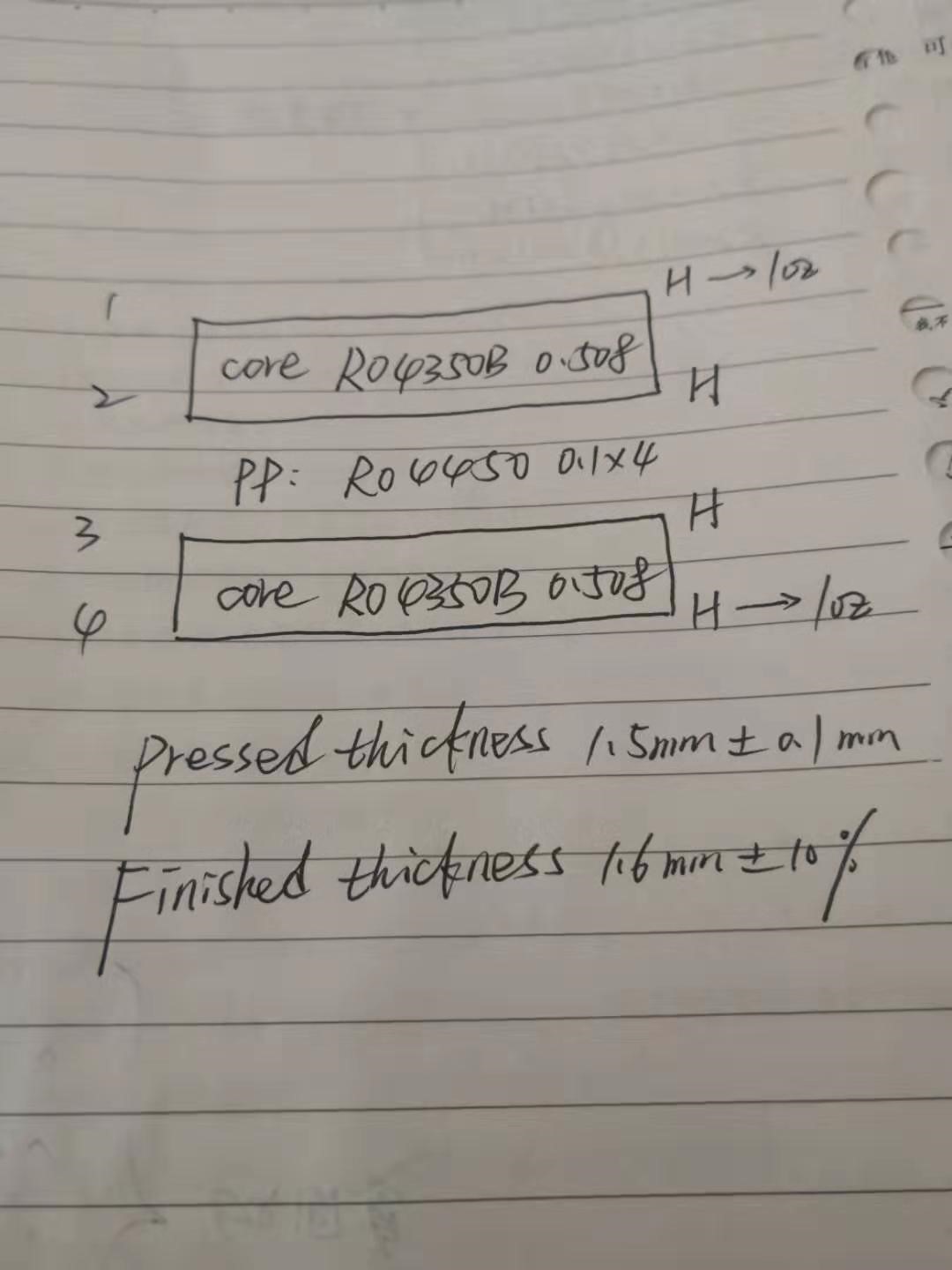


## Antenna

### Patch Antenna

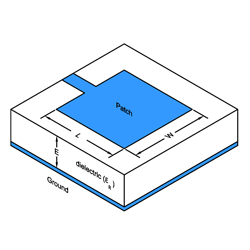
#### PCBWay

##### Layer Stack-up



##### Geometry

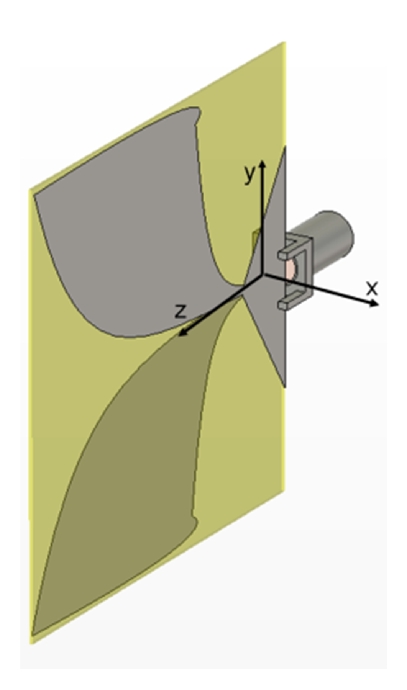
<https://www.pasternack.com/t-calculator-microstrip-ant.aspx>



### Antipodal Vivaldi Antenna

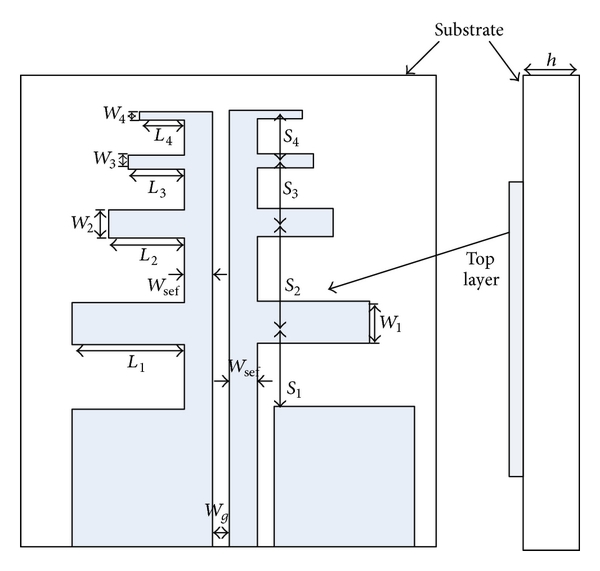
<https://www.hindawi.com/journals/ijge/2012/916176/>

<https://www.hindawi.com/journals/ijap/2017/9627649/>



### Printed Log-Periodic Dipole Antenna (PLPDA)

<https://www.hindawi.com/journals/ijap/2013/430618/>



Where is the total length from either end of the dipole, and is the scale factor. Look up Carrel’s Method for information regarding , , and .

Optimize

### Horn Antenna

#### Circular

#### Octagonal

## Power Divider

### Wilkinson

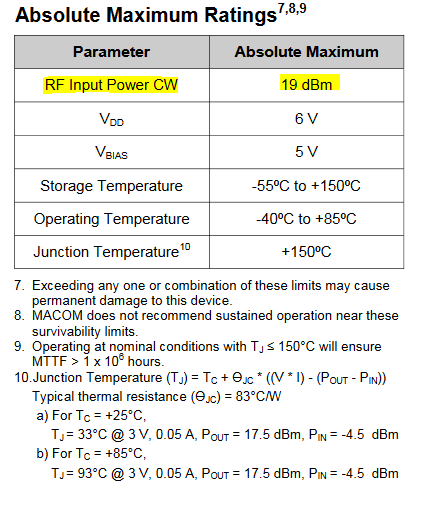
### Resistive

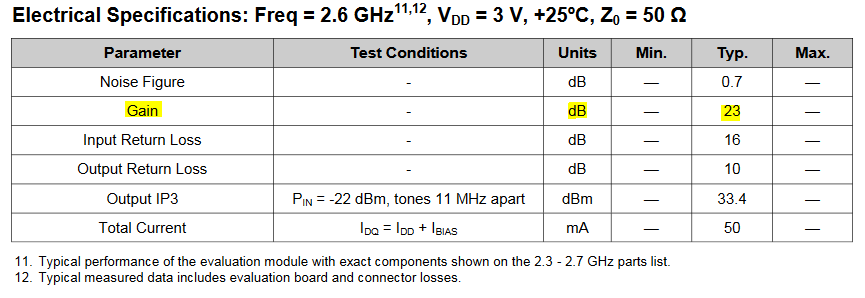
# Link Budget Analysis

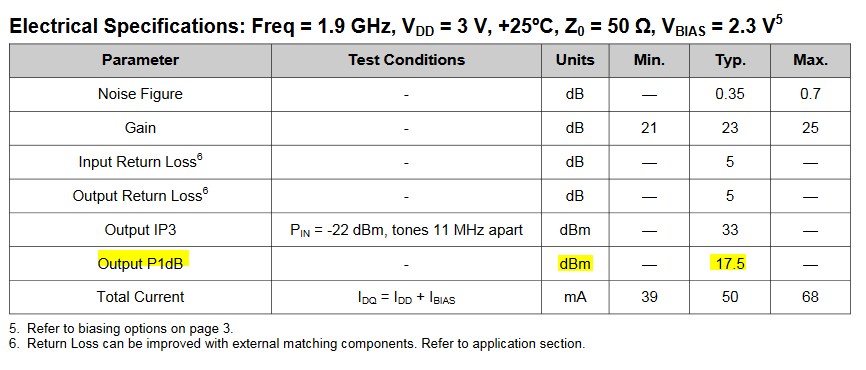
# Fault Analysis

## Receiver Damage Point

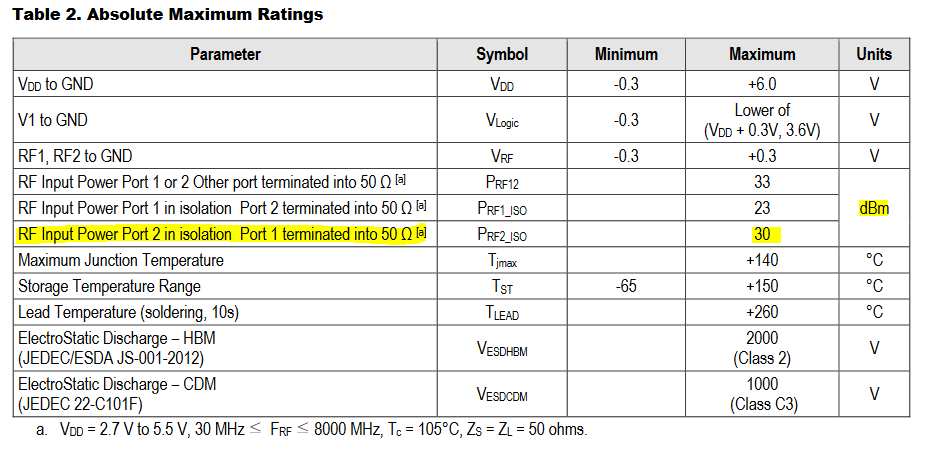
### Low-Noise Amplifier (MAAL-011078)

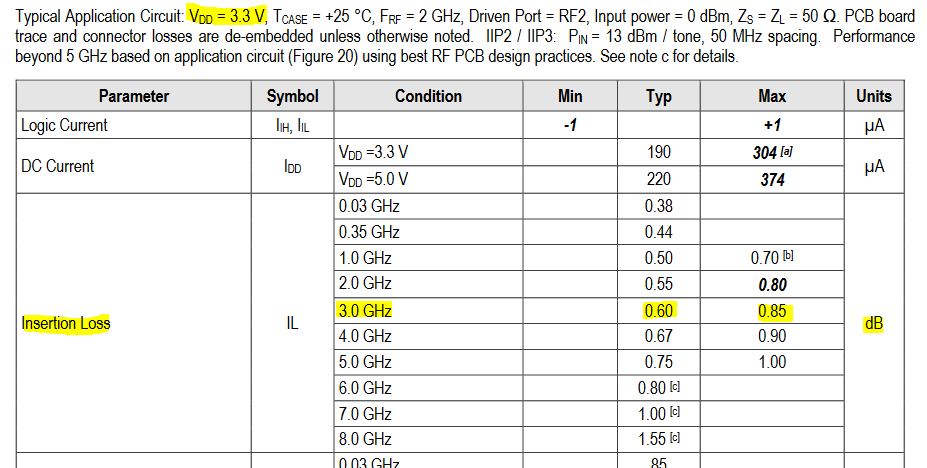




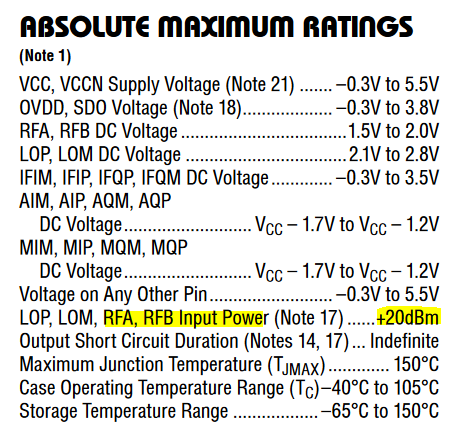


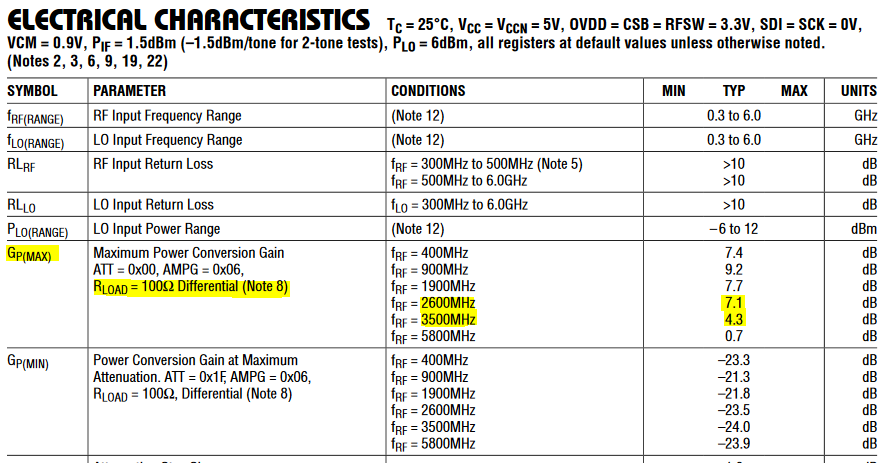
### Switch (F2910)





### Mixer (LTC5586)





### ADC (ADS4128)