**RISC-V Class Project Phase 10 – Project Report**

1. **Optimization Process Description**

After running the base test, I decided to first test the cache modes. Tests 1 and 2 were used to test changing the mode variable – as expected, a writeback cache is more efficient than a writethrough. The data memory is only accessed and changed when the cache line is changed in a writeback as compared to writing every time the cache data is replaced in writethrough, so memory writes are drastically decreased. Tests 3 through 7 were then experimenting with the number of words per cache and memory line. Since the number of words per memory line must be less than or equal to the number of words per cache line, the combinations of 1/0, 2/0, 1/1, 2/1, and 2/2 were all tested, with 1/2, 0/1, and 0/2 invalid and 0/0 already tested in Tests 1 and 2. The best result from these tests were 4 words per cache line and 4 words per memory line (2/2) – these conditions create the largest cache and memory lines, increasing the odds that the data requested has already been moved to the cache (spatial locality). Finally, Tests 8 through 12 were used to gradually expand the cache size. Each increment in cache size (doubling, since it is log2) decreased the cost only slightly, but enough to make an improvement of 120 points by the final test. Thus, the best cache configuration is a 4 word per line writeback cache reading from a 4 word per line memory with 2^7 lines.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Test # | MODE | CWDS | MWDS | CAC\_INDEX | Cost | Hit Ratio |
| 0 | 0 | 0 | 0 | 2 | 7,609,142 | 0 |
| 1 | 1 | 0 | 0 | 2 | 7,134,002 | 13 |
| 2 | 2 | 0 | 0 | 2 | 5,703,021 | 33 |
| 3 | 2 | 1 | 0 | 2 | 8,065,964 | 49 |
| 4 | 2 | 2 | 0 | 2 | 10,448,762 | 65 |
| 5 | 2 | 1 | 1 | 2 | 3,760,520 | 59 |
| 6 | 2 | 2 | 1 | 2 | 4,988,186 | 70 |
| 7 | 2 | 2 | 2 | 2 | 2,257,898 | 79 |
| 8 | 2 | 2 | 2 | 3 | 2,257,894 | 79 |
| 9 | 2 | 2 | 2 | 4 | 2,257,886 | 79 |
| 10 | 2 | 2 | 2 | 5 | 2,257,870 | 79 |
| 11 | 2 | 2 | 2 | 6 | 2,257,838 | 79 |
| 12 | 2 | 2 | 2 | 7 | 2,257,774 | 79 |

1. **Final Configuration**

CACHEMODE = 2 (writeback structure)

CWDS = 2 (4 words per line)

MWDS = 2 (4 words per line)

CAC\_INDEX = 7 (2^7 lines)

Cost = 2,257,774

Cache Size in Bytes = 2 bytes/word \* 4 words/line \* 2^7 lines = 2^10 bytes = 1024 bytes

Address Fields

Byte Offset = 2 ([1..0])

Block Offset = 2 ([3..2])

Index = 7 ([10..4])

Upper Address = 21 ([31..11])

Transfer Cycles = 4 words/cache line / 4 words/memory line = 1