

## **ECEN3002 Lab 3**

**Due Thursday, September 17<sup>th</sup>, 3:45pm**

**24 points (each question is 3 points)**

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The purpose of this lab is to familiarize yourself with the Quartus Timing Analyzer tool, and to work through a simple design to demonstrate the concepts of Setup Slack timing and Hold Slack timing.

A timing cheat sheet is provided on the next page for your reference.

Work through this lab and answer questions where indicated. I encourage you to not speed through this Lab but to take the time to understand what you see and what is being asked. There is no more critical skill needed to be a successful FPGA designer than a competent understanding of timing and how timing is reported.

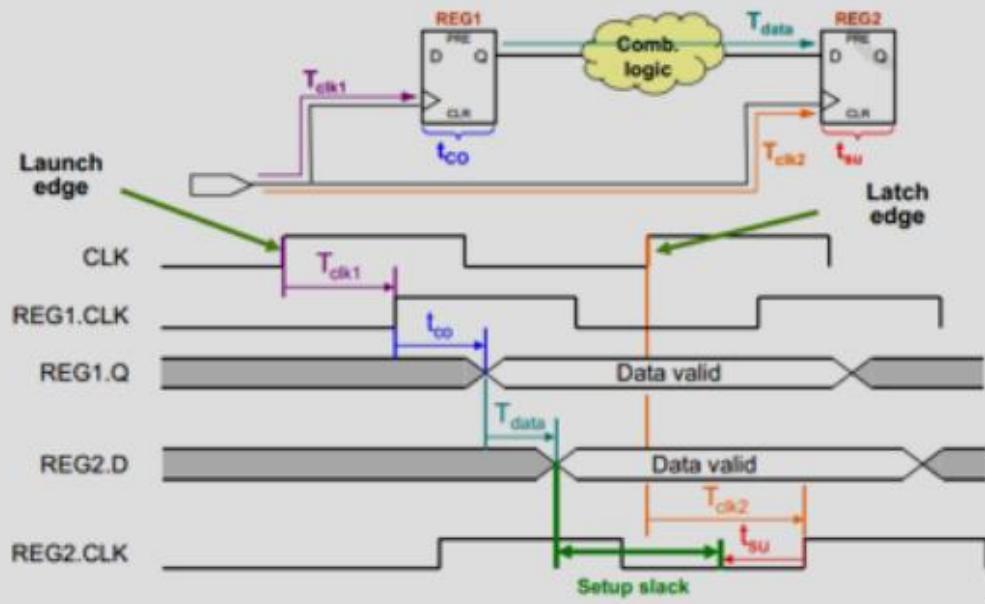
Quartus provides a tool called Timing Analyzer that can be used to create timing constraints for a design, and to allow you to analyze design timing to whatever level of detail you wish. You should use Timing Analyzer to assist you in the creation of timing constraints, and also to analyze failing timing path so that you can make the appropriate modifications to achieve timing closure.

FPGA vendors, and Intel is no exception, report timing values in a format that matches their internal representations. The reports are often difficult to decipher, especially if you are attempting to understand every detail. Areas of confusion will be pointed out as you work through this lab. We will not have time in this class to become experts in all aspects of timing analysis, or experts in Quartus Timing Analyzer reporting. However, if you have specific questions please contact the instructor or TA and we will work to get you answers.

*Setup Slack = Min Data Required Time (setup) – Max Data Arrival Time*

*Data Required Time(setup) = Latch Edge + clock delay to destination register – setup time*

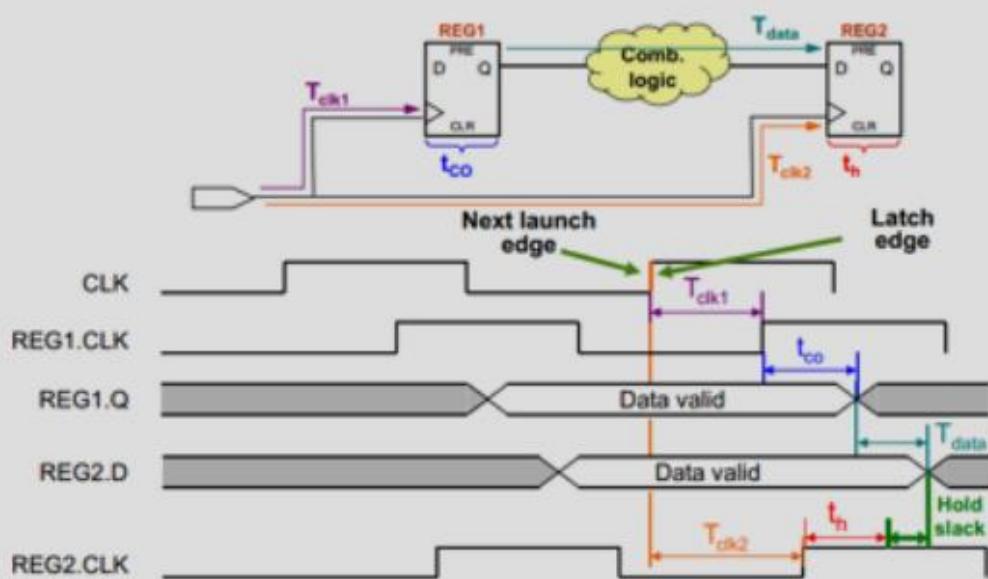
*Data Arrival Time = Launch Edge + clock delay to source register + clock to out time + max propagation delay between registers*



*Hold Slack = Min Data Arrival Time – Max Data Required Time (hold)*

*Data Required Time(Hold) = Latch Edge + clock delay to destination register + hold time*

*Data Arrival Time = Latch Edge + clock delay to source register + clock to out time + min propagation delay between registers*



## Part 1

1. Create a new Quartus project. The Verilog source file for this project is Lab3.v (provided). Review the file to understand the design. Note the use of **synthesis keep** directives which prevent the compiler from optimizing any of the logic, in order to help us better understand what Timing Analyzer reports. **Make sure you do not have a .sdc file in your project directory**, as we will create this file later in the lab.

You will not use your DE10-Standard board for this lab, so pin assignments are not necessary.

2. Compile the design in Quartus. Notice that the Timing Analyzer header in the Table of Contents is red, indicating timing errors. The reason for this is that Quartus assumes a clock period of 1ns for all clocks that are not properly constrained. Since we do not have a .sdc file in the project, our clock period is assumed to be 1 ns. You can see this by selecting the Clocks section under Timing Analyzer in the Table of Contents.

The screenshot shows the Quartus Table of Contents window. On the left, there is a tree view of project components. Under the 'Timing Analyzer' node, the 'Clocks' item is selected and highlighted with a blue border. The main pane on the right is titled 'Clocks' and displays a table with one row. The table has columns for 'Clock Name', 'Type', 'Period', and 'Frequency'. The single entry is 'clock' (Type: Base, Period: 1.000, Frequency: 1000.0 MHz).

	Clock Name	Type	Period	Frequency
1	clock	Base	1.000	1000.0 MHz

3. Right click on clock in the Clocks section above, and select Report Timing.

The screenshot shows a context menu for the 'clock' entry in the 'Clocks' table. The menu items include: Copy (Ctrl+C), Select All (Ctrl+A), Undo Sort, Collapse All, Expand All, Edit Clock Constraint... (In Timing Analyzer UI), Create Setup Slack Histogram (In Timing Analyzer UI), Report Timing... (In Timing Analyzer UI), Remove Clock... (In Timing Analyzer UI), and Locate Node.

4. Timing Analyzer opens, and a Report Timing window is displayed. In the From clock: drop down, select or enter clock. At the bottom of the Report Timing window, notice that a Tcl command has been created that

shows the command that will be run when the Report Timing button is pressed. As you become more familiar with Quartus and Timing Analyzer, you may want to create your own scripts to automate certain steps, so you can use the Tcl command from this window to help with creation of your scripts. For now, we will just press the Report Timing button.

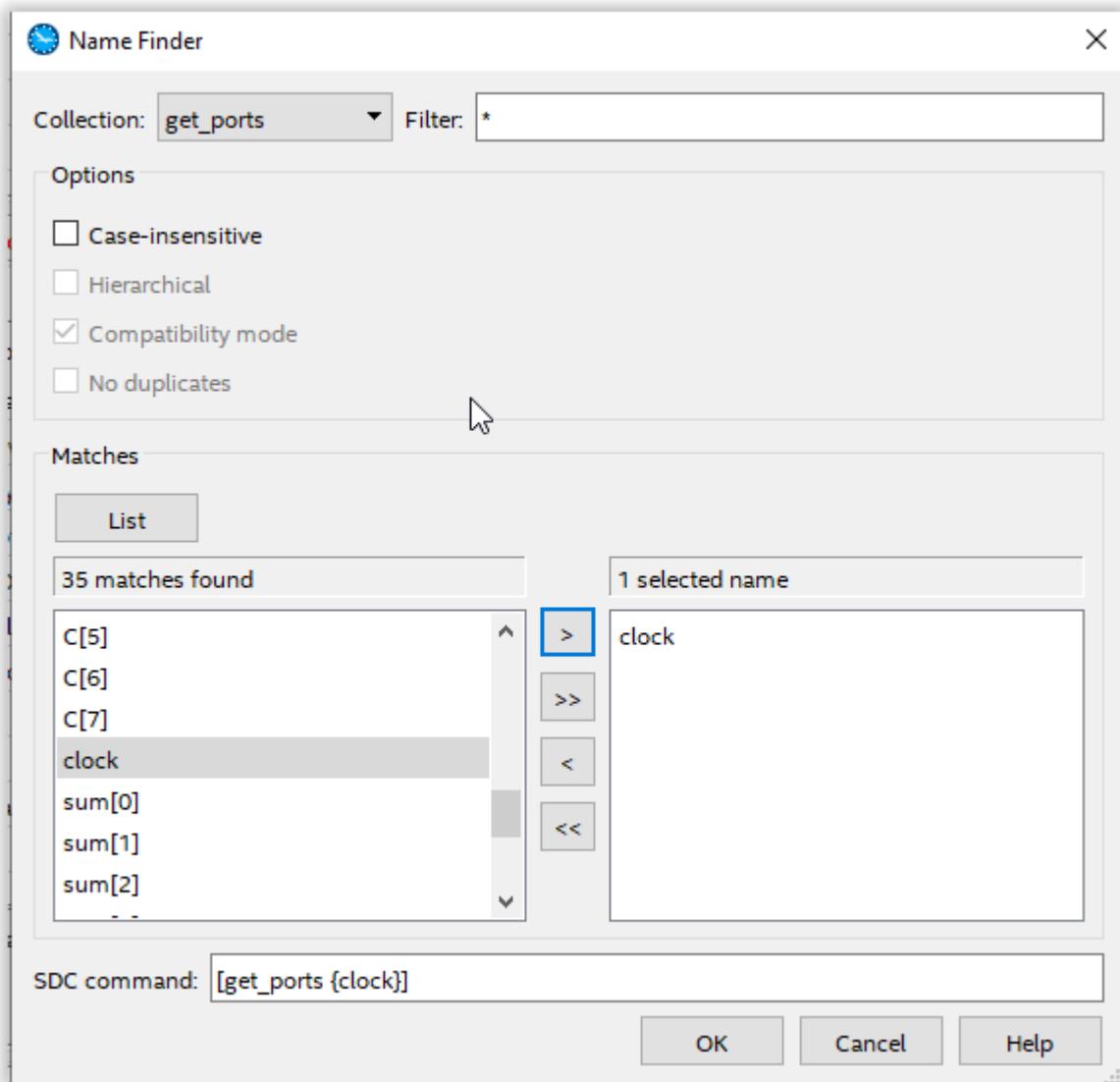
- 0.955 ns

Question 1: What is the worst case Setup Slack value?

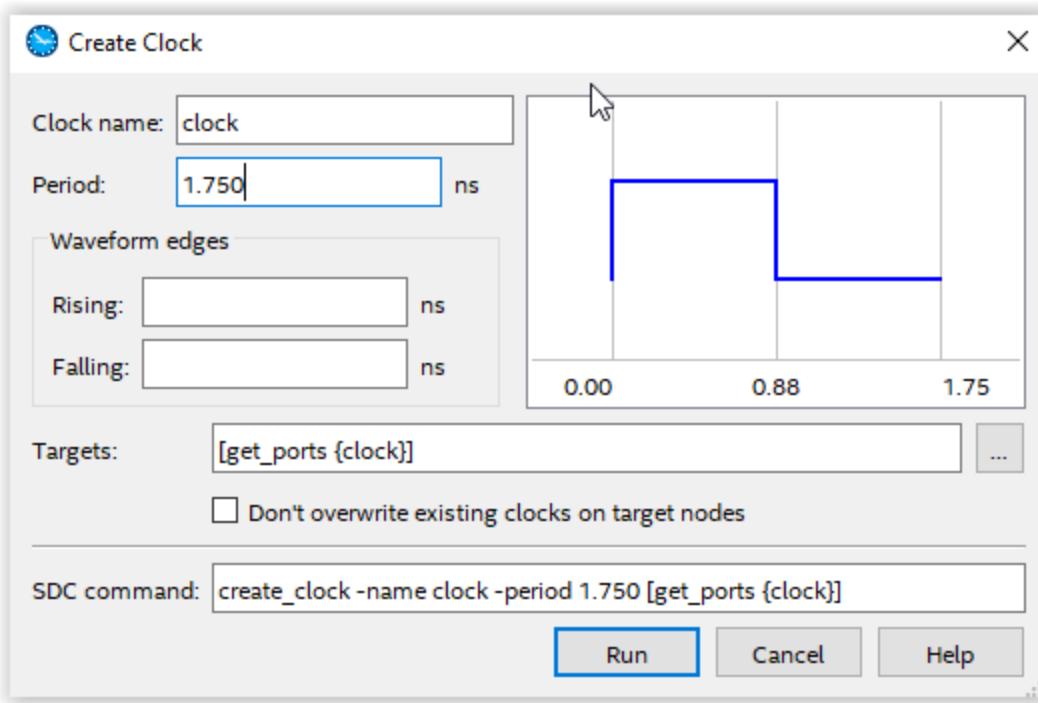
The worst case value is the first value displayed.

5. At this point we probably don't care what Timing Analyzer is reporting, because Timing Analyzer is assuming a 1ns period for clock. We need to provide a clock period constraint that matches the clock in our design.

6. Assume we want our clock period to be 1.75ns, which corresponds to approximately 570Mhz. To create this constraint, go to Constraints > Create Clock, and the Create Clock window opens. For Clock name:, enter clock. For Period, enter 1.750, and for Targets, click the 3 dots to open the Name Finder Window. Click the List button, select clock and add it to the selected signal list, and close the window. Notice that the SDC command is created.

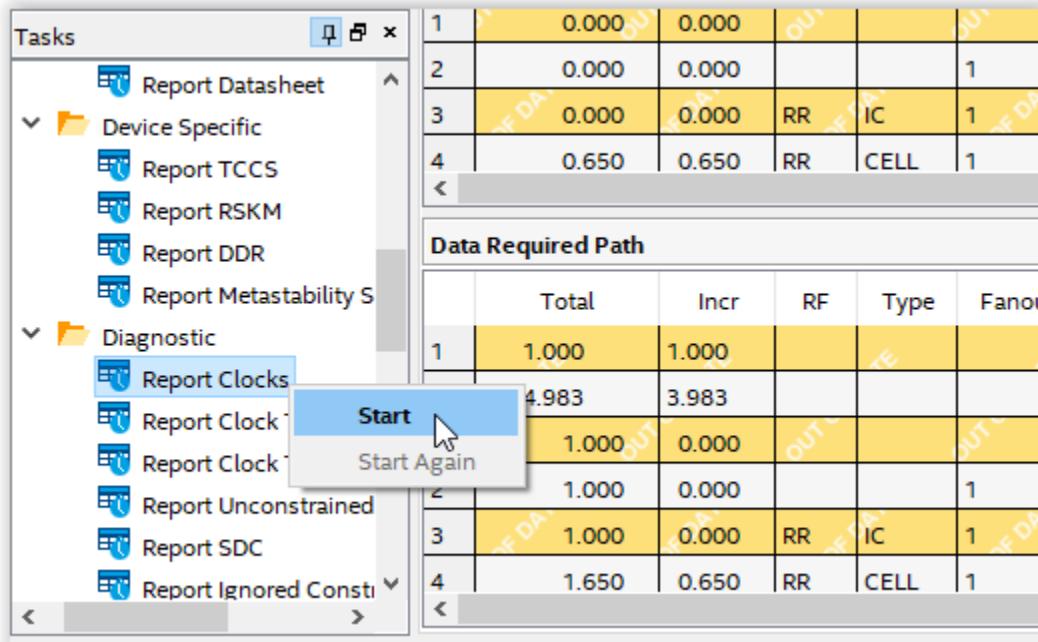


The Create Clock window will look like this.



Hit the Run button. The Timing Analyzer main screen will show a lot of yellow highlights, which indicates that a constraint has been changed and that the report needs to be regenerated.

7. Locate Report Clocks in the Tasks pane, right click and select Start. When the Clocks Summary window is displayed, repeat the step from step 3 above to create a new timing report.



Question 2: What is the worst case Slack reported?

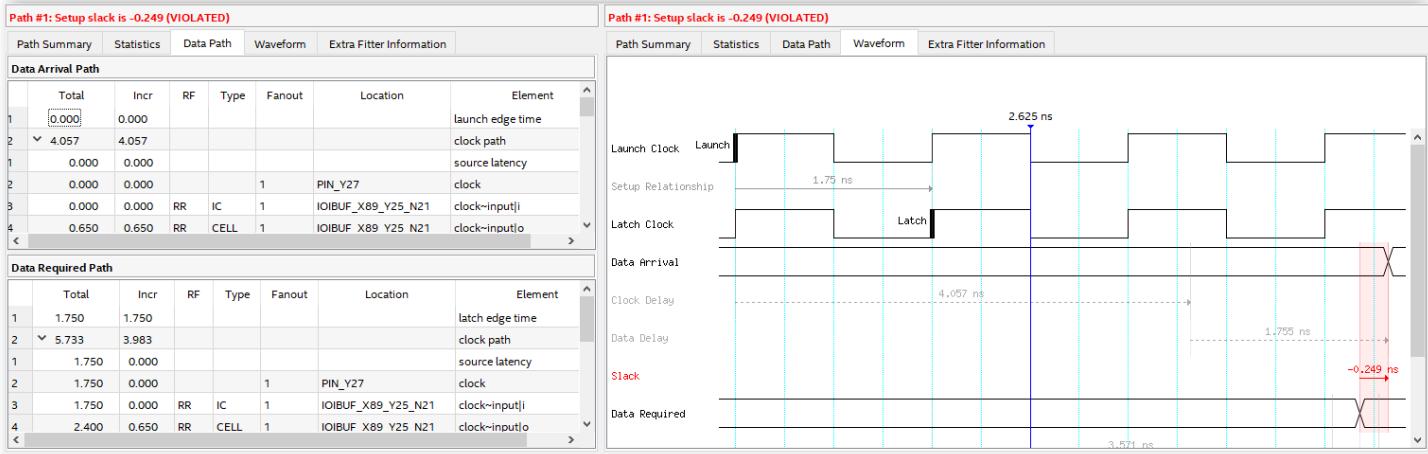
~ 0.205 ns

## Part 2

You will now use Timing Analyzer to see how the timing information is provided, and how the Slack calculations are done.

The information displayed in the various panes of Timing Analyzer will match the specific path that is highlighted in the Summary of Paths tab. Highlight Line 1 so we see the timing information for the worst case path (the path with the largest negative Slack).

The center section of the Timing Analyzer display allows you to display different information. To begin, make sure that you select the Waveform tab on the right side of the screen.



1. Start by selecting the Path Summary tab on the left side of the view above. You can see information on the failing path, the launch and latch clocks, the Data Arrival and Data Required Times, and the resulting Slack (which is a negative value in this example, meaning the design has a timing violation).

Question 3: What is the worst case path? from rg\_c[1] to rg\_sum[8]

2. Look at the Statistics tab. A given data or clock path delay is the sum of logic (Cell) and interconnection (IC) delays, and this view shows the percentages in the % of total column. If you are trying to determine how to address a timing problem, a path that has a high percentage of logic delay can usually be recoded to modify the logic created (or maybe you add pipeline registers). This usually indicated a large number of logic element blocks in a path. Paths that are a large percentage of routing delay can sometimes be improved by doing manual placement of logic blocks, to bring those blocks closer together.

Path Summary		Statistics	Data Path	Waveform	Extra Fitter Information		
	Property	Value	Count	Total Delay	% of Total	Min	Max
5	Physical Delays						
1	Arrival Path						
1	Clock						
1	IC	3	2.566	63	0.000	2.075	
2	Cell	3	1.491	37	0.382	0.650	
2	Data						
1	IC	9	0.244	14	0.000	0.244	
2	Cell	10	1.511	86	0.000	0.858	
3	uTco	1	0.000	0	0.000	0.000	
2	Required Path						
1	Clock						
1	IC	3	2.155	60	0.000	1.694	
2	Cell	3	1.416	40	0.356	0.650	

3. Select the Data Path tab on the left hand side of the Timing Analyzer screen.

Path Summary		Statistics	Data Path	Waveform	Extra Fitter Information		
<b>Data Arrival Path</b>							
	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	> 4.057	4.057					clock path
3	> 5.812	1.755					data path
<							
<b>Data Required Path</b>							
	Total	Incr	RF	Type	Fanout	Location	Element
1	1.750	1.750					latch edge time
2	> 5.733	3.983					clock path
3	5.563	-0.170					clock uncertainty
4	5.563	0.000	uTsu	1		FF_X74_Y4_N25	reg_sum[8]

The top half of the display shows the details of the Data Arrival Path, and the bottom half shows the details of the Data Required Path.

The Data Arrival Path is defined as the latch clock delay + tco + the data path delay. The launch clock delay is shown to be 4.057ns, and the data path delay is 1.755ns, for a total data arrival time of 5.812ns.

Data Arrival Path							
	Total	Incr	RF	Type	Fanout	Location	Element
2	4.057	4.057					clock path
1	0.000	0.000					source latency
2	0.000	0.000			1	PIN_Y27	clock
3	0.000	0.000	RR	IC	1	IOIBUF_X89_Y25_N21	clock~input i
4	0.650	0.650	RR	CELL	1	IOIBUF_X89_Y25_N21	clock~input o
5	1.141	0.491	RR	IC	1	CLKCTRL_G10	clock~inputCLKENA0 ir
6	1.523	0.382	RR	CELL	34	CLKCTRL_G10	clock~inputCLKENA0 o
7	3.598	2.075	RR	IC	1	FF_X74_Y4_N35	reg_B[1] clk
8	4.057	0.459	RR	CELL	1	FF_X74_Y4_N35	reg_B[1]

4. An analysis of the clock arrival time can be done using the expanded view above.

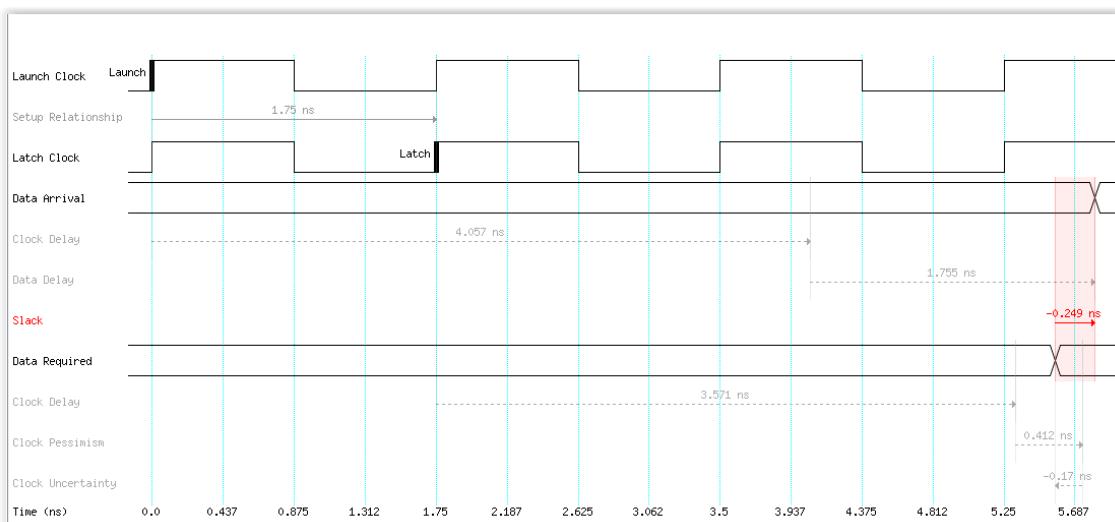
When you see IC in the Type column, the value displayed is a routing or interconnect (IC) delay. CELL in the Type column indicates logic delay, which can be buffers or logic elements.

Lines 3 and 4 show the delay though the input buffer at the I/O cell of the FPGA where the clock is connected. The delay of this input buffer is 650ps. The output of this buffer is then routed to a global clock buffer (Lines 5 and 6). The routing delay is 491ps, and the global clock buffer propagation delay is 382ps.

The delay of the clock from the global clock buffer consists of the main clock route (2.075ns) plus delay as the clock enters the LE and is routed to the destination register (459ps). The sum of all these delays results in the 4.057ns clock path delay.

5. Expanding the data path section of the Data Arrival Path window shows many rows of delays, and many of the delays are Ons. This highlights the situation where the Intel timing database often combines look up table delays with route delays to adjacent look up tables, which makes the table difficult to decipher. You may never need to understand all the details in this table, so review the details, but don't worry about identifying everything. The important information is the overall data path delay.

6. Review the waveform view on the right side of the display and answer the following questions.



**Question 4:** What is the relationship of the Latch Edge to the Launch Edge?

The launch edge is the clock edge upon which a source register outputs its data; the latch edge is the clock edge upon which a destination register accepts the input from its input port. The latch edge always occurs after the launch edge, but it is not always exactly 1 cycle.

**Question 5:** Why does this design demonstrate negative slack? Try to explain what is happening in words, and not in an equation.

This design demonstrates negative slack because, as calculated by the Timing Analyzer, the data in this program would not physically travel fast enough to be properly processed at the current clock speed.

7. Two bottom two items shown on the timing diagram are Clock Pessimism and Clock Uncertainty. What are those items?

Clock pessimism explained by Intel:

Within a timing corner, there are two timing "sub-models", basically a fast and a slow timing model. So when doing setup analysis on a path, it will use the slow sub-model for the source clock and data delay, and the fast sub-model for the destination clock path. For hold analysis on the exact same path, it will do the opposite. If you compare setup and hold analysis on the exact same path, you can visually see different numbers. Part of this is rise-fall variation, but a large component is for On-Die Variation, which models the fact that different paths may not be at the exact fastest or slower allowed at the same time. This is all a good thing.

The problem is that the same clock feeds the source and destination. It's impossible to have on-die variation and rise/fall variation on the exact same signal, so it goes up to the point until the clock tree split, figures out how much pessimism was added because of these two models, and removes it. Again, it makes timing easier and is correct.

Got that?

There is a launch clock and a latch clock. The timing tool will make worst case assumptions on delays for both clocks, in order to model timing in a conservative manner. As mentioned above for setup time analysis, the launch clock will be modeled with the slow timing model, and the latch clock will use the faster timing model. However, there is a large section of the overall launch and latch clock paths that share common buffers and routing. For the sections of the clock paths that are identical for the launch and latch clocks, it makes no sense to model the timing as different, the timing must be identical.

Once the launch clock path is analyzed using the slow timing model, and the latch clock path is modeled using the fast timing model, the overall timing is much more pessimistic than reality, since much of the clock paths are identical. The differences on the common portion of the path are then removed, making the calculation match reality, and this removal value is called clock pessimism. Clock pessimism is your friend, and something that must be calculated by the timing tool.

What about clock uncertainty?

Clock uncertainty is a catch all phrase for (primarily) different types of clock jitter that occur that reduce overall timing margins. We will discuss jitter (briefly) in the lectures. For now recognize that real world imperfections do have small negative impacts on timing margins, and Quartus will provide realistic clock uncertainty values when clock constraints are created by Timing Analyzer.

8. Go to Constraints > Create Clock, and change the clock period to 4 ns, and regenerate the timing report.

2.045 ns

Question 6: What is the worst case Setup Slack now?

Yes!

Question 7: Does the design meeting timing?

### Part 3

1. Before closing Timing Analyzer, look in your project directory. Do you see a .sdc file?

The answer should be no. Even though a clock constraint was created, you need to explicitly write the constraint into an .sdc file, otherwise the constraints may be lost when Timing Analyzer is closed. Timing Analyzer should prompt you to save any .sdc file changes when you close it.

2. Go to Constraints > Write SDC File, and save your .sdc file.

Question 8: What constraints were written into the .sdc file?

```
set_time_format -unit ns -decimal_places 3
```

```
create_clock -name {clock} -period 4.000 -waveform { 0.000 2.000 } [get_ports {clock}]
```

```
set_clock_uncertainty -rise_from [get_clocks {clock}] -rise_to [get_clocks {clock}] -setup 0.100
set_clock_uncertainty -rise_from [get_clocks {clock}] -rise_to [get_clocks {clock}] -hold 0.060
set_clock_uncertainty -rise_from [get_clocks {clock}] -fall_to [get_clocks {clock}] -setup 0.100
set_clock_uncertainty -rise_from [get_clocks {clock}] -fall_to [get_clocks {clock}] -hold 0.060
set_clock_uncertainty -fall_from [get_clocks {clock}] -rise_to [get_clocks {clock}] -setup 0.100
set_clock_uncertainty -fall_from [get_clocks {clock}] -rise_to [get_clocks {clock}] -hold 0.060
set_clock_uncertainty -fall_from [get_clocks {clock}] -fall_to [get_clocks {clock}] -setup 0.100
set_clock_uncertainty -fall_from [get_clocks {clock}] -fall_to [get_clocks {clock}] -hold 0.060
```

Don't forget, you will need to add the .sdc file as a source file in your Quartus project for future compilations.