ECEN3002 Lab2

25 points

Due Thursday, September 10th, 345pm

Learning how to deal with FPGA pinouts, and understanding your options for how you can do so is a very important skill to acquire. The purpose of this lab is provide guidelines for the different options, and have you work through those options and understand the steps. At points along this lab are questions for you to answer. Please answer the questions honestly as it will not impact your grade. The goal is to have everyone successfully complete the lab.

✓ 1. Using your Lab1 project, compile the project and verify that all pins are correctly assigned, the design works on your DE10-Standard board.

✓ 2. Close Quartus. Make a backup copy of your .qsf file. Remove all pin assignment information from your current project .qsf file.

✓ 3. Rerun the project and confirm the missing pin assignments using these methods:
   a. Filter on I/O in the Quartus Transcript Window 23/23 missing
   b. In the Table of Contents in the Compilation Report, Fitter > Resource Section > All Package Pins (sort on User Assignment) All N or blank
   c. In the Table of Contents in the Compilation Report, Fitter > Resource Section > I/O Standards Section > I/O Assignment Warnings "Incomplet"/"Missing"

✓ 4. In your Quartus project, Assignments > Back-Annotate Assignments, and rerun your project. Since the only thing you changed was pin assignments, you can run Rapid Recompile (use the drop down in the Tasks pane, then click on the first item in the task list).
   ✓ a. Recheck the pin assignments like you did in #3 above. The pins should now be assigned, but recognize that the assignments are random and do not match your DE10-Standard board. Do not match copy of .qsf

Note: When you ran the Quartus project with no pin assignments, the Quartus fitter provided random assignments in order to complete the entire compilation flow. In order to update your .qsf file with the fitter assignments, you must run the Back-Annotate Assignment step. Once you do this, your project .qsf file will contain the fitter assignments.

5. Open the Pin Planner. Using information from the backup copy of your .qsf file, modify the Location and I/O Standard for CLOCK_50 to match the DE10-Standard board. Also put in correct Location and I/O Standard information for LEDR[9], including Current Strength of 4ma and Slew Rate of 0 (slowest).
   a. File > Export, and export the .csv file, and then export the .tcl file using the provided drop down item.
   b. Review both files to be certain the expected changes are included. Note that in the .csv file, the new pin locations are written to the Location column, not the Fitter Location column.
   c. Close Pin Planner

Are the .csv and .tcl files as expected?: Yes, both match copy of .qsf

6. In Quartus, open a Tcl console, and type these commands (assumes file name is Pinouts, just use your file name)
   a. source Pinouts.tcl (note, if your tcl file is in another directory, you will need to include directory information.
   b. export_assignments
   c. Review your current .qsf file, you should see the complete pinout in the .qsf file, and that CLOCK_50 and LEDR[9] contain the information from the Pin Planner. You many need to refresh you editor if the file was open when you performed the export_assignments step.

so here is where qsf updates

Do you have a complete pinout, with 2 correct pin locations?: Yes

7. Open the .csv file that was exported from Pin Planner in step 5. Edit the lines containing KEY[0] and KEY[1] by putting in the I/O Locations and I/O Standard setting that match your DE10-Standard board. Note that you need to change the Location field, not the Fitter Location field.
   a. Save the .csv file.
   b. Assignments > Import Assignments, and read in the .csv file.
   c. export_assignments , and verify your changes are now in the .qsf file.
   d. Recompile your design. Did you get errors?

Did you get errors?: _____

Error importing CSV - did not recompile

Do you understand why?: _____

8. Once you assign a few pins with correct pinout and I/O standards, it is possible that the fitter assigned pins will now cause conflicts, usually due to I/O banking rules.

a. Close Quartus, and remove all pinout constraints from your .qsf file. Open Quartus.
b. Open the exported .tcl file, and remove all constraints except constraints for CLOCK_50, KEY[0] and KEY[1].
c. source the .tcl file again, export_assignments, and recompile
d. You should see CLOCK_50, KEY[0], and KEY[1], correctly assigned. Verify this using your preferred method.
e. Back Annotate your current pinout.

Are 3 Pins Correctly Assigned?: Yes, 4 if you count LEDR[9]

9. Open Pin Planner. Modify the locations of some or all remaining incorrectly placed pins using Pin Planner.
   a. You can drag and drop pins on the BGA graphic, or
   b. Use the All Pins view at the bottom of the screen to reassign locations.
   c. Make all LEDR pins 4ma drive strength and slow slew rate.
   d. If you don't correct all pin assignments using Pin Planner, use your method of choice to complete the correct assignments. Follow the approaches you took earlier in this lab.

All Pins Assigned Correctly?: Yes, via TCL

10. Confirm that your design runs correctly on your DE10-Standard board.

Does Your Design Run Properly?: YES!

↑ a little doodle, as requested