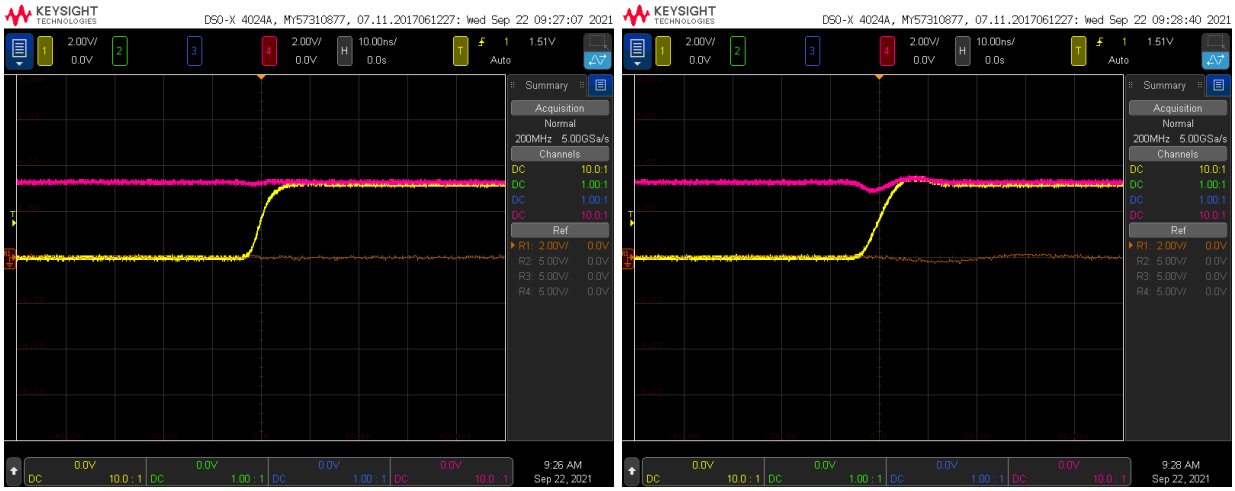
Lab Report 5 - Sam Freed

In this lab, we compared the effects of the design choices we have explored in the past few weeks, namely the location of a decoupling capacitor and the use of a return plane. The sample board's design also reminded us to consider the location and layout of test points and important components in order to increase efficiency.



- Yellow signal is triggering on the Y3 output from the 7414 hex inverter
- Pink signal is the quiet HIGH signal from the 7414 hex inverter
- Orange reference signal is the quiet LOW signal from the 7414 hex inverter

The left image shows the good signal, the layout that follows the standards of the return plane and close proximity decoupling capacitor. The right image shows the bad signal, the layout that was intentionally designed without these strategies. All three signals are affected by the poorer design, with much more switching noise causing voltage fluctuations in all three signals. The HIGH and LOW signals both ring slightly, and the Y3 output actually overshoots its expected voltage by almost half a volt. Even in a relatively simple circuit like this, these design choices can have significant impacts.