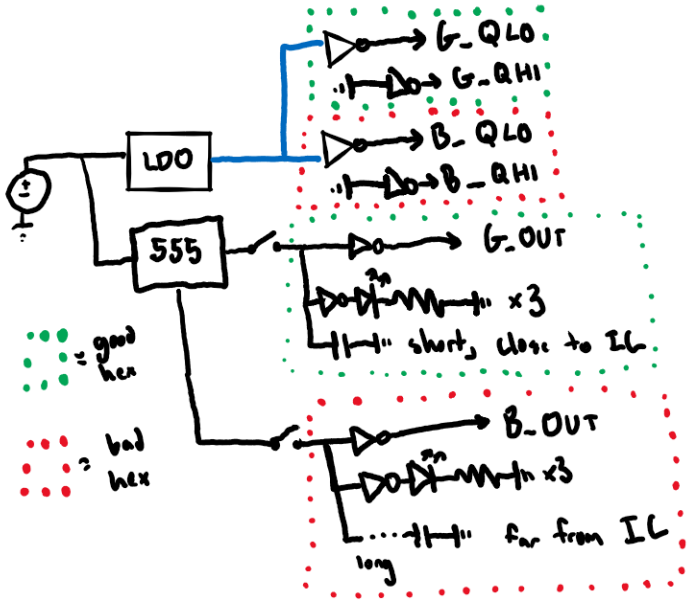
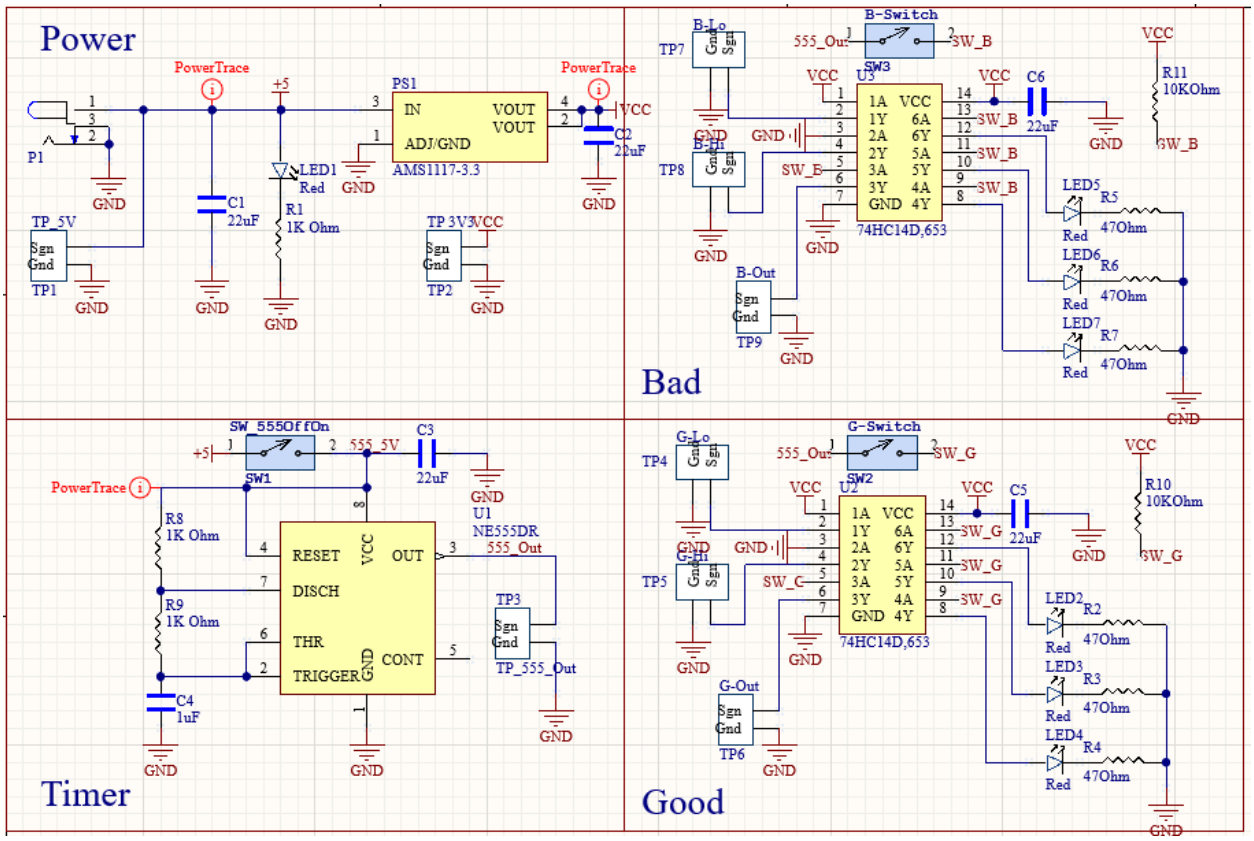
# Board 2 Report - Sam Freed

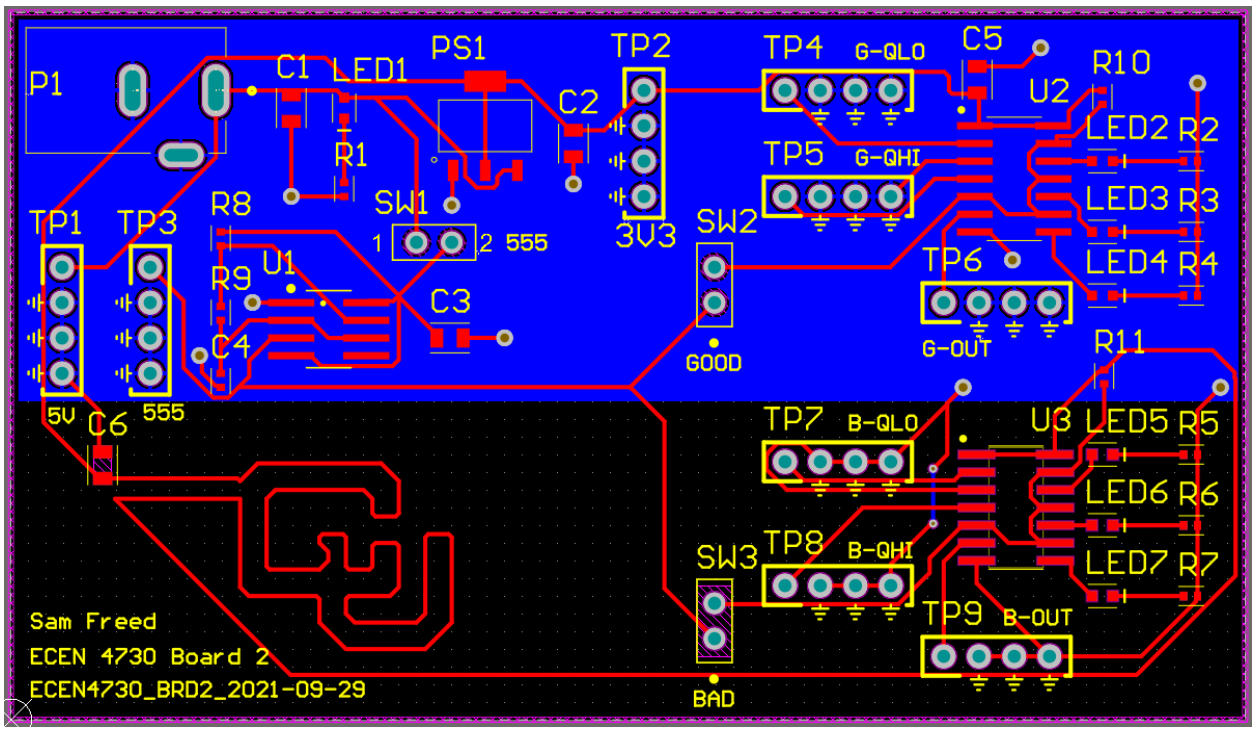
## Engineering Requirements

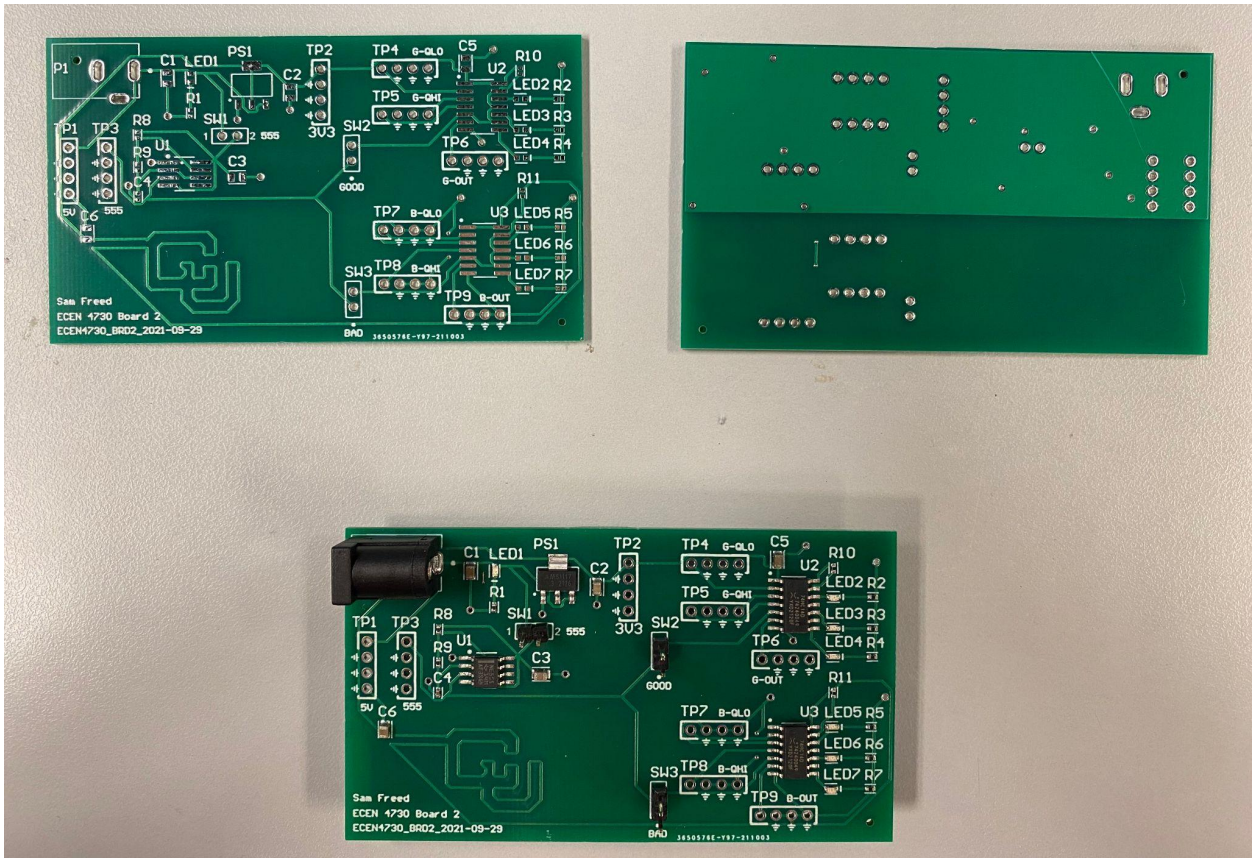
1. Board is powered using a 5V barrel-connector style AC to DC regulator.
2. Low Dropout Regulator (LDO) outputs a steady 3.3V power signal.
3. Indicator LEDs are placed throughout the board to represent the power and signal status of various components.
4. A 555 timer generates a square wave signal at approximately 500Hz and a 65% duty cycle when unloaded.
5. Hex inverters are used to invert signals, both power signals and PWM signals from the output of the 555 timer.
6. The quiet high, quiet low, and inverted 555 signals should be observable using voltage test points.
7. Hex inverters are placed in two different structures: one with good noise-reduction practices, one with poor noise-reduction practices.
8. Switches allow for a division between the different stages of the circuit.

## Board Images: From Sketch to Board



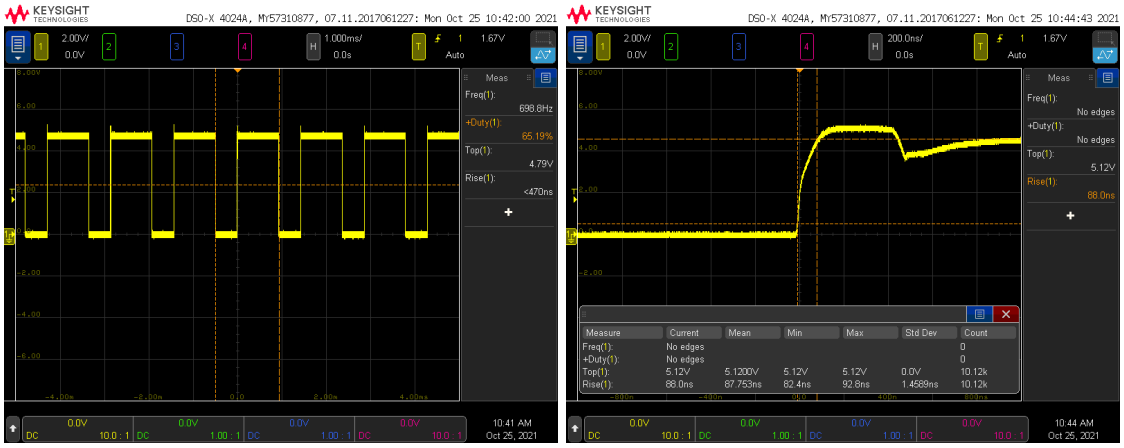

Power
PowerTrace
PS1
IN
VOUT
ADJ/GND
AMS1117-3.3
P1
TP_5V
TP1
C1
22uF
R1
1K Ohm
LED1
Red
TP 3V3
TP2
C2
22uF
VCC
GND
Bad
B-Switch
B-Lo
B-Hi
B-Out
TP7
TP8
TP9
SW3
SW_B
555_Out
U3
74HC14D,653
C6
R11
10KOhm
LED5
LED6
LED7
R5
R6
R7
47Ohm
Timer
SW_555OffOn
SW1
C3
22uF
U1
NE555DR
RESET
DISCH
THR
TRIGGER
OUT
CONT
R8
1K Ohm
R9
1K Ohm
C4
1uF
TP3
TP_555_Out
Good
G-Lo
G-Hi
G-Out
TP4
TP5
TP6
G-Switch
SW2
SW_G
U2
C5
R10
LED2
LED3
LED4
R2
R3
R4


P1
C1
LED1
PS1
C2
TP2
TP4
G-QLO
C5
U2
R10
R1
TP5
G-QHI
LED2
R2
TP1
TP3
R8
SW1
1
2
555
3V3
SW2
LED3
R3
R9
U1
C3
TP6
LED4
R4
C4
G-OUT
GOOD
R11
5V
C6
555
TP7
B-QLO
U3
LED5
R5
LED6
R6
SW3
TP8
B-QHI
LED7
R7
TP9
B-OUT
Sam Freed
ECEN 4730 Board 2
ECEN4730_BRD2_2021-09-29
BAD



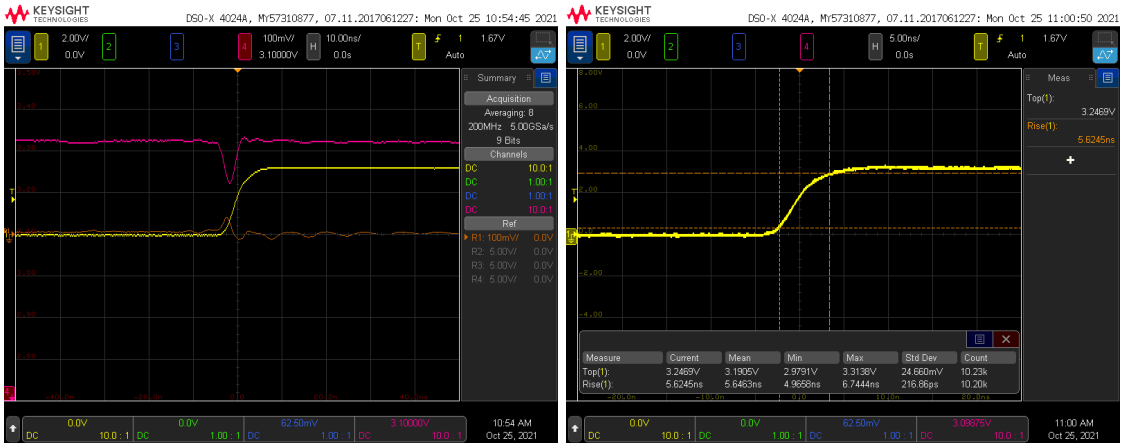

# Key Signals

1. 555 Voltage Output, Unloaded



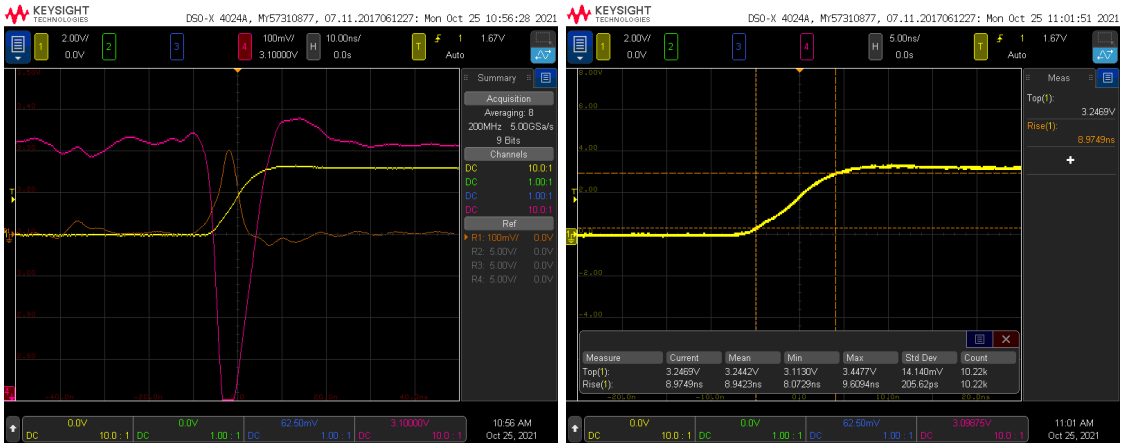

   a. Frequency: 698 Hz - higher than 460Hz from lab 1 but as expected
   b. Duty Cycle: 65% - matches previous expectations
   c. Rise Time: 87.7ns - matches previous expectations
   d. Top Voltage: 4.79V - matches previous expectations

2. Good Noise-Reduction Structure Outputs



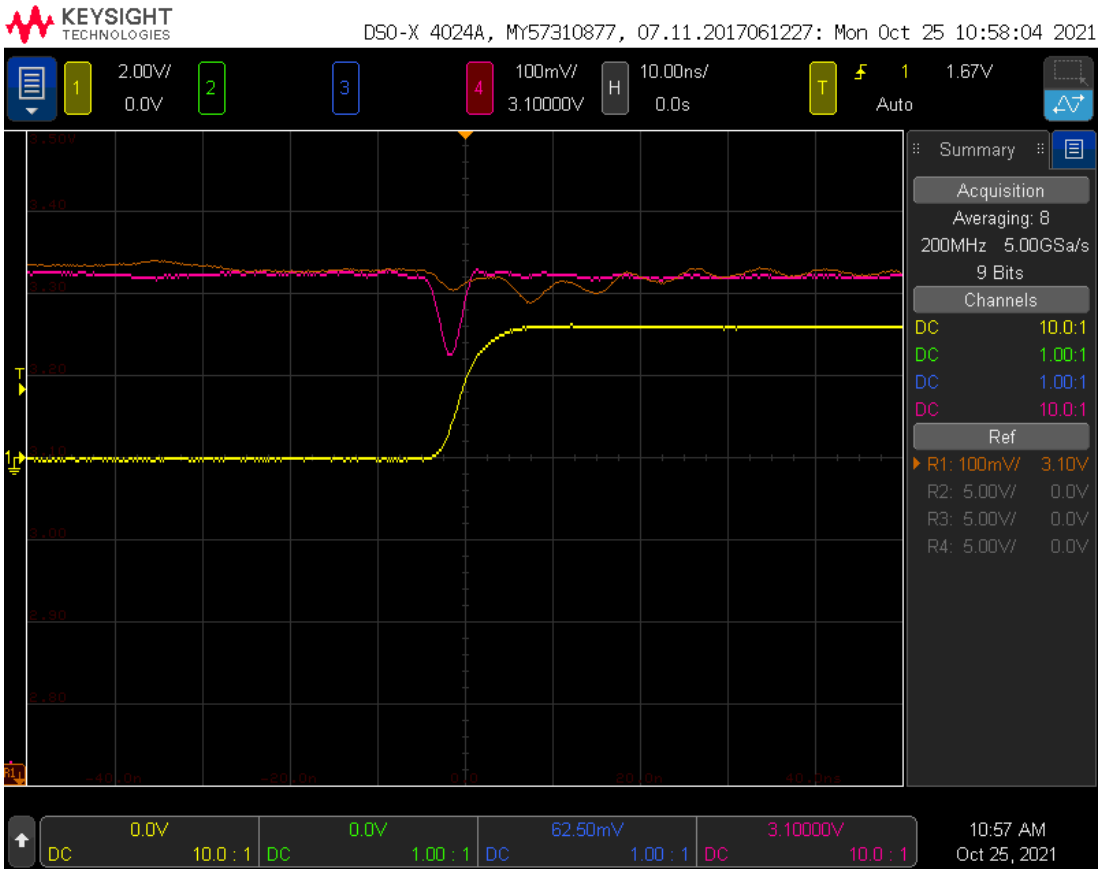

a. Yellow Signal - signal from 555 timer triggering the scope capture, 5.6ns rise time
b. Pink Signal - QHI signal from hex inverter with good design, ~100mV switching noise
c. Orange Signal - QLO signal from hex inverter with good design, ~50mV switching noise

3. Poor Noise-Reduction Structure Outputs




a. Yellow Signal - signal from 555 timer triggering the scope capture, 8.9ns rise time
b. Pink Signal - QHI signal from hex inverter with poor design, >600mV switching noise
c. Orange Signal - QLO signal from hex inverter with good design, 200mV switching noise

4. Noise on 3V3 LDO Output




   a. Yellow Signal - signal from 555 timer triggering the scope capture
   b. Pink Signal - noise on 3.3V rail when poor design was active
   c. Orange Signal - noise on 3.3V rail when good design was active

## Seven Steps

1. POR - The basic structure of the plan of record was provided by the lab guidance, with the goals largely being to recreate the board structure we had been experimenting with in the prior lab session.
2. Preliminary BOM - This was also based on the previous board, however, some of my peers faced some issues with stock concerns from our manufacturer.
3. Final Schematic and BOM - These were finalized as I recreated the board in my own structure.
4. Board Layout and Parts - Completing my own layout was somewhat difficult, as the design rules I had set for trace widths did not transfer over properly, so all of the traces ended up being 15mil, the Altium default. Aside from this, this step was relatively easy, especially without having to order parts on my own.

5. Assembly - I did not attempt my own assembly, so the pre-assembled JLCPCB boards were used for testing.
6. Bring Up/Troubleshoot/Test - Verification of connectivity and part functionality was done by hand, using the separator switches that were placed throughout the design.
7. Documentation - Documentation is being developed as I type this document!

## Takeaways

The most important thing I will be taking away from this project is the importance of noise reduction, as this lab aimed to show. The amount of noise on the quiet high of the poor design - dropping more than half a volt on the rising edge - was more than I expected, and I will definitely be aware of the better design practices in the future. I also recognize the importance of using switches and other separators between various stages of a PCB. I did not include switches in my next board design, and I now am more uncertain about the success of my Golden Arduino because I have no way to ensure that power is conditioned properly without connecting the rest of the items on the board, namely the microcontroller.