Chapter 9 Wk 5 Mon: testing the switching noise on our version of your brd 2

This is the beginning of your brd 2 design: demonstrating good and bad layout for switching noise.

This board will demonstrate the two important design principles to reduce switching noise:

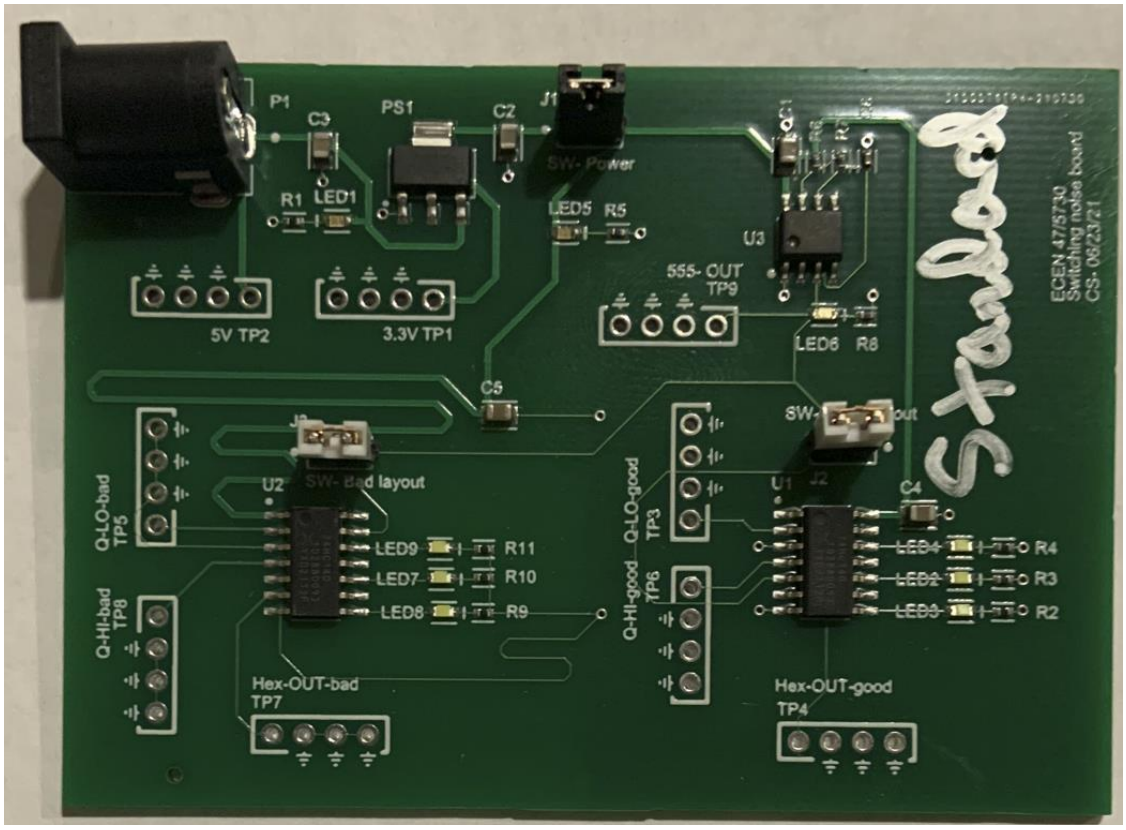
1. *Use a continuous return path under the signal traces*
2. *Use low inductance decoupling capacitors in close proximity to the IC power pins.*

In this board, you will use a 555 timer as a clock and two different hex inverter circuits, one circuit designed following best design principles and, in another region of the board, the same circuit but with really bad design practices.

Three of the output signals from the hex will drive red LEDs with series resistors to limit the current. These will generate the dI/dt for the signal cross talk and the power rail noise.

For this lab, you will use a version of brd 2 that we designed. Your board does not have to be exactly the same as this one. In fact, you should be able to identify at least three important changes you would want to implement in your board compared to this one.

Here is the board you will use for the switch noise measurements for this lab:



9.1 The schedule

In wk 5 (this week) you will get a heads up on the brd 2 design.

In wk 6, you will complete the schematic and layout of board 2. On Thurs Sept 30, we will order all the brd 2 fabs.

In wk 9, your brd 2 boards will come in and you will do the analysis of them.

9.2 Purpose of this lab

In this lab, you will get to measure some of the switching properties of a version of your brd 2 that we built for you.

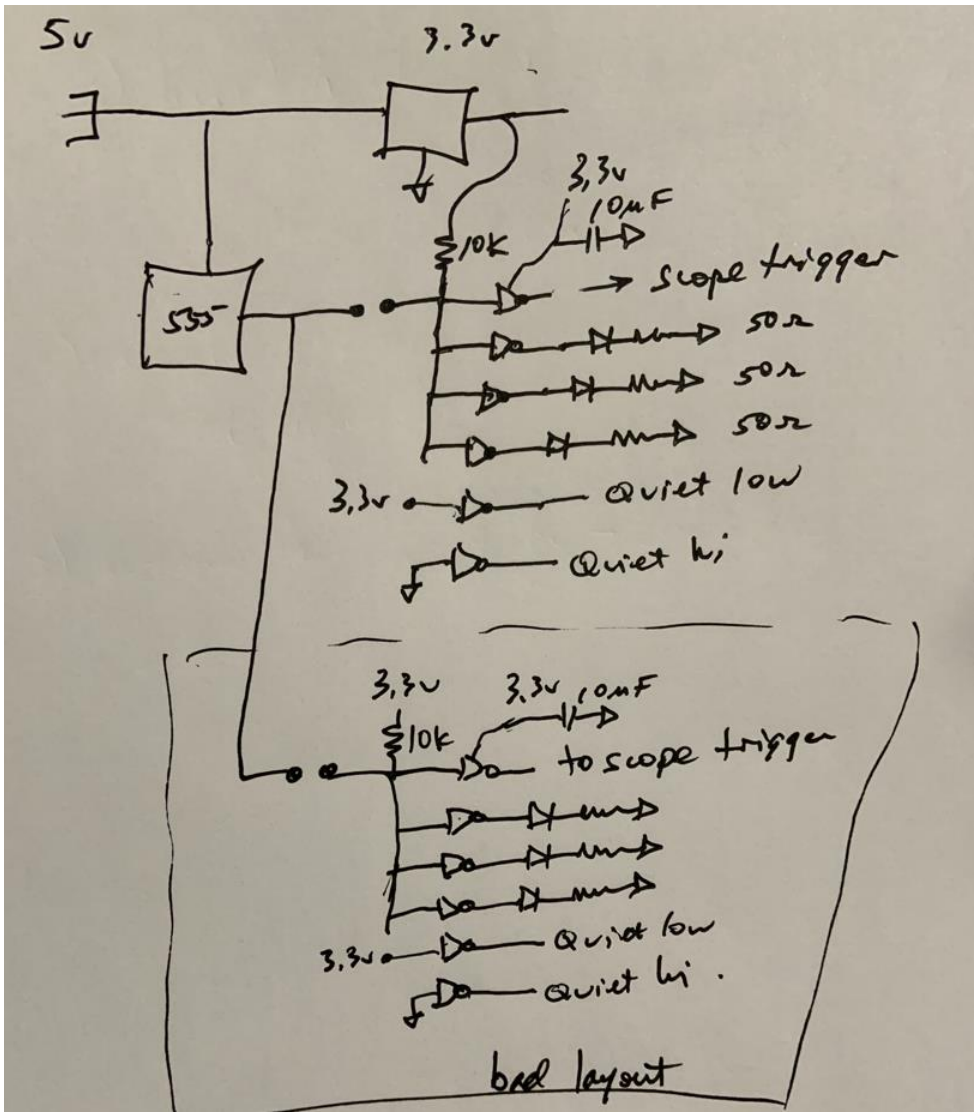
This board will give you an idea of how the board 2 design will be implemented. Review its layout carefully. Note the test points, switches and indictors.

9.3 Circuit Design for brd 2

The circuit design for brd 2 is very similar to board 1, the practice board. 5 V will come in from the power jack and power a 555 timer. We add a few more circuit elements.

The timer signal will connect to two different 7414 hex inverter chips. In each chip, there are 6 inverters. An inverter flips the input level to the output level. A LOW input creates a HIGH output. These 6 inverters in each chip are independent.

The starting place for any design is a rough sketch with as much detail as necessary to convey the important design features. Here is my rough sketch, in the figure below.



In addition to the 555 timer, you will use two new parts in your board 2: a low voltage dropout (LDO) 3.3 V regulator and a 7414 hex inverter.

These two new parts can be found in the newly released integrated libraries JLC_2021_08 release. There is just one LDO option, the AMS1117. It converts the 5 V in to 3.3 V out. You will need a capacitor on its output, not for decoupling, but to filter out the high frequency noise and prevent the LDO from going into oscillation.

There are three different 7414 options in the library. The parts we will use for the brd 2 design are the 74HC14 chips, if they are available. You can open up the specs for these parts. Be sure to use the latest 2021_08 release as this library has the latest footprints for the hex inverters.

You will add a decoupling capacitor to the 555 IC and each of the 7414 ICs. In the case of the good layout circuit, of course, the capacitor should be placed as close as practical to the IC it is decoupling. In the case of the bad layout section, you can place the decoupling capacitor anywhere you like.

In addition to these components, you will also add various test points, indictor LEDs and switches.

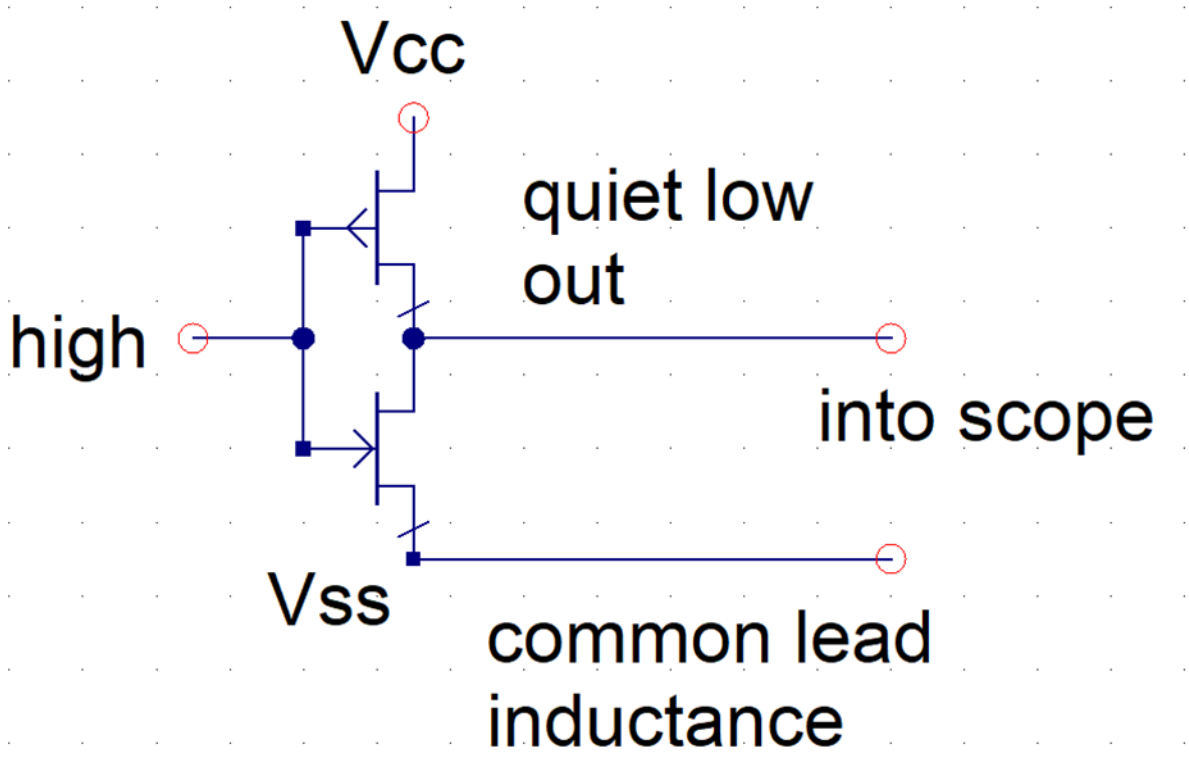
The hex inverter is a collection of 6 independent inverters that share the same power rails in the IC package.

In each circuit, four of the hex inverters act like normal inverters. The output of one inverter is used to trigger the scope.

The output of three of the inverters will drive LEDs with current limiting resistors, so that we have some dI/dt that switches.

Two of the inverters are special.

When the input to one is tied to 3.3 V. This means its output is always a low. The actual transistor level circuit for one inverter is shown below:



When the input is a high, the p-channel MOSFET connecting the output pin to the VCC rail on the die is open and the n-channel MOSFET on the low side is shorted. This connects the output pin to the Vss rail on the die.

When we measure the voltage on the output pin on the board, with the 10x probe, we are measuring the voltage of the output pin, relative to the local ground on the board. If there is any ground bounce noise from the local ground where the 10x probe is to the Vss rail on the die, it will appear as a voltage on the probe. This is how we measure ground bounce noise or cross talk between the quiet output signal-return loop that is not switching and the other signal-return loops that switch.

Likewise, a quiet HIGH output connects the output pin to the internal VCC rail on the die. This allows us to measure the switching noise on the power rail when the other I/Os switch.

We call these two pins quiet HIGH and quiet LOW because nominally, these pins are not switching and they should have no changing voltage on them. Any voltage we measure must be noise.

In the circuit you will build, and that we have already built and provided you, there are three signals to measure for each circuit:

- *Trigger output for the scope*
- *A quiet LOW*
- *A quiet HIGH*

Use the scope trigger to measure the switching of one of the I/O. Using this to trigger the scope, measure the switching noise on the quiet LOW and quiet HIGH pins. This is the noise synchronous with the I/Os switching.

There are other test points available on this board.

Here is a special note: the input to an inverter is very high impedance. If there is no connection to the inverter, stary ESD fields present in your hands will trigger the inverter. It is always important when you are not connecting to an inverter, to always tie it high thru a 10k resistor. This way the output is always a low.

In the circuit for brd 2, a switch connects the 555 output to the various inverters. When the switch is closed, the 555 will drive the inverters. When the switch is open, and the 555 is not connected to the inverters, they should be tied to 3.3 V through a 10k resistor. This keeps the inverters form switching unless you want them to.

On our board, we did not add the 10k pull up resistor. This means when the inputs to the inverters float, we can change their state by waving our hand over the inputs- like magic.

9.4 What you will measure on our board

Identify the good layout part of the board. Turn on the hex inverter on the good side of the board and turn off the hex inverter on the bad side.

Measure the signal on the output pin of the hex with the 10x probe. What is the rise and fall time? Use the rising edge as the reference.

Use this output to set the trigger for the scope. Measure the switching noise on as many test points as you can, such as:

- *The 5 V rail*
- *The 3.3 V rail*
- *The quiet LOW*
- *The quiet HIGH*

Then, turn off the good hex circuit and turn on the bad hex circuit. Repeat these measurements. How does the noise on each test point compare in the bad layout region compared to the good layout region?

What can you conclude about how the different layout features in the good layout region and the bad layout region affects the switching noise?

9.5 In your report

Remember, this report will look good in your portfolio. This is a classic example of how layout affects switching noise. If you write this up well, you will impress any hiring manager with how much you understand about switching noise.

Show a scope trace comparison of the I/O signal that is switching and the synchronous noise on the quiet high and quiet low of the good layout and bad layout. Try to use the same scales so you can do a direct comparison of the magnitude of the noise.

Comment on what features in the layout account for this difference.

Be sure to have your TA check off your measurements and your explanation. Be prepared to show an example of your measurements and the features on this board that contributes to more, or less switching noise.

Remember. The two circuits are identical, yet, they have a very large difference in the amount of noise, just because of their layout.

9.6 Grading rubric

2 points if you show the difference in switching noise between the good layout and bad layout and include an explanation of the layout features that contribute to the noise differences.

1 point if you only look at one section or do not have a clue what you are doing

0 points if you do not submit a report or do not get checked off by your TA.