Chapter 7 Wk 3 Wed: SBB PDN and slammer circuit

In this lab, you will build a simple slammer circuit which will draw a fast transient current from the power rail. This is exactly what happens when an IC suddenly switches current as when it drives I/O signals, or the core logic eats a lot of current to perform some computational operation.

When there is a sudden current draw on the power rail, the current flows through the inductance of the power rail. The dI/dt through this inductance causes a voltage drop. This is a serious type of noise which can be dramatically reduced with a decoupling capacitor.

You will measure the signature and value of this voltage drop and see how much you can reduce it using the local charge storage of a decoupling capacitor.

You will explore the six most important design principles to reduce noise in the power delivery path:

1. *Reduce the loop inductance between the IC that switches (the aggressor) and the nearest decoupling capacitor.*
2. *Keep the decoupling capacitor as physically close as possible to the IC it is decoupling.*
3. *Use at least 10 uF of decoupling capacitance, and then as large a capacitance as practical.*
4. *Where you measure the noise on the power path influences how much noise you measure.*
5. *Short rise time signals have a larger dI/dt and show more power rail noise than long rise time signals.*
6. *When there is a step change in the current on the power rail there is more noise generated than just from the dI/dt. There is also an IR drop from the Thevenin resistance of the VRM and power rail.*

7.1 Purpose of the lab

1. *To build a circuit demonstrating the origin of switching noise in the power path and the role of loop inductance.*
2. *To measure the switching noise on the power rail when there is a large current transient.*
3. *To explore the role of loop inductance between the IC and the decoupling capacitors.*
4. *To see the difference in switching noise for different dI/dt values of current transient.*
5. *To estimate how much capacitance is needed to provide adequate local charge storage.*

7.2 Prep before you start this lab

Read the section in the textbook about power rail switching noise: Chapter 13.

7.3 The big picture

You will build your circuits using a solderless breadboard, using best design practices as described in the textbook.

The slammer circuit is a transistor that turns on and draws a fixed current from the power rail. It will be triggered by either a digital signal from and Arduino digital I/O which has a 5 nsec rise time or by an opAmp output with a rise time of about 1 usec.

The different rise times for the current from the power rail to turn on mean very different dI/dt. You will measure the switching noise on the collector pin for these different rise times with and without decoupling capacitors.

7.4 Set up the two base driver signals

The Arduino will provide the input signal to turn on the transistor's base, the slammer circuit.

Pin 13 of the Arduino will be used to generate the signal that triggers the slammer circuit. Modify the blink code to use an on-time of 1 msec and an off-time of 20 msec.

The code is simply:

```
void setup() {
  pinMode(13, OUTPUT);
}
void loop() {
  digitalWrite(13, HIGH);
  delay(1);
  digitalWrite(13, LOW);
  delay(20);
}
```

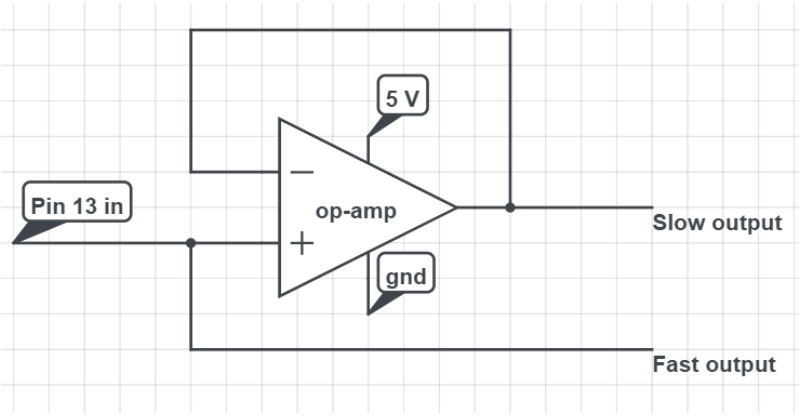
You can literally copy this sketch from this soft copy and paste it in a blank sketch, upload it and it will run.

Pin 13 (and the ground connection) will be the signal source.

Be sure to use a duty cycle less than 10% or the transistor may get too hot.

On the solderless breadboard, add the op-amp follower at the bottom end of the solderless breadboard. Set up an op-amp in your board as a follower. Connect the output of pin 13 to the input of the follower circuit.

The circuit you will build is very simple, shown in the figure below



Simple buffer follower to generate two signals from pin 13, one with a fast edge and one with a slow edge.

1. *Use the external 9 V AC to DC supply to power the Arduino.*
2. *Connect the USB cable to the Arduino and make sure you can upload a sketch.*
3. *Write a modified Blink sketch to turn Pin 13 on for 1 msec and off for 20 msec*
4. *Measure this signal with the scope when it is running and verify the duty cycle is less than 10%.*
5. *Be sure to use color coding for the solderless breadboard and the power and ground right hand side columns.*
6. *Did you verify that the top half of the columns are connected to the bottom half of columns on your solderless breadboard?*
7. *You will be using two power rails on your solderless breadboard. Use the left columns for 5 V and the right column for 9 V, the power rail on which you will measure the switching noise.*
8. *Power the opAmp with 5 V from the Arduino using a black and red wire from the Arduino to the solderless breadboard.*
9. *Did you use the correct color code?*

In all the measurements in this lab we will use the 10x probe.

Remember, it is easy to make a measurement. It is hard to make a measurement without introducing artifacts.

When the pin 13 signal (and its return ground pin connection), is connected to the opAmp buffer, there will be two signals available to drive the rest of the circuit: the raw input from the Arduino and the buffered output from the opAmp follower.

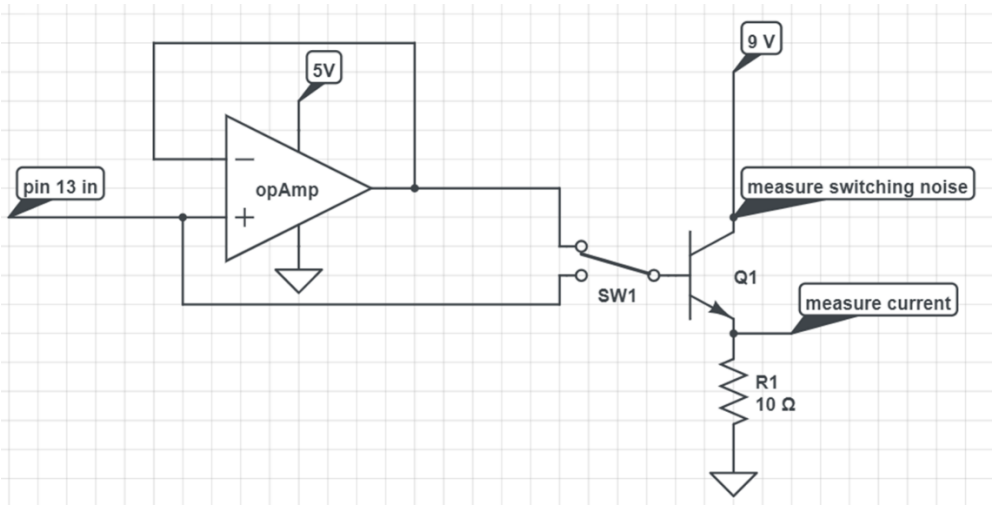
What is the rise and fall times of these two signals?

Be sure to measure both the rise and fall time for both of these signals using a 10x probe. It is very important to verify that the on-time is about 1 msec and the off-time is at least 20 msec or longer. If the duty cycle is larger than 10%, the circuit may heat up too much.

Remember if you have large loops at the tip of the 10x probe, you will have the potential of cross talk noise ***in the probes***. What consistency test can you think of to verify how much of your scope measurement is just induced noise in the tip's loop?

7.5 Build the slammer circuit with no decoupling capacitors and the slow edge.

We will build the slammer circuit in stages. First, we start with just the transistor and NO decoupling capacitors. The slammer circuit is shown in the figure below.



Simple slammer circuit with the transistor connected to the power rail.

The transistor circuit is often called a slammer circuit in that it will slam or sink a high current from the power rail.

This is also a constant current-source circuit. The transistor will turn on with whatever current flow through it so the voltage across the sense resistor and the base to emitter voltage drop adds up to the voltage on the base.

The only way we get a voltage across the sense resistor is with a current through it. You should derive the current through the resistor as:

$$I = \frac{(5V - 0.6V)}{10\Omega} = 440mA$$

When the signal to the base turns on, there will be about 440 mA current draw from the power rail. This current will turn on with the rise time of source filtered by the response of the transistor.

In the first series of measurement, use the slow edge, from the buffered signal.

Now it should be obvious why it is so important to use a signal with a duty cycle less than 10%. At steady state, the power consumption in the transistor is about 5 V x 0.4 A = 2 watts. This will heat the transistor.

The 10 ohm resistor acts as both a sense resistor to measure the current and a current limiting resistor to set the current. If the current through the resistor is 440 mA, instantaneous power dissipation through the resistor would be:

$$P = I^2R = 0.44^2 \times 10 = 1.9 \text{watts}$$

The resistor is rated at only ¼ watt. This power consumption would be way more than the resistor can handle without heating to a high temperature. This power consumption is almost 10x the rated power dissipation of the resistor. If we run this current at DC, the resistor will get so hot that it will probably smoke, or worse.

This means, to send this much current through the resistor, we can't keep it on very long. To keep the average power consumption down by 10x, we use a pulse width modulated signal, with a duty cycle of less than 10%.

If we want the on-time to be 1 msec, the off-time should be at least 10 msec, and preferably 20 msec. This would be a frequency of 1/21 msec or about 50 Hz.

7.6 Measure switching noise with a slow rise time

Construct the circuit in this order:

1. *Build the slammer circuit in the solderless breadboard. Use the best practices for the solderless breadboard as described in the text. Use discrete wires, not the long floppy jumper wires.*
2. *Connect the transistor. Check the* datasheet for the transistor.
3. *Add the 10 ohm series resistor from the emitter to ground.*
4. *This is the configuration of a board with no decoupling capacitors.*
5. *Initially, connect the slow rise time signal from the buffered output to the base of the transistor. It should be a 5 V signal, 5% duty cycle.*

Practice Rule #9 for all measurements.

6. *Measure the voltage on the base. What did you expect to see?*
7. *Measure the voltage on the sense resistor. What is the current through the collector?*
8. *What is the rise time of the current and the dI/dt?*
9. *Use the current through the emitter as the trigger for the scope on chan1*
10. *On chan2, measure the switching noise on the power rail of the die- this is the collector pin.*
11. *What is the switching noise on the collector? Why does it have the shape it does? At short rise time and long rise time.*

12. *How much of the voltage on your probe is from inductive coupling in the loops of the probe? How can you minimize the loop area?*
13. *From the steady state voltage droop on the power rail for a 400 mA current load, after the initial inductive spike, what do you estimate the Thevenin source resistance of the VRM to be? Remember, every voltage source can be modeled as a Thevenin source.*
14. *Does the noise change as you move down the power rail on the solderless breadboard?*
15. *Be sure to measure the switching noise on both the rising and falling edge of the current.*

If the actual circuit is only the circuit in the figure above, there should be no voltage noise on the 9 V rail. Afterall, the 9 V source is an ideal voltage source in the schematic.

But, this is not the complete circuit. It is missing two important elements, the Thevenin model of the VRM and the loop inductance of the power conductors from the VRM on the Arduino to the collector of the transistor.

Draw the equivalent circuit model that includes these elements. Since the Thevenin resistance of the VRM and the interconnect inductance of the conductors from the VRM to the collector of the transistor are not actual discrete components you can see on the board, you must learn to see them with your engineer's mind's eye.

Where would you add them into the equivalent circuit model?

Given this model, why do you see the signature of the voltage noise you see?

This is the switching noise with a slow edge. The biggest impact is from the IR drop from the source resistance of the VRM. It is a small amount of noise.

Given the voltage you measure, what do you estimate the Thevenin voltage and resistance of the Arduino VRM?

If you wanted to reduce this IR drop noise, what could you do to reduce the DC IR drop?

Is it any wonder that when your signal rise time is long, switching noise is not important?

7.7 Measure switching noise with a fast rise time signal

Now we will use the Arduino pin signal as the input to the base.

1. *Repeat these measurements using the fast rise time signal into the base, instead of the slow rise time signal.*
2. *What is the rise time of the current turn on and turn off?*
3. *Measure the switching noise on the collector pin for the rising and falling edges.*
4. *Look at the signal on a very fast time scale and a slow time scale.*
5. *From the equivalent circuit including the interconnect loop inductance in the power rail, can you explain the features in the switching noise from this circuit model?*

6. *Why is the switching noise so different between the slow edge and the fast edge?*
7. *What do you think the small ripple voltage noise on the power rail is from? Hint its frequency is about 16 MHz, the same as the clock of the Arduino. And it is only present when the Arduino pin drives the current load on the power rail.*

Remember, the voltage drop across an inductor is:

$$\Delta V = L\frac{dI}{dt}$$

If we see a voltage drop of 8 V across the inductor, and the dI = 400 mA and the dt = 50 nsec, then the loop inductance is 8 V/0.4 A x 50 nsec = 1000 nH.

Why did we not see any switching noise with the opAmp signal having a rise time of 2 usec?

The expected switching noise was 1000 nH x 0.4 A /2 usec = 0.2 V, too small a value to see compared to the pattern of the changing current.

7.8 Add the decoupling capacitor

In this experiment we will explore the impact on the switching noise we measure at the collector from the location of the decoupling capacitor and its value.

The voltage noise on the collector is due to the inductance and the dI/dt in the power rail. First do not add the decoupling capacitor.

As you move the measurement point closer to the VRM and measure the switching noise, you will see less switching noise because there is less loop inductance to the VRM.

1. *Measure the switching noise on the collector pin with the fast edge. This is the switching noise that would appear on the die itself.*
2. *Repeat these measurements using the slow rise time signal. Is there any difference?*

Be sure to apply Rule #9. What do you expect to see happen to the switching noise signature?

3. *Measure the switching noise with the fast edge first.*
4. *Use a large value capacitor as the decoupling capacitor. Before you insert it in the power rail between the 9 V and the ground, check its polarity.*
5. *If you reverse the polarity and insert the + side to the ground and the – side to the 9 V, it will literally explode. DO NOT DO THIS. (see the demo of the exploding capacitor)*
6. *Place the large capacitor far away from the collector pin and measure the switching noise on the collector pin.*
7. *What do you think will happen to the switching noise if we move the capacitor closer to the transistor's collector pin?*
8. *Why does the switching noise decrease as you move the capacitor closer to the collector pin?*

9. *Look at the switching noise on different time scales and with the current switching off and switching on.*
10. *What is the impact on the switching noise from using a short rise time with pin 13 and long rise time, using the output of the opAmp?*
11. *When the decoupling capacitor is close to the collector pin, what is the switching noise on the rest of the power rail?*
12. *From this behavior, what is the decoupling capacitor actually decoupling?*
13. *Does the value of the decoupling capacitor, either then 1000 uF or the 1 uF capacitor, effect the amount of switching noise?*

7.9 Charge depletion time in the capacitor

When the 440 mA of current flows through the collector on the power rail, there are three features in the voltage response:

1. *The initial voltage droop due to the loop inductance in the power delivery path*
2. *The slow drop in voltage due to the charge depletion in the capacitor*
3. *The steady state DC voltage drop in the VRM due to its Thevenin source resistance*

From the steady state voltage drop on the 5 V rail, calculate the Thevenin resistance of the 9 V VRM you are using to power the rail.

If the capacitor provides some charge storage, how slowly will the voltage drop with the 440 mA of current draw? How does this slope compare with the slope you measure for the voltage drop? You should be able to derive that:

$$\frac{dV}{dt} = \frac{1}{C} \times I$$

How does your estimate of the slope of the voltage droop match what you actually measure?

If you want to reduce the droop voltage, do you want a big or small capacitor value? How will the sharp dip from the L dI/dt noise be affected by using the 1 uF or 1000 uF capcaitor? How much charge depletion is there in the capacitor during the dt time?

7.10 Check out by your TA

Before you leave the lab, call your TA over for a check out of your experiment. Be prepared to answer any of the above or following questions:

1. *What is the equivalent circuit model for your circuit, including the VRM and the power rail inductance?*

2. *What is the transient current through the transistor? What is the rise and fall time?*
3. *Where does the power rail switching noise come for?*
4. *Why is it called switching noise?*
5. *How are you triggering the scope?*
6. *How much inductive pick up noise is there between your probes?*
7. *When decoupling the power rail, what will be the impact of using a larger value decoupling capacitor?*
8. *What is the most important quality of a decoupling capcaitor to decouple the power rail noise?*
9. *What did you observe for the switching noise with the slow and fast edges and the rising and falling current edges and no decoupling capacitors? How do you interpret the results?*
10. *Why is switching noise a bigger concern for shorter rise time signals?*
11. *What did you observe after you added the decoupling capacitor? To reduce the switching noise, where do you want to place the decoupling capacitor and why?*
12. *What do you conclude about the size of the decoupling capacitor to use to reduce switching noise and its location? What is the most important quality of the decoupling capacitor?*
13. *What feature of the interconnect are you reducing by moving the decoupling capacitor as close to the collector pin as practical?*
14. *Based on these observations, what do you conclude about the best design practices for designing the power delivery path and the use of decoupling capacitors?*

7.11 In your report, you should include

1. *Draw the equivalent circuit of the slammer circuit including the Thevenin model of the 9 V VRM and the loop inductance of the path from the VRM to the transistor collector.*
2. *Show a photo of your circuit.*
3. *With a scope screen capture, illustrate the impact on the switching noise with and without the decoupling capcaitor*
4. *With a scope screen capture, illustrate the impact on the switching noise of the 1 uF and 1000 uF capcaitor.*
5. *Based on your measurements:*
    a. *What is the Thevenin voltage and resistance of the VRM?*
    b. *What is the loop inductance of the power path from the collector to the VRM?*
    c. *Show your measured values and how you made these estimates.*
6. *Be sure to add your analysis and interpretation of each scope trace you include. Just including a scope screen with no explanation is worthless.*
7. *You may need 2 pages to fit the scope plots, your analysis and your calculations.*

8. *Remember, a good explanation and associated scope traces to illustrate your explanation will look great on your portfolio.* ***Hiring managers will eat this up****.*

7.12 Grading rubric:

2 points if your scope traces clearly show the features you want to illustrate the cause of switching noise ad your explanations are clear.

1 point if you made an attempt but do not demonstrate understanding of switching noise.

0 if you did not complete the lab, or if you were not checked off by your TA, or if you demonstrated you do not have a clue.