CHR ROM

U101
2364

CHR_A0, CHR_A1, CHR_A2, CHR_A3, CHR_A4, CHR_A5, CHR_A6, CHR_A7, CHR_A8, CHR_A9, CHR_A10, CHR_A11, CHR_A12
SOCKET
CHR_D0, CHR_D1, CHR_D2, CHR_D3, CHR_D4, CHR_D5, CHR_D6, CHR_D7

CHR_CE — CE

U1
2364

CHR_A0, CHR_A1, CHR_A2, CHR_A3, CHR_A4, CHR_A5, CHR_A6, CHR_A7, CHR_A8, CHR_A9, CHR_A10, CHR_A11, CHR_A12
8K x 8 CHR ROM
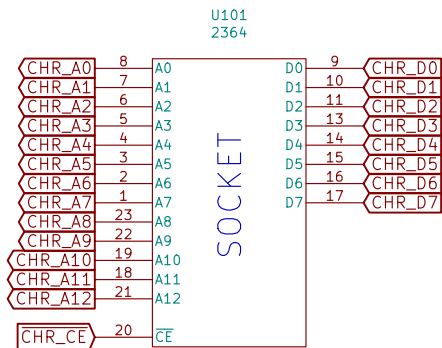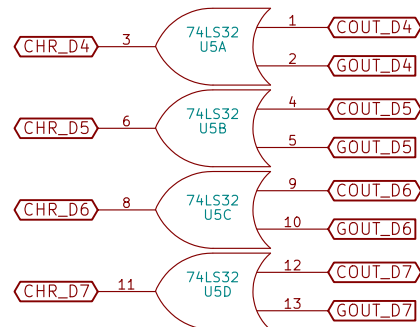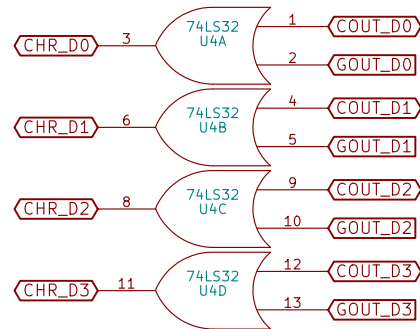COUT_D0, COUT_D1, COUT_D2, COUT_D3, COUT_D4, COUT_D5, COUT_D6, COUT_D7
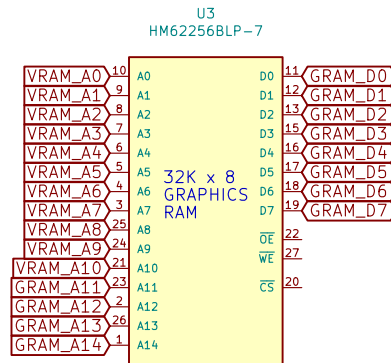
CHR_CE — CE

The CHARACTER ROM outputs CHARACTER DATA. It's output is combined with the GRAPHICS DATA. The CHARACTER ROM also supplies ADDRESS lines to the GRAPHICS RAM.
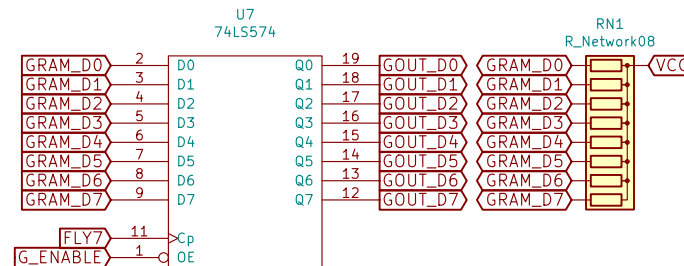
CHR/GRAPHICS MERGE

CHR_D0 — 74LS32 U4A — COUT_D0 / GOUT_D0
CHR_D1 — 74LS32 U4B — COUT_D1 / GOUT_D1
CHR_D2 — 74LS32 U4C — COUT_D2 / GOUT_D2
CHR_D3 — 74LS32 U4D — COUT_D3 / GOUT_D3

CHR_D4 — 74LS32 U5A — COUT_D4 / GOUT_D4
CHR_D5 — 74LS32 U5B — COUT_D5 / GOUT_D5
CHR_D6 — 74LS32 U5C — COUT_D6 / GOUT_D6
CHR_D7 — 74LS32 U5D — COUT_D7 / GOUT_D7

GRAPHICS RAM

U3
HM62256BLP-7

VRAM_A0, VRAM_A1, VRAM_A2, VRAM_A3, VRAM_A4, VRAM_A5, VRAM_A6, VRAM_A7, VRAM_A8, VRAM_A9, VRAM_A10, GRAM_A11, GRAM_A12, GRAM_A13, GRAM_A14
32K x 8 GRAPHICS RAM
GRAM_D0, GRAM_D1, GRAM_D2, GRAM_D3, GRAM_D4, GRAM_D5, GRAM_D6, GRAM_D7
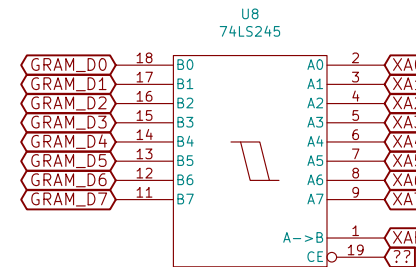OE, WE, CS

The GRAPHICS RAM takes it's ADDRESS as a combination of the TEXT RAM and CHARACTER ROM address lines. The upper 4 address lines come from the USER PORT when the CPU is accessing it and from the CHARACTER ROM when the VIDEO system is accessing it.
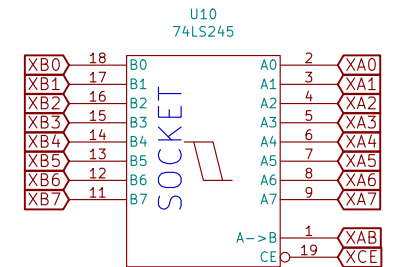
U7
74LS574

GRAM_D0, GRAM_D1, GRAM_D2, GRAM_D3, GRAM_D4, GRAM_D5, GRAM_D6, GRAM_D7 — D0..D7
Q0..Q7 — GOUT_D0, GOUT_D1, GOUT_D2, GOUT_D3, GOUT_D4, GOUT_D5, GOUT_D6, GOUT_D7 — GRAM_D0, GRAM_D1, GRAM_D2, GRAM_D3, GRAM_D4, GRAM_D5, GRAM_D6, GRAM_D7

RN1
R_Network08 — VCC

FLY7 — Cp
G_ENABLE — OE

This ENABLES/DISABLES the output of the GRAPHICS DATA

TRANCEIVERS

U8
74LS245

GRAM_D0, GRAM_D1, GRAM_D2, GRAM_D3, GRAM_D4, GRAM_D5, GRAM_D6, GRAM_D7 — B0..B7
A0..A7 — XA0, XA1, XA2, XA3, XA4, XA5, XA6, XA7
A->B, CE — XAB / ??

This X'CVR controls DATA to/from the Graphics RAM

U10
74LS245

XB0, XB1, XB2, XB3, XB4, XB5, XB6, XB7 — B0..B7
SOCKET
A0..A7 — XA0, XA1, XA2, XA3, XA4, XA5, XA6, XA7
A->B, CE — XAB / XCE

The Tranceivers determine the flow of data to/from the DATA BUS.

U9
74LS245

XB0, XB1, XB2, XB3, XB4, XB5, XB6, XB7 — B0..B7
A0..A7 — XA0, XA1, XA2, XA3, XA4, XA5, XA6, XA7
A->B, CE — XAB / XCE
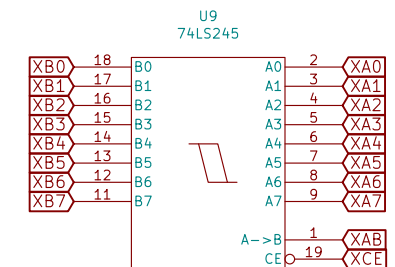
This is the original X'CVR transplanted from the motherboard to the HiRes board.

TEXT RAM

U102
6116

VRAM_A0, VRAM_A1, VRAM_A2, VRAM_A3, VRAM_A4, VRAM_A5, VRAM_A6, VRAM_A7, VRAM_A8, VRAM_A9, VRAM_A10
SOCKET
Q0..Q7 — VRAM_D0, VRAM_D1, VRAM_D2, VRAM_D3, VRAM_D4, VRAM_D5, VRAM_D6, VRAM_D7

VRAM_OE — OE
VRAM_WE — WE
VRAM_CS — CS

U2
6116

VRAM_A0, VRAM_A1, VRAM_A2, VRAM_A3, VRAM_A4, VRAM_A5, VRAM_A6, VRAM_A7, VRAM_A8, VRAM_A9, VRAM_A10
2K x 8 VIDEO RAM
Q0..Q7 — VRAM_D0, VRAM_D1, VRAM_D2, VRAM_D3, VRAM_D4, VRAM_D5, VRAM_D6, VRAM_D7

VRAM_OE — OE
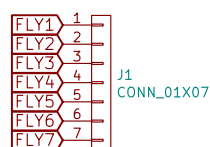VRAM_WE — WE
VRAM_CS — CS

The VIDEO RAM supplies it's ADDRESS lines to the GRAPHICS RAM. The /OE line seems to be controlled to be able to blank the TEXT SCREEN.
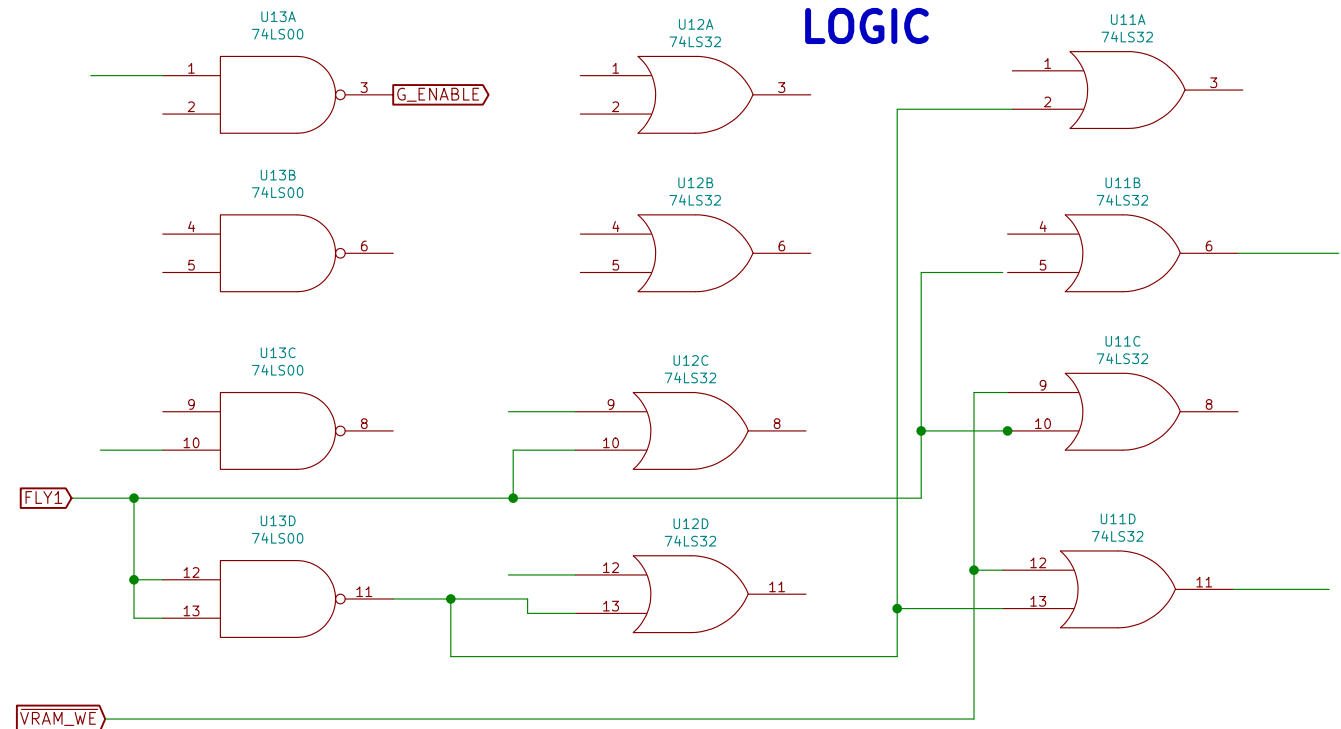
CPU/GRAPHICS SELECTOR

U6
74LS157

CHR_A0 / FLY5 — I0a / I1a — Za — GRAM_A11
CHR_A1 / FLY4 — I0b / I1b — Zb — GRAM_A12
CHR_A3 / FLY2 — I0c / I1c — Zc — GRAM_A14
CHR_A2 / FLY3 — I0d / I1d — Zd — GRAM_A13
FLY6 — S
??? — E
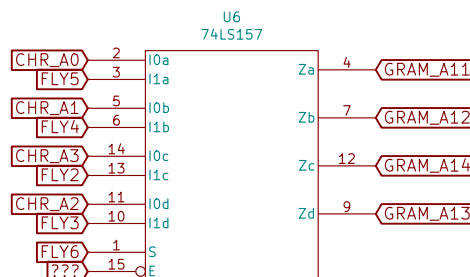
FLYOUTS

FLY1 – LOGIC ???
FLY2 – USER – GRAM14
FLY3 – USER – GRAM13
FLY4 – USER – GRAM12
FLY5 – USER – GRAM11
FLY6 – CPU Phase
FLY7 – CLOCK? (U7p11)

FLY1, FLY2, FLY3, FLY4, FLY5, FLY6, FLY7
J1
CONN_01X07

LOGIC

U13A 74LS00 — G_ENABLE
U13B 74LS00
U13C 74LS00
U13D 74LS00

U12A 74LS32
U12B 74LS32
U12C 74LS32
U12D 74LS32

U11A 74LS32
U11B 74LS32
U11C 74LS32
U11D 74LS32

FLY1
VRAM_WE

B700 HIRES CARD for CBM-II

Steve J. Gray
Sheet: /
File: b700-hires.sch
Title:
Size: A3   Date: Rev:
KiCad E.D.A. kicad (2018-01-29 revision d44494bed)-makepkg   Id: 1/1

** WORK IN PROGRESS!!!!! **