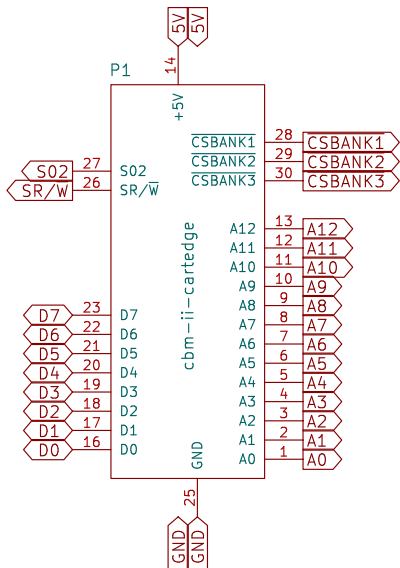
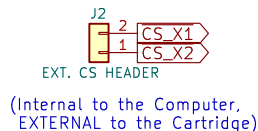


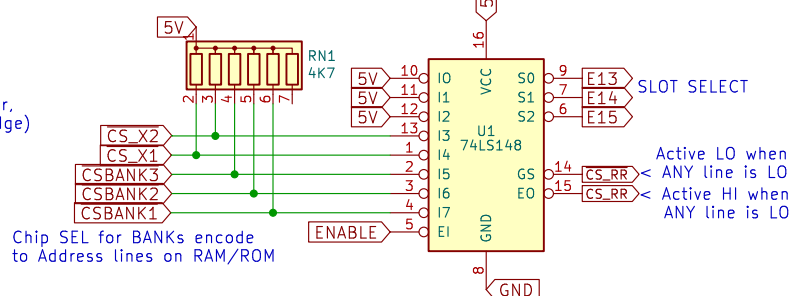
CBM-II CART CONNECTOR



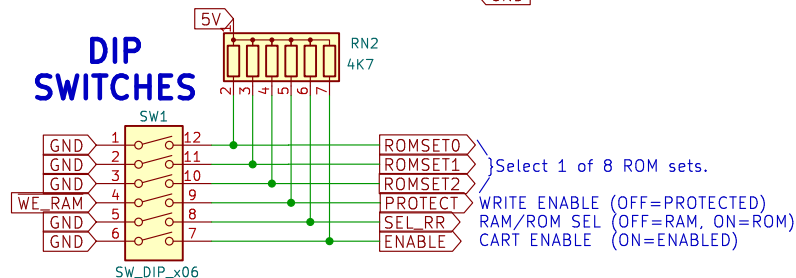
EXTERNAL CS



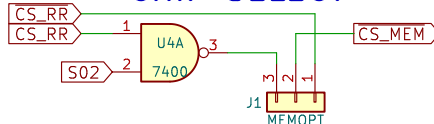
SLOT SELECT



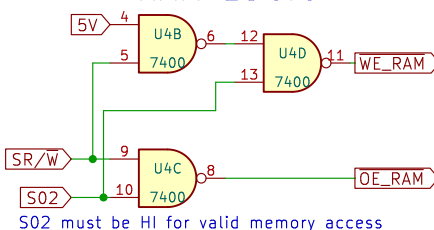
DIP SWITCHES



CHIP SELECT



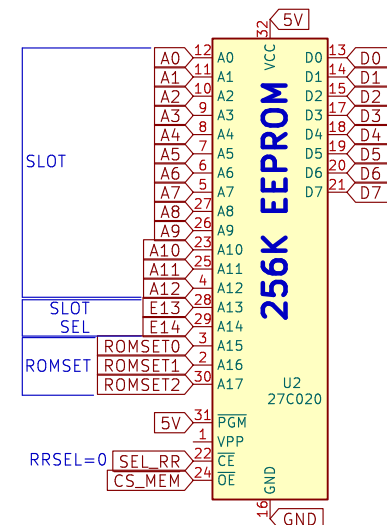
RAM LOGIC



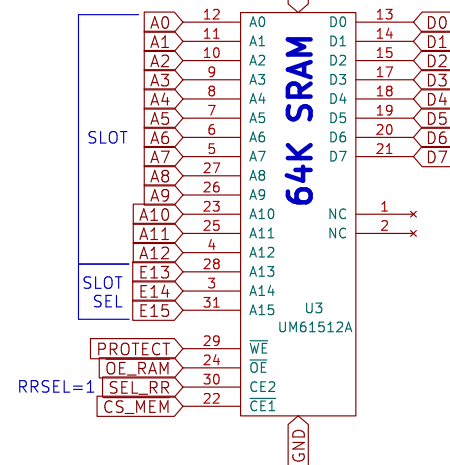
| S02 | SR/W | OE_RAM | WE_RAM |
|-----|------|--------|--------------|
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 <RAM WRITE |
| 1 | 1 | 0 | 1 <RAM READ |

S02 must be HI for valid memory access

ROM



RAM



DESCRIPTION

The CBM-II cartridge is designed for addressing 24K of memory in three 8K "Slots": \$2000-3FFF, \$4000-5FFF, and \$6000-7FFF, which are all located in the CPU's BANK 15. Each slot has a dedicated chip select line.

One 256K PLCC ROM chip provides 8 ROM SETS selectable via DIP switch. Each set consists of 24K ROM to fill the 3 cartridge slots. You can not control each slot separately.

One 64K SRAM provides 32K of RAM for 5 SLOTS. Each slot is reserved 8K in the RAM chip (40K total). There is a switch to write protect the RAM.

One switch controls whether RAM or ROM is selected.

There is a header allowing two external (to the cartridge, ie: In the computer) CHIP SELECTS to be included as well. This would normally be \$1000-1FFF (4K) and \$C000-CFFF (4K) range (Not available on P500).

Updated: 2025-05-20

CBM-II ROM+RAM CART

Steve J. Gray

Sheet: /
File: cbm2rrcart.kicad_sch

Title: CBM-II ROM+RAM CART

Size: A4 Date: 2025-05-20

KiCad E.D.A. 9.0.0

Rev:
Id: 1/1

STATUS: Working