CBM-II CART CONNECTOR

P1 — cbm-ii-cartedge

+5V

| S02 27 | S02 |
| SR/W 26 | SR/W |

			CSBANK1 28	CSBANK1
			CSBANK2 29	CSBANK2
			CSBANK3 30	CSBANK3

A12 13	A12
A11 12	A11
A10 11	A10
A9 10	A9
A8 9	A8
A7 8	A7
A6 7	A6
A5 6	A5
A4 5	A4
A3 4	A3
A2 3	A2
A1 2	A1
A0 1	A0

D7 23	D7
D6 22	D6
D5 21	D5
D4 20	D4
D3 19	D3
D2 18	D2
D1 17	D1
D0 16	D0

GND 25 GND

EXTERNAL CS

J2 — EXT. CS HEADER

| 2 | CS_X1 |
| 1 | CS_X2 |

(Internal to the Computer,
EXTERNAL to the Cartridge)

SLOT SELECT

RN1 4K7

U1 74LS148

5V 10	I0	VCC 16
5V 11	I1	
5V 12	I2	
CS_X2 13	I3	S0 9	E13
CS_X1 1	I4	S1 7	E14
CSBANK3 2	I5	S2 6	E15
CSBANK2 3	I6	GS 14	CS_RR
CSBANK1 4	I7	E0 15	CS_RR
ENABLE 5	EI	GND 8	

SLOT SELECT

Active LO when
< ANY line is LO

< Active HI when
ANY line is LO

Chip SEL for BANKs encode
to Address lines on RAM/ROM

DIP SWITCHES

RN2 4K7

SW1 — SW_DIP_x06

GND 1		12 ROMSET0
GND 2		11 ROMSET1
GND 3		10 ROMSET2
WE_RAM 4		9 PROTECT
GND 5		8 SEL_RR
GND 6		7 ENABLE

}Select 1 of 8 ROM sets.

WRITE ENABLE (OFF=PROTECTED)
RAM/ROM SEL (OFF=RAM, ON=ROM)
CART ENABLE (ON=ENABLED)

CHIP SELECT

U4A 7400

CS_RR 1	
CS_RR	3 CS_MEM
S02 2	

J1 MEMOPT

This is here in case the
output from '148 doesn't
give enough time for E13/E14
to stabilize if Chip Select
happens at the same time.

RAM LOGIC

| 5V 4 | U4B 7400 6 | U4D 7400 | 12 / 11 WE_RAM |
| | 5 | | 13 |

| SR/W 9 | U4C 7400 | 8 OE_RAM |
| S02 10 | | |

S02	SR/W		OE_RAM	WE_RAM
0	0		1	1
0	1		1	1
1	0		1	0 <RAM WRITE
1	1		0	1 <RAM READ

S02 must be HI for valid memory access

U4E 7400 (VCC 14 / GND 7)

C1 0.1uf   C2 0.1uf   C3 0.1uf   C4 0.1uf

PWR_FLAG — 5V — VCC
PWR_FLAG — GND — GND

ROM

U2 27C020 — 256K EEPROM

A0 12	A0	D0 13	D0
A1 11	A1	D1 14	D1
A2 10	A2	D2 15	D2
A3 9	A3	D3 17	D3
A4 8	A4	D4 18	D4
A5 7	A5	D5 19	D5
A6 6	A6	D6 20	D6
A7 5	A7	D7 21	D7
A8 27	A8		
A9 26	A9		
A10 23	A10		
A11 25	A11		
A12 4	A12		
E13	A13		
E14	A14		
ROMSET0 3	A15		
ROMSET1 2	A16		
ROMSET2 30	A17		

VCC 32 5V

SLOT
SLOT SEL
ROMSET

RRSEL=0

31	PGM
1	VPP
22	CE
24	OE

SEL_RR
CS_MEM

GND 16

RAM

U3 UM61512A — 64K SRAM

A0 12	A0	D0 13	D0
A1 11	A1	D1 14	D1
A2 10	A2	D2 15	D2
A3 9	A3	D3 17	D3
A4 8	A4	D4 18	D4
A5 7	A5	D5 19	D5
A6 6	A6	D6 20	D6
A7 5	A7	D7 21	D7
A8 27	A8		
A9 26	A9		
A10 23	A10		
A11 25	A11		
A12 4	A12	NC 1	
E13 28	A13	NC 2	
E14 3	A14		
E15 31	A15		

5V VCC

SLOT
SLOT SEL

RRSEL=1

PROTECT 29	WE
OE_RAM 24	OE
SEL_RR 30	CE2
CS_MEM 22	CE1

GND

DESCRIPTION

The CBM-II cartridge is designed for addressing 24K of memory
in three 8K "Slots": $2000-3FFF, $4000-5FFF, and $6000-7FFF,
which are all located in the CPU's BANK 15. Each slot has a
dedicated chip select line.

One 256K PLCC ROM chip provides 8 ROM SETS selectable via DIP switch.
Each set consists of 24K ROM to fill the 3 cartridge slots. You can
not control each slot separately.

One 64K SRAM provides 40K of RAM for 5 SLOTS. There is a switch to
write protect the RAM.

One switch controls whether RAM or ROM is selected.

There is a header allowing two external (to the cartridge, ie: In the
computer) CHIP SELECTS to be included as well. This would normally be
$1000-1FFF (2K DOS ROM) and $C000-CFFF (4K) range (Not available on
P500).

Updated: 2024-04-16

STATUS: Untested Prototype