Report - Wilkinson Power Divider

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Microstrip

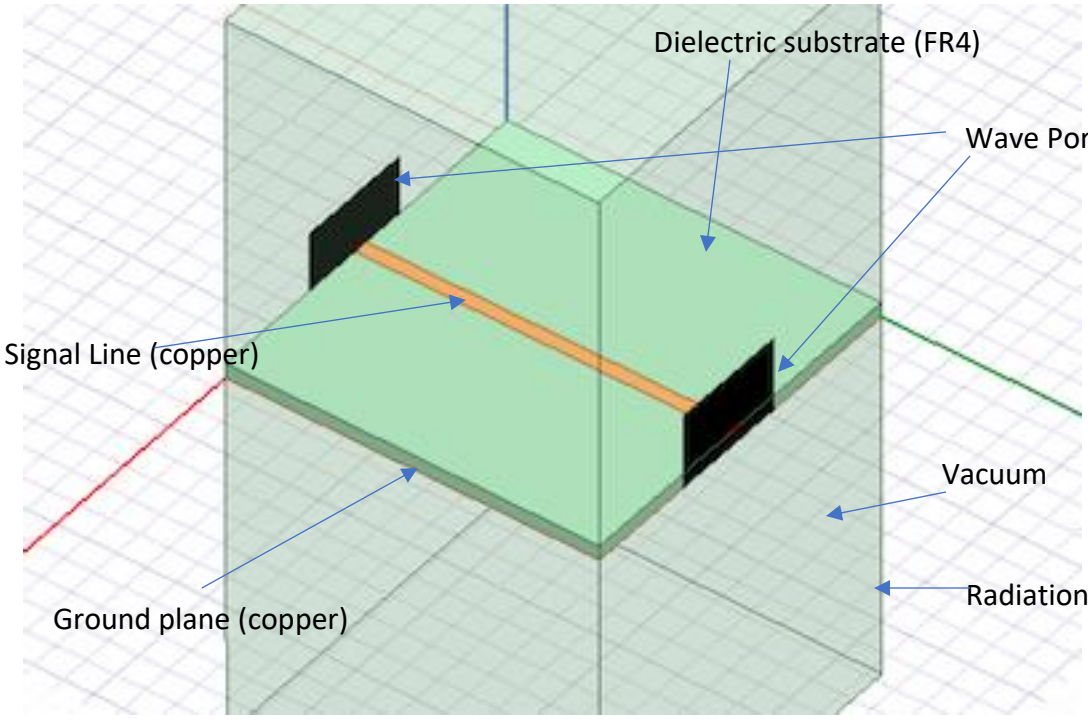
Design

Initially, we designed a microstrip with a ground plane, dielectric substrate, a signal line and 2 wave ports (reference plane) by using our ANYSYS Electronics Desktop application. This app will help us design and simulate high-frequency electronic products.

By assigning excitation to the wave ports, we can renormalize the modes and have the full port impedance as 50 ohms. I made the wave ports be 8*(width of the signal line) wide and 5*(width of signal line) high and made sure to center it down the middle.

We make sure the surrounding box material is assigned as a vacuum with the boundary as type radiation.

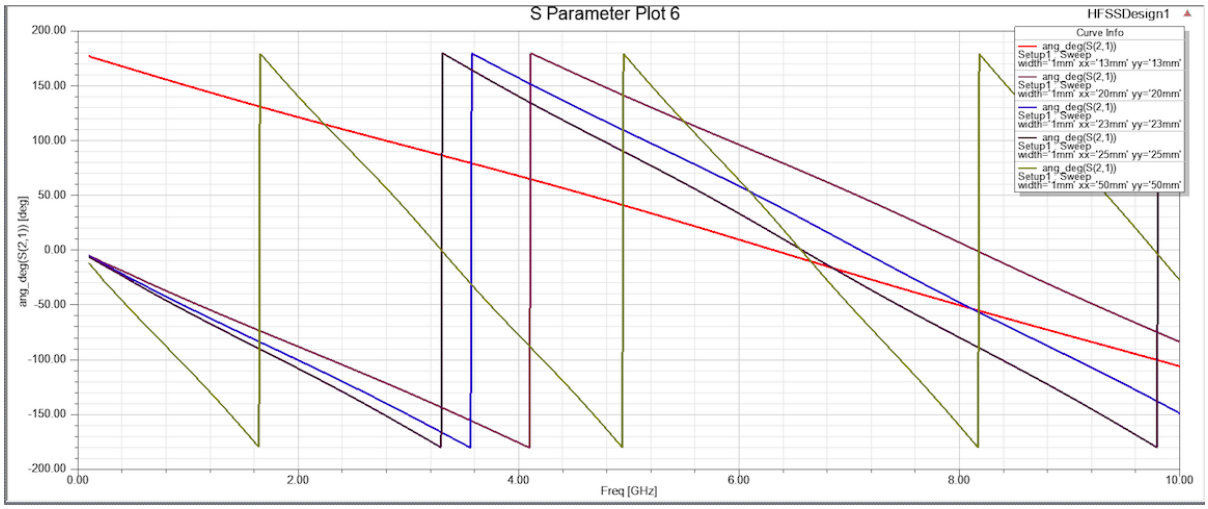
The dielectric substrate is assigned with FR4 material and the signal line is assigned boundary as finite conductivity with the material as copper. The material of the ground plane is also assigned as finite conductivity with the material as copper. The signal line has width w mm and length of yy mm.



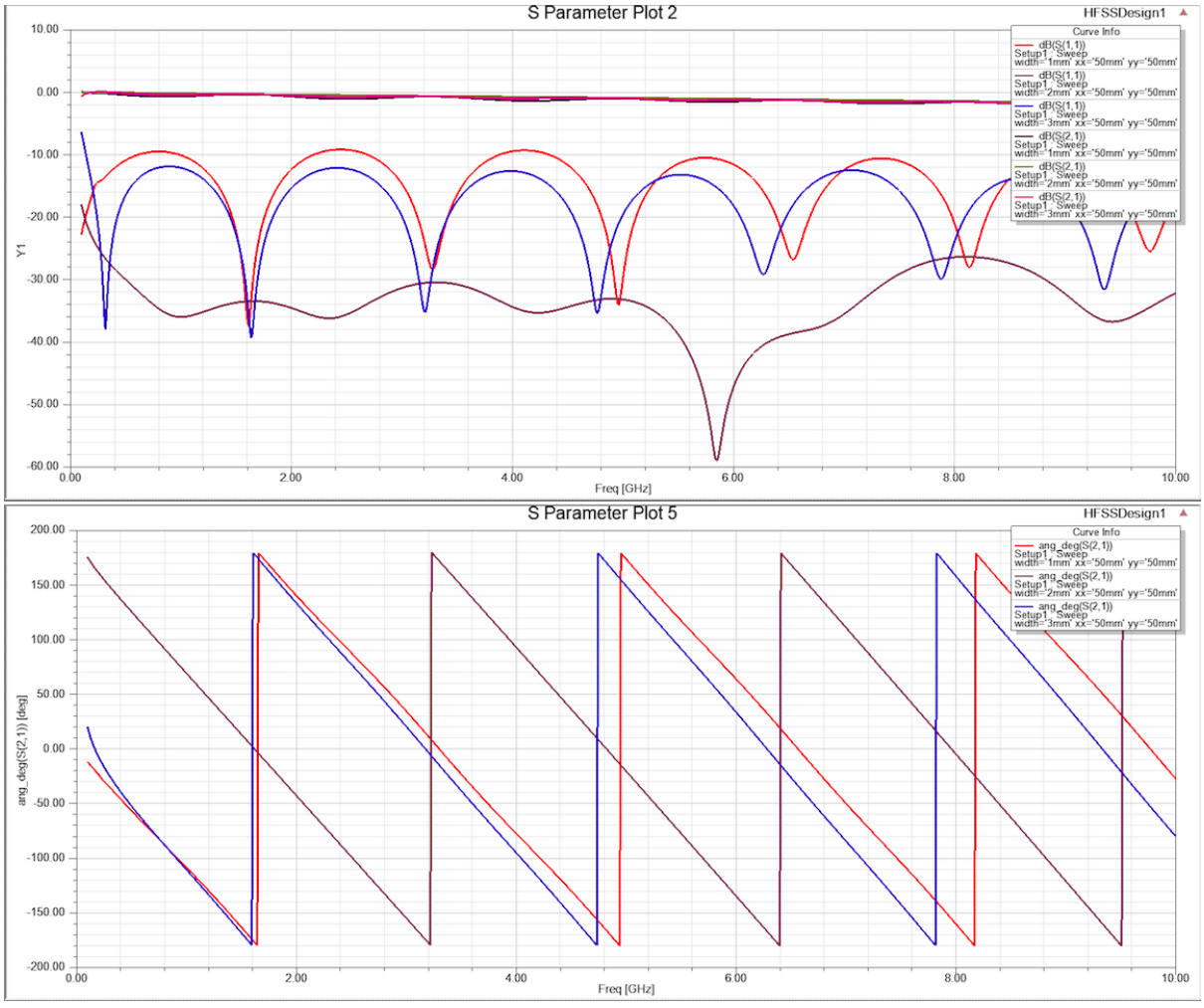
After analysis of our design we can create a S parameter plot that provides a rectangular plot of our results with phase and magnitude of different lines.

Simulation

From our S parameter plots we can find out what is the best length and width of the signal line for our product.



Here we see the effects of the changes in length of our product.



Here we can see the effects of the changes in width of our signal line.

Results

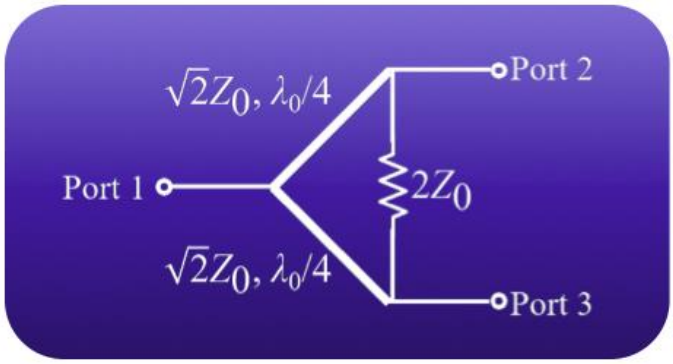
From trial and error, we get the answer that at 50 ohms the width should be 2mm and at 70.7 ohms the width is 1mm. At 3 GHz, for the S parameter plot to show λ/4 the ideal length is 13.1 mm. This is because at 3 GHz it needs to be -90 if the plot starts at 0 and 0 at 3 GHz if it starts at 180.

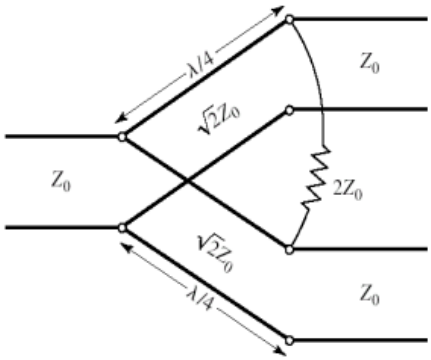
Wilkinson Power Divider

Design

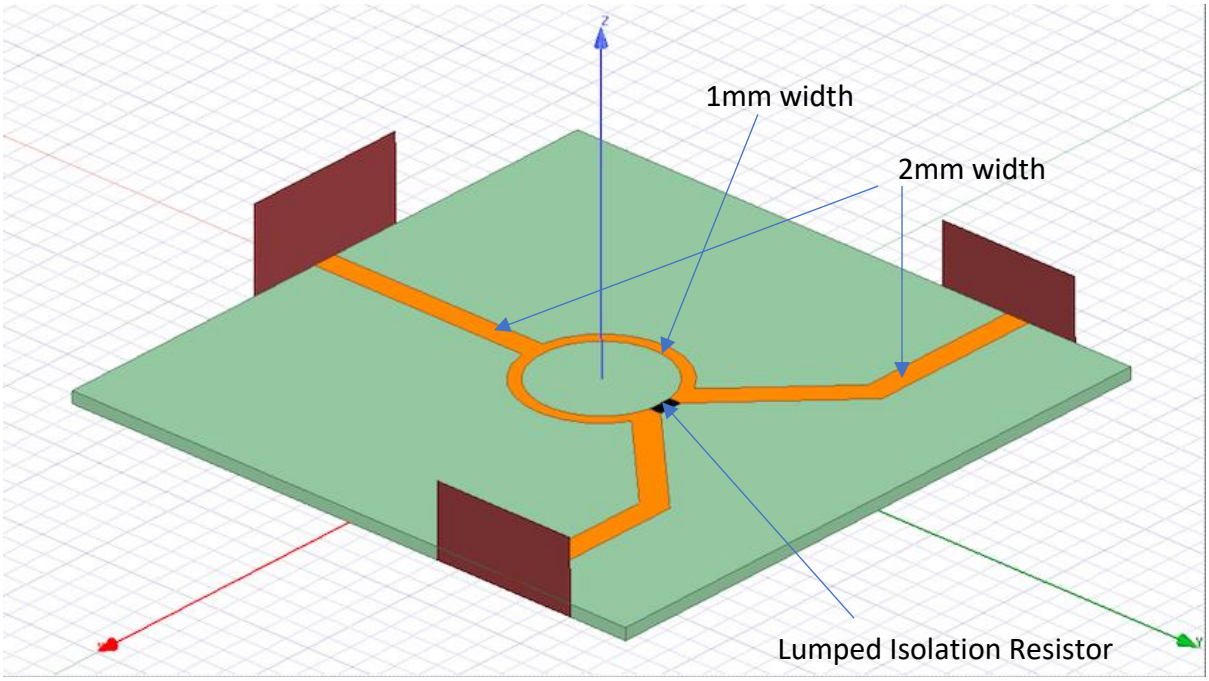
Next, we start to design our Wilkinson Power Divider on our ANYSYS Electronics Desktop application.

Our Wilkinson power divider will be a 3-port network that is symmetric and lossless with the ports being matched. The circuit schematics will look like this





We will have $\lambda_0/4$ impedance transformers having $\sqrt{2}Z_0$ impedance and a lumped isolation resistor of $2Z_0$ with port 1, 2 and 3 all matched to Z_0. We will make $Z_0 = 50$ ohms making the isolation resistor $2Z_0 = 100$ ohms. The $\sqrt{2}Z_0$ impedance will become 70.7 ohms. From our microstrip experiment earlier, we found out that for 50 ohms width of 2mm and for 70.7 ohms 1mm is best.



We changed from our first microstrip design by adding a new wave port and having a circle separated by an isolation resistor on one side to represent the branching into the two output ports.

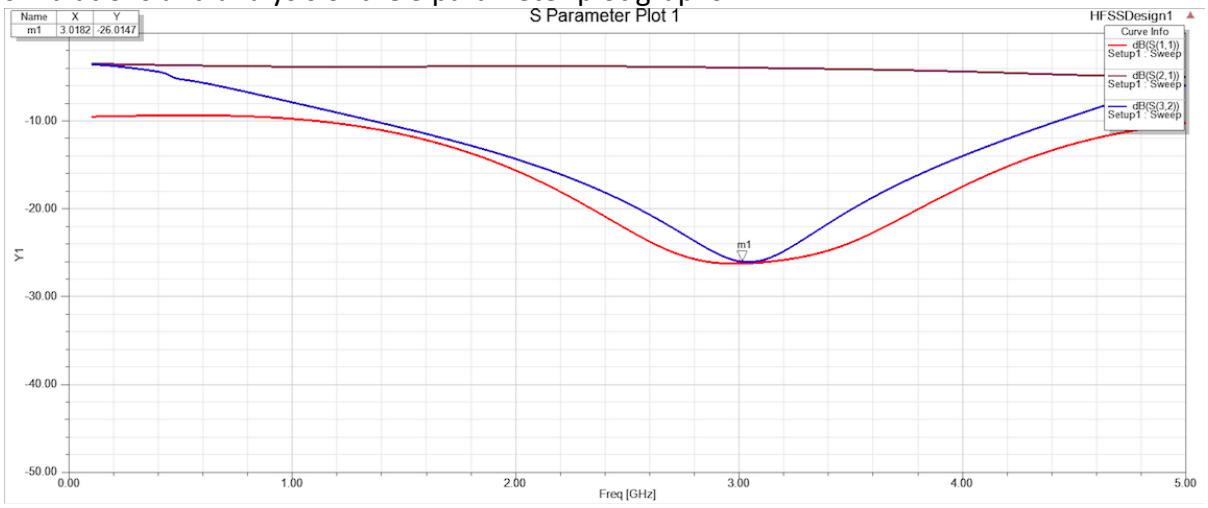
We centered our design right in the middle so it is easier to make a circular line with width 1mm by subtracting the circle with another circle at position (0,0,0) that is smaller in radius by 1. This width is best for $\lambda_0/4$ transmission line as √2 *50 = 70.7 ohms. The rest of the signal line is 2mm as the wave ports are all matched and set at Z_0 = 50 ohms. Our resistor will be set at double that at $2Z_0$ = 100 ohms. Since our circuit is symmetric there will be no current flowing through our resistor.

The resistor will have 1mm width to match the circle signal line and 2mm long to separate the circuit as they diverge towards the two output ports. The type is set to Lumped RLC. After the resistor, the signal line will go back to 2mm width and split off diagonally at √2 multiples away so it lands on a whole number so a new connected rectangle can make it go back evenly to the output wave ports.

I designed my Wilkinson power divider this way from what I learnt in our first practice design of a microstrip. As we are using 50 ohm wave ports the signal line will have width of 2mm with the exception of the circle having 1mm as this width is best for $\lambda_0/4$ transmission line as √2 *50 = 70.7 ohms.

<u>Simulation</u>

This High Frequency Simulator System (HFSS) will show how my product will work through simulations and analysis of the S parameter plot graphs.



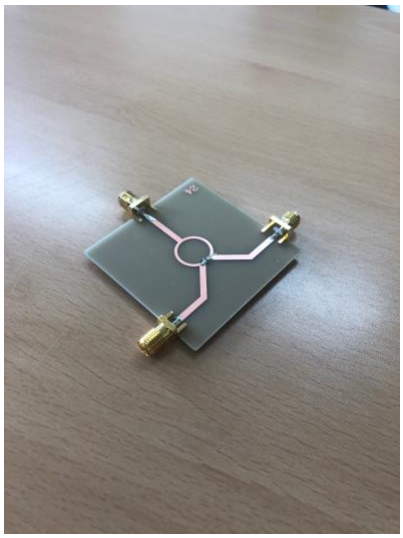
Here we see our dip with the marker at 3.0182 GHz from the S parameter plotted by our simulation. We will see how this change when we make our product in real life and check the actual results.

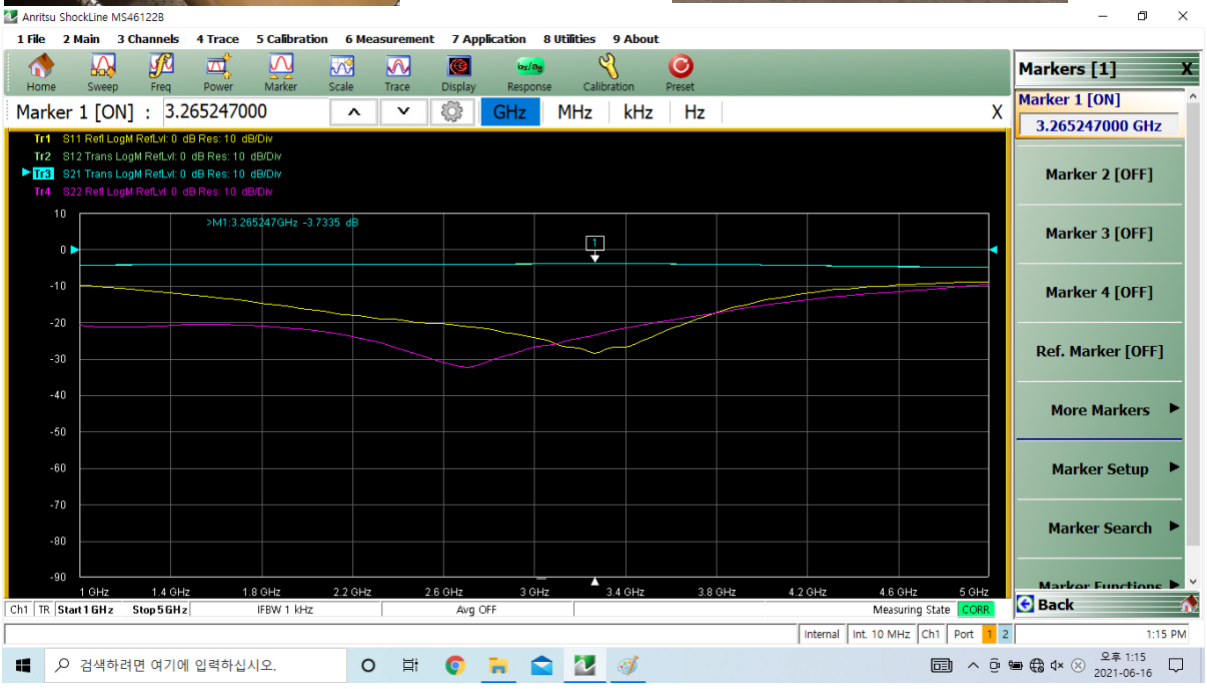
Results

Measure 1

When we measure using two ports the remaining port will just match.

We will use wave port 1 as the input and wave port 2 as the output, the remaining output wave port 3 will just match to the rest.





The yellow line S11 dip is at 3.265247 GHz

The line is off from 3 GHz because the lengths of my signal lines were too long. They need to be reduced further.

S21 also peaks at this point. Their wavelength is similar. S12 and S21 are the same as reciprocity applies. S21 peaks at -3.7335 db. There should be approximately -3 db as coupling will half the power between the input wave port and the output wave port.

Measure 2

We now use the two output wave ports: wave port 2 and wave port 3

Here my S21 is not really S21 but S32 as I have changed the wave port from measure 1.
Here my marker for S32 is at 3.075509 GHz which is much closer to 3 GHz.

Conclusion

By analyzing our data, we see that there should be an equal split between S11 and S32 but mine does not show it. The dips should be showing at 3.01 GHz but our real results show 3.08 in measure 2 and 3.26, which is a larger error, in measure 1. For the small shift to the right in measure 2, there may be various reasons for why this is the case when applying our simulation to real life.

Our simulation by using the ANYSYS Electronics Desktop has objects that are of 2 dimensional planes. Only in simulation we can apply objects with no width but, in real life application, there are no objects with width being zero. We had made the wave ports and signal lines as a 2D object in our simulation. For a more accurate assessment we need to take into consideration of the actual widths in the real world even if they may seem to be negligible because every small thing will factor into our final real-time results. Also, we assumed that there would be a vacuum but that is also near impossible for an average university student to achieve. In the electrical circuit the epsilon is set at 4.4 but that is hard to replicate in the real world.

Furthermore, making the actual product itself is reliant on humans so there will always be human error at all times. The way that the resistor and wave ports were soldered to our product could be slightly offsetting the results as well.

I believe I should have reduced the length of my signal line and in turn the whole Wilkinson power divider. This was shown evidently in the simulations of microstrip that the ideal length would have to be shorter to shift it accordingly but I did not consider those findings in my final design for my Wilkinson power divider. I did not use the ideal length of 13.1mm in the microstrip design and apply that knowledge to my Wilkinson power divider. I did not have much time as my PC laptop was too slow to run many analysis results so I had to work with the best I could get with my limited time.

A true Wilkinson power divider would be lossless and match all ports but it is hard to have any loss of power and have all ports matched. The reflected power could be dissipated through the resistor if there are some human error in making it and the circuit is not symmetrical. The dielectric substrate FR4 material could also be the cause for our product to not be lossless. FR4 material is cheap but can cause a significant dielectric induced loss.