COSE222, COMP212 Computer Architecture
Assignment #6

Solutions

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Exercise 5.2.1

	4 16 bytes = 4 × 32 bits

Exercise 5.2.2

a.	I, J, B[I][0]
b.	I, J

Exercise 5.2.3

a.	A[I][J]
b.	A[J][I]

Exercise 5.3.1

a.

Word Address	Binary Form* (Byte Address)	Tag	Index	Hit/Miss
3	0000 0000 0000 0000 0000 0000 0000 1100	0…0000	0011	Miss
180	0000 0000 0000 0000 0000 0010 1101 0000	0…1011	0100	Miss
43	0000 0000 0000 0000 0000 0000 1010 1100	0…0010	1011	Miss
2	0000 0000 0000 0000 0000 0000 0000 1000	0…0000	0010	Miss
191	0000 0000 0000 0000 0000 0010 1111 1100	0…1011	1111	Miss
88	0000 0000 0000 0000 0000 0001 0110 0000	0…0101	1000	Miss
190	0000 0000 0000 0000 0000 0010 1111 1000	0…1011	1110	Miss
14	0000 0000 0000 0000 0000 0000 0011 1000	0…0000	1110	Miss
181	0000 0000 0000 0000 0000 0010 1101 0100	0…1011	0101	Miss
44	0000 0000 0000 0000 0000 0000 1011 0000	0…0010	1100	Miss
186	0000 0000 0000 0000 0000 0010 1110 1000	0…1011	1010	Miss
253	0000 0000 0000 0000 0000 0011 1111 0100	0…1111	1101	Miss

* The upper 30 bits surrounded by a border is block address.

* The 28 bits shaded yellow is tag and other 4 bits shaded blue is index.

b.

Word Address	Binary Form* (Byte Address)	Tag	Index	Hit/Miss
21	0000 0000 0000 0000 0000 0000 0101 0100	0…0001	0101	Miss
166	0000 0000 0000 0000 0000 0010 1001 1000	0…1010	0110	Miss
201	0000 0000 0000 0000 0000 0011 0010 0100	0…1100	1001	Miss
143	0000 0000 0000 0000 0000 0010 0011 1100	0…1000	1111	Miss
61	0000 0000 0000 0000 0000 0000 1111 0100	0…0011	1101	Miss
166	0000 0000 0000 0000 0000 0010 1001 1000	0…1010	0110	Hit
62	0000 0000 0000 0000 0000 0000 1111 1000	0…0011	1110	Miss
133	0000 0000 0000 0000 0000 0010 0001 0100	0…1000	0101	Miss

111	0000 0000 0000 0000 0000 0001 1011 1100	0…0110	1111	Miss
143	0000 0000 0000 0000 0000 0010 0011 1100	0…1000	1111	Miss
144	0000 0000 0000 0000 0000 0010 0100 0000	0…1001	0000	Miss
61	0000 0000 0000 0000 0000 0000 1111 0100	0…0011	1101	Hit

* The upper 30 bits surrounded by a border is block address.

* The 28 bits shaded yellow is tag and the 4 bits shaded blue is index.

Exercise 5.3.2

a.

Word Address	Binary Form* (Byte Address)	Tag	Index	Hit/Miss
3	0000 0000 0000 0000 0000 0000 0000 1100	0…0000	001	Miss
180	0000 0000 0000 0000 0000 0010 1101 0000	0…1011	010	Miss
43	0000 0000 0000 0000 0000 0000 1010 1100	0…0010	101	Miss
2	0000 0000 0000 0000 0000 0000 0000 1000	0…0000	001	Hit
191	0000 0000 0000 0000 0000 0010 1111 1100	0…1011	111	Miss
88	0000 0000 0000 0000 0000 0001 0110 0000	0…0101	100	Miss
190	0000 0000 0000 0000 0000 0010 1111 1000	0…1011	111	Hit
14	0000 0000 0000 0000 0000 0000 0011 1000	0…0000	111	Miss
181	0000 0000 0000 0000 0000 0010 1101 0100	0…1011	010	Hit
44	0000 0000 0000 0000 0000 0000 1011 0000	0…0010	110	Miss
186	0000 0000 0000 0000 0000 0010 1110 1000	0…1011	101	Miss
253	0000 0000 0000 0000 0000 0011 1111 0100	0…1111	110	Miss

* The upper 29 bits surrounded by a border is block address.

* The 28 bits shaded yellow is tag and the 3 bits shaded blue is index.

b.

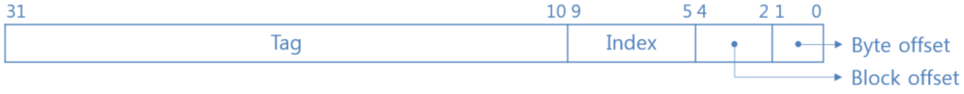
Word Address	Binary Form* (Byte Address)	Tag	Index	Hit/Miss
21	0000 0000 0000 0000 0000 0000 0101 0100	0…0001	010	Miss
166	0000 0000 0000 0000 0000 0010 1001 1000	0…1010	011	Miss
201	0000 0000 0000 0000 0000 0011 0010 0100	0…1100	100	Miss
143	0000 0000 0000 0000 0000 0010 0011 1100	0…1000	111	Miss
61	0000 0000 0000 0000 0000 0000 1111 0100	0…0011	110	Miss
166	0000 0000 0000 0000 0000 0010 1001 1000	0…1010	011	Hit
62	0000 0000 0000 0000 0000 0000 1111 1000	0…0011	111	Miss
133	0000 0000 0000 0000 0000 0010 0001 0100	0…1000	010	Miss
111	0000 0000 0000 0000 0000 0001 1011 1100	0…0110	111	Miss
143	0000 0000 0000 0000 0000 0010 0011 1100	0…1000	111	Miss
144	0000 0000 0000 0000 0000 0010 0100 0000	0…1001	000	Miss
61	0000 0000 0000 0000 0000 0000 1111 0100	0…0011	110	Hit

* The upper 29 bits surrounded by a border is block address.

* The 28 bits shaded yellow is tag and the 3 bits shaded blue is index.

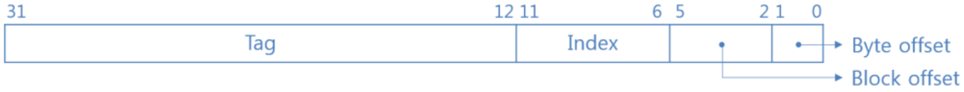
Exercise 5.4.1

a. 8-word



3-bit block offset can represent $2^3 = 8$ different words in a cache line.

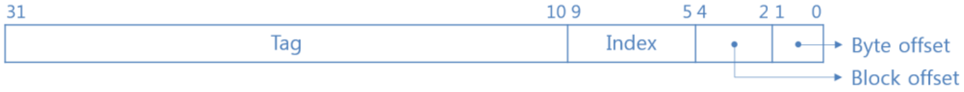
b. 16-word



4-bit block offset can represent $2^4 = 16$ different words in a cache line.

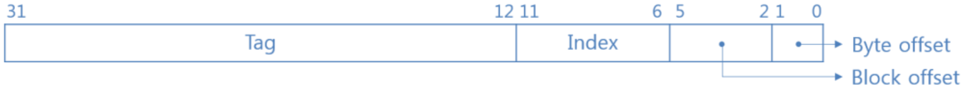
Exercise 5.4.2

a. 32 entries



5-bit index can represent $2^5 = 32$ different entries.

b. 64 entries



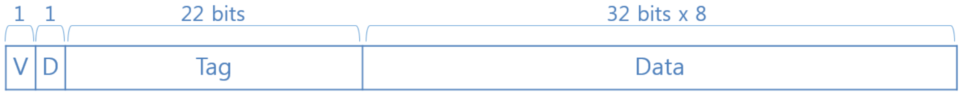
6-bit index can represent $2^6 = 64$ different entries.

Exercise 5.4.3

a. 1.094

(Without V and D bits, the answer would be 1.086)

Assuming we have one valid bit and one dirty bit in our cache implementation, the cache entry looks as below:

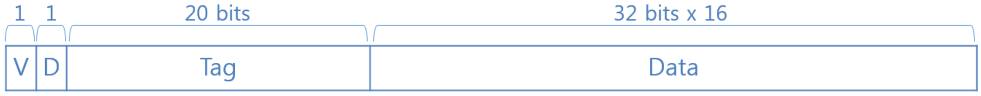


$$\frac{Total\ bits}{Data\ storage\ bits} = \frac{(V + D + Tag + Data)}{Data} = \frac{1 + 1 + 22 + 256}{256} = 1.094$$

b. 1.043

(Without V and D bits, the answer would be 1.039)

Assuming we have one valid bit and one dirty bit in our cache implementation, the cache entry looks as below:



$$\frac{Total\ bits}{Data\ storage\ bits} = \frac{(V + D + Tag + Data)}{Data} = \frac{1 + 1 + 20 + 512}{512} = 1.094$$

Exercise 5.4.4

a.

4 blocks

Byte Address	0	4	16	132	232	160	1024	30	140	3100	180	2180
Index	0	0	0	4	7	5	0	0	4	0	5	4
Hit/Miss	M	H	H	M	M	M	M	M	H	M	H	M
Replace	N	N	N	N	N	N	Y	Y	N	Y	N	Y

* $Index = (Block\ Addr) \bmod (\#\ of\ Entries) = \{Address \gg (Block\ off + Byte\ off)\} \bmod (\#\ of\ Entries) = \lfloor Address/2^5 \rfloor \bmod 32$

b.

0 blocks

Byte Address	0	4	16	132	232	160	1024	30	140	3100	180	2180
Index	0	0	0	2	3	2	16	0	2	48	2	34
Hit/Miss	M	H	H	M	M	H	M	H	H	M	H	M
Replace	N	N	N	N	N	N	N	N	N	N	N	N

* $Index = (Block\ Addr) \bmod (\#\ of\ Entries) = \{Address \gg (Block\ off + Byte\ off)\} \bmod (\#\ of\ Entries) = \lfloor Address/2^6 \rfloor \bmod 64$

Exercise 5.4.5

a.

0.33

Byte Address	0	4	16	132	232	160	1024	30	140	3100	180	2180
Index	0	0	0	4	7	5	0	0	4	0	5	4
Hit/Miss	M	H	H	M	M	M	M	M	H	M	H	M
Replace	N	N	N	N	N	N	Y	Y	N	Y	N	Y

* $Index = (Block\ Addr) \bmod (\#\ of\ Entries) = \{Address \gg (Block\ off + Byte\ off)\} \bmod (\#\ of\ Entries) = \lfloor Address/2^5 \rfloor \bmod 32$

b.

0.5

Byte Address	0	4	16	132	232	160	1024	30	140	3100	180	2180
Index	0	0	0	2	3	2	16	0	2	48	2	34
Hit/Miss	M	H	H	M	M	H	M	H	H	M	H	M
Replace	N	N	N	N	N	N	N	N	N	N	N	N

* $Index = (Block\ Addr) \bmod (\#\ of\ Entries) = \{Address \gg (Block\ off + Byte\ off)\} \bmod (\#\ of\ Entries) = \lfloor Address/2^6 \rfloor \bmod 64$

Exercise 5.7.1

a.

P1 : 1.52 GHz

P2 : 1.11 GHz

$1\ \text{second}/0.66\ \text{ns} = 1.52\text{G}$

$1\ \text{second}/0.90\ \text{ns} = 1.11\text{G}$

b.

P1 : 0.926 GHz (926 MHz)

P2 : 0.495 GHz (495 MHz)

$1\ \text{second}/1.08\ \text{ns} = 0.926\text{G}$

$1\ \text{second}/2.02\ \text{ns} = 0.495\text{G}$

Exercise 5.7.2

a.

P1 : 6.26 ns

P2 : 5.1 ns

$\text{AMAT} = \text{Hit time} + \text{Miss rate} \times \text{Miss penalty}$

$\text{AMAT}_{\text{P1}} = 0.66\text{ns} + 8.0\% \times 70\text{ns}$

$\text{AMAT}_{\text{P2}} = 0.90\text{ns} + 6.0\% \times 70\text{ns}$

b.

P1 : 3.46 ns

P2 : 4.05 ns

$\text{AMAT} = \text{Hit time} + \text{Miss rate} \times \text{Miss penalty}$

$\text{AMAT}_{\text{P1}} = 1.08\text{ns} + 3.4\% \times 70\text{ns}$

$\text{AMAT}_{\text{P2}} = 2.02\text{ns} + 2.9\% \times 70\text{ns}$

Exercise 5.7.3

a.	P1 : 4.05 CPI P2 : 2.68 CPI ⇒ P2 is faster than P1. $\text{L1 miss penalty}_{\text{P1}} = 70\text{ns} = 70\text{ns}/0.66\text{ns (cycles)} = 106 \text{ cycles}$ $\text{CPI}_{\text{P1}} = 1 + 0.36 \times (0.08 \times 106) = 4.02$ $\text{L1 miss penalty}_{\text{P2}} = 70\text{ns} = 70\text{ns}/0.90\text{ns (cycles)} = 78 \text{ cycles}$ $\text{CPI}_{\text{P2}} = 1 + 0.36 \times (0.06 \times 78) = 2.68$
b.	P1 : 1.80 CPI P2 : 1.37 CPI ⇒ P2 is faster than P1. $\text{L1 miss penalty}_{\text{P1}} = 70\text{ns} = 70\text{ns}/1.08\text{ns (cycles)} = 65 \text{ cycles}$ $\text{CPI}_{\text{P1}} = 1 + 0.36 \times (0.034 \times 65) = 1.80$ $\text{L1 miss penalty}_{\text{P2}} = 70\text{ns} = 70\text{ns}/2.02\text{ns (cycles)} = 35 \text{ cycles}$ $\text{CPI}_{\text{P2}} = 1 + 0.36 \times (0.029 \times 35) = 1.37$

Exercise 5.7.4

a.	6.42 ns, Worse $\text{AMAT} = \text{Hit time} + \text{Miss rate} \times \text{Miss penalty}$ $\text{AMAT}_{\text{P1}} = 0.66\text{ns} + 8.0\% \times \{5\% \times 5.62\text{ns} + 95\% \times (5.62\text{ns} + 70\text{ns})\} = 6.42\text{ns}$
b.	3.50 ns, Worse $\text{AMAT} = \text{Hit time} + \text{Miss rate} \times \text{Miss penalty}$ $\text{AMAT}_{\text{P1}} = 1.08\text{ns} + 3.4\% \times \{32\% \times 23.52\text{ns} + 68\% \times (23.52\text{ns} + 70\text{ns})\} = 3.50\text{ns}$

Exercise 5.7.5

a.	4.16 CPI $\text{L2 \\$ access time} = 5.62\text{ns}$ $\text{L1 miss penalty} = 5.62\text{ns}/0.66\text{ns (cycles)} = 9 \text{ cycles}$ $\text{Extra penalty} = 70\text{ns}/0.66\text{ns (cycles)} = 106 \text{ cycles}$ $\text{CPI}_{\text{P1}} = 1 + 0.36 \times \{0.08 \times (5\% \times 9 + 95\% \times (9 + 106)\} = 4.16$
b.	1.81 CPI $\text{L2 \\$ access time} = 23.52\text{ns}$ $\text{L1 miss penalty} = 23.52\text{ns}/1.08\text{ns (cycles)} = 22\text{cycles}$ $\text{Extra penalty} = 70\text{ns}/1.08\text{ns (cycles)} = 65 \text{ cycles}$ $\text{CPI}_{\text{P1}} = 1 + 0.36 \times \{0.034 \times (32\% \times 22 + 68\% \times (22 + 65)\} = 1.81$