Seung Jun Baek

1. Draw the logic diagram of a 2-to-4-line decoder using NOR gates only. Include an enable input.
2. Construct a 4-to-16-line decoder with five 2-to-4-line decoders with enable.
3. Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions:
   $F_1 = x'yz' + xz$
   $F_2 = xy'z' + x'y$
   $F_3 = x'y'z' + xy$
4. An 8×1 multiplexer has inputs A , B , and C connected to the selection inputs S_2 , S_1 , and S_0 , respectively. The data inputs I_0 through I_7 are as follows:

   $I_1 = I_2 = I_7 = 0; I_3 = I_5 = 1; I_0 = I_4 = D$; and I_6 = D ’
5. Implement the following Boolean function with a 4×1 multiplexer and external gates.

   $F_1(A, B, C, D) = \sum(1, 3, 4, 11, 12, 13, 14, 15)$
6. A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively.

   (a) * Derive the characteristic equation.
7. A sequential circuit has one flip-flop Q, two inputs x and y, and one output S . It consists of a full-adder circuit connected to a D flip-flop, as shown in Fig. P5.7 . Derive the state table and state diagram of the sequential circuit.

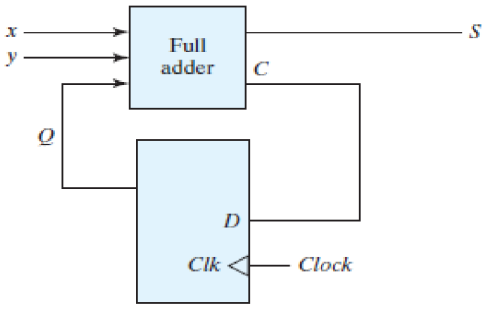

FIGURE P5.7

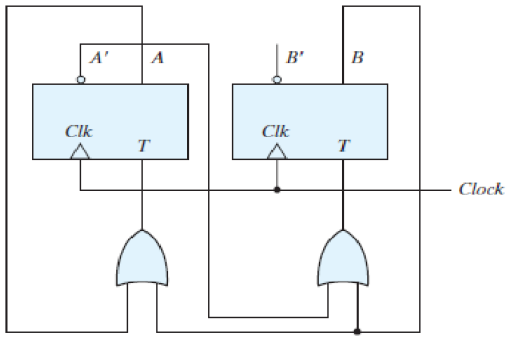

FIGURE P5.8

8. Derive the state table and the state diagram of the sequential circuit shown in Fig. P5.8 .Explain the function that the circuit performs. (HDL-see Problem 5.36.)

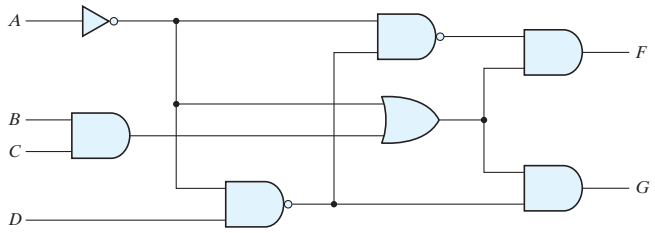

Figure 1

9. Find the critical path in Fig 1.

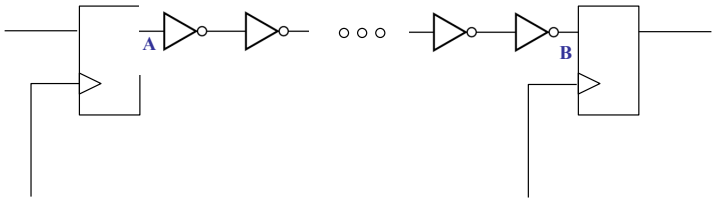

Figure 2

10. For Fig. 2 assume that

    (a) setup time is 2 ns

    (b) hold time is 2 ns

    (c) propagation delay of one inverter is 1 ns

(d) propagation delay from the clock edge to flip-flop output is 1 ns

(e) Clock frequency is 100 MHz.

How many inverters can be put in order to satisfy timing constraints?

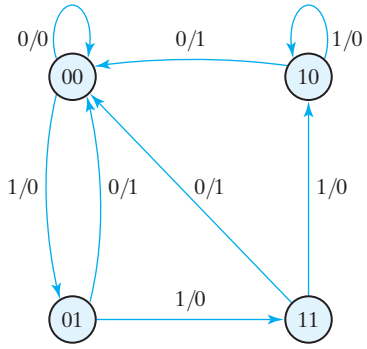

FIGURE 5.16

11. For the circuit described by the state diagram of Fig. 5.16

    (a) * Determine the state transitions and output sequence that will be generated when an input sequence of 010110111011110 is applied to the circuit and it is initially in the state 00.

12. For state table given by Table 1 tabulate the reduced state table.

Table 1: table

	Next State	Next State	Output	Output
Present State	x =0	x =1	x =0	x =1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

13. Design a sequential circuit with two D flip-flops A and B, and one input x_in . When x_in = 0, the state of the circuit remains the same. When x_in = 1, the circuit goes through the state transitions from 00 to 01, to 11, to 10, back to 00, and repeats.