Imperial College of Science Technology and Medicine
Department of Electrical and Electronic Engineering
1st Year Electronics Laboratory
EEBUG Group Design Project

# **Stage 2 Report** cover sheet

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***(EE1-LABE EEE 1st Year Electronics Lab (2014-2015)/ Group Design Project assessments)***

| | |
|---|---|
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| "A" or "B" Group | A |
| Design Group | CPA |
| Name of lab marker (see labweb) | Dr T Constandinou |
| Submission date | Friday, 27 March 2015 |

| **Checklist** (see labweb for guidance) | Yes / No |
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| *LATE SUBMISSION*<br>*The Department's publicised policy is that coursework submitted after the deadline automatically fails.*<br><br>*However, if there are genuine extenuating circumstances which make it impossible to submit on time, please explain.* | *Reasons for late submission:* |

# TABLE OF CONTENTS

1 Introduction ..... 3
2 Project Summary ..... 3
2.1 Timeline and Milestones ..... 3
2.2 Project Members, Contributions and Personnel Issues ..... 4
3 Design Brief and Enhancements ..... 5
4 High Level Design ..... 5
5 Low Level Design ..... 6
The Low Level Circuit Diagram ..... 7
5.1 Stage 1 ..... 8
5.1.1 Line Detection ..... 8
5.1.2 Line Following ..... 8
5.1.3 Conclusion/Comments ..... 9
5.2 Stage 2 ..... 9
5.2.1 End of Line Detection ..... 9
5.2.2 Triggering of Timer ..... 9
5.3 Stage 3 ..... 11
5.3.1 Latch ..... 11
5.3.2 Transition from Stage 1 to Stage 3 (Right motor) ..... 12
5.3.3 Transition from Stage 1 to Stage 3 (Left motor) ..... 13
5.3.4 Voltage Varying Control ..... 13
5.3.5 Stop ..... 14
5.3.6 Conclusion ..... 14
6 Testing ..... 15
6.1 Breadboard Configuration ..... 15
6.2 Test Procedure ..... 17
6.2.1 Stage 1 ..... 17
6.2.2 Stage 2 ..... 18
6.2.3 Stage 3 ..... 18
6.2.4 Conclusion ..... 19
7 Budgeting and Costing ..... 20
8 SuperBug ..... 21
8.1 Spiral Setting ..... 21

8.2 Remote Start ..... 21
9 References ..... 22
Appendix 1. Meeting Minutes ..... 23
Appendix 2 – Calendar and Timeline ..... 27
Appendix 3 – Method of Approach ..... 29
Appendix 4 – Remote Starting of EEBug ..... 30
Appendix 5 – Picture of EEBug ..... 32
Appendix 6 – List of Lab Components ..... 33
Appendix 7 – Component Order Form ..... 34

# 1 INTRODUCTION

This team-based design project aims to encourage teamwork, creativity, application of theory and independent learning among its members. The end product envisioned is an enhanced EEBug that adheres to the design parameters and budget constraints.

Following the preliminary report, this report aims to formalise the analysis and testing of proposed ideas through high and low level design, simulations and experimental results as well as discuss budgeting and project management.

# 2 PROJECT SUMMARY

In the Autumn Term, ideas were generated for the EEBug to achieve the required functionality. Spring term was then used to implement the ideas through high level design, low level circuit design and testing.

The design criteria was delineated into three tasks with division of labour shown in Table 1.

| Task 1 | Task 2 | Task 3 |
|---|---|---|
| **Sam (Sub leader)**<br>Elliot | **Chung (Sub Leader)**<br>Barry | Benjamin<br>**Nicholas (Sub Leader)**<br>Savvas |

*Table 1: Division of Labour*

While each subgroup was tasked to focus on a single portion of the EEBug, all members were reminded to keep track of the various updates of the subgroups, this was ensured during weekly group meetings to update all members on respective progresses. Refer to Appendix 1 for meeting minutes.

## 2.1 TIMELINE AND MILESTONES

Table 2 details the various deadlines set and achieved. As detailed planning was already done in the Autumn Term, a large amount of time in Spring Term was allocated to the low level testing and integration and hence, there was excellent time management.

| No. | Milestone | Deadline/Timeline | Achieved | Comments |
|---|---|---|---|---|
| 1. | Preliminary Meeting and Administration | 28 Jan 15 | ✓ | |
| 2. | Submission of Individual High Level Designs | 02 Feb 15 | ✓ | |
| 3. | Discussion of Low Level Design | 04 Feb 15 | ✓ | |
| 4. | Private procurement of components | 06 Feb 15 | ✓ | 2 Op amps and 1 NAND Gate was procured from rapid |
| 5. | Preliminary Submission of Low Level Designs | 09 Feb 15 | ✓ | |
| 6. | Low Level Subgroup Lab Testing | 11 Feb 15 – 18 Feb 15 | ✓ | More time was required for subgroup testing |
| 7. | Preliminary Meeting with | 16 Feb 15 | ✓ | Preliminary Approval |

| | | | | |
|---|---|---|---|---|
| | Tutor | | | of Plan |
| 8. | Low Level Group Integration | 25 Feb 15 – 20 Mar 15 | ✓ | |
| 9. | Submission of Low Level Design Template | 27 Feb 15 | ✓ | |
| 10. | Follow Up Meeting with Tutor | 2 Mar 15 | ✓ | Final Approval of Plan |
| 11. | Submission of Budgeting Details | 10 Mar 15 | ✓ | |
| 12. | Finalised Group Testing | 21 Mar 15 | ✓ | |
| 13. | Completed Report | 26 Mar 15 | ✓ | |

*Table 2: Timeline and Milestones*

Refer to Appendix 2 for a calendar the group used as reference during the course of the project.

## 2.2 Project Members, Contributions and Personnel Issues

Table 3 lists the various members and their contributions based on their respective strengths.

| Member | CID | Role | Contributions |
|---|---|---|---|
| Ng, B.(Benjamin) | 986013 | Leader | 1. Overall management of the Project, ensuring meeting of deadlines (Lead)<br>2. Low level circuit integration<br>3. Compiled Report (Lead) |
| Low, Z.K.N (Zuo) | 941910 | Secretary | 1. Built Report<br>2. Low level circuit integration (Lead) |
| Poon, C.M. (Chung) | 949509 | Assistant Secretary | 1. Meeting Minutes<br>2. Low level circuit integration (Lead)<br>3. Built Report |
| Polychronis, S. (Savvas) | 969411 | Treasurer | 1. Budgeting (Lead)<br>2. Research on components and costs<br>3. Low level circuit integration |
| Steele, E. (Elliot) | 931869 | Counter-Signatory | 1. Approved purchases<br>2. Collected components |
| Zatland, S. (Samuel) | 818847 | Designer | 1. Simulation Tester (Lead)<br>2. Low level circuit integration |
| Alimi, M.O (Mubarak) | 937257 | Assistant Designer | 1. Assisted Designer |

*Table 3: Roles and Responsibilities*

# 3 DESIGN BRIEF AND ENHANCEMENTS

The design criteria can be decomposed into three main tasks:

Stage 1 – Follow a black track on a white background and leaves a mark to indicate its presence

Stage 2 – Continue straight for 20cm after track ends

Stage 3 – Draw a spiral with decreasing radius (minimum 12cm) and make a full turn before stopping

There are two main methods of implementation – modification through analogue methods or through a microcontroller. The advantages and disadvantages of both are as listed in Appendix 3. Through preliminary testing, it was decided that the motor noise would be difficult to reduce to avoid interfering with the microcontroller due to its large magnitude and random nature. Therefore, the following sections detail the group's analogue approach.

# 4 HIGH LEVEL DESIGN

Electronic engineering and design are complex tasks. Hence, it is essential to approach the task in two ways – through both High Level and Low Level Designs – allowing better project management.

High Level Design approaches the task by developing each subtask into a module with its input, output and function. This allows envisioning of the interconnections between modules, how they can be combined and controlled.

Figure 1 details the group's modularisation of the overall design, where inputs and outputs of each modules are defined as well as its function.

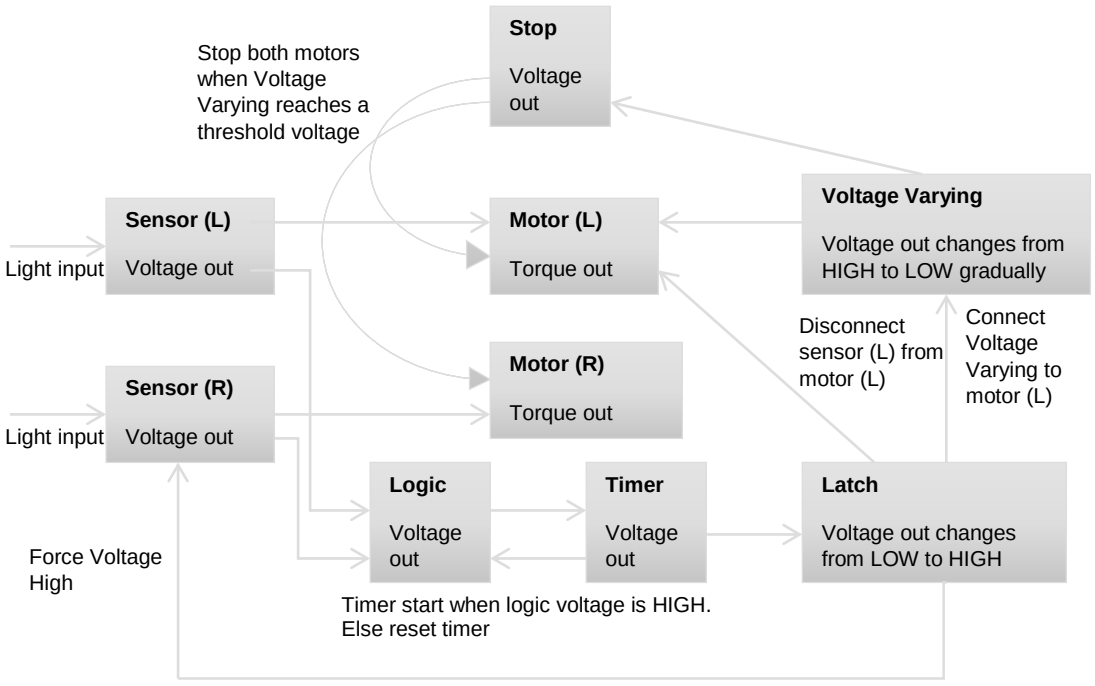


*Figure 1: The High Level Design*

# 5 LOW LEVEL DESIGN

With reference to the high level design and the earlier subdivision of the various tasks, the group started on their respective low level designs, with considerations of each stage's input and outputs.

While implementing the circuit from a High Level Design may result in complications at a low level, starting from a High Level Design allowed the design process to be simplified and ensured efficiently delegation of work.

This method of design also enabled individual troubleshooting of the modules and clarified the implementation process. Once the group had agreed on the low level implementation of the modules, the High Level Design was updated to reflect the current solution used.

## THE LOW LEVEL CIRCUIT DIAGRAM

**Red:** Line Detection and Following

**Blue:** End of Line Detection & Time 20cm run

**Green:** Latch

**Cyan:** Stage 1 Motor

**Pink:** Transition from Stage 1 to 3

**Brown:** Voltage varying control 3

**Stop: Orange**

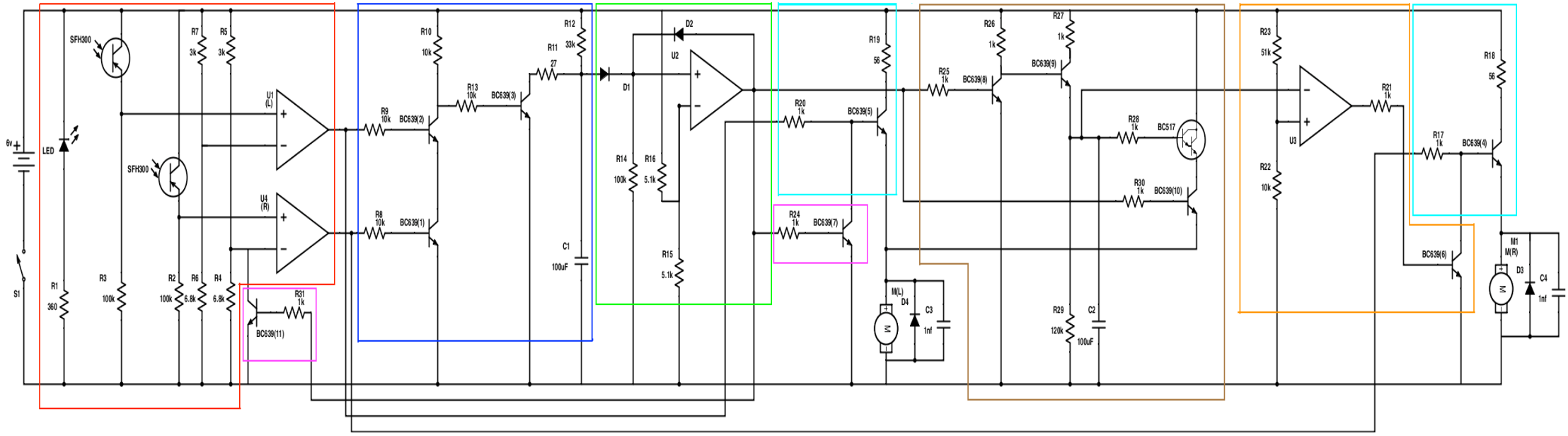


*Figure 2: Circuit Diagram*

## 5.1 STAGE 1

### 5.1.1 Line Detection

#### *5.1.1.1 Circuit Description*

As seen in Figure 2, the LED is connected across the supply rails along with a 430Ω Resistor for protection. The phototransistor SFH300 is connected in series with a 100kΩ resistor and to the positive input, $V_+$ of the Op-Amp. (1)

The Op-Amp is configured in a comparator circuit where $V_+$ is the input voltage and $V_-$ is the reference voltage. To ensure that voltage levels remained consistent, the sensors were fixed at 0.5cm from the surface. (2)

When a black line is detected, the phototransistor receives less light and thus less current flows through Resistor R2, resulting in a lower voltage drop across R2 and the voltage at $V_+$ is thus low. Consequently, when a white line is detected, the phototransistor receives more light, and thus more current flows through Resistor R2, resulting in a greater voltage drop across R2 and hence a higher voltage at $V_+$.

The reference voltage $V_-$ is chosen as the mean between the two possible voltages present at $V_+$. The input, outputs and implications of this circuit is as shown in Table 4.

| Input | Voltage Output | Comments |
|---|---|---|
| $V_+ > V_-$ | $V_{supply}$ | Bug detects a white surface (High) |
| $V_+ < V_-$ | 0V (ideally) | Bug detects a black surface (Low) |

*Table 4: Input-Output Relationship of the Comparator Circuit*

### 5.1.2 Line Following

#### *5.1.2.1 Circuit Description*

To control the movement of the bug, each motor is controlled by a BJT with its base connected to the output of the comparator circuit. (3)

The BJTs will prevent current flow through the motor when the comparator detects a black line and allow current through the motor when no black line is detected. In doing so, the bug will alter its path to follow the line by constant correction to maintain the line in the middle of the two phototransistors.

The diodes D3 and D4 function as clamping diodes. They prevent any back E.M.F. from the motor from damaging the sensitive op-amps. (4) Resistor R19 and R18 of 56Ω are used to limit the maximum speed of the motors to ensure that the momentum of the bug does not cause it to overshoot the line. However, the motors must be fast enough to distinguish gaps in the track from the end of the line.

The inputs, outputs and implications of this part of the circuit in given example situations is summarised in Table 5.

| Phototransistor | Input | Output | Comments |
|---|---|---|---|
| **Bug tends to the right (Line curves to the left)** | | | |
| **Left** | Low (Detects black) | Motors turned off | Differential turning to the left |
| **Right** | High (Detects white) | Motors turned on | |
| **Bug tends to the left (Line curves to the right)** | | | |
| **Left** | High (Detects white) | Motors turned on | Differential turning to the right |
| **Right** | Low (Detects black) | Motors turned off | |

*Table 5: Input Output Characteristics*

### 5.1.3 Conclusion/Comments

The phototransistor allows accurate line detection through the use of a reference voltage. The comparator circuit is essential for comparing white or black input values and consequently producing a high or low value.

## 5.2 STAGE 2

### 5.2.1 End of Line Detection

#### *5.2.1.1 Circuit Description*

To distinguish between cases when only one sensor and when both sensors detect a white surface, a NAND gate is used. From Table 6, the NAND output is LOW only when both inputs are HIGH. This implies that both sensors detect a white surface. If the line is detected, the NAND output would be HIGH. (5)

| Sensor 1 | Sensor 2 | NAND Output |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

*Table 6: Truth Table for NAND Gate*

### 5.2.2 Triggering of Timer

#### *5.2.2.1 Circuit Description*

There are two instances in which both sensors will detect a white surface – when there is a gap in the line and when the line has ended. A trigger timer circuit is implemented to distinguish between the two instances.

As seen in Figure 3, when the output of the NAND gate is HIGH, Q1 turns on, and provides a discharge path for capacitor C1. On the other hand, when the output of the NAND gate is LOW, Q1 turns off, and allows capacitor C1 to charge.

### *5.2.2.2 Simulation*

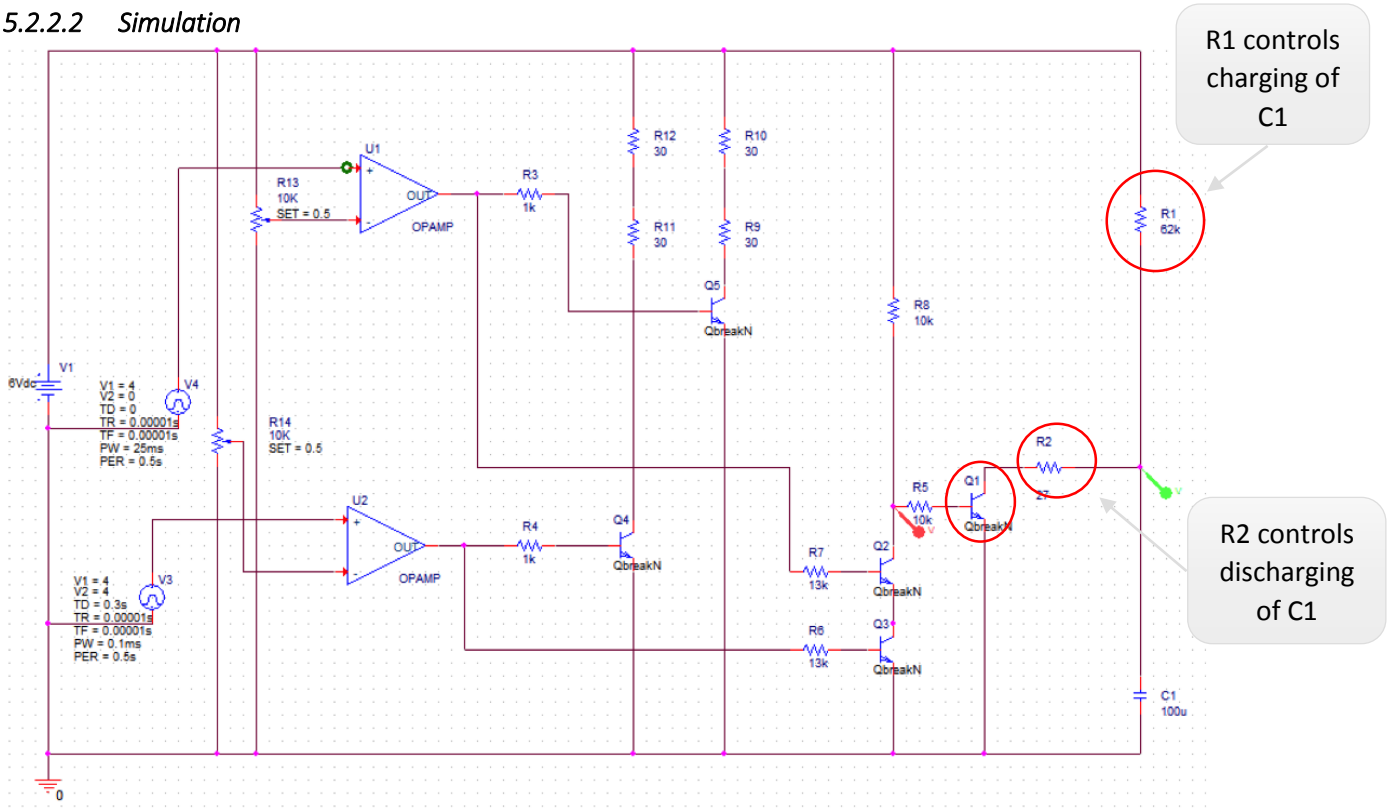


*Figure 3: PSPICE circuit for simulation of timer*

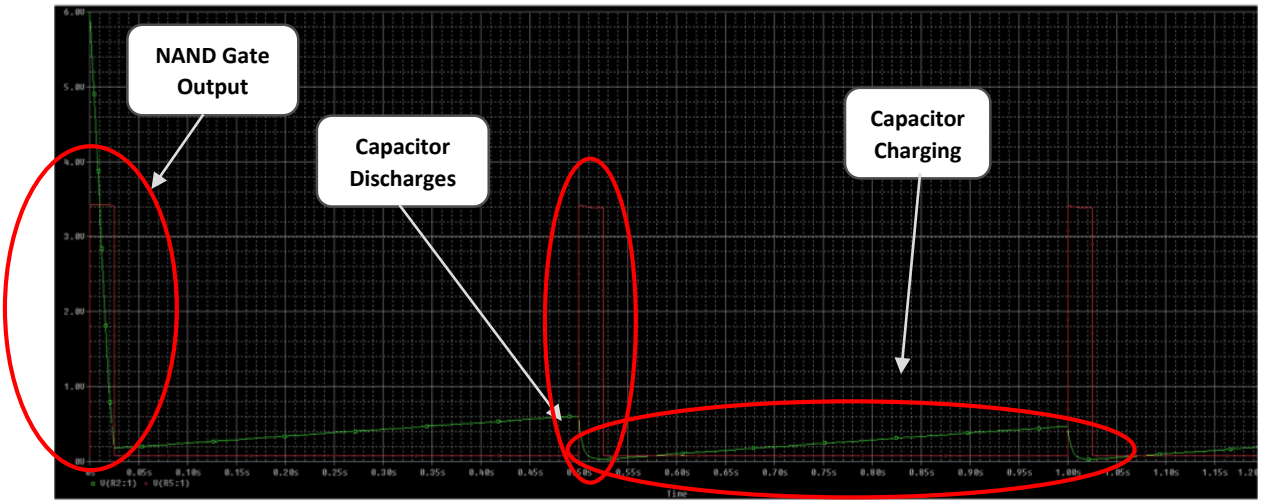


*Figure 4: Simulation of timer operation*

The red pulses in Figure 4 represent the NAND output while the green represents the capacitor's voltage. The capacitor discharges when the red pulse is high and charges when the red pulse is low. The charging time of the capacitor to a desired threshold voltage thus acts as the Debug's timer.

Throughout Stage 1, there are numerous instances when the EEBug will detect the line. Whenever the line is detected, the output of the NAND goes high and the capacitor is immediately discharged, resetting the timer. As long as the line is present, the timer will constantly be reset. Thus, the only instance the timer will not be reset is when the line has ended. (6)

| Sensor 1 | Sensor 2 | NAND Output | BJT Q1 | Capacitor Voltage | Timer |
|---|---|---|---|---|---|
| 0 | 0 | 1 | ON | Discharged | Reset |
| 0 | 1 | 1 | ON | Discharged | Reset |
| 1 | 0 | 1 | ON | Discharged | Reset |
| 1 | 1 | 0 | OFF | Charging | Timing |

*Table 7: States of individual components in Stage 2*

Hence, by choosing the appropriate resistor values, the timer is configured such that the EEBug must travel 20cm without detecting the line before the timer charges up to the threshold voltage which subsequently triggers Stage 3. This allows it to distinguish between the end of the line and simple gaps in the line due to the differences in charging times of the two situations.

## 5.3 STAGE 3

### 5.3.1 Latch

#### *5.3.1.1 Circuit Description*

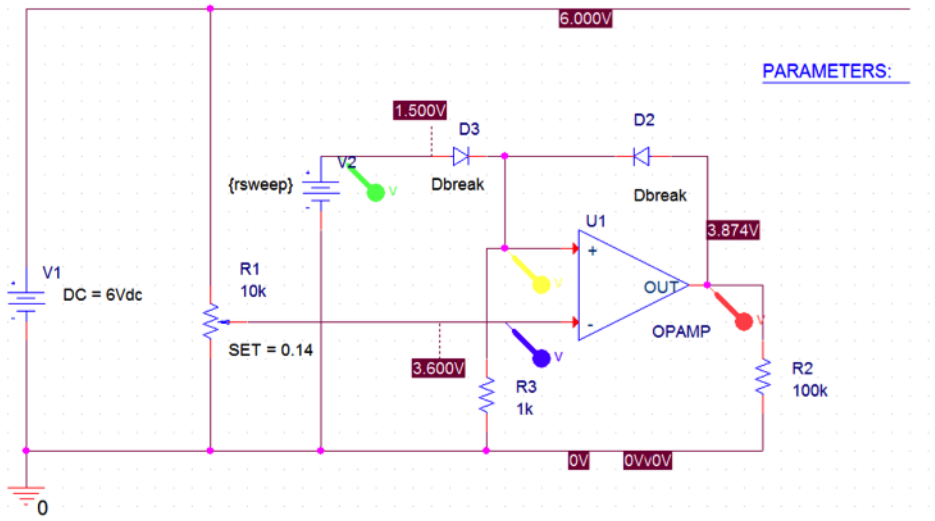


*Figure 5: Latch circuit*

When the timer has reached threshold voltage, Stage 3 is triggered. This desired voltage is equal to $V_-$ of the latch op-amp, while the timer voltage is connected to $V_+$. An op-amp is used as a latch circuit as an OpAmp latch circuit is both more 'reliable' than a transistor latch circuit and more space efficient. D2 applies positive feedback, while $V_-$ is chosen using an appropriate potential divider. (7) (8)

When the timer output $V_+$ is larger $V_-$, $V_{out}$ increases to 6V and also forces $V_+$ to remain at 5.3V (assuming diode drop of 0.7V) through positive feedback. D1 prevents the latch output from returning to 0V even if timer output decreases below $V_-$.

The latch circuit remains at 0V until the timer has reached the desired voltage and triggers it, after which it will remain 6V permanently. Thus, the latch acts as a control signal to indicate that stage 3 has begun.

#### *5.3.1.2 Simulation*

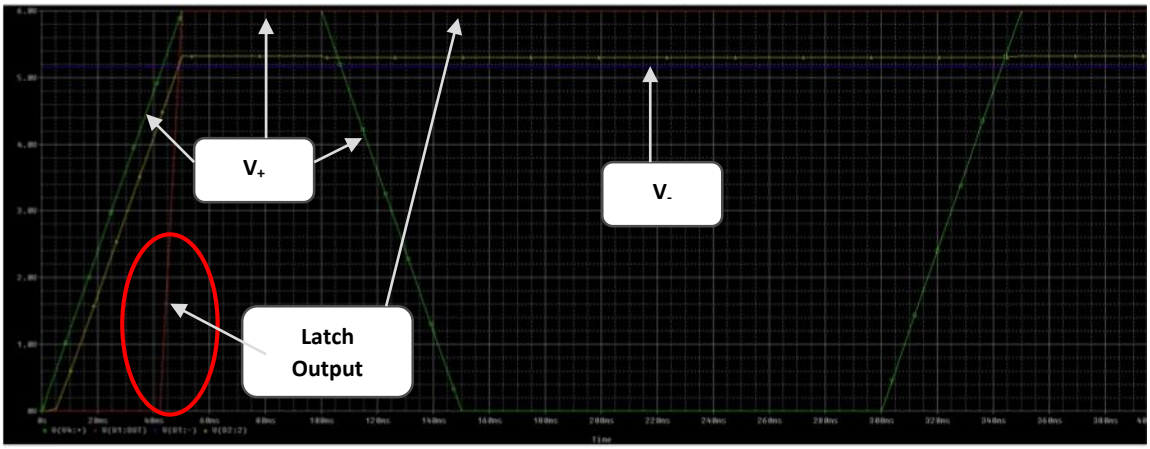


*Figure 6: Latch operation*

When the timer voltage $V_+$ (green pulse) exceeds the reference voltage (blue line) by 0.7V due to the diode voltage drop, the output of the latch goes high(red line). Even if the timer voltage decreases, the latch remains high.

Assuming that the op-amp supply rails are at 5.8V, the maximum reference voltage must be approximately 5.8 – 0.7 = 5.1V. If the reference voltage is any higher, the latch will never trigger since the required timer voltage will exceed the power supply.

In practice, the reference voltage will be set at a value the timer will exceed after the bug travels 20cm, which will not be close to the upper bound of 5.1V.

### 5.3.2 Transition from Stage 1 to Stage 3 (Right motor)

To enable differential turning of Stage 3, the Left motor is designed to move at decreasing speed, while the Right motor remains at constant speed.

#### *5.3.2.1 Circuit Description*

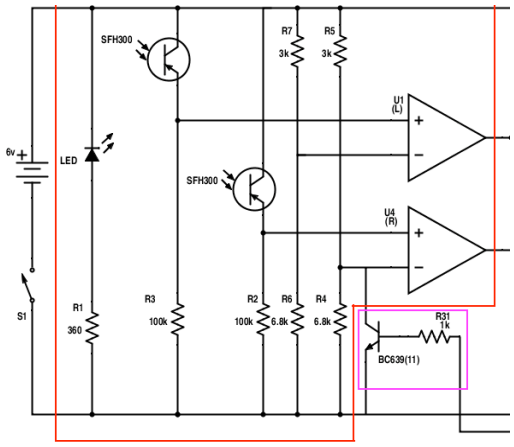


*Figure 7: Transition from Stage 1 to 3 (Right Motor)*

As seen from the High Level Design, a control signal from the latch must decouple Stage 1 from the motors and give full control to Stage 3 elements. This prevents sensory input from Stage 1 from affecting Stage 3 motion, and is achieved using the latch.

Figure 7 (pink) illustrates how this can be achieved. When the latch output goes HIGH, BC639 (11) will pull V- to ground. Now, regardless of sensory input, the op-amp output voltage will be always HIGH. As described in Stage 1, the Right motor will now be moving at a constant speed.

### 5.3.3 Transition from Stage 1 to Stage 3 (Left motor)

#### *5.3.3.1 Circuit Description (Decouple Stage 1)*

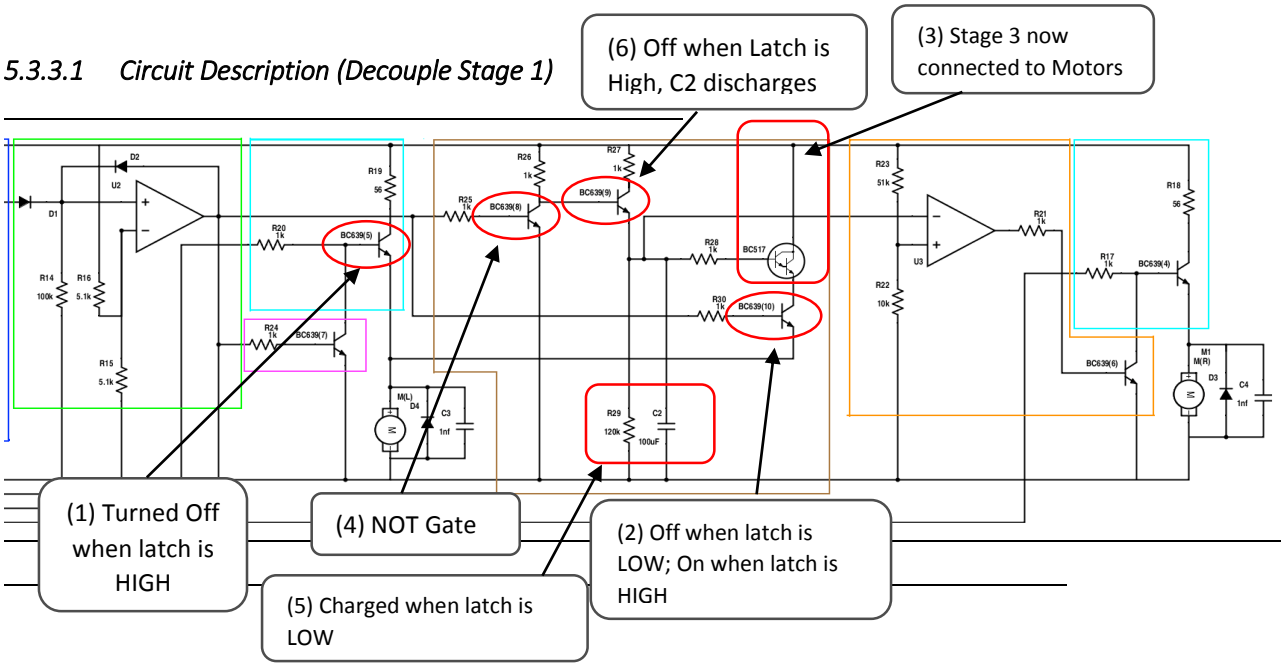


*Figure 8: Voltage Varying Control & Stop*

To decouple stage 1 from the Left motor, the principle is similar but with a few alterations. Instead of decoupling stage 1 through the sensor stage, a more direct approach is used.

Figure 8 (light blue) shows how Stage 1 controls the motor circuit. Figure 8 (pink) shows that when BC639 (7) is ON via latch output going HIGH, the base of BC639 (5) is pulled to ground. This effectively stops the motor circuit from Stage 1 regardless of input from the sensor stage.

#### *5.3.3.2 Circuit Description (Connect Stage 3)*

Unlike the Right motor, decoupling stage 1 is insufficient. Stage 3 must be connected to the motor circuit simultaneously. Additionally, Stage 3 cannot interfere with Stage 1 before the latch signals that Stage 3 begins.

This is done through BC639 (10). Figure 8(brown) shows that when the latch output is LOW, the motor circuit is disconnected from Stage 3 elements due to BC639 (10) being OFF. When latch is ON, BC639 (10) forms a closed path, connecting Stage 3 to the motor circuit.

### 5.3.4 Voltage Varying Control

#### *5.3.4.1 Circuit Description*

Varying the voltage across the motors varies their speed. In Stage 2, the timer circuit is one exemplifies a time varying voltage signal. The RC timer circuit is comprised of R29 and C2.

To reduce the speed of the motors gradually, a voltage varying signal that decreases over time is needed at the base of BC517, a Darlington pair which allows the motor to be controlled by a voltage signal by amplifying the current needed to power the motors.

This voltage varying signal is generated by charging the RC circuit during Stage 1 quickly, before Stage 3 occurs and discharging it when Stage 3 occurs.

This is implemented using BC639 (8) & (9). BC639 (8) acts as a NOT gate, inverting the latch control signal. Thus, during Stage 1, BC639 (9) receives an input of HIGH at the base, which provides a low resistance conduction path to charge the RC circuit. When Stage 3 occurs, BC639 (9) receives an input of LOW at the base and turns OFF, allowing the RC circuit to discharge slowly to 0V.

This voltage is then input to the base of BC517, which causes the left motor to move with decreasing speed before finally stopping.

### 5.3.5 Stop

#### *5.3.5.1 Circuit Description*

As the left motor stops independently while the right motor moves at a constant speed, the right motor has to stop when Stage 3 ends.

In Figure 8 (orange), an op-amp comparator compares the voltage of the left motor with a threshold voltage. Stage 3 ends with the left motor's voltage decreasing to the threshold voltage. The comparator's output voltage goes from LOW to HIGH, which then pulls the base of BC639 (4) to ground. As described in Section 5.3.3.1, this stops the motor.

### 5.3.6 Conclusion

When Stage 2 ends, the latch output is able to decouple Stage 1 from the motors and allow Stage 3 to take over, causing the EEBug to move in a spiral of decreasing radius before coming to a stop.

# 6 TESTING

To ensure that the bug performs according to the design brief, a prototype EEBug was created. Table 8 details the breadboard connections.

## 6.1 BREADBOARD CONFIGURATION

| Type | Pin 1 | Pin 2 | Pin 3 | Colour/value | Note |
|---|---|---|---|---|---|
| LED | I1 | W2 (6V) | | Purple/blue | |
| R1 | J1 | Y1(GND) | | 360Ω | |
| Phototransistor(1) | B9 | W3(6V) | | Green/Yellow | |
| Phototransistor(2) | I9 | Z1(6V) | | Grey/White | |
| MC33078p | F7 (pin1) | E7(pin8) | | | |
| R2 | A9 | X9 | | 100kΩ | |
| R3 | J9 | Y9 | | 100kΩ | |
| R4 | A8 | X8 | | 6.8kΩ | P. divider |
| R5 | B8 | W8 | | 3 kΩ | P. divider |
| R6 | J8 | Y8 | | 6.8 kΩ | P. divider |
| R7 | I8 | Z8 | | 3 kΩ | P. divider |
| NAND | | | | | |
| L1 | D7 | D14 | | pink | OpAmp o/p to NAND |
| L2 | G7 | G14 | | pink | ‘’ |
| L3 | E17 | F16 | | yellow | Connect NAND |
| L4 | J17 | Y17(GND) | | black | GND NAND |
| R8 | E14 | B15 | | 10 kΩ | NAND I/P |
| R9 | F14 | I15 | | 10 kΩ | NAND I/P |
| R10 | W16 | A16 | | 10kΩ | NAND to 6V |
| BC639(1) | D17 | D16 | D15 | | |
| BC639(2) | G17 | G16 | G15 | | |
| TIMER | | | | | |
| BC639(3) | F17 | E18 | D19 | | |
| R11 | B18 | E20 | | 27Ω | discharge |
| R12 | W20 | A20 | | 33kΩ | charge |
| R13 | C16 | A19 | | 10kΩ | NAND to timer |
| C1 | B20 | X19 | | 100uF | |
| LATCH | | | | | |
| L5 | H18 | G11 | | pink | |
| diode(1) | I13 | H11 | | | positive feedback |
| diode(2) | D20 | F18 | | | timer to latch |
| R14 | J11 | Y11(GND) | | 100kΩ | |
| R15 | J12 | W13(GND) | | 5.1kΩ | P. divider |
| R16 | I12 | Z13(6V) | | 5.1kΩ | P. divider |

| RIGHT MOTOR CONTROL (STAGE 1) | | | | | |
|---|---|---|---|---|---|
| L6 | X1 | A1 | | black | |
| L7 | B1 | MRA | | brown | |
| L8 | B2 | MRB | | orange | |
| diode(3) | C1 | A2 | | | |
| BC639(4) | E2 | E3 | E4 | | stage 1 |
| R17 | W3 | A3 | | 56Ω | |
| R18 | A4 | C7 | | 1kΩ | |
| LEFT MOTOR CONTROL (STAGE 1) | | | | | |
| L9 | J2 | Y2 | | black | |
| L10 | I2 | MLA | | brown | |
| L11 | G3 | MLB | | orange | |
| diode(4) | H2 | F3 | | | |
| BC639(5) | I3 | I4 | I5 | | stage 1 |
| R19 | J4 | Z4 | | 56Ω | |
| R20 | J5 | H7 | | 1kΩ | |
| LEFT MOTOR CONTROL (END STAGE 1) | | | | | |
| BC639(7) | F2 | F5 | D5 | | stop BJT |
| R24 | E5 | F6 | | 1kΩ | |
| L13 | G6 | G13 | | pink | latch o/p to stop BJT |
| RIGHT MOTOR CONTROL (START STAGE 3) | | | | | |
| L17 | A12 | X12 | | black | |
| L18 | C8 | C22 | | white | V- to BJT |
| L19 | F24 | E24 | | blue | latch o/p to R31 |
| R31 | C23 | D24 | | 1kΩ | |
| BC639(11) | B21 | B22 | B23 | | |
| BATTERIES AND SWITCH | | | | | |
| L20 | W29 | BR+ | | red | |
| L21 | A29 | BR- | | black | |
| L22 | X29 | Y29 | | black | |
| L23 | W28 | Z28 | | red | |
| L24 | J29 | BL+ | | red | |
| L25 | Y28 | BL- | | black | |
| Switch | E29 | F29 | | | Starts the EEBug |
| LEFT MOTOR CONTROL (START STAGE 3) | | | | | |
| L14 | H13 | I24 | | blue | to R25 |
| R25 | H24 | F27 | | 1kΩ | to NOT BJT |
| BC639(8) | I28 | I26 | G27 | | NOT BJT |
| L15 | J28 | Y27 | | black | |
| R26 | J26 | Z27 | | 1kΩ | to 6V |

| | | | | | |
|---|---|---|---|---|---|
| BC639(9) | G23 | F25 | F26 | | charging BJT |
| R27 | J25 | Z26 | | 1kΩ | to 6V |
| R28 | H22 | H23 | | 1kΩ | to BC517 |
| C2 | I23 | Y22 | | 100uF | |
| R29 | J23 | Y23 | | 120kΩ | |
| BC517(1) | Z21 | J22 | J20 | | |
| BC639(10) | I21 | I20 | I19 | | ON stage 3 |
| R30 | J13 | J19 | | 1kΩ | latch to ON stage 3 BJT |
| L16 | G21 | H3 | | white | |
| RIGHT MOTOR CONTROL (END STAGE 3) | | | | | |
| BC639(6) | D1 | C4 | C6 | | stop BJT |
| R21 | D6 | C13 | | 1kΩ | OpAmp o/p to stop BJT |
| R22 | X11 | A11 | | 10kΩ | P. divider |
| R23 | W11 | B11 | | 51kΩ | P. divider |
| L12 | C12 | F23 | | pink | $V_-$ to $V_{cap}$ |

*Table 8: Breadboard connections of prototype EEBug*

## 6.2 Test Procedure

The following considerations were taken to ensure the bug fulfils its required tasks and to circumvent real effects.

### 6.2.1 Stage 1

The EEBug must detect and follow the line.

#### *6.2.1.1 Phototransistor SFH 300*

A phototransistor has a linear relationship between light intensity and current as it produces a leakage current directly proportional to the intensity of light. As light intensity increases, the voltage across the 10kΩ increases linearly. Hence, threshold voltage is set between the two voltage values obtained when the EEbug senses white and black surfaces respectively.

#### *6.2.1.2 Placement of LED and SFH 300*

To reduce the interference from ambient light, the LED and phototransistors were soldered onto a Stripboard beside one another. It was experimentally verified that the radiation pattern of the LED and phototransistors were large enough for detection. The Stripboard was then mounted on the front of the EEBug using screws and nuts. The height of the LED and phototransistors from the surface was experimentally determined to be at 0.5cm. At this optimum height, there would be a greatest change in phototransistor voltage based on the colour of the surface detected.

#### *6.2.1.3 Use of Potentiometer*

A potentiometer was used to vary the reference voltage during testing as values of voltages varied as the relative positions of the LEDs and phototransistors changed during initial testing stages.

#### *6.2.1.4 Determining of Resistor R17 and R19 values*

These resistors control the speed of the motors. For reasons mentioned earlier and through experimental testing, a 56Ω resistor was used.

#### *6.2.1.5 Determining of Resistor R18 and R20 values*

As the comparator Op-Amp MCP6004 has very low output current, it must be verified that it is sufficient to trigger the BJT. From the datasheet, the MCP6004 has an output short circuit current of approximately 30mA, which is sufficient to trigger the NPN BC639 transistor. By limiting the current to 5.3mA, a 1kΩ resistor is required.

$$R = \frac{6 - 0.7}{5.3x10^{-3}} = 1k\Omega$$

### 6.2.2 Stage 2

The EEBug must be able to travel 20cm once the line has ended.

#### *6.2.2.1 Value for R13*

The NAND gate must be able to turn the BC639 (3) ON when its output is HIGH and OFF when its output is LOW.

However, if R13 is too low, it would draw leakage current from the NAND gate when its output is LOW and turn BC639 (3) ON. This is undesirable and hence R13 must be large enough to prevent this. R13 is chosen to be 10kΩ.

#### *6.2.2.2 Values for RC timer circuit*

As the amount of time the EEBug takes to travel 20cm was around 1-2 seconds, the RC timer circuit must take 1-2 seconds to charge to the threshold voltage of the latch op-amp. The values R12 and C1 were determined experimentally to be 33kΩ and 100uF respectively.

R11 is chosen to be 27Ω as it controls the time the capacitor takes to discharge, resulting in an immediate discharge of the timer.

#### *6.2.2.3 Use of Potentiometer*

Similar to Stage 1, a potentiometer was used to vary the threshold voltage of the latch module during testing.

### 6.2.3 Stage 3

The EEBug must be able to travel in a spiral of decreasing radius, making at least one turn before coming to a stop.

#### *6.2.3.1 Op-amp output current*

As the latch output is connected to 4 BC639s and must supply enough current to activate them, the resistor values R24, R25, R30 and R31 must be large enough to draw enough current from the latch op-amp. However, this cannot exceed the output short circuit current of the op-amp 30mA. Using the same reasoning in Stage 1, 1kΩ resistors are used, drawing a total of 20mA, well below the output short circuit current.

#### *6.2.3.2 Values for RC timer circuit*

R26 and R27 determine the end value to which C2 is able to charge up as there is a voltage drop across R26 and R27. For example, with R26 and R27 at 10kΩ, C2 is only able to charge up to 2V. Thus, R26 and R27 were chosen to be low at 1kΩ, allowing C2 to charge to 5.4V.

The time the left motor takes to decrease to zero determines the spiral movement. This in turn is determined by the RC timer circuit comprising of R29 and C2. If R29 and C2 are too small, the EEBug would not be able to complete at least one spiral of decreasing radius. Thus, R29 and C2 were

chosen to be 120kΩ and 100uF respectively to ensure that the voltage and speed of the left motor decrease over a longer duration, sufficient for the EEBug to make one full turn.

#### *6.2.3.3 Latch*

During testing, MC33078 op-amps were used. However, this resulted in an output of 1.4V on black surfaces. This is due to the assumption that the op-amp would reach supply rail values of 0 and 6V. In reality, normal op-amps have constraints on the output voltage swing.

This was solved through a rail-to-rail op-amp, MCP6004, where output voltages are closer to supply rail values.

#### *6.2.3.4 Stop*

Since the bug has to come to a complete stop after completing a full turn of decreasing radius, a potentiometer was used to vary the threshold voltage of the stop module during testing. This provides control over the number of spirals it can perform and hence when the EEBug will stop.

### 6.2.4 Conclusion

Through testing, the group was able to come up with exact values for components that will allow the EEBug to fulfil its design task. Individuals will be able to build their EEBug and by following the breadboard configuration and adjust the performance through the test procedures detailed above.

# 7 BUDGETING AND COSTING

Table 9 summarises the group's budget on the abovementioned enhancements. Appendix 6 details the component table the group used to decide which components were required to be bought. Refer to Appendix 7 for the Component Order Form.

| Supplier | Product Ref | Production Description | Quantity | Price | Subtotal | Order Date |
|---|---|---|---|---|---|---|
| RS | 403-181 | Microchip MCP6004-I/P Quad Operational A | 2 | £0.32 | £0.64 | 09/03/15 15:13 |
| EEDStores | VB0030 | Stripboard small 25mmX64mm | 2 | £0.3 | £0.6 | 06/03/15 14:20 |
| OneCall | 2290441 | Kingbright[1] L-53F3C IR, Emitter, 940NM | 6 | £0.09 | £0.54 | 05/03/15 17:56 |
| OneCall | 2290444 | Kingbright L-53P3C Phototransistor, 5M | 6 | £0.09 | £0.56 | 05/03/15 17:54 |
| **Total** | | | | | **£2.34** | |

*Table 9: Costing Sheet*

[1] While IR LEDs were obtained, it was subsequently decided that visible light LEDs had the required performance parameters. This is due to the need for a 1MΩ resistor when utilising IR LEDs and the fact that the voltage range of IR LEDs is less than that of visible light LEDs.

# 8 SUPERBUG

As an analogue method was adopted, it is relatively difficult to design additional enhancements for a SuperBug due to space constraints and less flexibility compared to a microprocessor. Nonetheless, a few enhancements have been attempted.

## 8.1 SPIRAL SETTING

As the number of spirals executed is dependent on the threshold voltage of the stop op-amp as elaborated earlier, this threshold voltage can be varied with a potentiometer. By marking the appropriate threshold voltages the left motor would reach at each spiral, the number of spirals done can be easily adjusted from 1 – 3 rounds. The higher the threshold voltage, the earlier the EEBug would stop.

Finally, the voltage varying control has to be extended to ensure that the Left motor does not stop before it can complete the maximum amount of spirals, three by increasing the time constant of the timer circuit.

## 8.2 REMOTE START

A remote starting mechanism has also been planned where the transmitter circuit is built on a separate solder board and only a receiver is required on the Superbug. Details of its implementation is in Appendix 4.

# 9 REFERENCES


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8. Rubasinghe A. Use an op amp as a set/reset flip-flop. [Online].; 2012 [cited 2015 March 17. Available from: http://www.edn.com/design/other/4373768/Use-an-op-amp-as-a-set-reset-flip-flop.

# APPENDIX 1. MEETING MINUTES

## MEETING 3

Author CHUNG POON

**ATTENDANCE**

Present: Ben, Chung, Sam, Savvas, Nicolas

Absence: Barry, Elliot

**CONTENT**

Ben: Chung is to organise the bookings. Wednesday 10am every week

Ben: Well done for getting an A. We are on track.

The report structure is split up as indicated on the template.

High level design is more in depth technically than the 1st report

Savvas: Speak to papa about absences

Ben: Plan of action – to the pairs (Sam &) Elliot/ (Chung &) Barry: in regard to their lack of cooperation, Ben shall manage Barry and Elliot; sub group should meet separately

Design Brief: follow the formatting requirement set out in the template docs
We are still following our plan on using passive components.

Sam: We will use PSPICE to test our low level final designs.

Ben: Compile part list after simulation. Follow template format to help Savvas and Elliot.
Savvas has to type out an excel sheet on all parts needed. Some parts can be obtained from the labs for free.

Nicolas: We will order from BATMAN and the online catalogue to order parts. Savvas shall familiarise self with the ordering system.

Ben: **Results of simulation:** summarise your simulation results to help integration of reports.
There are 2 weeks to get to the low level design simulation stage. For the next 6 weeks, work on go on for the sub circuit design, before the group integration.

Nicolas: We should use less timer, and combine the circuits timing.

Sam: Using passive components there is a lot of flexibility. For example, an inter-sub-circuit clock and using capacitor to time.

**ACTIONS NEEDED:**

URGENT Due Monday 2/2/2015: submit high level design

**Next meeting FRIDAY 1400 -1500 at room 210 in library for TECHNICAL brainstorming and Wednesday 10am**

Report to Ben every weekend. There are 2 weeks to drill down on the low level design.

Specific roles

1. Secretary – Start building up the report

2. Assistant Secretary – Book meeting rooms every Wednesday 1000 to 1100 and Friday 1200 to 1400
3. Treasurer and Counter Signatory – Familiarise yourselves with the BATMAN app for buying components and create an excel sheet of possible components and costs

Low Level Design Feb 27: Simulation results and design report

6 March: Group Integration finalisation

FINAL SUBMISSION DATE: 12 MARCH so time is freed for other coursework of other modules

Date: 2015 Jan 30
Author: Chung Poon

# MEETING 4

**ATTENDANCE**

Present: Ben, Chung, Savvas, Sam, Elliot, Barry, Nicolas

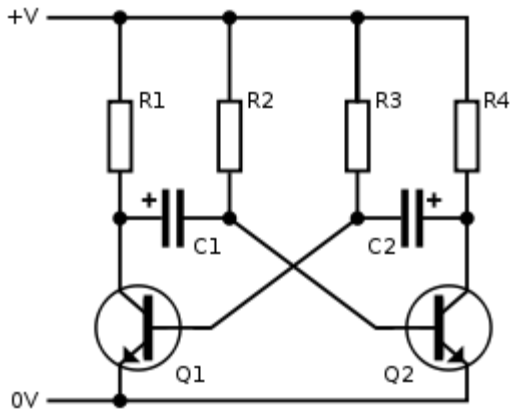
**MINUTES**

Ben: Introduced management issues and key dates to Barry and Elliot

Sam: We need technical discussion for the Bug's circuit

Sam: A clock could be used for timing centrally instead of using different timing circuits for each parts, and have all parts synchronised to one clock signal.

I know of 2 ways to achieve this, using a 555 timer, in astable, but has many limitations, such as not being to get a square wave. Another way is to use a "Bipolar Multi-vibrator"




This is a much elegant solution, as cheaper and easier to replace, as well as being to generate a square wave.

This clock pulse will always be on, like a heartbeat.

Savvas: Do we not need to disable it for a specific part when part of circuit is not in use?

Sam: That should be done on the part's side.

Now that we have a clock output, we can use it to process input and output.

At high-level, the detection phase reacts to the 2 measurements each side of the Bug.

This could be achieved be using an OpAmp to amplify the light intensity as a digital way so that a threshold is set, with a Schmitt trigger for when motor are switched on/off to change direction.

Chung: Or use transistors to control the speed of motors based on the light intensity directly like we did with the original EEBug.

Nicolas: So how do we make sure that the gap and end of line is accounted for? How do we use the clock signal.

Sam: We could use it to charge up a capacitor, then the voltage through a comparator to change the direction. Digital circuit may be more resistance to noise.

Chung: Beware of the limitation of space for digital circuits.

Sam: We try the digital circuit first. We will cover all possibilities.

# MEETING 5

Date 2015 February 20
Author Chung POON

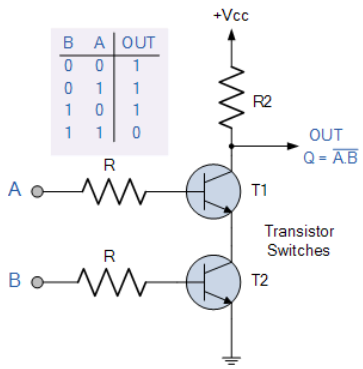
### ATTENDANCE

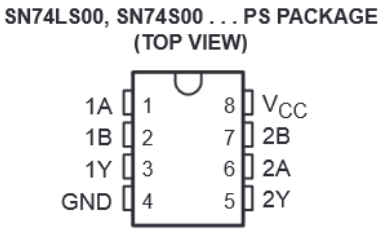
Present: all but Barry

### AGENDA

The previous timer circuit will not work, since the bias will not output a suitable logic voltage.

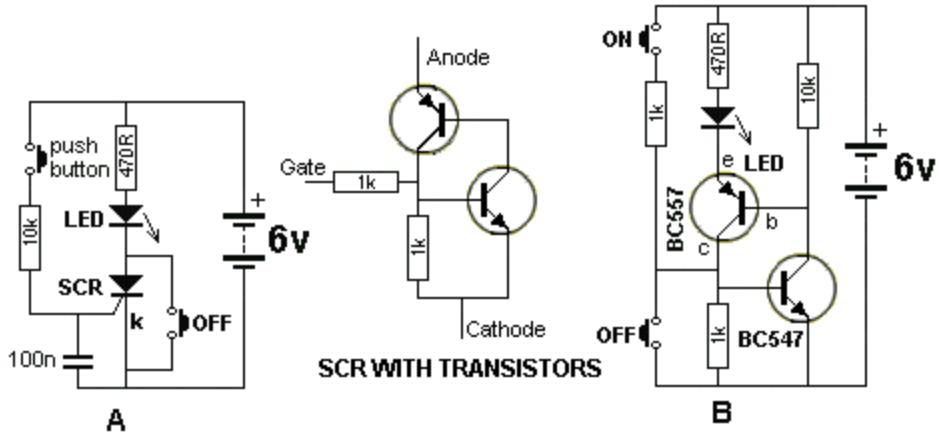
New CCT devised



Should we buy a NAND gate on an IC package? IC package saves time, but uses up space as the extra unused NAND gate. The NAND gate built from transistors may be more flexible.

The latch is viable, cct shown.



# APPENDIX 2 – CALENDAR AND TIMELINE

| | | | | | | |
|---|---|---|---|---|---|---|
| 25 | 26 | 27 | 28<br>Meeting 1 | 29 | 30 | 31 |

**January**

**February**

| Sunday | Monday | Tuesday | Wednesday | Thursday | Friday | Saturday |
|---|---|---|---|---|---|---|
| 1 | 2<br>Submission of High Level Design | 3 | 4<br>Meeting 2 (Discussion of low level designs) | 5 | 6<br>Treasurers to procure components | 7 |
| 8 | 9<br>-Preliminary Submission of Low Level Design<br>-***Subgroup Lab Simulations*** | 10 | 11<br>Meeting 3<br>***Subgroup Low Level Design Lab Simulation*** | 12<br>***Subgroup Low Level Design Lab Simulation*** | 13 | 14 |
| 15 | 16 | 17 | 18<br>***Subgroup Low Level Lab Simulation*** | 19 | 20<br>Meeting 4<br>**Start of Group Integration (Lab)** | 21 |
| 22 | 23 | 24 | 25<br>***Group Integration*** | 26 | 27<br>Submission of Low | 28 |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | ***(Lab)*** | | Level Design Template | |

## March

| Sunday | Monday | Tuesday | Wednesday | Thursday | Friday | Saturday |
|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 **Group Integration (Lab)** | 5 | 6 **Group Integration Report** | 7 |
| 8 | 9 Meeting with Tutor | 10 | 11 **Group Integration (Lab)** | 12 | 13 **Submission of ALL parts for compiling (if not already done so)** | 14 |
| 15 | 16 **Last minute Submissions** | 17 | 18 | 19 | 20 Meeting 5 | 21 |
| 22 | 23 | 24 | 25 | 26 | 27 **(Final Submission)** | 28 (Start of Easter Break) |

# APPENDIX 3 – METHOD OF APPROACH

Table 10 below details the various advantages and disadvantages listed for the two different methods.

| Method | Advantages | Disadvantages |
|---|---|---|
| **Analogue** | 1. Resistant to noise<br>2. Greater flexibility<br>3. Lower cost<br>4. Greater potential for learning<br>5. Greater team engagement | 1. Numerous parameters to account for<br>2. Complicated testing |
| **Microcontroller** | 1. Programming of the bug will be simple<br>2. Few parameters required | 1. Greatly affected by circuit noise<br>2. High cost |

*Table 10: Analogue vs Microcontroller*

# APPENDIX 4 – REMOTE STARTING OF EEBUG

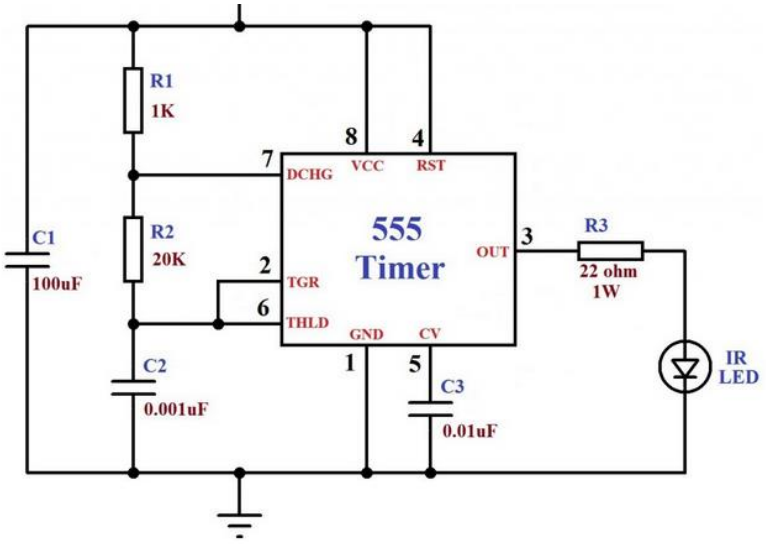



*Figure 1: Transmitter Circuit*

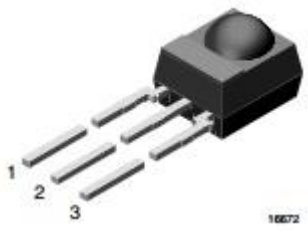



*Figure 2: Receiver*

Description:

As there is limited space on the original EEBug, this enhancement requires only a receiver on the original circuit while the bulk of the additional components are on a separate transmitter circuit.

The transmitter produces a 38 KHz infrared wave of wavelength 940 nm which is received by the receiver. The output from the receiver is active low. Thus, it will produce high output the signal link is broken, triggering the bug to start via a simple BJT switch.

Components Required:

1. TSOP 4828 IR Receiver 38Khz: £0.552 (with 950nm wavelength)
2. TLC555Cp IC, Timer CMOS DIP8 : Cost £0.676
3. Emitter: Already procured (at 940 nm Wavelength)
4. R20KΩ
5. R1KΩ
6. 100uF
7. 0.001uf
8. 0.01uf
9. R 22Ω

Theory of Operation:

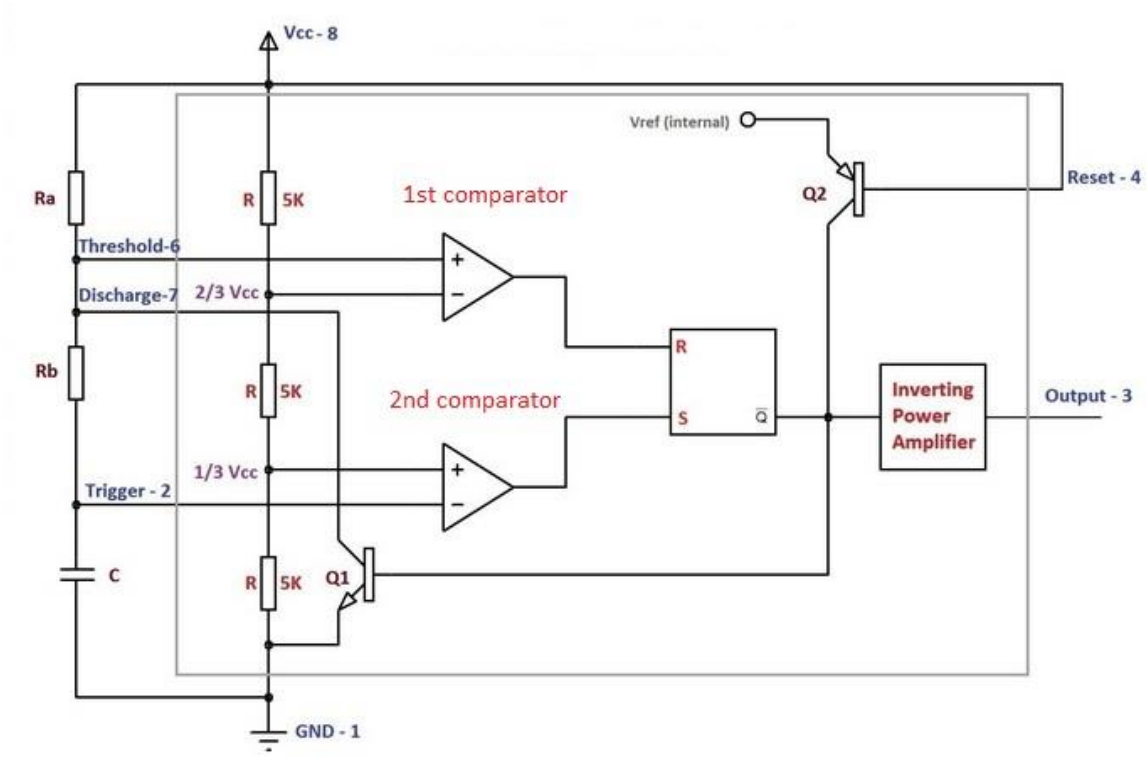



Figure 3: Inside the 555 Timer

1. The two resistors Ra and Rb are responsible for charging capacitor. At the start because voltage of capacitor is below 1/3 of the voltage source the output of the second comparator will be high while the first will be low giving a low output at the flip flop.
2. When the capacitor charges between the 1/3 and the 2/3 of the voltage source both comparators will give a low output giving a low output at the output of the flip flop.
3. There will be a time where the capacitor reaches a voltage of slightly above 2/3 of voltage source giving a high output on the first comparator and high at the output of the flip flop.
4. This will activate the discharging transistor and capacitor discharges by the Rb resistor. When it becomes less than 2/3 of voltage source the output of the two comparators becomes low while flip flop's output remains high.
5. As soon as the capacitor voltage becomes below 1/3 of voltage source the first comparator becomes low and the second becomes high giving a low output at the flip flop and charging process begins again.
6. The whole procedure produces a rectangular wave at the output. The frequency produced is used to turn on and of the IR LED producing the 38KHz waveform needed.

# APPENDIX 5 – PICTURE OF EEBUG

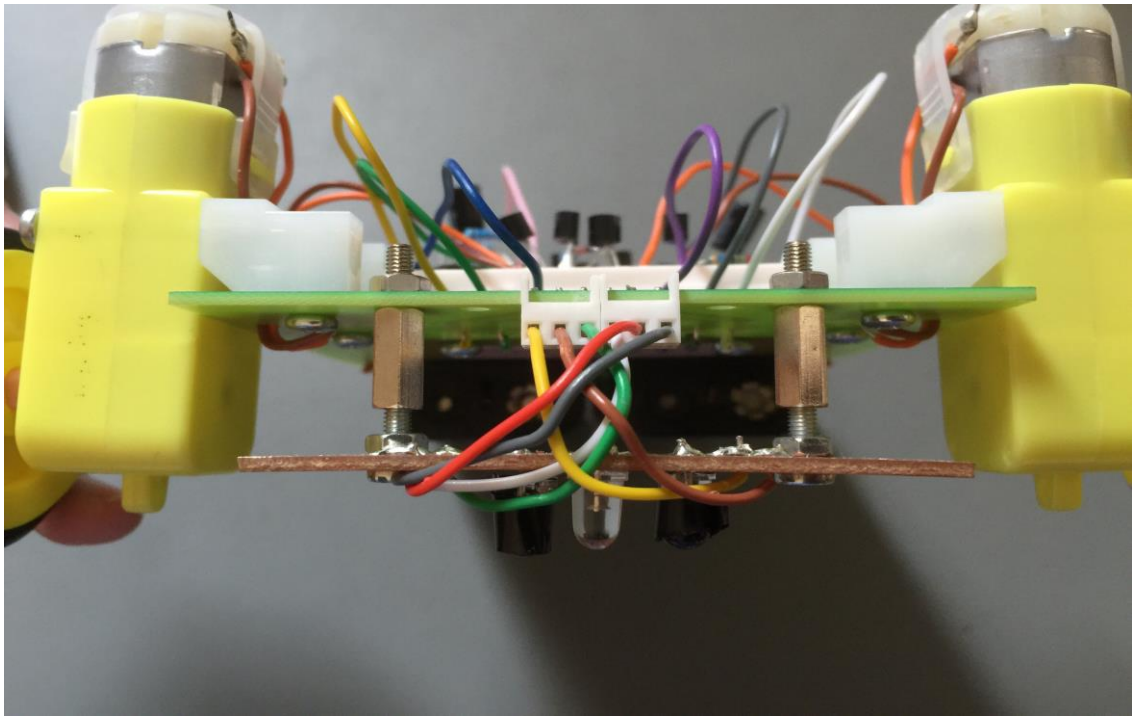


*Figure 4: EEBug Front View*

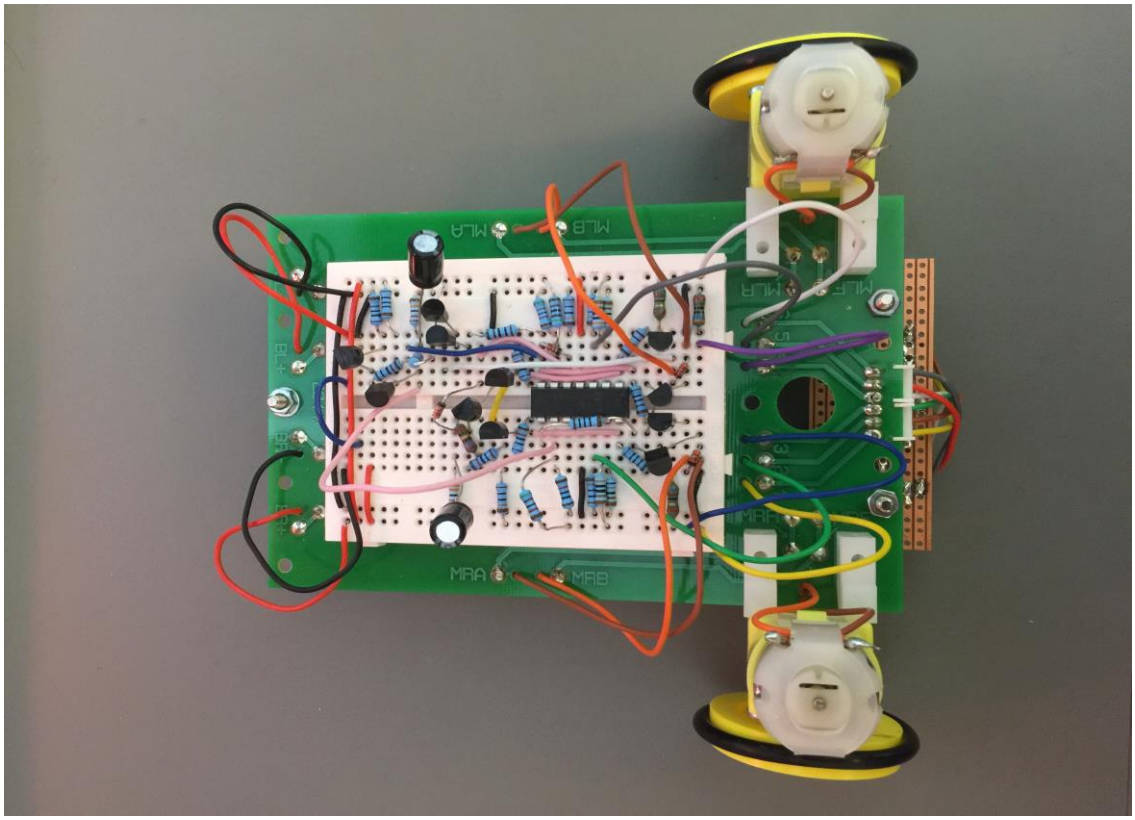



*Figure 5: EEBug Top View*

# APPENDIX 6 – LIST OF LAB COMPONENTS

## Resistors (Ohms)

| | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1.1 | 1.2 | 1.3 | 1.5 | 1.6 | 1.8 | 2 | 2.2 | 2.4 | 2.7 | 3 | 3.3 | 3.6 | 3.9 | 4.3 | 4.7 | 5.1 | 5.6 | 6.2 | 6.8 | 7.5 | 8.2 | 9.1 |
| 10 | 11 | 12 | 13 | 15 | 16 | 18 | 20 | 22 | 24 | 27 | 30 | 33 | 36 | 39 | 43 | 47 | 51 | 56 | 62 | 68 | 75 | 82 | 91 |
| 100 | 110 | 120 | 130 | 150 | 160 | 180 | 200 | 220 | 240 | 270 | 300 | 330 | 360 | 390 | 430 | 470 | 510 | 560 | 620 | 680 | 750 | 820 | 910 |
| 1K | 1.1K | 1.2K | 1.3K | 1.5K | 1.6K | 1.8K | 2K | 2.2K | 2.4K | 2.7K | 3K | 3.3K | 3.6K | 3.9K | 4.3K | 4.7K | 5.1K | 5.6K | 6.2K | 6.8K | 7.5K | 8.2K | 9.1K |
| 10K | 11K | 12K | 13K | 15K | 16K | 18K | 20K | 22K | 24K | 27K | 30K | 33K | 36K | 39K | 43K | 47K | 51K | 56K | 62K | 68K | 75K | 82K | 91K |
| 100K | 110K | 120K | 130K | 150K | 160K | 180K | 200K | 220K | 240K | 270K | 300K | 330K | 360K | 390K | 430K | 470K | 510K | 560K | 620K | 680K | 750K | 820K | 910K |
| 1M | 1.1M | 1.2M | 1.3M | 1.5M | 1.6M | 1.8M | 2M | 2.2M | 2.4M | 2.7M | 3M | 3.3M | 3.6M | 3.9M | 4.3M | 4.7M | 5.1M | 5.6M | 6.2M | 6.8M | 7.5M | 8.2M | 9.1M |
| 10M | | | | | | | | | | | | | | | | | | | | | | | |

## Capacitors

| Ceramic Disc | | | | | |
|---|---|---|---|---|---|
| 10pf | 15pf | 22pf | 33pf | 47pf | 68pf |
| 82pf | 100pf | 120pf | 150pf | 180pf | 220pf |
| 270pf | 330pf | 390pf | 470pf | 560pf | 820pf |
| 1nf | 2.2nf | 3.3nf | 3.9nf | 6.8nf | |

| Ceramic X7R | | |
|---|---|---|
| 1nf | 4.7nf | 10nf |
| 22nf | 33nf | 47nf |
| 68nf | 100nf | 220nf |
| 330nf | 680nf | |

| Polyester | | | | |
|---|---|---|---|---|
| 1nf | 1.2nf | 1.5nf | 2.2nf | 2.7nf |
| 4.7nf | 5.6nf | 6.8nf | 10nf | 15nf |
| 18nf | 22nf | 33nf | 47nf | 68nf |
| 100nf | 470nf | | | |

| Electrolytic | | | | |
|---|---|---|---|---|
| 0.47uf | 1uf | 2.2uf | 3.3uf | 4.7uf |
| 10uf | 22uf | 33uf | 47uf | 100uf |
| 220uf | 330uf | 470uf | | |

| Polystyrene | | | | |
|---|---|---|---|---|
| 18pf | 39pf | 680pf | 1.2nf | 3.3nf |

| Ceramaic V5V | |
|---|---|
| 470nf | 1uf |

| Tantalum | |
|---|---|
| 10uf | 15uf |

| Transistors |
|---|
| BC 107 |
| BC 108 |
| NPN BJT |
| NPN 2N3904 |
| HFe 250-300 |
| HFe 370 |

| DIODE |
|---|
| 1N4148 |
| 1N914 |
| Silicon Zener Diodes: |
| BZX79-C6V8 |
| BZX79 3V6 |

| OP-AMPS | | |
|---|---|---|
| 741 | LF411 | Dual opamps: |
| TLC072 | 71 | MC33078 |
| E121600N | | TL072 |

| IC SOCKETS |
|---|
| 16 DIL |
| 14 DIL |
| 8 DIL |
| 6 DIL |

| Tools |
|---|
| Adjustment |
| Track Cutter |
| Screw driver |
| Sodlering iron trip cleaner |
| Single-core wire to 4mm socket |
| Prototyping Boards |

| Other |
|---|
| LDR |
| BNCT style |
| Crocodile/Alligator |
| Ni plated steel chip |
| Double Sided Ahesive pad |
| Patch wire for PCB Rework |
| Terminal Test Pin (Blue/Red/White) |
| Terminal Vero Pin (single/double sided) |

# APPENDIX 7 – COMPONENT ORDER FORM

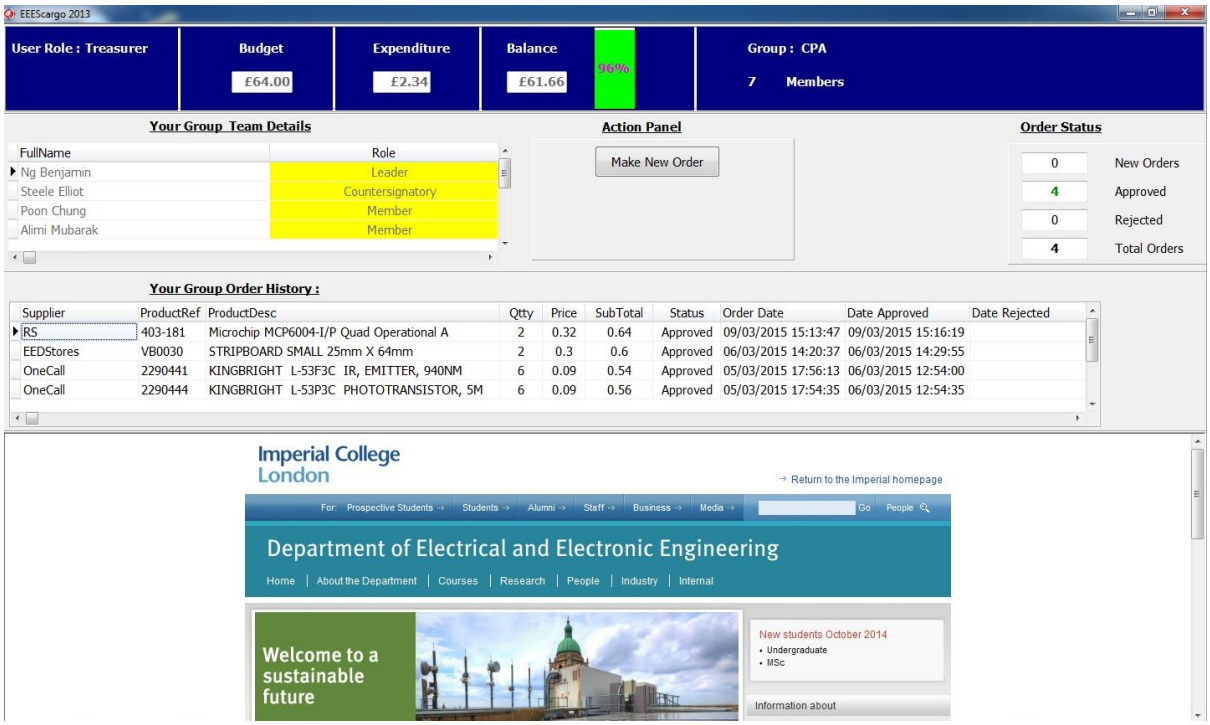



*Figure 6: Component Order Form*