

Intel® Edison Design Document This Intel® Edison design document is licensed by Intel under the terms of the Creative Commons Attribution Share-Alike License (ver. 3), subject to the following terms and conditions. The Intel® Edison design document IS PROVIDED "AS IS" AND "WITH ALL FAULTS." Intel DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED REGARDING THE EDISON DESIGN OR THIS EDISON DESIGN DOCUMENT INCLUDING, BUT NOT LIMITED TO, ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Intel® may make changes to the specifications, schematics and product descriptions at any time, without notice. The Customer must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel® reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. ENJOY!

- 1) TITLE PAGE
- 2) TABLE OF CONTENTS
- 3) POWER SUPPLIES
- 4) UART TO USB DEBUG PORT
- 5) SPI ADC AND SWIZZLER
- 6) ANALOG TRANSLATION
- 7) DIGITAL TRANSLATION
- 8) SD CARD
- 9) USB A AND B PORTS
- 10) BUTTON AND I/O CONNECTIONS
- 11) TEST POINTS

EDISON FOR ARDUINO* BOARD

Title
Table of Contents

Size Document Number Rev 5

Date: Tuesday, August 26, 2014 Sheet 2 of 11

5

3

















