

Processor

```
graph LR; Processor[Processor] --- L1[Level 1 Cache]; L1 --- L2[Level 2 Cache]; L2 --- L3[Level 3 Cache]; L3 --- MM[Main Memory]; MM --- STS[Secondary/Tertiary Storage];
```

The diagram illustrates a memory hierarchy. It starts with a 'Processor' box on the left. Inside the Processor box is a dashed rectangle labeled 'Level 1 Cache'. To the right of the Processor box is another dashed rectangle labeled 'Level 2 Cache'. To the right of the Level 2 Cache is a dashed rectangle labeled 'Level 3 Cache'. To the right of the Level 3 Cache is a dashed rectangle labeled 'Main Memory'. To the right of the Main Memory is a dashed rectangle labeled 'Secondary/Tertiary Storage'. All dashed rectangles are of increasing size from left to right, representing increasing memory capacity and distance from the processor.

Level 1  
Cache

Level 2  
Cache

Level 3  
Cache

Main  
Memory

Secondary/Tertiary  
Storage