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Assignment, Report & Laboratory Coversheet for Individual & Group Assignment

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SEE OVER FOR INFORMATION ON REFERENCING & PLAGIARISM

UWA ELEC5552

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Final Design Report
Volume 1

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Serena Joppich	22722165	Sensing and Protection – DC current measurement Ethical Issues Issues Identified During Design Process Safety Issues and Mitigations Design Outputs Recommendations: Protection Circuit
Myles Kelly	22722165	Final Requirements Software Architecture Final Design Element: Square Wave Modulation, DC Voltage Measurement Final Design: Construction/Assembly/Synthesis
Hannah Page	22498729	Executive Summary & Stakeholder Analysis Final Design Element: DC +AC Voltage Measurement, AC Current Measurement, Thermal Measurement, HMI Final Design: PCB
Vani Srivastava	22501707	Stakeholder Engagement Final Requirements Design Architecture – Hardware Final Design Element: AC Amplification Final Cost & Bill of Materials Top 5 Risks and Mitigations Recommendations: AC Amplification
Julia Taule	22388829	Report Structure Final Requirements Design Architecture – Block Diagram Final Design Element: DC Supply Recommendations: DC Supply Requirements Testing and Verification

1. Executive Summary

The project partner, the WA node of the Australian National Fabrication Facility (ANFF-WA), contributes to the research and development of micro electro-mechanical system (MEMS) devices. These devices require a variable power supply capable of producing high voltage, low current output for their testing and actuation. This project aimed to design and build such a power supply, with a physical first prototype presented in conjunction with this report.

As the capstone design report, this document will first review the stakeholder analysis and management that occurred throughout the project. The finalised requirements are then collated prior to a discussion of the overarching design architecture and philosophy. After identifying the key requirements and associated design modules, the individual design elements are discussed in detail, including any testing performed. Within the design section, the final PCB, overall system cost, construction methods, risks and safety issues are presented. This section also includes details of the final design outputs and where they are stored. Lastly, an extended discussion of recommendations for further works and prototypes is included, prior to concluding remarks.

The stakeholder engagement throughout the semester shaped the final requirements. Discussions with the group facilitator were instrumental to the final design. The overarching design has been divided into smaller modules and subcircuits, including the DC supply and modulation, the AC supply and modulation, measurement and protection, and lastly the user interface.

Some key requirements regarding the enclosure safety, voltage fidelity and tuneable current limit were not achieved due to time and budget constraints. Requirement validation was performed through the testing of individual circuits. The outcomes of these tests are included both within the main body of the report and the appendices. Whilst much prototyping and testing occurred as a part of the design process, further testing is still required. This is largely due to the construction issues that arose due to the inability to have a PCB made within the required timeframe.

One key recommendation for this project is to move the current prototype onto a custom PCB, as opposed to pre-produced protoboards. This will greatly reduce the construction complexity and issues associated with soldering the surface-mount components to the board. This would also enable the construction of the preferred design, which incorporates circuitry that delivers the necessary variable current limit and high voltage AC output, resulting in the fulfilment of more requirements.

This design meets many of the necessary requirements, and most of the design shortcomings can be attributed to design modifications made due to time constraints. Future design iterations will not be constrained by this, and with a professionally produced PCB as discussed in the tenders section, it is expected that this design will meet all the requirements.

Table of Contents

1. Executive Summary 5

1. Introduction 9
   - 1.3 Background and Purpose of the Project 9
   - 1.4 Scope of Report 9
   - 1.5 Report Structure 9
   - 1.6 Abbreviations 10

2. Stakeholder Engagement 12

3. Final Requirements 15
   - 3.3 Selection and Prioritisation Methodology 15
   - 3.4 Final Requirements 16
   - 3.5 Constraints 23

4. Design Architecture 25
   - 4.3 Hardware Architecture 25
   - 4.4 Software Architecture 26

5. Final Design Elements and Tests 27
   - 5.3 DC Supply 27
   - 5.4 Square Wave Modulation 31
   - 5.5 AC Supply 34
   - 5.6 Measurement 43
   - *5.7* Protection 51
   - 5.8 Human Machine Interface (HMI) 53

6. Final Design 55
   - 6.3 Final Cost 57
   - 6.4 Construction/Assembly/Synthesis 57
   - 6.5 Safety Issues and Mitigations 60
   - 6.6 Ethical Issues 63
   - 6.7 Issues Identified During Design Process 63
   - 6.8 Top 5 Risks and Mitigations 63
   - 6.9 Design Outputs 64
   - 6.10 Recommendations for Further Development 66
   - 6.11 Community Briefing 67
   - 6.12 Tenders 67

7. References 69

8. Appendices 72

8.1 Appendix A: Schematic and PCB layout 72
Overarching Schematic 73
Power Input 74
Microcontroller 75
AC Circuitry 76
DC Measurement & Modulation 77
Relay Control 78
8.2 Appendix B: Next Iteration Design Schematics and Simulations 79
8.3 Appendix C: Requirements Verification and Validation 83

List of Figures

Figure 1: Stakeholder analysis matrix. 14
Figure 2: Simplified block diagram of power supply design. 25
Figure 3: Software flow diagram. 26
Figure 4: DC circuit block diagram. 27
Figure 5: LV DC module voltage output before filtering (left) and after filtering (right). 28
Figure 6: MVDC module output voltage. 28
Figure 7: Dual 5VDC supply simulation. 29
Figure 8: Dual 5VDC supply output with 22V input. 29
Figure 9: Component voltage generation schematic (left) and simulation (right). 30
Figure 10: Typical connection diagram for the IRS2011PBF [4]. 32
Figure 11: Breadboarded MOSFET modulation circuit. 33
Figure 12: Power vs. Frequency, $fMCLK = 25\ MHz,\ fout = 60kHz\ left, fout = 600kHz\ right,$ adapted from [6]. 35
Figure 13: Arduino code used to modify frequency parameter. 35
Figure 14: Waveform for $fout$=300kHz, without capacitors (left) and with capacitors (right). 35
Figure 15: Noise performance of LT1818, extracted from [3]. 36
Figure 16: AC amplification with gain = 0.190, f=300kHz. 36
Figure 17: Dynamic increment implementation for inverter gain. 37
Figure 18: Waveform generation and low voltage AC breadboard. 37
Figure 19: Example of first order low pass filter and associated waveform. 38
Figure 20: Waveform of low voltage AC generation. 38
Figure 21: AC modulation switching process. 39
Figure 22: Circuit for bridge configuration of PA79 op-amp. 42
Figure 23: 0.5V input and ±5V supply at 50kHz (left) and 300kHz (right). 42
Figure 24: 5V input and ±125V supply at 50kHz (left) and 300kHz (right). 42
Figure 25: 5V input and ±175V supply at 50kHz (left) and 300kHz (right). 43
Figure 26: Oscilloscope reading for 0.5V input. 43
Figure 27: Voltage divider circuit [15]. 44
Figure 28: Voltage divider circuit for each of the DC module voltage measurements. 45
Figure 29: DC current measurement circuit (default 10mA output current limit). 46
Figure 30: DC current measurement circuit simulation (10mA load current). 47
Figure 31: DC current measurement circuit simulation (8mA load current). 47
Figure 32: DC current measurement circuit simulation (12mA load current). 47

Figure 33: Model of AC voltage measurement (left) and simulation output (right). 48
Figure 34: AC current measurement system model (left) and simulation (right). 49
Figure 35: Thermal measurement circuit (left) and code (right). 50
Figure 36: Simplified DC current measurement circuit. 50
Figure 37: Code output of DC current measurement circuit. 51
Figure 38: NPN relay switch circuit [14]. 52
Figure 39: Left: CAD model of initial case design. Right: Prototype metal case prior to final assembly. 53
Figure 40: Designed HMI with user inputs and outputs. 54
Figure 41: I/O block of the system. 54
Figure 42: Flow diagram for LCD menu screen. 54
Figure 43: Schematic of entire power supply unit. 55
Figure 44: PCB layout of entire power supply. 56
Figure 45: Protoboard of the DC modulation and measurement circuits. 58
Figure 46: Protoboard of the power selection and safety circuits. 58
Figure 47: Protoboard of AC amplification circuit, featuring the PA79 op-amp. 59
Figure 48: Breadboard testing of an op-amp with trace leads soldered on for testing. 59
Figure 49: PA85 schematic (left) and AC wave at f=300kHz. 66
Figure 50: Suggested PCB layout for -125V supply [22]. 79
Figure 51: -175V Supply circuit and simulation. 80
Figure 52: +175V Supply circuit and simulation. 81
Figure 53: DC current measurement and protection circuit for 10mA output current limit – 2mA load current. 82
Figure 54: DC current measurement and protection circuit for 10mA output current limit – 12mA load current. 82

List of Tables

Table 1: Abbreviations used in this report. 10
Table 2: Stakeholder identification, including justification and executed engagement. 12
Table 3: Requirement priority categories. 15
Table 4:Cost summary of design as per different modules. 57
Table 5: Top 5 hazards and mitigation strategies. 61
Table 6: Top 5 risks and mitigations. 63
Table 7: Design output files. 65

1. Introduction

1.3 Background and Purpose of the Project

The project partner for the ELEC5552 project, "MEMS testing power supply" is the WA Node of the Australian National Fabrication Facility (ANFF-WA). This facility supports the development and research of semiconductor devices, in particular micro electro-mechanical systems (MEMS). MEMS are such small-scale devices that they may be actuated utilising high voltage electrostatic charge. To achieve this electrostatic actuation, a variable power supply capable of producing a range of high voltage signals with low output current is required.

1.4 Scope of Report

This report will cover the entire ELEC5552 design process and resulting design. This includes a review of the stakeholder analysis, management and the finalised requirements. Each of the main modules will be discussed with respect to their associated requirements, design decisions and testing. The alternative design components will be briefly described, however in-depth discussion and calculation is outside the scope of this report.

There will be an additional operating and maintenance manual included in the design deliverables but excluded from the scope of this report.

1.5 Report Structure

This report starts with an introduction of the project stakeholders and their involvement in the project. The final requirements are then presented, along with any changes from the original developed requirements, followed by the overall design architecture developed to meet these requirements. Following this, the design components are described in further detail to explain how the requirements are met, along with the testing conducted to verify this. Reasoning for why certain requirements were not met or only partially fulfilled is presented. The final design and the associated cost are then presented, followed by safety, ethical and process related issues. Lastly, the report presents recommendations for future iterations, further development, and relevant tenders.

1.6 Abbreviations

Table 1 shows the abbreviations used in this report.

Table 1: Abbreviations used in this report.

Abbreviation	Description
AC	Alternating Current
AD	Administrative
ANFF-WA	WA node of the Australian National Fabrication Facility
BoM	Bill of Materials
CAD	Computer Aided Design
DC	Direct Current
EL	Elimination
ELV	Extra Low Voltage
EN	Engineering
ERAC	Electrical Regulatory Authorities Council
GBW	Gain Bandwidth
GD	Guarding
HMI	Human Machine Interface
HV	High Voltage
IC	Integrated Circuit
IN	Inspection
I/O	Input/Output
IS	Isolation
I2C	Inter-Integrated Circuit
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LMS	Learning Management System
LV	Low Voltage
MEMS	Micro Electro-Mechanical System
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MV	Medium Voltage

N-FET	N-channel Field-Effect Transistor
NPN	Negative Positive Negative
NTC	Negative Temperature Coefficient
OHL	Open Hardware License
Op-Amp	Operational Amplifier
PCB	Printed Circuit Board
P-FET	P-channel Field-Effect Transistor
PPE	Personal Protective Equipment
PPIR	Professional Performance, Innovation and Risk
PSU	Power Supply Unit
RoHS	Restriction of Hazardous Substances
RMS	Root Mean Square
SPDT	Single Pole Double Throw
SPI	Serial Peripheral Interface
SU	Substitution
SWOT	Strengths, Weaknesses, Opportunities and Threats
TQ	Technical Query
TR	Training
UWA	University of Western Australia
ZVS	Zero Voltage Switching

2. Stakeholder Engagement

Stakeholders are defined as parties that can materially affect the project's outcome and may or may not benefit from the project. These include both stakeholders who contribute and who are impacted by the project output [1].

Stakeholder identification was performed through the PPIR (Professional Performance, Innovation and Risk) process, brainstorming and investigation of the project documentation. They have been outlined in Table 2, along with their roles and responsibilities with respect to the project and rationale for their recognition as stakeholders. The engagement undertaken throughout the project is also outlined for each stakeholder.

Table 2: Stakeholder identification, including justification and executed engagement.

Stakeholder	Role and Responsibility	Executed Engagement
Design team	The design team will be responsible for all design and development decisions and is highly engaged due to the assessment of the project. The team aims to gain practical engineering experience and contribute to a successful project outcome.	Weekly meetings and shared drive for files. Teams channel and messaging for urgent matters. Clear task delegation. Skill development opportunities.
Dilusha Silva	As unit coordinator, Dilusha will provide guidance, access to testing and construction equipment and feedback. Additionally, he is acting as a project partner representative and as such is highly invested in the project outcome.	Weekly technical queries (TQ's) and information sessions. Communication via emails and meetings as required. Assessments submitted through LMS.
Michal Zawierta	As a project partner representative, Michal will be providing TQ information, and has high interest in the final design and functionality.	Weekly TQ's and information sessions. Meetings as required. Directed the team's soldering induction.
ANFF-WA	Project partner – has set the initial design brief and is the lab that will use the final design. Their end goal is successful development of a digitally controlled power supply for MEMS testing.	Engagement through project partners Dilusha Silva and Michal Zawierta.
Jega Gurusamy	As group facilitator, Jega will be present at weekly meetings and provide feedback on design processes. Additionally, he will approve components prior to purchasing, giving him higher	Weekly meetings, contribution reports and design reviews. Preliminary design review feedback outlined higher slew rate required for AC amplification op-amps. This was addressed in the critical design review

	stakeholder power.	where the op-amp chosen had the required high slew rate. However, the voltage outputs were not achieved for the required frequency range. The feedback provided at this review was to finetune the external components of the op-amp bridge circuit to increase the operating frequency range while maintaining the voltage range. This was subsequently addressed in the final design.
UWA Safety	Must approve Team Safety agreement prior to any construction or testing. May drastically impact project timeline if approval is not gained.	One-off safety agreement and additional paperwork sent through Dilusha as unit coordinator. Approval was not received by the UWA Safety team and hence the lack of stakeholder engagement hindered the progress of the design as testing of high voltage components was unable to be carried out.
End users-Researchers	Will use the final design, however, they have little power at this stage and will instead be represented through the project partner representatives.	Engagement through project partners and discussion with Jega for feedback on use of design such as fidelity of low voltage intervals of 0.05V.
Suppliers	Suppliers are crucial for meeting the team's time and cost constraints. Additionally, purchasing parts in small quantities may require additional supplier engagement.	Emails and queries sent through web portals.
UWA Purchasing Department	Will either purchase or reimburse component costs within budget. Require engagement to ensure components are purchased in time and design team is not purchasing with own money.	Submission of purchasing-orders or receipts for reimbursement.
Regulatory Bodies	Regulatory bodies such as ERAC (Electrical Regulatory Authorities Council) are not necessarily high power or interest at this point in the design, as the team's design is research-based and will not be going to market. However, organisations and associated standards contribute	Read provided material surrounding standards and safety. Did not engage with the bodies as the team's design and prototype is in its preliminary stages. The bodies will be engaged in later stages when the design is ready to go to market.

	helpful information about commercial or safety requirements that are required for future iterations.	

Following their identification, stakeholders were assessed with respect to their interest and power, as seen in Figure 1. This assessment was based on the roles and responsibilities outlined in Table 2. As highlighted, each quadrant relates to different levels of importance and required management. As the project progressed, some stakeholders' positions changed as the project requirements and scope were crystallised. These changes are depicted through the arrows and their direction within the matrix.

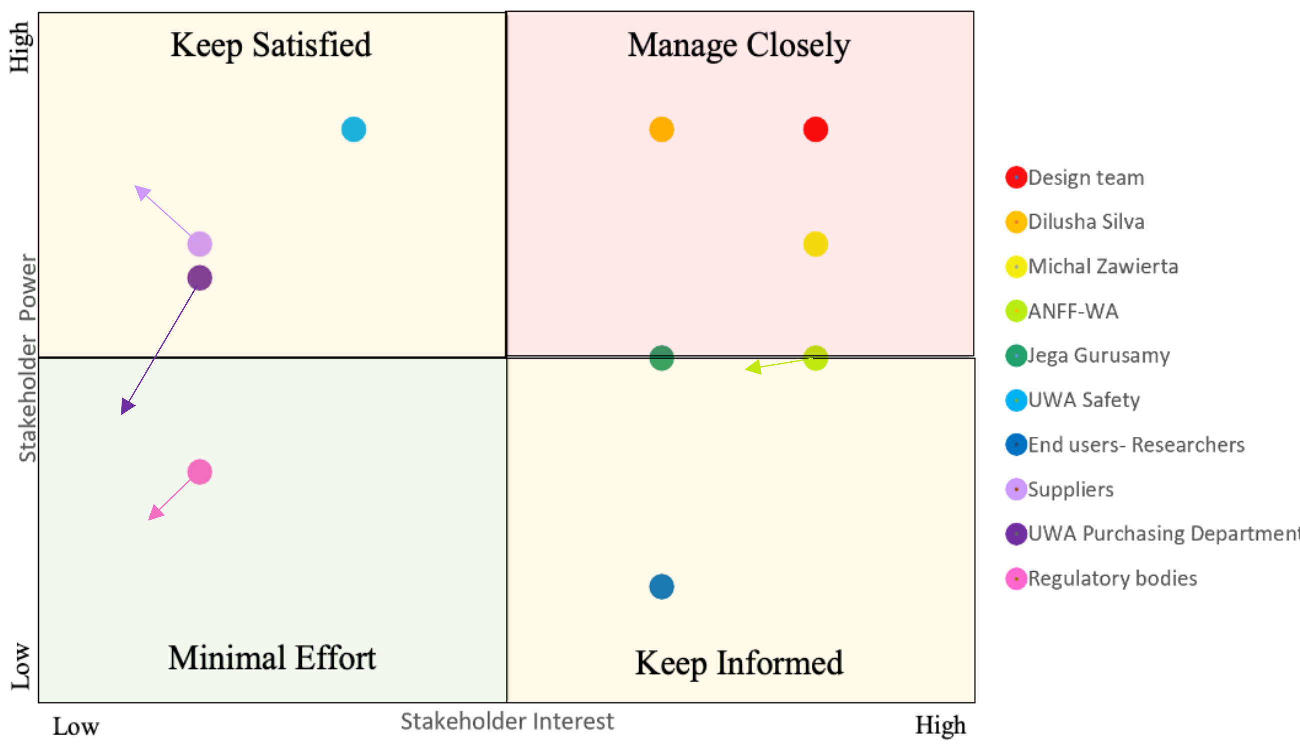


Figure 1: Stakeholder analysis matrix.

Lastly, the required stakeholder management and engagement was defined for each stakeholder, based on the interest-power matrix produced. This information has been included in Table 2 for conciseness and includes the executed format and frequency of stakeholder engagement.

3. Final Requirements

This section details the design requirements as formulated by the team. The requirements for the design were defined at the start of the project and were then refined throughout the design process. The requirement details include their priority category, the manner in which they were stated by the client, ranking, source, delivery method and testing/verification method.

3.3 Selection and Prioritisation Methodology

Table 3 outlines the requirement priority system as devised by the team. The requirement priority categories are as follows, from highest to lowest: Safety Critical, Critical, High, Medium and Low.

The requirements are also classified according to the nature they were stated by the client. The classifications are as follows:

- Spoken (S) – explicitly stated by the client.
- Unspoken (U) – not explicitly stated by the client but still expected to be delivered.
- Exciter (E) – may not be expected by the client but would be beneficial.

Table 3: Requirement priority categories.

Priority Category	Description
Safety Critical	Any requirement which presents a safety hazard to individual/s if not incorporated into the design.
Critical	Any requirement which is necessary to fulfil the design’s functional requirements and must be implemented for successful design delivery. Without meeting these requirements, the system will not operate.
High	Any requirement which is necessary to fulfil the design’s functional requirements and must be implemented to achieve client satisfaction.
Medium	Any requirement which is not necessary to fulfil the design’s functional requirements and is considered of high importance for client satisfaction.
Low	Any requirement which is not necessary to fulfil the design’s functional requirements and is considered of low importance for client satisfaction.

3.4 Final Requirements

The final design requirements are listed below, and any changes have been highlighted. Please refer to the Appendix for relevant testing conducted.

Req-01 – Compliance with Australian Standards

Requirement Description:
Design and testing carried out must comply with AS/NZS-61010.1 (Safety Requirements for Electrical Equipment) as well as other relevant standards such as AS/NZS-3000 and AS/NZS-3820.

Was the Requirement Met?	
Yes	
Priority Category:	Safety Critical
Source:	Design Team

Relevant Changes:	
Rank:	1
S/U/E	Unspoken

Req-02 – Overcurrent Output Voltage Cut-off

Requirement Description:
The device must incorporate output protection that switches off output voltage if the output current exceeds the set current limit (as per Req-17). Protection must be resettable to allow for repeat testing and give visual indication when cut-off is engaged.

Was the Requirement Met?	
Yes	
Priority Category:	Safety Critical
Source:	Project Brief

Relevant Changes:	
Rank:	2
S/U/E	Spoken

Req-03 – Maximum Response Time of Overcurrent Protection

Requirement Description:
The device must incorporate output protection capable of response times in the tens (10's) of milliseconds after current limit detection.

Was the Requirement Met?	
Yes	
Priority Category:	Safety Critical
Source:	Project Brief, TQ 31

Relevant Changes:	
Rank:	3
S/U/E	Spoken

Req-04 – DC Hardware Interlock

Requirement Description:
The device must incorporate a hardware interlock that limits the DC voltage to below 100V.

Was the Requirement Met?		**Relevant Changes:**	
Yes		A hardware interlock at 80V was implemented after consultation with client.	
Priority Category:	Safety Critical	**Rank:**	4
Source:	Project Brief	**S/U/E**	Spoken

Req-05 – AC Hardware Interlock

Requirement Description:
The device must incorporate a hardware interlock that limits the AC voltage to 50V RMS.

Was the Requirement Met?		**Relevant Changes:**	
No		This feature was incorporated as a software interlock instead	
Priority Category:	Safety Critical	**Rank:**	5
Source:	Project Brief	**S/U/E**	Spoken

Req-06 – Enclosure Construction Properties

Requirement Description:
Enclosure must be constructed to have sufficient rigidity, protection from electric shock and fire/elevated temperature.

Was the Requirement Met?		**Relevant Changes:**	
No			
Priority Category:	Safety Critical	**Rank:**	6
Source:	TQ 11	**S/U/E**	Spoken

Req-07 – Internal Failure Detection and Output Protection

Requirement Description:
The device will be designed such that, in the event of any internal failure, the output is disabled (no voltage) and a clear visual indication is given.

Was the Requirement Met?		**Relevant Changes:**	
Yes			
Priority Category:	Safety Critical	**Rank:**	7
Source:	TQ 51	**S/U/E**	Spoken

Req-08 – DC Output Voltage Range

Requirement Description:
The device must be capable of providing a DC output voltage over the range of 0-200V, adjustable as per Req-09.

Was the Requirement Met?	
Yes	
Priority Category:	Critical
Source:	Project Brief

Relevant Changes:	
Rank:	8
S/U/E	Spoken

Req-09 – Output Voltage Adjustment Fidelity

Requirement Description:
The device must be capable of output voltage adjustments of as little as 0.05V.

Was the Requirement Met?	
No (DC), Yes (AC)	
Priority Category:	Critical
Source:	Project Brief

Relevant Changes:	
Adjustments of <0.1V was achieved due to limitations in display fidelity and output signal noise.	
Rank:	9
S/U/E	Spoken

Req-10 – Maximum Current Output

Requirement Description:
The device must be capable of supplying up to 10 mA of current over the full range of AC and DC outputs.

Was the Requirement Met?	
Yes	
Priority Category:	Critical
Source:	Project Brief

Relevant Changes:	
Rank:	10
S/U/E	Spoken

Req-11 – Switchable Output Signal Amplitude Modulation for DC Outputs

Requirement Description:
The device must incorporate a switchable output signal amplitude modulator (100% level) using a square wave signal over the range of 10–100Hz for all DC outputs.

Was the Requirement Met?	
Yes	
Priority Category:	Critical
Source:	Project Brief, TQ 2

Relevant Changes:	
Rank:	11
S/U/E	Spoken

Req-12 – Tuneable AC Voltage Output Capability

Requirement Description:
The device must be capable of providing an AC output over the range of 0-200V RMS, adjustable as per Req-9, with a frequency range of 50-300kHz, tuneable as per Req-16.

Was the Requirement Met?	
No	
Priority Category:	Critical
Source:	Project Brief, TQ 1

Relevant Changes:	
Full frequency range for partial AC range	
Rank:	12
S/U/E	Spoken

Req-13 – Switchable Output Signal Amplitude Modulation for AC Outputs

Requirement Description:
The device must incorporate a switchable output signal amplitude modulator (100% level) using a square wave signal over the range of 10–100Hz for all AC outputs, tuneable as per Req-15.

Was the Requirement Met?	
No	
Priority Category:	Critical
Source:	Project Brief, TQ 2

Relevant Changes:	
10 Hz and 100Hz amplitude modulation	
Rank:	13
S/U/E	Spoken

Req-14 – Operation using a Specific Voltage from an External Power Supply Adapter

Requirement Description:
The device must be designed to operate using an external power supply adapter that provides a specified DC voltage in the range of 5 to 30V. If possible, the design will utilise a 12V input.

Was the Requirement Met?	
Yes	
Priority Category:	Critical
Source:	Project Brief

Relevant Changes:	
12V input utilised.	
Rank:	14
S/U/E	Spoken

Req-15 – Square Wave Frequency Adjustment Step Size

Requirement Description:
The device must be capable of adjusting the output square wave modulation frequency in steps of 10Hz.

Was the Requirement Met?	
Yes	
Priority Category:	Critical
Source:	TQ 2

Relevant Changes:	
Rank:	15
S/U/E	Spoken

Req-16 – AC Frequency Adjustment Step Size

Requirement Description:
The device must be capable of AC frequency adjustments steps of ~10 kHz.

Was the Requirement Met?	
Yes	
Priority Category:	Critical
Source:	TQ 1

Relevant Changes:	
Rank:	16
S/U/E	Spoken

Req-17 – Current Limit Tuning Fidelity

Requirement Description:
The current limit is tuneable between 1 and 10 mA, using steps of ~2 mA.

Was the Requirement Met?	
No	
Priority Category:	Critical
Source:	TQ 22

Relevant Changes:	
Functionality not included due to budget and time constraints.	
Rank:	17
S/U/E	Spoken

Req-18 – Effect of Noise on Output Signal

Requirement Description:
The device output voltage must not deviate more than 0.05V from the expected voltage under steady state conditions. This includes noise and the impact of voltage ripples.

Was the Requirement Met?	
No	
Priority Category:	Critical
Source:	TQ 61

Relevant Changes:	
Noise levels of ~0.1V after filters applied. Additional filtering not implemented due to budget and time constraints.	
Rank:	18
S/U/E	S

Req-19 – Use of CERN-OHL-P Licensed Hardware

Requirement Description:
The project hardware must be prepared using the open-source CERN-OHL-P License.

Was the Requirement Met?	
Yes	
Priority Category:	Critical
Source:	Project Brief

Relevant Changes:	
Rank:	19
S/U/E	Spoken

Req-20 – Project Handover Deadline

Requirement Description:
Project handover must occur on Friday Week 12 (20/10/2023). This is a project constraint.

Was the Requirement Met?	
No	
Priority Category:	Critical
Source:	Project Brief

Relevant Changes:	
Deadline extended to Wednesday (25/10/23).	
Rank:	20
S/U/E	Spoken

Req-21 – Overtemperature Shutdown

Requirement Description:
The device will shut down if internal temperature exceeds 80˚C.

Was the Requirement Met?	
Yes	
Priority Category:	High
Source:	Design Team

Relevant Changes:	
Rank:	21
S/U/E	U

Req-22 – BNC Output Ports

Requirement Description:
The device will use high-voltage BNC ports for the output signals. This is a project constraint.

Was the Requirement Met?	
Yes	
Priority Category:	High
Source:	TQ 24

Relevant Changes:	
Rank:	22
S/U/E	S

Req-23 – Sharing of Project Outcomes

Requirement Description:
Project outcomes will be shared with the project partner using GitHub. This is inclusive of: reports; designs; prototype documents; CAD Models; PCB Files; component registers; testing results; and may develop as the project progresses.

Was the Requirement Met?	
Yes	
Priority Category:	High
Source:	Project Brief

Relevant Changes:	
Rank:	23
S/U/E	Spoken

Req-24 – Component Selection

Requirement Description:
The process of selecting components shall be conducted with careful consideration of component availability, lead times, and the current manufacturing state. This approach aims to ensure timely procurement and seamless integration of components into the final product.

Was the Requirement Met?	
Yes	
Priority Category:	High
Source:	Design Team

Relevant Changes:	
Rank:	24
S/U/E	Exciter

Req-25 – Human-Machine Interface

Requirement Description:
The human-machine interface must allow users to set device parameters including the output signal type, frequency and voltage, as well as the output protection current limit.

Was the Requirement Met?	
Yes	
Priority Category:	Medium
Source:	Project Brief, TQ 59

Relevant Changes:	
Rank:	25
S/U/E	S

Req-26 – Repairability, Maintainability and Operational Lifespan

Requirement Description:
The design shall prioritise repairability, maintainability, and an operational lifespan of a minimum of 10 years. Some measures shall be considered to address potential component unavailability in the future by providing recommendations for suitable replacements.

Was the Requirement Met?	
Yes	
Priority Category:	Medium
Source:	TQ 51

Relevant Changes:	
Rank:	26
S/U/E	Exciter

Req-27 – Use of Restriction of Hazardous Substances Directive compliant components

Requirement Description:
Design shall use Restriction of Hazardous Substances Directive (RoHS) compliant components wherever feasible.

Was the Requirement Met?	
Yes	
Priority Category:	Medium

Relevant Changes:	
Rank:	27

Source:	Design Team	**S/U/E**	Exciter

Req-28 – Project Budget

Requirement Description:
The project budget will be less than $350 inclusive of all prototyping, testing and final design. This is a project constraint.

Was the Requirement Met?		**Relevant Changes:**	
No		Final cost was $378.36 and was $28.36 over budget.	
Priority Category:	Low	**Rank:**	28
Source:	Project Brief	**S/U/E**	Spoken

Req-29 – Programmability

Requirement Description:
The device should incorporate a programmable output feature that allows users to define precise voltage and frequency parameters for designated durations. Once defined, output can be run using one button press. This feature will work for either AC or DC output for a given run.

Was the Requirement Met?		**Relevant Changes:**	
No		Feature not included in design due to time and budget constraints.	
Priority Category:	Low	**Rank:**	29
Source:	End User	**S/U/E**	E

3.5 Constraints

Project constraints are specifications and/or restrictions which affect the execution of the project [1].

Req-01 Safety Standards
Design and testing carried out must comply with AS61010.1 (Safety Requirements for Electrical Equipment). Safety requirements imposes a constraint on testing permitted and possible design solutions.

Req-14 – Operation using a Specific Voltage from an External Power Supply Adapter
The device will require a specific input voltage (i.e., 12V) and will not support a range of voltages. The input DC voltage is assumed to be stable under load and have negligible ripple and noise such that minimal input clean-up and regulation is required.

Req-19 – Use of CERN-OHL-P Licensed Hardware
This is a project constraint, as it imposes a limit on the type of hardware used in the design.

Req-20 - Project Handover Deadline
This is a project constraint, as it imposes a limit on the time available for the team to complete the project.

Req-22 – BNC Output Ports

This is a project constraint, as the requirement to accommodate this port type will affect the design of the circuity and the selection of components used in the design.

Req-28 – Project Budget
This is a project constraint, as it imposes limitations on the components and resources that can be used to deliver the project.

4. Design Architecture

4.3 Hardware Architecture

The architectural framework of the MEMS power supply design is structured around distinct modules, each catering to specific functionalities, as shown in Figure 2. The primary module is the microcontroller, which serves as the central processing unit for control and coordination. It interfaces with the extra low voltage (ELV) supply controlled by a switch, and with the high voltage (HV), medium (MV) and low voltage (LV) DC and AC circuits via a 4-way rotary switch. These hardware modules are equipped with relay protection and modulation components to ensure the proper functioning of the power supply system.

This modular approach to the hardware architecture allows for precise control and flexibility, ensuring seamless operation of the power supply design. Additionally, it enables systematic troubleshooting if a component malfunctions, offering a streamlined approach to component replacement rather than requiring the replacement of the entire system.

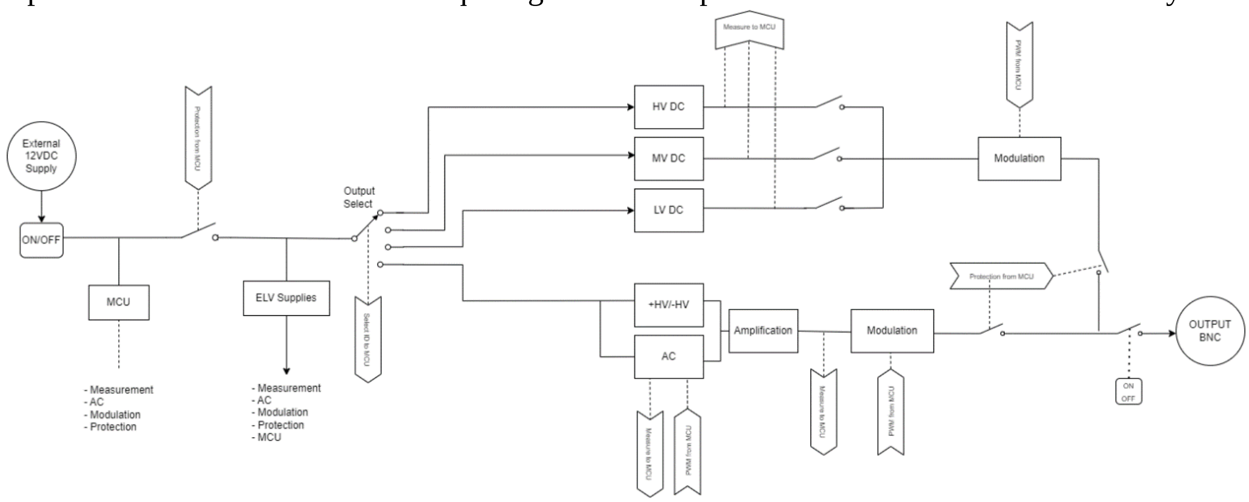


Figure 2: Simplified block diagram of power supply design.

4.4 Software Architecture

The design's hardware architecture was designed such that the software could have a relatively simple, state-machine type design. This is reflected through the use of manual switches and physical potentiometers which directly change the operating state and parameters of the system, with the Arduino simply monitoring the changes and providing this information to the user the via a display.

This design was chosen in favour of the alternative option, which would involve sending digital commands/changes to the microcontroller, which would execute the corresponding system changes via electronic control (i.e., electronic switches and digital potentiometers).

Thus, the resulting code is similar to a state machine, where the states are the selection of modes: AC, LV, MV or HV, with each mode changing the input pins that the Arduino is monitoring, in addition to the switching of a few relays and changing the display output to suit.

The system checks the mode status at the beginning of every loop, and should multiple or no pins be HIGH, the system enters an error state.

If the mode has changed since the previous loop (where loops will take fractions of a second), this is recognised, and the system enters mode setup. In this mode, multiple delays and relay switching are performed to ensure that each part of the circuit does not interact with one another, as much of the LV DC circuitry is not rated to the MV or HV voltages.

Following the setup, the main loop is entered. This effectively monitors the system output voltage from a given pin, determined by the current mode. If modulation is ON, then the microcontroller also sends switching signals to the MOSFETs for DC modulation, or changes the SPI signal sent to the waveform generator for AC. The corresponding settings and measurements are then displayed to the user on the screen.

The system software flow diagram is shown in Figure 3.

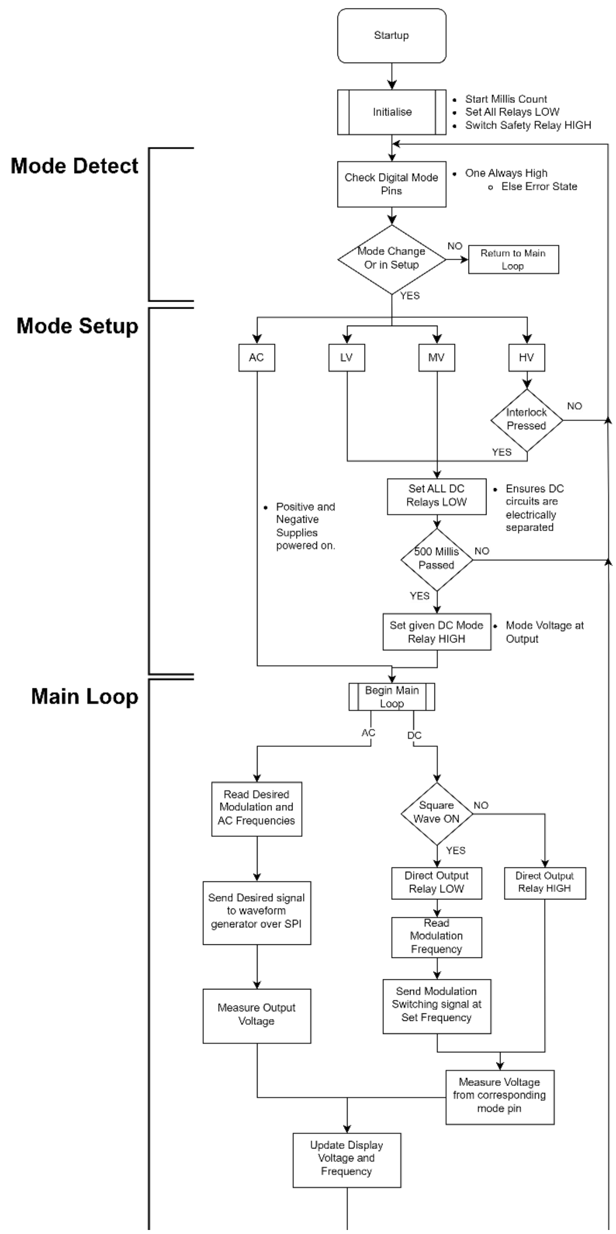


Figure 3: Software flow diagram.

5. Final Design Elements and Tests

5.3 DC Supply

5.3.1 Relevant requirements

The following requirements are relevant to the DC subcircuit of this design.

Requirement ID	Short Description
04	Hardware interlock that limits the DC voltage to 100V.
08	DC output voltage over the range of 0-200V.
09	Output voltage adjustments of as little as 0.05V.
10	Up to 10 mA of current supply over the full range of AC and DC outputs.
14	External power DC voltage in the range of 5 to 30 V. If possible, the design will utilise a 12V input.
18	The output voltage must not deviate more than 0.05V from the expected voltage under steady state conditions.

5.3.2 Circuit design

The DC supply circuit is split into three subcircuits; Low Voltage (LV) ranging from 0 to 30V, Medium Voltage (MV) from 12 to 80V and High Voltage (HV) from 50V to 200V (Req-09). A modular design approach was utilised as this allows for separate circuits to be built and tested in isolation. The LV circuit can be tested by the design team without supervision and the separation of the MV and LV allows for simple and safe hardware interlock by preventing the selection of the HV circuit when the interlock is engaged (Req-04). All modules can deliver the minimum required current as per Req-10, which was confirmed by consulting the datasheets and through testing after receiving the modules.

As shown in the block diagram below, all subcircuits are supplied from the 12V input and have a common output channel, with diodes installed for reverse current protection and a rotary switch for circuit stream selection.

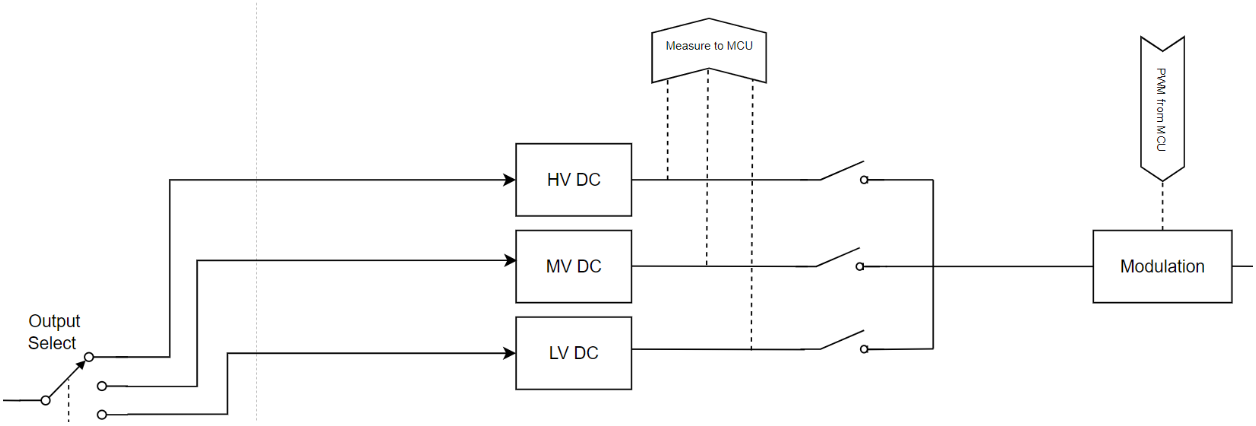


Figure 4: DC circuit block diagram.

The LV circuit is a buck-boost converter controlled by LTC3780, with a potentiometer used to adjust the output voltage. This board delivers voltages down to 0.8V but features some switching noise, as seen in the below figure. The addition of an RC filter successfully removed most of the switching noise, allowing for finer adjustment and more stable output (Req-09). Due to limitations in the measuring circuitry, the supply cannot read voltage adjustments below 0.1V. At this level, the output of this circuit is accurate and stable with a final noise level of 96mV, as observed in the below oscilloscope readings (Y2 measured across the yellow waveform).

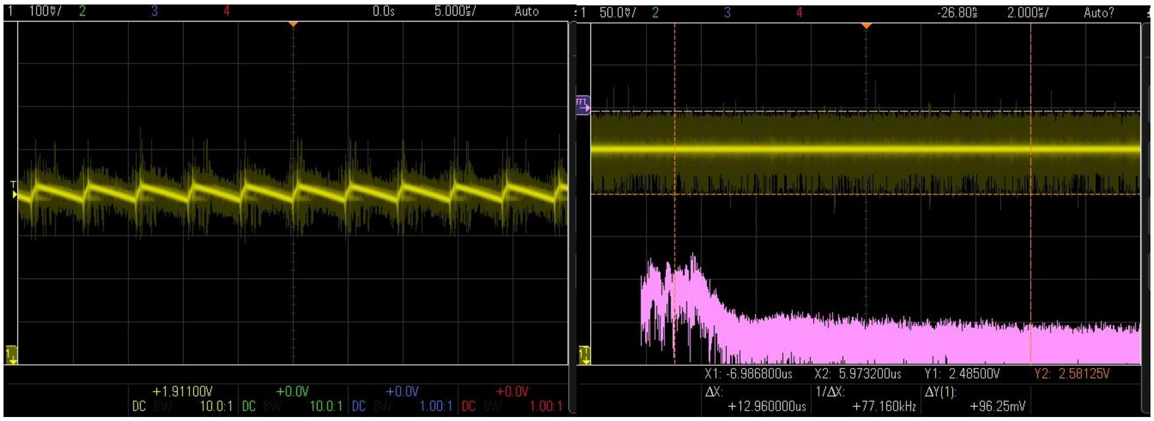


Figure 5: LV DC module voltage output before filtering (left) and after filtering (right).

The MV circuit is a boost converter, stepping up the voltage from 12V to 80V, with a potentiometer used to adjust the output voltage within this range. No filter was employed on this module. The output voltage signal is shown below with a noise level of 325mV. This is higher than preferred, as this does not meet Req-18.

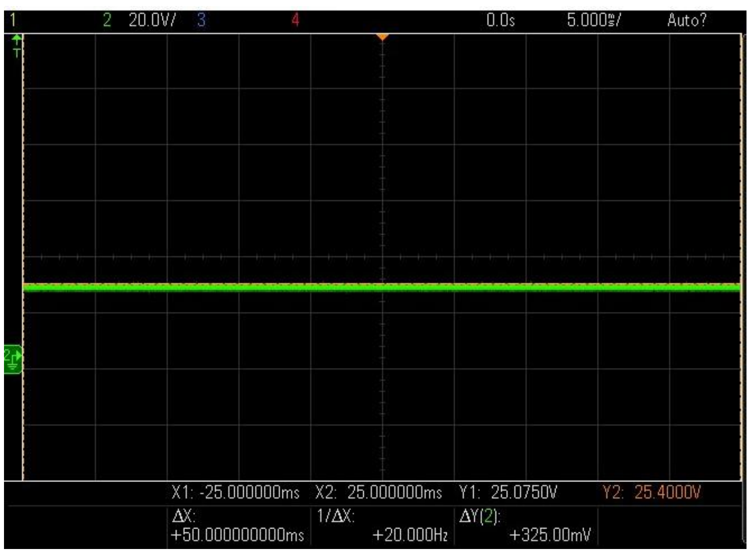


Figure 6: MVDC module output voltage.

The HV DC Module supplies voltages up to 200V using a ZVS (Zero Voltage Switching) driver circuit and a flyback transformer to generate the high voltage from the 12V input. Due to testing limitations, the characteristic noise of the HV circuit output could not be provided.

The selection between the three subcircuits is performed by a 2-pole, 4-way rotary switch, as shown at the input in the block diagram. This allows these switches to also act as the hardware interlock, as it is impossible to have 80V at the output if the LV/MV circuit is selected. This provides a hardware interlock limiting the output to 80V, as opposed to the originally requested 100V.

5.3.2.1 Dual DC supply for AC circuitry

Dual 5V supply is required for the AC preamplification module. This is achieved by a simple voltage divider circuit from the external supply. A virtual ground is generated between the two resistors, rendering the output voltages to ±5.5V with a 12V supply. The operational amplifier is added as a buffer to ensure a stable output voltage regardless of the load. As seen in the circuit, simulation and oscilloscope output below, this successfully generates a dual power supply.

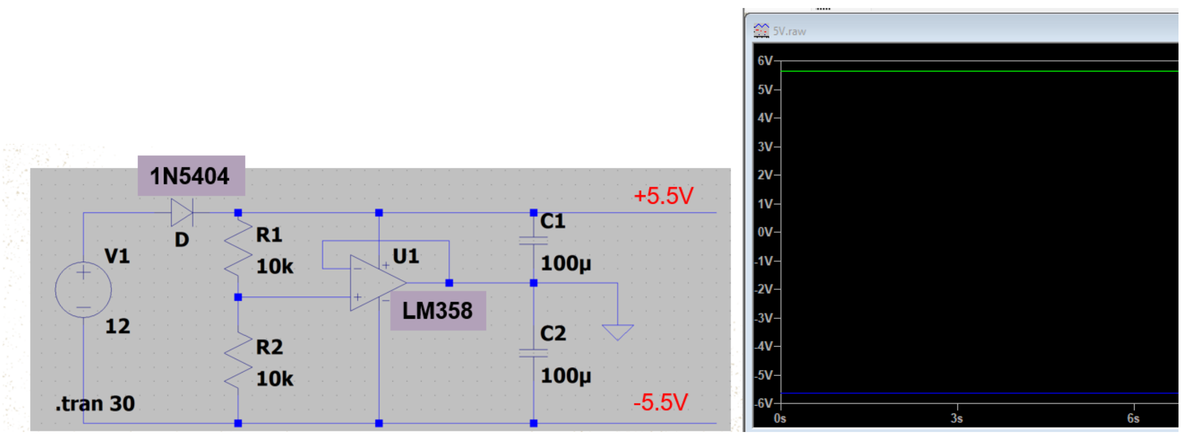


Figure 7: Dual 5VDC supply simulation.

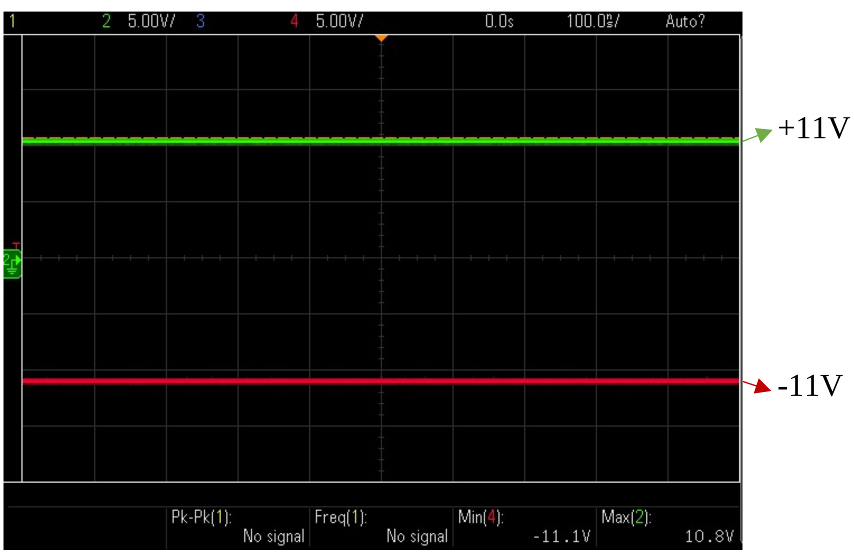


Figure 8: Dual 5VDC supply output with 22V input.

The AC amplification stage requires a dual DC supply at higher voltages. For this design ±125V was to be supplied. This renders the AC output slightly lower than what was required, however, due to the limited budget this requirement has been limited. The required components were purchased; however, time did not allow for the design and delivery of a custom PCB which would be required for their functionality. Hence, this circuit was not built, but a suggested PCB layout can be found in the Appendix. This design can also easily be modified as per the circuit shown in the Appendix via the addition of an additional charge pump circuit.

The positive supply is delivered from a HVDC module equivalent to that utilised in the HV DC circuit. The negative supply is generated by the below circuit based around the boost controller LT8365. This design allows for the AC supply to be independent of the main DC subcircuit, hence the safety interlock is separate for the two sections. So, any fault in the DC circuitry will not impact the AC supply, improving the reliability of the overall design due to this added redundancy.

5.3.2.2 DC supply for components

Establishing a robust low voltage power supply for subcomponents is essential for the correct function of every module. As components typically require similar voltage ranges a small number of low voltage power supply modules are needed and a similar architecture can be leveraged with small deviations. Analog Device's LTC1085 can intake a wide range of voltages and provide up to 3 A which is more than adequate for our requirements. The output voltage for a given module is determined by the following formula [2]:

$$V_{Out} = V_{Ref}\left(1 + \frac{R_2}{R_1}\right), \qquad for\ V_{Ref} = 1.25, \qquad R_1 = 90.9$$

This means for a 5V and 9V module we require resistors of 272.2 Ω and 563.58 Ω respectively. As the closest cheap and readily available values on mouser were 277 Ω and 560 Ω, our final modules will generate approximately 5.06 V and 8.95 V which is an acceptable deviation. Figure 9 shows the resultant schematic and simulation, with capacitors added to minimise overshoot to less than 10% of V_{out}.

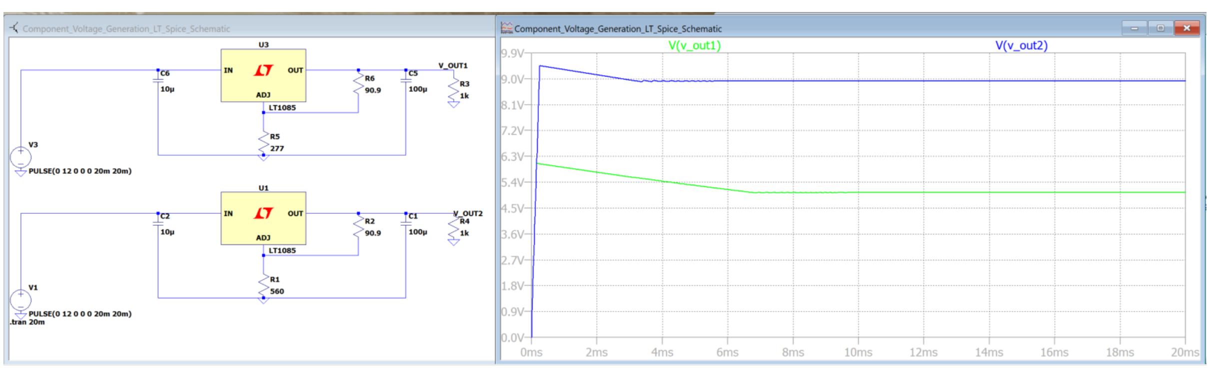


Figure 9: Component voltage generation schematic (left) and simulation (right).

5.4 Square Wave Modulation

5.4.1 Relevant requirements

The following requirements are relevant to the DC square wave modulation function of the design.

Requirement ID	Short Description
11	Device must incorporate a switchable output signal amplitude modulator (100% level) using a square wave signal over the range of 10–100Hz for all DC outputs.
13	The device must incorporate a switchable output signal amplitude modulator (100% level) using a square wave signal over the range of 10–100Hz for all AC outputs.
15	The device must be capable of adjusting the output square wave modulation frequency in steps of 10Hz.

5.4.2 Circuit design

To complete the DC square wave modulation for the design, a pair of high-side, high voltage bootstrap driven MOSFETs were chose to switch the generated DC voltage on the output of any of the three DC circuits. These MOSFETs can be either N-FET or P-FET devices, however N-FET were chosen for this design due to their superior switching performance, voltage rating and availability at lower price points than P-FET alternatives.

In order to drive such MOSFETs in a high side configuration, there are multiple challenges that must accounted for in the circuit design to achieve the desired performance and expected system output [3], notably:

1. Gate voltages must be driven 10V to 15V higher than the source voltage (in this case, the device output voltage). As this is a high-side switch, the gate voltage must be higher than the rail voltage, which is the highest available voltage in the system.
2. The gate voltage must be controllable via a logic level input (i.e., 5V digital Arduino pins). As a result, the control signal must have its voltage boosted above the high voltage rail.
3. The capacitive nature of the MEMS load means that a single FET switch on the high side (i.e., in series with the positive output channel) could result in the connected device holding the positive rail voltage above ground, causing inaccurate or incorrect square wave modulation from the view of the MEMS device. Using a low-side FET in tandem solves this, allowing any stored charge to short to ground when the square wave should be grounded.

These issues can be resolved by implementing a high-side floating MOS-gate driver that is able to control a pair of N-FETs. The chose IC was the IRS2011PBF from Infineon Technologies, which can handle up to 200V, a gate supply range of 10V-20V, is compatible with 5V logic, has independent low and high side channels, a maximum delay of 20ns and is relatively low-cost at under $6 dollars. This IC has the typical connection diagram as follows:

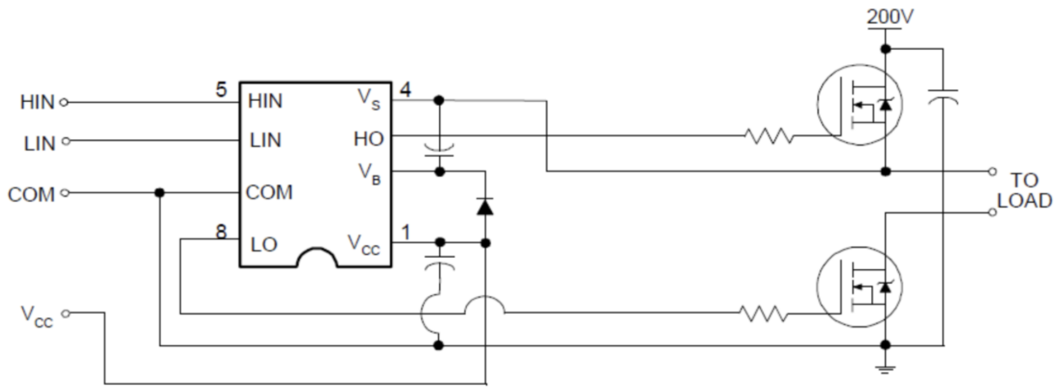


Figure 10: Typical connection diagram for the IRS2011PBF [4].

There was no documentation on the choice and sizing of the shown components, but further research shows that a majority are for a bootstrap power supply [5].

MOSFETS:

The choice of MOSFET is influenced by the maximum voltage rating (230V safety margin), high switching speed and low on-resistance. The IRF740 from Vishay was chosen as it fulfills the system requirements and is available at Altronics for ~$2. It has a maximum voltage rating of 400V, 0.46 Ohm on-resistance, a turn on delay time of 17ns and a rise time of 10ns. Regarding the delay and rise time, the device only needed to be capable of switching at 100Hz as per the modulation requirements, which means that the total delay must be less than 0.01s, which is relatively easy to achieve with modern silicon.

Bootstrap Diode:

The bootstrap diode needs to be able to fully block the full power rail voltage and must have a fast recovery time to minimise the amount fed from the bootstrap capacitor into the V_{cc} supply. The chosen diode was the 1N4148 diode as it can block up to 100V with a reverse recovery time of 4ns, both of which is more than sufficient.

Gate Resistors:

These were left as 0 Ohms for this device, as there was a need to maximise the switching speed of the MOSFETs, and as the total gate charge was relatively small, they were deemed unnecessary.

V_{cc} Capacitor:

This capacitor serves to stabilise and boost the V_{cc} input at a steady 12V so that the gate driver can act quickly without any voltage drop interfering with the switching. As such, a small, generic 220nF capacitor was chosen from the large selection in the soldering lab.

Bootstrap Capacitor:

The bootstrap capacitor is responsible for boosting the available voltage above the given rail voltage using the supplied V_{cc} voltage, and providing the charge needed to drive the MOS gates for the given duty cycle. The sizing of this capacitor uses the following formula:

$$C \geq \frac{2\left[2Q_g + \frac{I_{qbs(\max)}}{f} + Q_{ls} + \frac{I_{Cbs(leak)}}{f}\right]}{V_{cc} - V_f - V_{LS} - V_{Min}}$$

where:

Q_g = Gate charge of high-side FET
f = frequency of operation
$I_{Cbs\,(leak)}$ = bootstrap capacitor leakage current
$I_{qbs\,(max)}$ = Maximum V_{BS} quiescent current
V_{CC} = Logic section voltage source
V_f = Forward voltage drop across the bootstrap diode
V_{LS} = Voltage drop across the low-side FET or load
V_{Min} = Minimum voltage between V_B and V_S.
Q_{ls} = level shift charge required per cycle (typically 5 nC for 500 V/600 V MGDs and 20 nC for 1200 V MGDs)

By inputting the device values and multiplying the result by ~15x (as is good practice) [5], the chosen capacitance was $\sim 20\mu F$, with a voltage rating greater than V_{cc}. As such, a generic capacitor was chosen for this.

A notable design requirement was for the modulation be toggleable. To achieve this with the high-side MOSFETs, the high side FET had to be constantly on during this mode. With the current bootstrap circuit this would likely not be possible, as the bootstrap capacitor would eventually run out of charge to drive the gate, resulting in the FET having to switch off eventually. This can be solved using a charge pump circuit, however due to its high complexity of implementation, the overall circuit was designed to be able to entirely bypass the modulation using a relay when this functionality was desired.

The microcontroller can adjust the switching frequency of the gate driver using the HIN and LIN pins, which would ALWAYS operate in opposition to each other, i.e., if the HIN is high, LIN must be low, and vice versa. The frequency of these signals can be adjusted using a rotary encoder connected to the microcontroller. Note that the gate driver is always operating at a 50% duty cycle.

Testing of this circuit on an oscilloscope was not able to be completed but testing at nominal frequencies (1-100Hz) was successfully performed using a resistive load (a LED) for the full range of voltages on a breadboard. The breadboarded MOSFET modulation circuit is shown in Figure 11.

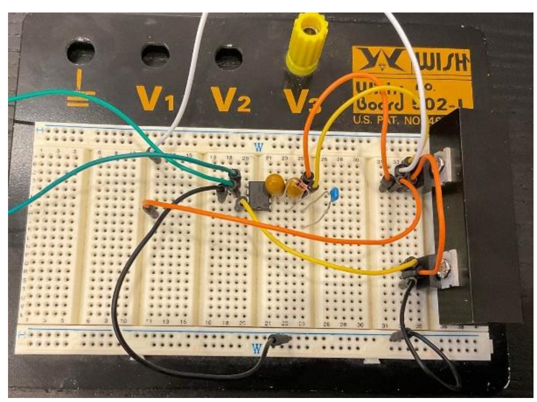


Figure 11: Breadboarded MOSFET modulation circuit.

5.5 AC Supply

5.5.1 AC Waveform Generation

Requirement ID	Short Description
5	The device must incorporate a hardware interlock that limits the AC voltage to 50V RMS.
9	The device must be capable of output voltage adjustments of as little as 0.05V.
12	The device must be capable of providing an AC output over the range of 0-200V RMS, adjustable as per Req-9, with a frequency range of 50-300kHz, tuneable as per Req-16.
13	The device must incorporate a switchable output signal amplitude modulator (100% level) using a square wave signal over the range of 10–100Hz for all AC outputs, tuneable as per Req-15.
15	The device must be capable of adjusting the output square wave modulation frequency in steps of 10Hz.
16	The device must be capable of AC frequency adjustments steps of ~10 kHz.

Waveform generation was performed by a dedicated chip to ensure minimal complexity and a streamlined configuration process. The required frequency range of 50kHz-300kHz rendered H-bridge architectures unsuitable due to the high associated $\frac{dV}{dt}$ inherent to this switching configuration. Thus, a waveform generator that produced a sine wave based on a high-resolution frequency and phase register was elected as the best methodology.

Analog Device's AD9833 has a 28-bit resolution frequency register allowing for 0.1Hz increments between 0MHz and 12.5MHz and can be simply interfaced via SPI [6]. As it requires 10µF and 0.1µF bypass capacitors between V_{DD} and A_{GND} [6], its implementation requires only three components for complete implementation. In terms of noise performance, it does not perform as strongly in the kHz range, however Figure 12 shows that it can more than capably produce the desired frequency range with adequately low noise.

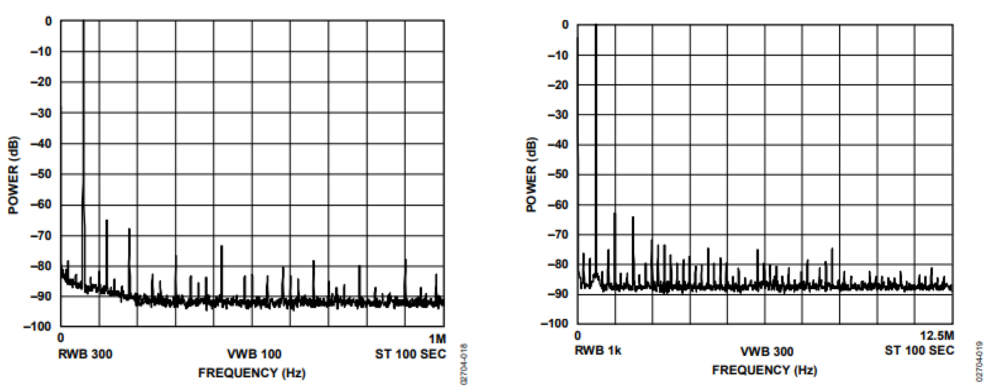


Figure 12: Power vs. Frequency, $f_{MCLK} = 25\ MHz,\ f_{out} = 60kHz\ (left), f_{out} = 600kHz\ (right)$, adapted from [6].

A high degree of liberty can be taken by the user with the Arduino code to allow for greater increment accuracy or frequency corrections based off internal measurement. For component validation, a variable potentiometer was measured at port A0, with this being able to be outsourced to a digital input in the final implementation. Figure 13 highlights the simplicity of implementing the AD9833.

```
void setup() {
    // This MUST be the first command after declaring the AD9833 object
    gen.Begin();

    gen.ApplySignal(SINE_WAVE,REG0,rate);

    gen.EnableOutput(true);   // Turn ON the output - it defaults to OFF

    pinMode(A0,INPUT);
    pinMode(A5,INPUT);

    Serial.begin(9600);
}
```

Figure 13: Arduino code used to modify frequency parameter.

The *void loop()* section in the remaining body of the code breaks down the analogue voltage range to correspond to different kHz values. The importance of bypass capacitors is illustrated in Figure 14, showing the occurrence of voltage spikes in their absence.

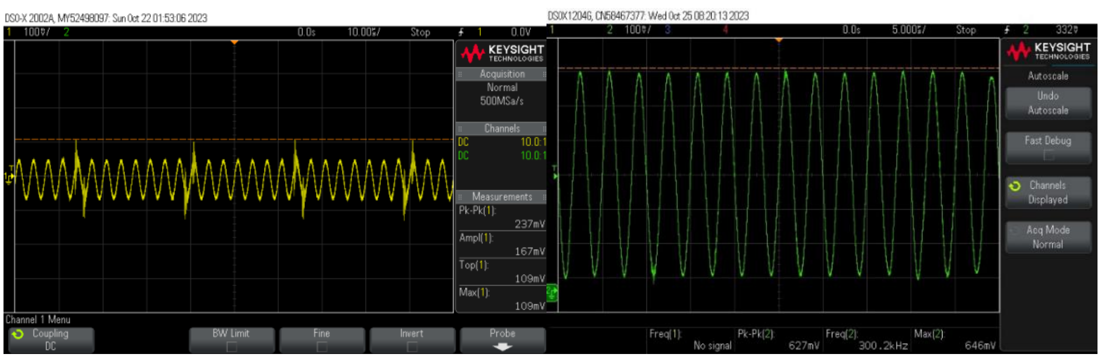


Figure 14: Waveform for f_{out}=300kHz, without capacitors (left) and with capacitors (right).

Thus, Req-12 (partially) and Req-16 were achieved through this component implementation.

5.5.2 Low Voltage AC Generation

As high noise immunity and gain fidelity were of greatest importance to this stage, the LT1818 and Renesas 1k and 10k Digitally Controlled Potentiometer was used to buffer the generated waveform and allow for small increments in gain. The LT1818 was selected based on its strong noise performance illustrated in Figure 15.

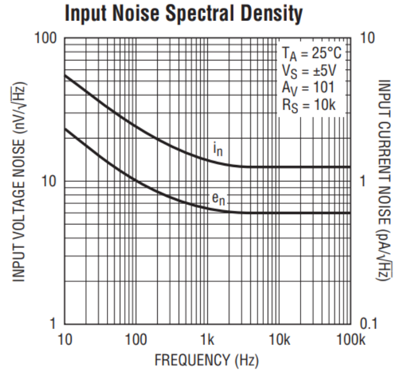


Figure 15: Noise performance of LT1818, extracted from [3].

The potentiometers have 100 wiper positions and a wiper resistance of 40Ω [7], allowing them to increment by 10Ω and 100Ω respectively. The wipers can be programmed to produce a continuous Ohmic range in 10Ω increments from 190Ω to 11080Ω. An inverter amplifier's gain is based on the following equation:

$$G = \frac{R_F}{R_I}$$

This would result in a gain range of 0.019% to 1108% of the input signal's amplitude. Due to the op-amp and potentiometer's maximum voltage range of ±5V, the maximum resistance would be capped at 6920Ω in the final implementation, using a global variable which counts the resistance. This corresponds to 90% of the gain required to achieve a ±5V AC signal with the maximum input signal voltage (650mV). This could also have been capped dynamically based on measuring the gain through voltage measurement, however the voltage measurement was not feasible at the time of submission.

This could be further capped when the AC Hardware interlock is activated, ensuring the gain can never exceed a value which produces a 50 VRMS+ AC Wave. The minimum and maximum AC amplitudes from this method were 0.1235V and 4.498V, with a gain increment of 0.01 corresponding to an amplitude increment of 6.5mV. Figure 16 outlines the schematic and waveform of the lowest possible gain.

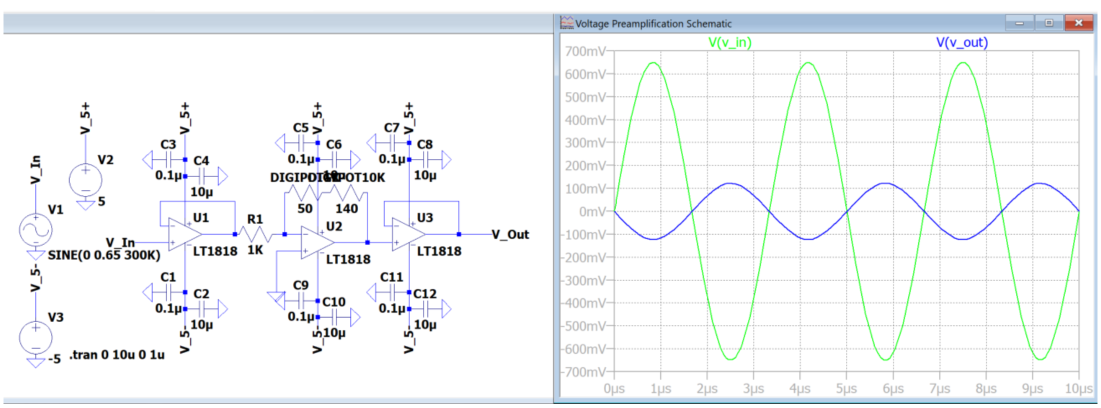


Figure 16: AC amplification with gain = 0.190, f =300kHz.

The increment rate was based on the potentiometer's dial position to allow users to quickly achieve a broad gain and a specific gain more precisely.

```
void adjustPotentiometer(int potValue) {
    float rangeFifth = 1023.0 / 5;

    if (potValue < rangeFifth) {
        decrementPotFast();
    } else if (potValue < 2 * rangeFifth) {
        decrementPotSlow();
    } else if (potValue < 3 * rangeFifth) {
        // Middle fifth - do nothing}
        else if (potValue < 4 * rangeFifth) {
        incrementPotSlow();   }
        else {
        incrementPotFast(); }}

void incrementPotFast() {
    if (x9cResistance < 10040) { // 10k + 40 ohms wiper resistance
        digitalWrite(UD_PIN, HIGH);
        changeWiper(5);  // Adjust the value as needed
        x9cResistance += 100; // Each step is approx 100 ohms for X9C103 }}

void decrementPotFast() {
    if (x9cResistance > 140) {  // 100 + 40 ohms wiper resistance
        digitalWrite(UD_PIN, LOW);
        changeWiper(5);
        x9cResistance -= 100;}}

void incrementPotSlow() {
    if (x9cResistance < 10040) {
        digitalWrite(UD_PIN, HIGH);
        changeWiper(1);
        x9cResistance += 100;}}
```

Figure 17: Dynamic increment implementation for inverter gain.

After its arrival, it became immediately apparent that the LT1818 was not compatible with prototyping due to its S5 package. This required the use of the TL071C in its place, which had comparable performance but worse noise immunity and slew rate characteristics. The slew rate required for the preamplification stage was:

$$Slew\ rate = 2\pi f_{max} v_{max} = 9.425\ V/us$$

Therefore, the TL071C with its slew rate of 20 V/us can adequately replace the LT1818 [8]. This resulted in the protoboard shown in Figure 18.

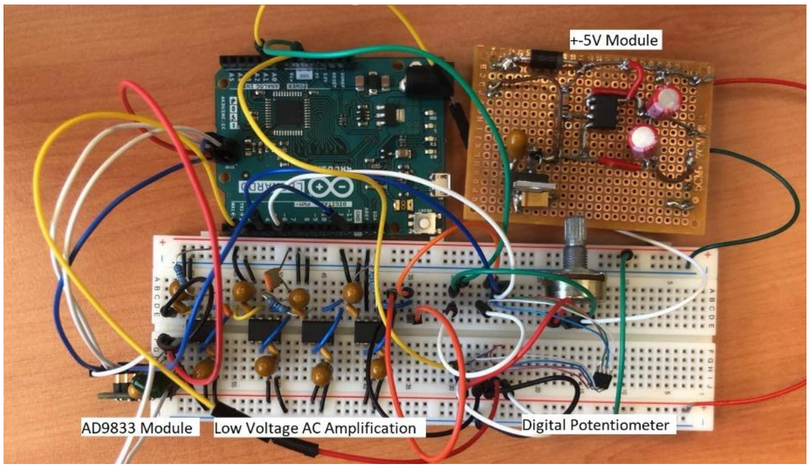


Figure 18: Waveform generation and low voltage AC breadboard.

The 1k potentiometer was omitted due to the complexity of its implementation. A low pass filter and high pass filter were also included in the low voltage preamplification stage over the first two op-amps to remove DC bias from the AC wave and reduce high frequency noise. They were sized as follows:

$$f_{corner\ frequency} = \frac{1}{2\pi RC}, for\ R = 1k$$

$$50{,}000\ Hz = \frac{1}{2\pi 1000 * C}, \qquad C = 3.18nF$$

$$300{,}000\ Hz = \frac{1}{2\pi 1000 * C}, \qquad C = 530.5pF$$

As these were not common values, 500pF and 3.3nF were selected, resulting in corner frequencies of 318.31kHz and 48.04kHz respectively. The low pass filter was validated on an earlier variant of the AC module, with the following signal improvement shown in green.

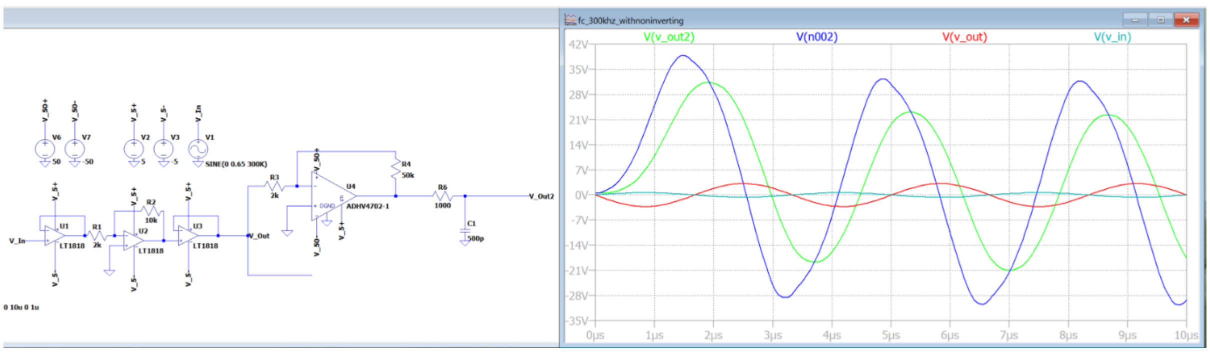


Figure 19: Example of first order low pass filter and associated waveform.

The testing of the breadboard was inconclusive, with reduced gain proven but containing significantly more noise, as per Figure 20.

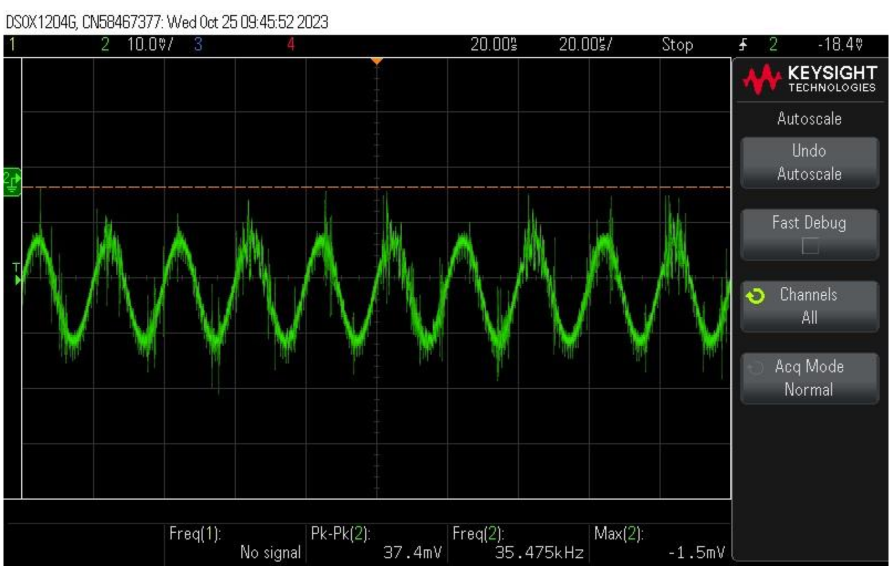


Figure 20: Waveform of low voltage AC generation.

Thus Req-05, Req-09 and Req-12 (partially) were achieved through this methodology.

5.5.3 AC Modulation

AC modulation was performed by connecting the generated low voltage AC wave to a single pole double throw (SPDT) switch due to its simple implementation and its added potential to allow for a dedicated low voltage AC line in future implementations. As the DG419LE presented a cheap option with worst-case scenario switching speeds of 40ns, it was selected to implement this feature [9]. Figure 21 highlights the modulation process once activated:

```
  // Perform switching based on mode
  switch (currentMode) {
    case MODE_OFF:
      // Do nothing
      break;
    case MODE_10HZ:
      if (currentMillis - lastSwitchTime >= interval10Hz) {
        toggleSwitch();
        lastSwitchTime = currentMillis;
      }
      break;
    case MODE_100HZ:
      if (currentMillis - lastSwitchTime >= interval100Hz) {
        toggleSwitch();
        lastSwitchTime = currentMillis;
      }
      break;
  }
}
```

Figure 21: AC modulation switching process.

Thus, Req-13 and Req-15 could be achieved with this implementation.

5.5.4 High Voltage AC Amplification

5.5.4.1 Relevant requirements

The following requirements are relevant to the AC amplification subcircuit of this design.

Requirement ID	Short Description
12	AC output over 0-200V_{RMS} with a frequency of 50-300kHz, tuneable.
18	Deviation of 0.05V from expected voltage under steady state conditions. This includes noise and impact of voltage ripples.

5.5.4.2 Circuit Design

The AC amplification stage is achieved through the use of operational amplifiers (op-amps). Op-amps amplify the difference in voltage between its input terminals using external feedback components such as resistors and capacitors [10]. Its input terminals are known as the inverting (-) and non-inverting (+) terminals, and it has a singular output. The amplification of the voltage is achieved through an extremely high gain. The op-amp maintains a virtual short circuit i.e., the voltage at the inverting input equals the voltage at the non-inverting input. This is achieved through the gain of the circuit, which maintains the output voltage to a level that allows the two inputs to remain equal.

There are two configurations of op-amps that are most commonly used to amplify voltage; these include the non-inverting voltage amplifier and inverting voltage amplifier [11]. Op-amps are used in a variety of applications such as amplifiers, active filters, integrators, differentiators, oscillators and detectors [12].

Op-amp characteristics which are vital to its application and thus should be carefully chosen include the slew rate, configuration, gain-bandwidth product (GBW), common-mode rejection ratio, feedback and compensation techniques, as well as cost. The slew rate of an op-amp is the acceptable rate at which the output voltage can change for the specified op-amp and is typically expressed in V/μs [12]. This value determines how quickly an op-amp can respond to rapid changes in the input signal. This determines the distortion or signal degradation of the output voltage. This value is vital when choosing an op-amp in applications with high-frequency responses or fast signal changes, to allow the output signal to remain stable. The slew rate is calculated as:

$$f_{max} = \frac{SR}{2\pi V_{CC}} \rightarrow SR = 2\pi V_{CC} f_{max}$$

V_{CC} is the maximum allowable peak amplitude of the output for linear operation and f_{max} is maximum frequency of the circuit. For the power supply requirements, the required slew rate would be:

$$SR = 2\pi V_{CC} f_{max} = 2\pi(283)(300kHz) = 533.172V/\mu s$$

The gain-bandwidth product is the product of the bandwidth and the open-loop gain which is typically used to express the relationship between the achievable gain and bandwidth in op-amp [13]. This can be calculated as:

$$GBW = Gain \times Bandwidth = A \times BW = \frac{V_{out}}{V_{in}} \times BW$$

The gain and bandwidth are inversely proportionate and thus, the selection of an op-amp with an appropriate GBW is of paramount importance and must be carefully chosen by optimising the two variables [13]. The GBW value is dependent on the application of the op-amp circuit and its bandwidth and gain requirements. The power supply design demands a high gain, as it is a precision amplification, thus requiring an op-amp with a higher GBW to ensure that the desired bandwidth is available at the specified gain. The GBW required for the system is calculated as:

$$GBW = \frac{V_{out}}{V_{in}} \times BW = \frac{283}{5} \times 250 \cdot 10^3 = 14.15\ MHz$$

As the GBW is an inherent characteristic of an op-amp and cannot be changed, other methods may need to be used to ensure an appropriate GBW is chosen for the circuit. One such method is cascading op-amps to achieve the desired overall gain without sacrificing bandwidth.

Another factor to consider when designing op-amps is the correct compensation techniques to apply. Compensation techniques are used to enhance the stability of the op-amp as well as reduce distortion and improve performance. As signals propagate through the feedback loops, they pass through both the op-amp and the external feedback network. The feedback loop introduces delays due to components like resistors and capacitors. These delays can lead to phase shifts in the signal, potentially jeopardising the stability of the circuit [14]. Compensation techniques are employed to prevent these issues. This includes the addition of components like capacitors or resistors to the op-amp or the feedback network. These components can help shape the frequency response of the circuit, by ensuring that the overall phase shift in the feedback loop remains below 180° and that the gain does not exceed unity [14].

Based on the specific requirements and considerations for the power supply design, these vital characteristics of op-amps were meticulously examined to ensure optimal performance. While this led to the identification of optimal parameters, the practical selection process introduced budgetary constraints. Specifically, the considered op-amps were assessed, including the Apex Microtechnology PA85, Microchip Technology HV264, Analog Devices LT1097 and Maxim Integrated MAX4036AAXK+T.

The PA85 op-amp, characterised by its impressive slew rate of 1000V/µs and capacity to achieve an output voltage of 450V, exhibited outstanding performance; however, its cost amounted to $333.43, exceeded the predefined budget constraints. Conversely, the HV264 op-amp was economically viable at a cost of $12.26 and could supply 152V_{RMS}. However, its gain of 66.7V/V and slew rate of 9V/µs did not align with the design's specifications.

Precision op-amps, such as the LT1097 and MAX4036AAXK+T, were able to fulfill the required output voltage, particularly when utilised in a cascading configuration alongside an op-amp like the HV264. These op-amps, priced at $9.90 and $1.94 respectively, presented a cost-effective option, however they did not meet the expected requirements due to their relatively low slew rates and low output voltage of 17V and 3.7V, respectively.

Ultimately, the PA79 was chosen as it met the required criteria. This dual op-amp integrated circuit (IC) boasts the capability to deliver 350V or ±175V, and its distinctive bridge configuration allows its slew rates to surpass 350V/µs. The PA79 aligns with the budgetary limits with an achievable cost of $91, thus satisfying both the performance and financial constraints.

The PA79 is uniquely configured in a bridge mode to amplify the voltage with a higher slew rate. The configuration consists of two op-amps, a master and a slave. The master op-amp accepts the input signal and provides the necessary gain to develop a full output swing from the input signal. The slave op-amp is configured as a unity gain inverting amplifier and is driven from the output of the master. The desired gain is set by selecting appropriate resistors in its feedback loop.

To enhance the slew rate in a bridge configuration, the master amplifier is set up with a high slew rate which allows the slew rate to be further amplified by the slave amplifier. As the input signal goes through the master op-amp, the output is a voltage that has been amplified according to the gain. This output voltage is then the input to the slave op-amp, which inverts it while maintaining the same magnitude. The overall output voltage is these two outputs combined, which effectively doubles the voltage magnitude from the master. The typical performance graphs were examined to determine the optimal external component values. The circuit schematic is shown in Figure 22.

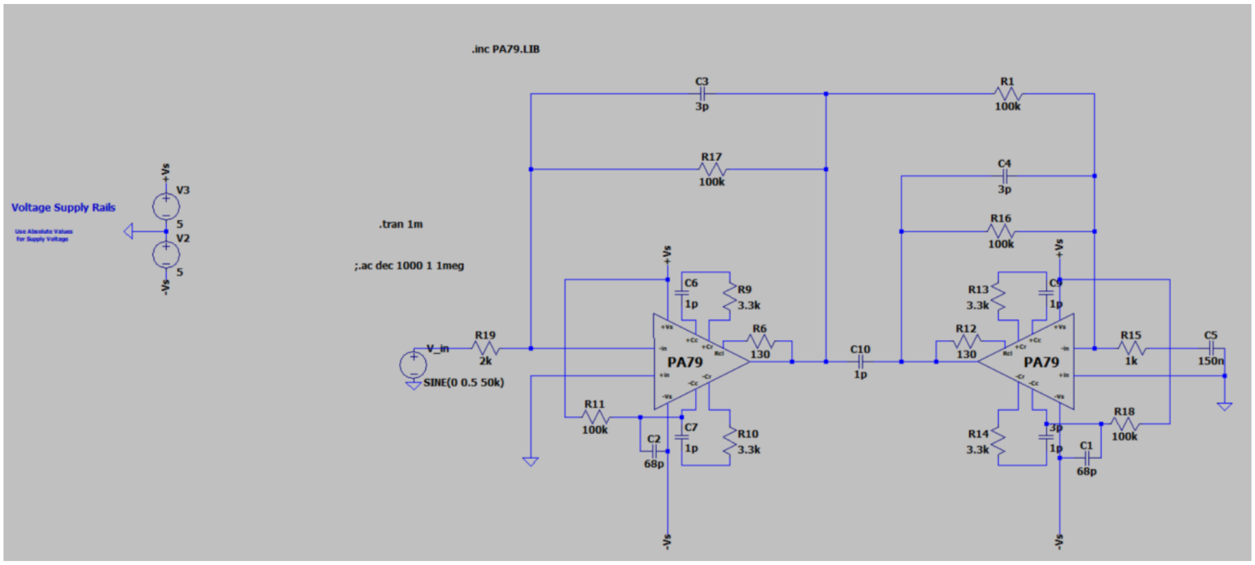


Figure 22: Circuit for bridge configuration of PA79 op-amp.

The circuit was initially modelled in LTspice and simulated at varying input voltage and frequency values. This is demonstrated in the simulation figures below.

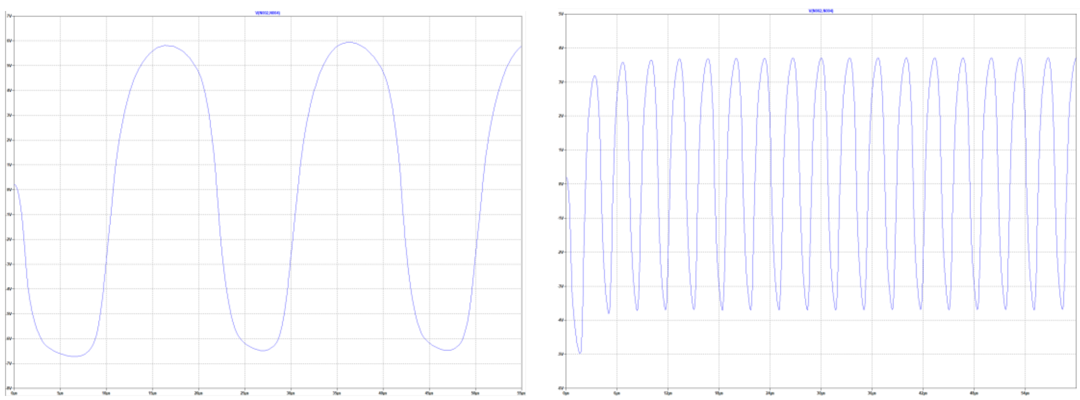


Figure 23: 0.5V input and ±5V supply at 50kHz (left) and 300kHz (right).

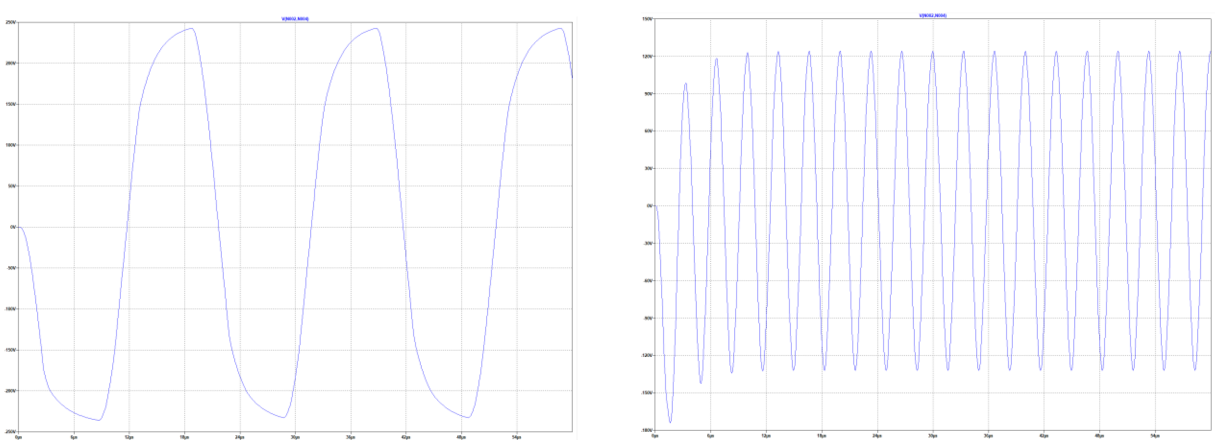


Figure 24: 5V input and ±125V supply at 50kHz (left) and 300kHz (right).

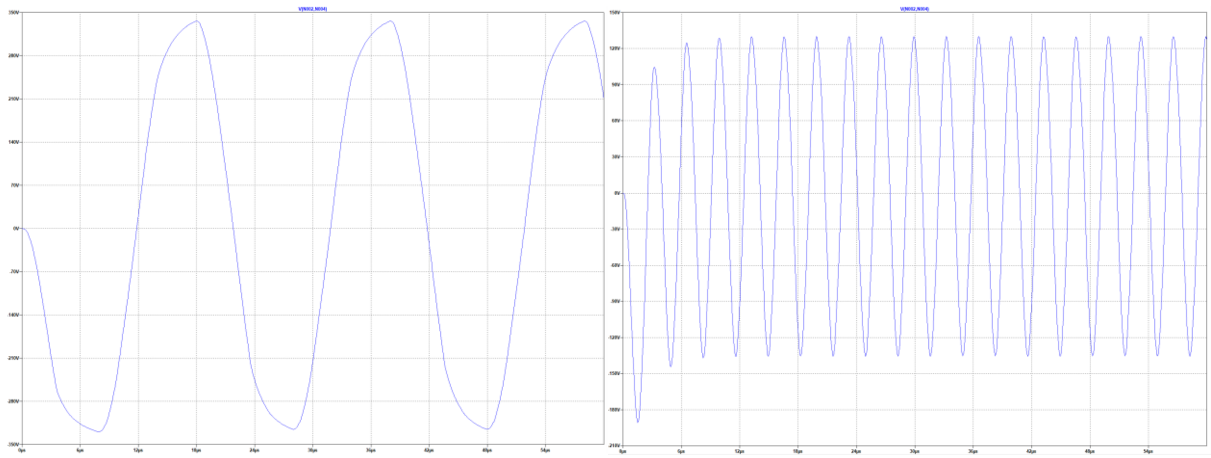


Figure 25: 5V input and ±175V supply at 50kHz (left) and 300kHz (right).

5.5.4.3 Testing

Continuity tests were conducted at every circuit node and connection, followed by successful amplification of a 0.5V input to a 25 V_{P-P} output during circuit performance testing. This can be seen in Figure 26 . However, it exhibited sensitivity to positioning and was unable to perform at varying frequencies and voltages, likely due to interconnection issues, which could be resolved by implementing a PCB design.

Figure 26: Oscilloscope reading for 0.5V input.

5.6 Measurement

5.6.1 Relevant requirements

The following requirements are relevant to the current and measurement functions of the design. This includes the measurement of the output voltage and current for both AC and DC, as well as the thermal measurement and over-temperature protection.

Requirement ID	Short Description
09	The device must be capable of output voltage adjustments of as little as 0.05V.

10	The device must be capable of supplying up to 10 mA of current over the full range of AC and DC outputs.
17	The current limit is tuneable between 1 and 10 mA, using steps of ~2 mA.
21	The device will shut down if internal temperature exceeds 80˚C.

5.6.2 DC Voltage Measurement

DC voltage measurement was implemented using a voltage divider circuit, as shown in Figure 29. This scales the voltage to a maximum voltage of ~5V to ensure compatibility with the maximum 5V input voltage of the Arduino microcontroller (although it can withstand voltages of up to 6V without damage).

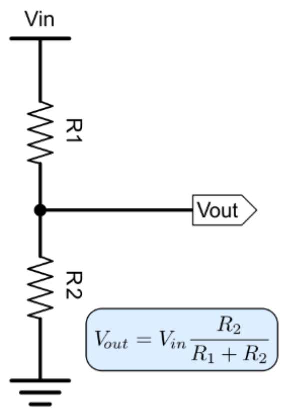


Figure 27: Voltage divider circuit [15].

The voltage measurements were performed prior to the combination of the different DC module outputs. This made it possible to size the voltage divider to maximise the specificity of each reading without additional switching or digital potentiometers. The resistors were sized according to the voltage divider calculation $V_{out} = V_{\text{in}} \cdot \frac{R_2}{R_{1+}R_2}$.

The resistor values for the HV subcircuit, which has a maximum output voltage of 200V, were as follows:

$$R_1 = 220k\Omega, R_2 = 5.6k\Omega$$
$$V_{out,max} = 200V \cdot \frac{5.6k\Omega}{220k\Omega + 5.6k\Omega} = 4.965V$$

The resistor values for the MV subcircuit, which has a maximum output voltage of 80V, were as follows:

$$R_1 = 100k\Omega, R_2 = 5.6k\Omega$$
$$V_{out,max} = 80V \cdot \frac{5.6k\Omega}{100k\Omega + 5.6k\Omega} = 4.24V$$

The resistor values for the LV subcircuit, which has a maximum output voltage of 30V, were as follows:

$$R_1 = 100k\Omega, R_2 = 22k\Omega$$

$$V_{out,max} = 30V \cdot \frac{22k\Omega}{100k\Omega + 22k\Omega} = 5.23V$$

The DC voltage measurement circuit can be seen in Figure 28.

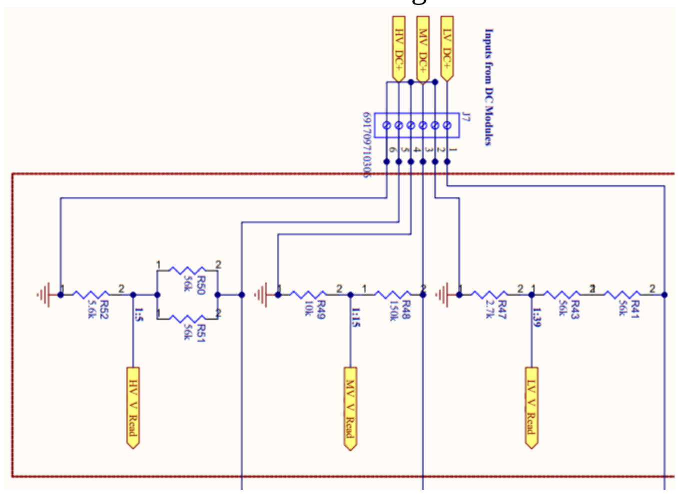


Figure 28: Voltage divider circuit for each of the DC module voltage measurements.

The specific resistor values were selected based on the resistors already available to the team. For the HV module, the required value was split across two resistors to prevent overheating of the resistors.

The required 0.05V deviations for the output require a similarly precise measurement system, however the resolution achieved by each of the modules is given by:

$$ADC\ Resolution = \left(\frac{V_H - V_L}{2^n}\right) \therefore$$

$$LV: \left(\frac{30-0}{2^{10}}\right) = 0.0293V/bit$$

$$MV: \left(\frac{80-0}{2^{10}}\right) = \frac{0.078125V}{bit}$$

$$HV: \left(\frac{200-0}{2^{10}}\right) = 0.195V/bit$$

Therefore, only the low voltage circuit has the required precision to measure the desired 0.05V.

5.6.3 DC Current Measurement

After extensive component research, it was determined that there were no available current sensing ICs with the necessary sensitivity to accurately measure 10mA of current.

The chosen design approach was to implement high-side current sensing, which involves measuring the current on the high side of the load. This was chosen over the low-side current sensing method due to the capacitive nature of the MEMS load.

Figure 29 shows the DC current measurement circuit for the power supply design with a 10mA output current limit.

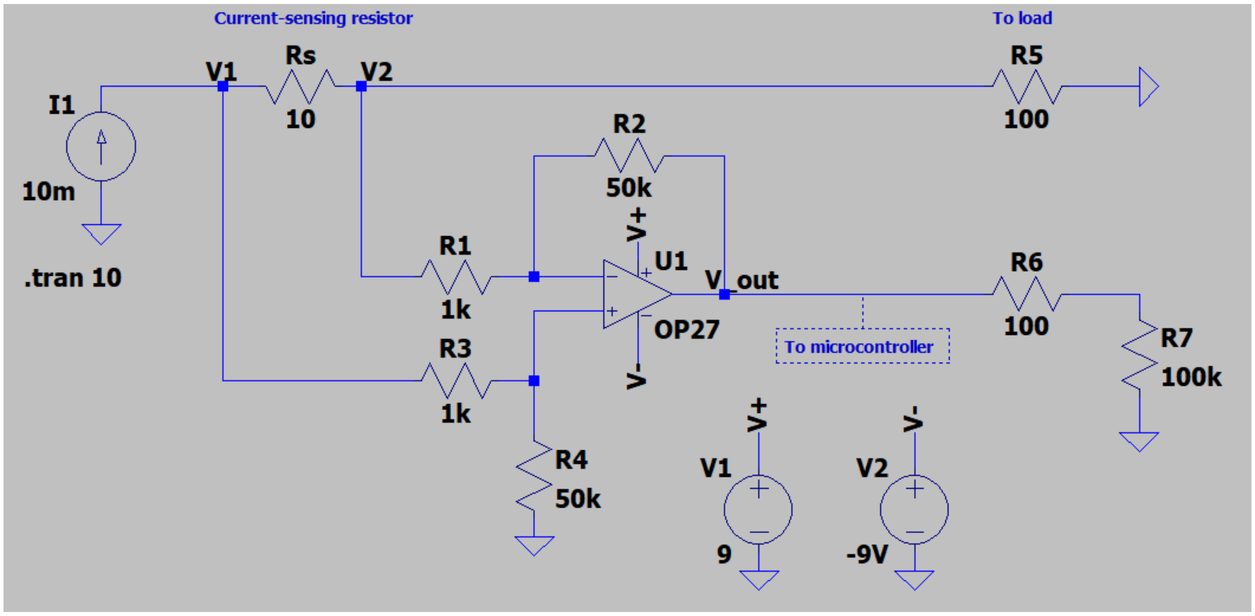


Figure 29: DC current measurement circuit (default 10mA output current limit).

The circuit consists of a 10Ω current-sensing resistor placed in series with the load on the high side. The voltage drop across the 10Ω current-sensing resistor goes to a differential amplifier circuit, consisting of an op-amp and 2 pairs of resistors, R_1 and R_2. This voltage drop is amplified with a gain of $\frac{R_2}{R_1} = \frac{V_{out}}{(V_1 - V_2)}$.

The op-amp output voltage is proportional to the current according to the formula:

$$V_{out} = (V_1 - V_2) \cdot \frac{R_2}{R_1}$$
$$= I_{DC} \cdot R_S \cdot \frac{R_2}{R_1}$$

This voltage is sent to the microcontroller, which activates a relay switch circuit that cuts off the output to the load if the current limit is exceeded (corresponding to a voltage of 5V). The current measurement is performed by converting this voltage to current using this formula:

$$\mathrm{I}_{DC} = \frac{V_{out}}{\mathrm{R_s}} \cdot \frac{\mathrm{R_1}}{\mathrm{R_2}}$$

The tuneable current limit requirement of the design is achieved by adjusting the R_2 resistor values via digital potentiometers to change the R_2/R_1 ratio. The resistor values were chosen such that the op-amp output voltage was 5V when the current limit was reached to activate the relay circuit. Using a fixed R_1 value of 1kΩ, it was calculated that R_2 would range between 50kΩ and 500kΩ to vary the output current limit between 10mA and 1mA, respectively. The calculations are shown below.

$$10\text{mA} = \frac{5V}{10\Omega} \cdot \frac{1\text{k}\Omega}{R_2} \rightarrow R_2 = 50k\Omega$$

$$1\text{mA} = \frac{5V}{10\Omega} \cdot \frac{1\text{k}\Omega}{R_2} \rightarrow R_2 = 500k\Omega$$

The simulation results of the circuit for various load currents are shown in the below figures.

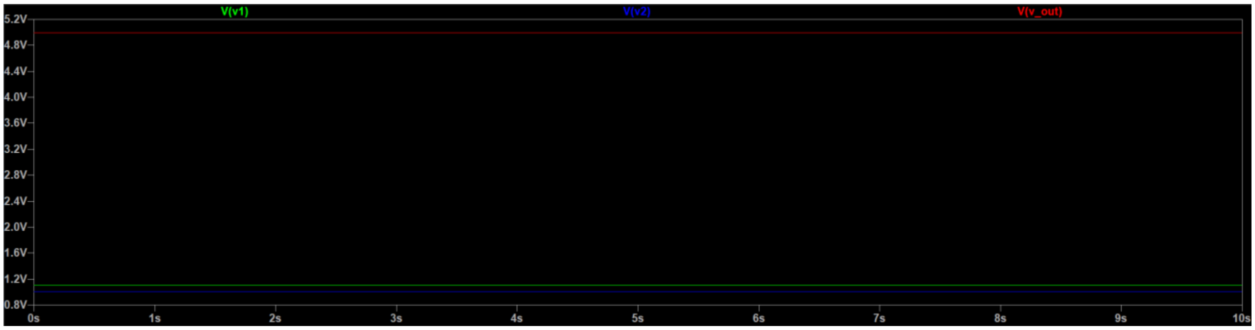


Figure 30: DC current measurement circuit simulation (10mA load current).

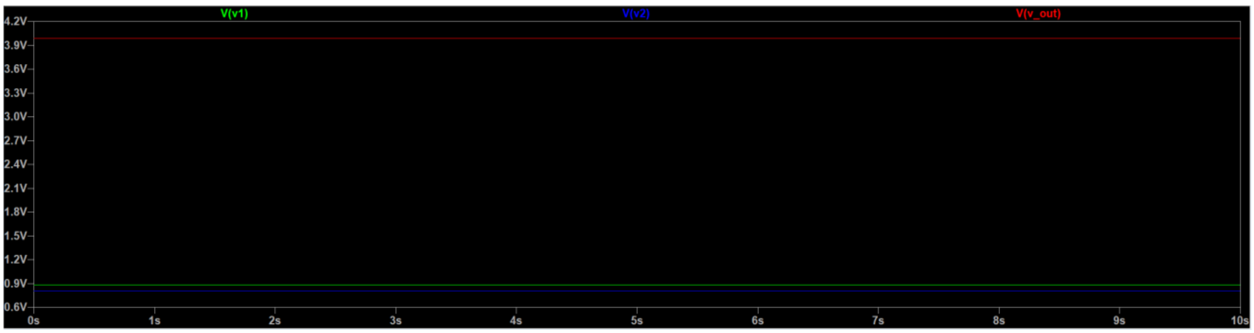


Figure 31: DC current measurement circuit simulation (8mA load current).

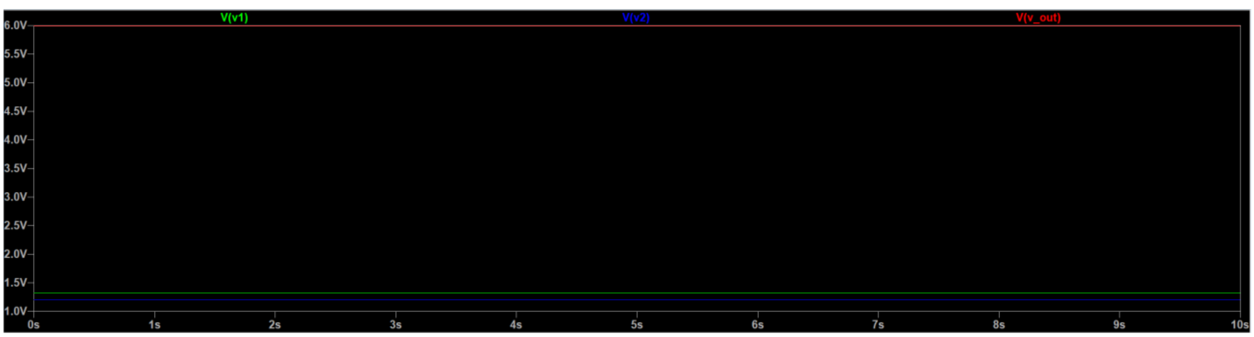


Figure 32: DC current measurement circuit simulation (12mA load current).

In Figure 30, 10mA is sent through the current-sensing resistor, producing a V1 voltage of 1.1V, V2 voltage of 1V and an op-amp output voltage of 5V. These values align with the derived formula as shown below, thus confirming the functionality of the circuit.

$$V_{out} = (V_1 - V_2) \cdot \frac{R_2}{R_1} = (1.1V - 1V) \cdot \frac{50k\Omega}{1k\Omega} = 5V$$

In Figure 31, the load current is decreased to 8mA, below the 10mA output current limit. This produces a V1 voltage of 884.3mV, V2 voltage of 804.5mV and op-amp output voltage of 3.99V, which is below 5V and thus does not activate the relay switch circuit. This is confirmed in the below formula.

$$V_{out} = (V_1 - V_2) \cdot \frac{R_2}{R_1} = (0.8843V - 0.8045V) \cdot \frac{50k\Omega}{1k\Omega} = 3.99V$$

In Figure 32, the load current is changed to 12mA, exceeding the output current limit of 10mA. This results in a V1 voltage of 1.33V, V2 voltage of 1.21V and an op-amp output voltage of 6V. This is greater than 5V and thus activates the relay switch circuit, as expected. This is confirmed in the below formula.

$$V_{out} = (V_1 - V_2) \cdot \frac{R_2}{R_1} = (1.33V - 1.21V) \cdot \frac{50k\Omega}{1k\Omega} = 6V$$

The chosen op-amp model was the Microchip Technology MIC920YC5-TR Operational Amplifier, which has a gain-bandwidth product of 80MHz, supply voltage range of 2.5-9V, 500 uA supply current and 3000V/us slew rate [16].

The chosen potentiometer model was the Microchip Technology MCP4018T-104E/LT Digital Potentiometer IC, with a resistance range of 5-100 kOhms, 7-bit resistor network resolution, I2C digital interface, operating supply voltage range of 1.8-5.5V and operating supply current of 80uA [17].

5.6.4 AC Voltage Measurement

For both the AC voltage and current measurement, the output was first sent to a full-bridge rectifier. This produced a DC voltage with the same amplitude as the AC output. This output can be used to calculate the voltage using the same voltage divider logic as above. The full-bridge rectifier, DF06MA-E3/45, was selected as it met the required voltage rating, was a through-hole component, and was low-cost. The AC voltage measurement circuit and simulation are shown in Figure 33.

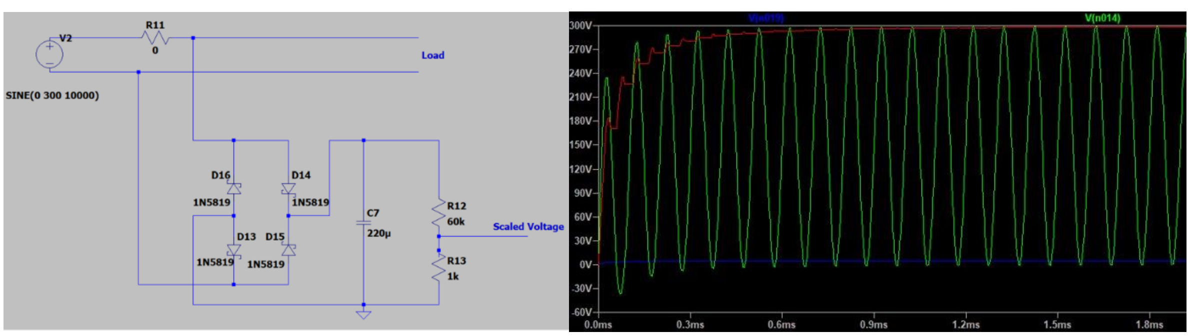


Figure 33: Model of AC voltage measurement (left) and simulation output (right).

A voltage divider ratio of 1:60 to ensure that even if the AC voltage exceeded $200V_{RMS}$, the microcontroller would not receive a voltage greater than 5V. However, by using the microcontroller's ADC and only a single circuit for all AC voltages, the fidelity and precision of the measurement was reduced. The resolution of the voltage measurement can be calculated as:

$$ADC\ Resolution = \left(\frac{V_H - V_L}{2^n}\right) = \left(\frac{282 - 0}{2^{10}}\right) = 0.2753V/bit$$

The project brief specified that the voltage must be adjustable by 0.05V intervals. As the AC measurement is not this precise, even if the adjustment meets this specification, the system will not. This can be improved by using a higher-performance ADC in the next iteration of the design. An ADC with 16 bits would be able to have the required resolution. However, due to budget constraints, it was decided that an additional ADC would not be included in the first prototype.

5.6.5 AC Current Measurement

The AC current measurement circuit is an amalgamation of the full-bridge rectifier and the DC current measurement system. Similar to the DC current measurement, the circuit underwent numerous iterations due to technical difficulties soldering the op-amp and programming the digital potentiometers required to make the op-amp system variable. The final circuit used in the prototype involves a simple voltage divider circuit after the voltage across the current-sensing resistor is rectified, as seen in Figure 34.

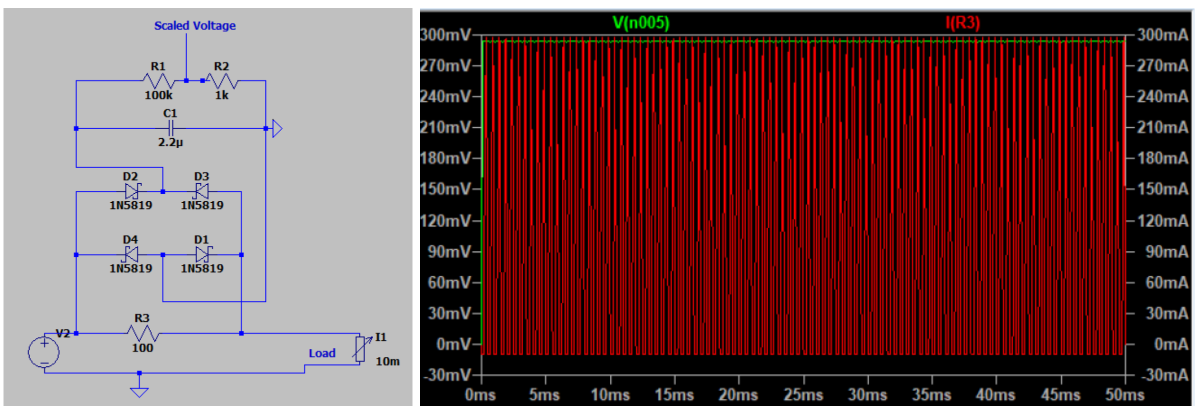
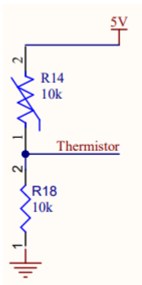


Figure 34: AC current measurement system model (left) and simulation (right).

The scaled voltages can be directly used to calculate the current through the current-sensing resistor. As the system current is quite low, a relatively large current-sensing resistor was used to ensure that the measurement could be read without introducing any power loss issues.

5.6.6 Thermal Measurement

To ensure that the system does not overheat, a simple thermistor circuit was used to monitor the internal temperature of the enclosure. This consists of an 10kOhm NTC (negative temperature coefficient) thermistor in a voltage divider circuit, as seen in Figure 35. The measured voltage is then converted to a temperature reading using the code below.




```
void temp_check() {
  // reads the thermistor, calculates the temp
  Vo = analogRead(Thermistor); //Reads voltage
  R2 = R1*(1023.0 / (float)Vo - 1.0);
  logR2 = log(R2);
  T = (1.0 / (c1 + c2*logR2 + c3*logR2*logR2*logR2));
  T = T - 273.15;         //Calculates Temperature
  Serial.print("Temp: "); //for fault finding
  Serial.print(T);
  lcd.setCursor(17,0);    //additional display
  lcd.print(T);           //for protoyping
```

```
unsigned long currentMills = millis();
// flashes LED if getting too hot, solid on
//if the overheating protection enabled
if(T>= Temp_Limit) {                //Temp_Limit =80
  ledState = HIGH;                  //LED on
  protectionState = HIGH;           //shuts off output
} else if(T>=Temp_Warning) {        //Temp_Warning =70s
    protectionState = LOW;
    if(currentMills - prevMills >= interval) {
      prevMills = currentMills;
      if(ledState == LOW) {         //LED Blinks
        ledState = HIGH;
      } else {
      ledState = LOW;
    }}}
else {···
digitalWrite(ledPin,ledState); ///visual indication
digitalWrite(Thermal_Protection,protectionState);
                                    // to output switch
```

Figure 35: Thermal measurement circuit (left) and code (right).

The input to the safety relay is set to high through the Thermal_Protection pin seen in the above code. This activates the same relay circuit as discussed in the protection section, cutting off the output to the loads.

5.6.7 Testing

Due to difficulties soldering the op-amp and programming the digital potentiometers as well as the lack of a delivered custom PCB, the first prototype of the DC sensing circuit involved a simplified circuit, which is shown in Figure 36.

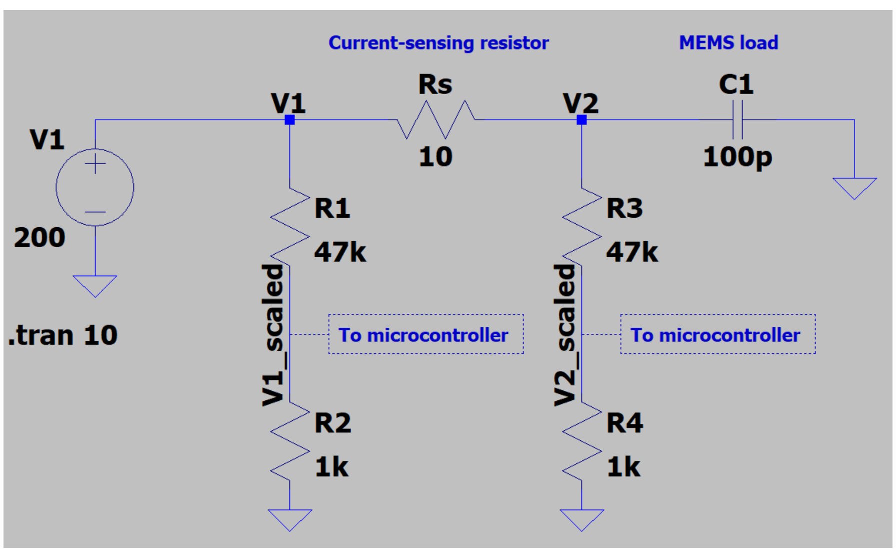


Figure 36: Simplified DC current measurement circuit.

Similar to the originally designed circuit, this consists of a 10Ω current-sensing resistor placed in series with the load on the high side. The voltage across this resistor goes through a 47kΩ /1kΩ voltage divider circuit (instead of the op-amp), the values of which were calculated assuming a maximum output voltage of 200V and maximum 5V input to the microcontroller. This scales the voltage to a value between 0-4.17V before it is sent to the microcontroller. The load current is calculated in the microcontroller code by scaling the voltage up to its original value and dividing this by the 10Ω resistor, as shown in the following formula.

$$DC\ current = \frac{(V1_{scaled} - V2_{scaled}) * 48}{R_s = 10\Omega}$$

The circuit was connected to a 12VDC supply and its ability to calculate the current was confirmed, producing results consistent with readings from a multimeter. The code output showing the scaled voltages, calculated current and transistor signal to the relay circuit is shown in Figure 37.

```
Scaled Voltages: 0.26V, 0.25V --> Voltage drop: 0.01V
DC Current: 0.05A
Transistor signal: HIGH
```

Figure 37: Code output of DC current measurement circuit.

Testing of the thermal monitoring and protection was performed in part at the design review. It was demonstrated that the thermistor circuit could monitor the temperature and turn on an LED when it exceeded the preset limits. Further testing to ensure the consistency of this behaviour at 80˚degrees will be required.

5.7 Protection

5.7.1 Relevant requirements

The following requirements are relevant to the overcurrent protection function of the design.

Requirement ID	Short Description
02	The device must incorporate output protection that switches off output voltage if the output current exceeds the set current limit (as per Req-17).
03	The device must incorporate output protection capable of response times in the tens (10’s) of milliseconds after current limit detection.

5.7.2 Circuit

If the current is detected to exceed the set current limit, the microcontroller is programmed to send a signal to a transistor which triggers a relay, cutting off the output to the MEMS device. This is achieved via an NPN (negative-positive-negative) relay switch circuit, in which the relay coil is triggered by a NPN transistor, as shown in Figure 38 (the 10kΩ resistor was omitted from the design for simplicity). The collector is connected to the relay, the emitter is connected to ground and the base is connected to the 5V digital output of the microcontroller.

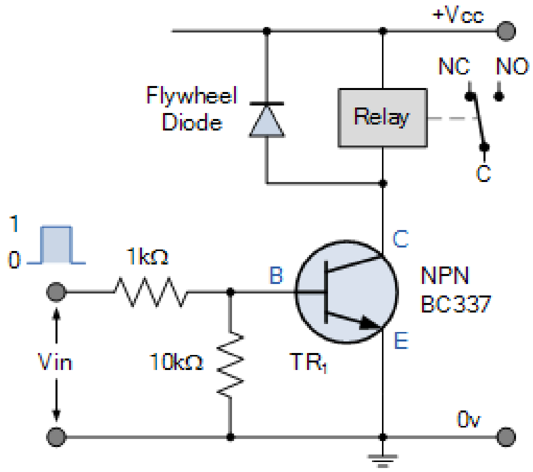


Figure 38: NPN relay switch circuit [14].

When there is negative or zero voltage applied to the base terminal, there is no collector current and therefore the transistor acts like an open circuit, so no current flows through the relay coil. However, if sufficient voltage is applied to the base, current flows from the base to the emitter and the transistor acts like a short circuit, energising the relay coil. A flywheel diode is placed in parallel with the relay to protect the circuit from voltage spikes caused by the collapse of the coil's magnetic field when the transistor is turned off [18].
The chosen transistor model was the 2N2222A NPN transistor which has the following properties [19]:

- Collector-Base voltage: 75V
- Collector-Emitter Voltage: 40V
- Emitter-Base Voltage: 6V
- Collector Current: 0.6A
- Power Dissipation: 0.5W

The chosen diode model was the Vishay 1N4004 General Purpose Plastic Rectifier which has a forward current of 1A, forward voltage of 1.1V and maximum reverse voltage of 400V [20].

The chosen relay model was the Amphenol AWHSH112DM00G General Purpose Relay, which has the following properties [21]:

- Coil nominal voltage: 12VDC
- Coil nominal current: 30mA
- Pull-in voltage: 9V
- Drop-out voltage: 0.6VDC
- Maximum allowable voltage: 15.6V
- Maximum operating time: 10ms – this satisfies Req-03 regarding the protection response time in the tens of milliseconds.

This relay switch circuit is utilised due to the relay's relatively high trigger current of 30mA. Drawing this current directly from the microcontroller could overload it, as each pin can only supply 40mA and the overall microcontroller's capacity is limited to approximately 300mA. To resolve this, the relay switch circuit is utilised, as it requires significantly less current from the microcontroller to produce the required 30mA current for the relay.

5.8 Human Machine Interface (HMI)

Requirement ID	Short Description
Req-06	Enclosure must be constructed to have sufficient rigidity, protection from electric shock and fire/elevated temperature.
Req-25	The human-machine interface must allow users to set device parameters including the output signal type, frequency and voltage, as well as the output protection current limit.

5.8.1 Enclosure Design

A 3D model prototype of a case was initially designed (shown in left Figure 39), however due to the constant changes in the expected dimensions of the final circuit, it was not printed in time for the demonstration.

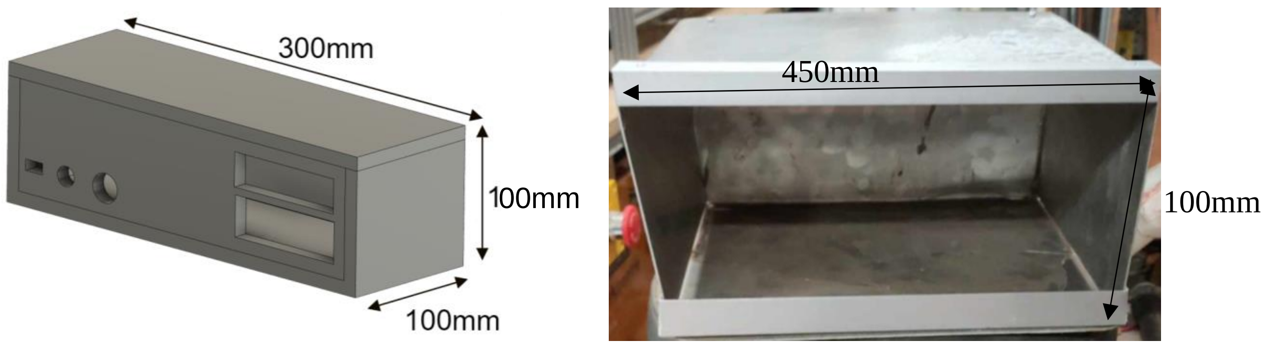


Figure 39: Left: CAD model of initial case design. Right: Prototype metal case prior to final assembly.

An alternative case was repurposed from aluminium sheet metal prior to the demonstration, as seen on the right. However, time did not permit the production of the front face which was essential to hold and support the user interface components such as the switches and LCD screen. Additionally, further work was required to ensure that the container was structurally sound. As such, it was not included within the demonstration.

5.8.2 HMI

The HMI encompasses the user inputs and displays the outputs of the system. The initial design brief specified much of the system to be digitally tuneable, which is enabled through the HMI.

There were three main user inputs to the system; tuning of a mechanical potentiometer, adjustment of a physical switch, or input from the rotary encoder. The mechanical potentiometers were used for the DC module tuning. The physical switches were used for key safety and control parameters, such as whether the interlock or the entire system's power was on. The rotary encoder was used to input the values for all other parameters, such as modulation control and frequency, as seen in Figure 40 showing the designed physical HMI.

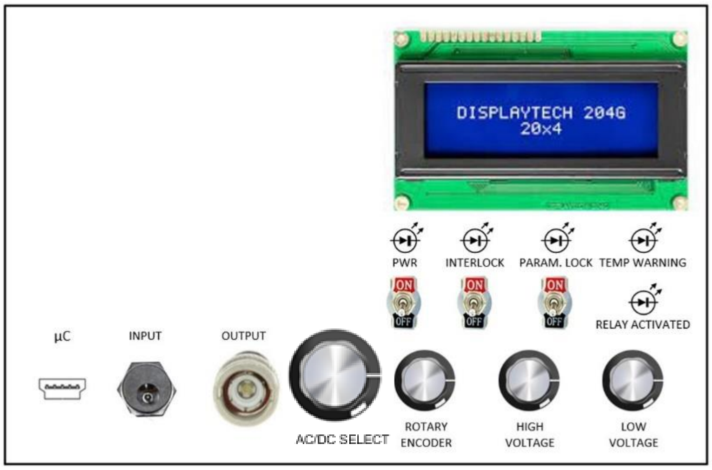


Figure 40: Designed HMI with user inputs and outputs.

The I/O block of the system is shown in Figure 41.

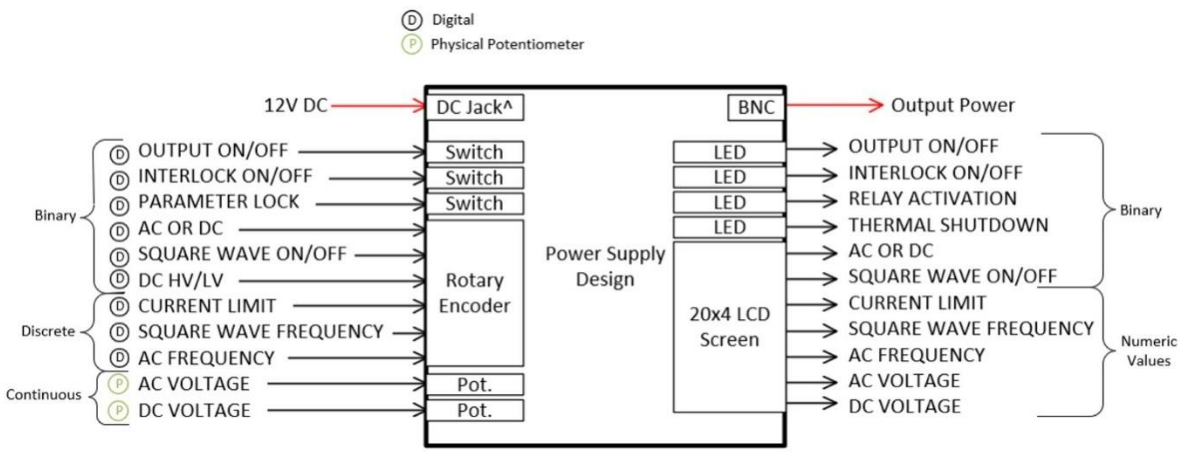


Figure 41: I/O block of the system.

The LCD was designed to act as a menu screen, with the below logical flow-diagram supporting the code. The full code is included with the design deliverables.

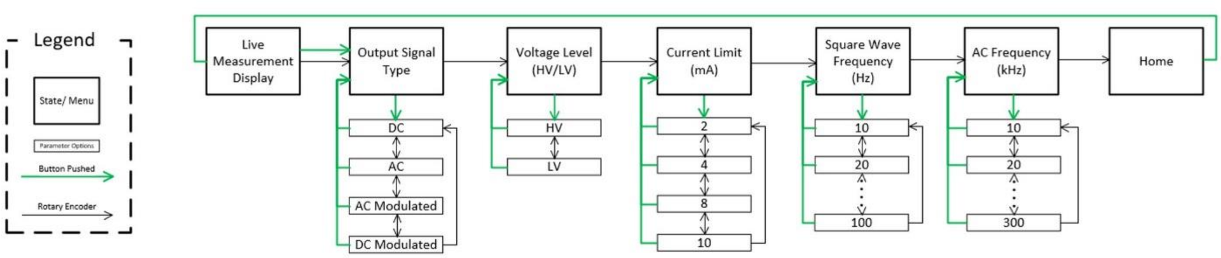


Figure 42: Flow diagram for LCD menu screen.

The menu screen and associated switches were tested at the design review and confirmed that the system worked as expected.

6. Final Design

The final top-level schematic can be seen in Figure 43. To aid in the modular design and readability of the schematic, each of the above design elements have been collated into the lower-level schematics represented by the green boxes. The entire schematic has been included in Appendix A, as well as a high-quality copy in the GitHub repository.

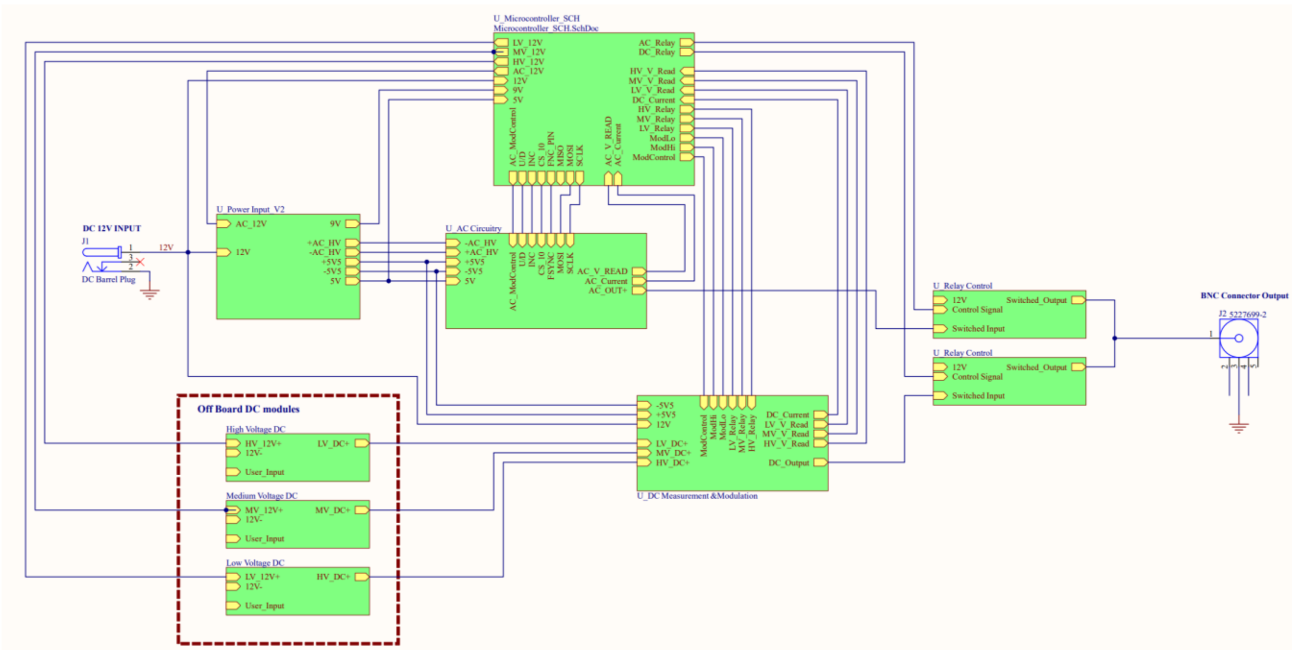


Figure 43: Schematic of entire power supply unit.

Although a PCB was not delivered in time for the demonstration, an initial PCB was still designed for the project deliverables. The 3D view of the PCB may be seen below, where the main sections corresponding to the modules above have been delineated by a silkscreen box.

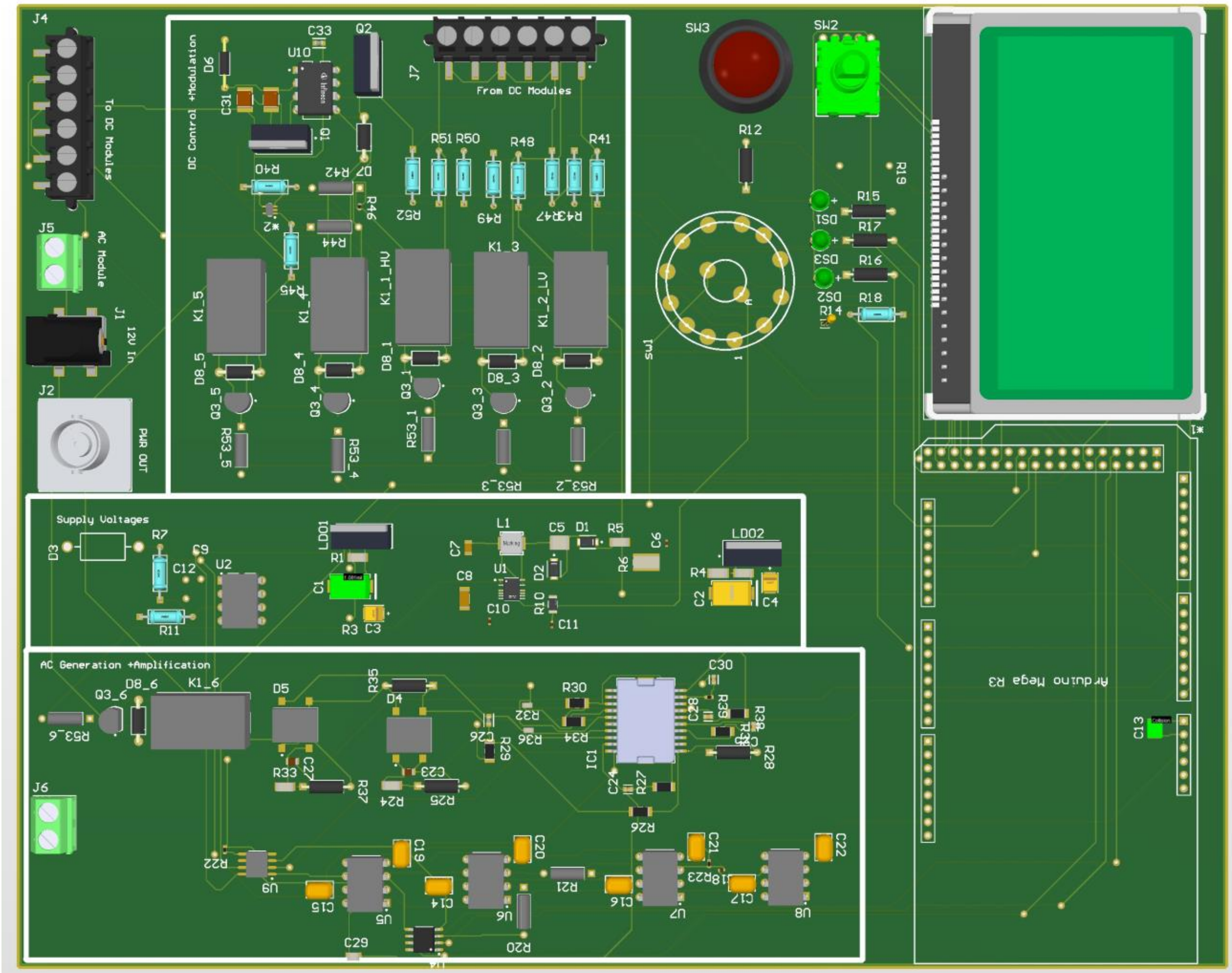


Figure 44: PCB layout of entire power supply.

To pre-emptively reduce the impact of the AC circuitry on any noise or coupled traces, it was kept to the base left of the board. In future designs, this section of the board could be a separate PCB to further decouple any issues presented by the relatively high frequency circuit.

Additionally, as the user interface (including the switches, LEDs and LCD screens) would be mounted to the enclosure with only wires attaching the components to the board, they were all kept together to reduce the number of wired sections of the final connected system.

6.3 Final Cost

The final costs of the design have been collated in Table 4. A full bill of materials and associated costs for each module can be found as a design deliverable in the GitHub repository.

Table 4:Cost summary of design as per different modules.

Module	Price ($ AUD)
Low Voltage Generation	54.48
Low Voltage DC Regulation	16.96
Dual DC Supply	32.39
Waveform Generator and AC Pre-Amplification	96.60
AC Voltage Amplification	104.33
Parameter measurement	26.22
Switching and modulation	16.42
HMI Interface	25.28
Miscellaneous	5.68
Total:	**378.36**

6.4 Construction/Assembly/Synthesis

In this section, the construction, assembly, and synthesis of the power supply design will be addressed. Due to the time constraints, a hybrid delivery approach was chosen, combining prototyping on protoboards and a PCB design in CAD for the final design demonstration and report. The rationale for this approach and a few of the encountered challenges and creative solutions will be discussed.

<u>Delivery Rationale:</u>

After completion of the SWOT (Strengths, Weaknesses, Opportunities and Threats) analysis early in the semester, it was clear that the team did not possess extensive experience in circuit design, let alone PCB design. Due to the limitation of the project to a single semester, it was determined that it was possible to develop and deliver a single PCB delivered before the deadline, if all resources were allocated to this. However, this would leave insufficient time for the prototyping of circuits and components due to the extended lead time of the PCB delivery and the time required to develop the circuit schematics, become familiar with the PCB CAD software, and integrate everything together. As a result, there was low confidence in the functionality of the developed PCB if this design approach was used.

To resolve this, the decision to focus resources on the development of a design on protoboards was chosen. A disadvantage was that the delivered design would be much less likely to meet all the requirements of the design (specifically the noise and signal integrity requirements). However, this greatly improved the confidence in the potential for the final design to show progress towards the design requirements and with a few additional weeks of development, produce a design that fully satisfied the client requirements.

<u>Construction & Assembly:</u>

This phase of the project was primarily carried out after Week 10, due to the time required for the finalisation and delivery of the components. After the arrival of the components, it was apparent that a majority of them were not available in packages that could be easily implemented on protoboards and would instead require dedicated PCBs to be implemented correctly. This was unfortunately not an option due to budget and time constraints, so alternative solutions had to be devised to test some of the more critical components and ensure their viability in the final design PCB.

The protoboards of various subcircuits are shown in the below figures, showing the soldering and wiring connections of components.

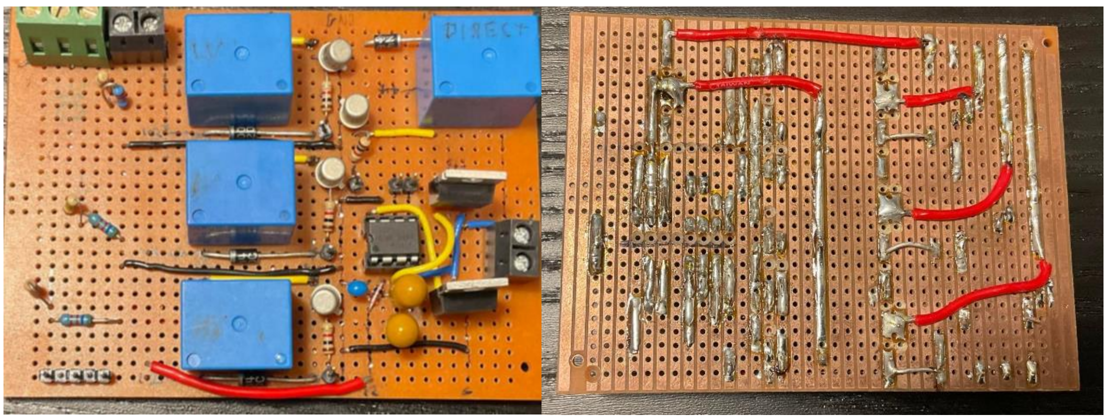


Figure 45: Protoboard of the DC modulation and measurement circuits.

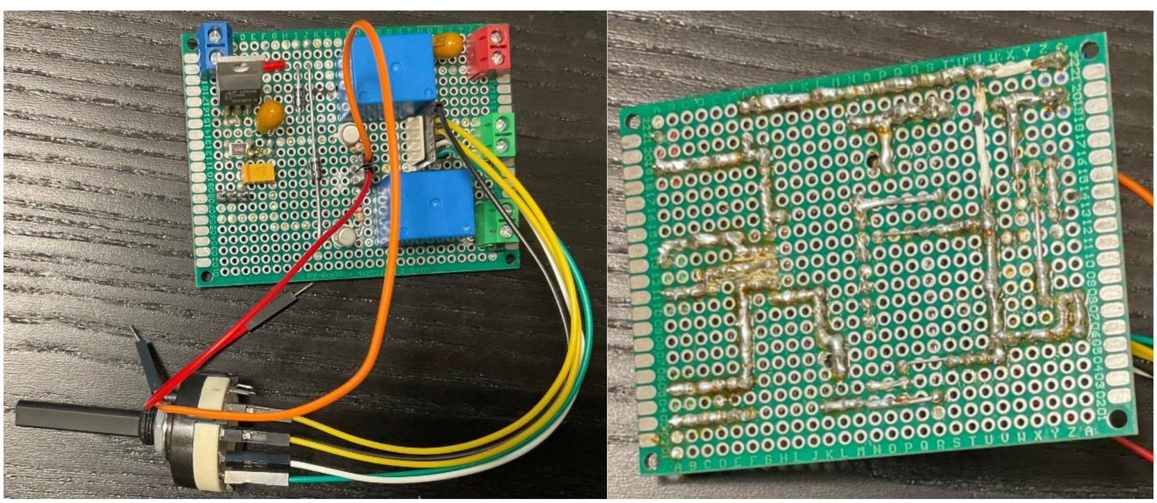


Figure 46: Protoboard of the power selection and safety circuits.

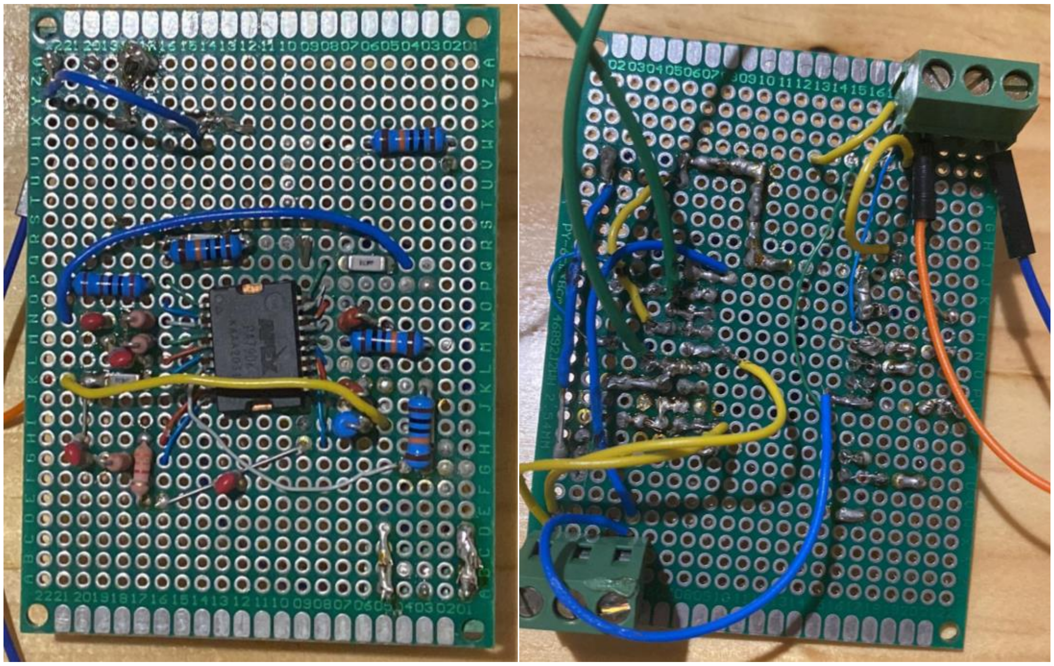


Figure 47: Protoboard of AC amplification circuit, featuring the PA79 op-amp.

Figure 48 shows an example of the breadboard testing undertaken for an op-amp, with trace leads soldered on to it to enable testing.

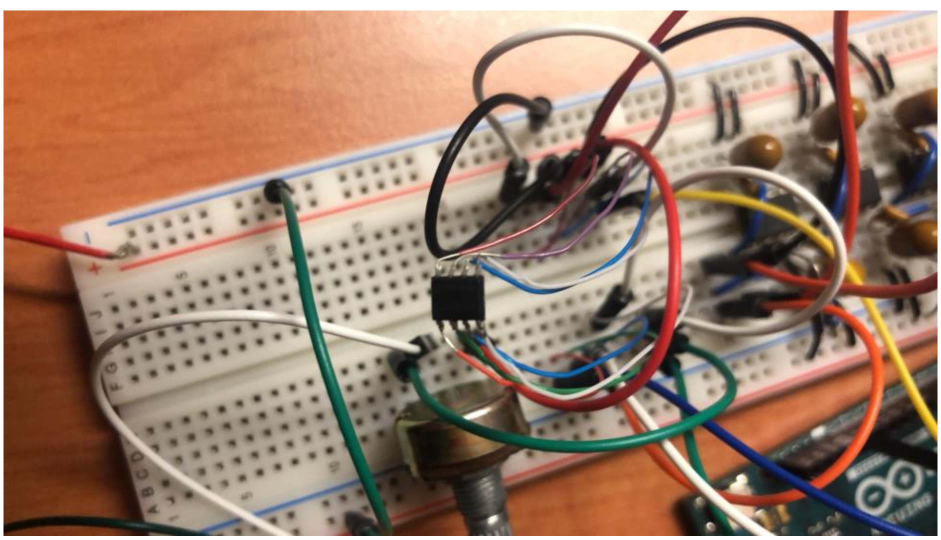


Figure 48: Breadboard testing of an op-amp with trace leads soldered on for testing.

Unfortunately, the full system build could not be completed due to challenges in circuit troubleshooting, and the implementation of the code alongside a user interface was not complete in time for the demonstration. Nonetheless, the team maintains the belief that this was the correct approach, as prioritising a PCB design would have likely led to similar issues, which would be more challenging to resolve on a PCB. The team is confident that with additional development time, the prototype boards would have closely met the requirements of the design, representing a substantial first step in the design process.

6.5 Safety Issues and Mitigations

A risk assessment was conducted to identify, assess and mitigate the hazards associated with the assembly and testing of the power supply. Proactively identifying and addressing these hazards minimises the likelihood of major alterations to the design in the future (which can incur significant costs and project delays), enhancing the overall design quality and enabling smooth execution of the project.

The inherent risk rating, which is the risk posed by the hazard if no control strategies are put in place, is calculated by considering the following factors:

- Consequence of hazard exposure, ranging from 1 (Noticeable) to 100 (Catastrophe)
- Likelihood of hazard exposure resulting in the identified consequences, ranging from 0.1 (Practically impossible) to 10 (Almost certain).
- Exposure to the hazard, in terms of frequency (ranging from Unheard of to Continuous) or the number of people involved (ranging from one person to a crowd).

The consequences (C), likelihood (L) and exposure (E) values are multiplied together to calculate the inherent risk rating. Control strategies are then recommended to mitigate the risk of the hazard, reducing its inherent risk value to a residual risk value. The hierarchy of control measures are as follows:

- Elimination (EL)
- Substitution (SU)
- Engineering (EN), Isolation (IS) and Guarding (GD)
- Administrative (AD), Training (TR) and Inspection (IN)
- Personal Protective Equipment (PPE)

Table 5 shows the hazards with the 5 highest risk ratings and their mitigating control strategies.

Table 5: Top 5 hazards and mitigation strategies.

Identified hazard	Risk description	Inherent risk rating				Type of control measure	Control measure description	Residual risk rating			
		C	L	E	=			C	L	E	=
Energy release	Components such as capacitors are required in the design. These components store and release energy, posing an energy release hazard for people working on and in the vicinity of the equipment.	50	3	5	750	IN, AD, PPE	All team members to be made aware that capacitors may be live for a period of time after disconnecting the system. Components to be inspected and tested for faults prior to use. Electrically rated gloves to be worn when handling components.	50	1	2	100
Slip and trips	Trip hazards such as power cords or dropped objects may be present as people outside the team utilise the space.	25	6	5	750	AD, IN	Workspace to be inspected prior to use and any identified hazards are to be removed or highlighted. Workspace to be kept tidy during work and upon completion.	25	1	2	50
Carcinogens	Team members will be exposed to solder flux.	25	6	3	450	AD, TR, PPE	Soldering to only be conducted by trained team members and safety glasses and gloves to be worn to reduce exposure when working. Extraction fans are also to be utilised. First aid and running water is available.	25	32	2	150
Burns	Soldering requires	25	6	3	450	TR, PPE	Gloves to be worn where				

	high heat. Worker is exposed to the hot soldering iron as well as the solder itself and the component being soldered. Heat guns may also be utilised to test components. Finally, equipment may be hot due to heat losses during operation.						practicable. Soldering training/induction is also required for any team member undertaking soldering tasks. Locations of first aid equipment and water to be identified prior to commencing work.				
240V equipment	The power supply to be constructed is required to provide 200V AC and DC. This could present an electric shock hazard if faulty and/or isolation/earthing is disconnected. The power supplies provided for testing are powered from the mains and may present a similar hazard.	25	3	5	375	AD, EN	Equipment to be visually inspected and electrically tested for faults prior to energisation. Equipment to be tested at low voltages initially, with testing of higher voltages to be conducted under supervision.	25	1	2	50

6.6 Ethical Issues

One identified ethical issue was the sourcing of components for the design. While it is beneficial to favour low-cost components to stay within the allocated budget and give the design a competitive market advantage, it is also important to consider the human rights issues associated with such low-cost components, such as working conditions and fair wages. This was mitigated by sourcing local components where possible and only purchasing components from reputable suppliers.

Another ethical issue was the environmental footprint of the design. The manufacturing and disposal of components can result in adverse environmental consequences, such as pollution and resource depletion. This was mitigated by prioritising components with longer lifetimes to reduce the need for replacements, and components with high power efficiencies to minimise the energy consumption of the design.

6.7 Issues Identified During Design Process

One issue encountered during the design process was the project budget. The team was allocated $350 from the project partner for the entire design. This restricted the selection of components, as high-performance components were found to be more expensive. Therefore, careful selection of components was necessary to achieve a balance between performance and cost-effectiveness. A component spreadsheet was created to log all purchased components and monitor the team's current expenses.

Another issue was the timeline constraint. It was required that the design prototype and all associated project files needed to be delivered by the Week 13 deadline. Although a well-structured project schedule had been created, there were several issues which disrupted the project timeline. For example, extended lead times for components delayed the commencement of prototype construction, limiting the time available for testing and further design iterations.

6.8 Top 5 Risks and Mitigations

A comprehensive risk analysis was conducted at the start of the project, leading to defined mitigation strategies. These strategies were documented in a risk register, which were reviewed at the project's midpoint to validate the continued relevance of the risks and the mitigation measures. The top five identified risks along with their mitigation strategies are presented in Table 6.

Table 6: Top 5 risks and mitigations.

Risk	Description	Mitigation Strategy
Technical challenges	The team has limited technical knowledge and experience in the field of power electronics and microelectronics design, which could result in suboptimal or non-	The team allocated different areas of power supply design to each member for in-depth research, as well as researching current industry practices. This allowed a deeper gain of knowledge for the whole team. Technical queries were conducted with the client as well as obtaining additional support from the unit

	functional design outputs.	coordinator, client and meetings with the facilitator for additional clarification and guidance.
Budgetary Constraints	The overall cost of the power supply system might exceed the allocated budget of $350.	The team has implemented cost-tracking mechanisms to ensure the budget is maintained. Regular budget reviews, resource optimisation, and leveraging cost-effective sourcing options for components were essential strategies throughout the project. Mouser Electronics was primarily used to source components due to its wide product range and low costs; and a bulk order was placed to reduce shipping costs.
Schedule Delays	Delays may occur due to an unclear scope, undefined tasks, ambiguous scheduling and delayed information gathering.	The team employed a Gantt chart for the entire project to track milestones and progress. The project controller was responsible for ensuring management and adherence to the schedule. This was regularly addressed in team meetings to ensure adjustments were made as necessary to achieve critical tasks in a timely manner.
Team Member Availability	Team members may not be available due to unforeseen circumstances or commitments to other units, thus impacting project continuity.	A comprehensive communication plan was maintained to ensure all team members are well-informed about each other's situations. Well-defined roles, cross-training, and knowledge sharing further mitigate the risk of extended unavailability of critical team members.
Limited High-Voltage Testing Access	Limited access to high-voltage testing facilities, as well as lab access, leading to delays in the testing and validation of critical components. Acquiring lab access may require a long waiting period.	The project team proactively communicated with the unit coordinator to gain access in advance. Contingency plans were developed, such as using other lab facilities on campus (Makers Lab and Soldering Lab), to allow for alternative testing options.

6.9 Design Outputs

All project files were stored in a Microsoft SharePoint folder to facilitate easy access and collaboration among the team members. The file path is: https://uniwa.sharepoint.com/sites/ELEC5552SEM-22023-Team14/Shared%20Documents/Team14

The design output files were shared with the project partner via a GitHub repository, along with a physical prototype of the design and a demonstration of its functionalities. The GitHub repository link is: sjoppich/ELEC5552-Team-14: ELEC5552 project files (github.com). The description and location of the design output files are shown in Table 7.

Table 7: Design output files.

File description	Purpose	Location in SharePoint
Operating and Maintenance Manual	Provides details regarding the specifications, operation, maintenance and troubleshooting of the power supply.	10. Design/06. Design Outputs/ Operating and Maintenance Manual
Altium Circuit Schematics and PCB Layout Files	Depicts the layout and interconnection of components within each module of the design, as well as the PCB layouts.	10. Design/06. Design Outputs / Altium Schematics+PCB
Block Diagram	Provides a high-level visual representation of the design, showing the interconnections between the different modules.	10. Design/06. Design Outputs/Block Diagram
LTspice Simulation Files	Models the performance of the individual modules of the design.	10. Design/Design Outputs /Simulation Files
Arduino Code	Provides the necessary logic for the microcontroller to control the design's various modules and components.	10. Design/Design Outputs /Code
Bill of Materials (BoM)	Itemises and details all the components utilised in the design and their associated costs.	10. Design/06. Design Outputs/Bill of Materials
Requirements Review	Provides a summary of the finalised project requirements and their testing methods, whether they were met, and learnings.	10. Design/06. Design Outputs/Requirements Review
Reports	Safety analysis, requirements and final report produced by the team.	10. Design/06. Design Outputs/Reports

6.10 Recommendations for Further Development

DC Supply filtering

Further filtering of the output signals is recommended to minimise the switching noise and so allow for finer adjustment fidelity as well as a more stable output. This may be done by tuning of the low pass RC filter as applied to the output of the LV circuit.

Protection

For safety reasons, the protection circuit should ideally be hardware-based and not involve the microcontroller at all, to minimise the risk of malfunction and ensure a fail-safe response. The proposed circuit and simulations are found in Appendix C.

AC voltage amplification

To improve AC output accuracy and reliability, as well as prototyping efficacy, the Apex Microtechnology PA85 op-amp should be used in the next design iteration. The PA85 offers a notably higher slew rate of 1000V/µs and an extended voltage swing of 450V. The complementary improved noise immunity allows the component to better deliver the full V_{RMS} range. As the amplifier bridge only requires a 3.75V amplitude wave to deliver 200 V_{RMS}, more precise potentiometer increments can be used to have a greater degree of control over AC voltage step changes.

The below figure illustrates the PA85 schematic and associated AC waveform.

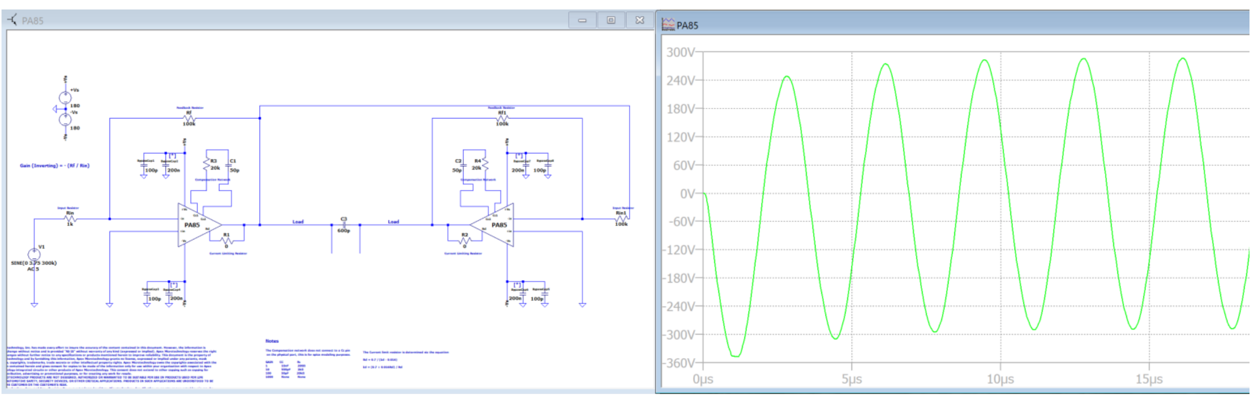


Figure 49: PA85 schematic (left) and AC wave at f=300kHz.

The op-amp reduces the number of external components needed, streamlining both troubleshooting and simulation efforts. The PA85 documentation also provides compensation circuits for different gain settings, thus minimising circuit design and setup time. However, this op-amp exceeds the budgetary constraint, costing $333.

The proposed circuit and simulations are found in the Appendix.

Customised PCB

By utilising a PCB rather than protoboards, lower impedance connections and smaller distances between components can be achieved. This would improve the overall system functionality, as grounding and noise levels would be improved. Additionally, circuity such as the ±175V supply that was not possible to solder onto protoboards could be implemented as shown in the proposed PCB layout in the Appendix.

Utilising a PCB also improves the durability of the design due to the incorporation of printed copper traces, which are more robust than manually soldered connections or wires that may come loose due to vibrations over time. Also, it would allow for cheaper reproduction of the final design should this be desired.

6.11 Community Briefing

The MEMS power supply is an open-source student-designed project which aims to supplement MEMS research by offering a high voltage and frequency range power supply at a substantially lower cost than typical power supplies of similar parameters. As it is tailored to ANFF's needs, it represents the culmination of the potential of student-researcher collaboration at UWA.

Benefits and Features:

- The power supply unit (PSU) can accurately produce DC voltages between 0V and 200V and limit output current with hardware components dedicated to ensuring the safe delivery of power.
- The PSU can accurately produce AC voltages between 0V to 200 V_{RMS} at a range of 50kHz to 300kHz with this being expandable to any desired increment range and wider frequency ranges.
- The PSU can safely interlock components to strictly produce lower voltages of 50V or $50V_{RMS}$.
- The PSU can increment voltages in the range of 0.05V, allowing for the precise tuning of outputs.
- The PSU uses inexpensive, highly available components, which allow for easy part replacement and component modification.
- The PSU uses RoHS compliant components and open-source code.

For further information refer to the Operating and Maintenance Manual or contact Team 14.

6.12 Tenders

The tendering process for the successful implementation of this design requires adequate information about the project's background, requirements, contractor obligations and handover requirements. This will ensure that the design is delivered on time to the specification required by the client and to the client's overall satisfaction. Due to the specialist nature and pricing constraints of the design, the client should look to contract both local and global manufacturers to ensure the delivery of a high quality and affordable unit.

The first tender required to ensure design feasibility is a manufacturing tender pertaining to component availability and PCB production. This will help guarantee low-cost production and feasible maintainability of the design. Due to the bespoke service this design provides, ANFF may wish to commercialise this design, which will be contingent on mass production feasibility.

The second tender should revolve around ensuring proper laboratory testing and validation of the design is conducted. This will ensure the safety and reliability of the device and ensure that users can get a return on their investment. Ensuring that a laboratory that complies with Australian safety and conducts this testing will allow for an easier integration of the device into the ANFF's research suite. As commercialising this device may introduce liabilities to ANFF, it is of paramount importance that the design is signed off by a reputable validation laboratory.

Lastly, a tender pertaining to software validation and ensuring that the design's prescribed code categorically abides by all requirements and safety features. This will ensure the prevention of a Therac-25 type event, reinforcing the reliability of the design. This will also help cement the design's commercial viability and increase the feasibility of commercialisation.

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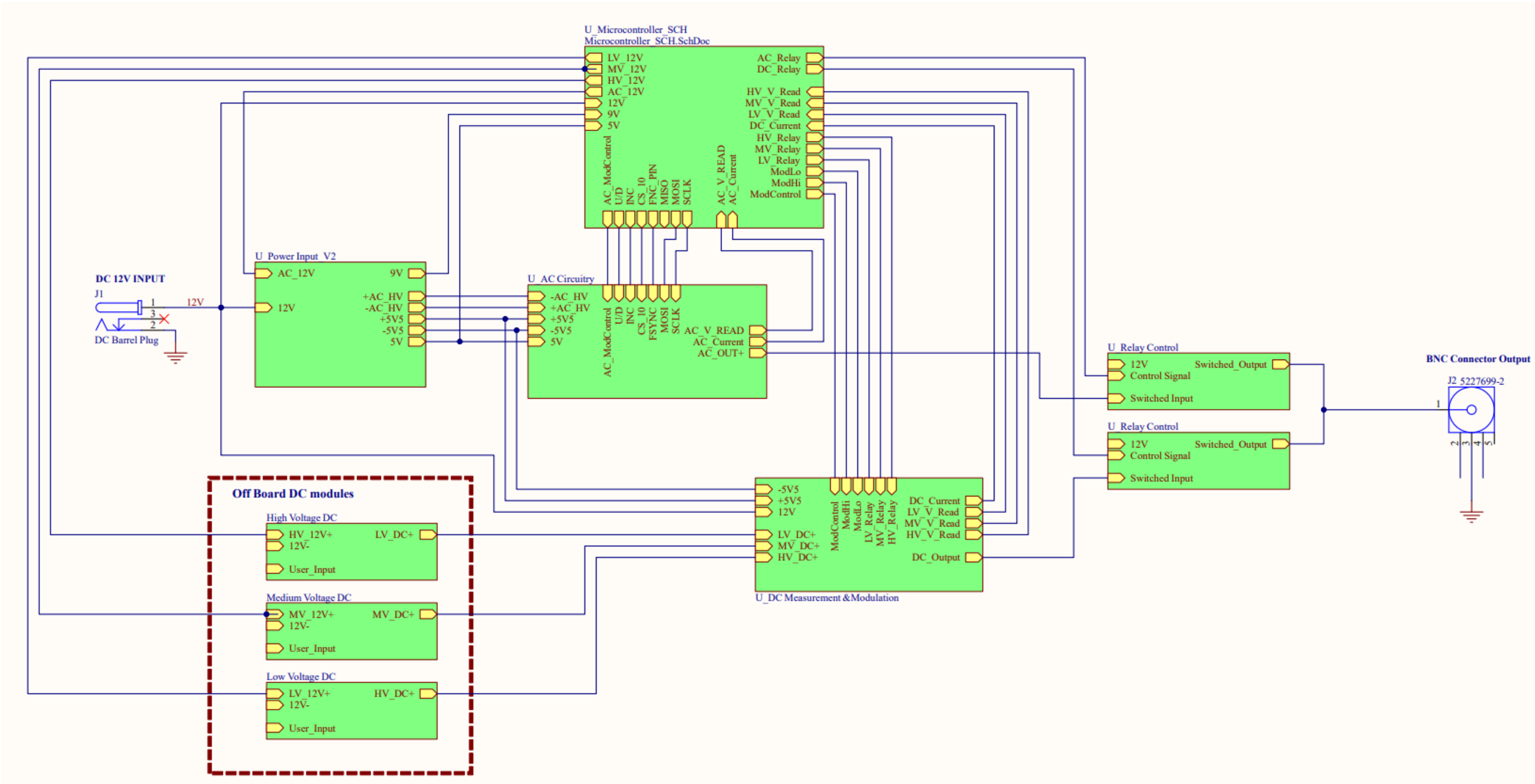
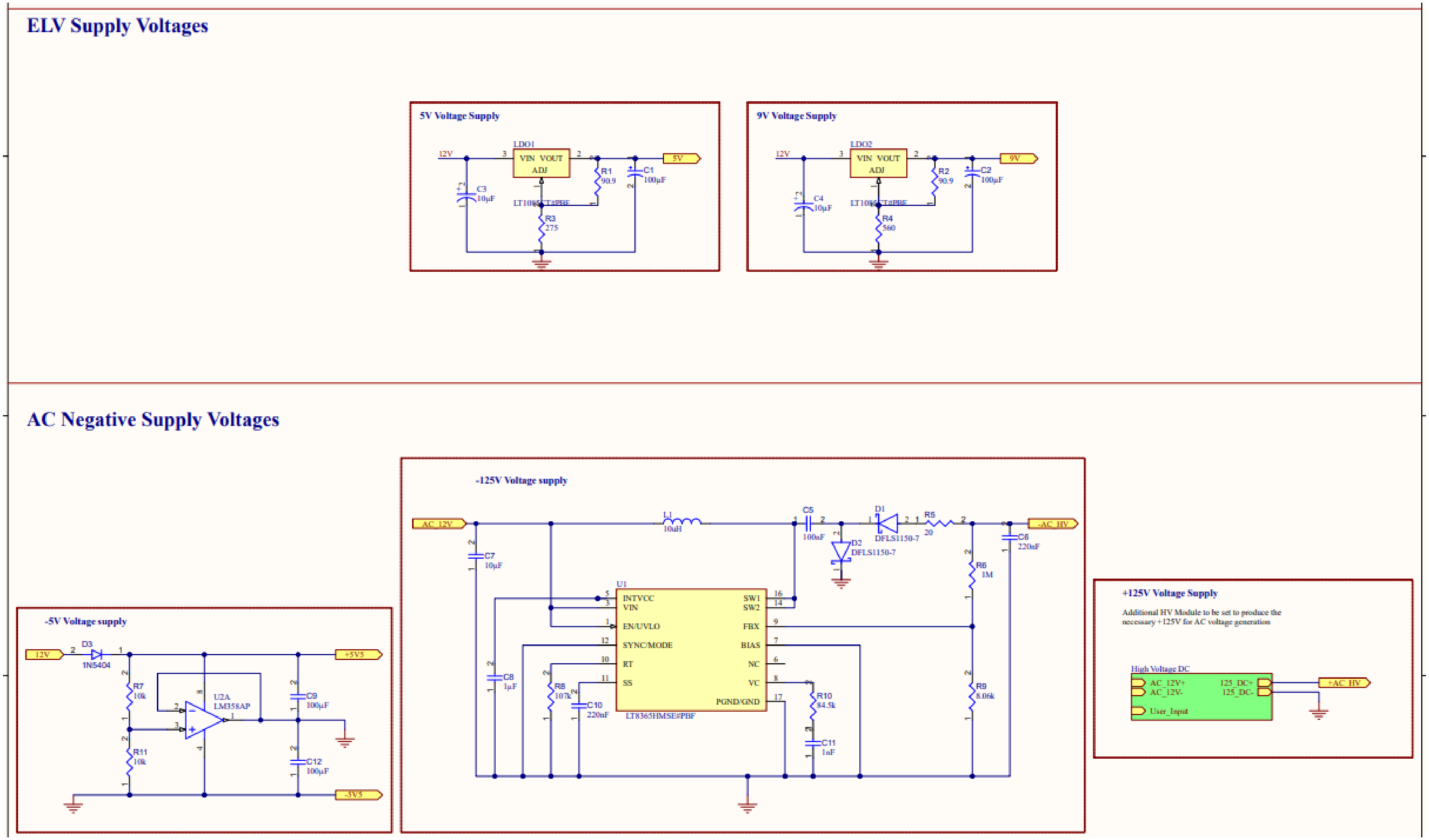
8. Appendices

8.1 Appendix A: Schematic and PCB layout

Overarching Schematic

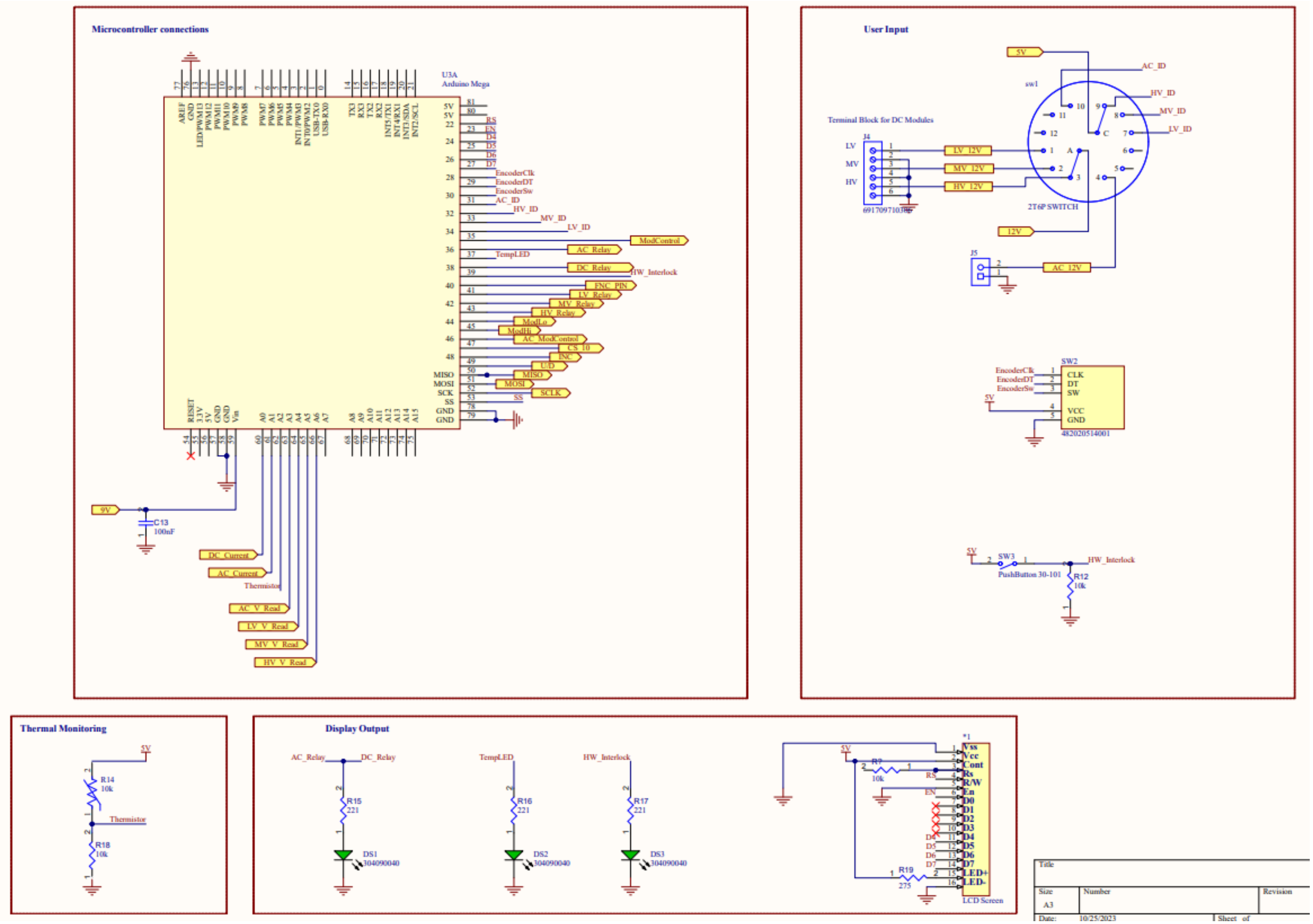


Power Input

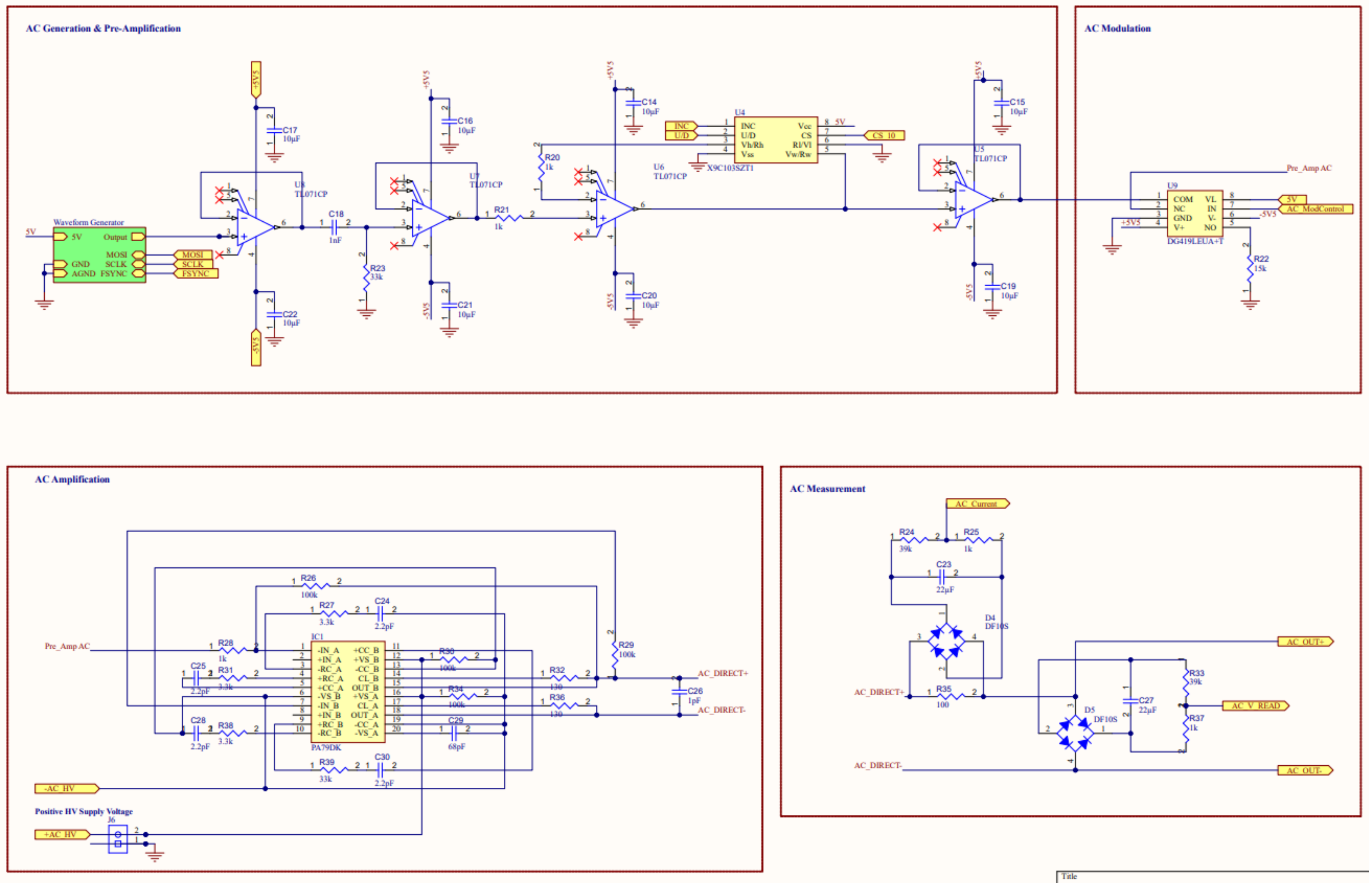


ELV Supply Voltages
5V Voltage Supply
9V Voltage Supply
AC Negative Supply Voltages
-125V Voltage supply
-5V Voltage supply
+125V Voltage Supply
Additional HV Module to be set to produce the necessary +125V for AC voltage generation
High Voltage DC
LT8365HMSE#PBF
LM358AP
1N5404
DFLS1150-7

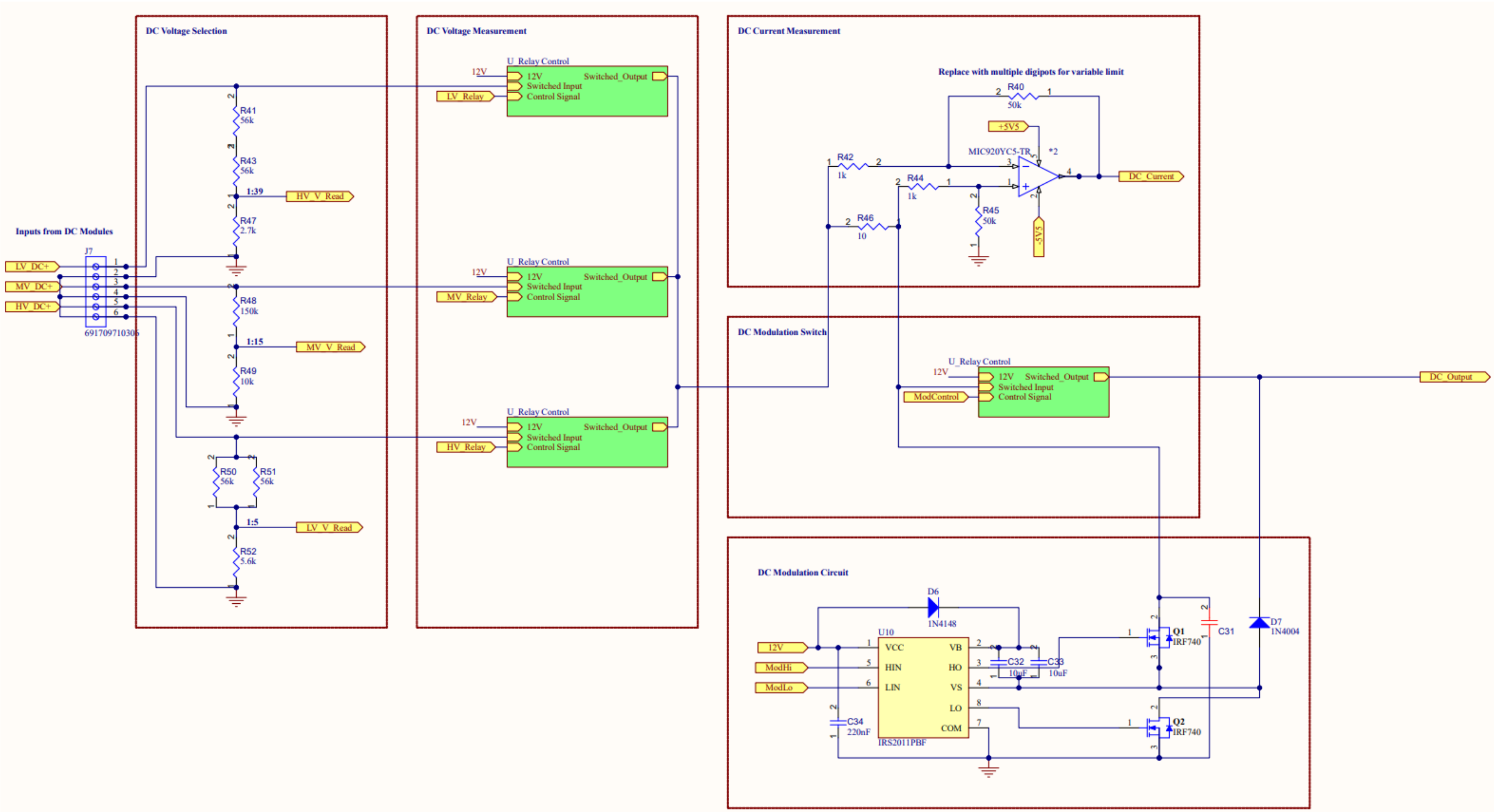
Microcontroller:



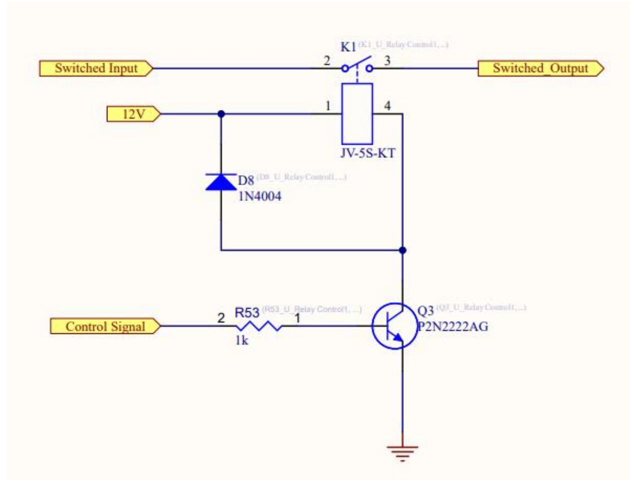
AC Circuitry



DC Measurement & Modulation



Relay Control



8.2 Appendix B: Next Iteration Design Schematics and Simulations

Suggested PCB Layout for -125V Circuit

The below figure shows the suggested PCB layout for the circuit from Analog Devices. The layout and distances between components must be carefully considered in this design. If the paths to some of the components, such as capacitors and inductors, are of too high impedance, the circuit will not perform as desired.

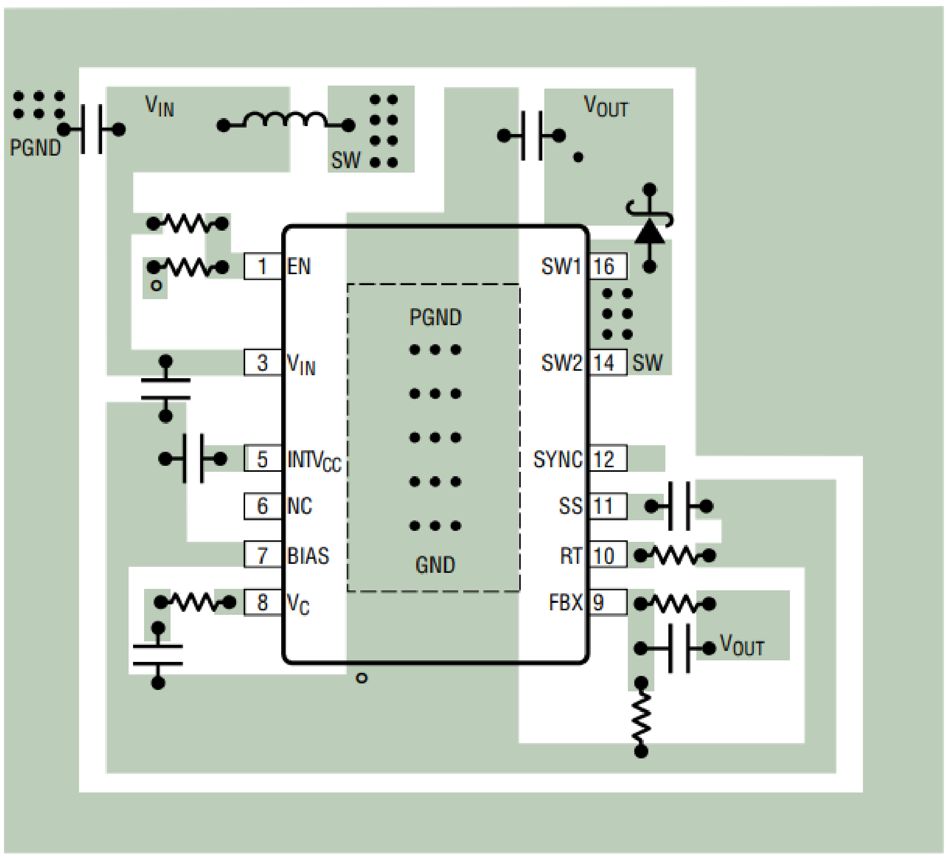


Figure 50: Suggested PCB layout for -125V supply [22].

+/- HV Supply Circuit Simulation with Added Charge Pump for increased Capacity

The below figure shows the suggested circuit for -175V supply to the AC Amplification circuitry. The circuit is modelled in LT Spice, proving the desired voltage of -175V is achieved after 4ms.

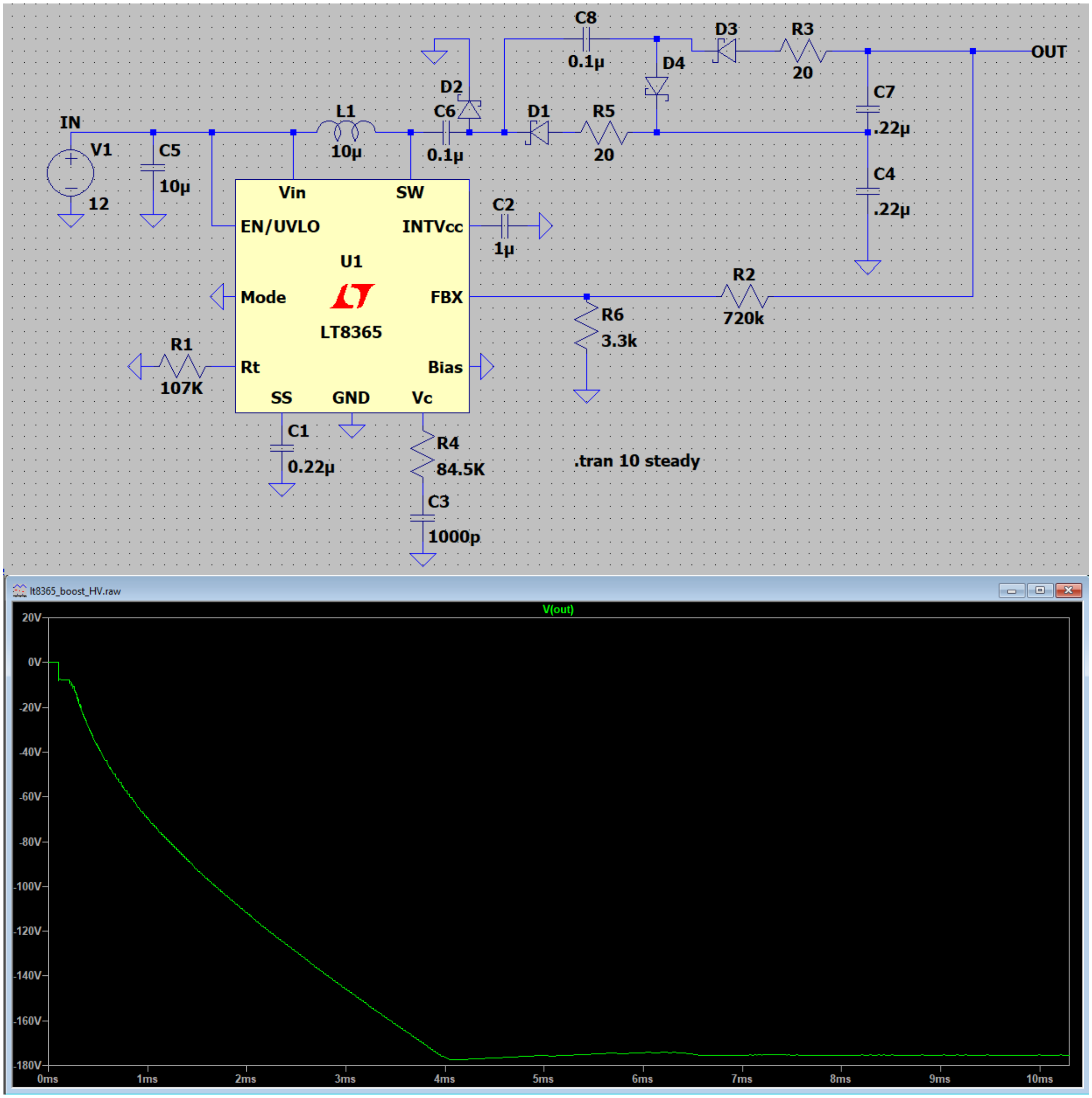


Figure 51: -175V Supply circuit and simulation.

The below figure shows the +175V supply circuit and associated simulation result, proving that the desired voltage is achieved after less than 1ms.

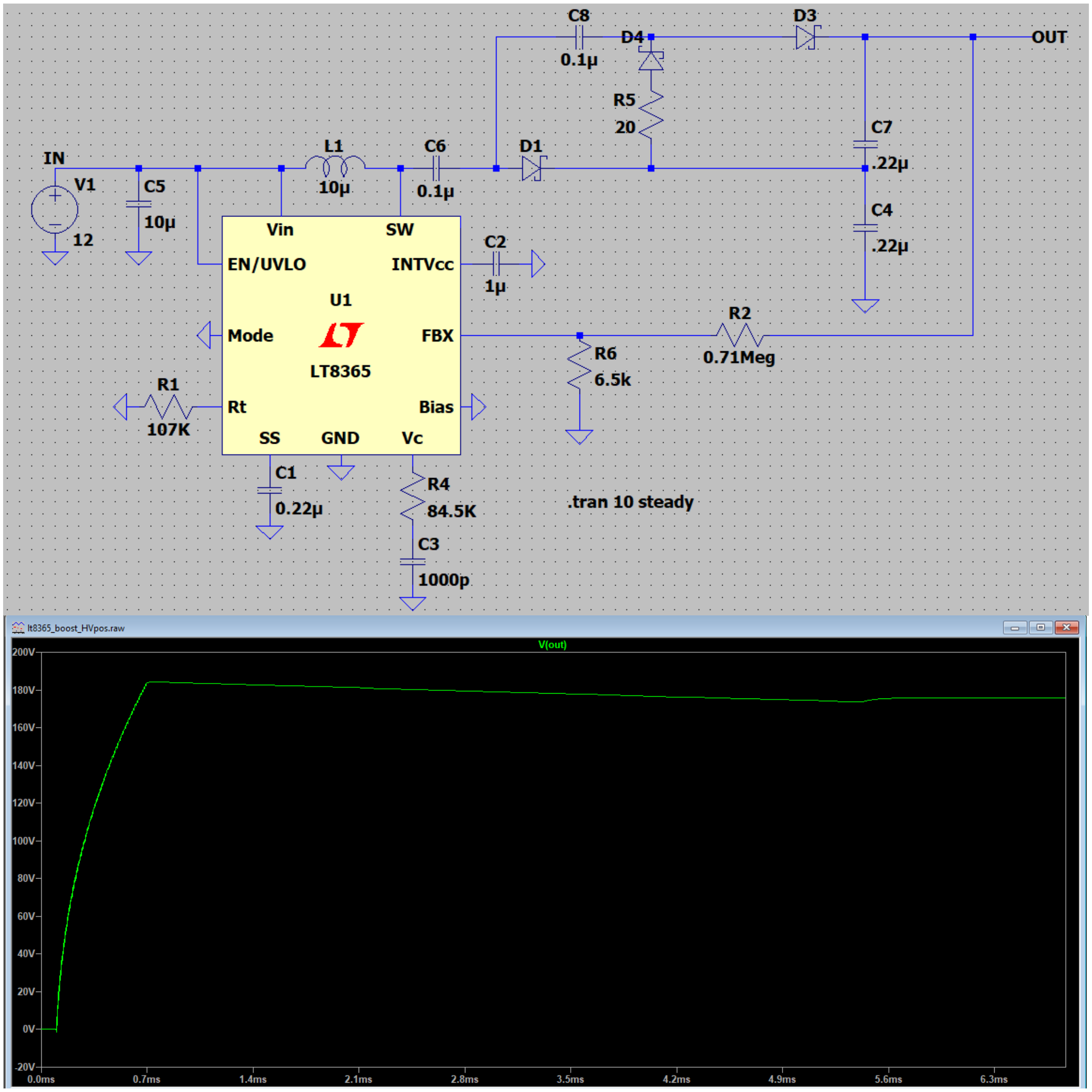


Figure 52: +175V Supply circuit and simulation.

Protection Circuit

Instead of going to the microcontroller, the output voltage of the op-amp is sent directly to a relay with a coil voltage of 5V, which cuts off the output to the MEMS load if the current limit is exceeded (corresponding to a voltage of 5V).

Figure 53 and Figure 54 show the proposed circuit simulations for a 10mA output current limit (R_2=50kΩ), demonstrating the relay switching for a load current of 2mA and 12mA respectively.

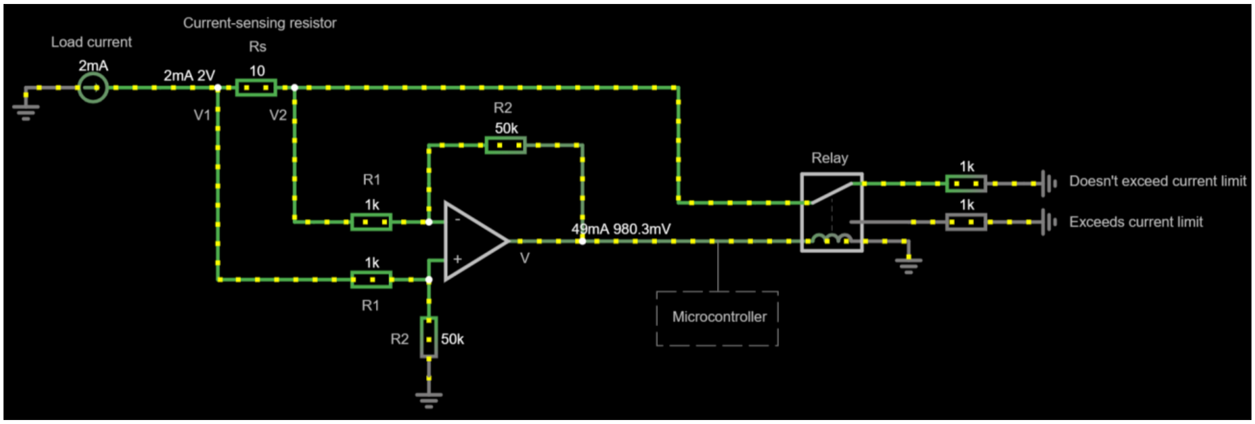


Figure 53: DC current measurement and protection circuit for 10mA output current limit – 2mA load current.

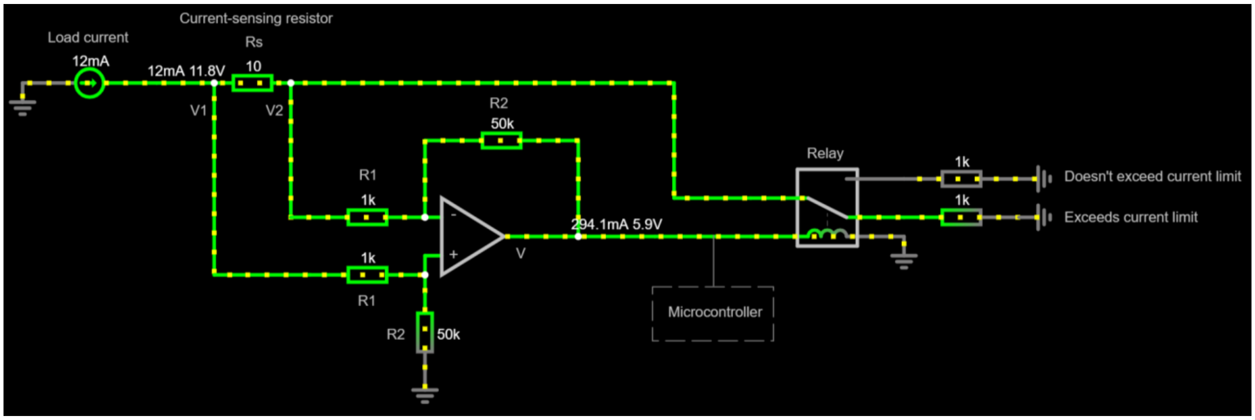


Figure 54: DC current measurement and protection circuit for 10mA output current limit – 12mA load current.

8.3 Appendix C: Requirements Verification and Validation

ID	Requirement Description	Test	Passed	Learnings
Req-01	Design and testing carried out must comply with AS61010.1 (Safety Requirements for Electrical Equipment).	Performing safety tests (such as overcurrent protection, leakage current, grounding, etc.) to ensure compliance with the relevant AS61010.1 safety requirements.	Yes	
Req-02	The device must incorporate output protection that switches off output voltage if the output current exceeds the set current limit (as per Req-17). Protection must be resettable to allow for repeat testing and give visual indication when cut-off is engaged.	Using an oscilloscope to measure the output current under various load conditions and ensure that the output voltage is switched off when the current limit is exceeded.	Yes	The first prototype of the DC current sensing circuit was able to detect the current and send a high signal to the transistor pin if the current exceeded the output current limit.
Req-03	The device must incorporate output protection capable of response times in the tens (10’s) of milliseconds after current limit detection.	Under standard test conditions, an oscilloscope can measure and verify the 1%, 5% and average response times of output protection for various loads are compliant.	Yes	The maximum operation time of the protection relay is 10ms.
Req-04	The device must incorporate a hardware interlock that limits the DC voltage to 100 Volts.	Under standard testing conditions the output terminal voltage should be measured with interlock open to validate 100V limit. Closing the interlock allows voltage up to 200V, testing the output protection by opening the interlock when above 105V.	Yes	The device interlock is 80V after consultation with client as this was deemed sufficient. The functionality was proved during testing.

Req-05	The device must incorporate a hardware interlock that limits the AC voltage to 50V RMS.	Under standard testing conditions, the output terminal voltage should be measured using an oscilloscope with interlock open to validate 50V RMS limit. Closing the interlock allows voltage up to 200V RMS, testing the output protection by opening the interlock when above 50V RMS.	Not Validated	The Ohmic lock on the digital potentiometer in the Low V AC stage needs to be tested to confirm that it never generates a gain that results in $V > 50V_{RMS}$.
Req-06	Enclosure must be constructed to have sufficient rigidity, protection from electric shock and fire/elevated temperature.	Performing thermal, electrical insulation, and mechanical testing to ensure the case can withstand typical lab treatment and accidental mishandling. Further verification using the AS3820 and AS61010.1 Clause 8 guidelines can be performed upon client request.	Yes	Metal enclosure was built and earthed to eliminate electric shock hazards.
Req-07	The device will be designed such that, in the event of any internal failure, the output is disabled (no voltage) and a clear visual indication is given.	Prior to circuit integration into case, an internal failure can be simulated by grounding a high voltage component during operation to ensure detection, output cut-off and isolation occurs.	Yes	Safety relay implemented on the output, actuated through microcontroller.
Req-08	The device must be capable of providing a DC output voltage over the range of 0-200V, adjustable as per Req-09.	Under standard testing conditions, output voltage can be measured and verified throughout the desired range, checking for consistency, accuracy and settling time.	Yes	Capability is achieved and test passed.

Req-09	The device must be capable of output voltage adjustments of as little as 0.05 Volts.	Under standard testing conditions, measuring the AC and DC outputs as desired voltage is changed to confirm minimum adjustment.	No	Circuitry is capable of an adjustment fidelity of <0.1V, but the measurement and readout design cannot display values down to required step-size.
Req-10	The device must be capable of supplying up to 10 mA of current over the full range of AC and DC outputs.	Under standard testing conditions, an oscilloscope can be used to measure the output currents and validate the maximum current.	Yes	Each circuit has been tested and passed.
Req-11	The device must incorporate a switchable output signal amplitude modulator (100% level) using a square wave signal over the range of 10–100Hz for all DC outputs, tuneable as per Req-15.	Under standard testing conditions, an oscilloscope can be used to verify the frequency of the modulating wave (square wave), ensuring the switching speed is sufficient for negligible rise/fall times.	Yes	Circuit is tested and passed.
Req-12	The device must be capable of supplying a full range of 0 to 200 Volts RMS AC, tuneable between 50-300 kHz.	Under standard testing conditions, an oscilloscope can be used to measure the output voltage and frequency.	Not Validated	The selected circuitry should be capable of reaching the requirement, however was not prototyped fully as this required additional -145 supply.

Req-13	The device must incorporate a switchable output signal amplitude modulator (100% level) using a square wave signal over the range of 10–100 Hz for all AC outputs, tuneable as per Req-15.	Under the standard testing conditions, waveform analysis (using an oscilloscope) will ensure output waveform accuracy and smoothness over the full voltage range for all frequency steps. 'Smoothness' meaning minimal skew and consistent rise, fall and peak-peak times.	Not Validated	Code created; component not validated.
Req-14	The device must be designed to operate using an external power supply adapter that provides a specified DC voltage in the range of 5 to 30 V DC. If possible, the design will utilise a 12 V input.	Final design capability can be verified demonstrably to the client under standard test conditions, showing the device is capable of the required range of output functionality using the specified external power adapter. A recommendation of a preferred, market available, adapters alongside alternatives tested will be provided with the final design.	Yes	Incorporated in design architecture, utilises 12VDC input.
Req-15	The device must be capable of adjusting the output square wave modulation frequency in steps of 10Hz.	Under standard testing conditions, the step frequency change can be verified using an oscilloscope.	Not Validated	Code created; component not validated.
Req-16	The device must be capable of AC frequency adjustments steps of ~10 kHz.	Under standard testing conditions, the step frequency change can be verified using an oscilloscope.	Yes	Circuit tested and passed.

Req-17	The current limit is tuneable between 1 and 10 mA, using steps of ~2 mA.	Under standard testing conditions, the step current protection cut-off changes can be verified using an oscilloscope.	No	The first prototype of the DC sensing circuit did not include this functionality.
Req-18	The device output voltage must not deviate more than 0.05V from the expected voltage. This includes noise and the impact of voltage ripples.	Under standard testing conditions, the level of noise present in the system should be evaluated and verified using an oscilloscope for the full range of AC and DC voltages and current outputs. Testing under non-ideal conditions (increased heat, electromagnetically noisy lab settings etc) should be considered at this stage to increase device versatility.	No	The switching noise amplitude exceeds the 0.05V requirement. Filtering circuitry was deployed to attempt achieving this requirement, but the team was not able to achieve sufficient filtering to meet the requirement.
Req-19	The project must be prepared using hardware under the CERN-OHL-P License.	Provide documentation for relevant hardware.	Yes	
Req-20	Project handover must occur on Friday Week 12 (20/10/2023).	Submission complete and on-time.	No	This deadline was extended to Wednesday (25/10/2023).
Req-21	The device will shut down if internal temperature exceeds 80˚C.	Ideally this should not occur given proper heatsink and (if necessary) active cooling solutions. The total output power is only 2W, hence the system is unlikely to trigger the overtemperature under normal conditions (triggering when component fault or excessive external heat). Thus, to test the system, using a heat gun on the sensor directly may be required, verifying its activation.	Yes	Test conducted and passed.

Req-22	The device will use high-voltage BNC ports for the output signals. This is a project constraint, as the requirement to accommodate this port type will affect the design of the circuity and the selection of components used in the design.	Testing the output signal is as desired from the ports, using an oscilloscope.	Yes	HV BNC port installed on output.
Req-23	Project outcomes will be shared with the project partner using GitHub. This is inclusive of: reports; designs; prototype documents; CAD Models; PCB Files; component registers; testing results; a design modification registry and may develop as the project progresses.	GitHub is well structured, complete and on-schedule.	Yes	All deliverables presented in the requested format.
Req-24	The process of selecting components shall be conducted with careful consideration of component availability, lead times, and the current manufacturing state. This approach aims to ensure timely procurement and seamless integration of components into the final product.	As part of the final design, identifying and providing recommendations for component replacements/alternatives should stock be unavailable or be discontinued.	Yes	Components were sourced on time and recommendations for potential improvements if time allowed.
Req-25	The human-machine interface must allow user's to set device parameters including the output signal type, frequency and voltage, as well as the output protection current limit	Connect the output to a multimeter and check outputs correctly correspond to the user input.	Yes	Test conducted and passed.

Req-26	The lab voltage supply design shall prioritise repairability, maintainability, and an operational lifespan of a minimum of 10 years. Some measures shall be considered to address potential component unavailability in the future by providing recommendations for suitable replacements.	As part of final design, provide recommendations to the client on replacement/alternative components should specific parts get discontinued. Should a necessary part look likely to be unavailable within the lifespan, advocate for a last-time buy strategy to stockpile that part.	Yes	was implemented through component selection, ensuring no components were scheduled for obsolescence.
Req-27	Design shall use Restriction of Hazardous Substances Directive (RoHS) compliant components wherever feasible.	Inspecting the documentation of components to verify their RoHS certification.	Yes	All utilised components adhere to the RoHS certification.
Req-28	The project budget will be less than $350 inclusive of all prototyping, testing and final design.	Inspecting the project budget to ensure adherence to the allocated amount.	No	Budget was exceeded. Please refer to final design BoM.
Req-29	The device may incorporate a programmable output feature that allows users to define precise voltage and frequency parameters for designated durations. Once defined, output can be run using one button press. This feature will work for either AC or DC output for a given run.	Testing the programmable output feature under various voltage and frequency settings to ensure that the user can define these parameters and run the output with a single button press.	No	This feature was not included in the design due to budget and time constraints.