ES152 Final Project Report.

1. Summary.

1.1 Algorithmic Simplification.

$$F(x) = \frac{ax+b}{cx+d}$$

$$= \frac{a}{c} + \left(\frac{b}{c} - \frac{ad}{c^2}\right)\frac{1}{x+\frac{d}{c}}$$

$-1 < X < 1$.

1.2. numerical to physical values mapping.

The specifications of parameters are:

① $a, b, c, d \in \mathbb{R}$.

② $X \in \mathbb{R}$, $-1 < x < 1$.

Because F(x) is calculated by physical values, it can't be infinity, thus $1 < \frac{d}{c}$ or $\frac{d}{c} < -1$

Another specification is $c \neq 0$; other wise

$F(x) = \frac{a}{d}x + \frac{b}{d}$ is easy to implement.

To make physical values are ~~handet~~ handled by transistors properly, a mapping:

$$G(a) = a \cdot I_{ref}$$

is ~~designed~~ assigned.

This the actual function performed is

$$F(x) = \frac{G(a)}{G(c)} + \left(\frac{G(b)}{G(c)} - \frac{G(a)G(d)}{G(c)G(c)}\right)\frac{1}{x+\frac{G(d)}{G(c)}}$$

$$G(F(x)) = \frac{G(a)}{G(c)}I_{ref} + \left(\frac{G(b)}{G(c)} - \frac{G(a)G(d)}{G(c)G(c)}\right)\frac{I_{ref}}{G(x)+\frac{G(a)I_{ref}}{G(c)}} \quad (1)$$

Equation (1) is implemented through circuit.

G(a) are presented by currents.

1.3. Design Specifications.

From Equ.(1) and mapping G(a) we know that

$$G(-a) = -G(a)$$

and the direction of currents can be changed according to current's positively or negatively.

Thus we can assume that

$a, b, c, d > 0$.

and

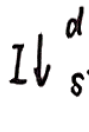
$$\frac{c}{d} > 1.$$

other conditions can be handled in same way, rather than change some direction of currents.

1.4. Choice of I_{ref}

I_{ref} is choosen to make all the values in circuits work in designed condition.

In this project. Sub-threshold mode is used, nmos



$I \propto e^{V_{gs}/V_T}$ when $W = 6\mu m$, $l = 3\mu m$, in the region of

$20pA < I < 12nA$.

$0.3V < V_{gs} < 0.6V$.

$V_{ds} > V_{Th}$.

Thus I_{ref} is choosen according to

$$\frac{G(a)}{G(c)}, \frac{G(b)}{G(c)}, \frac{G(a)G(d)}{G(c)G(d)}, G(x)+\frac{G(d)}{G(c)}I_{ref}, \frac{G(d)}{G(c)}$$

and $G(a), G(b), G(c), G(d)$ in region of

$[20\,pA, 12nA]$.

In later section of experiment,

$I_{ref} = 1nA$, $a=1$, $b=2$, $c=5$, $d=12$.

2. Circuit Schematic.

2.1. Calculation.

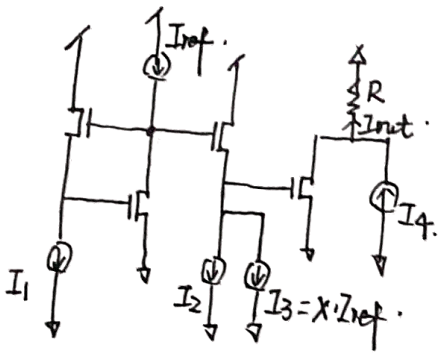


Fig 1: Simplified calculation.

$$I_1 = \left[\frac{G(a)G(d)}{G(c)^2} - \frac{G(b)}{G(c)}\right] I_{ref} = 0.08nA.$$

$$I_2 = \frac{G(d)}{G(c)} I_{ref} = 2.4nA.$$

$$I_4 = \frac{G(a)}{G(c)} I_{ref} = 0.4nA. \qquad I_3 = X \cdot I_{ref} = G(x).$$

$R = 10k\Omega$.

We can check that

$$I_{out} = G(F(x)) = F(x) \cdot I_{ref}.$$

I_1, I_2, I_4 don't depend on X, can be assigned in simulation.

2.2. Fixed-point schematic.

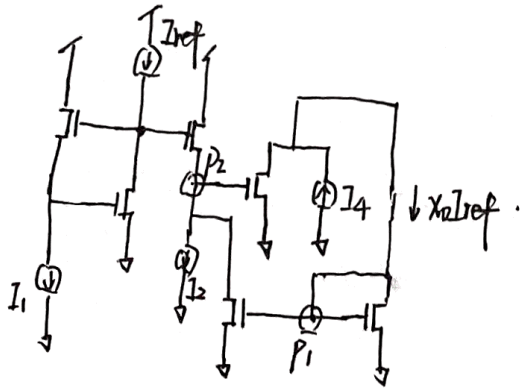


Fig 2: Simplified fixed-point calculation.

A great point of that design is we don't need to worry about stability issue in fixed-point feedback. because there are 2 poles in changing feedback and a right hand zero, it is easy to do frequency compensation by adding miller capacitor from p1 to p2.

In this simulation, no problem of stability is met.

2.3. Full design

Fig 3 shows a multiplier & Divider.

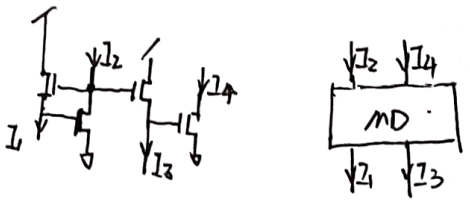


Fig 3.

We can show that $I_4 = \frac{I_1 I_2}{I_3}$.

Thus,

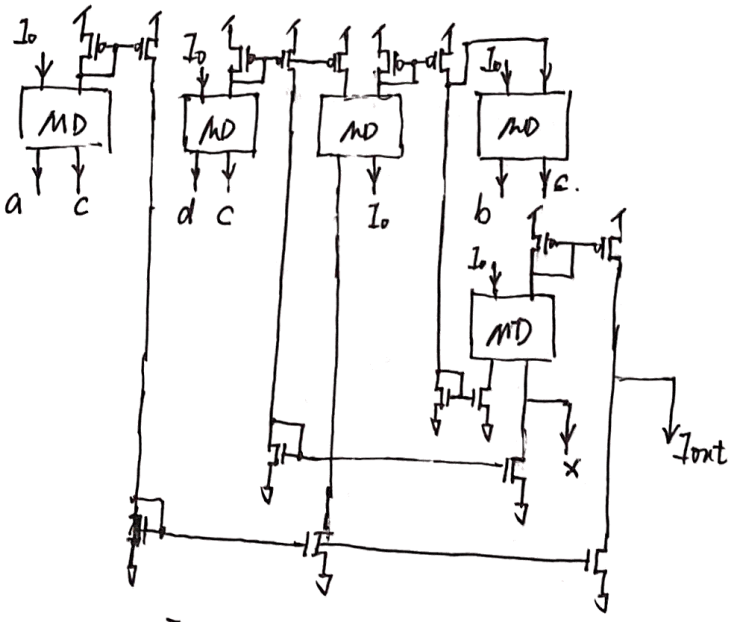


Fig 4: Full design. $I_o = I_{ref}$.

Fig 4 shows a full design, which take a,b,c,d,x as input, and Iout as output.

36 transistor.