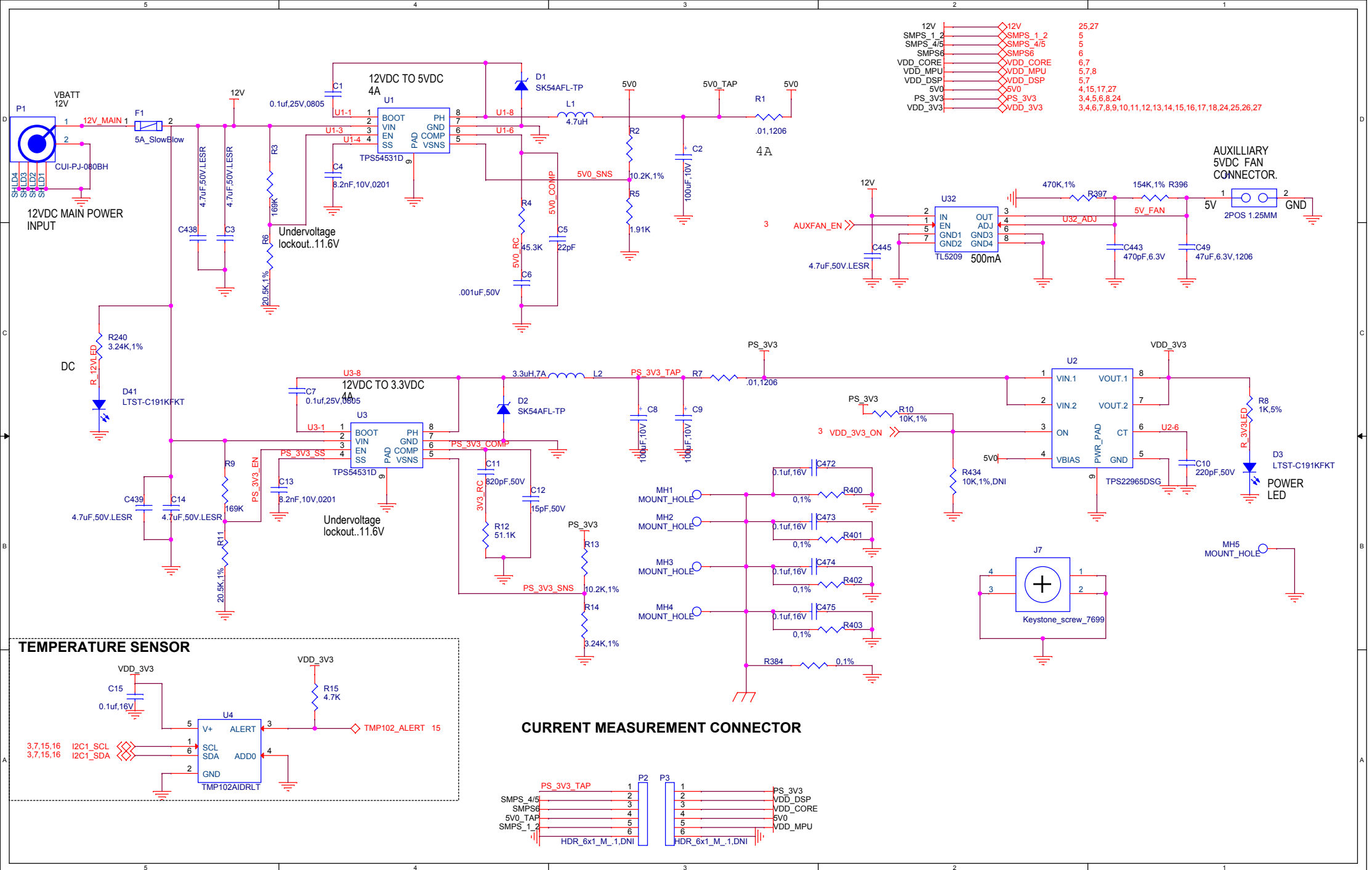
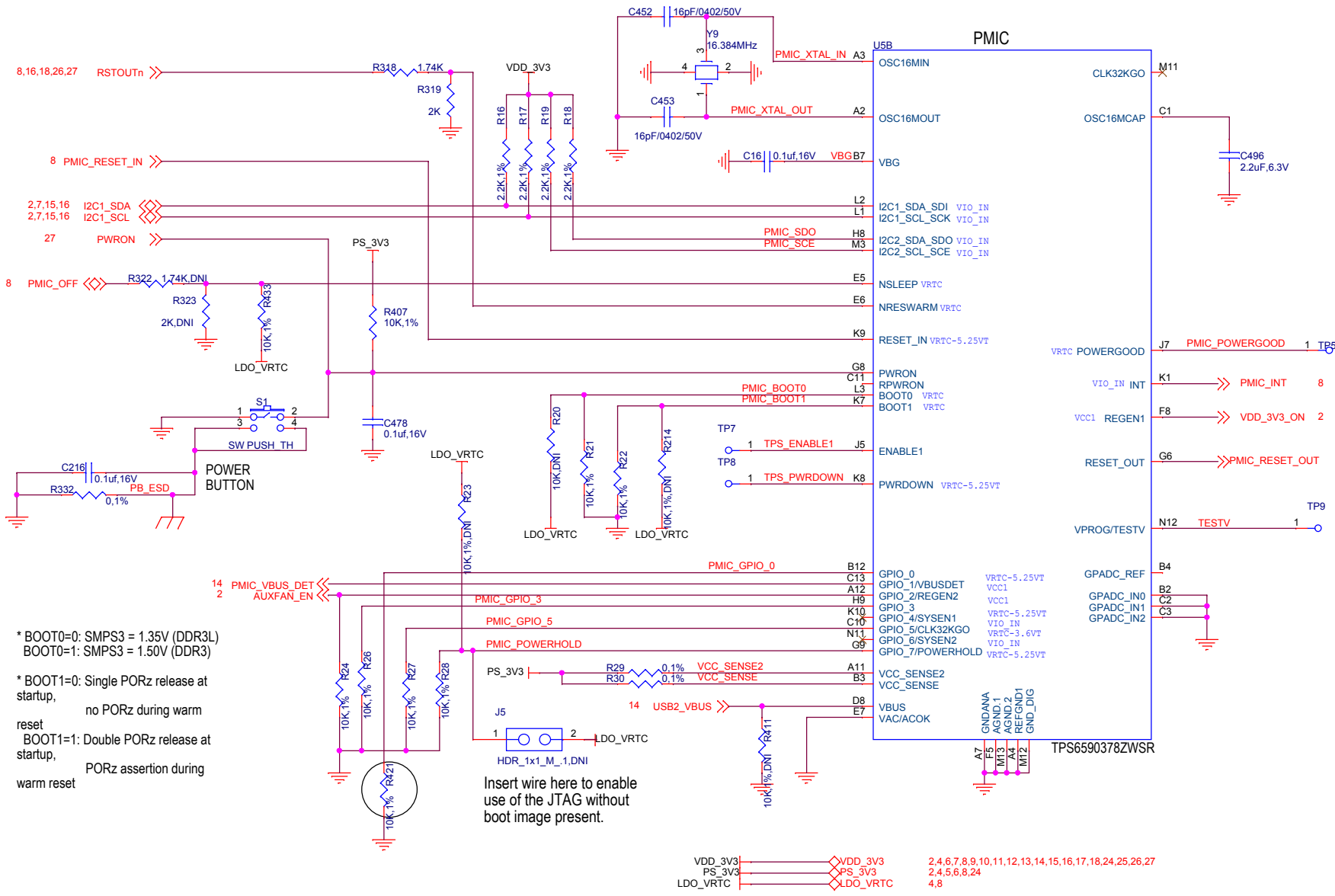


```
P01 TITLE PAGE
P02 12V INPUT, 3.3V AND 5V SWITCHERS
P03 TPS6590378 1 CONTROL
P04 TPS6590378 2 RESET, & RTC
P05 TPS6590378 3 MPU,DDR, & DSP SWITCHERS
P06 TPS6590378 4 CORE & 1.8V
P07 AM5749 CORE POWER & EEPROM
P08 AM5749 CLOCKS AND RESET
P09 AM5749 IO POWER AND GROUND
P10 AM5749 DDR3 POWER & JTAG
P11 AM5749 ETHERNET 1
P12 AM5749 ETHERNET 2
P13 AM5749 GPMC & LCD
P14 AM5749 USB INTERFACES
P15 AM5749 I/O, LEDs, AND GPIO
P16 AM5749 AUDIO & DEBUG SERIAL
P17 AM5749 HDMI PORT
P18 AM5749 eMMC, MMC3, & uSD
P19 AM5749 DDR INTERFACE 1
P20 AM5749 DDR INTERFACE 2
P21 DDR3 BANK 1
P22 DDR3 BANK 2
P23 DDR3 BANK 2 CAPS & TERM
P24 DDR3 BANK 1 CAPS & TERM
P25 USB & SATA CONNECTOR
P26 PCIe, SATA, & SERDES CLOCK
P27 EXPANSION HEADERS
P28 MECHANICAL
```



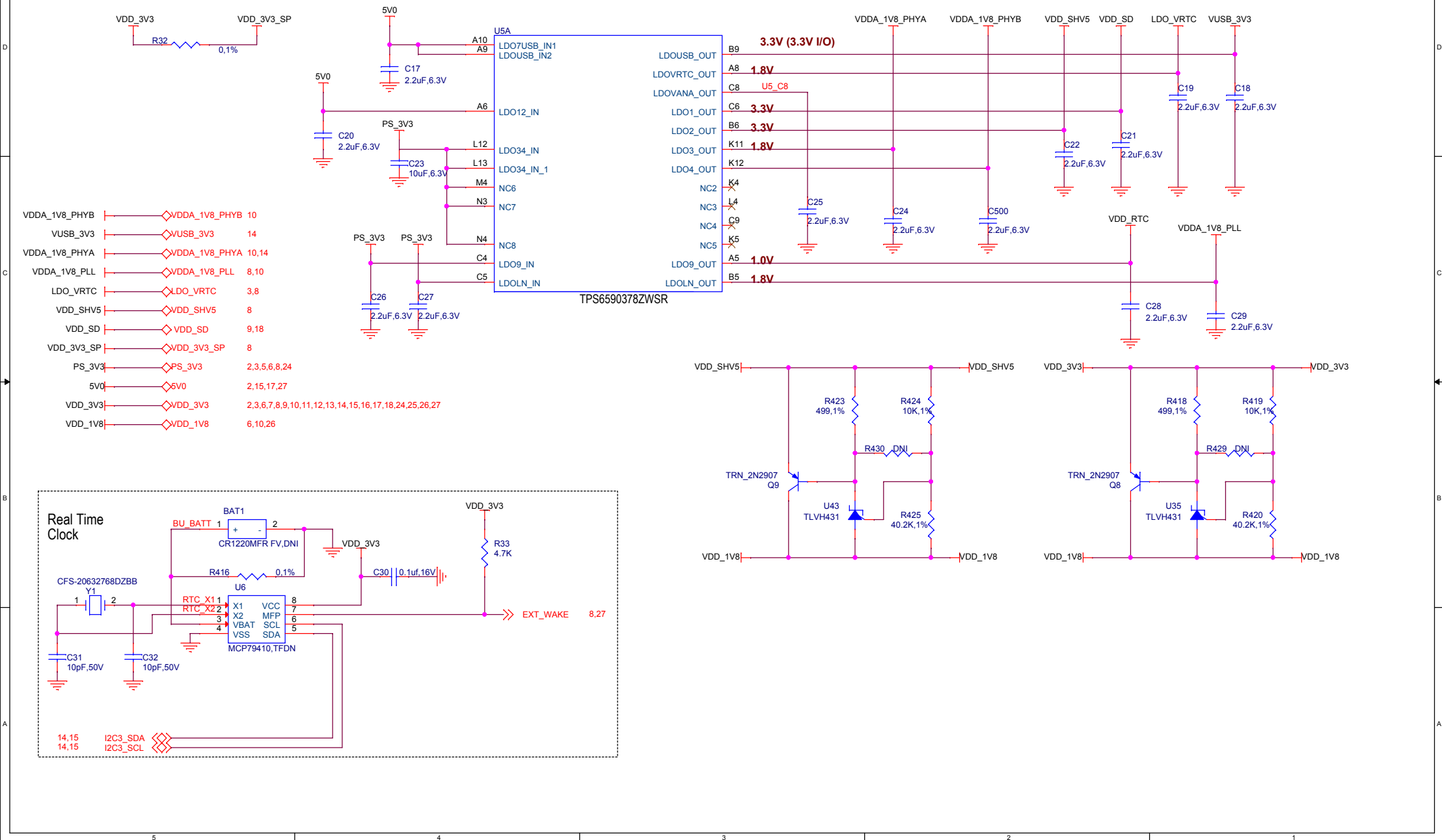


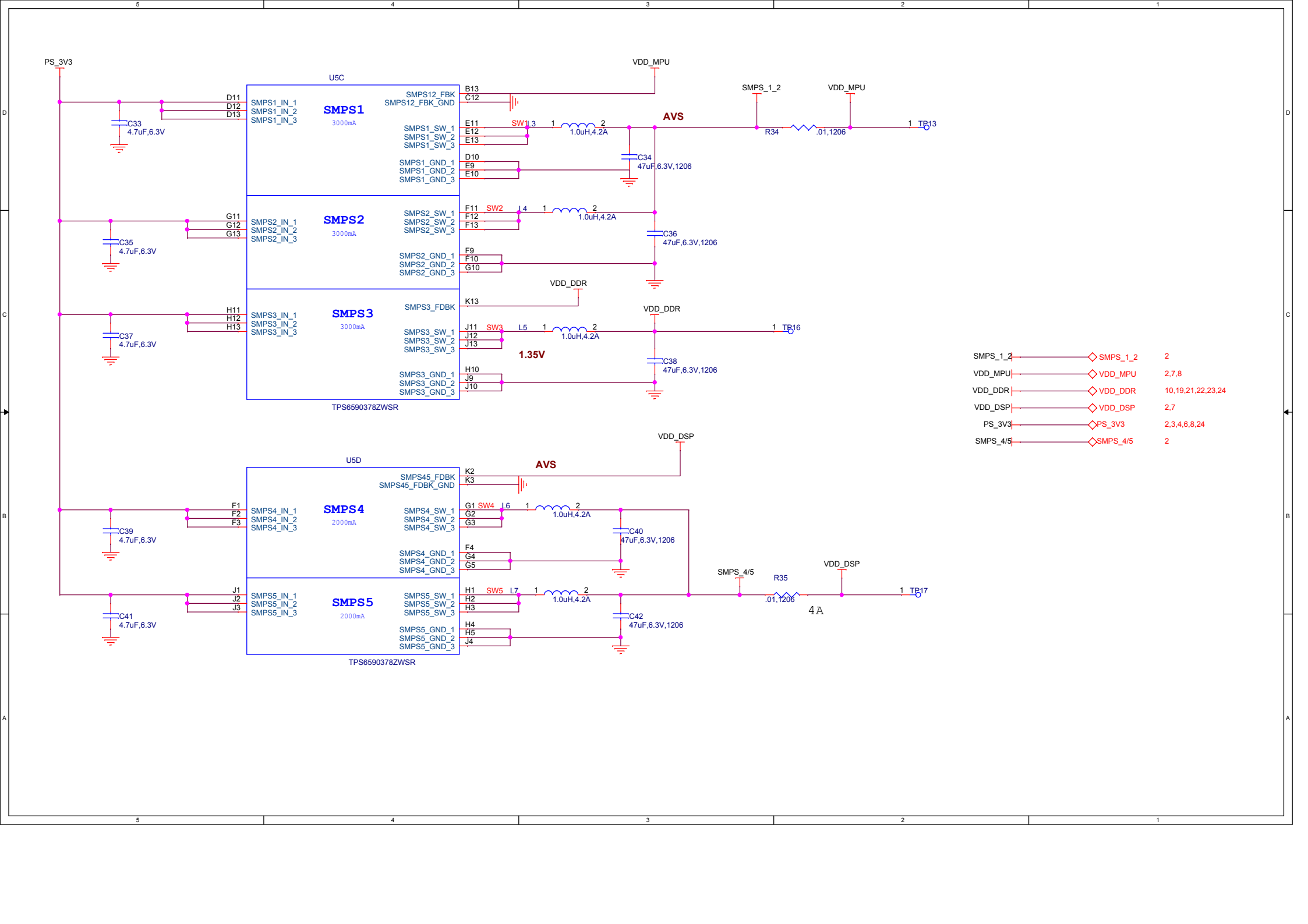
* BOOT0=0: SMPS3 = 1.35V (DDR3L)
BOOT0=1: SMPS3 = 1.50V (DDR3)

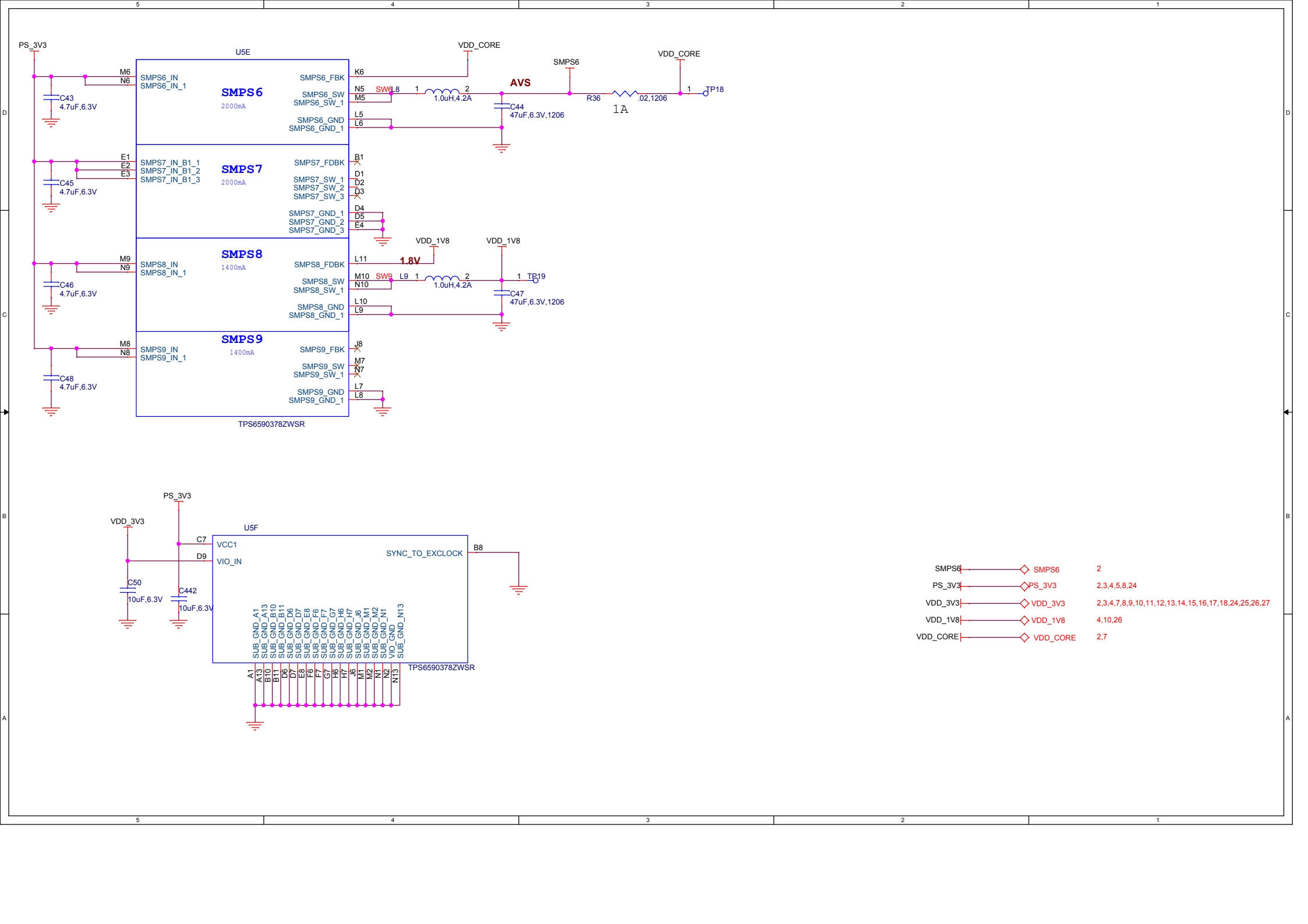
* BOOT1=0: Single PORz release at startup,
no PORz during warm reset
BOOT1=1: Double PORz release at startup,
PORz assertion during warm reset

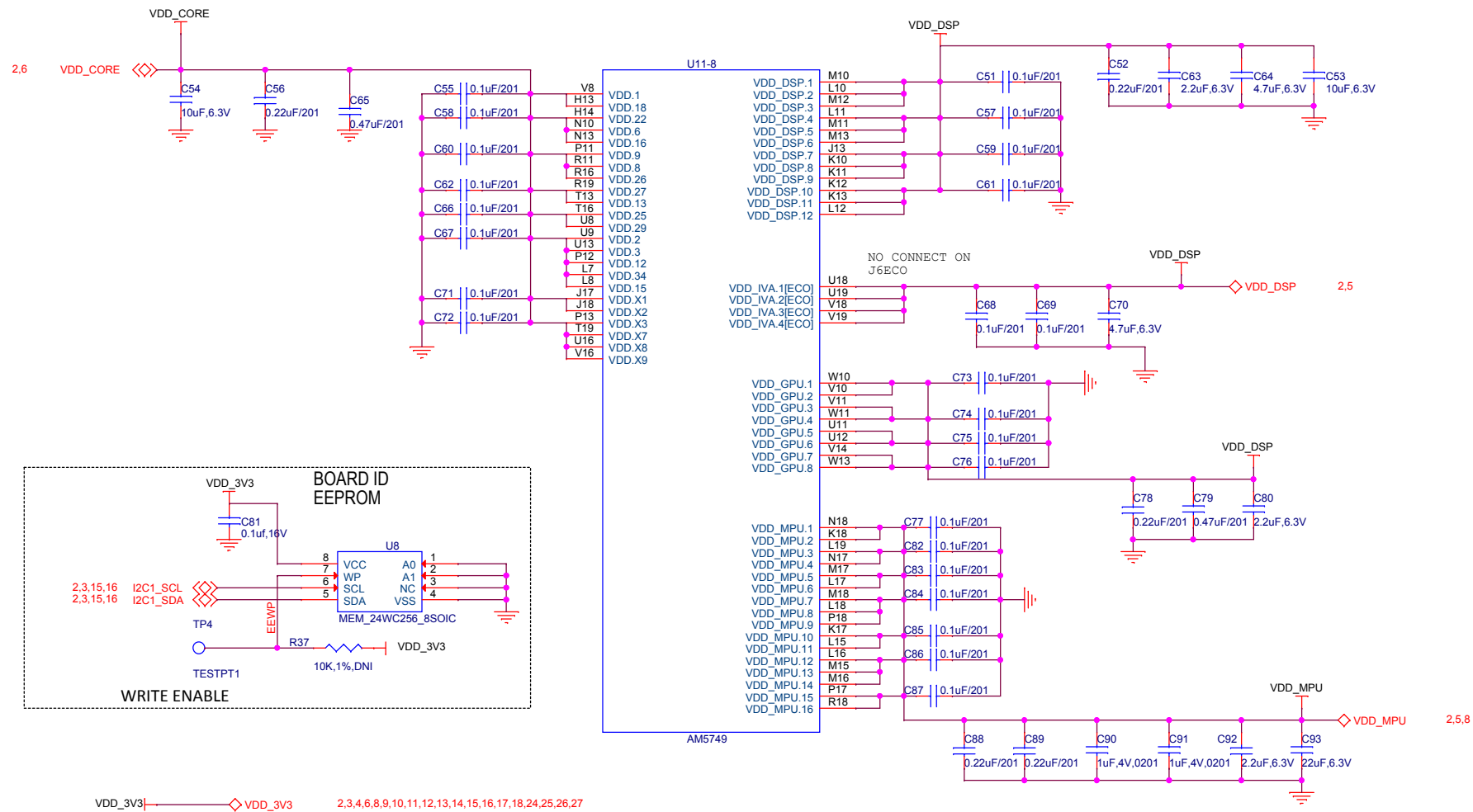
Insert wire here to enable use of the JTAG without boot image present.

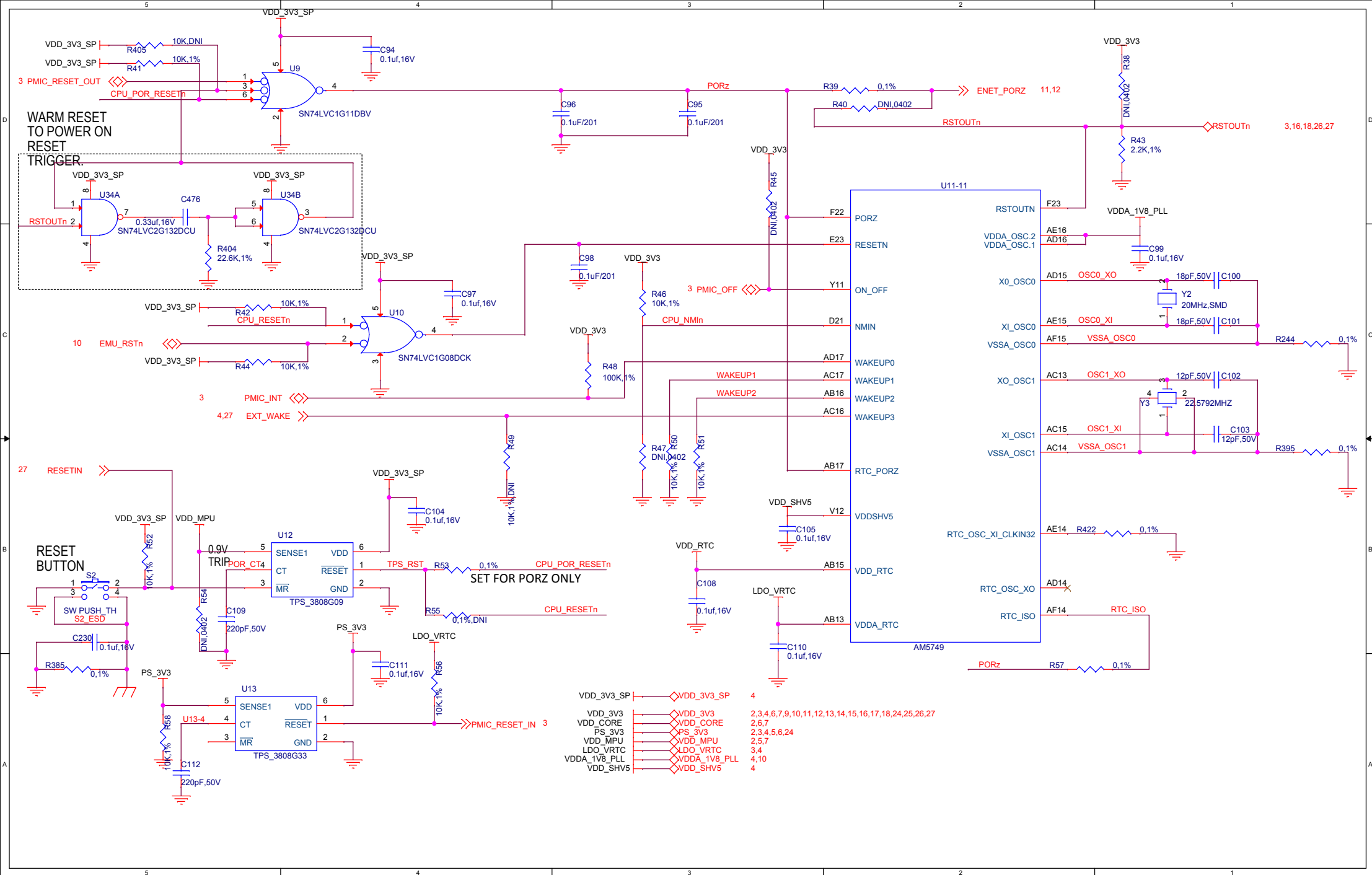
VDD_3V3		VDD_3V3	2,4,6,7,8,9,10,11,12,13,14,15,16,17,18,24,25,26,27
PS_3V3		PS_3V3	2,4,5,6,8,24
LDO_VRTC		LDO_VRTC	4,8

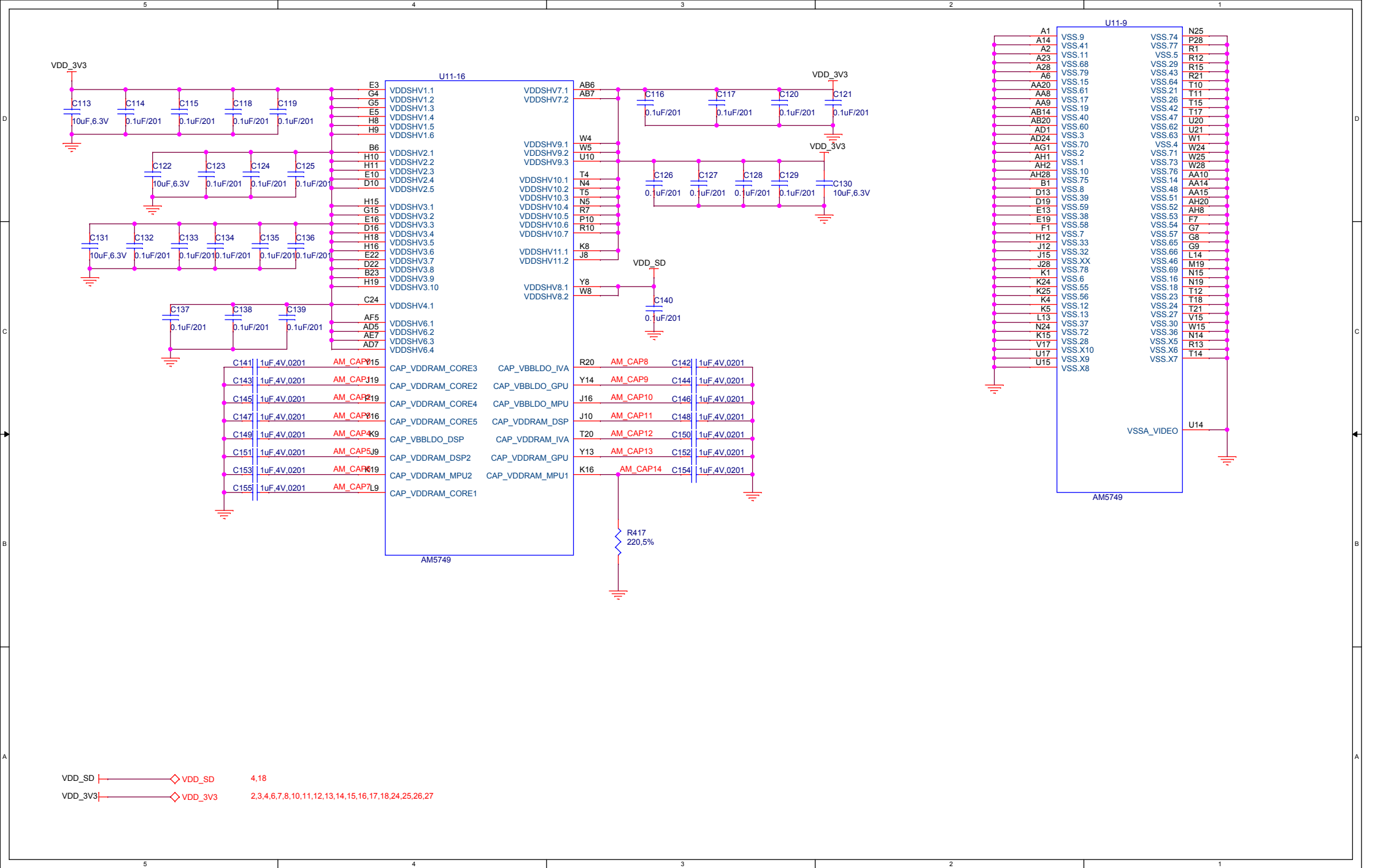


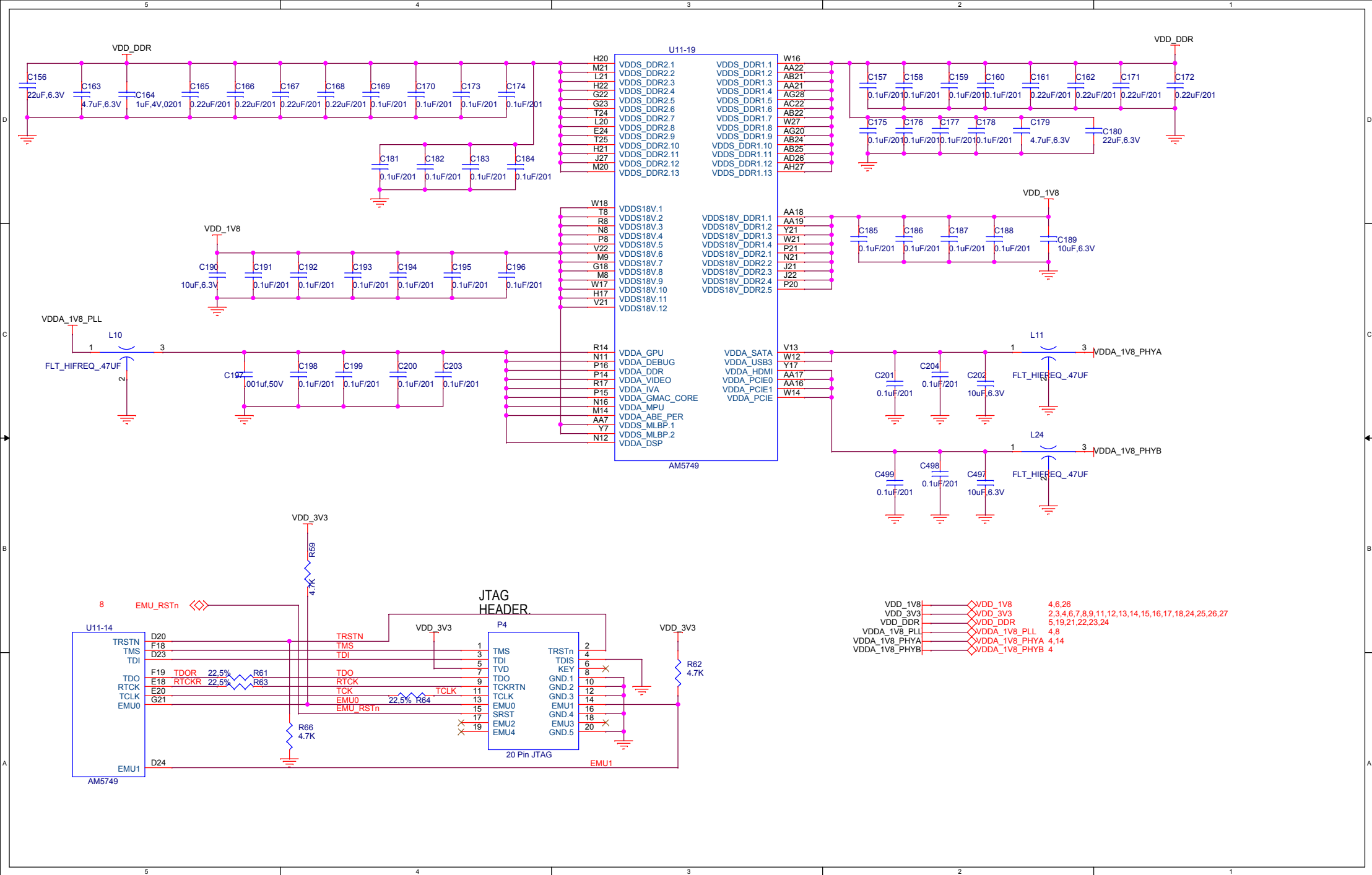


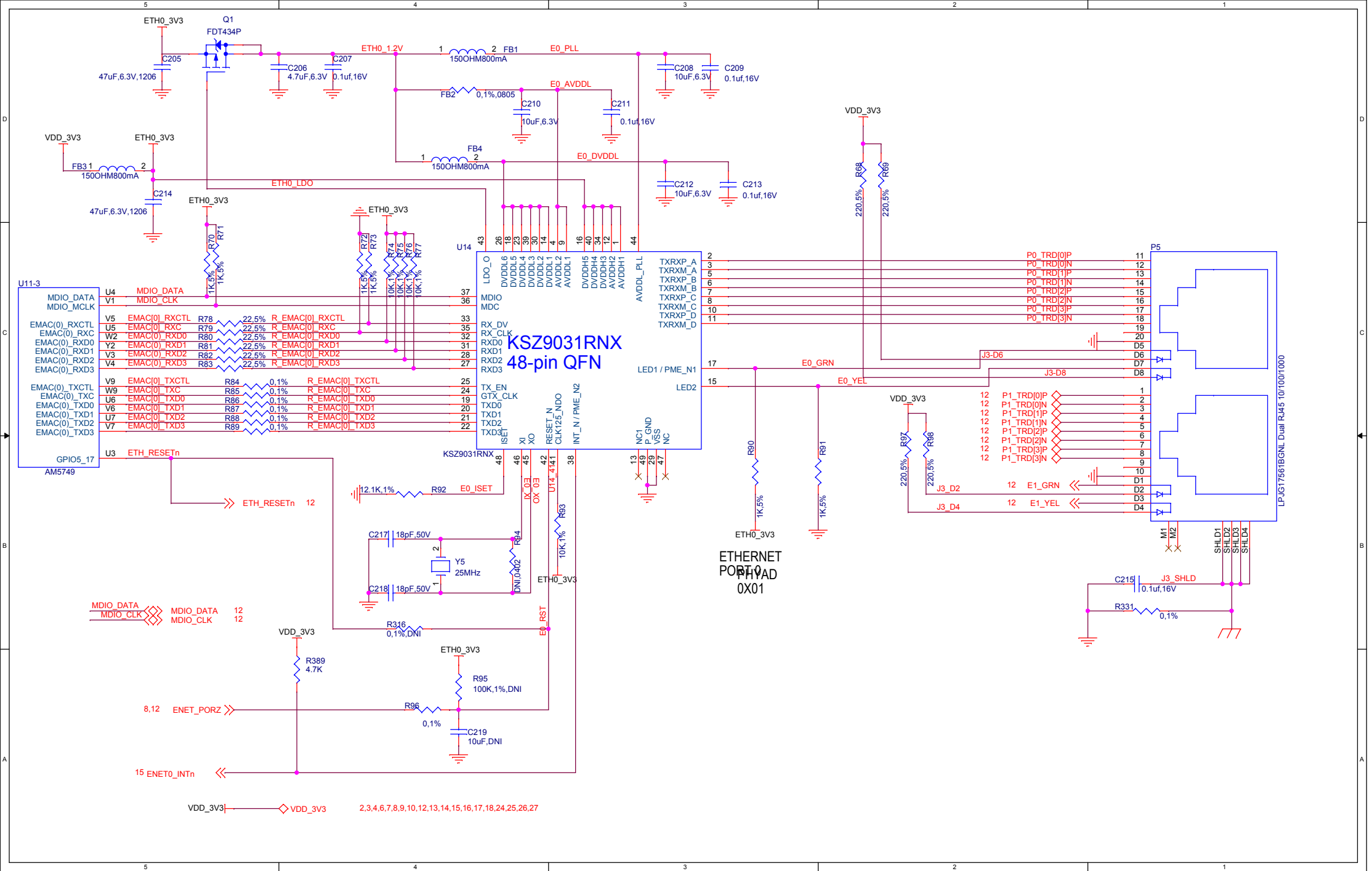


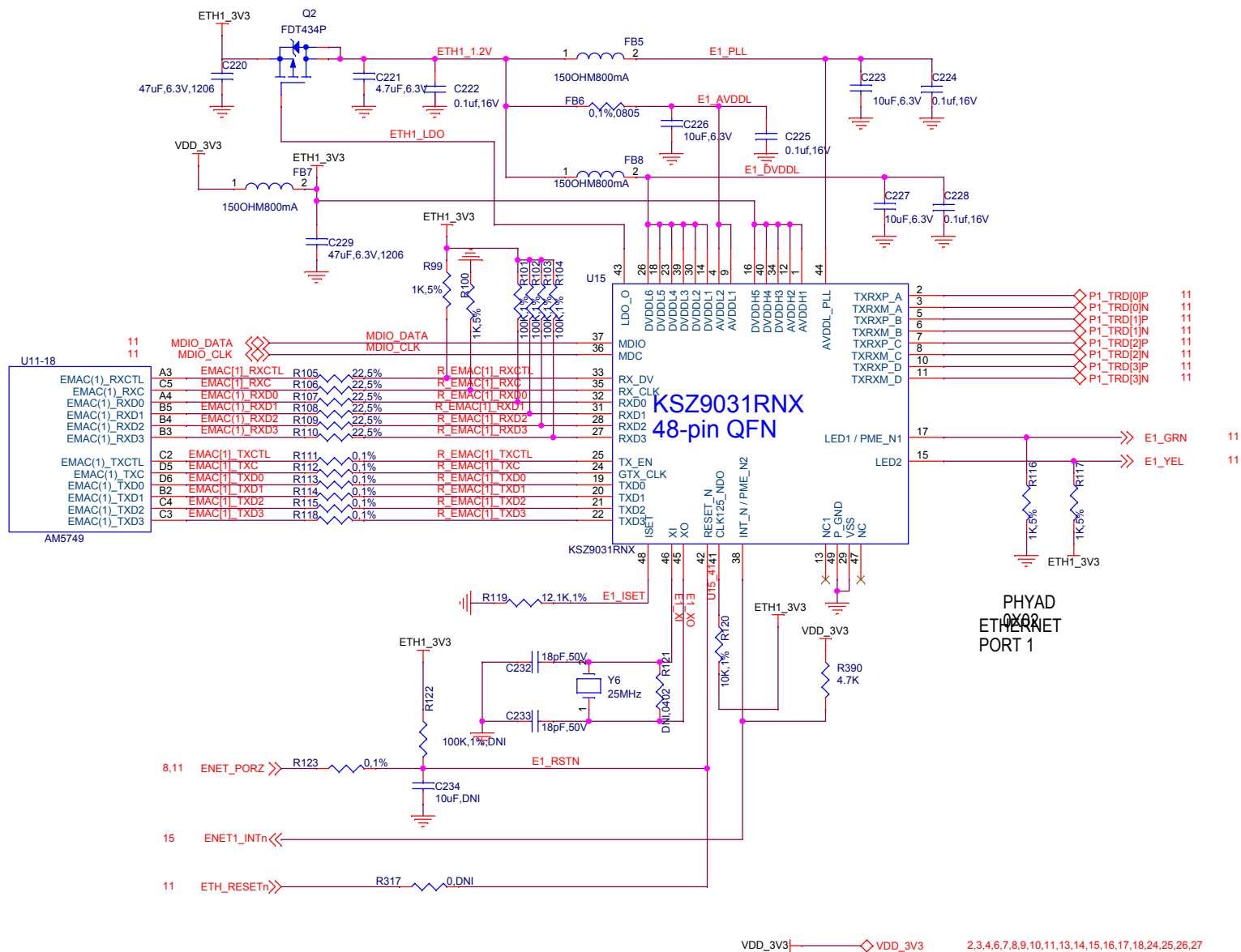


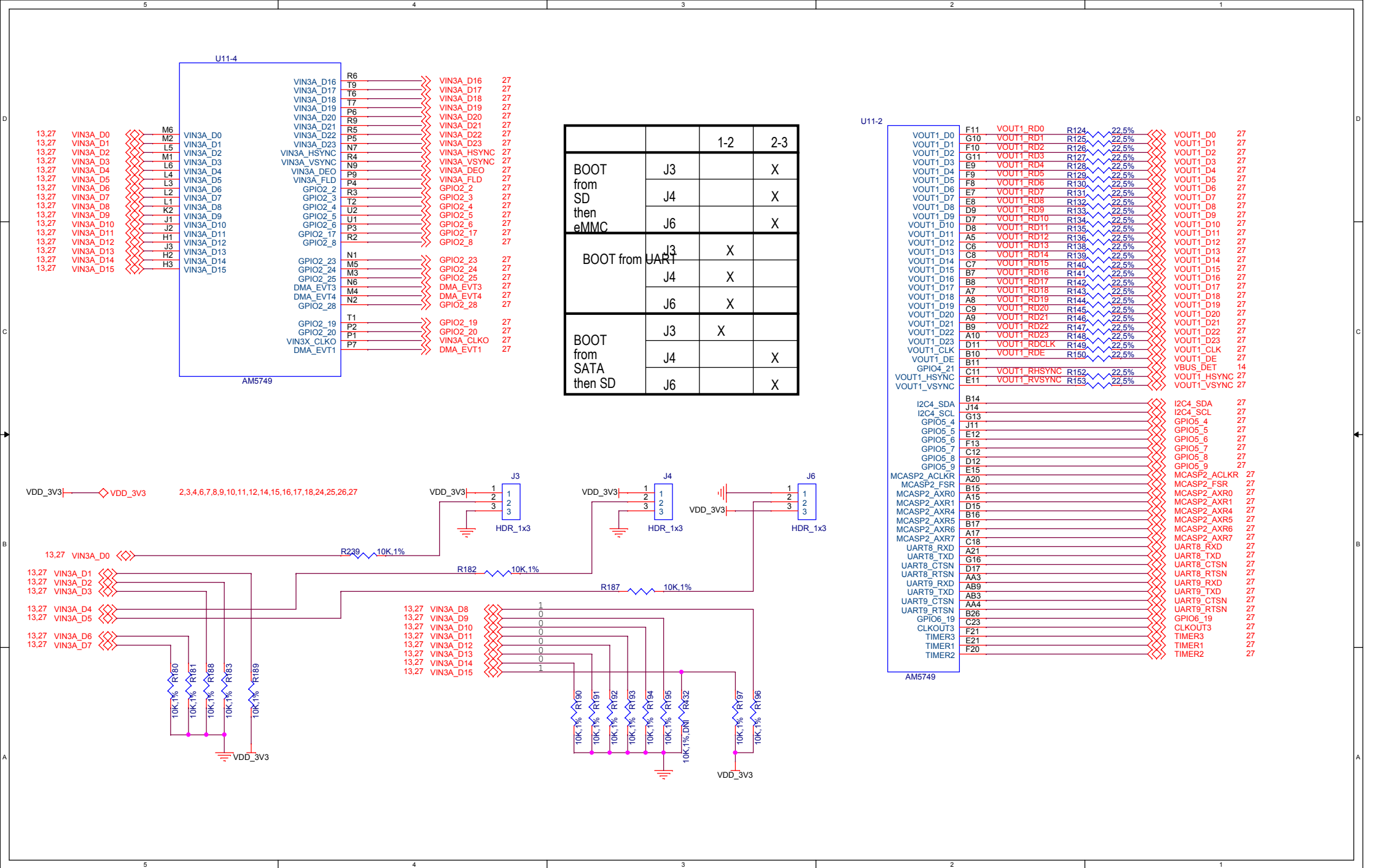


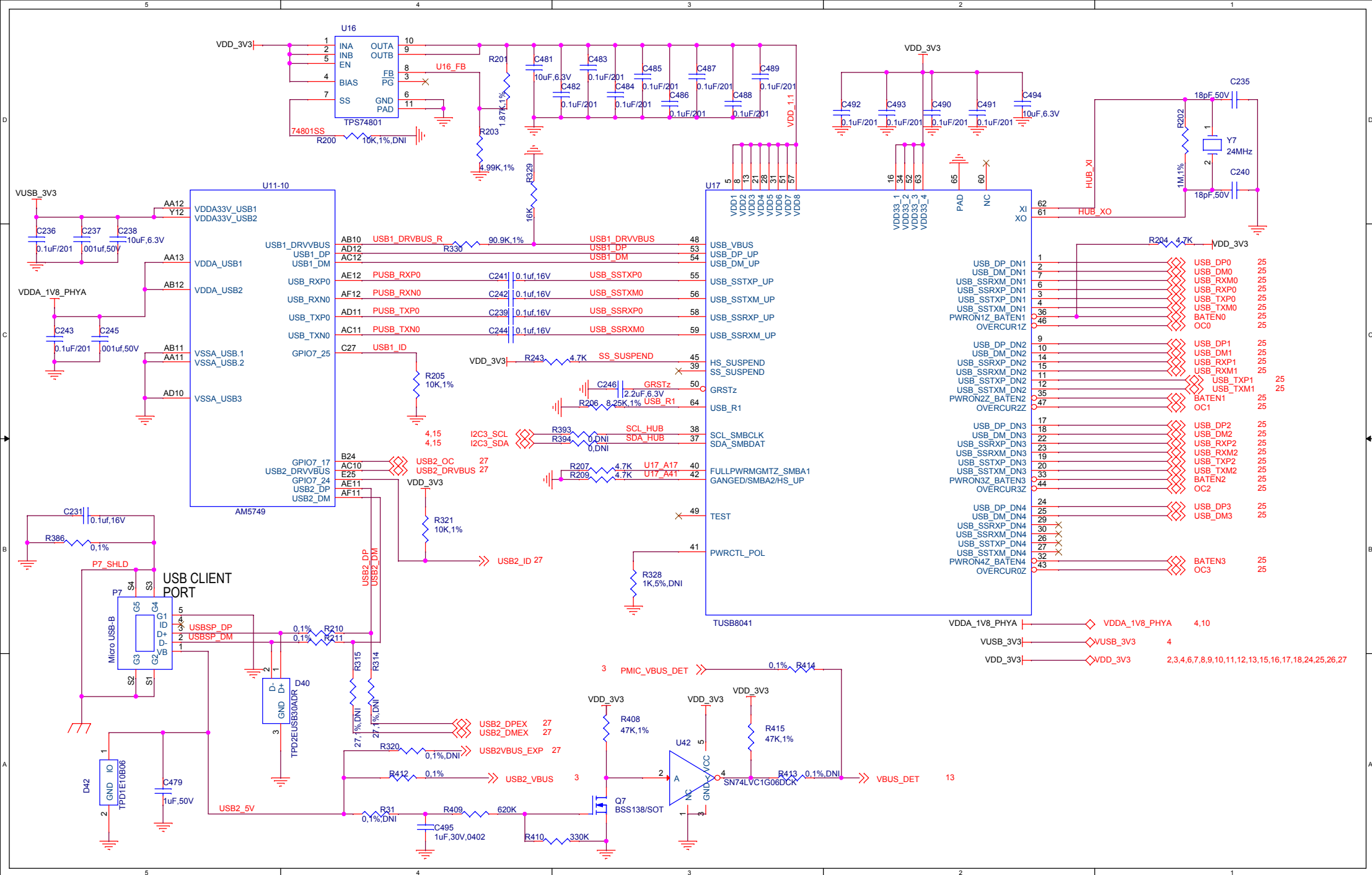




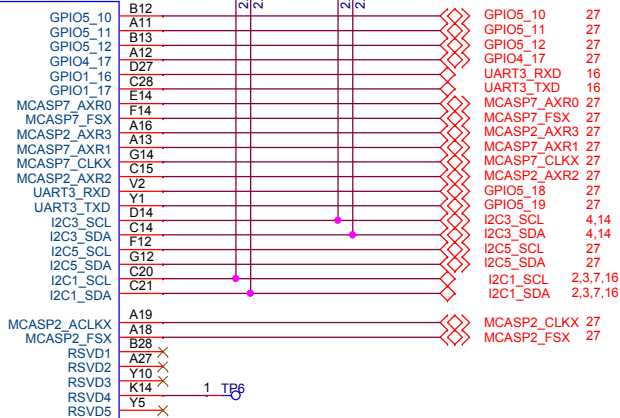




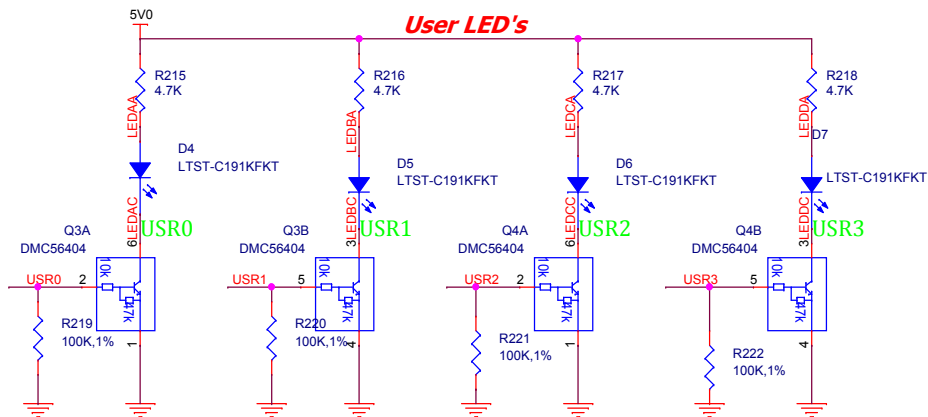




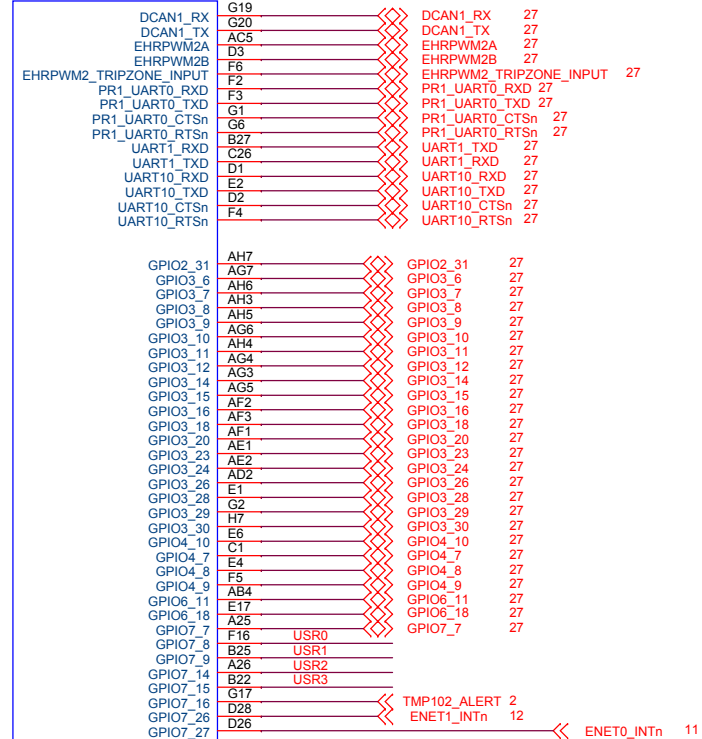
U11-7

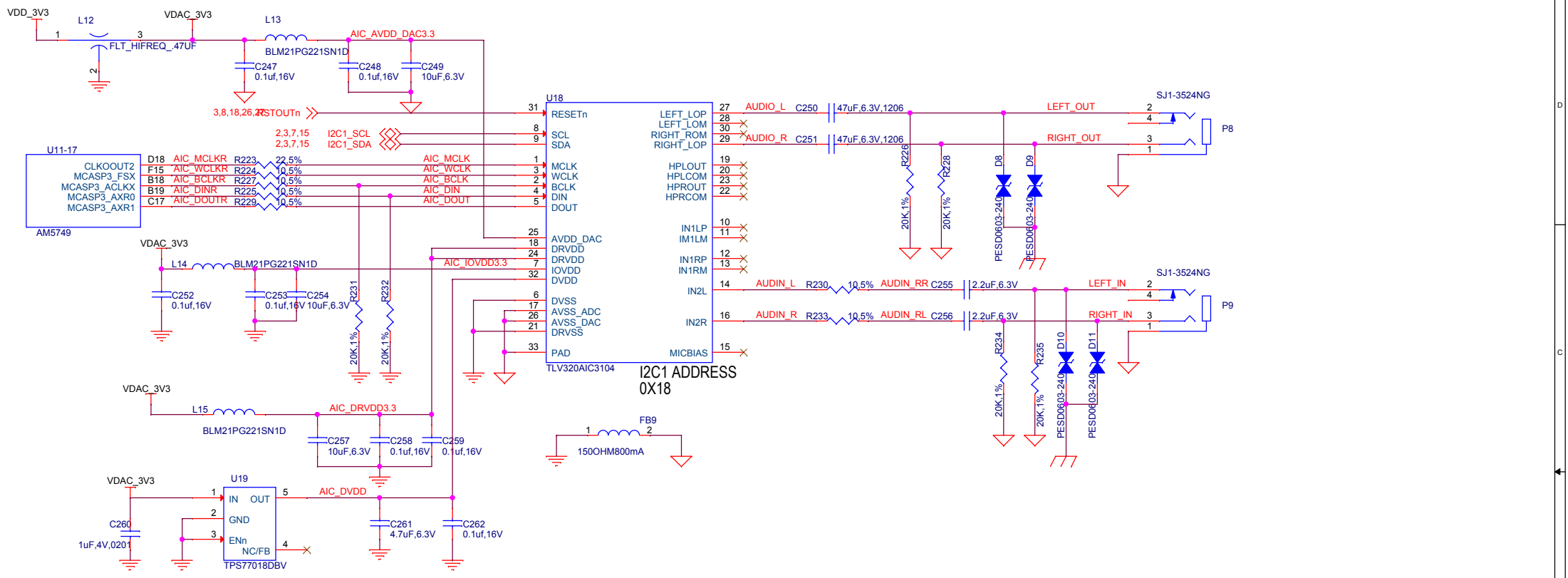


User LED's

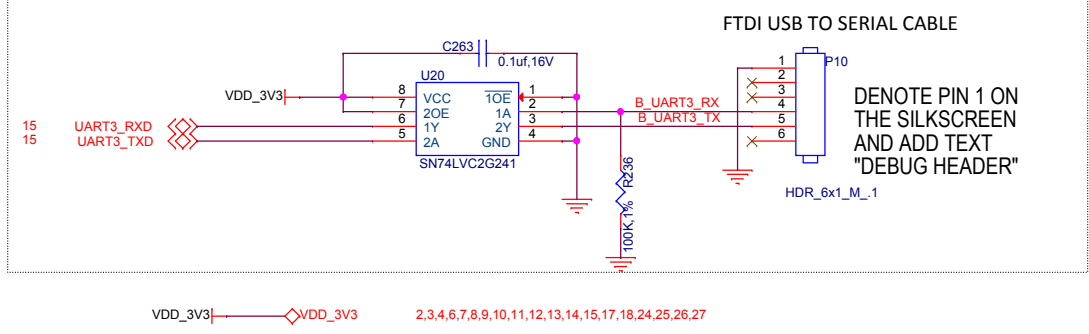


U11-12





DEBUG
HEADER



VDD_3V3 2,3,4,6,7,8,9,10,11,12,13,14,15,17,18,24,25,26,27

