Sanjeev Krishnan Kamalamurugan

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OBJECTIVE: Seeking internship in ASIC Design and Verification starting January 2026.

EDUCATION

M.S., Electrical and Computer Engineering **GPA: 3.4 / 4.0**
Portland State University, Portland, Oregon (Expected Graduation: June 2026)

Coursework: Pre-Silicon Validation, Assertion Based Verification, Microprocessor System Design, Advanced Computer Architecture. **Courses by June 2026:** Post Silicon Validation, Formal Verification

B.E., Electronics and Communication Engineering **GPA: 8.3 / 10**
Anna University, Chennai, India (Graduated: April 2023)

TECHNICAL SKILLS

Programming & Scripting Languages	Verilog, SystemVerilog, C/C++, CUDA C++, TCL, Python(Basics)
Hardware Concepts & Architectures	x86, RISC-V, MIPS, NVIDIA GPU Architecture, ISA, DDR DRAM, Cache, Branch Prediction, Pipelining, Out-of-order execution
Verification Methods & Concepts	UVM, Class based Verification, Assertions, Functional Coverage, Constraints and Randomization, Object Oriented Programming (OOP)
Protocols & Interfaces	AMBA, MESIF, UART, I2C, SPI
Tools & Operating System	Mentor QuestaSim, Synopsis VCS, Cadence JasperGold, Vivado, Vitis, Git, Visual Studio Code, Linux

PROJECTS

UVM-Based Arithmetic Floating Point Unit Verification[System Verilog]
Designed **IEEE 754-compliant Arithmentic FPU** in achieving **95% functional and 80% code coverage**. Generated **300+ stimulus** through constraints and randomization verifying corner cases like **Infinity, NaN, and subnormals** to ensure full compliance of the unit.

Assertion Based Verification of Asynchronous FIFO[System Verilog]
Designed and verified an **Asynchronous FIFO using SystemVerilog Assertions**, achieving **100% coverage** through **system verilog cover properties**. Validated data **integrity, metastability, and boundary conditions like data loss, timing hazards**.

RISC-V RV32IM Simulator in C
Implemented **5-stage pipelined RISC-V ISA** functionality in single cycle model, addressing the **64KB memory constraint** managing the initialisation of **program counter and stack pointer**. Developed robust testcases in assembly language and generated **memory image files** using **RISC-V cross compiler**.

System Verilog Design and Verification of Cache Controller
Designed and simulated **Last Level cache** featuring **16-way associativity** and **64-byte line size** using **write-back and write-allocate** policies. Implemented **P-LRU policy** and **MESI protocol** for eviction and coherence. Verified with comprehensive test cases achieving performance of **99.6% hit ratio**.

EXPERIENCE

Frontend Developer Intern **July 2022 – Aug 2023**
Freightify - Chennai, India
Developed web interface in React and maintained CI/CD pipeline via GitHub and Jenkins.

CERTIFICATION

Accelerated Computing in Modern CUDA C++ Issued by Nvidia · **(July 2025)**
Completed hands-on training in CUDA C++ for GPU-accelerated computing, covering parallel programming, memory optimization, kernel execution, thread hierarchy, and performance profiling.

Basic Static Timing Analysis Issued by Cadence Design Systems · **(April 2025)**
Covered concepts like **cell delay**, **net delay**, **timing paths**, and **timing checks**. Gained understanding of timing constraints and analysis techniques essential for **digital circuit timing verification**.