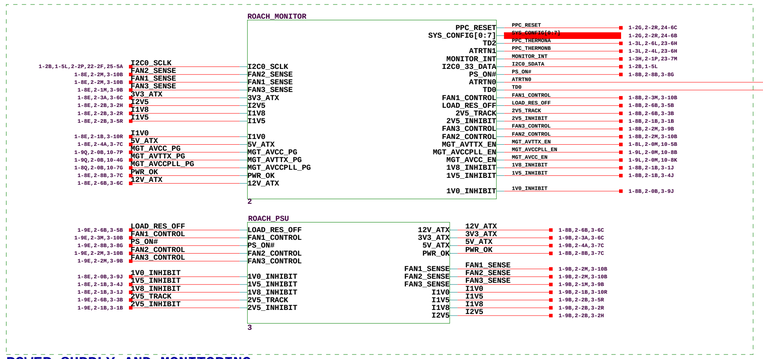
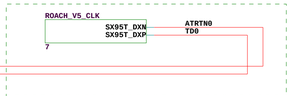
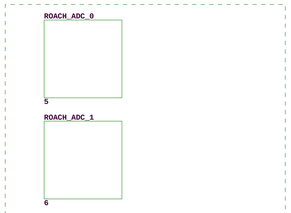
VIRTEX5



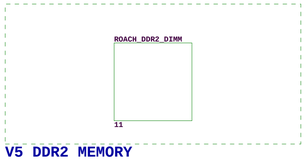
POWER SUPPLY AND MONITORING



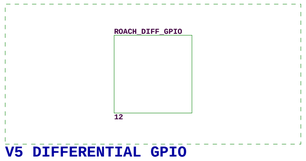
VIRTEX5 CLOCKS



ZDOK/ADC INTERFACE

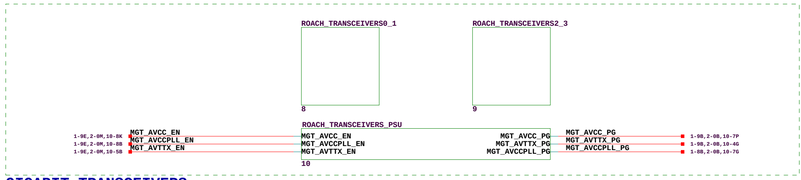


V5 DDR2 MEMORY

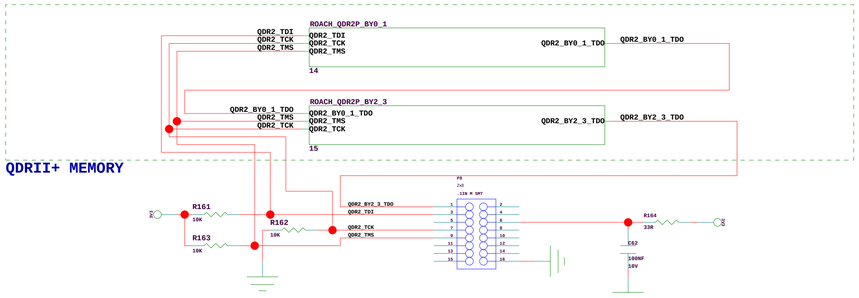


V5 DIFFERENTIAL GPIO

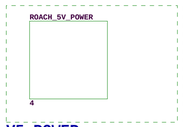
V5 SE GPIO & MISCELLANEOUS



GIGABIT TRANSCEIVERS



QDRII+ MEMORY



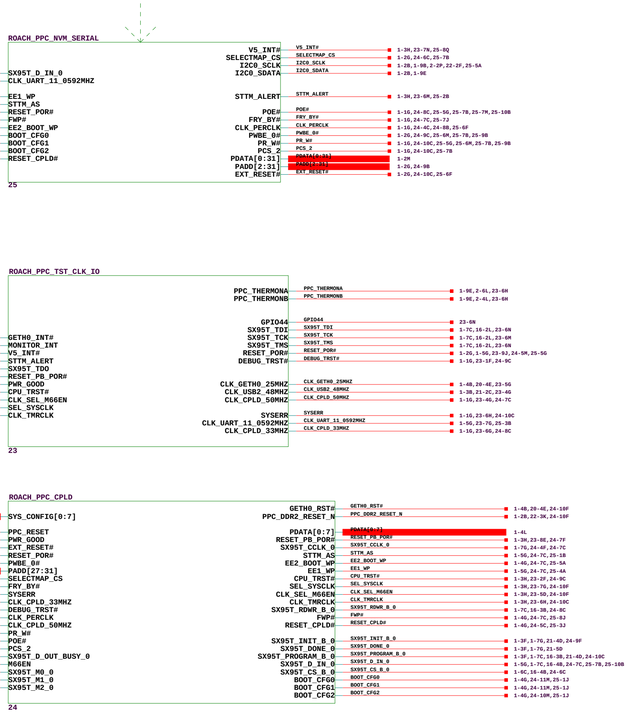
V5 POWER

VIRTEX5 CONFIGURATION

V5 SE GPIO & MISCELLANEOUS

PPC

PPC



MECHANICAL

BOARD FIDUCIALS

LOGO'S

PLACEHOLDER FOR PCB
MEERKAT LOGO

PLACEHOLDER FOR PCB
CASPER LOGO

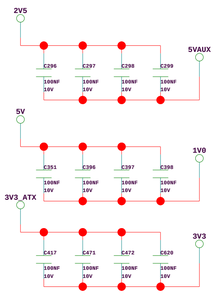
PLACEHOLDER FOR PCB
ROACH LOGO

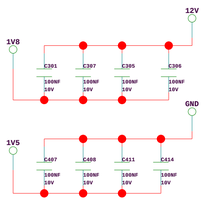
PLACEHOLDER FOR PCB
NRAO LOGO

BOARD SERIAL NUMBER

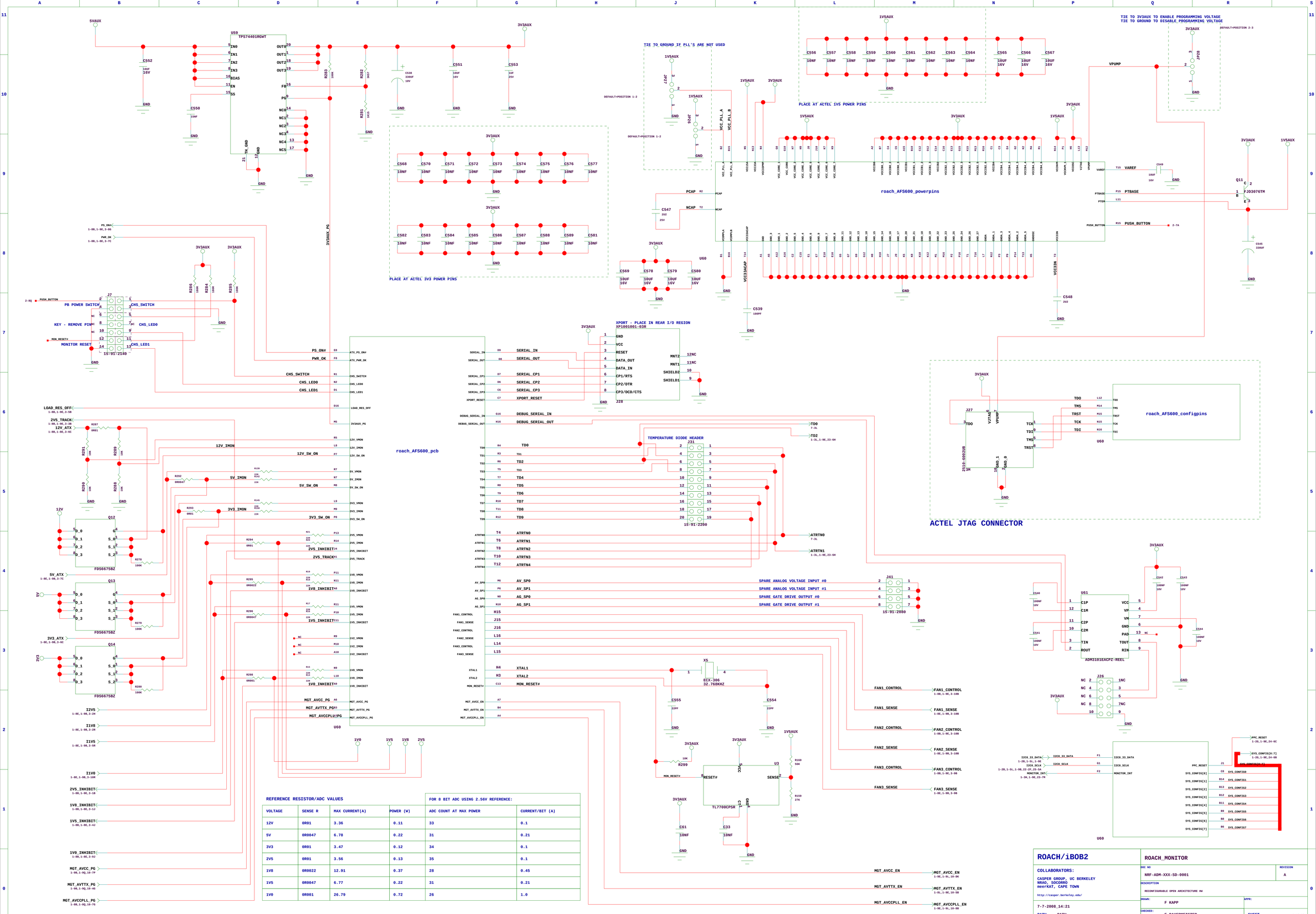
CONTRIBUTORS

ETIENNE BAUERMEISTER
HENRY CHEN
STEVE DURAND
FRANCOIS KAPP
ALAN LANGMAN
GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHIMER





ROACH/iBOB2	ROACH_TOP
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-7-2008_14:21	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 1 OF 25



REFERENCE RESISTOR/ADC VALUES				FOR 8 BIT ADC USING 2.56V REFERENCE:	
VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)	ADC COUNT AT MAX POWER	CURRENT/BIT (A)
12V	0R01	3.36	0.11	33	0.1
5V	0R0047	6.78	0.22	31	0.21
3V3	0R01	3.47	0.12	34	0.1
2V5	0R01	3.56	0.13	35	0.1
1V8	0R0022	12.91	0.37	28	0.45
1V5	0R0047	6.77	0.22	31	0.21
1V0	0R001	26.79	0.72	26	1.0

ROACH/iBOB2	ROACH_MONITOR
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A; DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-7-2008_14:21	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 2 OF 25

AUX FAN CONNECTORS - ATX 4 PIN

J21
1 GND
2 12V
3 SENSE
4 CONTROL
47053-1000

FAN1_SENSE 1-8E,1-9B,2-2B
FAN1_CONTROL 1-8B,1-9E,2-2M
FAN1_SENSE
FAN1_CONTROL
PLACE ON SILKSCREEN: FAN1

J20
1 GND
2 12V
3 SENSE
4 CONTROL
47053-1000

FAN2_SENSE 1-8E,1-9B,2-2M
FAN2_CONTROL 1-8B,1-9E,2-2M
FAN2_SENSE
FAN2_CONTROL
PLACE ON SILKSCREEN: FAN2

J19
1 GND
2 12V
3 SENSE
4 CONTROL
47053-1000

FAN3_SENSE 1-8E,1-9B,2-1K
FAN3_CONTROL 1-8B,1-9E,2-2H
FAN3_SENSE
FAN3_CONTROL
PLACE ON SILKSCREEN: FAN3

GND

ATX POWER CONNECTORS

5VAUX
N12V

J18
1 3V3_1
2 3V3_2
3 COM_1
4 5V_1
5 COM_2
6 5V_2
7 COM_3
8 PWR_OK
9 5VSB
10 12V1_1
11 12V1_2
12 3V3_3
13 3V3_4
14 _12V
15 COM_4
16 PS_ON#
17 COM_5
18 COM_6
19 COM_7
20 NC
21 5V_3
22 5V_4
23 5V_5
24 COM_8
44206-0007

PS_ON# 1-8B,1-9E,2-8B
PWR_OK 1-8B,1-8E,2-8B
PWR_OK
5VAUX

J32
2 1
4 3
6 5
8 7
10 9
8510-4500PL

5V_ATX 1-8E,1-9B,2-4A
3V3_ATX 1-8E,1-9B,2-3A
12V_ATX 1-8B,1-8E,2-6B

GND

LOAD RESISTORS FOR ATX PSU MIN LOAD
SWITCH OFF ONCE LOAD EXCEEDS MINIMUM SPEC
ADJUST RESISTOR VALUES FOR ACTUAL SUPPLY

5VAUX
R180 10K
Q9 NDS331N
R185 10R 5W AC05000001009JL800
Q8 BSS138
Q10 NDS331N
R187 56R 5W AC05000005609JL800
LOAD_RES_OFF 1-8B,1-9E,2-6B
R181 10K
GND

BOARD LAYOUT NOTE
SEPARATE GROUND RETURN CURRENTS FROM MAIN BOARD GROUND PLANES
BETWEEN POWER INPUT CONNECTORS AND REGULATOR AREA ON BOARD.

1V0
ROUTE FROM LOAD
R13 22R
PLACE RESISTOR CLOSE TO U50
ROUTE SHORTEST
R144 6R

PSU INPUT SUMMARY

VOLTAGE	5.0V +- 10%
CURRENT (MAX)	6.0A

5V
L6 BLM31PG121SN1B
L5 BLM31PG121SN1B
L16 BLM31PG121SN1B
C403 330UF 16V
C401 330UF 16V
C419 22UF 16V
GND

U50
30A SMPS MODULE
13 TURBOTRANS
10 SENSE+
2 VI_1
6 VI_0
1 INHIBIT/UVLADJ
14 TRACK
11 SENSE-
PTH05T210WAD
4 GND_3
7 GND_2
8 GND_1
3 GND_0

1V5
1V0_INHIBIT 1-8B,1-8E,2-6B
Q4 BSS138
ROUTE FROM LOAD

VO_0 5
VO_1 9
VOADJUST 12
R143 634K
DIRECT TO P8 ON U50, DEDICATED TRACE
C418 10UF
C117 10UF
C402 1000UF 2V5
C400 1000UF 2V5
C104 1000UF 2V5
C105 1000UF 2V5
I1V0 1-8E,1-9D,2-1B

PSU RAIL SUMMARY

VOLTAGE	1.0V +- 5%
SUPPLIES	FPGA CORE
CURRENT (QUIESCENT)	1.5A
CURRENT (ACTIVE)	26.8A
LOAD STEP	25.3A

1.2V SUPPLY DELETED - NOT REQUIRED

1V5
ROUTE FROM LOAD
R12 22R
PLACE RESISTOR CLOSE TO U51
ROUTE SHORTEST
R146 10K

PSU INPUT SUMMARY

VOLTAGE	12V +- 10%
CURRENT (MAX)	0.8A

12V
L7 BLM31PG121SN1B
C404 330UF 16V
C420 22UF 16V
GND

U51
16A SMPS MODULE
9 TURBOTRANS
6 SENSE+
2 VI
11 INHIBIT/UVLADJ
10 TRACK
7 SENSE-
1 SMARTSYNC
PTH08T240WAD
4 GND_1
3 GND_0

1V8
1V5_INHIBIT 1-8B,1-8E,2-1B
Q5 BSS138
ROUTE FROM LOAD

VO 5
VOADJUST 8
R147 649R
DIRECT TO P8 ON U51, DEDICATED TRACE
C421 10UF
C405 1000UF 2V5
I1V5 1-8E,1-9D,2-2B

PSU RAIL SUMMARY

VOLTAGE	1.5V +- 5%
SUPPLIES	FPGA IO, QDR, PPC
CURRENT (QUIESCENT)	0.25A
CURRENT (ACTIVE)	6.8A
LOAD STEP	6.55A

2V5
ROUTE FROM LOAD
R10 22R
PLACE RESISTOR CLOSE TO U53
ROUTE SHORTEST
R177 649R

PSU INPUT SUMMARY

VOLTAGE	12V +- 10%
CURRENT (MAX)	0.8A

2V5_TRACK 1-8B,1-9E,2-6B
R183 1K
12V
L15 BLM31PG121SN1B
C412 330UF 16V
C426 10UF
C424 22UF 16V
GND

U53
8 TURBOTRANS
5 SENSE+
2 VI
10 INHIBIT/UVLADJ
9 TRACK
6 SENSE-
1 SMARTSYNC
PTH08T230WAD
3 GND

VO 4
VOADJUST 7
R179 2K87
C425 10UF 16V
C413 680UF 4V
I2V5 1-8E,1-9D,2-2B
DIRECT TO P8 ON U53, DEDICATED TRACE

2V5_INHIBIT 1-8B,1-9E,2-1B
Q7 BSS138
ROUTE FROM LOAD

PSU RAIL SUMMARY

VOLTAGE	2.5V +- 5%
SUPPLIES	FPGA, ZDOK PPC, PHY
CURRENT (QUIESCENT)	0.1A
CURRENT (ACTIVE)	3.6A
LOAD STEP	3.5A

1V8
ROUTE FROM LOAD
R11 22R
PLACE RESISTOR CLOSE TO U52
ROUTE SHORTEST
R149 243R

PSU INPUT SUMMARY

VOLTAGE	12V +- 10%
CURRENT (MAX)	1.8A

12V
L14 BLM31PG121SN1B
C409 330UF 16V
C423 22UF 16V
GND

U27
16A SMPS MODULE
9 TURBOTRANS
6 SENSE+
2 VI
11 INHIBIT/UVLADJ
10 TRACK
7 SENSE-
1 SMARTSYNC
PTH08T220WAD
4 GND_1
3 GND_0

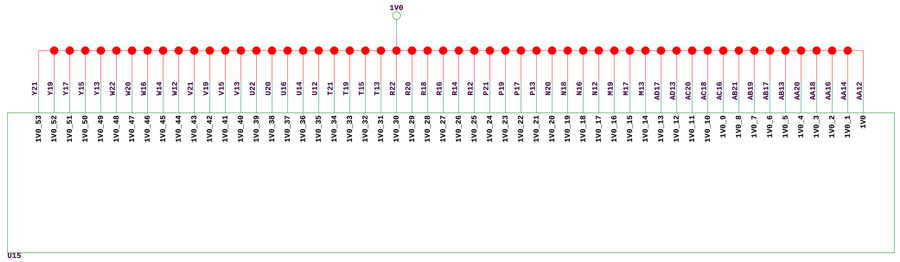
2V5
1V8_INHIBIT 1-8B,1-8E,2-1B
Q6 BSS138
ROUTE FROM LOAD

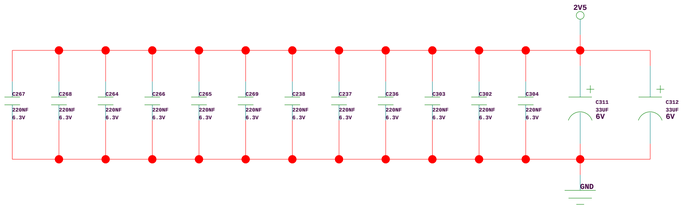
VO 5
VOADJUST 8
R148 487R
DIRECT TO P8 ON PTH08T210W, DEDICATED TRACE
C422 10UF
C410 1000UF 2V5
I1V8 1-8E,1-9D,2-2B

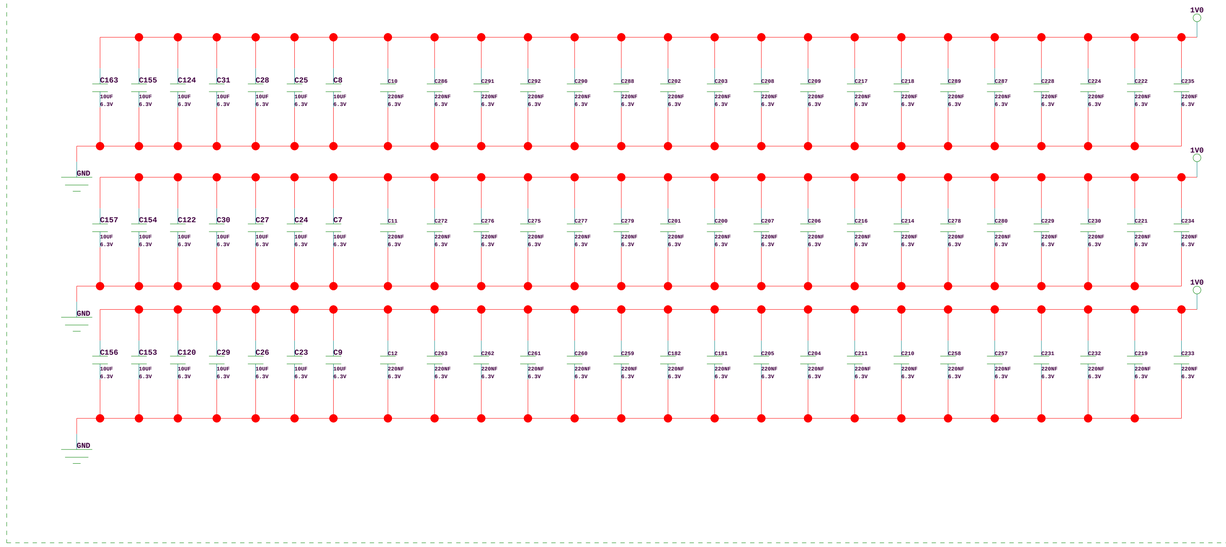
PSU RAIL SUMMARY

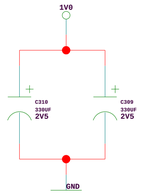
VOLTAGE	1.8V +- 5%
SUPPLIES	FPGA IO, DDR2 x 2
CURRENT (QUIESCENT)	1A
CURRENT (ACTIVE)	12.9A
LOAD STEP	11.9A

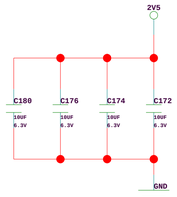
ROACH/iBOB2	ROACH_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-7-2008_14:21	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 3 OF 25

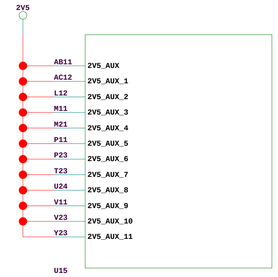


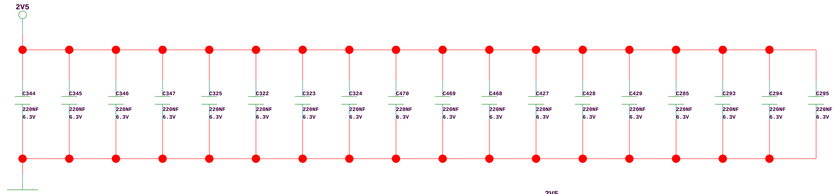


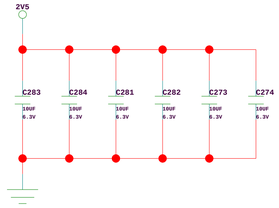


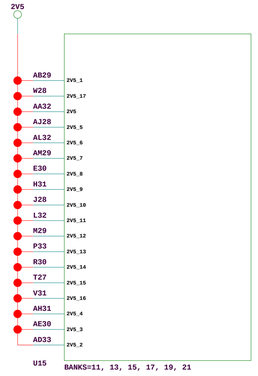


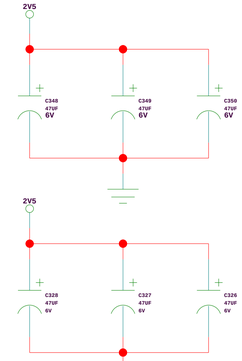


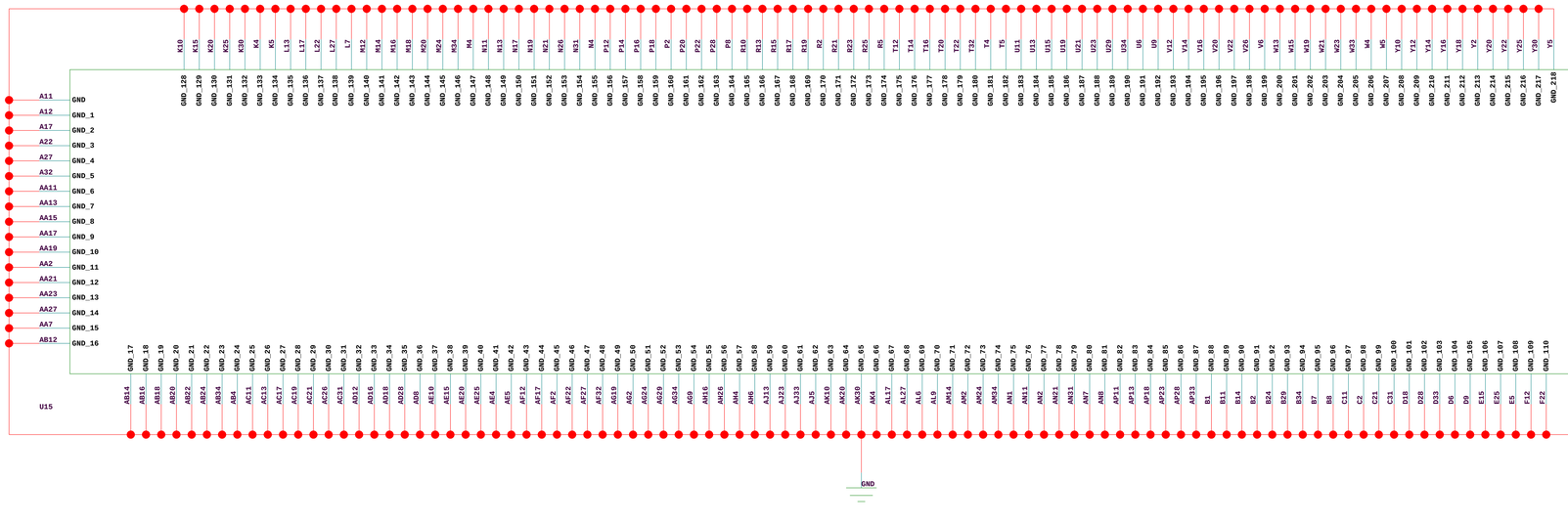












ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
7-7-2008_14:21 PATH PATH	

| | | |

A		B		C		D		E		F		G		H		J		K		L		M		

7																								7
6																								6
5																								5
4																								4
3																								3
2																								2
1																								1
0																								0

6-5L ZDOK1_CLK0_P H17 → ZDOK1_CLK0_P
6-5L ZDOK1_CLK0_N H18 → ZDOK1_CLK0_N
6-3L ZDOK1_CLK1_P K17 → ZDOK1_CLK1_P
6-3L ZDOK1_CLK1_N L18 → ZDOK1_CLK1_N

ZDOK1_DP_P[37]	AD31	ZDOK1_DP_P37	6-3L
ZDOK1_DP_N[37]	AE31	ZDOK1_DP_N37	6-3L
ZDOK1_DP_P[36]	AF33	ZDOK1_DP_P36	6-3L
ZDOK1_DP_N[36]	AE33	ZDOK1_DP_N36	6-3L
ZDOK1_DP_P[35]	AF31	ZDOK1_DP_P35	6-4L
ZDOK1_DP_N[35]	AG31	ZDOK1_DP_N35	6-4L
ZDOK1_DP_P[34]	AG32	ZDOK1_DP_P34	6-4L
ZDOK1_DP_N[34]	AH32	ZDOK1_DP_N34	6-4L
ZDOK1_DP_P[33]	AG28	ZDOK1_DP_P33	6-4L
ZDOK1_DP_N[33]	AH28	ZDOK1_DP_N33	6-4L
ZDOK1_DP_P[32]	AF24	ZDOK1_DP_P32	6-4L
ZDOK1_DP_N[32]	AG25	ZDOK1_DP_N32	6-4L
ZDOK1_DP_P[31]	AJ30	ZDOK1_DP_P31	6-4L
ZDOK1_DP_N[31]	AH30	ZDOK1_DP_N31	6-4L
ZDOK1_DP_P[30]	AK28	ZDOK1_DP_P30	6-5L
ZDOK1_DP_N[30]	AK27	ZDOK1_DP_N30	6-5L
ZDOK1_DP_P[29]	AK26	ZDOK1_DP_P29	6-5L
ZDOK1_DP_N[29]	AJ27	ZDOK1_DP_N29	6-5L
ZDOK1_DP_P[28]	AB27	ZDOK1_DP_P28	6-5L
ZDOK1_DP_N[28]	AC27	ZDOK1_DP_N28	6-5L
ZDOK1_DP_P[27]	AD30	ZDOK1_DP_P27	6-5L
ZDOK1_DP_N[27]	AC29	ZDOK1_DP_N27	6-5L
ZDOK1_DP_P[26]	AE29	ZDOK1_DP_P26	6-6L
ZDOK1_DP_N[26]	AD29	ZDOK1_DP_N26	6-6L
ZDOK1_DP_P[25]	AG33	ZDOK1_DP_P25	6-6L
ZDOK1_DP_N[25]	AH33	ZDOK1_DP_N25	6-6L
ZDOK1_DP_P[24]	AF29	ZDOK1_DP_P24	6-6L
ZDOK1_DP_N[24]	AF30	ZDOK1_DP_N24	6-6L
ZDOK1_DP_P[23]	AG27	ZDOK1_DP_P23	6-6L
ZDOK1_DP_N[23]	AG26	ZDOK1_DP_N23	6-6L
ZDOK1_DP_P[22]	AK34	ZDOK1_DP_P22	6-6L
ZDOK1_DP_N[22]	AK33	ZDOK1_DP_N22	6-6L
ZDOK1_DP_P[21]	AL34	ZDOK1_DP_P21	6-7L
ZDOK1_DP_N[21]	AL33	ZDOK1_DP_N21	6-7L
ZDOK1_DP_P[20]	AJ25	ZDOK1_DP_P20	6-7L
ZDOK1_DP_N[20]	AH25	ZDOK1_DP_N20	6-7L
ZDOK1_DP_P[19]	AB30	ZDOK1_DP_P19	6-3J
ZDOK1_DP_N[19]	AC30	ZDOK1_DP_N19	6-3J
ZDOK1_DP_P[18]	AC28	ZDOK1_DP_P18	6-3J
ZDOK1_DP_N[18]	AD27	ZDOK1_DP_N18	6-3J
ZDOK1_DP_P[17]	AC25	ZDOK1_DP_P17	6-3J
ZDOK1_DP_N[17]	AC24	ZDOK1_DP_N17	6-3J
ZDOK1_DP_P[16]	AE28	ZDOK1_DP_P16	6-4J
ZDOK1_DP_N[16]	AF28	ZDOK1_DP_N16	6-4J
ZDOK1_DP_P[15]	AD24	ZDOK1_DP_P15	6-4J
ZDOK1_DP_N[15]	AE24	ZDOK1_DP_N15	6-4J
ZDOK1_DP_P[14]	AF25	ZDOK1_DP_P14	6-4J
ZDOK1_DP_N[14]	AF26	ZDOK1_DP_N14	6-4J
ZDOK1_DP_P[13]	AH29	ZDOK1_DP_P13	6-4J
ZDOK1_DP_N[13]	AG30	ZDOK1_DP_N13	6-4J
ZDOK1_DP_P[12]	AH27	ZDOK1_DP_P12	6-4J
ZDOK1_DP_N[12]	AJ26	ZDOK1_DP_N12	6-4J
ZDOK1_DP_P[11]	AM33	ZDOK1_DP_P11	6-5J
ZDOK1_DP_N[11]	AM32	ZDOK1_DP_N11	6-5J
ZDOK1_DP_P[10]	AN32	ZDOK1_DP_P10	6-5J
ZDOK1_DP_N[10]	AP32	ZDOK1_DP_N10	6-5J
ZDOK1_DP_P[9]	AC34	ZDOK1_DP_P9	6-5J
ZDOK1_DP_N[9]	AD34	ZDOK1_DP_N9	6-5J
ZDOK1_DP_P[8]	AD32	ZDOK1_DP_P8	6-5J
ZDOK1_DP_N[8]	AE32	ZDOK1_DP_N8	6-5J
ZDOK1_DP_P[7]	AF34	ZDOK1_DP_P7	6-5J
ZDOK1_DP_N[7]	AE34	ZDOK1_DP_N7	6-5J
ZDOK1_DP_P[6]	AD26	ZDOK1_DP_P6	6-6J
ZDOK1_DP_N[6]	AD25	ZDOK1_DP_N6	6-6J
ZDOK1_DP_P[5]	AE27	ZDOK1_DP_P5	6-6J
ZDOK1_DP_N[5]	AE26	ZDOK1_DP_N5	6-6J
ZDOK1_DP_P[4]	AH34	ZDOK1_DP_P4	6-6J
ZDOK1_DP_N[4]	AJ34	ZDOK1_DP_N4	6-6J
ZDOK1_DP_P[3]	AJ32	ZDOK1_DP_P3	6-6J
ZDOK1_DP_N[3]	AK32	ZDOK1_DP_N3	6-6J
ZDOK1_DP_P[2]	AJ31	ZDOK1_DP_P2	6-6J
ZDOK1_DP_N[2]	AK31	ZDOK1_DP_N2	6-6J
ZDOK1_DP_P[1]	AK29	ZDOK1_DP_P1	6-7J
ZDOK1_DP_N[1]	AJ29	ZDOK1_DP_N1	6-7J
ZDOK1_DP_P[0]	AN34	ZDOK1_DP_P0	6-7J
ZDOK1_DP_N[0]	AN33	ZDOK1_DP_N0	6-7J

U15
BANKS=11, 13, 15, 17, 19, 21

5V
3V3
2V5
1V8

C337 1UF 16V — C336 100NF 10V
C339 1UF 16V — C338 100NF 10V
C340 1UF 16V — C341 100NF 10V
C343 1UF 16V — C342 100NF 10V

P7

W1	W1	B1	B1
X1	X1	B2	B2
Y1	Y1	B3	B3
Z1	Z1	B4	B4
W2	W2	B5	B5
X2	X2	B6	B6
Y2	Y2	B7	B7
Z2	Z2	B8	B8
W3	W3	B9	B9
X3	X3	B10	B10
Y3	Y3	B11	B11
Z3	Z3	B12	B12
W4	W4	B13	B13
X4	X4	B14	B14
Y4	Y4	B15	B15
Z4	Z4	B16	B16
W5	W5	B17	B17
X5	X5	B18	B18
Y5	Y5	B19	B19
Z5	Z5	B20	B20
W6	W6	E1	E1
X6	X6	E2	E2
Y6	Y6	E3	E3
Z6	Z6	E4	E4
		E5	E5
		E6	E6
		E7	E7
		E8	E8
		E9	E9
		E10	E10
		E11	E11
		E12	E12
		E13	E13
		E14	E14
		E15	E15
		E16	E16
		E17	E17
		E18	E18
		E19	E19
		E20	E20

6367550-5
ZDOK40

P7

6-0E	ZDOK1_DP_P0	A1	A1	C1	ZDOK1_DP_P20 6-4E
6-0E	ZDOK1_DP_N0	A2	A2	C2	ZDOK1_DP_N20 6-4E
6-0E	ZDOK1_DP_P1	A3	A3	C3	ZDOK1_DP_P21 6-4E
6-0E	ZDOK1_DP_N1	A4	A4	C4	ZDOK1_DP_N21 6-4E
6-0E	ZDOK1_DP_P2	A5	A5	C5	ZDOK1_DP_P22 6-4E
6-0E	ZDOK1_DP_N2	A6	A6	C6	ZDOK1_DP_N22 6-4E
6-1E	ZDOK1_DP_P3	A7	A7	C7	ZDOK1_DP_P23 6-5E
6-1E	ZDOK1_DP_N3	A8	A8	C8	ZDOK1_DP_N23 6-5E
6-1E	ZDOK1_DP_P4	A9	A9	C9	ZDOK1_DP_P24 6-5E
6-1E	ZDOK1_DP_N4	A10	A10	C10	ZDOK1_DP_N24 6-5E
6-1E	ZDOK1_DP_P5	A11	A11	C11	ZDOK1_DP_P25 6-5E
6-1E	ZDOK1_DP_N5	A12	A12	C12	ZDOK1_DP_N25 6-5E
6-1E	ZDOK1_DP_P6	A13	A13	C13	ZDOK1_DP_P26 6-5E
6-1E	ZDOK1_DP_N6	A14	A14	C14	ZDOK1_DP_N26 6-5E
6-1E	ZDOK1_DP_P7	A15	A15	C15	ZDOK1_DP_P27 6-5E
6-1E	ZDOK1_DP_N7	A16	A16	C16	ZDOK1_DP_N27 6-5E
6-2E	ZDOK1_DP_P8	A17	A17	C17	ZDOK1_DP_P28 6-6E
6-2E	ZDOK1_DP_N8	A18	A18	C18	ZDOK1_DP_N28 6-6E
6-2E	ZDOK1_DP_P9	A19	A19	C19	ZDOK1_CLK0_P 6-7B
6-2E	ZDOK1_DP_N9	A20	A20	C20	ZDOK1_CLK0_N 6-7B
6-2E	ZDOK1_DP_P10	D1	D1	F1	ZDOK1_DP_P29 6-6E
6-2E	ZDOK1_DP_N10	D2	D2	F2	ZDOK1_DP_N29 6-6E
6-2E	ZDOK1_DP_P11	D3	D3	F3	ZDOK1_DP_P30 6-6E
6-2E	ZDOK1_DP_N11	D4	D4	F4	ZDOK1_DP_N30 6-6E
6-2E	ZDOK1_DP_P12	D5	D5	F5	ZDOK1_DP_P31 6-6E
6-2E	ZDOK1_DP_N12	D6	D6	F6	ZDOK1_DP_N31 6-6E
6-3E	ZDOK1_DP_P13	D7	D7	F7	ZDOK1_DP_P32 6-6E
6-3E	ZDOK1_DP_N13	D8	D8	F8	ZDOK1_DP_N32 6-6E
6-3E	ZDOK1_DP_P14	D9	D9	F9	ZDOK1_DP_P33 6-7E
6-3E	ZDOK1_DP_N14	D10	D10	F10	ZDOK1_DP_N33 6-7E
6-3E	ZDOK1_DP_P15	D11	D11	F11	ZDOK1_DP_P34 6-7E
6-3E	ZDOK1_DP_N15	D12	D12	F12	ZDOK1_DP_N34 6-7E
6-3E	ZDOK1_DP_P16	D13	D13	F13	ZDOK1_DP_P35 6-7E
6-3E	ZDOK1_DP_N16	D14	D14	F14	ZDOK1_DP_N35 6-7E
6-3E	ZDOK1_DP_P17	D15	D15	F15	ZDOK1_DP_P36 6-7E
6-3E	ZDOK1_DP_N17	D16	D16	F16	ZDOK1_DP_N36 6-7E
6-4E	ZDOK1_DP_P18	D17	D17	F17	ZDOK1_DP_P37 6-7E
6-4E	ZDOK1_DP_N18	D18	D18	F18	ZDOK1_DP_N37 6-7E
6-4E	ZDOK1_DP_P19	D19	D19	F19	ZDOK1_CLK1_P 6-7B
6-4E	ZDOK1_DP_N19	D20	D20	F20	ZDOK1_CLK1_N 6-7B

6367550-5

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

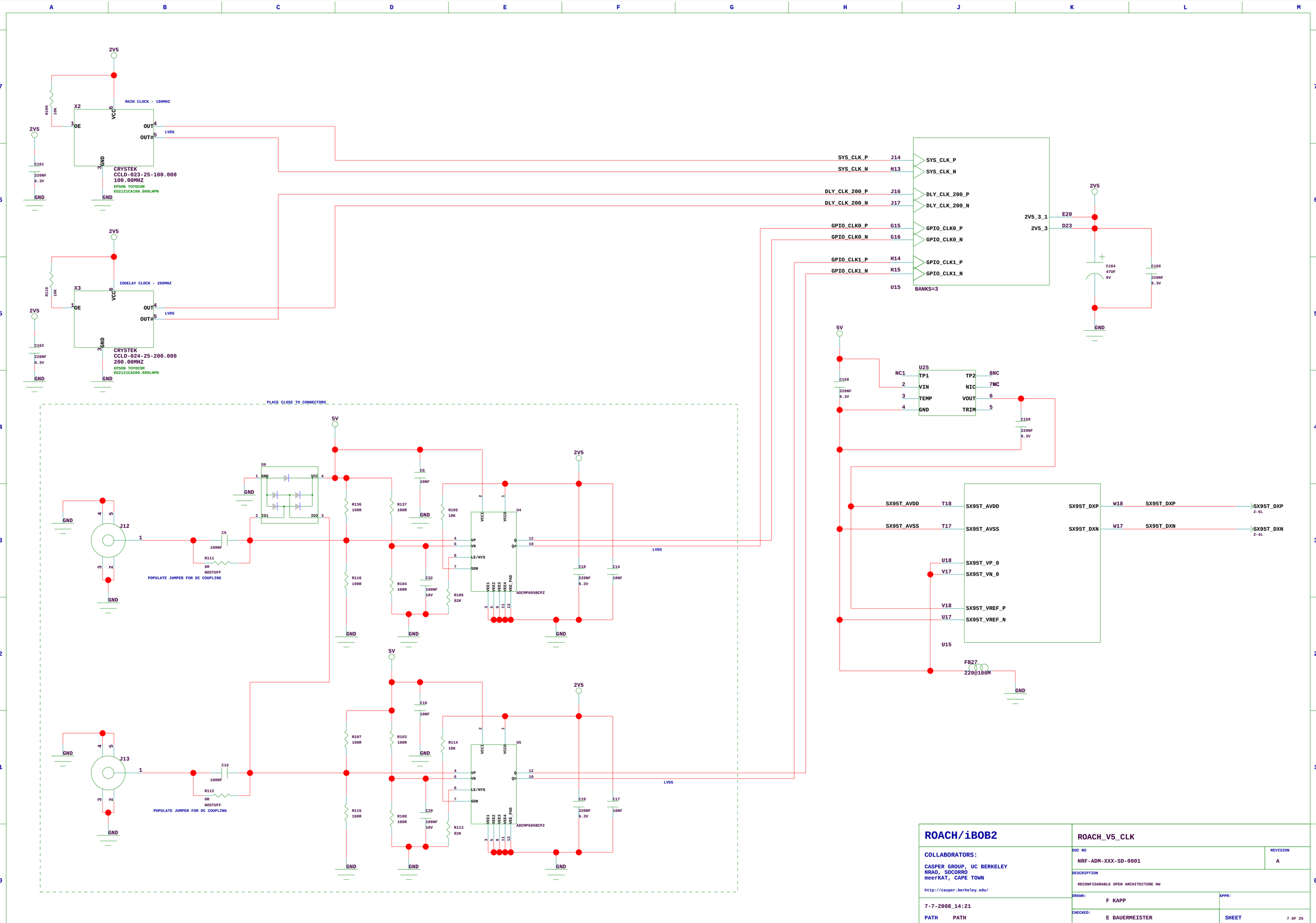
http://casper.berkeley.edu/

7-7-2008_14:21

PATH PATH

ROACH_ADC_1

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	6 OF 25



ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

7-7-2008_14:21

PATH PATH

ROACH_V5_CLK

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

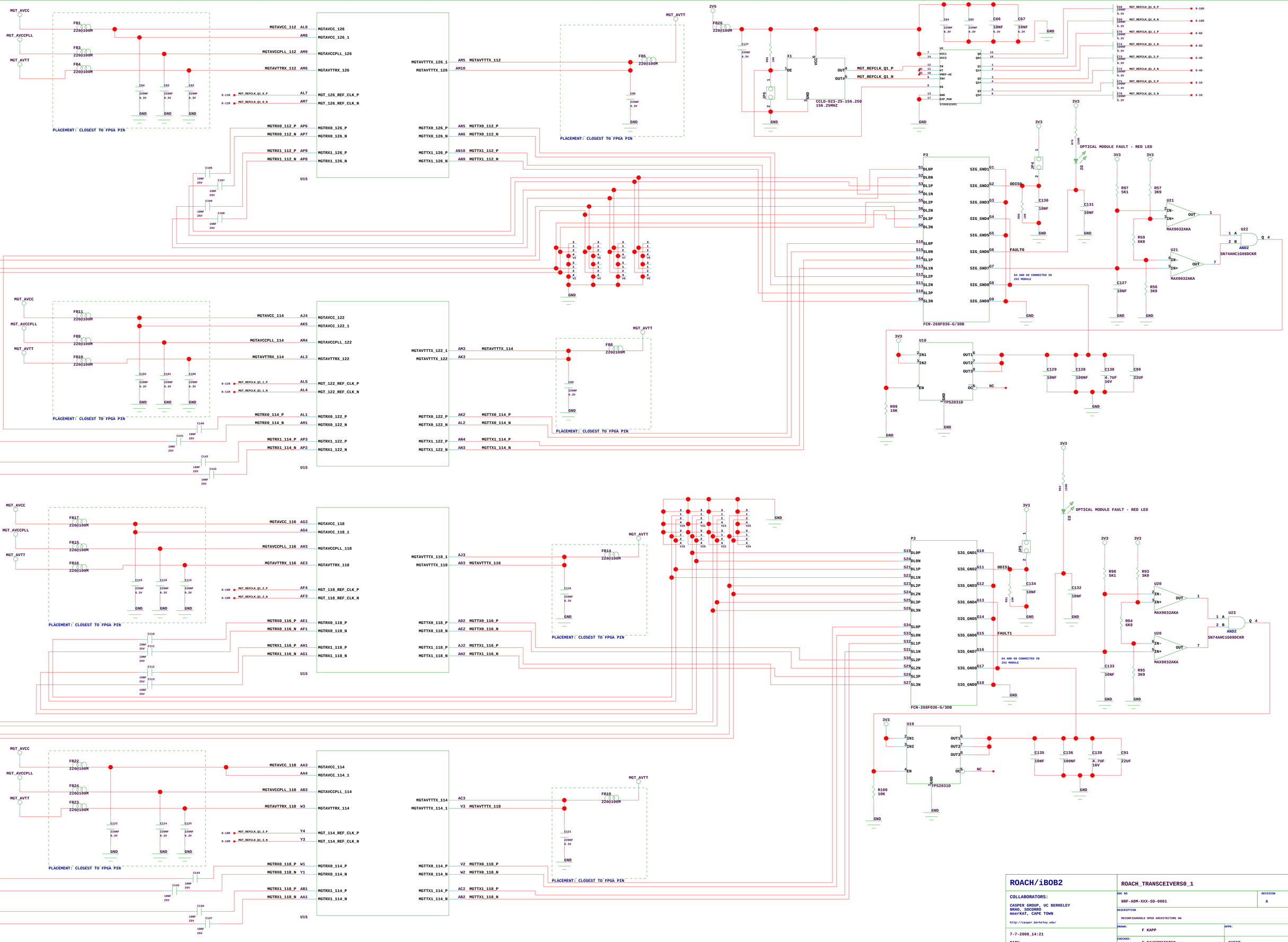
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 7 OF 25


MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB3 220@100M
FB4 220@100M
C84 220NF 6.3V
C93 220NF 6.3V
C92 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_112 AL8 MGTAVCC_126
AM8 MGTAVCC_126_1
MGTAVCCPLL_112 AM9 MGTAVCCPLL_126
MGTAVTTRX_112 AM6 MGTAVTTRX_126
B-11R MGT_REFCLK_Q3_0_P AL7 MGT_126_REF_CLK_P
B-11R MGT_REFCLK_Q3_0_N AM7 MGT_126_REF_CLK_N
MGTRX0_112_P AP6 MGTRX0_126_P
MGTRX0_112_N AP7 MGTRX0_126_N
MGTRX1_112_P AP9 MGTRX1_126_P
MGTRX1_112_N AP8 MGTRX1_126_N
U15
MGTAVTTTX_126_1 AM5 MGTAVTTTX_112
MGTAVTTTX_126 AM10
MGTTX0_126_P AN5 MGTTX0_112_P
MGTTX0_126_N AN6 MGTTX0_112_N
MGTTX1_126_P AN10 MGTTX1_112_P
MGTTX1_126_N AN9 MGTTX1_112_N
MGT_AVTT
FB5 220@100M
C96 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C106 10NF 25V
C107 10NF 25V
C109 10NF 25V
C108 10NF 25V
V2 V3 V4 V5 V6 V7 V8
GND
2V5
FB26 220@100M
C137 220NF 6.3V
R84 10K
X1
OE
VCC
OUT
GND
JP6
CCLD-023-25-156.250
156.25MHZ
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
C64 220NF 6.3V
C65 220NF 6.3V
C66 10NF 6.3V
C67 10NF 6.3V
U8
VCC1
VCC2
IN
VT
VREF-AC
CMF
EN
GND
EXP_PAD
SY89832UMI
Q0 Q0# Q1 Q1# Q2 Q2# Q3 Q3#
C68 100NF 6.3V MGT_REFCLK_Q1_0_P B-10D
C69 100NF 6.3V MGT_REFCLK_Q1_0_N B-10D
C75 100NF 6.3V MGT_REFCLK_Q1_1_P B-6D
C74 100NF 6.3V MGT_REFCLK_Q1_1_N B-6D
C73 100NF 6.3V MGT_REFCLK_Q1_2_P B-4D
C72 100NF 6.3V MGT_REFCLK_Q1_2_N B-4D
C71 100NF 6.3V MGT_REFCLK_Q1_3_P B-1D
C70 100NF 6.3V MGT_REFCLK_Q1_3_N B-1D
P3
S1 DL0P
S2 DL0N
S3 DL1P
S4 DL1N
S5 DL2P
S6 DL2N
S7 DL3P
S8 DL3N
S16 SL0P
S15 SL0N
S14 SL1P
S13 SL1N
S12 SL2P
S11 SL2N
S10 SL3P
S9 SL3N
SIG_GND1 G1
SIG_GND2 G2
SIG_GND3 G3
SIG_GND4 G4
SIG_GND5 G5
SIG_GND6 G6
SIG_GND7 G7
SIG_GND8 G8
SIG_GND9 G9
ODIS0
FAULT0
G4 AND G8 CONNECTED IN 2X2 MODULE
FCN-268F036-G/3DB
3V3
JP4
R85 10K
C130 10NF
C131 10NF
R79 100R
D2
OPTICAL MODULE FAULT - RED LED
R97 5K1
RS7 3K9
RS9 6K8
RS8 3K9
U21 MAX9032AKA
U22 AND2 SN74AHC1G08DCKR
C127 10NF
U18 TPS2031D
IN1 IN2 EN
OUT1 OUT2 OUT3
OC NC
R99 10K
C129 10NF
C128 100NF
C138 4.7UF 16V
C90 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB11 220@100M
FB9 220@100M
FB10 220@100M
C102 220NF 6.3V
C101 220NF 6.3V
C100 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_114 AJ4 MGTAVCC_122
AK5 MGTAVCC_122_1
MGTAVCCPLL_114 AM4 MGTAVCCPLL_122
MGTAVTTRX_114 AL3 MGTAVTTRX_122
B-11R MGT_REFCLK_Q3_1_P AL5 MGT_122_REF_CLK_P
B-11R MGT_REFCLK_Q3_1_N AL4 MGT_122_REF_CLK_N
MGTRX0_114_P AL1 MGTRX0_122_P
MGTRX0_114_N AM1 MGTRX0_122_N
MGTRX1_114_P AP3 MGTRX1_122_P
MGTRX1_114_N AP2 MGTRX1_122_N
U15
MGTAVTTTX_122_1 AM3 MGTAVTTTX_114
MGTAVTTTX_122 AK3
MGTTX0_122_P AK2 MGTTX0_114_P
MGTTX0_122_N AL2 MGTTX0_114_N
MGTTX1_122_P AN4 MGTTX1_114_P
MGTTX1_122_N AN3 MGTTX1_114_N
FB8 220@100M
C99 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C140 10NF 25V
C141 10NF 25V
C142 10NF 25V
C143 10NF 25V
V9 V10 V11 V12 V13 V14 V15 V16
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB17 220@100M
FB15 220@100M
FB16 220@100M
C119 220NF 6.3V
C118 220NF 6.3V
C115 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_116 AG3 MGTAVCC_118
AG4 MGTAVCC_118_1
MGTAVCCPLL_116 AH3 MGTAVCCPLL_118
MGTAVTTRX_116 AE3 MGTAVTTRX_118
B-10R MGT_REFCLK_Q3_2_P AF4 MGT_118_REF_CLK_P
B-10R MGT_REFCLK_Q3_2_N AF3 MGT_118_REF_CLK_N
MGTRX0_116_P AE1 MGTRX0_118_P
MGTRX0_116_N AF1 MGTRX0_118_N
MGTRX1_116_P AH1 MGTRX1_118_P
MGTRX1_116_N AG1 MGTRX1_118_N
U15
MGTAVTTTX_118_1 AJ3
MGTAVTTTX_118 AD3 MGTAVTTTX_116
MGTTX0_118_P AD2 MGTTX0_116_P
MGTTX0_118_N AE2 MGTTX0_116_N
MGTTX1_118_P AJ2 MGTTX1_116_P
MGTTX1_118_N AH2 MGTTX1_116_N
FB14 220@100M
C110 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C110 10NF 25V
C111 10NF 25V
C112 10NF 25V
C113 10NF 25V
V17 V18 V19 V20 V21 V22 V23 V24 V25
GND
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB22 220@100M
FB24 220@100M
FB23 220@100M
C123 220NF 6.3V
C114 220NF 6.3V
C125 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_118 AA3 MGTAVCC_114
AA4 MGTAVCC_114_1
MGTAVCCPLL_118 AB3 MGTAVCCPLL_114
MGTAVTTRX_118 W3 MGTAVTTRX_114
B-10R MGT_REFCLK_Q3_3_P Y4 MGT_114_REF_CLK_P
B-10R MGT_REFCLK_Q3_3_N Y3 MGT_114_REF_CLK_N
MGTRX0_118_P W1 MGTRX0_114_P
MGTRX0_118_N Y1 MGTRX0_114_N
MGTRX1_118_P AB1 MGTRX1_114_P
MGTRX1_118_N AA1 MGTRX1_114_N
U15
MGTAVTTTX_114 AC3
MGTAVTTTX_114_1 V3 MGTAVTTTX_118
MGTTX0_114_P V2 MGTTX0_118_P
MGTTX0_114_N W2 MGTTX0_118_N
MGTTX1_114_P AC2 MGTTX1_118_P
MGTTX1_114_N AB2 MGTTX1_118_N
FB19 220@100M
C121 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C144 10NF 25V
C145 10NF 25V
C146 10NF 25V
C147 10NF 25V
V26 V27 V28 V29 V30 V31 V32 V33 V34
GND
P3
S19 DL0P
S20 DL0N
S21 DL1P
S22 DL1N
S23 DL2P
S24 DL2N
S25 DL3P
S26 DL3N
S34 SL0P
S33 SL0N
S32 SL1P
S31 SL1N
S30 SL2P
S29 SL2N
S28 SL3P
S27 SL3N
SIG_GND1 G10
SIG_GND2 G11
SIG_GND3 G12
SIG_GND4 G13
SIG_GND5 G14
SIG_GND6 G15
SIG_GND7 G16
SIG_GND8 G17
SIG_GND9 G18
ODIS1
FAULT1
G4 AND G8 CONNECTED IN 2X2 MODULE
FCN-268F036-G/3DB
3V3
JP5
R91 10K
C134 10NF
C132 10NF
RS2 100R
D3
OPTICAL MODULE FAULT - RED LED
R98 5K1
R93 3K9
R94 6K8
R95 3K9
U20 MAX9032AKA
U23 AND2 SN74AHC1G08DCKR
C133 10NF
U19 TPS2031D
IN1 IN2 EN
OUT1 OUT2 OUT3
OC NC
R100 10K
C135 10NF
C136 100NF
C139 4.7UF 16V
C91 22UF
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
7-7-2008_14:21
PATH
ROACH_TRANSCEIVERS0_1
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE MW
DRAWN: F KAPP
CHECKED: E BAUERMEISTER
APPR:
SHEET 8 OF 25

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

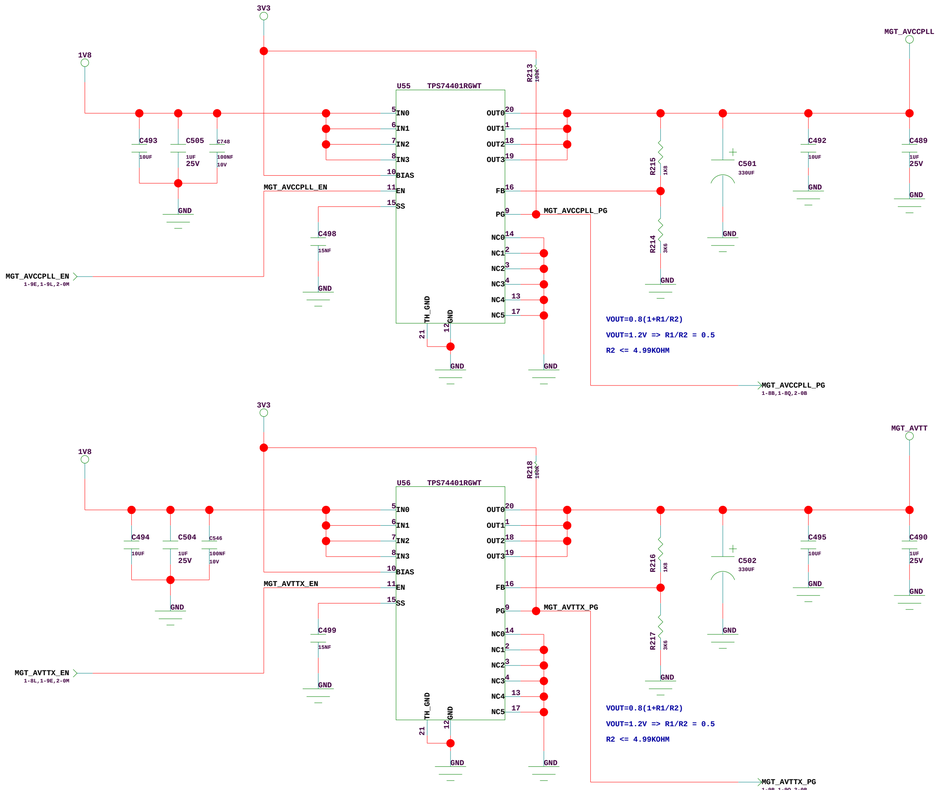
G4 AND G8 CONNECTED IN 2X2 MODULE

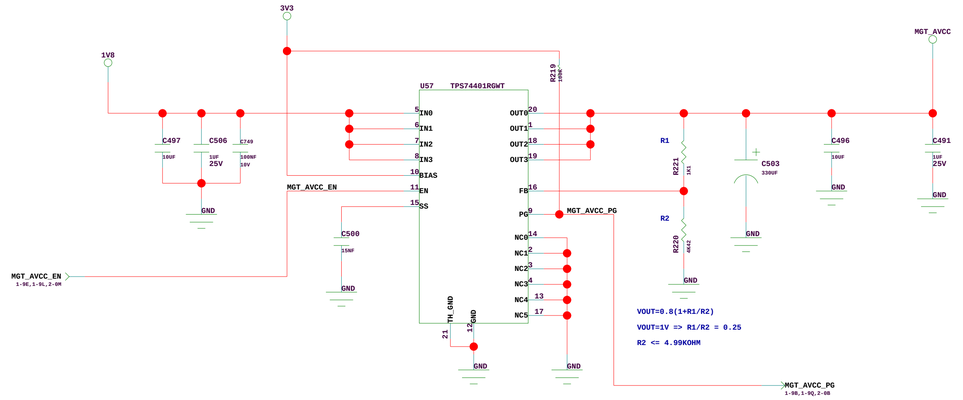
OPTICAL MODULE FAULT - RED LED

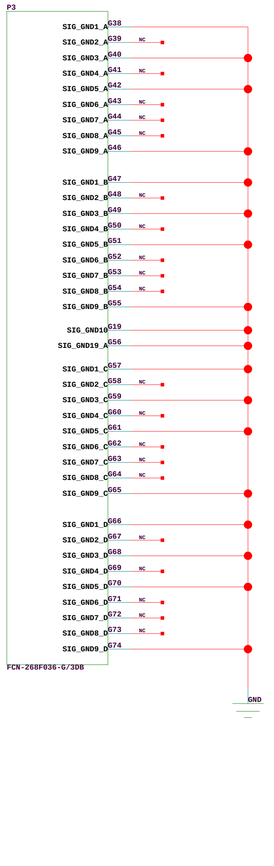
CCLD-023-25-156.250 156.25MHZ

FCN-268F036-G/3DB

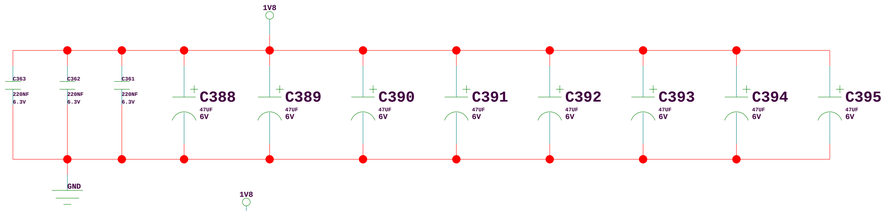
ROACH/iBOB2	ROACH_TRANSCEIVERS2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-7-2008_14:21	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 9 OF 25

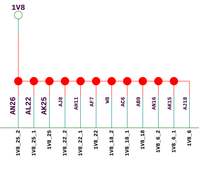


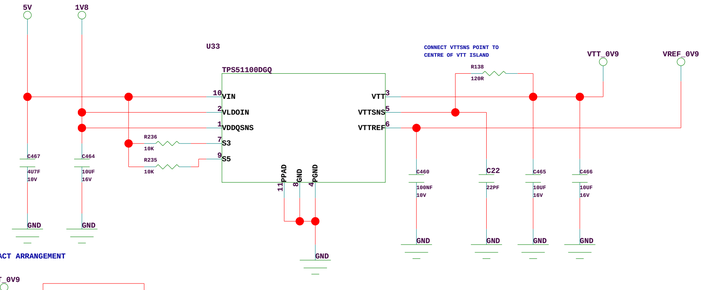




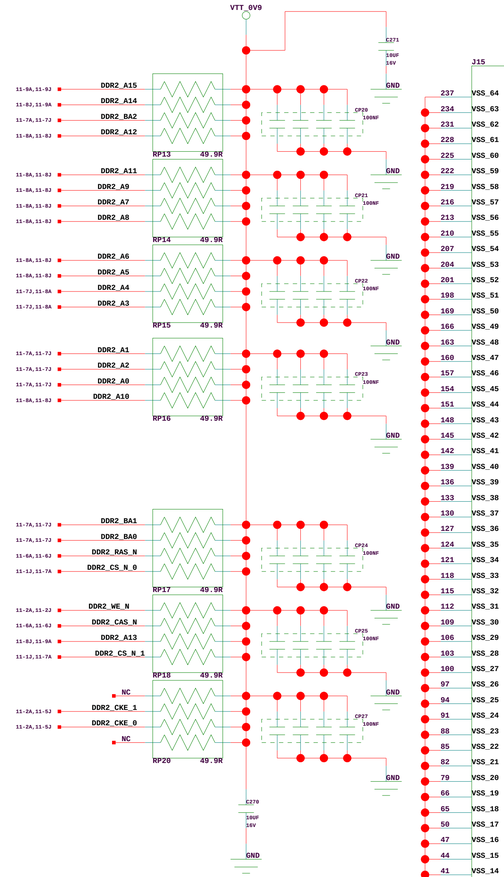
ROACH/iBOB2	ROACH_TRANSCEIVERS_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-7-2008_14:21	DRAWN: F KAPP · APPR:
PATH PATH	CHECKED: E BAUERMEISTER · SHEET 10 OF 25

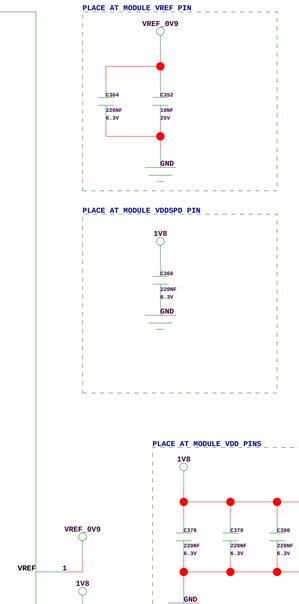


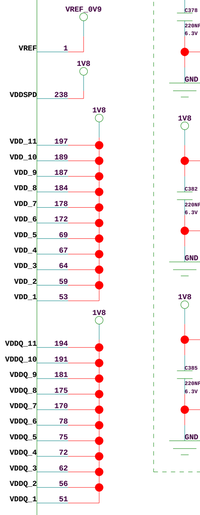




VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
PLACE ONE 10uF CAPACITOR ON EITHER END OF ISLAND



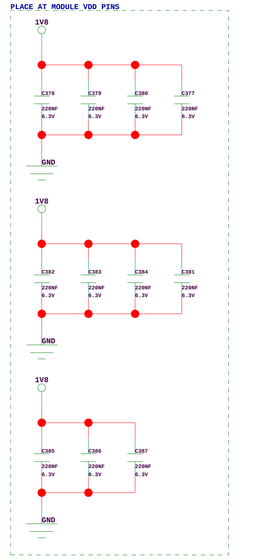


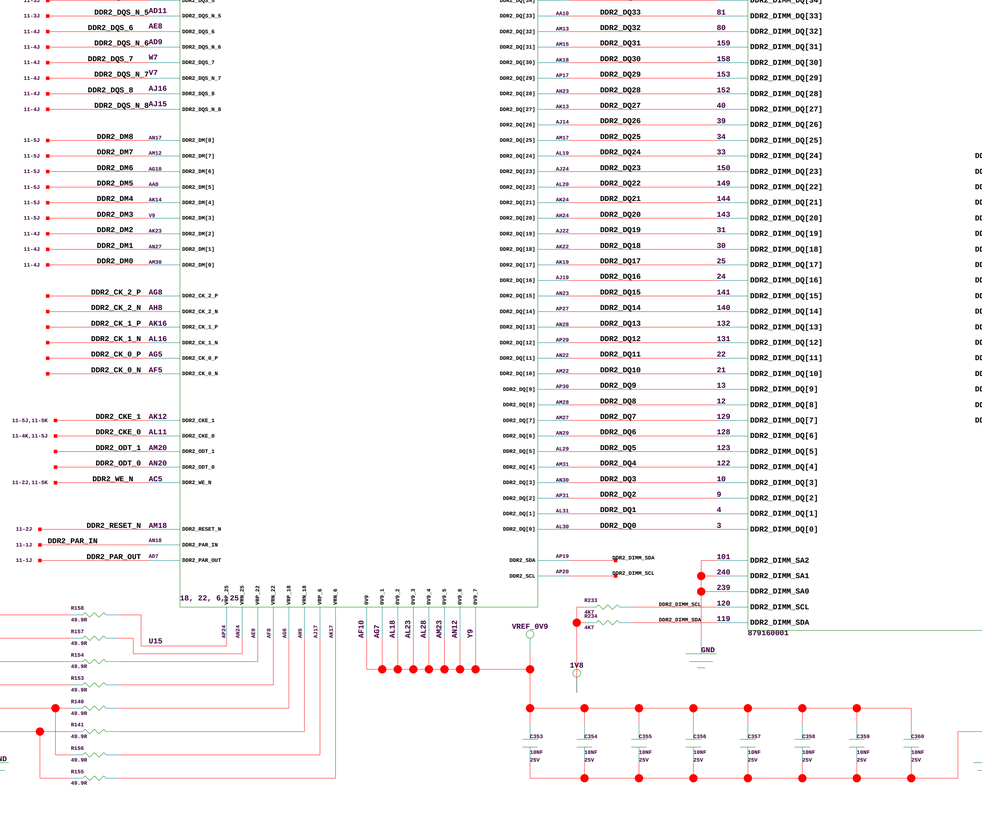


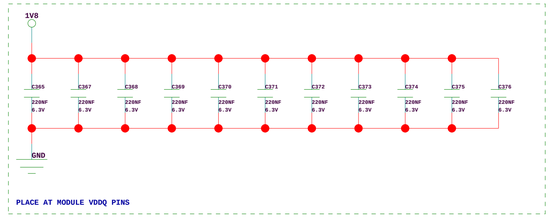
PLACE AT MODULE VREF PIN

PLACE AT MODULE VDDSPD PIN

PLACE AT MODULE VDD PINS

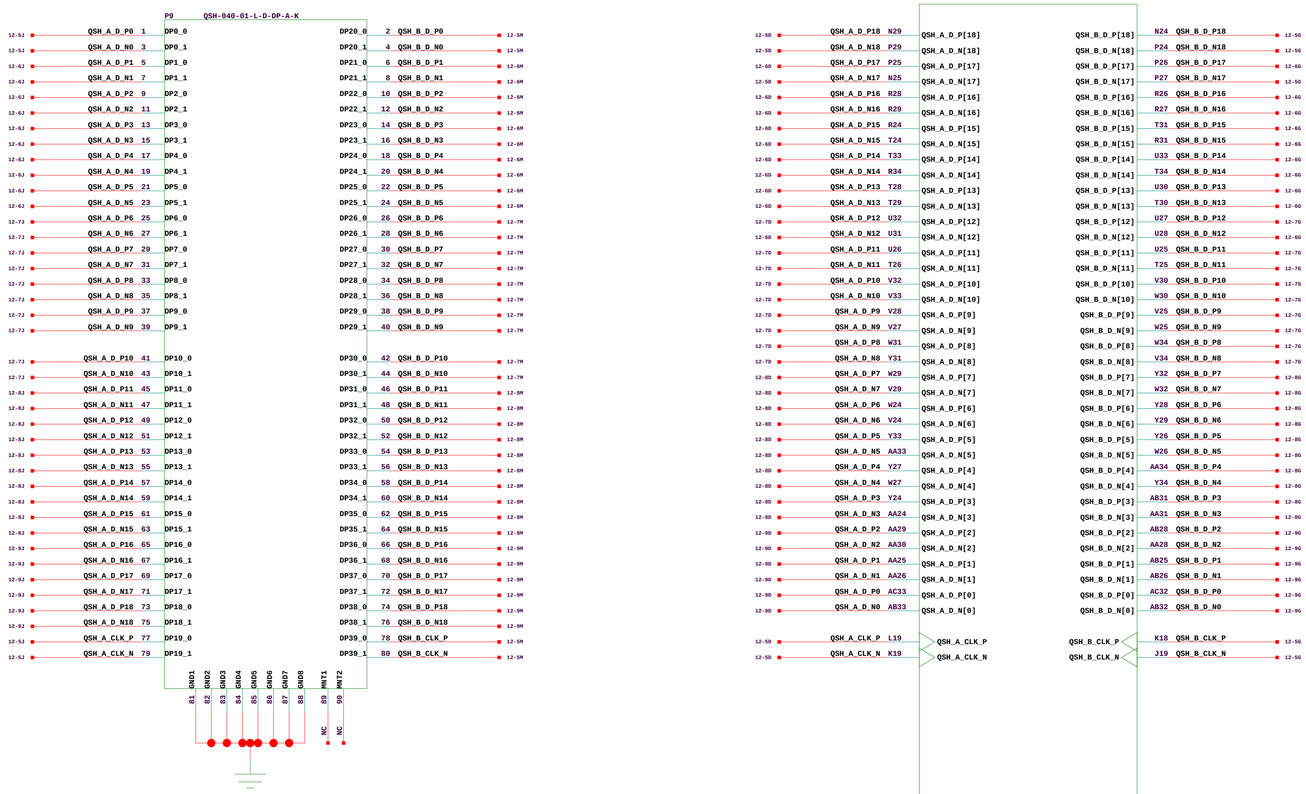






PLACE AT MODULE VDDQ PINS

ROACH/iBOB2	ROACH_DDR2_DIMM
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A; DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE NW
7-7-2008_14:21 PATH PATH	DRAWN: F KAPP; APPR: ; CHECKED: E BAUERMEISTER; SHEET 11 OF 25



ROACH/iBOB2

ROACH_DIFF_GPIO

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

7-7-2008_14:21

PATH PATH

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

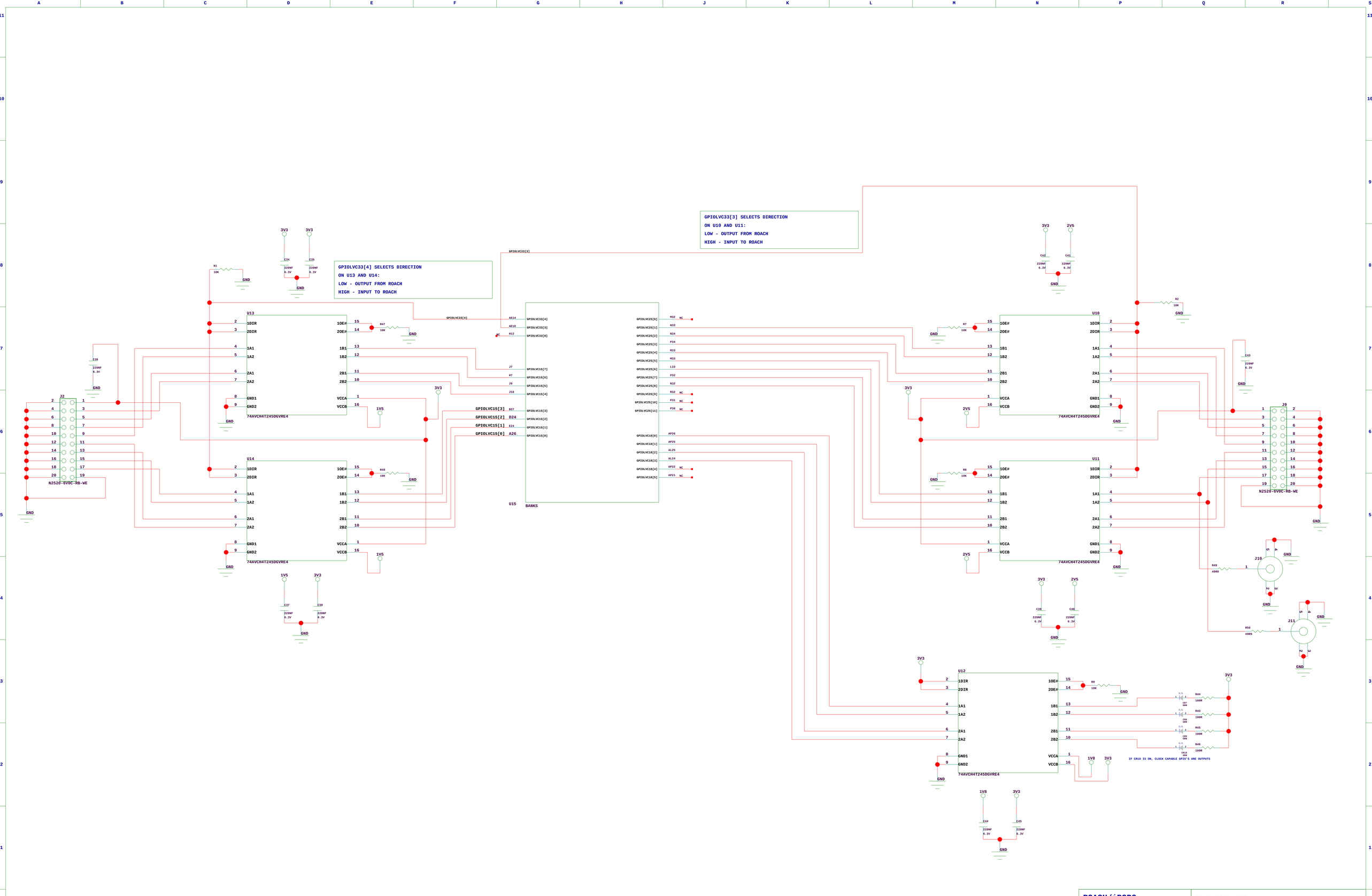
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW

DRAWN: F KAPP

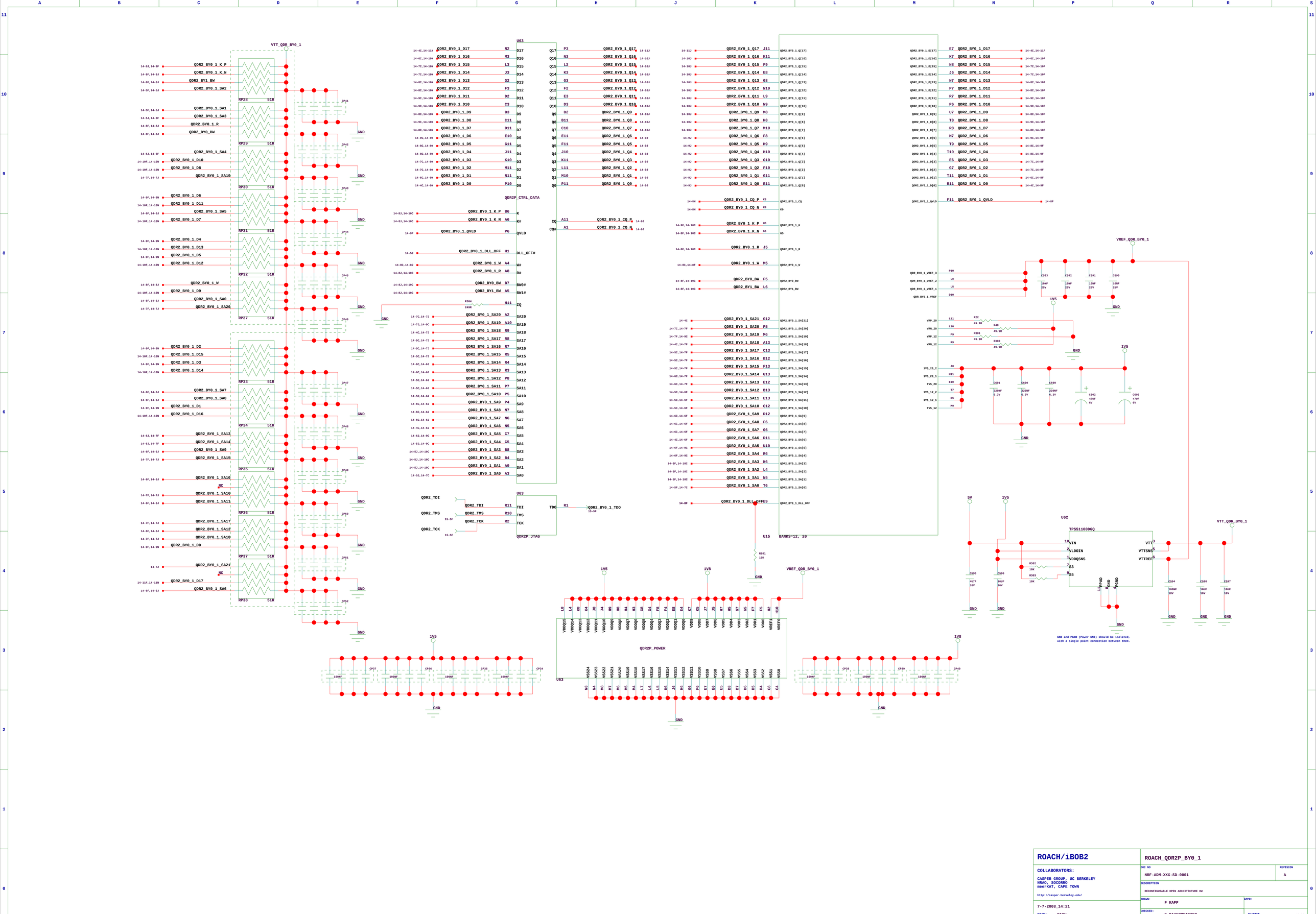
APPR:

CHECKED: E BAUERMEISTER

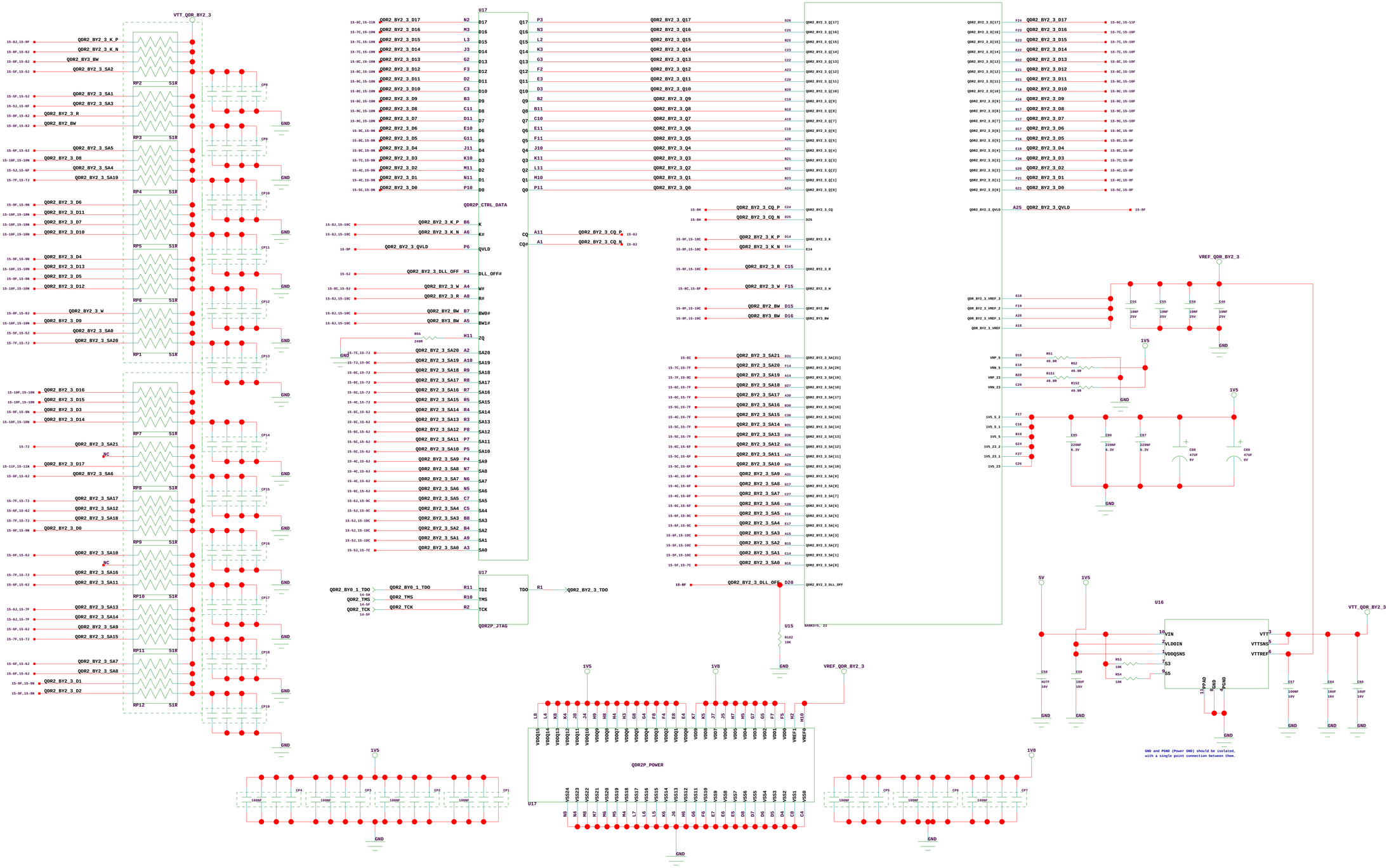
SHEET 12 OF 25



ROACH/iBOB2	**ROACH_GPIO_MISC**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-7-2008_14:21 PATH PATH	DRAWN: F KAPP — APPR:
	CHECKED: E BAUERMEISTER — SHEET 13 OF 25



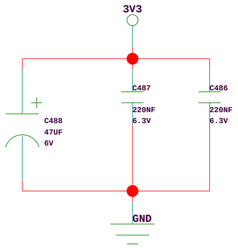
ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-7-2008_14:21	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 14 OF 25

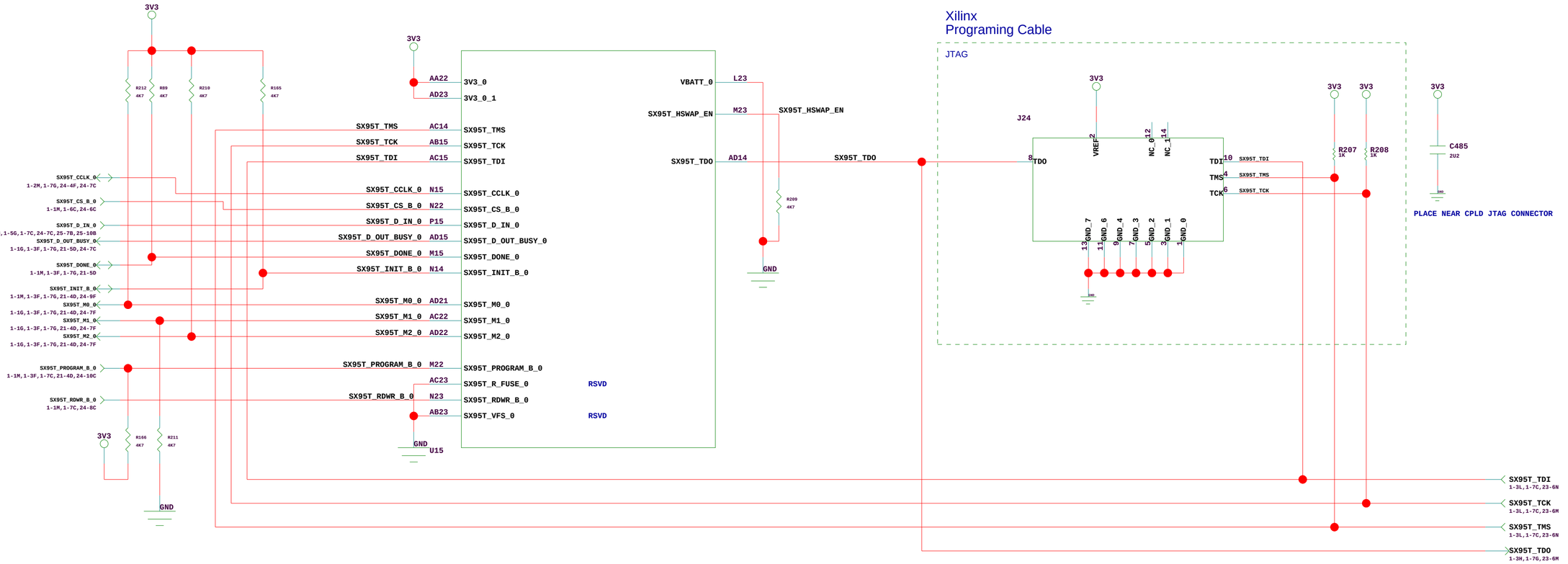


ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-7-2008_14:21	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 15 OF 25

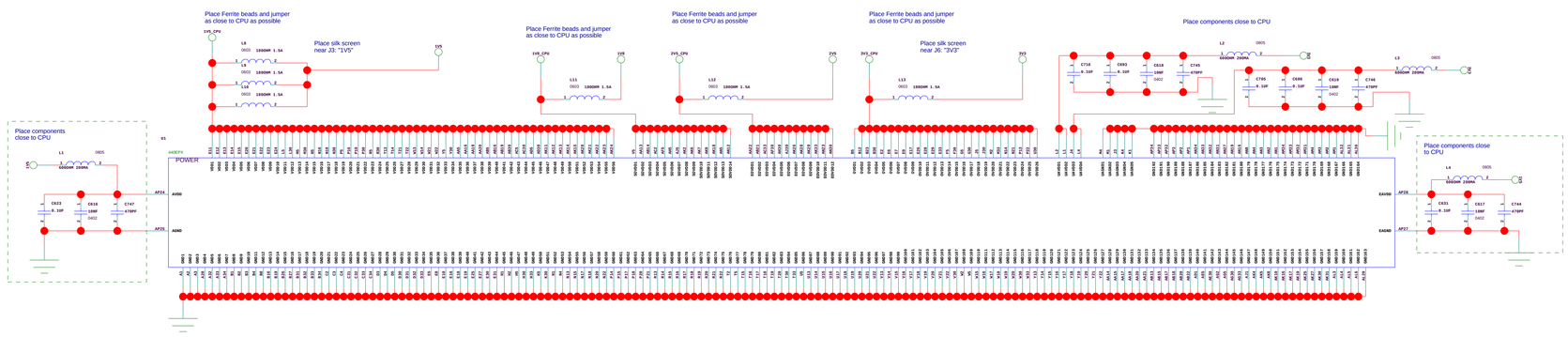
TBD

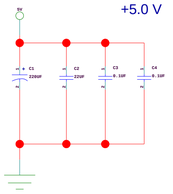
VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

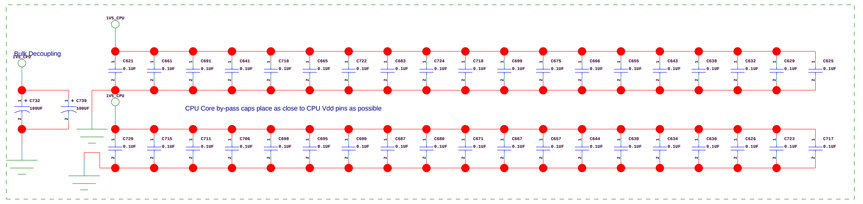


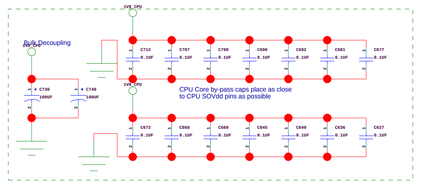


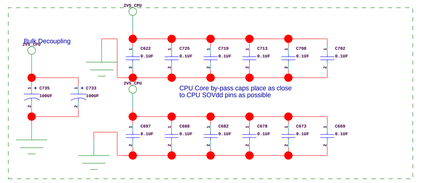
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
7-7-2008_14:21 PATH PATH	

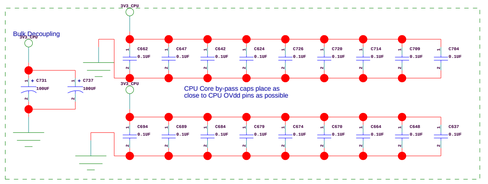


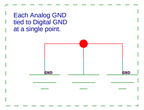










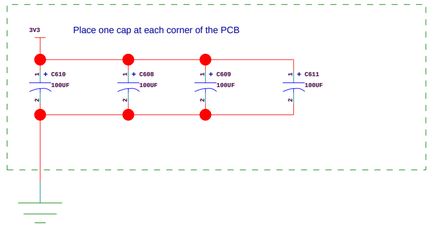


REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: **CASPER GROUP, UC BERKELEY** **NRAO, SOCORRO** **meerKAT, CAPE TOWN** http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 17 OF 25
7-7-2008_14:21 PATH PATH	

REMOVED 3V3 GENERATION



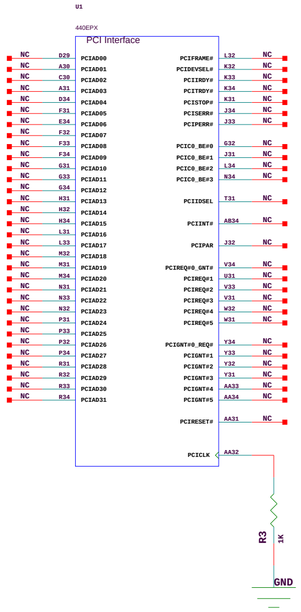
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET: 18 OF 25
7-7-2008_14:21 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-7-2008_14:21 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

Place nearest PHY pin 96

Place nearest PHY pin 101

Place nearest PHY pin 98

Place nearest PHY pin 100

Place as close to PHY CORE VDD power pins as possible

Place as close to PHY IO VDD power pins as possible

UNUSED SECOND ETHERNET MAC

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.
Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place jumers in line with signals

Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5

Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

Bottom LED
Green/Toggle = ACTIVITY

HFJ11-1G02E-L12

ETHERNET Mgt.

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

NOSTUFF

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

JUMPER DEFAULTS

JP10, JP11	2 - 3	PHY ADD0 = 1
JP12, JP13	1 - 2	Adertised Modes 1000BASE-T, 100BASE-TX, 10BASE-T
JP14, JP15	1 - 2	
JP16, JP17	2 - 3	FULL DUPLEX
JP18, JP19	2 - 3	AUTO NEGOTIATION ENABLED
JP20-23	1 - 2	PHY ADD4:1 = 1111

ROACH/iBOB2	ROACH_PPC_ETH1
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 20 OF 25
7-7-2008_14:21	
PATH PATH	

U1
USB 2.0 DEVICE
440EPX

USB2CLK — A5 — NC

SECOND USB INTERFACE NOT IMPLEMENTED

NOTE:
SX95T_D_IN_0 ON SHEET 25, GPIO10

GPIO28/USB2TXVAL	C6	NC	SX95T_D_OUT_BUSY_0	SX95T_D_OUT_BUSY_0 1-1G,1-3F,1-7G,16-4B,24-7C
USB2TXRDY_REFEN	B6			
USB2RXACT_HOLDREQ_RCVINH	D7	NC		
USB2RXVAL_LEAKTEST2	C8	NC		
GPIO27/USB2RXERR_EXTREQ#	A4		SX95T_DONE_0	SX95T_DONE_0 1-1M,1-3F,1-7G
GPIO30/USB2XCVRSEL_EXTACK#	M3		SX95T_INIT_B_0	SX95T_INIT_B_0 1-1M,1-3F,1-7G,24-9F
GPIO31/USB2TERMSEL_BUSREQ	P4			
USB2LS0_DRVINH1	R2	NC	SX95T_M0_0	SX95T_M0_0 1-1G,1-3F,1-7G,16-3B,24-7F
USB2LS1_LEAKTEST_HOLDPRI	P1	NC		
GPIO32/USB2OM0	R3		SX95T_M1_0	SX95T_M1_0 1-1G,1-3F,1-7G,16-3B,24-7F
GPIO33/USB2OM1	R4			
GPIO29/USB2SUSP_HOLDACK	C5		SX95T_M2_0	SX95T_M2_0 1-1G,1-3F,1-7G,16-3B,24-7F
			SX95T_PROGRAM_B_0	SX95T_PROGRAM_B_0 1-1M,1-3F,1-7C,16-3B,24-10C

NOTE:
USB HOST ONLY

USB 2.0 PHY
HOST/DEVICE

USB2XCVR — J2 — USB2_XCVR_D+
USB2XCVR# — J1 — USB2_XCVR_D-
USB2REXT — L3 — R182 3K4 0402 — GND
USB2XTAL — N2
USB2XTAL# — N3

CLK_USB2_48MHZ
1-3B,1-3L,23-4G
CLK_USB2_48MHZ

5V — PTC1 1206L050 500MA — 1 — 2

C614 220UF 10V
C612 100NF 10V
C613 1NF 50V

CRITICAL PLACEMENT
Place SP2 very close to P6

SP2
SOT23
PGB102ST23WR
PGB102ST23WR
SP2

VR4 0603 5.5V 20A

NONE P6
1X4 USBA
5 — 1 VCC — 2 D- — 3 D+ — 4 GND — 6
292303-1

GND

ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: **CASPER GROUP, UC BERKELEY** **NRAO, SOCORRO** **meerKAT, CAPE TOWN** http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25
7-7-2008_14:21 PATH PATH	

Z_ADDR

DDR_PA[15:0]

DDR_PDQ[63:0]

PPC_ECC[7:0]

DDR SDRAM

U1 — 44GEPX

DDR_PDQ0	AB2	MEMDATA00	MEMADDR00
DDR_PDQ1	AF22	MEMDATA01	MEMADDR01
DDR_PDQ2	AK26	MEMDATA02	MEMADDR02
DDR_PDQ3	AL28	MEMDATA03	MEMADDR03
DDR_PDQ4	AJ22	MEMDATA04	MEMADDR04
DDR_PDQ5	AK22	MEMDATA05	MEMADDR05
DDR_PDQ6	AH21	MEMDATA06	MEMADDR06
DDR_PDQ7	AF21	MEMDATA07	MEMADDR07
DDR_PDQ8	AF28	MEMDATA08	MEMADDR08
DDR_PDQ9	AL18	MEMDATA09	MEMADDR09
DDR_PDQ10	AH17	MEMDATA10	MEMADDR10
DDR_PDQ11	AF17	MEMDATA11	MEMADDR11
DDR_PDQ12	AH26	MEMDATA12	MEMADDR12
DDR_PDQ13	AF18	MEMDATA13	MEMADDR13
DDR_PDQ14	AH18	MEMDATA14	
DDR_PDQ15	AF16	MEMDATA15	
DDR_PDQ16	AH16	MEMDATA16	
DDR_PDQ17	AF15	MEMDATA17	
DDR_PDQ18	AF14	MEMDATA18	
DDR_PDQ19	AL17	MEMDATA19	
DDR_PDQ20	AH17	MEMDATA20	
DDR_PDQ21	AH13	MEMDATA21	
DDR_PDQ22	AH15	MEMDATA22	
DDR_PDQ23	AH14	MEMDATA23	
DDR_PDQ24	AF13	MEMDATA24	
DDR_PDQ25	AH13	MEMDATA25	
DDR_PDQ26	AF12	MEMDATA26	
DDR_PDQ27	AL12	MEMDATA27	
DDR_PDQ28	AH14	MEMDATA28	
DDR_PDQ29	AH14	MEMDATA29	
DDR_PDQ30	AL13	MEMDATA30	
DDR_PDQ31	AH12	MEMDATA31	
DDR_PDQ32	AF3	MEMDATA32	
DDR_PDQ33	AF1	MEMDATA33	
DDR_PDQ34	AD4	MEMDATA34	
DDR_PDQ35	AD3	MEMDATA35	
DDR_PDQ36	AB3	MEMDATA36	
DDR_PDQ37	AF2	MEMDATA37	
DDR_PDQ38	AE2	MEMDATA38	
DDR_PDQ39	AE1	MEMDATA39	
DDR_PDQ40	AC3	MEMDATA40	
DDR_PDQ41	AC1	MEMDATA41	
DDR_PDQ42	AA4	MEMDATA42	
DDR_PDQ43	AA3	MEMDATA43	
DDR_PDQ44	AD2	MEMDATA44	
DDR_PDQ45	AC4	MEMDATA45	
DDR_PDQ46	AB1	MEMDATA46	
DDR_PDQ47	AB2	MEMDATA47	
DDR_PDQ48	Y3	MEMDATA48	
DDR_PDQ49	Y2	MEMDATA49	
DDR_PDQ50	Y4	MEMDATA50	
DDR_PDQ51	Y1	MEMDATA51	
DDR_PDQ52	AA2	MEMDATA52	
DDR_PDQ53	AA1	MEMDATA53	
DDR_PDQ54	W3	MEMDATA54	
DDR_PDQ55	W1	MEMDATA55	
DDR_PDQ56	V1	MEMDATA56	
DDR_PDQ57	U2	MEMDATA57	
DDR_PDQ58	W2	MEMDATA58	
DDR_PDQ59	Y4	MEMDATA59	
DDR_PDQ60	R1	MEMDATA60	
DDR_PDQ61	V3	MEMDATA61	
DDR_PDQ62	T2	MEMDATA62	
DDR_PDQ63	T3	MEMDATA63	

		MEMADDR00	AM5
		MEMADDR01	AP4
		MEMADDR02	AM6
		MEMADDR03	AM6
		MEMADDR04	AP6
		MEMADDR05	AN6
		MEMADDR06	AL7
		MEMADDR07	AN7
		MEMADDR08	AP7
		MEMADDR09	AL2
		MEMADDR10	AL8
		MEMADDR11	MEMADDR11
		MEMADDR12	AN8
		MEMADDR13	AG4
DDR_PBA0	AJ3	BA0	
DDR_PBA1	AK3	BA1	
DDR_PBA2	AF6	BA2	
DDR_PRAS#	AJ4	RAS#	
DDR_PCAS#	AN4	CAS#	
DDR_PWE#	AJ2	WE#	
DDR_PDM0	AL21	DM0	
DDR_PDM1	AP18	DM1	
DDR_PDM2	AP15	DM2	
DDR_PDM3	AL14	DM3	
DDR_PDM4	AD4	DM4	
DDR_PDM5	AB3	DM5	
DDR_PDM6	Y3	DM6	
DDR_PDM7	V3	DM7	
DDR_PDM8	AN18	DM8	
DDR_PDQS0	AM21	DQS0	
DDR_PDQS1	AM19	DQS1	
DDR_PDQS2	AL15	DQS2	
DDR_PDQS3	AM13	DQS3	
DDR_PDQS4	AE3	DQS4	
DDR_PDQS5	AB4	DQS5	
DDR_PDQS6	W4	DQS6	
DDR_PDQS7	T4	DQS7	
DDR_PDQS8	AP10	DQS8	
DDR_PODT0	AN3	MEMODT0	
DDR_PODT1	AG1	MEMODT1	
DDR_PCS0#	AN2	BANKSELA0	
DDR_PCS1#	AM1	BANKSELA1	
DDR_PCKE	AN9	MEMCLKEN	
DDR_PCLKOUT	AL1	MEMCLKOUT	
DDR_PCLKOUT#	AK1	MEMCLKOUT#	
PPC_ECC0	AM11	ECC0	
PPC_ECC1	AL11	ECC1	
PPC_ECC2	AN9	ECC2	
PPC_ECC3	AL9	ECC3	
PPC_ECC4	AM11	ECC4	
PPC_ECC5	AN11	ECC5	
PPC_ECC6	AM10	ECC6	
PPC_ECC7	AF9	ECC7	

		SVREF1A	AL10
		SVREF2A	AF4
		SVREF1B	AL19
		SVREF2B	AL19

22-7L,22-8K
22-8L,22-8L
22-8K,22-10L
22-7K,22-7L
22-7L,22-8K
22-3K,22-7L
22-5K
22-6K
22-6K
22-6K
22-6K
22-6K
22-6K
22-4K
22-4K
22-4K
22-4K
22-5K
22-5K
22-5K
22-7L
22-6L
22-3K,22-7L
22-3K,22-7L
22-6K,22-11L
22-2A
22-2A

J8

DDR_PDQ63	153	DDR2_DIMM_CB7	PPC_ECC7	168
DDR_PDQ62	152	DDR2_DIMM_CB6	PPC_ECC6	167
DDR_PDQ61	40	DDR2_DIMM_CB5	PPC_ECC5	162
DDR_PDQ60	39	DDR2_DIMM_CB4	PPC_ECC4	161
DDR_PDQ59	34	DDR2_DIMM_CB3	PPC_ECC3	49
DDR_PDQ58	33	DDR2_DIMM_CB2	PPC_ECC2	48
DDR_PDQ57	150	DDR2_DIMM_CB1	PPC_ECC1	43
DDR_PDQ56	149	DDR2_DIMM_CB0	PPC_ECC0	42
DDR_PDQ55	144			
DDR_PDQ54	143	DDR2_DIMM_DQ[63]	DDR_PDQ63	236
DDR_PDQ53	31	DDR2_DIMM_DQ[62]	DDR_PDQ62	235
DDR_PDQ52	30	DDR2_DIMM_DQ[61]	DDR_PDQ61	230
DDR_PDQ51	25	DDR2_DIMM_DQ[60]	DDR_PDQ60	229
DDR_PDQ50	24	DDR2_DIMM_DQ[59]	DDR_PDQ59	117
DDR_PDQ49	141	DDR2_DIMM_DQ[58]	DDR_PDQ58	116
DDR_PDQ48	140	DDR2_DIMM_DQ[57]	DDR_PDQ57	111
DDR_PDQ47	132	DDR2_DIMM_DQ[56]	DDR_PDQ56	110
DDR_PDQ46	131	DDR2_DIMM_DQ[55]	DDR_PDQ55	227
DDR_PDQ45	22	DDR2_DIMM_DQ[54]	DDR_PDQ54	226
DDR_PDQ44	21	DDR2_DIMM_DQ[53]	DDR_PDQ53	218
DDR_PDQ43	13	DDR2_DIMM_DQ[52]	DDR_PDQ52	217
DDR_PDQ42	12	DDR2_DIMM_DQ[51]	DDR_PDQ51	108
DDR_PDQ41	129	DDR2_DIMM_DQ[50]	DDR_PDQ50	107
DDR_PDQ40	128	DDR2_DIMM_DQ[49]	DDR_PDQ49	99
DDR_PDQ39	123	DDR2_DIMM_DQ[48]	DDR_PDQ48	98
DDR_PDQ38	122	DDR2_DIMM_DQ[47]	DDR_PDQ47	215
DDR_PDQ37	10	DDR2_DIMM_DQ[46]	DDR_PDQ46	214
DDR_PDQ36	9	DDR2_DIMM_DQ[45]	DDR_PDQ45	209
DDR_PDQ35	4	DDR2_DIMM_DQ[44]	DDR_PDQ44	208
DDR_PDQ34	3	DDR2_DIMM_DQ[43]	DDR_PDQ43	96
		DDR2_DIMM_DQ[42]	DDR_PDQ42	95
		DDR2_DIMM_DQ[41]	DDR_PDQ41	90
		DDR2_DIMM_DQ[40]	DDR_PDQ40	89
		DDR2_DIMM_DQ[39]	DDR_PDQ39	206
		DDR2_DIMM_DQ[38]	DDR_PDQ38	205
		DDR2_DIMM_DQ[37]	DDR_PDQ37	200
		DDR2_DIMM_DQ[36]	DDR_PDQ36	199
		DDR2_DIMM_DQ[35]	DDR_PDQ35	87
		DDR2_DIMM_DQ[34]	DDR_PDQ34	86
		DDR2_DIMM_DQ[33]	DDR_PDQ33	81
		DDR2_DIMM_DQ[32]	DDR_PDQ32	80
		DDR2_DIMM_DQ[31]	DDR_PDQ31	159
		DDR2_DIMM_DQ[30]	DDR_PDQ30	158
		DDR2_DIMM_DQ[29]	DDR_PDQ29	153
		DDR2_DIMM_DQ[28]	DDR_PDQ28	152
		DDR2_DIMM_DQ[27]	DDR_PDQ27	40
		DDR2_DIMM_DQ[26]	DDR_PDQ26	39
		DDR2_DIMM_DQ[25]	DDR_PDQ25	34
		DDR2_DIMM_DQ[24]	DDR_PDQ24	33
		DDR2_DIMM_DQ[23]	DDR_PDQ23	150
		DDR2_DIMM_DQ[22]	DDR_PDQ22	149
		DDR2_DIMM_DQ[21]	DDR_PDQ21	144
		DDR2_DIMM_DQ[20]	DDR_PDQ20	143
		DDR2_DIMM_DQ[19]	DDR_PDQ19	31
		DDR2_DIMM_DQ[18]	DDR_PDQ18	30
		DDR2_DIMM_DQ[17]	DDR_PDQ17	25
		DDR2_DIMM_DQ[16]	DDR_PDQ16	24
		DDR2_DIMM_DQ[15]	DDR_PDQ15	141
		DDR2_DIMM_DQ[14]	DDR_PDQ14	140
		DDR2_DIMM_DQ[13]	DDR_PDQ13	132
		DDR2_DIMM_DQ[12]	DDR_PDQ12	131
		DDR2_DIMM_DQ[11]	DDR_PDQ11	22
		DDR2_DIMM_DQ[10]	DDR_PDQ10	21
		DDR2_DIMM_DQ[9]	DDR_PDQ9	13
		DDR2_DIMM_DQ[8]	DDR_PDQ8	12
		DDR2_DIMM_DQ[7]	DDR_PDQ7	129
		DDR2_DIMM_DQ[6]	DDR_PDQ6	128
		DDR2_DIMM_DQ[5]	DDR_PDQ5	123
		DDR2_DIMM_DQ[4]	DDR_PDQ4	122
		DDR2_DIMM_DQ[3]	DDR_PDQ3	10
		DDR2_DIMM_DQ[2]	DDR_PDQ2	9
		DDR2_DIMM_DQ[1]	DDR_PDQ1	4
		DDR2_DIMM_DQ[0]	DDR_PDQ0	3
		DDR2_DIMM_SA2		101
		DDR2_DIMM_SA1		240
		DDR2_DIMM_SA0		239
		DDR2_DIMM_SCL	I2C0_SCLK	120
		DDR2_DIMM_SDA	I2C0_SDATA	119

879160001

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA2	22-9D,22-10L
DDR2_DIMM_BA[1]	190	DDR_PBA1	22-8L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-7L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	DDR_PCLKOUT2	
DDR2_DIMM_CK_N[2]	221	DDR_PCLKOUT2#	
DDR2_DIMM_CK_P[1]	137	DDR_PCLKOUT1	
DDR2_DIMM_CK_N[1]	138	DDR_PCLKOUT1#	
DDR2_DIMM_CK_P[0]	185	DDR_PCLKOUT0	
DDR2_DIMM_CK_N[0]	186	DDR_PCLKOUT0#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-8D,22-11L
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-8D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	1-2B,1-2M,24-10F
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D
PAR_OUT	55	PPC_DDR2_ERROR	1
PAR_IN	68	PAR_IN	1

TP4
TP5

C313 5PF 50V
C308 5PF 50V
C655 5PF 50V

R226 4K7
R227 4K7

PPC_DDR2_RESET_N

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

DDR_VTT

22-8K,22-8D	DDR_PCKE	RP24	CP26
	DDR_PA15		
	DDR_PA14		
22-8K,22-8D	DDR_PBA2		
	DDR_PA12	RP23	CP28
	DDR_PA11		
	DDR_PA9		
	NC		
	DDR_PA7	RP22	CP29
	DDR_PA8		
	DDR_PA6		
	DDR_PA5		
	DDR_PA4	RP21	CP30
	DDR_PA3		
	DDR_PA1		
	DDR_PA2		
22-8K,22-8D	DDR_PA0	RP25	CP32
	DDR_PBA1		
	DDR_PA10		
22-8K,22-8D	DDR_PBA0		
22-7K,22-8D	DDR_PRAS#	RP26	CP31
22-3K,22-8D	DDR_PWE#		
22-3K,22-8D	DDR_PCS0#		
22-8K,22-8D	DDR_PCAS#		
22-3K,22-8D	DDR_PCS1#	RP19	CP33
22-8D	DDR_PODT0		
	DDR_PA13		
22-8D	DDR_PODT1		

GND

J8

VSS_64	237	187	VDD_9
VSS_63	234	184	VDD_8
VSS_62	231	178	VDD_7
VSS_61	228	172	VDD_6
VSS_60	225	69	VDD_5
VSS_59	222	67	VDD_4
VSS_58	219	64	VDD_3
VSS_57	216	59	VDD_2
VSS_56	213	53	VDD_1
VSS_55	210		
VSS_54	207	194	VDDQ_11
VSS_53	204	191	VDDQ_10
VSS_52	201	181	VDDQ_9
VSS_51	198	175	VDDQ_8
VSS_50	169	170	VDDQ_7
VSS_49	166	78	VDDQ_6
VSS_48	163	75	VDDQ_5
VSS_47	160	72	VDDQ_4
VSS_46	157	62	VDDQ_3
VSS_45	154	56	VDDQ_2
VSS_44	151	51	VDDQ_1
VSS_43	148		
VSS_42	145		
VSS_41	142		
VSS_40	139		
VSS_39	136		
VSS_38	133		
VSS_37	130		
VSS_36	127		
VSS_35	124		
VSS_34	121		
VSS_33	118		
VSS_32	115		
VSS_31	112		
VSS_30	109		
VSS_29	106		
VSS_28	103		
VSS_27	100		
VSS_26	97		
VSS_25	94		
VSS_24	91		
VSS_23	88		
VSS_22	85		
VSS_21	82		
VSS_20	79		
VSS_19	66		
VSS_18	65		
VSS_17	50		
VSS_16	47		
VSS_15	44		
VSS_14	41		
VSS_13	38		
VSS_12	35		
VSS_11	32		
VSS_10	29		
VSS_9	26		
VSS_8	23		
VSS_7	20		
VSS_6	17		
VSS_5	14		
VSS_4	11		
VSS_3	8		
VSS_2	5		
VSS_1	2		

879160001

GND

DDR_VREF_0V9
VREF 1
3V3
VDDSPD 238
1V8

PowerPC DRAM Interface:

- DDR2 240 pin DIMM
- 72 bit ECC
- Unbuffered and Registered DIMMs supported
- Up to 2GB supported
- CAS Latencies: 2, 2.5 or 3
- Clock Frequencies: 133MHz to 166MHz
- Single Ended Strobes

Z_IN

DDR_PCLKOUT#
DDR_PCLKOUT
R168 120R
CLK
CLK#

Z_OUT

DDR_PCLKOUT1
DDR_PCLKOUT1#
DDR_PCLKOUT0
DDR_PCLKOUT0#
DDR_PCLKOUT2
DDR_PCLKOUT2#

Z_FB

R169 120R
FBIN
FBIN#
FBOUT
FBOUT#
U6 CDCU877ARHAT
GND1
GND2
FBOUT#
FBOUT

U32 TPS51100DGQ

VIN
VLDOIN
VDDQSNS
S3
S5
VTT
VTTSNS
VTTREF
PPAD
GND
PGND

R230 10K
R229 10K
R6 120R
C459 4U7F 10V
C456 10UF 10V
C453 100NF 10V
C21 22PF
C457 10UF 10V
C458 10UF 10V

L17

1000HM 1.5A

C329 4U7F 10V
C300 100NF 10V
C63 10NF 25V
R167 10K
AVDD
AGND
OE
OS

Place parts as close to CPU as possible

C150 0.10F
C149 0.10F
C151 0.10F 0402
C152 0.10F 0402
C148 10NF 0402

DDR_VREF_0V9 / 1V8 / 5V / GND

C432 C433 C454 C434 C439 C443 C431 C444 C436 C445 C435 C446 — 100NF 10V / 10NF 25V

C438 C451 C437 C452 C439 C449 C440 C450 C441 C448 C442 C447 — 100NF 10V / 10NF 25V

PLACE NEAREST DDR2 MODULE PINS

PPC DDR2 LAYOUT NOTES

- ROUTE ALL DDR CLOCKS AS LENGTH MATCHED ONLY - DIFFERENTIAL ROUTING NOT REQUIRED
- CLOCK DELAYS MUST ADHERE TO THE FOLLOWING:
  Z_IN + Z_OUT - Z_FB = Z_ADDR + 500 ps (+-25 ps)
  WHERE:
  Z_IN = PROPAGATION DELAY ON DDR_PCLKOUT/DDR_PCLKOUT#
  Z_OUT = PROPAGATION DELAY ON DDR_PCLKOUTn/DDR_PCLKOUTn#
  Z_FB = PROPAGATION DELAY ON FBOUT/FBOUT#
  Z_ADDR = PROPAGATION DELAY ON DDR_PADD[13:0]
- DDR_PCLKOUTn/DDR_PCLKOUTn# NETS CAN BE SWAPPED ON CLOCK BUFFER TO EASE ROUTING
- ALL DQ, DQS, DM, ADDR, CMD AND CTRL LINES LENGTH MATCHED TO 400 ps
  MATCHING WITHIN BYTE LANE: 50 ps
  209 ps < TRACE LENGTH < 800 ps
- U6 THERMAL TAB TO BE CONNECTED TO GND PLANE WITH THERMAL VIAS

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

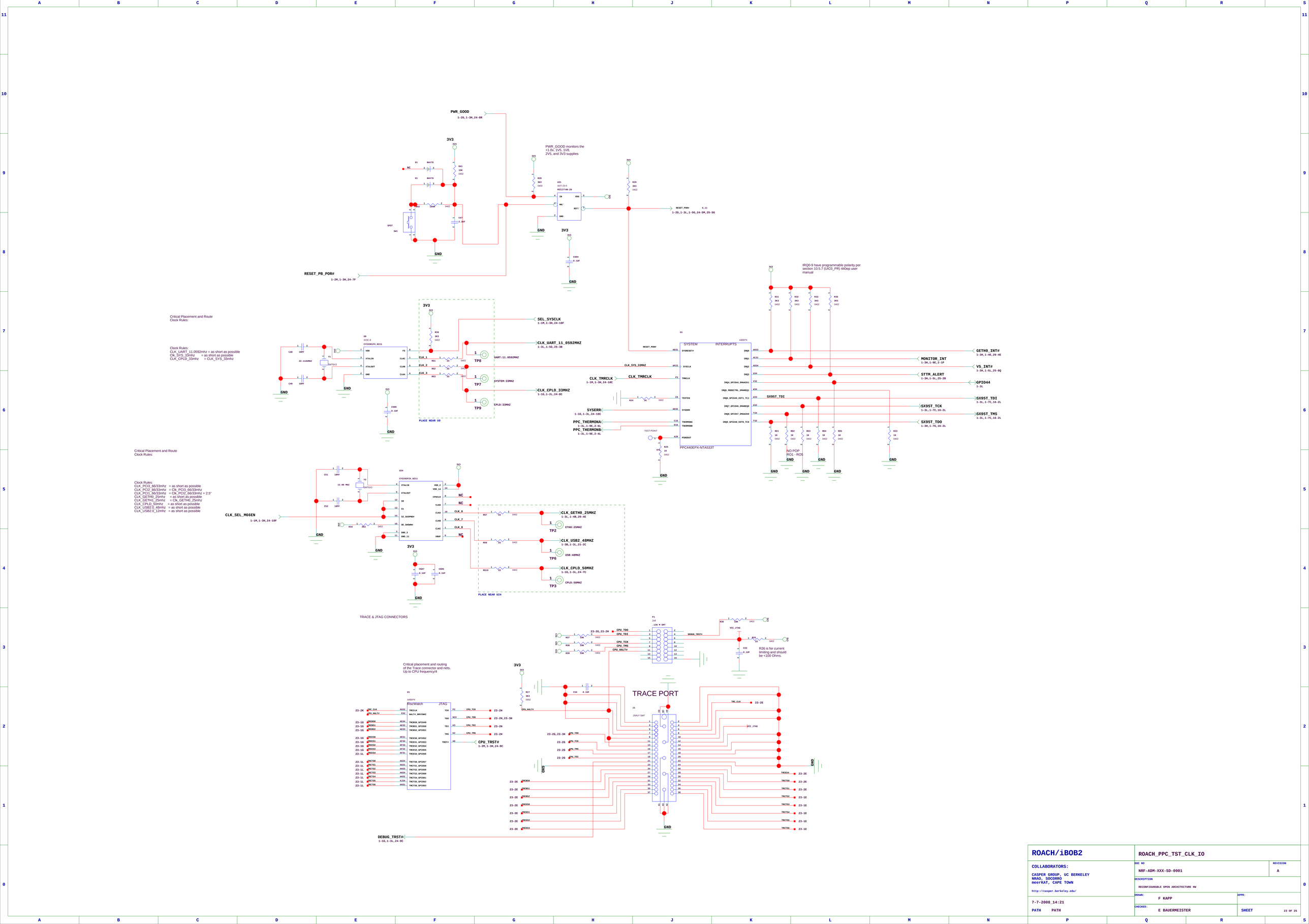
http://casper.berkeley.edu/

7-7-2008_14:21

PATH PATH

ROACH_PPC_DDR2

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE MW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	22 OF 25



ROACH/iBOB2	**ROACH_PPC_TST_CLK_IO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-7-2008_14:21	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 23 OF 25

roach_cpld_XC2C256_7VQ100C_pcb

CLK_TMCLK	4	PAD4	PAD217 142 NC
SYSRR	7	PAD8	PAD214 140 NC
EXT_RESETf	9	PAD10	PAD213 139 GETH0_RST#
SX95T_PROGRAM_B_0	10	PAD12	PAD212 138 PPC_DDR2_RESET_N
SX95T_DONE_0	11	PAD15	PAD211 137 CLK_SEL_MGGEN
PCS_2	12	PAD16	PAD208 136 SEL_SYSCLK
PB_WI	13	PAD17	PAD207 135 NC
DEBUG_TRSTf	14	PAD18	PAD206 134 NC
CPU_TRSTn	15	PAD19	PAD204 133 NC
FWBE_0#	16	PAD20	PAD199 132 NC
PADO[27:31]	17	PAD21	PAD197 131 SX95T_INIT_B_0
	18	PAD23	PAD196 130 NC
	19	PAD28	PAD195 129
	20	PAD29	PAD194 128
	21	PAD30	PAD192 126
PDATA[0:7]	22	PAD31	PAD191 125 NC
	23	PAD32	PAD190 124 NC
	24	PAD33	PAD187 121
	25	PAD34	PAD186 120 DAT1
	26	PAD35	PAD178 119 DAT0_DO
	28	PAD44	PAD177 118 DAT7
CLK_CPLD_33MHZ	30	PAD48	PAD176 117 DAT6
	31	PAD49	PAD175 116 CLK_SCLK
CLK_PERCLK	32	PAD50	PAD173 115 DAT5
	33	PAD52	PAD171 114 DAT4
PDE#	34	PAD54	PAD169 113 CMD_DI
SX95T_RDWR_B_0	35	PAD55	PAD168 112 DAT3
CLK_CPLD_50MHZ	38	PAD59	PAD167 111 DAT2
SX95T_D_IN_0	40	PAD64	PAD166 110
SX95T_D_OUT_BUSY_0	41	PAD65	PAD163 107
PER_CCLK_ENf	42	PAD66	PAD162 106 SX95T_M0_0
SX95T_CCLK_0	43	PAD67	PAD161 105 SX95T_M1_0
FRY_BY#	44	PAD68	PAD160 104 SX95T_M2_0
FWPC	45	PAD69	PAD158 103 NC
EE1_WP#	46	PAD70	PAD156 102 RESET_PB_POR#
EE2_BOOT_WP	48	PAD73	PAD154 101 USER_LED1
STTM_ASC	49	PAD74	PAD152 100 SYSERR#
SELECTMAP_CS	50	PAD75	PAD146 98 RESET_BUFPOR0#
	51 NC	PAD76	PAD145 97
SX95T_CS_B_0	52	PAD77	PAD144 96 USER_DIP0
	53 NC	PAD81	PAD143 95 USER_DIP1
PPC_RESET	54	PAD82	PAD142 94 USER_DIP2
SYS_CONFIG0	56	PAD86	PAD138 92 USER_DIP3
SYS_CONFIG1	57	PAD87	PAD137 91
SYS_CONFIG2	58	PAD88	PAD134 88
SYS_CONFIG3	59	PAD89	PAD133 87
SYS_CONFIG4	60	PAD90	PAD132 86 NC
SYS_CONFIG5	61	PAD95	PAD131 85 NC
SYS_CONFIG6	64	PAD100	PAD125 83 NC
SYS_CONFIG7	66	PAD102	PAD121 82 NC
	68 NC	PAD105	PAD120 81 NC
	69 NC	PAD107	PAD119 80 NC
	70 NC	PAD108	PAD118 79 NC
RESET_CPLD#	71	PAD109	PAD117 78 NC
	74 NC	PAD112	PAD115 77 NC
	75 NC	PAD113	PAD114 76 NC

SYS_CONFIG[0:7] 1-2G,1-9E,2-2R — SYS_CONFIG[0:7]

RESET_CPLD# 1-1M,1-4G,25-3J

U54 XC2C256_7VQ144C

RESETS

CPU_TRSTn = '1' when JTAG_TRSTn = '1' and RESET_PORn = '1' else '0'; see errata sheet

SD/MMC/MMCPLUS CONNECTOR

J17 SDSR13-A0-0005

10	CMD/DI	DAT0/DO	2
6	CLK/SCLK	DAT1	1
		DAT2	13
7	VDD	DAT3	12
8	VSS1	DAT4	11
4	VSS2	DAT5	9
		DAT6	5
14	SD_CD_COM	DAT7	3
15	SD_WP_COM		
		MNT1	16
		MNT2	17

SX95T_INIT_B_0 1-1M,1-3F,1-7G,21-4D

GETH0_RST# 1-2M,1-4B,20-4E

PPC_DDR2_RESET_N 1-1B,1-2M,22-5K

CLK_SEL_MGGEN 1-1M,1-3H,23-5D

SEL_SYSCLK 1-1M,1-3H,23-7G

BOOT_CFG0 1-1M,1-4G,25-1J

BOOT_CFG1 1-1M,1-4G,25-1J

BOOT_CFG2 1-1M,1-4G,25-1J

SX95T_M0_0 1-1G,1-3F,1-7G,16-3D,21-4D

SX95T_M1_0 1-1G,1-3F,1-7G,16-3D,21-4D

SX95T_M2_0 1-1G,1-3F,1-7G,16-3D,21-4D

RESET_PB_POR# 1-2M,1-3G,23-8E

USER_LED0

USER_LED1 R201 330R D402 — LED0 CR3

SYSERR# R202 330R D402 — LED1 CR4

RESET_BUFPOR0# R203 330R D402 — LED2 CR5

SysErr will be used to drive Status LED (active H)

R198 10K D402 — SW2

R194 10K D402 — USER_DIP0

R195 10K D402 — USER_DIP1

R196 10K D402 — USER_DIP2

4POLE User DIP-Switch

Boot Configuration

R204 10K D402 — CFG_DIP0

R205 10K D402 — CFG_DIP1

R206 10K D402 — CFG_DIP2

MGGEN

SW3 4POLE Configuration DIP-Switch

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

ENABLE PER_CLK CONNECTION TO CONFIGURATION I/F MUST CO-ORDINATE WITH SX95T_CCLK_0 AND MODE TO AVOID CLASH

R135 10K — PER_CCLK_ENf

R305 330R — CLK_PERCLK 1-1G,1-4L,24-8B,25-6F

R306 240R

SN74AHC1G125DCKT U2 — DE# VCC A Y GND — C13 100NF 10V

SX95T_CCLK_0 — SX95T_CCLK_0 1-2M,1-7G,24-7C

PLACE AT END OF DAISY CHAIN

U54 XC2C256_7VQ144C

roach_cpld_XC2C256_7VQ100C_powerpins

VCC 1 · VAUX 8 · VCCIO_3 27 · VCC_1 37 · VCCIO_4 55 · VCCIO_5 73 · VCC_2 84 · VCCIO_6 93 · VCCIO 109 · VCCIO_1 127 · VCCIO_2 141

GND_3 29 · GND_4 36 · GND_5 47 · GND_6 62 · GND_7 72 · GND_8 89 · GND_9 90 · GND_10 99 · GND 108 · GND_1 123 · GND_2 144

C473 C474 C475 C476 C477 C478 C479 C480 C481 C482 C483 100NF 10V

PLACE NEAR CPLD POWER PINS

U54

NC	2	PAD1	
NC	3	PAD3	
NC	5	PAD5	
NC	6	PAD7	
NC	39	PAD62	
	63	TDI	
	65	TMS	
	67	TCK	
	122	TDO	
	143	PAD218	

roach_cpld_XC2C256_7VQ100C_configpins

XC2C256_7VQ144C

RESET_PORn 1-2G,1-3L,1-5G,23-9J,25-5G

Xilinx
Programing Cable

JTAG

J22 — TDO 1 · VREF 2 · NC_0 12 · NC_1 14 · TDI 10 CPLD_TDI · TMS 8 CPLD_TMS · TCK 6 CPLD_TCK · GND_7 11 · GND_6 9 · GND_4 7 · GND_3 5 · GND_2 3 · GND_1 1 · GND_0 13

R193 1K · R192 1K

C484 22Z

PLACE NEAR CPLD JTAG CONNECTOR

R197 330R D402 — CR1 GRN

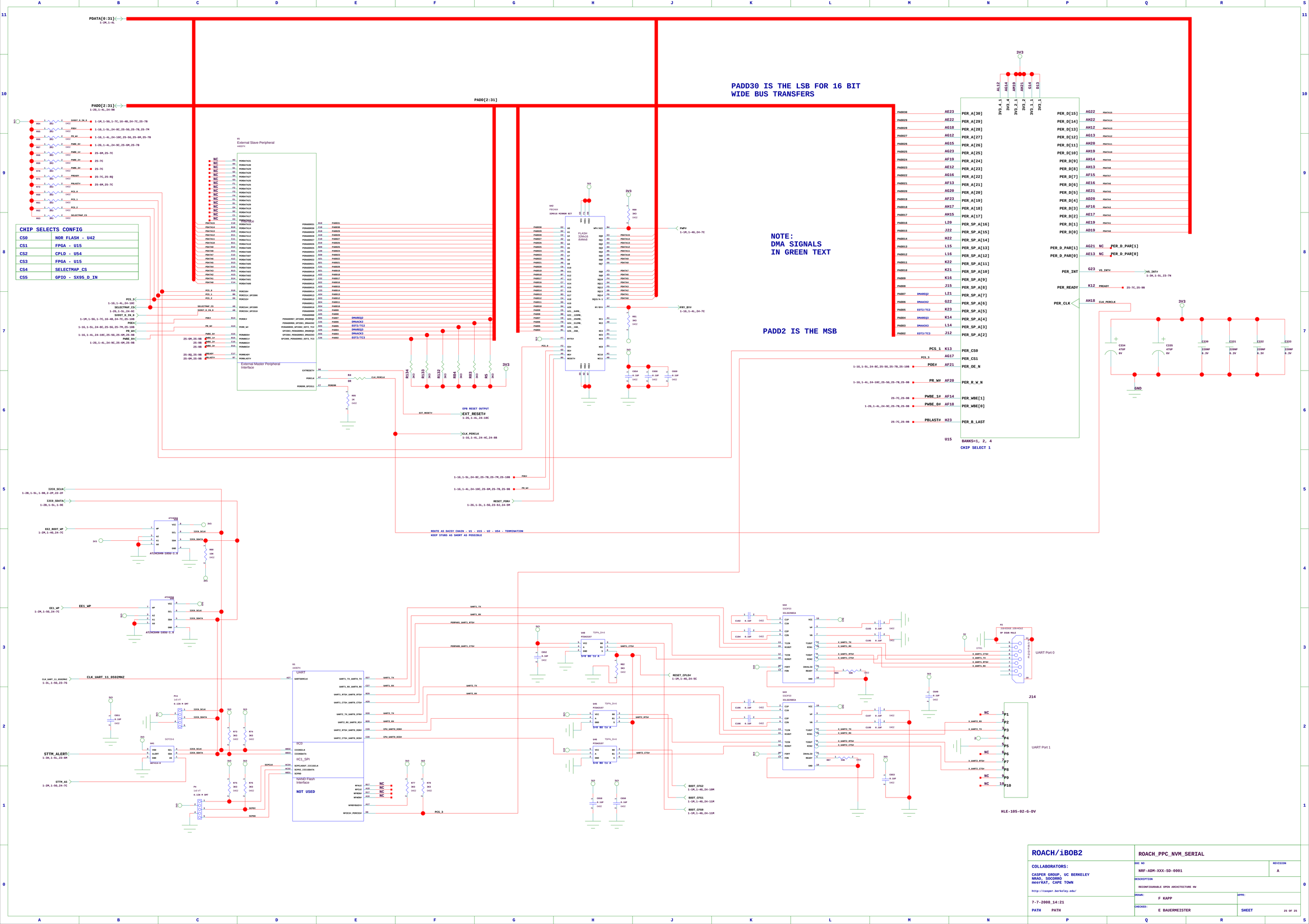
R199 330R D402 — CR2 GRN

U35 SC70-5 74LVC1G08 — VCC 5 · A 4 · B 2 · GND 3 — Y 1

C615 0.1UF

PWR_GOOD 1-2G,1-3H,23-10G

ROACH/iBOB2	ROACH_PPC_CPLD
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
http://casper.berkeley.edu/	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-7-2008_14:21 PATH PATH	DRAWN: F KAPP · APPR: · CHECKED: E BAUERMEISTER · SHEET 24 OF 25



ROACH/iBOB2	ROACH_PPC_NVM_SERIAL
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-7-2008_14:21	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 25 OF 25