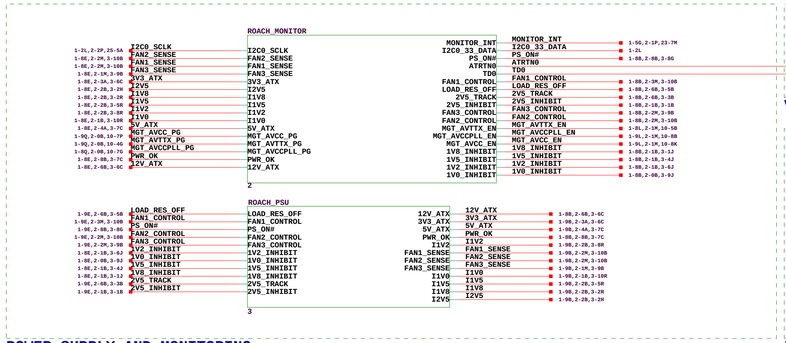
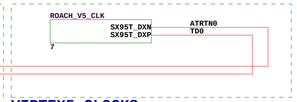
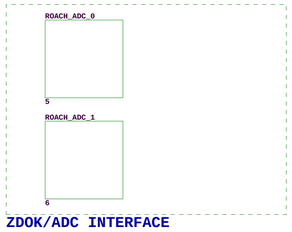
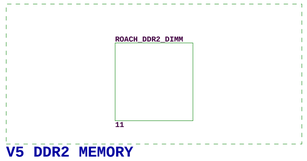
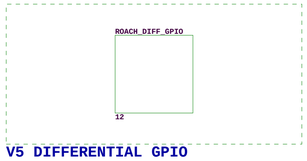
VIRTEX5

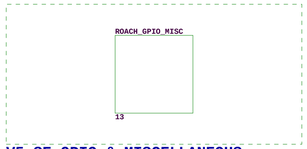


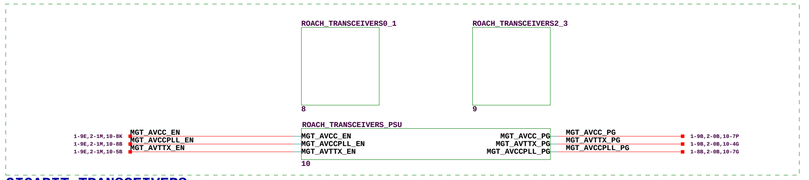


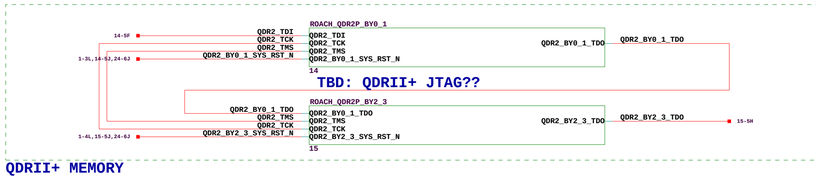


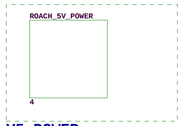




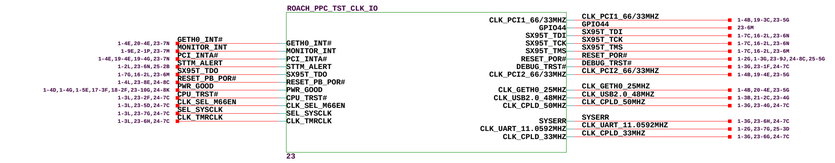




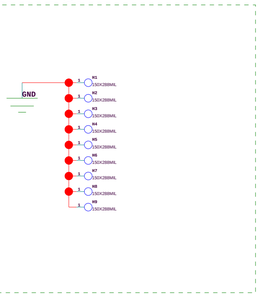




PPC



MECHANICAL



CONTRIBUTORS

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MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

10-5-2007_16:36

PATH PATH

ROACH_TOP

DOC NO: NRF-ADM-XXX-SD-0001
REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 1 OF 25

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

TIE TO GROUND IF PLL'S ARE NOT USED

PLACE AT ACTEL 1V5 POWER PINS

PLACE AT ACTEL 3V3 POWER PINS

roach_AFS600_powerpins

roach_AFS600_pcb

XPORT - PLACE IN REAR I/O REGION

TEMPERATURE DIODE HEADER

PUSH BUTTON POWER SWITCH

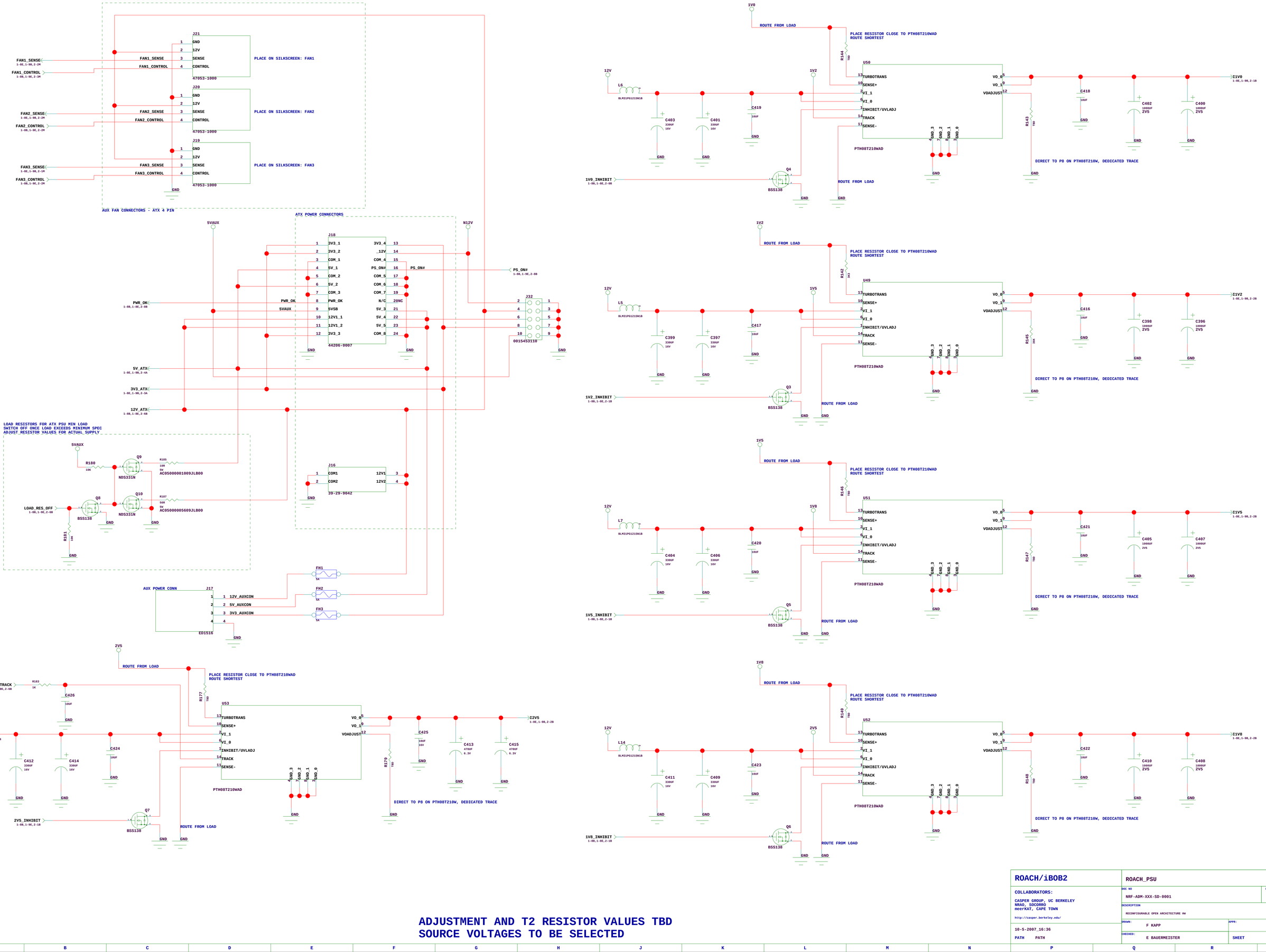
roach_AFS600_configpins

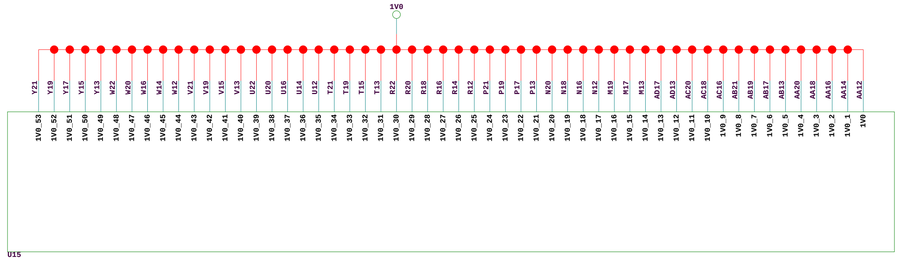
ACTEL JTAG CONNECTOR

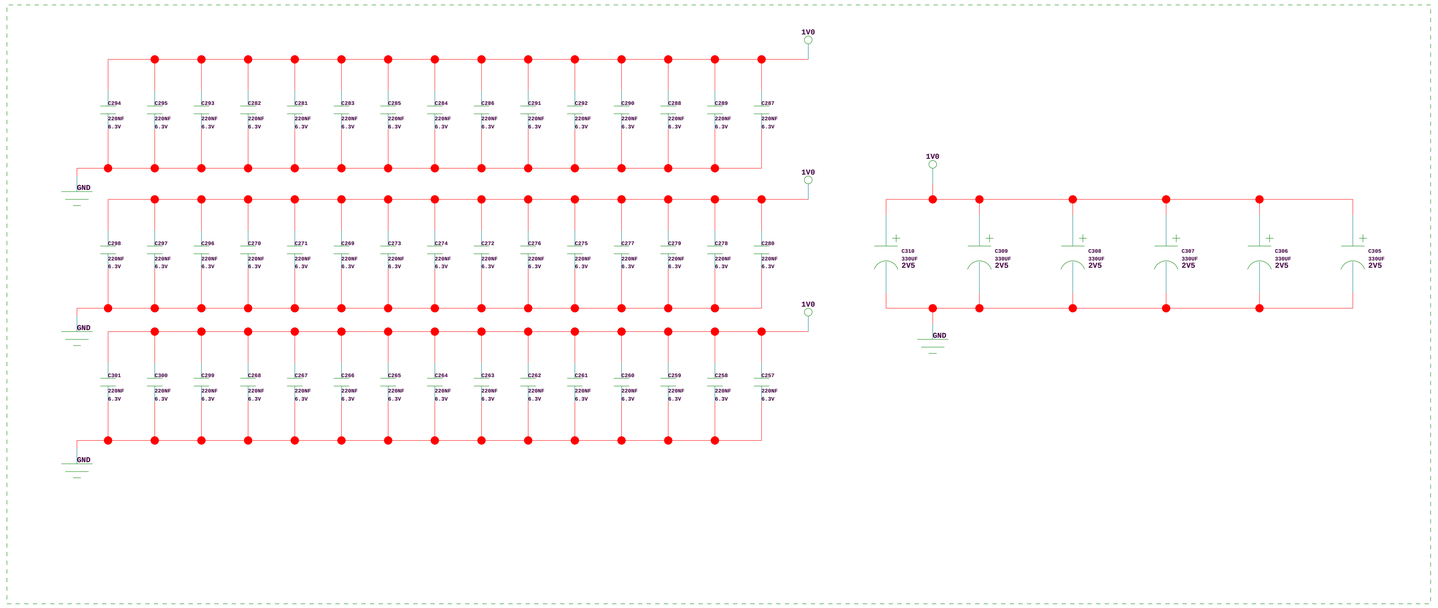
SPARE ANALOG VOLTAGE INPUT #0
SPARE ANALOG VOLTAGE INPUT #1
SPARE GATE DRIVE OUTPUT #0
SPARE GATE DRIVE OUTPUT #1

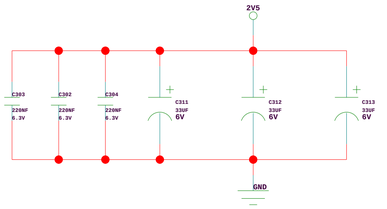
MONITOR RESET

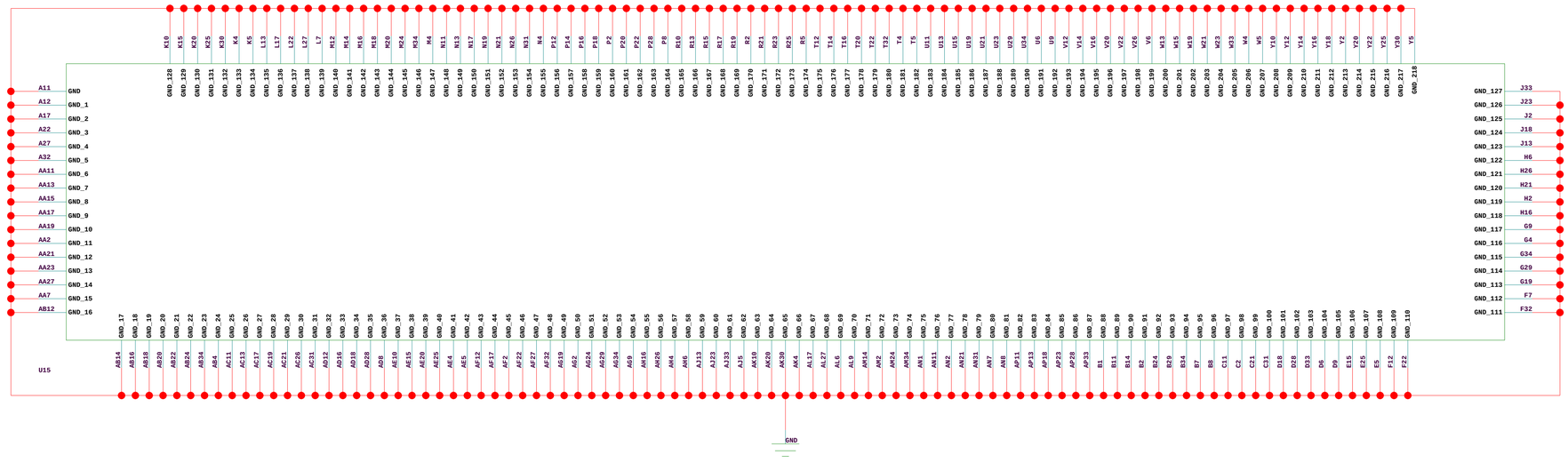
ROACH/iBOB2	ROACH_MONITOR
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_16:36	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 2 OF 25


AUX FAN CONNECTORS - ATX 4 PIN
J21
J20
J19
FAN1_SENSE
FAN1_CONTROL
FAN2_SENSE
FAN2_CONTROL
FAN3_SENSE
FAN3_CONTROL
PLACE ON SILKSCREEN: FAN1
PLACE ON SILKSCREEN: FAN2
PLACE ON SILKSCREEN: FAN3
47053-1000
ATX POWER CONNECTORS
J18
44206-0007
J32
0015453110
PS_ON#
PWR_OK
5V_ATX
3V3_ATX
12V_ATX
LOAD RESISTORS FOR ATX PSU MIN LOAD
SWITCH OFF ONCE LOAD EXCEEDS MINIMUM SPEC
ADJUST RESISTOR VALUES FOR ACTUAL SUPPLY
Q9
Q8
Q10
NDS331N
BSS138
AC05000001009JLB00
AC05000005609JLB00
LOAD_RES_OFF
J16
39-29-9042
AUX POWER CONN
J17
ED1516
12V_AUXCON
5V_AUXCON
3V3_AUXCON
FH1
FH2
FH3
1V0
ROUTE FROM LOAD
PLACE RESISTOR CLOSE TO PTH08T210WAD
ROUTE SHORTEST
R144
U50
PTH08T210WAD
L6
BLM31PG121SN1B
C403
C401
C419
C418
C402
C400
I1V0
1V0_INHIBIT
Q4
DIRECT TO P8 ON PTH08T210W, DEDICATED TRACE
1V2
R142
U49
L5
C399
C397
C417
C416
C398
C396
I1V2
1V2_INHIBIT
Q3
1V5
R146
U51
L7
C404
C406
C420
C421
C405
C407
I1V5
1V5_INHIBIT
Q5
2V5
R177
U53
2V5_TRACK
2V5_INHIBIT
Q7
R179
1V8
R149
U52
L14
C411
C409
C423
C422
C410
C408
I1V8
1V8_INHIBIT
Q6
ADJUSTMENT AND T2 RESISTOR VALUES TBD
SOURCE VOLTAGES TO BE SELECTED
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
10-5-2007_16:36
PATH
ROACH_PSU
DOC NO
NRF-ADM-XXX-SD-0001
REVISION
A
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE RW
DRAWN:
F KAPP
APPR:
CHECKED:
E BAUERMEISTER
SHEET
3 OF 25









ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
10-5-2007_16:36 PATH PATH	


ZDOK0_CLK0_P K18
ZDOK0_CLK0_N J19
ZDOK0_CLK1_P J16
ZDOK0_CLK1_N J17
2V5
R133 100R
R132 100R
VRP_20 L11
VRN_20 L10
R134 100R
R135 100R
VRP_12_GPIOLVC25 P9
VRN_12_GPIOLVC25 R9
M9 2V5_12
N6 2V5_12_1
T7 2V5_12_2
E10 2V5_20
H11 2V5_20_1
J8 2V5_20_2
C328 47UF 6V
C327 47UF 6V
C326 47UF 6V
C329 47UF 6V
C325 220NF 6.3V
C322 220NF 6.3V
C323 220NF 6.3V
C324 220NF 6.3V
U15
BANKS=20, 12
ZDOK0_DP_P[37] E6 ZDOK0_DP_P[37]
ZDOK0_DP_N[37] E7 ZDOK0_DP_N[37]
ZDOK0_DP_P[36] T9 ZDOK0_DP_P[36]
ZDOK0_DP_N[36] U10 ZDOK0_DP_N[36]
ZDOK0_DP_P[35] G6 ZDOK0_DP_P[35]
ZDOK0_DP_N[35] G7 ZDOK0_DP_N[35]
ZDOK0_DP_P[34] T10 ZDOK0_DP_P[34]
ZDOK0_DP_N[34] T11 ZDOK0_DP_N[34]
ZDOK0_DP_P[33] F5 ZDOK0_DP_P[33]
ZDOK0_DP_N[33] F6 ZDOK0_DP_N[33]
ZDOK0_DP_P[32] R11 ZDOK0_DP_P[32]
ZDOK0_DP_N[32] P10 ZDOK0_DP_N[32]
ZDOK0_DP_P[31] H5 ZDOK0_DP_P[31]
ZDOK0_DP_N[31] G5 ZDOK0_DP_N[31]
ZDOK0_DP_P[30] H7 ZDOK0_DP_P[30]
ZDOK0_DP_N[30] J7 ZDOK0_DP_N[30]
ZDOK0_DP_P[29] T8 ZDOK0_DP_P[29]
ZDOK0_DP_N[29] U7 ZDOK0_DP_N[29]
ZDOK0_DP_P[28] R7 ZDOK0_DP_P[28]
ZDOK0_DP_N[28] R8 ZDOK0_DP_N[28]
ZDOK0_DP_P[27] J6 ZDOK0_DP_P[27]
ZDOK0_DP_N[27] J5 ZDOK0_DP_N[27]
ZDOK0_DP_P[26] R6 ZDOK0_DP_P[26]
ZDOK0_DP_N[26] T6 ZDOK0_DP_N[26]
ZDOK0_DP_P[25] K7 ZDOK0_DP_P[25]
ZDOK0_DP_N[25] K6 ZDOK0_DP_N[25]
ZDOK0_DP_P[24] P7 ZDOK0_DP_P[24]
ZDOK0_DP_N[24] P6 ZDOK0_DP_N[24]
ZDOK0_DP_P[23] L4 ZDOK0_DP_P[23]
ZDOK0_DP_N[23] L5 ZDOK0_DP_N[23]
ZDOK0_DP_P[22] N5 ZDOK0_DP_P[22]
ZDOK0_DP_N[22] P5 ZDOK0_DP_N[22]
ZDOK0_DP_P[21] M7 ZDOK0_DP_P[21]
ZDOK0_DP_N[21] L6 ZDOK0_DP_N[21]
ZDOK0_DP_P[20] N8 ZDOK0_DP_P[20]
ZDOK0_DP_N[20] N7 ZDOK0_DP_N[20]
ZDOK0_DP_P[19] M6 ZDOK0_DP_P[19]
ZDOK0_DP_N[19] M5 ZDOK0_DP_N[19]
ZDOK0_DP_P[18] F13 ZDOK0_DP_P[18]
ZDOK0_DP_N[18] G13 ZDOK0_DP_N[18]
ZDOK0_DP_P[17] N10 ZDOK0_DP_P[17]
ZDOK0_DP_N[17] N9 ZDOK0_DP_N[17]
ZDOK0_DP_P[16] E12 ZDOK0_DP_P[16]
ZDOK0_DP_N[16] E13 ZDOK0_DP_N[16]
ZDOK0_DP_P[15] M10 ZDOK0_DP_P[15]
ZDOK0_DP_N[15] L9 ZDOK0_DP_N[15]
ZDOK0_DP_P[14] F11 ZDOK0_DP_P[14]
ZDOK0_DP_N[14] E11 ZDOK0_DP_N[14]
ZDOK0_DP_P[13] M8 ZDOK0_DP_P[13]
ZDOK0_DP_N[13] L8 ZDOK0_DP_N[13]
ZDOK0_DP_P[12] G11 ZDOK0_DP_P[12]
ZDOK0_DP_N[12] G12 ZDOK0_DP_N[12]
ZDOK0_DP_P[11] B13 ZDOK0_DP_P[11]
ZDOK0_DP_N[11] C13 ZDOK0_DP_N[11]
ZDOK0_DP_P[10] K8 ZDOK0_DP_P[10]
ZDOK0_DP_N[10] K9 ZDOK0_DP_N[10]
ZDOK0_DP_P[9] J10 ZDOK0_DP_P[9]
ZDOK0_DP_N[9] J9 ZDOK0_DP_N[9]
ZDOK0_DP_P[8] A13 ZDOK0_DP_P[8]
ZDOK0_DP_N[8] B12 ZDOK0_DP_N[8]
ZDOK0_DP_P[7] H10 ZDOK0_DP_P[7]
ZDOK0_DP_N[7] H9 ZDOK0_DP_N[7]
ZDOK0_DP_P[6] D12 ZDOK0_DP_P[6]
ZDOK0_DP_N[6] C12 ZDOK0_DP_N[6]
ZDOK0_DP_P[5] K11 ZDOK0_DP_P[5]
ZDOK0_DP_N[5] J11 ZDOK0_DP_N[5]
ZDOK0_DP_P[4] D11 ZDOK0_DP_P[4]
ZDOK0_DP_N[4] D10 ZDOK0_DP_N[4]
ZDOK0_DP_P[3] G8 ZDOK0_DP_P[3]
ZDOK0_DP_N[3] H8 ZDOK0_DP_N[3]
ZDOK0_DP_P[2] F10 ZDOK0_DP_P[2]
ZDOK0_DP_N[2] G10 ZDOK0_DP_N[2]
ZDOK0_DP_P[1] F9 ZDOK0_DP_P[1]
ZDOK0_DP_N[1] F8 ZDOK0_DP_N[1]
ZDOK0_DP_P[0] E9 ZDOK0_DP_P[0]
ZDOK0_DP_N[0] E8 ZDOK0_DP_N[0]
5V0
3V3
2V5
1V8
C315 1UF 16V
C314 100NF 10V
C317 1UF 16V
C316 100NF 10V
C318 1UF 16V
C319 100NF 10V
C321 1UF 16V
C320 100NF 10V
P5
6367550-5
ZDOK40
ZDOK0_DP_P[0] A1
ZDOK0_DP_N[0] A2
ZDOK0_DP_P[1] A3
ZDOK0_DP_N[1] A4
ZDOK0_DP_P[2] A5
ZDOK0_DP_N[2] A6
ZDOK0_DP_P[3] A7
ZDOK0_DP_N[3] A8
ZDOK0_DP_P[4] A9
ZDOK0_DP_N[4] A10
ZDOK0_DP_P[5] A11
ZDOK0_DP_N[5] A12
ZDOK0_DP_P[6] A13
ZDOK0_DP_N[6] A14
ZDOK0_DP_P[7] A15
ZDOK0_DP_N[7] A16
ZDOK0_DP_P[8] A17
ZDOK0_DP_N[8] A18
ZDOK0_DP_P[9] A19
ZDOK0_DP_N[9] A20
ZDOK0_DP_P[10] D1
ZDOK0_DP_N[10] D2
ZDOK0_DP_P[11] D3
ZDOK0_DP_N[11] D4
ZDOK0_DP_P[12] D5
ZDOK0_DP_N[12] D6
ZDOK0_DP_P[13] D7
ZDOK0_DP_N[13] D8
ZDOK0_DP_P[14] D9
ZDOK0_DP_N[14] D10
ZDOK0_DP_P[15] D11
ZDOK0_DP_N[15] D12
ZDOK0_DP_P[16] D13
ZDOK0_DP_N[16] D14
ZDOK0_DP_P[17] D15
ZDOK0_DP_N[17] D16
ZDOK0_DP_P[18] D17
ZDOK0_DP_N[18] D18
ZDOK0_DP_P[19] D19
ZDOK0_DP_N[19] D20
C1 ZDOK0_DP_P[20]
C2 ZDOK0_DP_N[20]
C3 ZDOK0_DP_P[21]
C4 ZDOK0_DP_N[21]
C5 ZDOK0_DP_P[22]
C6 ZDOK0_DP_N[22]
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C8 ZDOK0_DP_N[23]
C9 ZDOK0_DP_P[24]
C10 ZDOK0_DP_N[24]
C11 ZDOK0_DP_P[25]
C12 ZDOK0_DP_N[25]
C13 ZDOK0_DP_P[26]
C14 ZDOK0_DP_N[26]
C15 ZDOK0_DP_P[27]
C16 ZDOK0_DP_N[27]
C17 ZDOK0_DP_P[28]
C18 ZDOK0_DP_N[28]
C19 ZDOK0_CLK0_P 5-7B
C20 ZDOK0_CLK0_N 5-7B
F1 ZDOK0_DP_P[29]
F2 ZDOK0_DP_N[29]
F3 ZDOK0_DP_P[30]
F4 ZDOK0_DP_N[30]
F5 ZDOK0_DP_P[31]
F6 ZDOK0_DP_N[31]
F7 ZDOK0_DP_P[32]
F8 ZDOK0_DP_N[32]
F9 ZDOK0_DP_P[33]
F10 ZDOK0_DP_N[33]
F11 ZDOK0_DP_P[34]
F12 ZDOK0_DP_N[34]
F13 ZDOK0_DP_P[35]
F14 ZDOK0_DP_N[35]
F15 ZDOK0_DP_P[36]
F16 ZDOK0_DP_N[36]
F17 ZDOK0_DP_P[37]
F18 ZDOK0_DP_N[37]
F19 ZDOK0_CLK1_P 5-7B
F20 ZDOK0_CLK1_N 5-7B
6367550-5
ZDOK40
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
10-5-2007_16:36
PATH PATH
ROACH_ADC_0
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 5 OF 25

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

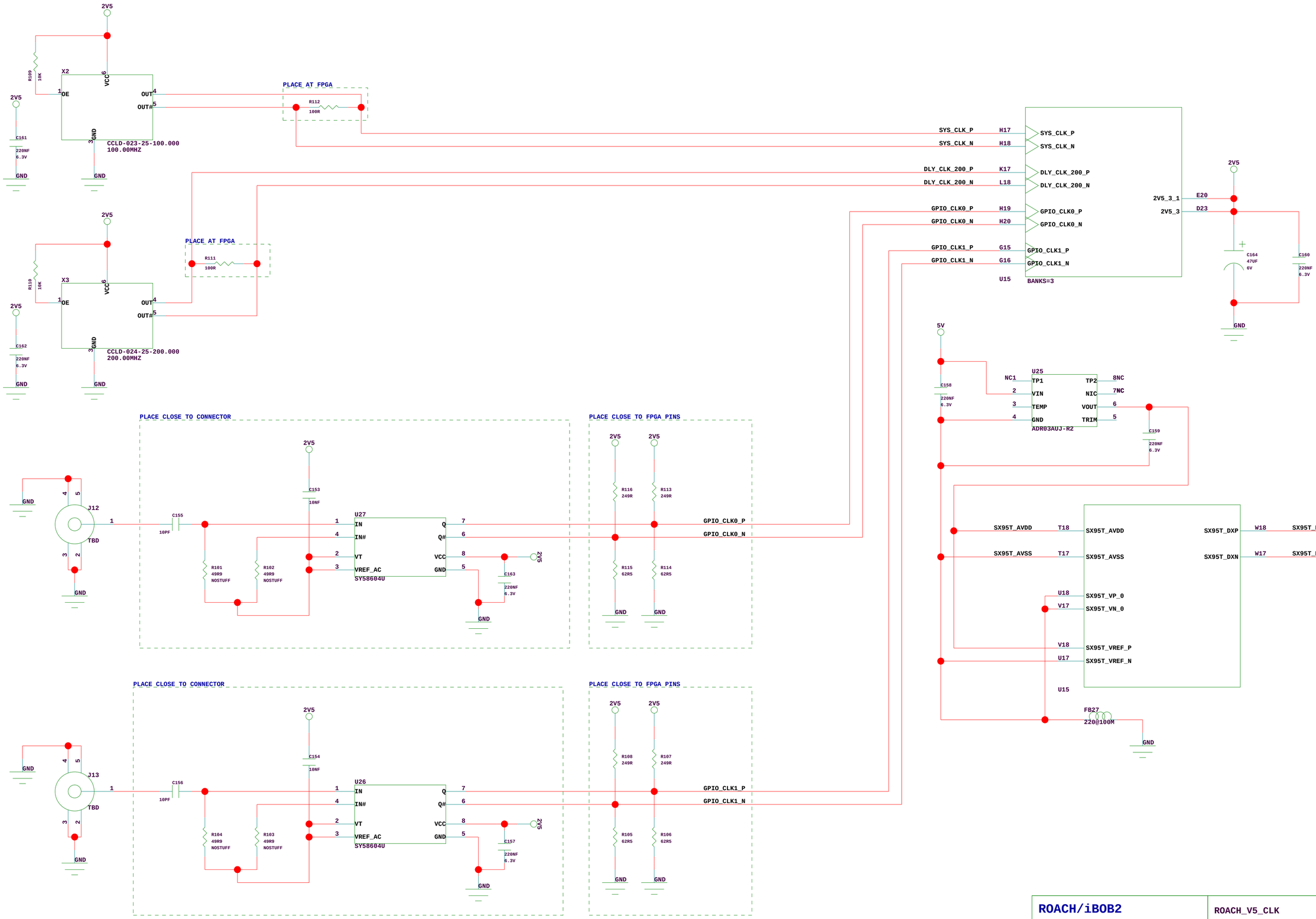
http://casper.berkeley.edu/

10-5-2007_16:36

PATH PATH

ROACH_ADC_1

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	6 OF 25

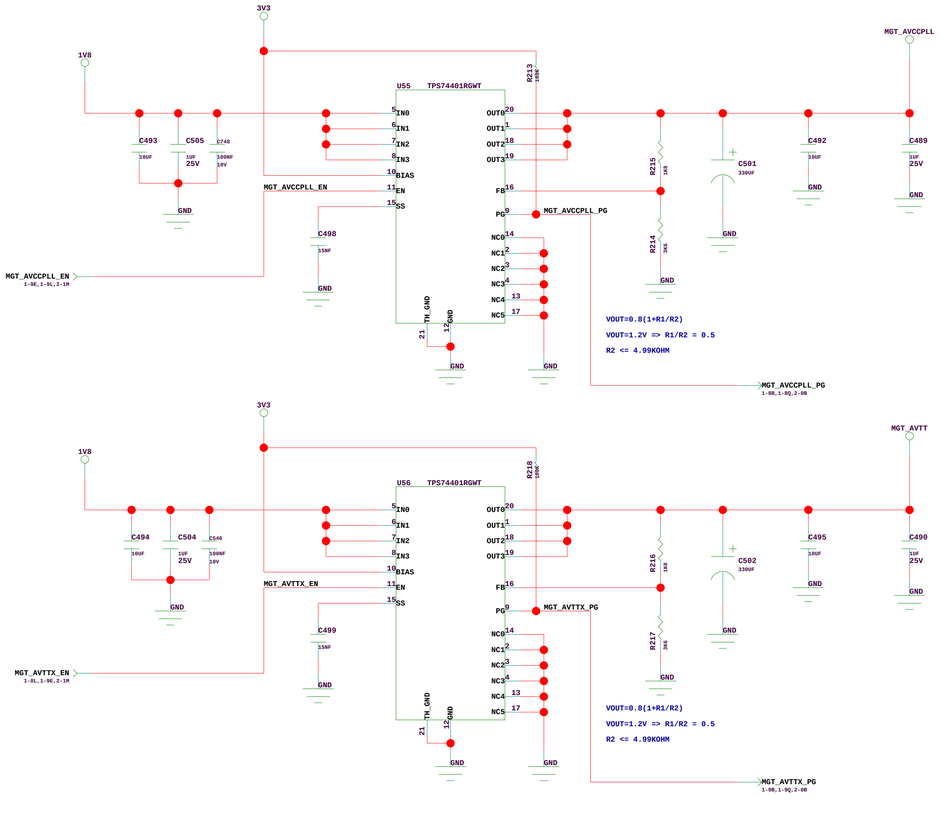


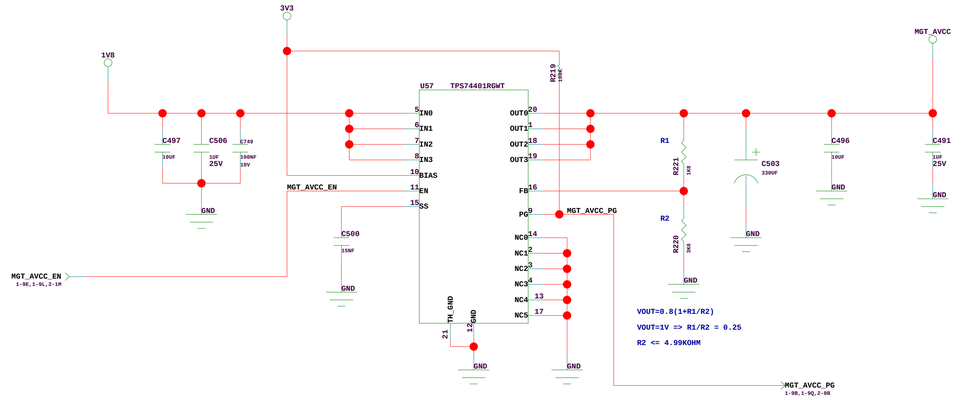
ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
10-5-2007_16:36 PATH PATH	

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB2 220@100M
FB3 220@100M
FB4 220@100M
C95 220NF 6.3V
C94 220NF 6.3V
C93 220NF 6.3V
C92 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_112 R3 MGTAVCC_112
MGTAVCC_112_1 R4 MGTAVCC_112_1
MGTAVCCPLL_112 T3 MGTAVCCPLL_112
MGTAVTTRX_112 N3 MGTAVTTRX_112
MGT_112_REF_CLK_P P4 MGT_112_REF_CLK_P
MGT_112_REF_CLK_N P3 MGT_112_REF_CLK_N
MGTRX0_112_P N1 MGTRX0_112_P
MGTRX0_112_N P1 MGTRX0_112_N
MGTRX1_112_P T1 MGTRX1_112_P
MGTRX1_112_N R1 MGTRX1_112_N
U15
MGTRREF V4 MGTRREF
MGT_VTRXC V5 MGTAVTTRXC
MGTAVTTTX_112 M3 MGTAVTTTX_112
MGTAVTTTX_112_1 U3 MGTAVTTTX_112_1
MGTTX0_112_P M2 MGTTX0_112_P
MGTTX0_112_N N2 MGTTX0_112_N
MGTTX1_112_P U2 MGTTX1_112_P
MGTTX1_112_N T2 MGTTX1_112_N
R56 49.9R
MGT_AVTT
FB25 220@100M
FB5 220@100M
FB6 220@100M
C126 220NF 6.3V
C97 220NF 6.3V
C96 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
2V5
FB26 220@100M
C137 220NF 6.3V
R84 10K
X1
CCLD-023-25-156.250
156.25MHZ
JP6
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
C104 10NF 25V
C105 10NF 25V
C106 10NF 25V
C107 10NF 25V
C109 10NF 25V
C108 10NF 25V
MGTAVTTTX_114 AC3 MGTAVTTTX_114
MGTAVTTTX_114_1 V3 MGTAVTTTX_114_1
MGTTX0_114_P V2 MGTTX0_114_P
MGTTX0_114_N W2 MGTTX0_114_N
MGTTX1_114_P AC2 MGTTX1_114_P
MGTTX1_114_N AB2 MGTTX1_114_N
MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT
FB8 220@100M
FB7 220@100M
C98 220NF 6.3V
C99 220NF 6.3V
P3
FCN-268F036-G/3DB
ODIS
FAULT
SIG_GND1 G1
SIG_GND2 G2
SIG_GND3 G3
SIG_GND4 G4
SIG_GND5 G5
SIG_GND6 G6
SIG_GND7 G7
SIG_GND8 G8
SIG_GND9 G9
SIG_GND10 G19
JP4
R50 10K
C130 10NF
3V3
R79 150R
D2
OPTICAL MODULE FAULT - RED LED
C131 10NF
R97 5K1
RS7 3K9
R59 6K8
RS8 3K9
U21 MAX9032AKA
U20 MAX9032AKA
C127 10NF
U22 AND2 SN74AHC1G08DCKR
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB11 220@100M
FB12 220@100M
FB9 220@100M
FB10 220@100M
C103 220NF 6.3V
C102 220NF 6.3V
C101 220NF 6.3V
C100 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_114 AA3 MGTAVCC_114
MGTAVCC_114_1 AA4 MGTAVCC_114_1
MGTAVCCPLL_114 AB3 MGTAVCCPLL_114
MGTAVTTRX_114 W3 MGTAVTTRX_114
MGT_114_REF_CLK_P NC Y4 MGT_114_REF_CLK_P
MGT_114_REF_CLK_N NC Y3 MGT_114_REF_CLK_N
MGTRX0_114_P W1 MGTRX0_114_P
MGTRX0_114_N Y1 MGTRX0_114_N
MGTRX1_114_P AB1 MGTRX1_114_P
MGTRX1_114_N AA1 MGTRX1_114_N
U15
C140 10NF 25V
C141 10NF 25V
C142 10NF 25V
C143 10NF 25V
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB17 220@100M
FB18 220@100M
FB15 220@100M
FB16 220@100M
C120 220NF 6.3V
C119 220NF 6.3V
C118 220NF 6.3V
C115 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_116 J3 MGTAVCC_116
MGTAVCC_116_1 J4 MGTAVCC_116_1
MGTAVCCPLL_116 K3 MGTAVCCPLL_116
MGTAVTTRX_116 G3 MGTAVTTRX_116
MGT_116_REF_CLK_P NC H4 MGT_116_REF_CLK_P
MGT_116_REF_CLK_N NC H3 MGT_116_REF_CLK_N
MGTRX0_116_P G1 MGTRX0_116_P
MGTRX0_116_N H1 MGTRX0_116_N
MGTRX1_116_P K1 MGTRX1_116_P
MGTRX1_116_N J1 MGTRX1_116_N
U15
C110 10NF 25V
C111 10NF 25V
C112 10NF 25V
C113 10NF 25V
MGTAVTTTX_116_1 L3 MGTAVTTTX_116_1
MGTAVTTTX_116 F3 MGTAVTTTX_116
MGTTX0_116_P F2 MGTTX0_116_P
MGTTX0_116_N G2 MGTTX0_116_N
MGTTX1_116_P L2 MGTTX1_116_P
MGTTX1_116_N K2 MGTTX1_116_N
FB14 220@100M
FB13 220@100M
C116 220NF 6.3V
C117 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
P3
FCN-268F036-G/3DB
ODIS
FAULT
SIG_GND1 G10
SIG_GND2 G11
SIG_GND3 G12
SIG_GND4 G13
SIG_GND5 G14
SIG_GND6 G15
SIG_GND7 G16
SIG_GND8 G17
SIG_GND9 G18
SIG_GND10 G19
JP5
R51 10K
C134 10NF
3V3
R82 150R
D3
OPTICAL MODULE FAULT - RED LED
C132 10NF
R98 5K1
R93 3K9
R94 6K8
R95 3K9
U23 AND2 SN74AHC1G08DCKR
MAX9032AKA
C133 10NF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB22 220@100M
FB21 220@100M
FB24 220@100M
FB23 220@100M
C123 220NF 6.3V
C124 220NF 6.3V
C114 220NF 6.3V
C125 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_118 AG3 MGTAVCC_118
MGTAVCC_118_1 AG4 MGTAVCC_118_1
MGTAVCCPLL_118 AH3 MGTAVCCPLL_118
MGTAVTTRX_118 AE3 MGTAVTTRX_118
MGT_118_REF_CLK_P NC AF4 MGT_118_REF_CLK_P
MGT_118_REF_CLK_N NC AF3 MGT_118_REF_CLK_N
MGTRX0_118_P AE1 MGTRX0_118_P
MGTRX0_118_N AF1 MGTRX0_118_N
MGTRX1_118_P AH1 MGTRX1_118_P
MGTRX1_118_N AG1 MGTRX1_118_N
U15
C144 10NF 25V
C145 10NF 25V
C146 10NF 25V
C147 10NF 25V
MGTAVTTTX_118_1 AJ3 MGTAVTTTX_118_1
MGTAVTTTX_118 AD3 MGTAVTTTX_118
MGTTX0_118_P AD2 MGTTX0_118_P
MGTTX0_118_N AE2 MGTTX0_118_N
MGTTX1_118_P AJ2 MGTTX1_118_P
MGTTX1_118_N AH2 MGTTX1_118_N
FB19 220@100M
FB20 220@100M
C122 220NF 6.3V
C121 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
P3
FCN-268F036-G/3DB
ODIS
FAULT
SIG_GND1 G10
SIG_GND2 G11
SIG_GND3 G12
SIG_GND4 G13
SIG_GND5 G14
SIG_GND6 G15
SIG_GND7 G16
SIG_GND8 G17
SIG_GND9 G18
SIG_GND10 G19
R99 10K
U18 TPS2031D
C129 10NF
C128 100NF
C138 4.7UF 16V
C90 22UF
R100 10K
U19 TPS2031D
C135 10NF
C136 100NF
C139 4.7UF 16V
C91 22UF

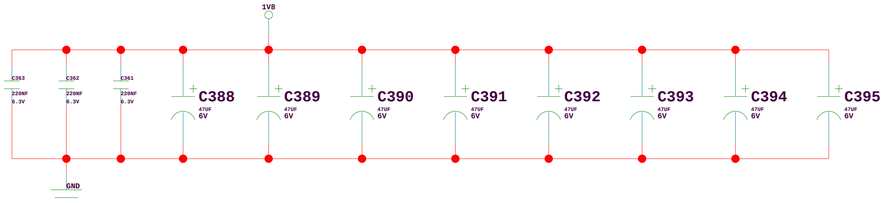
ROACH/iBOB2	**ROACH_TRANSCEIVERS0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 8 OF 25
10-5-2007_16:36	
PATH PATH	

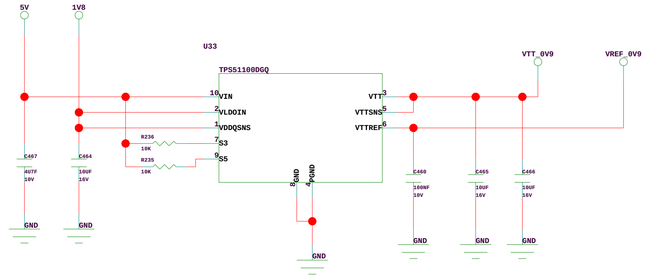
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB28 220@100M
FB29 220@100M
FB30 220@100M
FB31 220@100M
C172 220NF 6.3V
C171 220NF 6.3V
C170 220NF 6.3V
C169 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_120 D5 MGTAVCC_120
MGTAVCC_120_1 F4 MGTAVCC_120_1
MGTAVCCPLL_120 D3 MGTAVCCPLL_120
MGTAVTTRX_120 C3 MGTAVTTRX_120
MGT_120_REF_CLK_P E4 MGT_120_REF_CLK_P
MGT_120_REF_CLK_N D4 MGT_120_REF_CLK_N
MGTRX0_120_P A3 MGTRX0_120_P
MGTRX0_120_N A2 MGTRX0_120_N
MGTRX1_120_P D1 MGTRX1_120_P
MGTRX1_120_N C1 MGTRX1_120_N
U15
MGTAVTTTX_120_1 E3 MGTAVTTTX_120_1
MGTAVTTTX_120 C4 MGTAVTTTX_120
MGTTX0_120_P B4 MGTTX0_120_P
MGTTX0_120_N B3 MGTTX0_120_N
MGTTX1_120_P E2 MGTTX1_120_P
MGTTX1_120_N D2 MGTTX1_120_N
MGT_AVTT
FB32 220@100M
FB33 220@100M
C174 220NF 6.3V
C173 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
2V5
FB52 220@100M
C248 220NF 6.3V
R131 10K
X4
OE
VCC
OUT+ MGT_REFCLK_Q2_P
OUT- MGT_REFCLK_Q2_N
GND
JP9
CCLD-023-25-156.250
156.25MHZ
C181 10NF 25V
C182 10NF 25V
C183 10NF 25V
C184 10NF 25V
C186 10NF 25V
C185 10NF 25V
P3
S39 DL0P
S40 DL0N
S41 DL1P
S42 DL1N
S43 DL2P
S44 DL2N
S45 DL3P
S46 DL3N
S54 SL0P
S53 SL0N
S52 SL1P
S51 SL1N
S50 SL2P
S49 SL2N
S48 SL3P
S47 SL3N
SIG_GND1 G20
SIG_GND2 G21
SIG_GND3 G22
SIG_GND4 G23
SIG_GND5 G24
SIG_GND6 G25
SIG_GND7 G26
SIG_GND8 G27
SIG_GND9 G28
SIG_GND10 G19
FCN-268F036-G/3DB
ODIS
FAULT
JP7
R123 10K
C240 10NF
C242 10NF
3V3
R132 150R
OPTICAL MODULE FAULT - RED LED
R121 5K1
R120 3K9
R119 6K8
R118 3K9
C241 10NF
U34 MAX9032AKA
U30 MAX9032AKA
U36 AND2 SN74AHC1G08DCKR
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB38 220@100M
FB39 220@100M
FB36 220@100M
FB37 220@100M
C180 220NF 6.3V
C179 220NF 6.3V
C178 220NF 6.3V
C177 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_122 AJ4 MGTAVCC_122
MGTAVCC_122_1 AK5 MGTAVCC_122_1
MGTAVCCPLL_122 AM4 MGTAVCCPLL_122
MGTAVTTRX_122 AL3 MGTAVTTRX_122
MGT_122_REF_CLK_P NC AL5 MGT_122_REF_CLK_P
MGT_122_REF_CLK_N NC AL4 MGT_122_REF_CLK_N
MGTRX0_122_P AL1 MGTRX0_122_P
MGTRX0_122_N AM1 MGTRX0_122_N
MGTRX1_122_P AP3 MGTRX1_122_P
MGTRX1_122_N AP2 MGTRX1_122_N
U15
MGTAVTTTX_122_1 AM3 MGTAVTTTX_122_1
MGTAVTTTX_122 AK3 MGTAVTTTX_122
MGTTX0_122_P AK2 MGTTX0_122_P
MGTTX0_122_N AL2 MGTTX0_122_N
MGTTX1_122_P AN4 MGTTX1_122_P
MGTTX1_122_N AN3 MGTTX1_122_N
MGT_AVTT
FB35 220@100M
FB34 220@100M
C175 220NF 6.3V
C176 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C251 10NF 25V
C252 10NF 25V
C250 10NF 25V
C249 10NF 25V
C256 10NF 25V
C255 10NF 25V
C254 10NF 25V
C253 10NF 25V
U28
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
GND
TPS2031D
R130 10K
R117 10K
C246 10NF
C247 100NF
C168 4.7UF 16V
C166 22UF
C239 10NF
C227 100NF
C167 4.7UF 16V
C165 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB49 220@100M
FB48 220@100M
FB51 220@100M
FB50 220@100M
C224 220NF 6.3V
C225 220NF 6.3V
C191 220NF 6.3V
C226 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_126 AL8 MGTAVCC_126
MGTAVCC_126_1 AM8 MGTAVCC_126_1
MGTAVCCPLL_126 AM9 MGTAVCCPLL_126
MGTAVTTRX_126 AM6 MGTAVTTRX_126
MGT_126_REF_CLK_P NC AL7 MGT_126_REF_CLK_P
MGT_126_REF_CLK_N NC AM7 MGT_126_REF_CLK_N
MGTRX0_126_P AP6 MGTRX0_126_P
MGTRX0_126_N AP7 MGTRX0_126_N
MGTRX1_126_P AP9 MGTRX1_126_P
MGTRX1_126_N AP8 MGTRX1_126_N
U15
MGTAVTTTX_126_1 AM5 MGTAVTTTX_126_1
MGTAVTTTX_126 AM10 MGTAVTTTX_126
MGTTX0_126_P AN5 MGTTX0_126_P
MGTTX0_126_N AN6 MGTTX0_126_N
MGTTX1_126_P AN10 MGTTX1_126_P
MGTTX1_126_N AN9 MGTTX1_126_N
MGT_AVTT
FB46 220@100M
FB47 220@100M
C223 220NF 6.3V
C222 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_124 C7 MGTAVCC_124
MGTAVCC_124_1 D7 MGTAVCC_124_1
MGTAVCCPLL_124 C6 MGTAVCCPLL_124
MGTAVTTRX_124 C9 MGTAVTTRX_124
MGT_124_REF_CLK_P NC D8 MGT_124_REF_CLK_P
MGT_124_REF_CLK_N NC C8 MGT_124_REF_CLK_N
MGTRX0_124_P A9 MGTRX0_124_P
MGTRX0_124_N A8 MGTRX0_124_N
MGTRX1_124_P A6 MGTRX1_124_P
MGTRX1_124_N A7 MGTRX1_124_N
U15
MGTAVTTTX_124_1 C5 MGTAVTTTX_124_1
MGTAVTTTX_124 C10 MGTAVTTTX_124
MGTTX0_124_P B10 MGTTX0_124_P
MGTTX0_124_N B9 MGTTX0_124_N
MGTTX1_124_P B5 MGTTX1_124_P
MGTTX1_124_N B6 MGTTX1_124_N
MGT_AVTT
FB41 220@100M
FB40 220@100M
C213 220NF 6.3V
C214 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C187 10NF 25V
C188 10NF 25V
C189 10NF 25V
C190 10NF 25V
P3
S57 DL0P
S58 DL0N
S59 DL1P
S60 DL1N
S61 DL2P
S62 DL2N
S63 DL3P
S64 DL3N
S72 SL0P
S71 SL0N
S70 SL1P
S69 SL1N
S68 SL2P
S67 SL2N
S66 SL3P
S65 SL3N
SIG_GND1 G29
SIG_GND2 G30
SIG_GND3 G31
SIG_GND4 G32
SIG_GND5 G33
SIG_GND6 G34
SIG_GND7 G35
SIG_GND8 G36
SIG_GND9 G37
SIG_GND10 G19
FCN-268F036-G/3DB
ODIS
FAULT
JP8
R124 10K
C245 10NF
C243 10NF
3V3
R135 150R
OPTICAL MODULE FAULT - RED LED
R126 5K1
R127 3K9
R128 6K8
R129 3K9
C244 10NF
U34 MAX9032AKA
U30 MAX9032AKA
U37 AND2 SN74AHC1G08DCKR
U29
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
GND
TPS2031D
R136 10K
C247 100NF
C168 4.7UF 16V
C166 22UF
C246 10NF
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
10-5-2007_16:36
PATH PATH
ROACH_TRANSCEIVERS2_3
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE MW
DRAWN: F KAPP
CHECKED: E BAUERMEISTER
APPR:
SHEET 9 OF 25

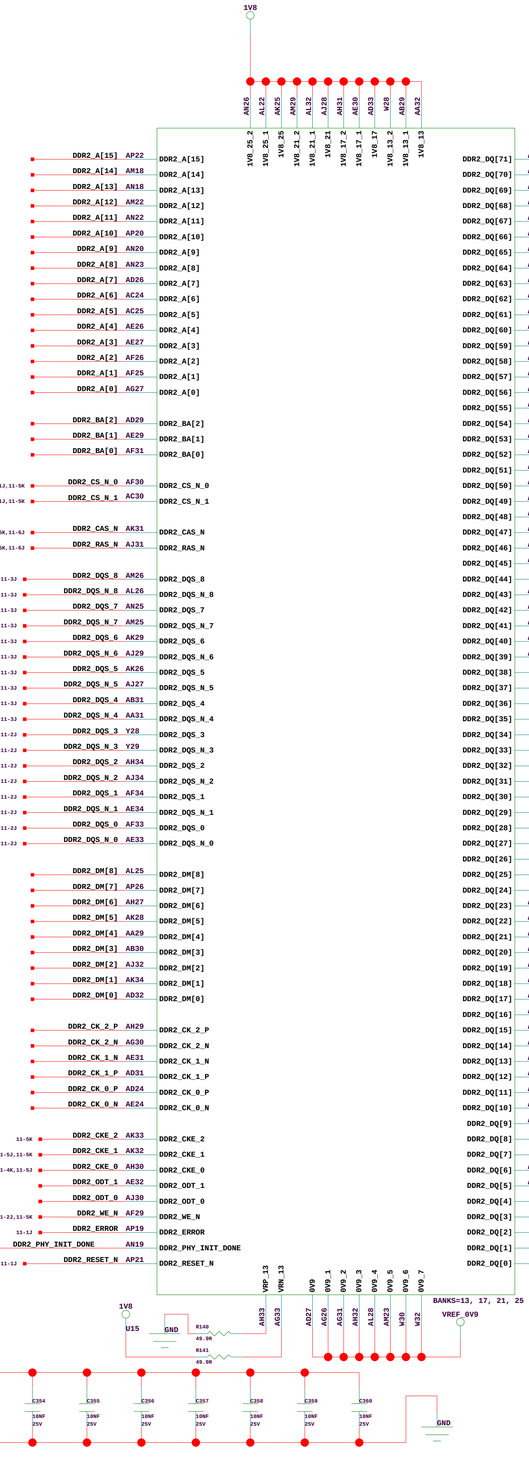


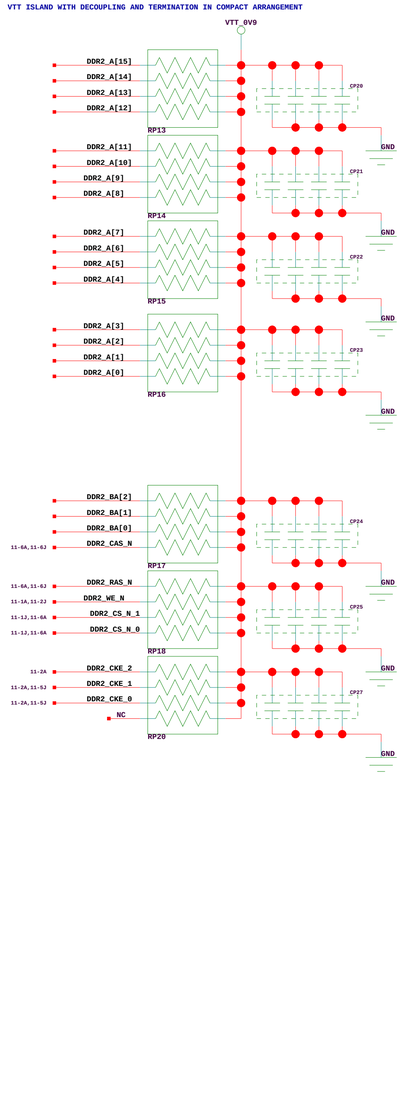


ROACH/iBOB2	**ROACH_TRANSCEIVERS_PSU**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 10 OF 25
10-5-2007_16:36 PATH PATH	

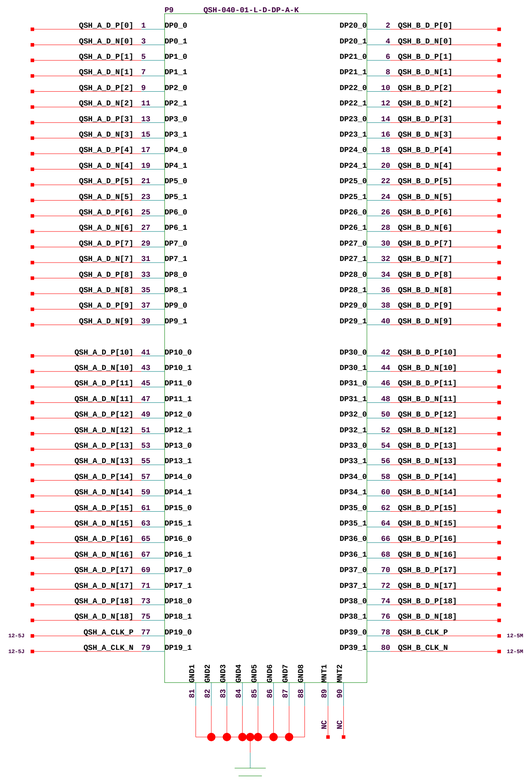


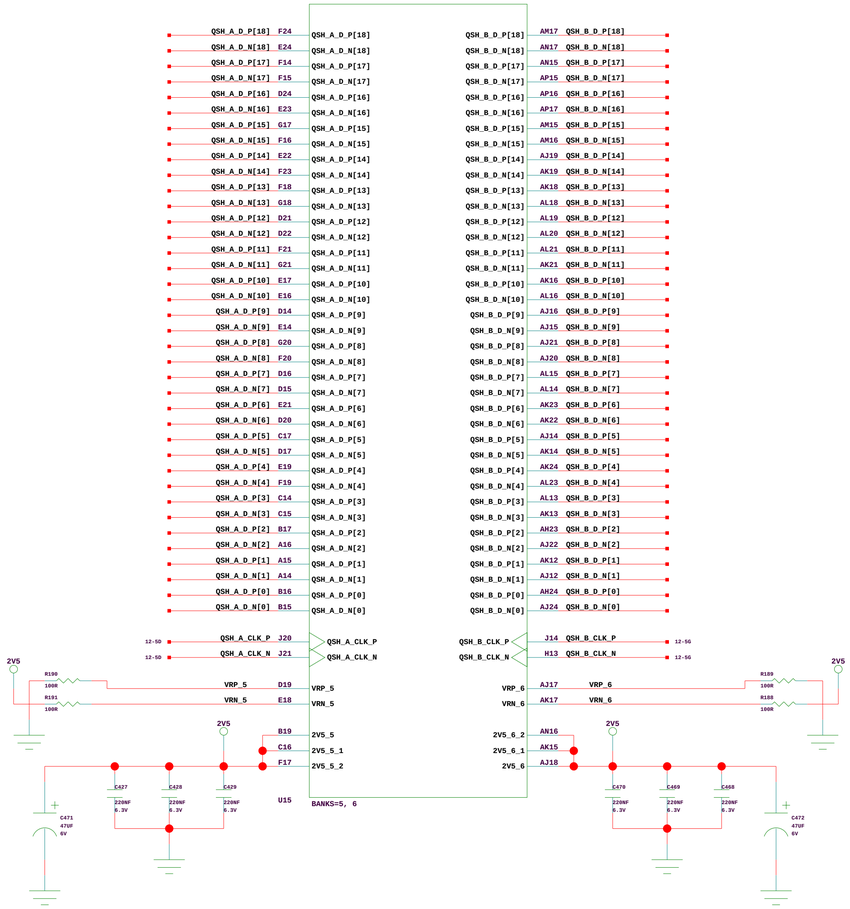






ROACH/iBOB2	**ROACH_DDR2_DIMM**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_16:36 PATH PATH	DRAWN: F KAPP APPR:
	CHECKED: E BAUERMEISTER SHEET 11 OF 25





ROACH/iBOB2	**ROACH_DIFF_GPIO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_16:36 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 12 OF 25

GPIOLVC33[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

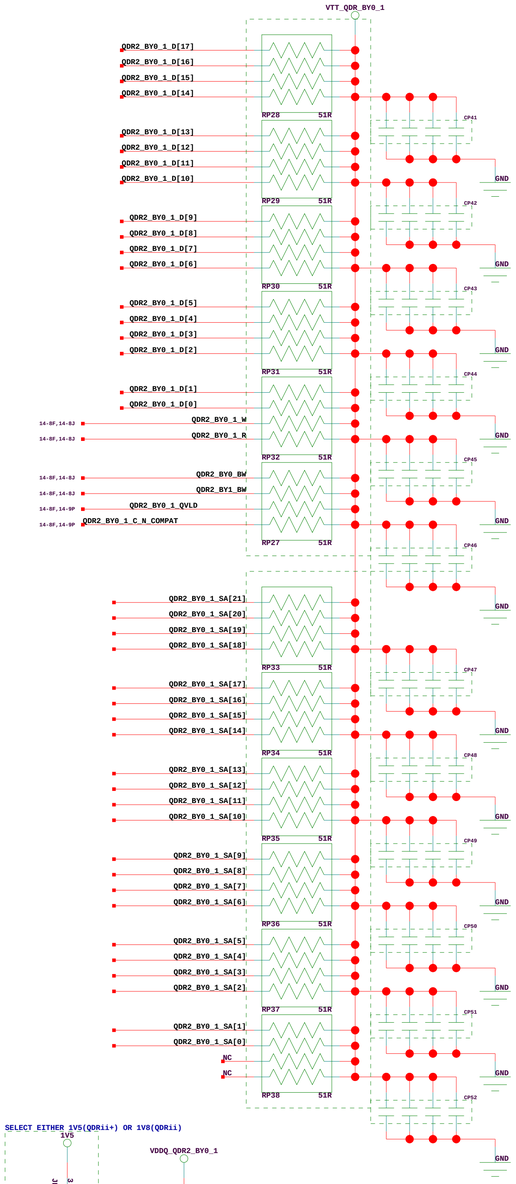
GPIOLVC18[20] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

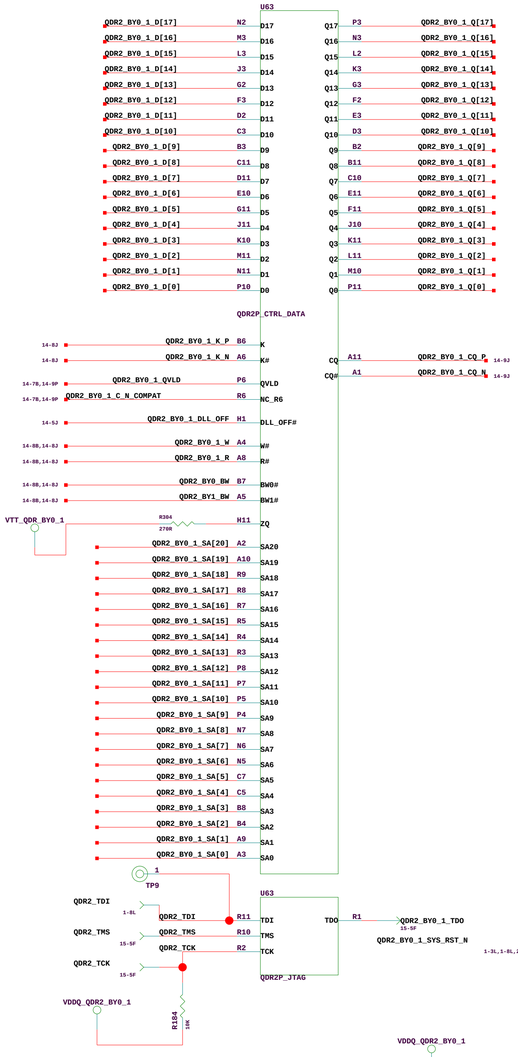
IO VOLTAGE LEVEL SELECT
1-2: 3.3V
2-3: 2.5V

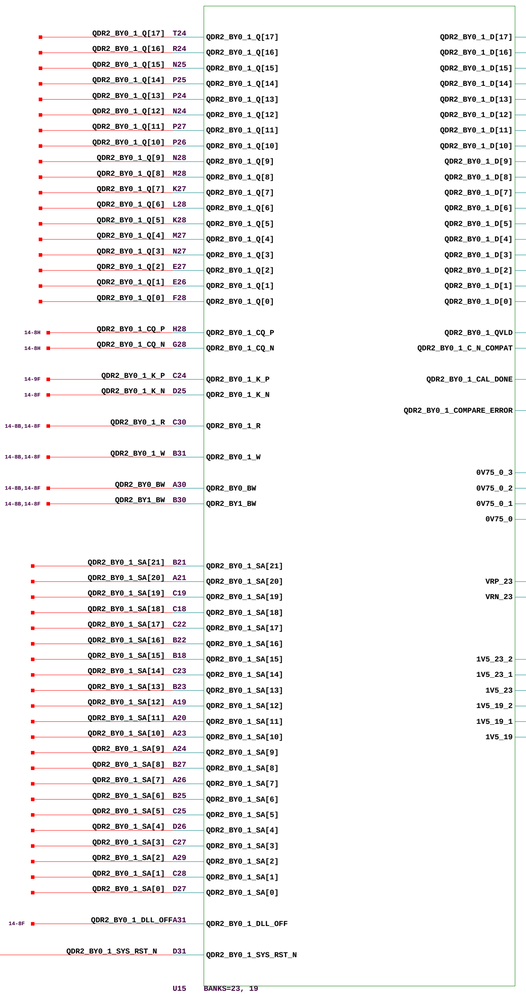
HLE-105-02-G-DV

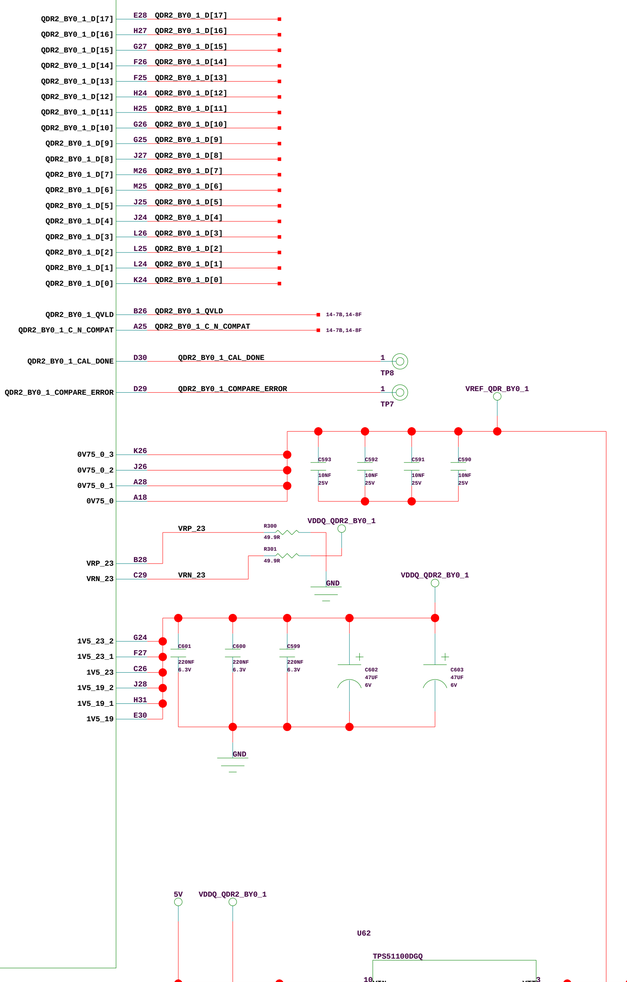
74AVCH4T245DGVRE4

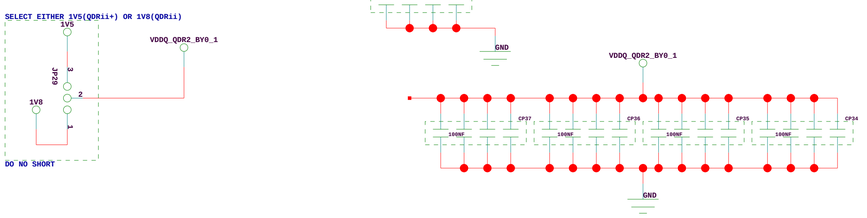
ROACH/iBOB2	ROACH_GPIO_MISC	
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
10-5-2007_16:36 PATH PATH	DRAWN: F KAPP CHECKED: E BAUERMEISTER	APPR: SHEET 13 OF 25

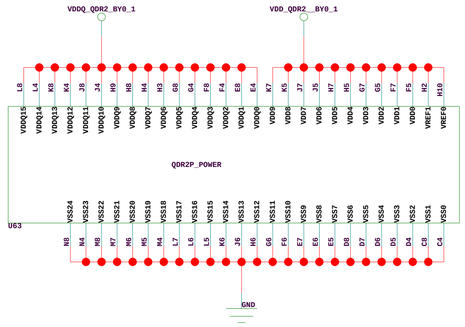


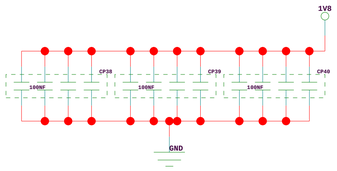


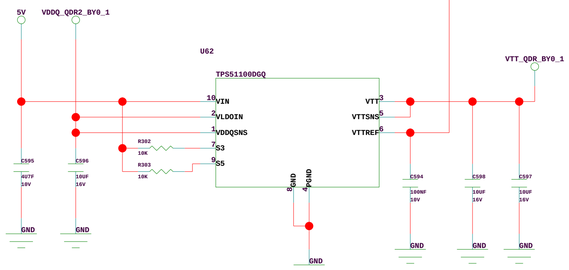




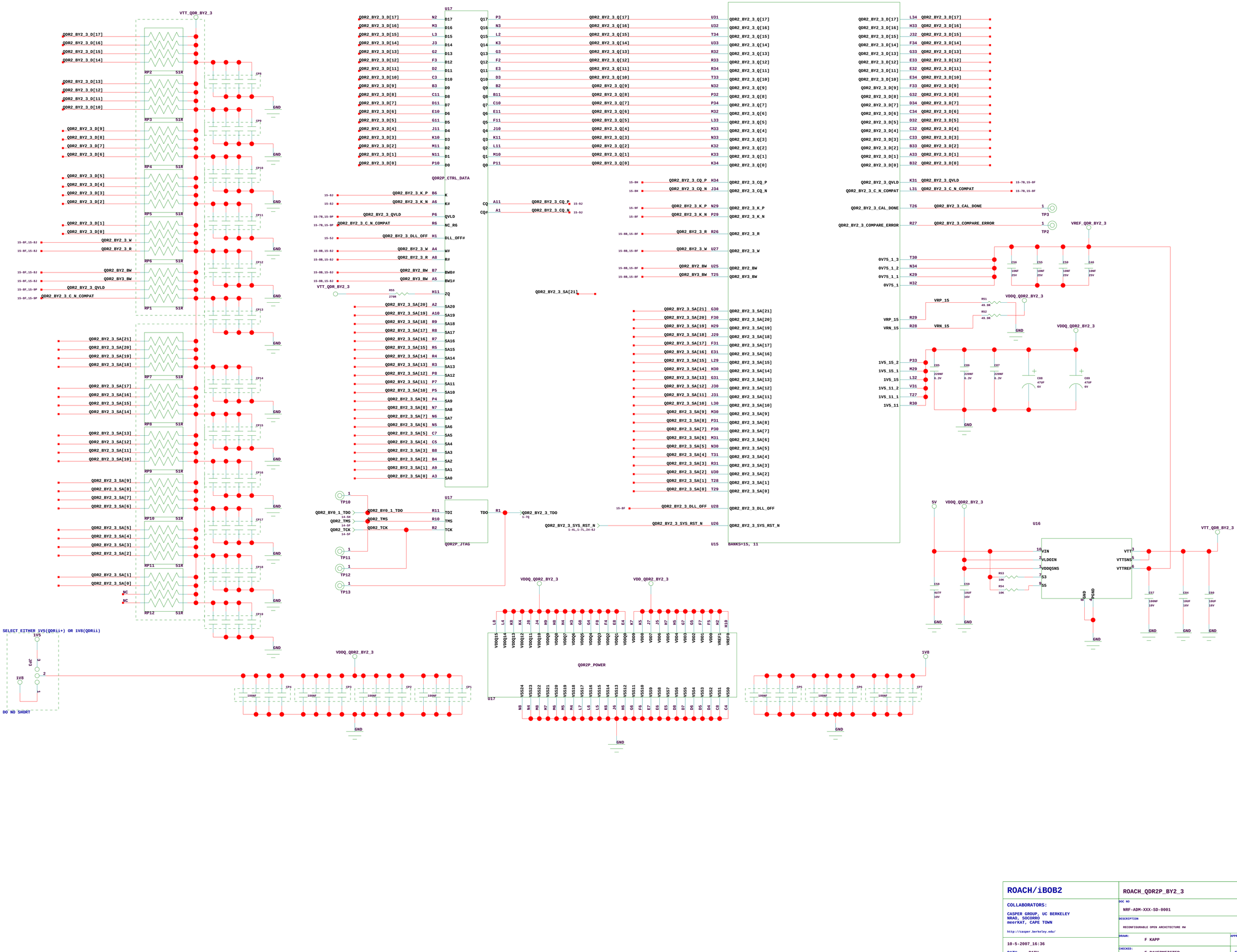








ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 14 OF 25
10-5-2007_16:36 PATH PATH	

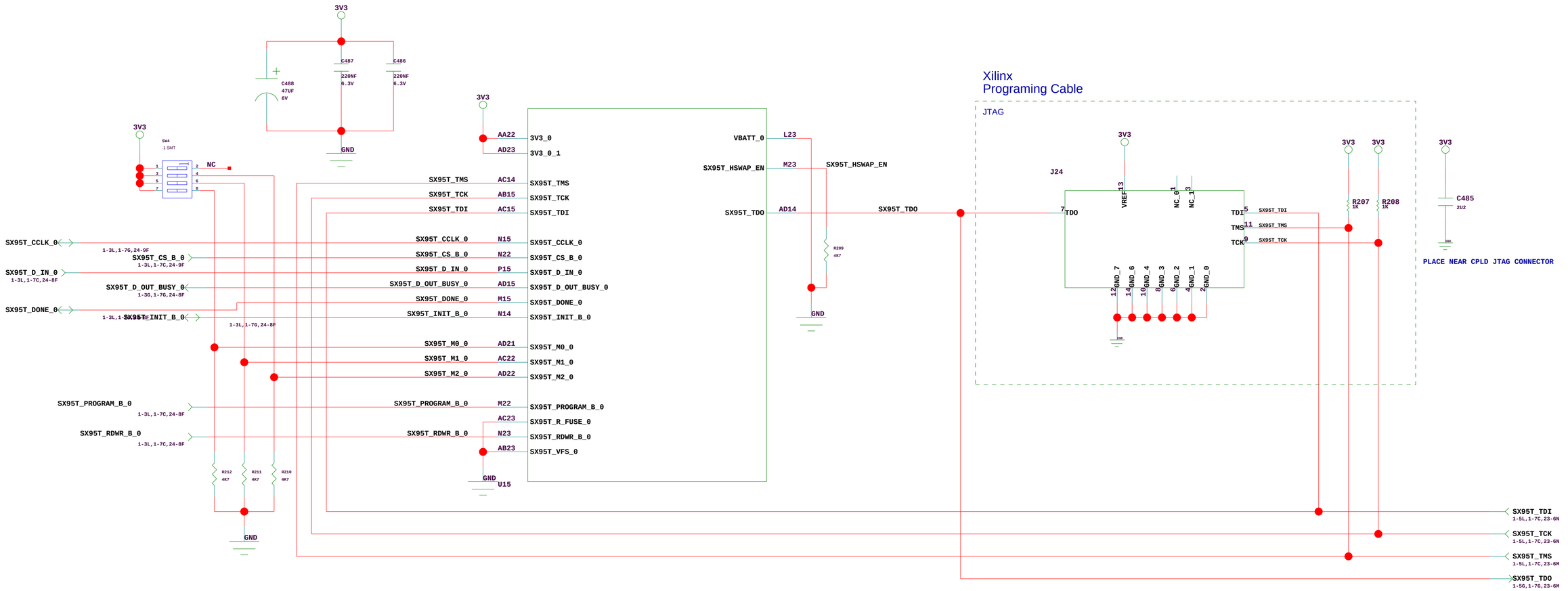


ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 15 OF 25
10-5-2007_16:36 PATH PATH	

TBD

VALID CONFIGURATION MODES

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input



ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
10-5-2007_16:36 PATH PATH	

Place components close to CPU

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J3: "1V5"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J4: "1V8"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J5: "2V5"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J6: "3V3"

Place components close to CPU

Place components close to CPU

Alternate power input terminal
Two 10A fuses result in 16A rating

+5.0 V

Bulk Decoupling

CPU Core by-pass caps place as close to CPU Vdd pins as possible

CPU Core by-pass caps place as close to CPU SOVdd pins as possible

CPU Core by-pass caps place as close to CPU DVdd pins as possible

Each Analog GND tied to Digital GND at a single point.

+1.8 V

Place all components within this block close together

~2.9Amp

~3.6Amp

Place these 4 caps close to DDR parts

VOUT= 0.6v(1+R1/R2)

+1.5 V

VOUT= 0.6v(1+R1/R2)
PLLLPF = VIN = 750khz

PWR_GOOD

1-4D,1-4G,1-5E,1-5G,18-2F,23-19G,24-8K

Place all components within this block close together

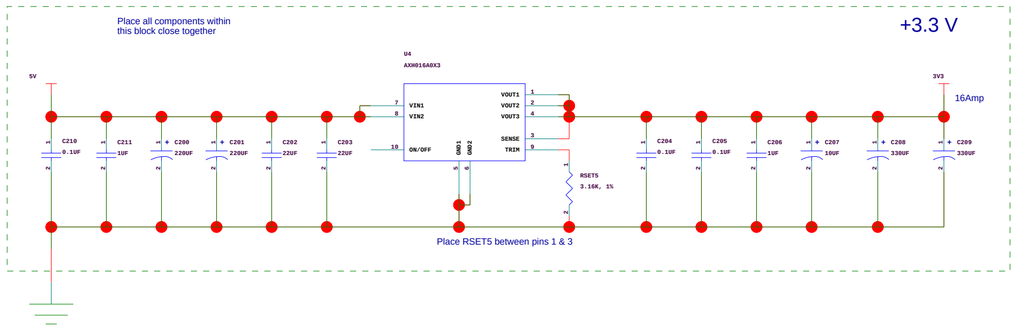
+0.9 V

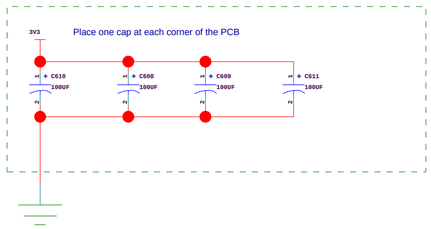
Use 25mil trace

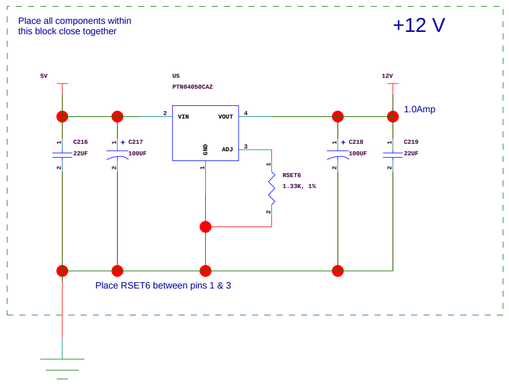
VTT_+0.9V
1-5E

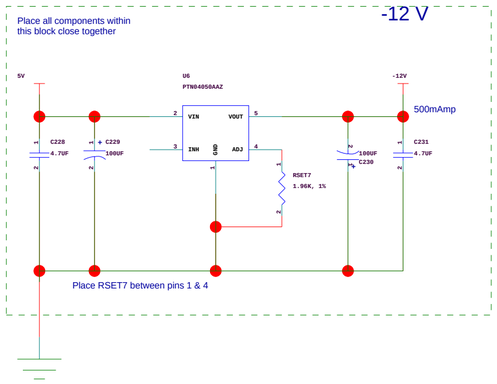
VTT island by-pass caps place evenly across VTT island
(1 cap for every 2 signals terminated)
(1 Tantalum Cap on each end of island)
VTT regulator placed at center of VTT island

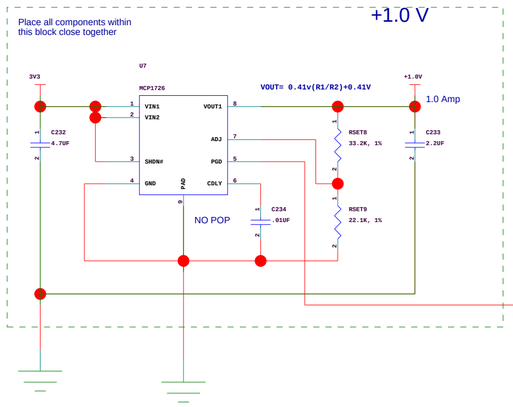
ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 17 OF 25
10-5-2007_16:36 PATH PATH	

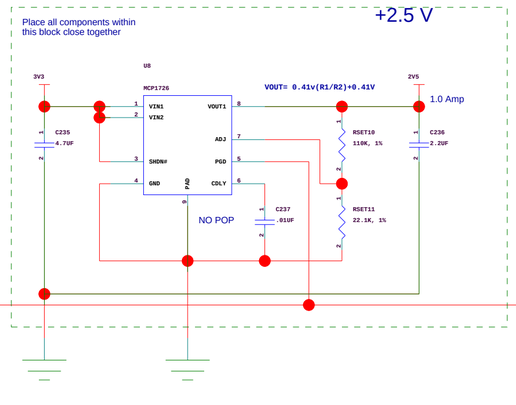






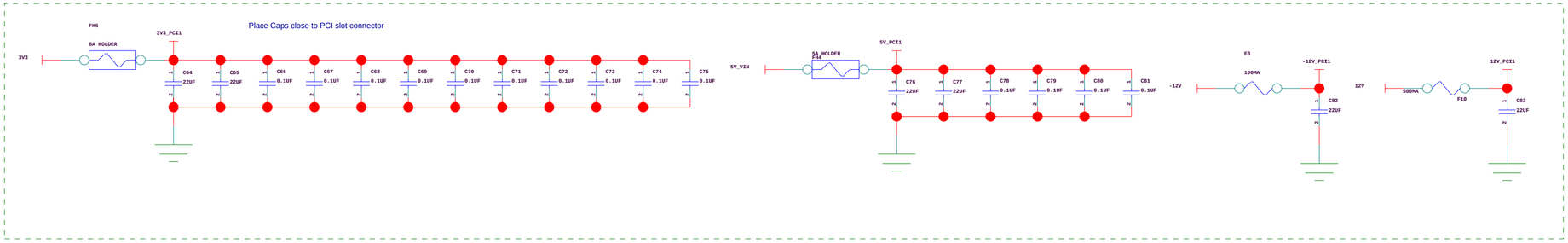


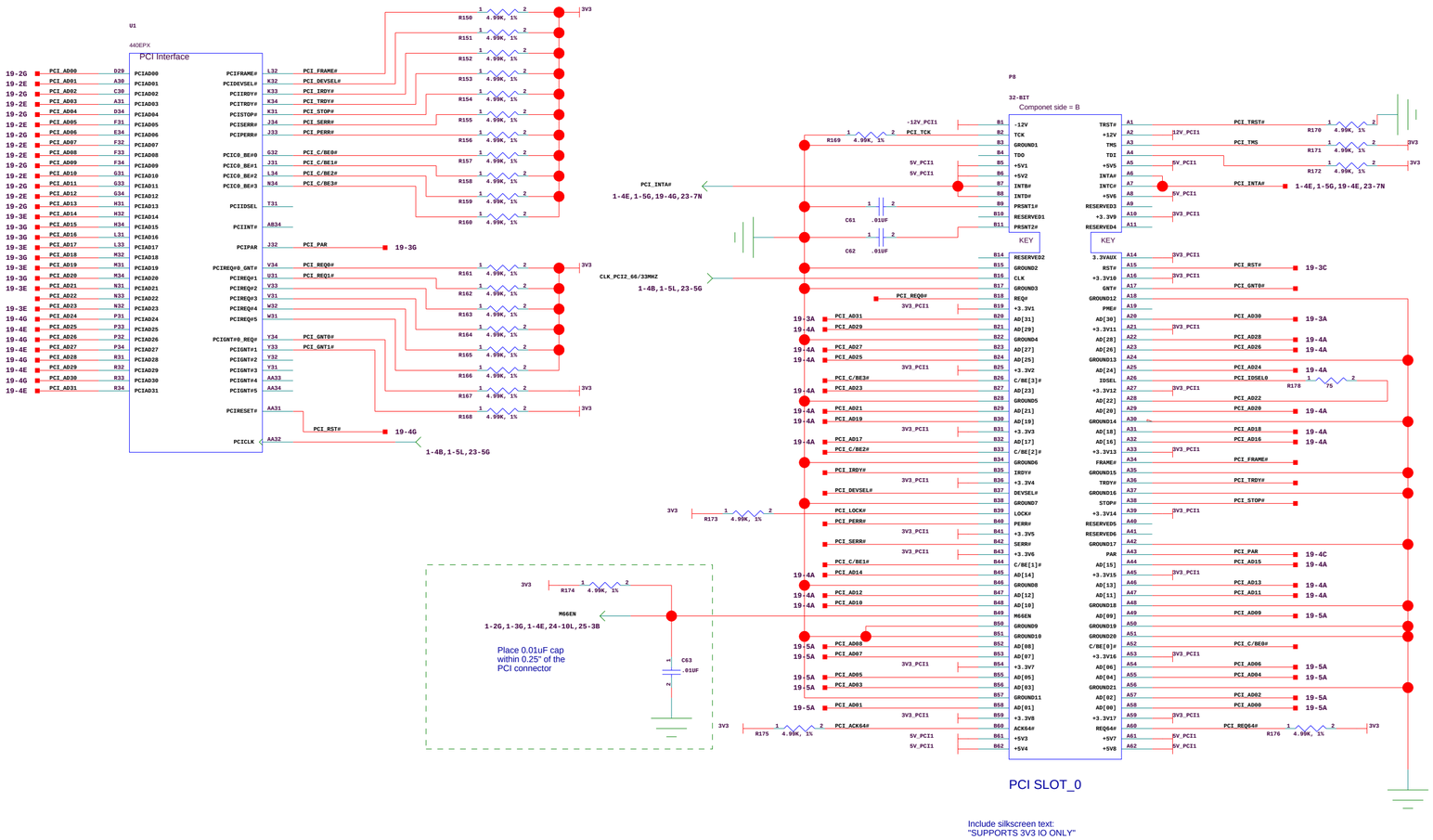




PWR_GOOD
1-4D,1-4G,1-5E,1-5G,17-3F,23-10G,24-8K

ROACH/iBOB2	**ROACH_PPC_POWER_2**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 18 OF 25
10-5-2007_16:36 PATH PATH	





PCI SLOT_0

Include silkscreen text:
"SUPPORTS 3V3 IO ONLY"

Optional PRSNT signals are not used, max 25W is available		
PRSNT1#	PRSNT2#	Expansion Configuration
Open	Open	No expansion board present
Ground	Open	Expansion board present, 25 W maximum
Open	Ground	Expansion board present, 15 W maximum
Ground	Ground	Expansion board present, 7.5 W maximum

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

10-5-2007_16:36

PATH PATH

ROACH_PPC_PCI

DOC NO	REVISION
NRF-ADM-XXX-SD-0001	A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN:	APPR:
F KAPP	
CHECKED: E BAUERMEISTER	SHEET 19 OF 25

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.
Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

ETHERNET Mgt.

Place nearest PHY pin 96

Place nearest PHY pin 101

Place nearest PHY pin 98

Place nearest PHY pin 100

Place as close to PHY CORE VDD power pins as possible

Place as close to PHY IO VDD power pins as possible

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place jumpers in line with signals

Place decoupling C close to termination R All traces 50Ohm WRT GND or 2V5

Ethernet LEDs

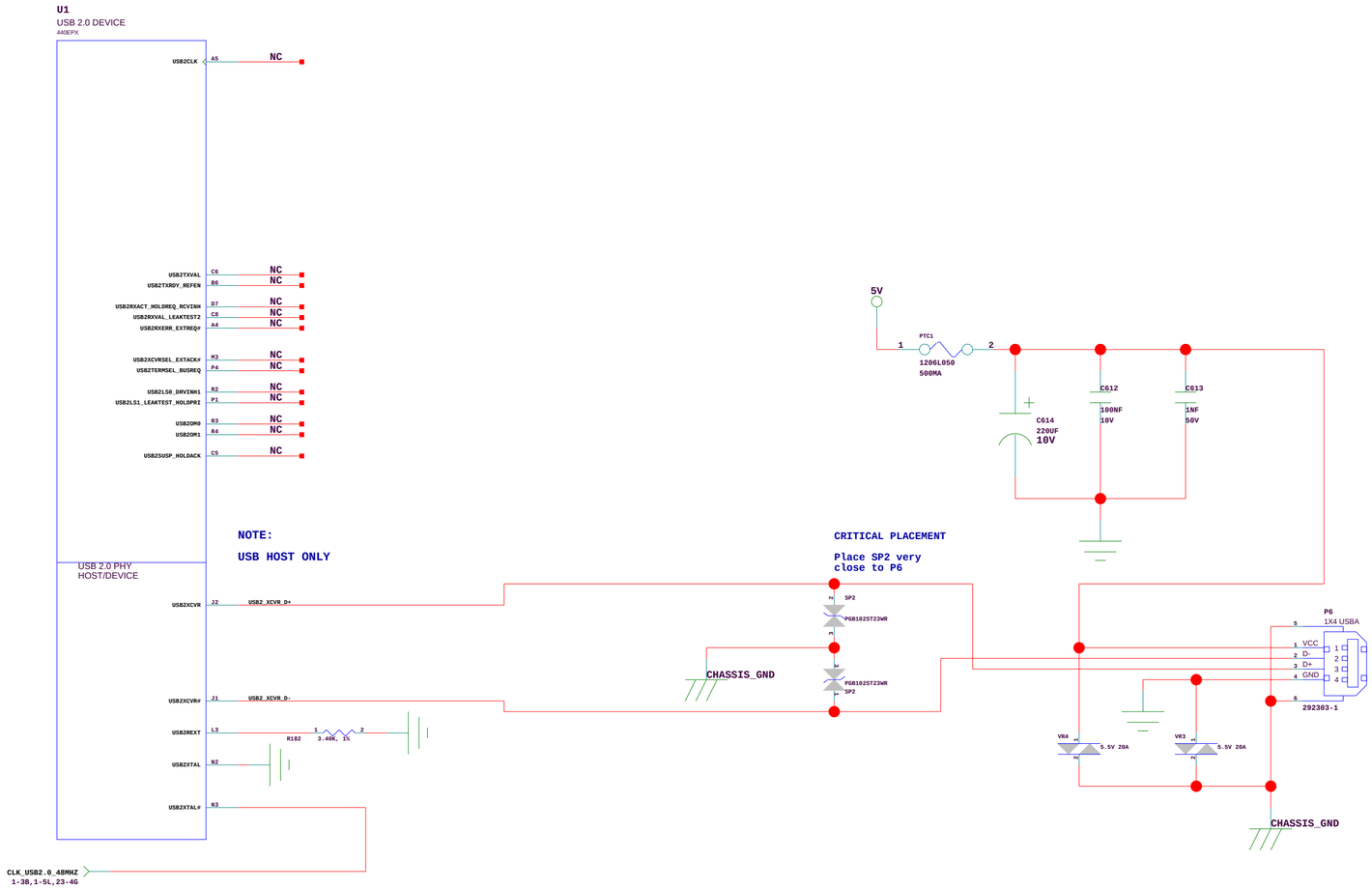
Top LED = SPEED/LINK
Green = 1000
Off = 10/100

Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY

UNUSED SECOND ETHERNET MAC

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

ROACH/iBOB2	ROACH_PPC_ETH1
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_16:36	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 20 OF 25



ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25
10-5-2007_16:36 PATH PATH	

DDR_PA[15:0]

DDR_PD0[63:0]

U1

DDR SDRAM

64DEPX

DDR_PD0	MEMDATA00	MEMADDR00	DDR_PA0
DDR_PD1	MEMDATA01	MEMADDR01	DDR_PA1
DDR_PD2	MEMDATA02	MEMADDR02	DDR_PA2
DDR_PD3	MEMDATA03	MEMADDR03	DDR_PA3
DDR_PD4	MEMDATA04	MEMADDR04	DDR_PA4
DDR_PD5	MEMDATA05	MEMADDR05	DDR_PA5
DDR_PD6	MEMDATA06	MEMADDR06	DDR_PA6
DDR_PD7	MEMDATA07	MEMADDR07	DDR_PA7
DDR_PD8	MEMDATA08	MEMADDR08	DDR_PA8
DDR_PD9	MEMDATA09	MEMADDR09	DDR_PA9
DDR_PD10	MEMDATA10	MEMADDR10	DDR_PA10
DDR_PD11	MEMDATA11	MEMADDR11	DDR_PA11
DDR_PD12	MEMDATA12	MEMADDR12	DDR_PA12
DDR_PD13	MEMDATA13	MEMADDR13	DDR_PA13
DDR_PD14	MEMDATA14		
DDR_PD15	MEMDATA15	BA0	DDR_PBA0
DDR_PD16	MEMDATA16	BA1	DDR_PBA1
DDR_PD17	MEMDATA17	BA2	DDR_PBA2
DDR_PD18	MEMDATA18		
DDR_PD19	MEMDATA19	RAS#	DDR_PRAS#
DDR_PD20	MEMDATA20	CAS#	DDR_PCAS#
DDR_PD21	MEMDATA21	WE#	DDR_PWE#
DDR_PD22	MEMDATA22		
DDR_PD23	MEMDATA23	DM0	DDR_PDM0
DDR_PD24	MEMDATA24	DM1	DDR_PDM1
DDR_PD25	MEMDATA25	DM2	DDR_PDM2
DDR_PD26	MEMDATA26	DM3	DDR_PDM3
DDR_PD27	MEMDATA27	DM4	DDR_PDM4
DDR_PD28	MEMDATA28	DM5	DDR_PDM5
DDR_PD29	MEMDATA29	DM6	DDR_PDM6
DDR_PD30	MEMDATA30	DM7	DDR_PDM7
DDR_PD31	MEMDATA31	DM8	DDR_PDM8
DDR_PD32	MEMDATA32		
DDR_PD33	MEMDATA33	DQS0	DDR_PDQS0
DDR_PD34	MEMDATA34	DQS1	DDR_PDQS1
DDR_PD35	MEMDATA35	DQS2	DDR_PDQS2
DDR_PD36	MEMDATA36	DQS3	DDR_PDQS3
DDR_PD37	MEMDATA37	DQS4	DDR_PDQS4
DDR_PD38	MEMDATA38	DQS5	DDR_PDQS5
DDR_PD39	MEMDATA39	DQS6	DDR_PDQS6
DDR_PD40	MEMDATA40	DQS7	DDR_PDQS7
DDR_PD41	MEMDATA41	DQS8	DDR_PDQS8
DDR_PD42	MEMDATA42		
DDR_PD43	MEMDATA43	MEMODT0	DDR_PODT0
DDR_PD44	MEMDATA44	MEMODT1	DDR_PODT1
DDR_PD45	MEMDATA45		
DDR_PD46	MEMDATA46	BANKSEL#0	DDR_PCS0#
DDR_PD47	MEMDATA47	BANKSEL#1	DDR_PCS1#
DDR_PD48	MEMDATA48		
DDR_PD49	MEMDATA49	MEMCLKEN	DDR_PCKE
DDR_PD50	MEMDATA50		
DDR_PD51	MEMDATA51	MEMCLKOUT	DDR_CLKOUT
DDR_PD52	MEMDATA52		
DDR_PD53	MEMDATA53	MEMCLKOUT#	DDR_CLKOUT#
DDR_PD54	MEMDATA54		
DDR_PD55	MEMDATA55		
DDR_PD56	MEMDATA56		
DDR_PD57	MEMDATA57		
DDR_PD58	MEMDATA58		
DDR_PD59	MEMDATA59		
DDR_PD60	MEMDATA60		
DDR_PD61	MEMDATA61		
DDR_PD62	MEMDATA62		
DDR_PD63	MEMDATA63		

ECC0	PPC_ECC0	22-9F
ECC1	PPC_ECC1	22-9F
ECC2	PPC_ECC2	22-9F
ECC3	PPC_ECC3	22-10F
ECC4	PPC_ECC4	22-10F
ECC5	PPC_ECC5	22-10F
ECC6	PPC_ECC6	22-10F
ECC7	PPC_ECC7	22-10F

DDR_CLKOUT

DDR_CLKOUT#

R813 1 2 500ps Loop

DDR_VREF_0V9

1V8

C158 0.1UF

C148 0.1UF

C151 0.1UF 0402

C152 0.1UF 0402

C148 0.01UF

Place parts as close to CPU as possible

5V

1V8

U32

VIN 10

VLDOIN 2

VDDQSNS 1

S3 7

S5 9

R230 10K

R229 10K

GND 8

PGND 4

VTT 3

VTTSNS 5

VTTREF 6

DDR_VTT

DDR_VREF_0V9

C459 4U7F 10V

C456 10UF 16V

C453 100NF 10V

C457 10UF 16V

C458 10UF 16V

GND

J8

22-6D	PPC_ECC7	168	DDR2_DIMM_CB7
22-6D	PPC_ECC6	167	DDR2_DIMM_CB6
22-7D	PPC_ECC5	162	DDR2_DIMM_CB5
22-7D	PPC_ECC4	161	DDR2_DIMM_CB4
22-7D	PPC_ECC3	49	DDR2_DIMM_CB3
22-7D	PPC_ECC2	48	DDR2_DIMM_CB2
22-7D	PPC_ECC1	43	DDR2_DIMM_CB1
22-7D	PPC_ECC0	42	DDR2_DIMM_CB0
DDR_PDQ63		236	DDR2_DIMM_DQ[63]
DDR_PDQ62		235	DDR2_DIMM_DQ[62]
DDR_PDQ61		230	DDR2_DIMM_DQ[61]
DDR_PDQ60		229	DDR2_DIMM_DQ[60]
DDR_PDQ59		117	DDR2_DIMM_DQ[59]
DDR_PDQ58		116	DDR2_DIMM_DQ[58]
DDR_PDQ57		111	DDR2_DIMM_DQ[57]
DDR_PDQ56		110	DDR2_DIMM_DQ[56]
DDR_PDQ55		227	DDR2_DIMM_DQ[55]
DDR_PDQ54		226	DDR2_DIMM_DQ[54]
DDR_PDQ53		218	DDR2_DIMM_DQ[53]
DDR_PDQ52		217	DDR2_DIMM_DQ[52]
DDR_PDQ51		108	DDR2_DIMM_DQ[51]
DDR_PDQ50		107	DDR2_DIMM_DQ[50]
DDR_PDQ49		99	DDR2_DIMM_DQ[49]
DDR_PDQ48		98	DDR2_DIMM_DQ[48]
DDR_PDQ47		215	DDR2_DIMM_DQ[47]
DDR_PDQ46		214	DDR2_DIMM_DQ[46]
DDR_PDQ45		209	DDR2_DIMM_DQ[45]
DDR_PDQ44		208	DDR2_DIMM_DQ[44]
DDR_PDQ43		96	DDR2_DIMM_DQ[43]
DDR_PDQ42		95	DDR2_DIMM_DQ[42]
DDR_PDQ41		90	DDR2_DIMM_DQ[41]
DDR_PDQ40		89	DDR2_DIMM_DQ[40]
DDR_PDQ39		206	DDR2_DIMM_DQ[39]
DDR_PDQ38		205	DDR2_DIMM_DQ[38]
DDR_PDQ37		200	DDR2_DIMM_DQ[37]
DDR_PDQ36		199	DDR2_DIMM_DQ[36]
DDR_PDQ35		87	DDR2_DIMM_DQ[35]
DDR_PDQ34		86	DDR2_DIMM_DQ[34]
DDR_PDQ33		81	DDR2_DIMM_DQ[33]
DDR_PDQ32		80	DDR2_DIMM_DQ[32]
DDR_PDQ31		159	DDR2_DIMM_DQ[31]
DDR_PDQ30		158	DDR2_DIMM_DQ[30]
DDR_PDQ29		153	DDR2_DIMM_DQ[29]
DDR_PDQ28		152	DDR2_DIMM_DQ[28]
DDR_PDQ27		40	DDR2_DIMM_DQ[27]
DDR_PDQ26		39	DDR2_DIMM_DQ[26]
DDR_PDQ25		34	DDR2_DIMM_DQ[25]
DDR_PDQ24		33	DDR2_DIMM_DQ[24]
DDR_PDQ23		150	DDR2_DIMM_DQ[23]
DDR_PDQ22		149	DDR2_DIMM_DQ[22]
DDR_PDQ21		144	DDR2_DIMM_DQ[21]
DDR_PDQ20		143	DDR2_DIMM_DQ[20]
DDR_PDQ19		31	DDR2_DIMM_DQ[19]
DDR_PDQ18		30	DDR2_DIMM_DQ[18]
DDR_PDQ17		25	DDR2_DIMM_DQ[17]
DDR_PDQ16		24	DDR2_DIMM_DQ[16]
DDR_PDQ15		141	DDR2_DIMM_DQ[15]
DDR_PDQ14		140	DDR2_DIMM_DQ[14]
DDR_PDQ13		132	DDR2_DIMM_DQ[13]
DDR_PDQ12		131	DDR2_DIMM_DQ[12]
DDR_PDQ11		22	DDR2_DIMM_DQ[11]
DDR_PDQ10		21	DDR2_DIMM_DQ[10]
DDR_PDQ9		13	DDR2_DIMM_DQ[9]
DDR_PDQ8		12	DDR2_DIMM_DQ[8]
DDR_PDQ7		129	DDR2_DIMM_DQ[7]
DDR_PDQ6		128	DDR2_DIMM_DQ[6]
DDR_PDQ5		123	DDR2_DIMM_DQ[5]
DDR_PDQ4		122	DDR2_DIMM_DQ[4]
DDR_PDQ3		10	DDR2_DIMM_DQ[3]
DDR_PDQ2		9	DDR2_DIMM_DQ[2]
DDR_PDQ1		4	DDR2_DIMM_DQ[1]
DDR_PDQ0		3	DDR2_DIMM_DQ[0]
		101	DDR2_DIMM_SA2
		240	DDR2_DIMM_SA1
		239	DDR2_DIMM_SA0
		120	DDR2_DIMM_SCL
		119	DDR2_DIMM_SDA

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1V8

R228 4K7

R227 4K7

PPC_DDR2_DIMM_SCL

PPC_DDR2_DIMM_SDA

GND

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA1	22-8L,22-9D
DDR2_DIMM_BA[1]	190	DDR_PBA2	22-8L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-8L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	NC	
DDR2_DIMM_CK_N[2]	221	NC	
DDR2_DIMM_CK_P[1]	137	NC	
DDR2_DIMM_CK_N[1]	138	NC	
DDR2_DIMM_CK_P[0]	185	DDR_CLKOUT	
DDR2_DIMM_CK_N[0]	186	DDR_CLKOUT#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-7L,22-8D
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-9D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D
ERR_OUT	55	PPC_DDR2_ERROR	
PAR_IN	68	PAR_IN	

R226 49R9 4K7

PPC_DDR2_RESET_N

1-3B,1-4L,24-5J

C455 5PF 50V

TP4

TP5

GND

VTT DDR

DDR_PA15 DDR_PA14 DDR_PA13 DDR_PA12 — RP24

DDR_PA11 DDR_PA10 DDR_PA9 DDR_PA8 — RP23

DDR_PA7 DDR_PA6 DDR_PA5 DDR_PA4 — RP22

DDR_PA3 DDR_PA2 DDR_PA1 DDR_PA0 — RP21

CP26 CP28 CP29 CP30

GND

22-8K,22-9D DDR_PBA1

22-8K,22-9D DDR_PBA2

22-8K,22-9D DDR_PBA0

22-8K,22-9D DDR_PCAS#

22-7K,22-9D DDR_PRAS#

22-6K,22-8D DDR_PCKE

22-3K,22-8D DDR_PWE#

22-3K,22-8D DDR_PCS0#

22-3K,22-8D DDR_PCS1#

22-8D DDR_PODT0

22-8D DDR_PODT1

NC

RP25 RP26 RP19

CP32 CP31 CP33

GND

J8

VREF	1	237	VSS_64
VDDSPD	238	234	VSS_63
VDD_11	197	231	VSS_62
VDD_10	189	228	VSS_61
VDD_9	187	225	VSS_60
VDD_8	184	222	VSS_59
VDD_7	178	219	VSS_58
VDD_6	172	216	VSS_57
VDD_5	69	213	VSS_56
VDD_4	67	210	VSS_55
VDD_3	64	207	VSS_54
VDD_2	59	204	VSS_53
VDD_1	53	201	VSS_52
VDDQ_11	194	198	VSS_51
VDDQ_10	191	169	VSS_50
VDDQ_9	181	166	VSS_49
VDDQ_8	175	163	VSS_48
VDDQ_7	170	160	VSS_47
VDDQ_6	78	157	VSS_46
VDDQ_5	75	154	VSS_45
VDDQ_4	72	151	VSS_44
VDDQ_3	62	148	VSS_43
VDDQ_2	56	145	VSS_42
VDDQ_1	51	142	VSS_41
		139	VSS_40
		136	VSS_39
		133	VSS_38
		130	VSS_37
		127	VSS_36
		124	VSS_35
		121	VSS_34
		118	VSS_33
		115	VSS_32
		112	VSS_31
		109	VSS_30
		106	VSS_29
		103	VSS_28
		100	VSS_27
		97	VSS_26
		94	VSS_25
		91	VSS_24
		88	VSS_23
		85	VSS_22
		82	VSS_21
		79	VSS_20
		66	VSS_19
		65	VSS_18
		50	VSS_17
		47	VSS_16
		44	VSS_15
		41	VSS_14
		38	VSS_13
		35	VSS_12
		32	VSS_11
		29	VSS_10
		26	VSS_9
		23	VSS_8
		20	VSS_7
		17	VSS_6
		14	VSS_5
		11	VSS_4
		8	VSS_3
		5	VSS_2
		2	VSS_1

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GND

DDR_VREF_0V9 1V8 1V8 1V8

C432 C433 C454 C434 C430 C443 C431 C444 C436 C445 C435 C446 100NF 10V 10NF 25V

GND

1V8 1V8 1V8

C438 C451 C437 C452 C439 C449 C440 C450 C441 C448 C442 C447 100NF 10V 10NF 25V

GND

PLACE NEAREST DDR2 MODULE PINS

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

ROACH/iBOB2	ROACH_PPC_DDR2
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_16:36	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 22 OF 25

PWR_GOOD
1-4G,1-4G,1-5E,1-5G,17-3F,18-2F,24-8K

3V3

PWR_GOOD monitors the +1.0v, 1V5, 1V8, 2V5, and 3V3 supplies

D1 BAV70

R41 10K

R42 100

C47 2.2UF

SPST SW1

U31 MIC2779R-29

R28 2.2K

R29 3.3K

RESET_PORW 6,11
1-29,1-3G,1-5L,24-8C,25-5G

GND

C604 0.1UF

RESET_PB_POR#
1-4L,1-5G,24-8C

IRQ0-9 have programmable polarity per section 10.5.7 (UIC0_PR) 440ep user manual

R31 3.3K

R32 2.2K

R33 3.3K

R35 3.3K

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_3V3_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz

U9 CY22381FX_8211

C48 18PF

C49 18PF

22.1184MHZ

Y1

R30 2.2K

R51 33

R52 33

R53 33

C605 0.1UF

SEL_SYSCLK
1-3L,1-5G,24-7C

CLK_UART_11.0592MHZ
1-2L,1-4L,25-3B

CLK_SYS_33MHZ

CLK_CPLD_33MHZ
1-3G,1-4L,24-7C

U1 440EPX

SYSTEM INTERRUPTS

RESET_PORW

CLK_TMRCLK
1-3L,1-5G,24-7C

SYSERR
1-3G,1-5L,24-7C

R24 1K

TEST POINT

R25 1K

PPC440EPX-NTA533T

GETH0_INT#
1-4E,1-5G,20-4E

MONITOR_INT
1-5G,1-9E,2-1P

PCI_INTA#
1-4E,1-5G,19-4E,19-4G

STTM_ALERT
1-2L,1-5G,25-2B

GPIO44
1-5L

SX95T_TDI
1-5L,1-7C,16-2L

SX95T_TCK
1-5L,1-7C,16-2L

SX95T_TMS
1-5L,1-7C,16-2L

SX95T_TDO
1-5G,1-7G,16-2L

R01 1K

R02 1K

R03 1K

R04 1K

R05 1K

R23 1K

NO POP
RO1 - RO5

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible

U24 CY22392FX_8211

CS1 18PF

CS2 18PF

12.00 MHZ

Y2

R34 2.2K

R54 33

R55 33

R57 33

R59 33

R510 33

CLK_PCI1_66/33MHZ
1-4B,1-5L,19-3C

CLK_PCI2_66/33MHZ
1-4B,1-5L,19-4B

CLK_GETH0_25MHZ
1-4B,1-5L,20-4B

CLK_USB2.0_48MHZ
1-3B,1-5L,21-2C

CLK_CPLD_50MHZ
1-3G,1-5L,24-7C

CLK_SEL_M66EN
1-3L,1-5G,24-7C

C607 0.1UF

C695 0.1UF

TRACE & JTAG CONNECTORS

P1 .12X H SMT

R37 10K

R38 10K

R39 10K

R49 10K

23-2G CPU_TDO
CPU_TDI
CPU_TCK
CPU_TMS
CPU_HALT#
DEBUG_TRST#

R36 10K

VCC_JTAG

R29 33

C53 0.1UF

R26 is for current limiting and should be <100 Ohms.

Critical placement and routing of the Trace connector and nets. Up to CPU frequency/4

U1 440EPX

RISEWatch JTAG

R27 2.2K

C54 0.1UF

R12

R14

R15

R22

CPU_TRST#
1-3L,1-5G,24-7C

DEBUG_TRST#
1-3G,1-5L,24-7C

TRACE PORT

J1 JSCN F SMT

R18

R11

R13

R16

R17

R19

R20

R21

TMC-CLK 23-2E

VCC_JTAG

TRCES4 23-2E
TRCTS0 23-2E
TRCTS1 23-2E
TRCTS2 23-1E
TRCTS3 23-1E
TRCTS4 23-1E
TRCTS5 23-1E
TRCTS6 23-1E

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

10-5-2007_16:36

PATH PATH

ROACH_PPC_TST_CLK_IO

DOC NO NRF-ADM-XXX-SD-0001

REVISION A

DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 23 OF 25

ROACH/iBOB2	ROACH_PPC_CPLD
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_16:36	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 24 OF 25

PDATA[0:31]
1-1L,1-4L

PADDE2cG2
1-1L,1-36,24-10B,25-10B,25-10M

PADD[2:31]

3V3

External Slave Peripheral

U1
AXEEPX

NC
PERDATA31
PERDATA30
PERDATA29
PERDATA28
PERDATA27
PERDATA26
PERDATA25
PERDATA24
PERDATA23
PERDATA22
PERDATA21
PERDATA20
PERDATA19
PERDATA18
PERDATA17
PERDATA16

PDATA15 C16 PERDATA15
PDATA14 B16 PERDATA14
PDATA13 A16 PERDATA13
PDATA12 B15 PERDATA12
PDATA11 C15 PERDATA11
PDATA10 B11 PERDATA10
PDATA9 D14 PERDATA9
PDATA8 A15 PERDATA8
PDATA7 C14 PERDATA7
PDATA6 A14 PERDATA6
PDATA5 D13 PERDATA5
PDATA4 C13 PERDATA4
PDATA3 B13 PERDATA3
PDATA2 A13 PERDATA2
PDATA1 B14 PERDATA1
PDATA0 C14 PERDATA0

PERADDR31 R10 PA0031
PERADDR30 A10 PA0030
PERADDR29 B10 PA0029
PERADDR28 A9 PA0028
PERADDR27 B9 PA0027
PERADDR26 C9 PA0026
PERADDR25 B8 PA0025
PERADDR24 C8 PA0024
PERADDR23 A8 PA0023
PERADDR22 B7 PA0022
PERADDR21 A7 PA0021
PERADDR20 B6 PA0020
PERADDR19 A6 PA0019
PERADDR18 B5 PA0018
PERADDR17 C5 PA0017
PERADDR16 D5 PA0016
PERADDR15 A5 PA0015
PERADDR14 A4 PA0014
PERADDR13 B4 PA0013
PERADDR12 C4 PA0012
PERADDR11 D4 PA0011
PERADDR10 B3 PA0010
PERADDR9 C3 PA009
PERADDR8 A3 PA008
PERADDR7 B2 PA007
PERADDR6 C2 PA006
PERADDR5 D3 PA005
PERADDR4 A2 PA004
PERADDR3 A1 PA003
PERADDR2 C1 PA002

25-5G,25-10B PCS_0 B16
25-7M,25-10B PCS_1 B6
PCS_2 B5
PERCS0# A12
25-9B PCS_3_GPIO09 A6
25-9B PCS_5_GPIO010 A4
PERCS4#_GPIO09
PERCS5#_GPIO10
POE# PERRDE# B14
PERWR_WP A16
PWBE_0# PERWBE0# A15
PWBE_1# PERWBE1# C15
PWBE_2# PERWBE2# D15
PWBE_3# PERWBE3# B15
25-9Q,25-9B PREADY C17
25-6M,25-8B PBLAST# B7
PERWBE_GPIO11

PERADDR07_GPIO08_SMARQ3
PERADDR06_GPIO01_SMAACK2
PERADDR05_GPIO02_EOT2_TC2
GPIO03_PERADDR04_SMARQ2
GPIO04_PERADDR03_SMAACK3
GPIO05_PERADDR02_EOT3_TC3

EXTRESET2 B6
PERCLK A7 CLK_PERCLK
PERERR_GPIO11 C7 PERERR

25-8Q

NO POP
R84 1K
R83 1K
R86 4.99K, 1%
R87 4.99K, 1%
R88 4.99K, 1%
3V3
R85 1K
J7
0.1UF W SMT
EXT_RESET#
1-1L,1-3D,24-5J
CLK_PERCLK
1-2L,1-3G,24-7C

External Master Peripheral Interface

CLK_UART_11.0592MHZ
1-2D,1-4L,23-7G
A27

UART

UARTSERCLK

UART1_TX_UART0_TX D27 UART1_TX
UART1_RX_UART0_RX C27 UART1_RX
UART1_RTS#_UART0_RTS# B29
UART1_CTS#_UART0_CTS# A29
UART2_TX_UART0_DTR# D28 UART2_TX
UART2_RX_UART0_RI# B28 UART2_RX
UART2_RTS#_UART0_DSR# C29 CPU_UART0_DSR#
UART2_CTS#_UART0_DCD# C28 CPU_UART0_DCD#

IIC0

IIC0SCLK AB32
IIC0SDATA AB33

IIC1_SPI

SCPCLKOUT_IIC1SCLK AC34
SCPDI_IIC1SDATA AC32
SCPDO AB31

NAND Flash Interface

NOT USED

NFALE R17 NC
NFCLE R18 NC
NFREN# R17 NC
NFWEN# R18 NC
NFRDYBUSY# A17
NFCE3#_PERCS3# D6

R77 3.3K
R78 3.3K

FLASH 32Mx16 (64MB)

U42
32MX16 HIGHROW BIT

PA0030 E2 A0
PA0029 D2 A1
PA0028 C2 A2
PA0027 A2 A3
PA0026 B2 A4
PA0025 B1 A5
PA0024 C1 A6
PA0023 A1 A7
PA0022 B6 A8
PA0021 A3 A9
PA0020 C6 A10
PA0019 B5 A11
PA0018 B7 A12
PA0017 A7 A13
PA0016 C7 A14
PA0015 B3 A15
PA0014 E1 A16
PA0013 G3 A17
PA0012 C3 A18
PA0011 D5 A19
PA0010 D6 A20
PA009 C5 A21_64MB
A22_128MB
A23_256MB
A24_512MB
A25_1GB

WP#/ACC E4 R4
DQ0 E3 PDATA15
DQ1 H3 PDATA14
DQ2 E4 PDATA13
DQ3 H4 PDATA12
DQ4 H5 PDATA11
DQ5 E5 PDATA10
DQ6 H6 PDATA9
DQ7 E6 PDATA8
DQ8 F3 PDATA7
DQ9 G3 PDATA6
DQ10 F4 PDATA5
DQ11 G4 PDATA4
DQ12 F5 PDATA3
DQ13 G5 PDATA2
DQ14 F6 PDATA1
DQ15/A-1 G7 PDATA0

RY/BSY A4
NC1 A5
NC2 A6
NC3 B1
NC4 C4
NC5 D1
NC6 E1
NC7 G1
NC8 H1
NC11 H6

BYTE# F7
CE# F2
OE# G2
WE# A5
RESET# B5

VSS1 F1
VSS2 G6
VSS3 H2

R80 3.3K
PWPU
1-2G,1-3L,24-6C
R81 3.3K
RY_BY#
1-2L,1-3G,24-6C
R82 3.3K
RESET_CPLD#
1-1G,1-3L,24-5C
BOOT_CFG2
1-1G,1-3L,24-9M
BOOT_CFG1
1-1G,1-3L,24-9M
BOOT_CFG0
1-2G,1-3L,24-9M

C654 0.1UF 0402
C656 0.1UF 0402
C659 0.1UF 0402
C652 0.1UF 0402
C658 0.1UF 0402
C660 0.1UF 0402

U40 P15A3157 SHB BD TO A
U45 P15A3157 SHB BD TO A
U46 P15A3157 SHB BD TO A

UART1_TX
UART1_RX
PERPARB_UART1_RTS#
PERPARB_UART1_CTS#
UART1_CTS#
UART2_TX
UART2_RX
UART2_RTS#
UART2_CTS#

U44 ICL3225ECA
U43 ICL3225ECA

C192 0.1UF 0402
C194 0.1UF 0402
C193 0.1UF 0402
C195 0.1UF 0402
C196 0.1UF 0402
C198 0.1UF 0402
C197 0.1UF 0402
C199 0.1UF 0402

C2P C1P C2N C1N VCC V+ V- T1IN T2IN R1OUT R2OUT FORCEOFF FORCEON INVALID READY GND

X_UART1_TX X_UART1_RX X_UART1_RTS# X_UART1_CTS#
X_UART2_TX X_UART2_RX X_UART2_RTS# X_UART2_CTS#

R85 10K
R87 10K

C649 0.1UF 0402
C653 0.1UF 0402

5V_VIN
CTRL
P2 9P DSUB MALE
UART Port 0

J14
UART Port 1
HLE-105-02-G-DV

NC P1
P2
P3
P4
P5
NC P6
P7
P8
NC P9
NC P10

PERIPHERAL

PER_D[31] AE12 PER_A[30]
PER_D[30] AF23 PER_A[29]
PER_D[29] AG23 PER_A[28]
PER_D[28] AF13 PER_A[27]
PER_D[27] AG12 PER_A[26]
PER_D[26] AE22 PER_A[25]
PER_D[25] AE23 PER_A[24]
PER_D[24] AG20 PER_A[23]
PER_D[23] AH15 PER_A[22]
PER_D[22] AG15 PER_A[21]
PER_D[21] AG18 PER_A[20]
PER_D[20] AF19 PER_A[19]
PER_D[19] AH17 PER_A[18]
PER_D[18] AG16 PER_A[17]
PER_D[17] L21 PER_SP_A[16]
PER_D[16] L20 PER_SP_A[15]
L15 PER_SP_A[14]
L16 PER_SP_A[13]
J22 PER_SP_A[12]
K21 PER_SP_A[11]
K16 PER_SP_A[10]
J15 PER_SP_A[9]
G22 PER_SP_A[8]
H22 PER_SP_A[7]
L14 PER_SP_A[6]
K14 PER_SP_A[5]
K23 PER_SP_A[4]
K22 PER_SP_A[3]
J12 PER_SP_A[2]

PCS_1 AE14 PER_CS0
POE# AF21 PER_OE_N
PR_W# AF20 PER_R_W_N
PWBE_1# AF18 PER_WBE[1]
PWBE_0# AF14 PER_WBE[0]
PBLAST# AE18 PER_B_LAST

U15
BANKS=1, 2, 4
CHIP SELECT 1

PER_D[15] AF15
PER_D[14] AE16
PER_D[13] AE21
PER_D[12] AD20
PER_D[11] AF16
PER_D[10] AE17
PER_D[9] AE19
PER_D[8] AD19
PER_D[7] AG22
PER_D[6] AH22
PER_D[5] AH12
PER_D[4] AG13
PER_D[3] AH20
PER_D[2] AH19
PER_D[1] AH14
PER_D[0] AH13

PER_D_PAR[1] AG21 NC
PER_D_PAR[0] AE13 NC

PER_ERR AG17 PERERR
PER_READY AH18 PREADY

C334 470F 6V
C335 470F 6V
C330 220NF 0.3V
C331 220NF 0.3V
C332 220NF 0.3V
C333 220NF 0.3V

GND

I2C

I2C0_SCLK
1-2L,1-9B,2-2P
I2C0_33_DATA
1-2L,1-9E

A7440B8 U39
EE2_BOOT_WP
1-2G,1-3L,24-6C
R89 15K

A7440B8 U38
R90 15K

A7440B8 U41
EE1_WP
1-2G,1-3L,24-6C
R91 15K

MGGEN
1-2G,1-3G,1-4E,19-2D,24-10L

P11 0.12K H SMT
C661 0.1UF 0402
R73 3.3K
R74 3.3K

STTM_ALERT
1-2L,1-9G,23-6N
U41 AD7414-0

P4 0.12K H SMT
R75 3.3K
R76 3.3K

STTM_AS
1-2G,1-3L,24-6C

SCPCLK
1-2L
SCPDI
1-2L
SCPDO
1-2L

NO POP
R69
U47 P15A3157 SHB BD TO A
I2C0_33_DATA
I2C0_66_DATA
I2C0_SDATA

PCS_0 25-8C,25-10B
PDRY 1-2L,1-3G,24-8C,25-7B,25-7M,25-9B
PR_WP 1-1L,1-3G,24-8C,25-6M,25-7B,25-9B
RESET_PORb 1-2G,1-3G,1-5L,23-9J,24-8C

ROACH/iBOB2	ROACH_PPC_NVM_SERIAL
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_16:36	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 25 OF 25