VIRTEX5

POWER SUPPLY AND MONITORING

ROACH_MONITOR

1-5I,2-2P,25-5A	I2C0_SCLK	I2C0_SCLK	
1-8E,2-2M,3-10B	FAN2_SENSE	FAN2_SENSE	
1-8E,2-2M,3-10B	FAN1_SENSE	FAN1_SENSE	
1-8E,2-1M,3-9B	FAN3_SENSE	FAN3_SENSE	
1-8E,2-3A,3-6C	3V3_ATX	3V3_ATX	
1-8E,2-2B,3-2H	I2V5	I2V5	
1-8E,2-2B,3-2R	I1V8	I1V8	
1-8E,2-2B,3-5R	I1V5	I1V5	
1-8E,2-1B,3-10R	I1V0	I1V0	
1-8E,2-4A,3-7C	5V_ATX	5V_ATX	
1-9Q,2-B0,19-7P	MGT_AVCC_PG	MGT_AVCC_PG	
1-9Q,2-B0,19-4G	MGT_AVTTX_PG	MGT_AVTTX_PG	
1-9Q,2-B0,19-7G	MGT_AVCCPLL_PG	MGT_AVCCPLL_PG	
1-8E,2-1B,3-7C	PWR_OK	PWR_OK	
1-8E,2-6B,3-6C	12V_ATX	12V_ATX	
		2	

		PPC_RESET	1-2G,2-2R,24-6C
		SYS_CONFIG[0:7]	1-2G,2-2R,24-6B
		TDZ	1-3L,2-6L,23-6H
		ATRTN1	1-3L,2-4L,23-6H
		MONITOR_INT	1-3H,2-1P,23-7M
		I2C0_33_DATA	1-5L
		PS_ONB	1-8B,2-8B,3-8G
		ATRTN0	
		TD0	
1-9E,2-6B,3-5B	LOAD_RES_OFF	FAN1_CONTROL	1-8B,2-3M,3-10B
1-9E,2-3M,3-10B	FAN1_CONTROL	LOAD_RES_OFF	1-8B,2-6B,3-5B
1-9E,2-B0,3-6G	PS_ONB	2V5_TRACK	1-8B,2-6B,3-3B
1-9E,2-2M,3-9B	FAN2_CONTROL	2V5_INHIBIT	1-8B,2-1B,3-1B
1-9E,2-2M,3-9B	FAN3_CONTROL	FAN3_CONTROL	1-8B,2-2M,3-9B
		FAN2_CONTROL	1-8B,2-2M,3-10B
		MGT_AVTTX_EN	1-8L,2-1M,10-5B
		MGT_AVCCPLL_EN	1-9L,2-1M,10-8B
		MGT_AVCC_EN	1-9L,2-1M,10-8K
		1V8_INHIBIT	1-8B,2-1B,3-1J
		1V5_INHIBIT	1-8B,2-1B,3-4J
1-8E,2-0B,3-9J	1V0_INHIBIT	1V0_INHIBIT	1-8B,2-0B,3-9J
		3	

ROACH_PSU

1-8E,2-0B,3-9J	1V0_INHIBIT	12V_ATX	1-8B,2-6B,3-6C
1-8E,2-1B,3-4J	1V5_INHIBIT	3V3_ATX	1-9B,2-3A,3-6C
1-8E,2-1B,3-1J	1V8_INHIBIT	5V_ATX	1-9B,2-4A,3-7C
1-8E,2-6B,3-3B	2V5_TRACK	PWR_OK	1-8B,2-8B,3-7C
1-8E,2-6B,3-2H	2V5_INHIBIT	FAN1_SENSE	1-9B,2-2M,3-10B
		FAN2_SENSE	1-9B,2-2M,3-10B
		FAN3_SENSE	1-9B,2-1M,3-9B
		I1V0	1-9B,2-1B,3-10R
		I1V5	1-9B,2-2B,3-5R
		I1V8	1-9B,2-2B,3-2R
		I2V5	1-9B,2-2B,3-2H

VIRTEX5 CLOCKS

ROACH_V5_CLK

SX95T_DXN	ATRTN0	
SX95T_DXP	TD0	
7		

ZDOK/ADC INTERFACE

ROACH_ADC_0

5

ROACH_ADC_1

6

V5 DDR2 MEMORY

ROACH_DDR2_DIMM

11

V5 DIFFERENTIAL GPIO

ROACH_DIFF_GPIO

12

V5 SE GPIO & MISCELLANEOUS

ROACH_GPIO_MISC

13

GIGABIT TRANSCEIVERS

ROACH_TRANSCEIVERS0_1

8

ROACH_TRANSCEIVERS2_3

9

1-9E,2-1M,10-8K	MGT_AVCC_EN	MGT_AVCC_EN	
1-9E,2-1M,10-8B	MGT_AVCCPLL_EN	MGT_AVCCPLL_EN	
1-9E,2-1M,10-5B	MGT_AVTTX_EN	MGT_AVTTX_EN	
		MGT_AVCC_PG	MGT_AVCC_PG
		MGT_AVTTX_PG	MGT_AVTTX_PG
		MGT_AVCCPLL_PG	MGT_AVCCPLL_PG

ROACH_TRANSCEIVERS_PSU

10

QDRII+ MEMORY

ROACH_QDR2P_BY0_1

14-5F	QDR2_TDI	QDR2_TDI	
	QDR2_TCK	QDR2_TCK	
	QDR2_TMS	QDR2_TMS	
		QDR2_BY0_1_TDO	QDR2_BY0_1_TDO

14

ROACH_QDR2P_BY2_3

QDR2_BY0_1_TDO	QDR2_BY0_1_TDO		
	QDR2_TMS	QDR2_TMS	
	QDR2_TCK	QDR2_TCK	
		QDR2_BY2_3_TDO	QDR2_BY2_3_TDO
			15-5H

15

V5 POWER

ROACH_5V_POWER

4

VIRTEX5 CONFIGURATION

ROACH_CONFIG

1-1M,16-4B,24-7C	SX95T_D_IN_0	SX95T_D_IN_0	
1-3L,16-2L,23-6H	SX95T_TCK	SX95T_TCK	
1-3L,16-2L,23-6N	SX95T_TMS	SX95T_TMS	
1-3L,16-2L,23-6R	SX95T_TDI	SX95T_TDI	
1-1M,16-3B,24-8C	SX95T_RDWR_B_0	SX95T_RDWR_B_0	
1-1M,1-3F,16-3B,21-4D,24-10C	SX95T_PROGRAM_B_0	SX95T_PROGRAM_B_0	
1-1M,16-4B,24-6C	SX95T_CS_B_0	SX95T_CS_B_0	
		SX95T_M2_0	SX95T_M2_0
		SX95T_M1_0	SX95T_M1_0
		SX95T_M0_0	SX95T_M0_0
		SX95T_DONE_0	SX95T_DONE_0
		SX95T_CCLK_0	SX95T_CCLK_0
		SX95T_D_OUT_BUSY_0	SX95T_D_OUT_BUSY_0
		SX95T_INIT_B_0	SX95T_INIT_B_0
		SX95T_TDO	SX95T_TDO

16

PPC

ROACH_PPC_POWER_1

17

ROACH_PPC_POWER_2

18

ROACH_PPC_PCI

19

ROACH_PPC_ETH1

1-2M,20-4E,24-10F	GETH0_RST#	GETH0_RST#	
1-3L,20-4E,23-5G	CLK_GETH0_25MHZ	CLK_GETH0_25MHZ	
		GMCMDIO	20-3C,20-4D
		GMCMDCLK	20-3C,20-4D
		GETH0_INT#	1-3H,20-4E,23-7N

20

ROACH_PPC_USB

CONTAINS GPIO TO CONFIG INTERFACE

		SX95T_D_OUT_BUSY_0	1-1G,1-7G,16-4B,21-5D,24-7C
SX95T_DONE_0	SX95T_DONE_0	SX95T_INIT_B_0	1-1M,1-7G,21-5D
SX95T_INIT_B_0	SX95T_INIT_B_0	SX95T_M0_0	1-1M,1-7G,21-4D,24-9F
SX95T_M0_0	SX95T_M0_0	SX95T_M1_0	1-1G,1-7G,16-3B,21-4D,24-7F
SX95T_M1_0	SX95T_M1_0	SX95T_M2_0	1-1G,1-7G,16-3B,21-4D,24-7F
SX95T_M2_0	SX95T_M2_0	SX95T_PROGRAM_B_0	1-1G,1-7G,16-3B,21-4D,24-7F
SX95T_PROGRAM_B_0	SX95T_PROGRAM_B_0		1-1M,1-7C,16-3B,21-4D,24-10C
1-3L,21-2C,23-4G	CLK_USB2_48MHZ		
	CLK_USB2_48MHZ		

21

ROACH_PPC_DDR2

1-2M,22-3K,24-10F	PPC_DDR2_RESET_N	PPC_DDR2_RESET_N

22

ROACH_PPC_NVM_SERIAL

1-3L,23-7G,25-3D	CLK_UART_11_0592MHZ	CLK_UART_11_0592MHZ	
1-1G,24-5N,25-3B	M66EN	M66EN	
1-3M,24-7C,25-3A	EE1_WP	EE1_WP	
1-2M,24-7C,25-1B	STTM_AS	STTM_AS	
1-2G,1-3L,23-5J,24-5M,25-5G	PDE#	PDE#	
1-1M,24-7C,25-8J	FWP#	FWP#	
1-2M,24-7C,25-5A	EE2_BOOT_WP	EE2_BOOT_WP	
1-1M,24-11M,25-1J	BOOT_CFG0	BOOT_CFG0	
1-1M,24-11M,25-1J	BOOT_CFG1	BOOT_CFG1	
1-1M,24-10M,25-1J	BOOT_CFG2	BOOT_CFG2	
1-1M,24-5C,25-3J	RESET_CPLD#	RESET_CPLD#	

25

		VS_INT#	1-3H,23-7N,25-8Q
		SELECTMAP_CS	1-2G,24-6C,25-7B
		I2C0_SCLK	1-9B,2-2P,25-5A
		I2C0_33_DATA	1-5E
		SCPDI	
		SCPCLK	25-1B
		STTM_ALERT	1-3H,23-6M,25-2B
		SCPDO	25-6B
		PDE#	1-1G,24-8C,25-5G,25-7B,25-7M,25-10B
		FRY_BY#	1-1G,24-7C,25-7J
		CLK_PERCLK	1-1G,24-4C,24-8B,25-6F
		PWBE_0#	1-2G,24-9C,25-6M,25-7B,25-9B
		PR_WP	1-1G,24-10C,25-5G,25-8M,25-7B,25-9B
		PCS_2	1-1G,24-10C,25-7B
		PDATA[4:31]	1-2M
		PADD[2:31]	1-2G,24-9B,25-10B
		EXT_RESET#	1-2G,24-10C,25-6F

ROACH_PPC_TST_CLK_IO

		PPC_THERMONA	1-9E,2-6L,23-6H
		PPC_THERMONB	1-9E,2-6L,23-6H
		GPIO44	23-6N
		SX95T_TDI	1-7C,16-2L,23-6N
		SX95T_TCK	1-7C,16-2L,23-6M
		SX95T_TMS	1-7C,16-2L,23-6N
		RESET_POR#	1-2G,1-5G,23-5J,24-5M,25-5G
		DEBUG_TRST#	1-1G,23-1F,24-9C
1-4E,20-4E,23-7N	GETH0_INT#	CLK_GETH0_25MHZ	
1-9E,2-1F,23-7M	MONITOR_INT	CLK_USB2_48MHZ	1-3B,21-2C,23-4G
1-5L,23-7M,25-8Q	VS_INT#	CLK_CPLD_50MHZ	1-1G,23-4G,24-7C
1-5L,23-6M,25-2B	STTM_ALERT		
1-7G,16-2L,23-6M	SX95T_TDO	SYSERR	1-1G,23-6M,24-10C
1-2M,23-8E,24-7F	RESET_PB_POR#	CLK_UART_11_0592MHZ	1-5G,23-7G,25-3D
1-2G,23-1BG,24-8R	PWR_GOOD	CLK_CPLD_33MHZ	1-1G,23-6G,24-8C
1-2M,23-2F,24-9C	CPU_TRST#		
1-1M,23-5D,24-10F	CLK_SEL_M66EN		
1-1M,23-7G,24-10F	SEL_SYSCLK		
1-1M,23-6B,24-10C	CLK_TMRCLK		

23

ROACH_PPC_CPLD

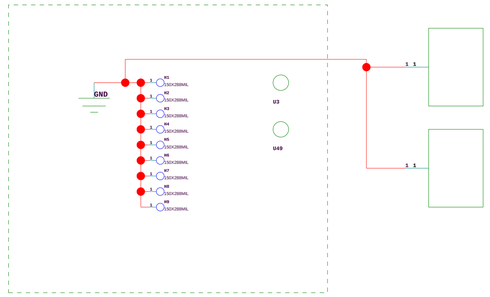
1-9E,2-2B,24-6B	SYS_CONFIG[0:7]	GETH0_RST#	1-4B,20-4E,24-10F
		PPC_DDR2_RESET_N	1-2B,22-3K,24-10F
1-9E,2-2B,24-6C	PPC_RESET	PDATA[0:7]	1-4L
1-3H,23-10G,24-8R	PWR_GOOD	RESET_PB_POR#	1-3H,23-8E,24-7F
1-4L,24-10C,25-8P	EXT_RESET#	SX95T_CCLK_0	1-7G,24-4F,24-7C
1-3L,1-5G,23-9J,24-5M,25-5G	RESET_POR#	STTM_AS	1-5G,24-7C,25-1B
1-4L,24-9C,25-6M,25-7B,25-9B	PWBE_0#	EE2_BOOT_WP	1-4G,24-7C,25-5A
1-4L,24-9B,25-10B	PADD[2:31]	EE1_WP	1-5G,24-7C,25-3A
1-5L,24-8C,25-7B	SELECTMAP_CS	CPU_TRST#	1-3H,23-2F,24-9C
1-4L,24-7C,25-7J	FRY_BY#	SEL_SYSCLK	1-3H,23-7G,24-10F
1-3L,23-6H,24-10C	SYSERR	CLK_SEL_M66EN	1-3H,23-5D,24-10F
1-2L,23-6G,24-7C	CLK_CPLD_33MHZ	CLK_TMRCLK	1-3H,23-6B,24-10C
1-3L,23-1F,24-9C	DEBUG_TRST#	SX95T_RDWR_B_0	1-7C,16-3B,24-8C
1-4L,24-4C,24-8B,25-6F	CLK_PERCLK	FWP#	1-4G,24-7C,25-8J
1-3L,23-4G,24-7C	CLK_CPLD_50MHZ	RESET_CPLD#	1-4G,24-5C,25-3J
1-4L,24-10C,25-5G,25-8M,25-7B,25-9B	PR_WP		
1-5L,24-8C,25-5G,25-7B,25-7M,25-10B	PDE#	SX95T_INIT_B_0	1-3F,1-7G,21-4D,24-9F
1-4L,24-10C,25-7B	PCS_2	SX95T_DONE_0	1-3F,1-7G,21-5D
1-3F,1-7G,16-4B,21-5D,24-7C	SX95T_D_OUT_BUSY_0	SX95T_PROGRAM_B_0	1-3F,1-7C,16-3B,21-4D,24-10C
1-5G,24-5B,25-3B	M66EN	SX95T_D_IN_0	1-7C,16-4B,24-7C
1-3F,1-7G,16-3B,21-4D,24-7F	SX95T_M2_0	SX95T_CS_B_0	1-6C,16-4B,24-6C
1-3F,1-7G,16-3B,21-4D,24-7F	SX95T_M1_0	BOOT_CFG0	1-4G,24-11M,25-1J
1-3F,1-7G,16-3B,21-4D,24-7F	SX95T_M0_0	BOOT_CFG1	1-4G,24-11M,25-1J
		BOOT_CFG2	1-4G,24-10M,25-1J

24

ROACH_PPC_ERR_LED

26

MECHANICAL



PLACEHOLDER FOR PCB
MEERKAT LOGO

PLACEHOLDER FOR PCB
CASPER LOGO

PLACEHOLDER FOR PCB
NRAO LOGO

BOARD SERIAL NUMBER

CONTRIBUTORS

ETIENNE BAUERMEISTER
HENRY CHEN
STEVE DURAND
FRANCOIS KAPP
ALAN LANDMAN
GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

2-29-2008_11:08

PATH PATH

ROACH_TOP

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	1 OF 25

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

TIE TO GROUND IF PLL'S ARE NOT USED

PLACE AT ACTEL 3V3 POWER PINS

PLACE AT ACTEL 1V5 POWER PINS

roach_AFS600_powerpins

roach_AFS600_pcb

roach_AFS600_configpins

XPORT - PLACE IN REAR I/O REGION
XP1001001-03R

TEMPERATURE DIODE HEADER

ACTEL JTAG CONNECTOR

PB POWER SWITCH

KEY - REMOVE PIN

MONITOR RESET

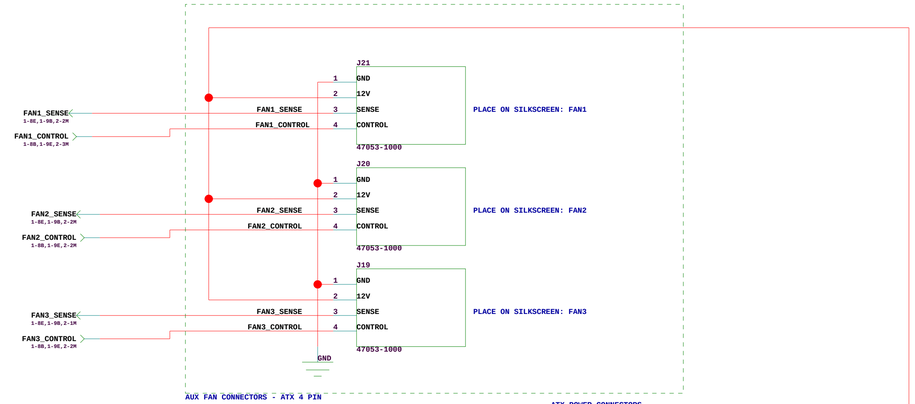
REFERENCE RESISTOR/ADC VALUES

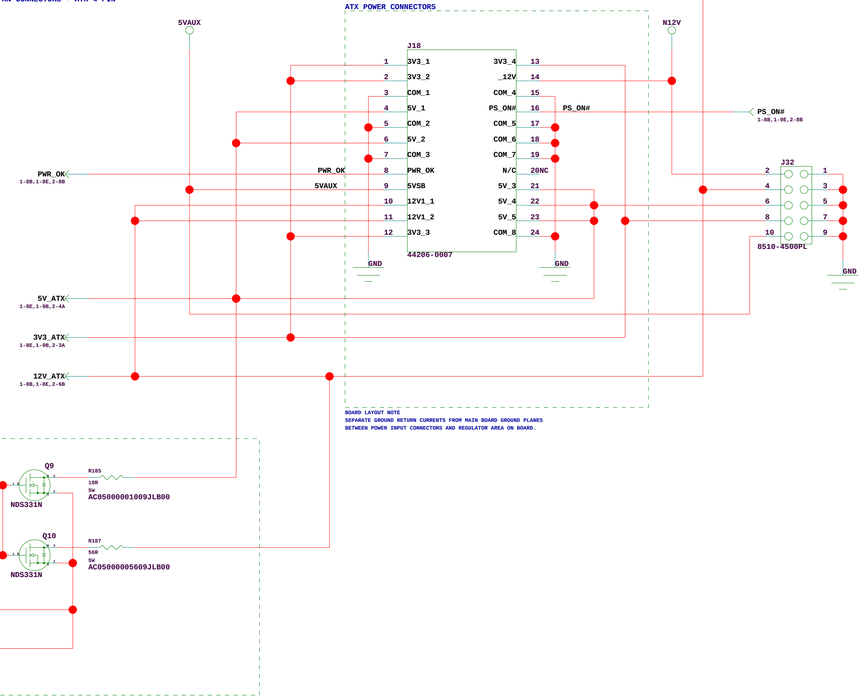
VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)
12V	0R01	3.36	0.11
5V	0R0047	6.78	0.22
3V3	0R01	3.47	0.12
2V5	0R01	3.56	0.13
1V8	0R0022	12.91	0.37
1V5	0R0047	6.77	0.22
1V0	0R001	26.79	0.72

FOR 8 BIT ADC USING 2.56V REFERENCE:

ADC COUNT AT MAX POWER	CURRENT/BIT (A)
33	0.1
31	0.21
34	0.1
35	0.1
28	0.45
31	0.21
26	1.0

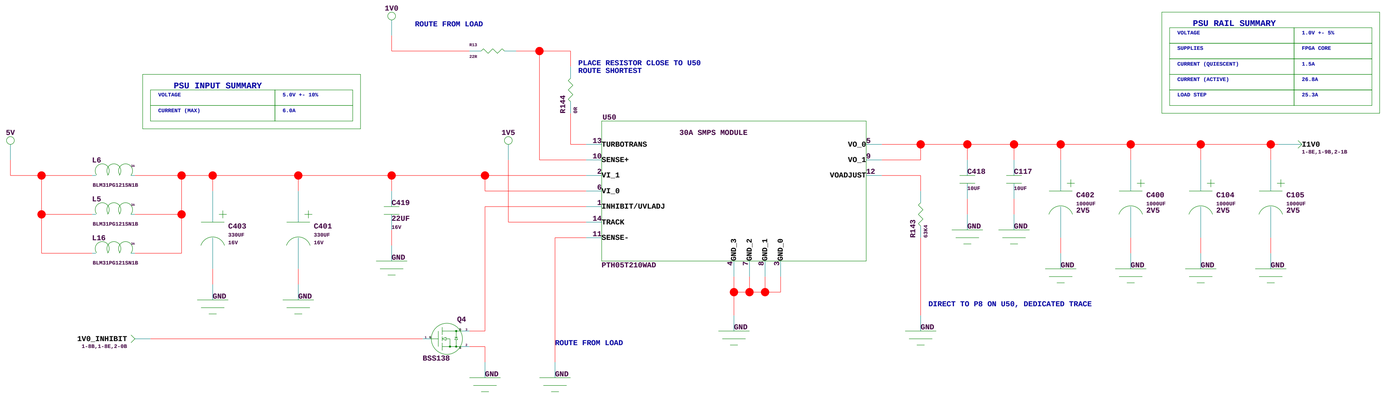
ROACH/iBOB2	ROACH_MONITOR
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-29-2008_11:08	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 2 OF 25



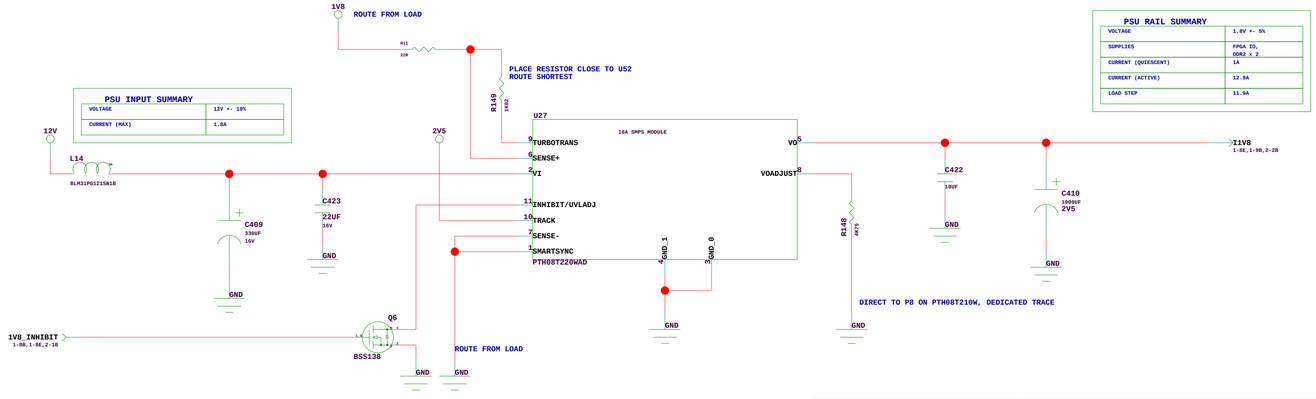


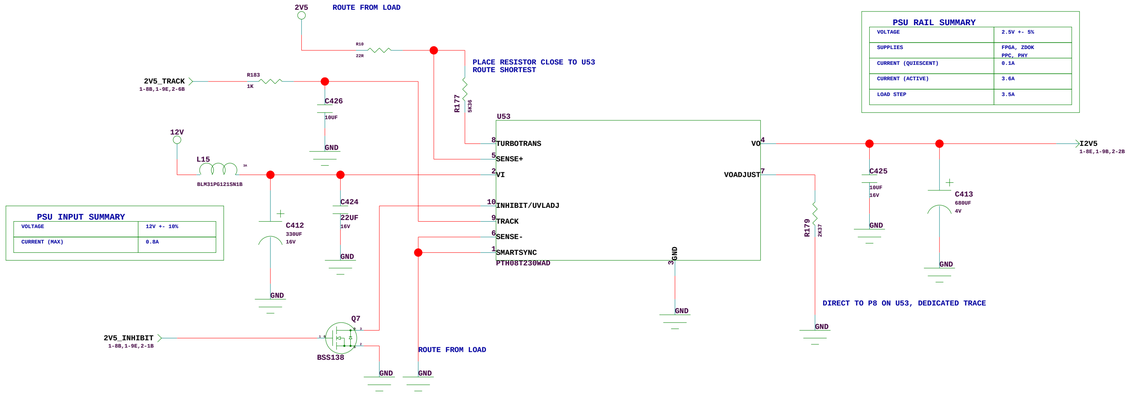
LOAD RESISTORS FOR ATX PSU MIN LOAD
SWITCH OFF ONCE LOAD EXCEEDS MINIMUM SPEC
ADJUST RESISTOR VALUES FOR ACTUAL SUPPLY

BOARD LAYOUT NOTE
SEPARATE GROUND RETURN CURRENTS FROM MAIN BOARD GROUND PLANES
BETWEEN POWER INPUT CONNECTORS AND REGULATOR AREA ON BOARD.



1.2V SUPPLY DELETED - NOT REQUIRED





ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

2-29-2008_11:08

PATH PATH

ROACH_PSU

DOC NO NRF-ADM-XXX-SD-0001

REVISION A

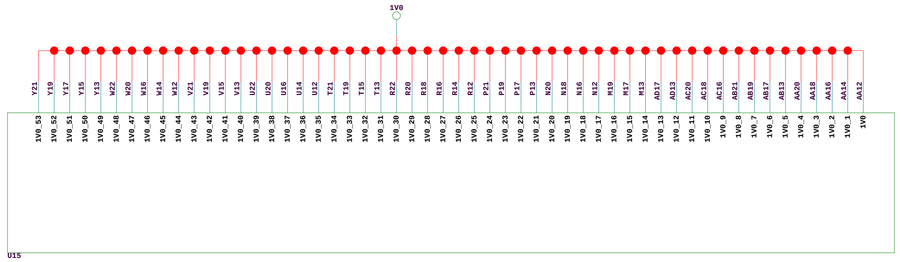
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW

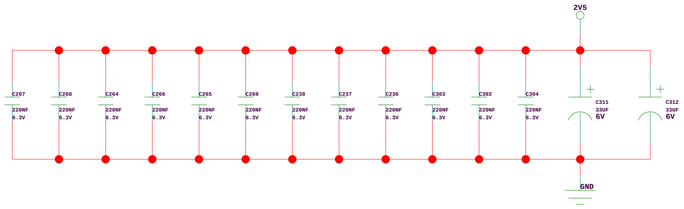
DRAWN: F KAPP

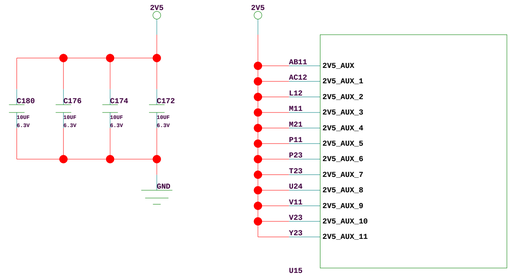
APPR:

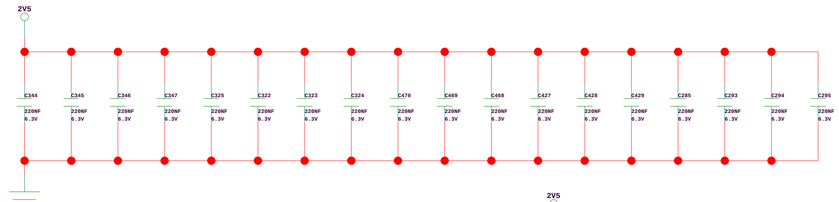
CHECKED: E BAUERMEISTER

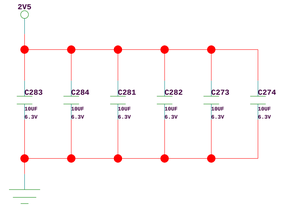
SHEET 3 OF 25

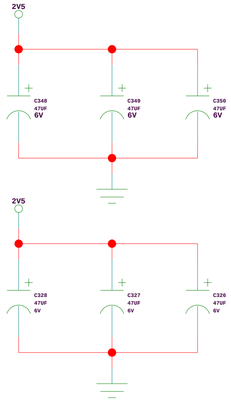


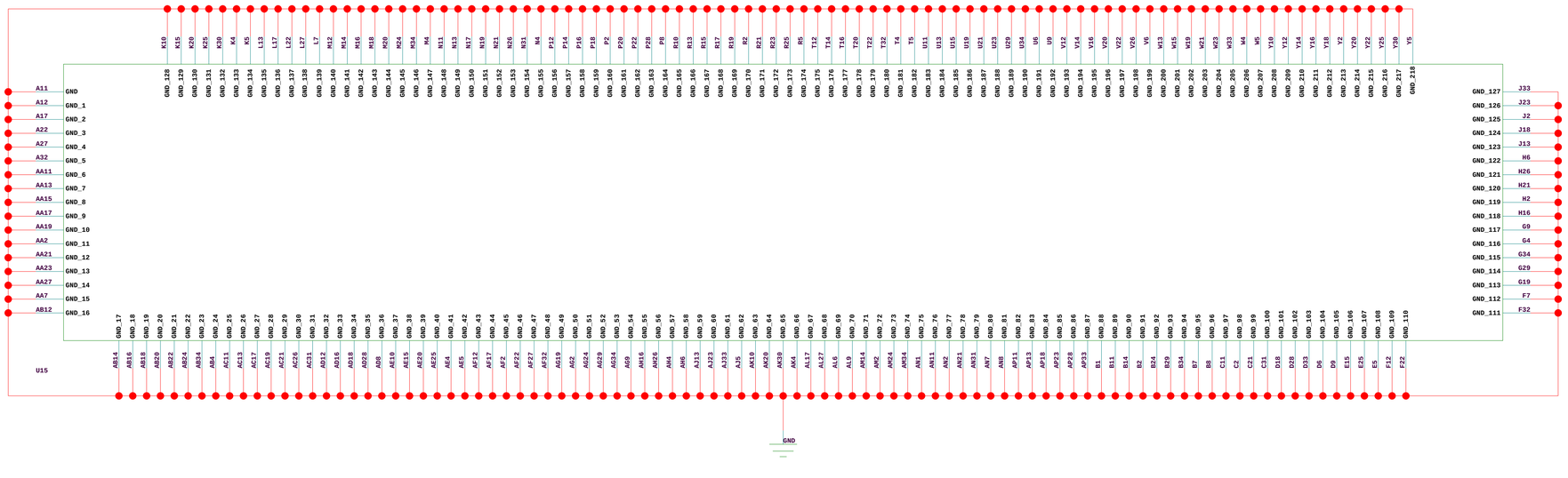












ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
2-29-2008_11:08 PATH PATH	

	A		B		C		D		E		F		G		H		J		K		L		M	
7																								7
		5-5L	ZDOK0_CLK0_P	J20	ZDOK0_CLK0_P		ZDOK0_DP_P[37]	B33	ZDOK0_DP_P37	5-3L														
		5-5L	ZDOK0_CLK0_N	J21	ZDOK0_CLK0_N		ZDOK0_DP_N[37]	C33	ZDOK0_DP_N37	5-3L														
		5-3L	ZDOK0_CLK1_P	H19	ZDOK0_CLK1_P		ZDOK0_DP_P[36]	F25	ZDOK0_DP_P36	5-3L														
		5-3L	ZDOK0_CLK1_N	H20	ZDOK0_CLK1_N		ZDOK0_DP_N[36]	F26	ZDOK0_DP_N36	5-3L														
							ZDOK0_DP_P[35]	E32	ZDOK0_DP_P35	5-4L														
							ZDOK0_DP_N[35]	E33	ZDOK0_DP_N35	5-4L														
							ZDOK0_DP_P[34]	F33	ZDOK0_DP_P34	5-4L														
							ZDOK0_DP_N[34]	E34	ZDOK0_DP_N34	5-4L														
							ZDOK0_DP_P[33]	G32	ZDOK0_DP_P33	5-4L														
							ZDOK0_DP_N[33]	H32	ZDOK0_DP_N33	5-4L														
							ZDOK0_DP_P[32]	J27	ZDOK0_DP_P32	5-4L														
							ZDOK0_DP_N[32]	J26	ZDOK0_DP_N32	5-4L														
							ZDOK0_DP_P[31]	H34	ZDOK0_DP_P31	5-4L														
							ZDOK0_DP_N[31]	J34	ZDOK0_DP_N31	5-4L														
							ZDOK0_DP_P[30]	K31	ZDOK0_DP_P30	5-5L														
							ZDOK0_DP_N[30]	L31	ZDOK0_DP_N30	5-5L														
							ZDOK0_DP_P[29]	L30	ZDOK0_DP_P29	5-5L														
							ZDOK0_DP_N[29]	M30	ZDOK0_DP_N29	5-5L														
							ZDOK0_DP_P[28]	C34	ZDOK0_DP_P28	5-5L														
							ZDOK0_DP_N[28]	D34	ZDOK0_DP_N28	5-5L														
							ZDOK0_DP_P[27]	E29	ZDOK0_DP_P27	5-5L														
							ZDOK0_DP_N[27]	F29	ZDOK0_DP_N27	5-5L														
							ZDOK0_DP_P[26]	H25	ZDOK0_DP_P26	5-6L														
							ZDOK0_DP_N[26]	H24	ZDOK0_DP_N26	5-6L														
							ZDOK0_DP_P[25]	G30	ZDOK0_DP_P25	5-6L														
							ZDOK0_DP_N[25]	F30	ZDOK0_DP_N25	5-6L														
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							ZDOK0_DP_N[24]	F34	ZDOK0_DP_N24	5-6L														
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							ZDOK0_DP_N[23]	J31	ZDOK0_DP_N23	5-6L														
							ZDOK0_DP_P[22]	L25	ZDOK0_DP_P22	5-6L														
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							ZDOK0_DP_P[21]	L29	ZDOK0_DP_P21	5-7L														
							ZDOK0_DP_N[21]	K29	ZDOK0_DP_N21	5-7L														
							ZDOK0_DP_P[20]	N27	ZDOK0_DP_P20	5-7L														
							ZDOK0_DP_N[20]	M27	ZDOK0_DP_N20	5-7L														
							ZDOK0_DP_P[19]	B32	ZDOK0_DP_P19	5-3J														
							ZDOK0_DP_N[19]	A33	ZDOK0_DP_N19	5-3J														
							ZDOK0_DP_P[18]	E26	ZDOK0_DP_P18	5-3J														
							ZDOK0_DP_N[18]	E27	ZDOK0_DP_N18	5-3J														
							ZDOK0_DP_P[17]	G25	ZDOK0_DP_P17	5-3J														
							ZDOK0_DP_N[17]	G26	ZDOK0_DP_N17	5-3J														
							ZDOK0_DP_P[16]	G27	ZDOK0_DP_P16	5-4J														
							ZDOK0_DP_N[16]	H27	ZDOK0_DP_N16	5-4J														
							ZDOK0_DP_P[15]	J24	ZDOK0_DP_P15	5-4J														
							ZDOK0_DP_N[15]	J25	ZDOK0_DP_N15	5-4J														
							ZDOK0_DP_P[14]	H30	ZDOK0_DP_P14	5-4J														
							ZDOK0_DP_N[14]	G31	ZDOK0_DP_N14	5-4J														
							ZDOK0_DP_P[13]	K27	ZDOK0_DP_P13	5-4J														
							ZDOK0_DP_N[13]	K26	ZDOK0_DP_N13	5-4J														
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							ZDOK0_DP_N[10]	K34	ZDOK0_DP_N10	5-5J														
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							ZDOK0_DP_N[6]	G28	ZDOK0_DP_N6	5-6J														
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							ZDOK0_DP_N[5]	J29	ZDOK0_DP_N5	5-6J														
							ZDOK0_DP_P[4]	K24	ZDOK0_DP_P4	5-6J														
							ZDOK0_DP_N[4]	L24	ZDOK0_DP_N4	5-6J														
							ZDOK0_DP_P[3]	K28	ZDOK0_DP_P3	5-6J														
							ZDOK0_DP_N[3]	L28	ZDOK0_DP_N3	5-6J														
							ZDOK0_DP_P[2]	M25	ZDOK0_DP_P2	5-6J														
							ZDOK0_DP_N[2]	M26	ZDOK0_DP_N2	5-6J														
							ZDOK0_DP_P[1]	M28	ZDOK0_DP_P1	5-7J														
							ZDOK0_DP_N[1]	N28	ZDOK0_DP_N1	5-7J														
							ZDOK0_DP_P[0]	M31	ZDOK0_DP_P0	5-7J														
							ZDOK0_DP_N[0]	N30	ZDOK0_DP_N0	5-7J														
6																								6
5																								5
4																								4
3																								3
2																								2
1																								1
0																								0
	A		B		C		D		E		F		G		H		J		K		L		M	

U15

BANKS=11, 13, 15, 17, 19, 21

5V

3V3

2V5

1V8

C315 1UF 16V

C314 100NF 10V

C317 1UF 16V

C316 100NF 10V

C318 1UF 16V

C319 100NF 10V

C321 1UF 16V

C320 100NF 10V

P5

W1 X1 Y1 Z1 W2 X2 Y2 Z2 W3 X3 Y3 Z3 W4 X4 Y4 Z4 W5 X5 Y5 Z5 W6 X6 Y6 Z6

B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20

6367550-5

ZDOK40

5-0E	ZDOK0_DP_P0	A1	A1	C1	C1	ZDOK0_DP_P20	5-4E																	
5-0E	ZDOK0_DP_N0	A2	A2	C2	C2	ZDOK0_DP_N20	5-4E																	
5-0E	ZDOK0_DP_P1	A3	A3	C3	C3	ZDOK0_DP_P21	5-4E																	
5-0E	ZDOK0_DP_N1	A4	A4	C4	C4	ZDOK0_DP_N21	5-4E																	
5-0E	ZDOK0_DP_P2	A5	A5	C5	C5	ZDOK0_DP_P22	5-4E																	
5-0E	ZDOK0_DP_N2	A6	A6	C6	C6	ZDOK0_DP_N22	5-4E																	
5-1E	ZDOK0_DP_P3	A7	A7	C7	C7	ZDOK0_DP_P23	5-5E																	
5-1E	ZDOK0_DP_N3	A8	A8	C8	C8	ZDOK0_DP_N23	5-5E																	
5-1E	ZDOK0_DP_P4	A9	A9	C9	C9	ZDOK0_DP_P24	5-5E																	
5-1E	ZDOK0_DP_N4	A10	A10	C10	C10	ZDOK0_DP_N24	5-5E																	
5-1E	ZDOK0_DP_P5	A11	A11	C11	C11	ZDOK0_DP_P25	5-5E																	
5-1E	ZDOK0_DP_N5	A12	A12	C12	C12	ZDOK0_DP_N25	5-5E																	
5-1E	ZDOK0_DP_P6	A13	A13	C13	C13	ZDOK0_DP_P26	5-5E																	
5-1E	ZDOK0_DP_N6	A14	A14	C14	C14	ZDOK0_DP_N26	5-5E																	
5-1E	ZDOK0_DP_P7	A15	A15	C15	C15	ZDOK0_DP_P27	5-5E																	
5-1E	ZDOK0_DP_N7	A16	A16	C16	C16	ZDOK0_DP_N27	5-5E																	
5-2E	ZDOK0_DP_P8	A17	A17	C17	C17	ZDOK0_DP_P28	5-6E																	
5-2E	ZDOK0_DP_N8	A18	A18	C18	C18	ZDOK0_DP_N28	5-6E																	
5-2E	ZDOK0_DP_P9	A19	A19	C19	ZDOK0_CLK0_P		5-7B																	
5-2E	ZDOK0_DP_N9	A20	A20	C20	ZDOK0_CLK0_N		5-7B																	
5-2E	ZDOK0_DP_P10	D1	D1	F1	ZDOK0_DP_P29		5-6E																	
5-2E	ZDOK0_DP_N10	D2	D2	F2	ZDOK0_DP_N29		5-6E																	
5-2E	ZDOK0_DP_P11	D3	D3	F3	ZDOK0_DP_P30		5-6E																	
5-2E	ZDOK0_DP_N11	D4	D4	F4	ZDOK0_DP_N30		5-6E																	
5-2E	ZDOK0_DP_P12	D5	D5	F5	ZDOK0_DP_P31		5-6E																	
5-2E	ZDOK0_DP_N12	D6	D6	F6	ZDOK0_DP_N31		5-6E																	
5-3E	ZDOK0_DP_P13	D7	D7	F7	ZDOK0_DP_P32		5-6E																	
5-3E	ZDOK0_DP_N13	D8	D8	F8	ZDOK0_DP_N32		5-6E																	
5-3E	ZDOK0_DP_P14	D9	D9	F9	ZDOK0_DP_P33		5-7E																	
5-3E	ZDOK0_DP_N14	D10	D10	F10	ZDOK0_DP_N33		5-7E																	
5-3E	ZDOK0_DP_P15	D11	D11	F11	ZDOK0_DP_P34		5-7E																	
5-3E	ZDOK0_DP_N15	D12	D12	F12	ZDOK0_DP_N34		5-7E																	
5-3E	ZDOK0_DP_P16	D13	D13	F13	ZDOK0_DP_P35		5-7E																	
5-3E	ZDOK0_DP_N16	D14	D14	F14	ZDOK0_DP_N35		5-7E																	
5-3E	ZDOK0_DP_P17	D15	D15	F15	ZDOK0_DP_P36		5-7E																	
5-3E	ZDOK0_DP_N17	D16	D16	F16	ZDOK0_DP_N36		5-7E																	
5-4E	ZDOK0_DP_P18	D17	D17	F17	ZDOK0_DP_P37		5-7E																	
5-4E	ZDOK0_DP_N18	D18	D18	F18	ZDOK0_DP_N37		5-7E																	
5-4E	ZDOK0_DP_P19	D19	D19	F19	ZDOK0_CLK1_P		5-7B																	
5-4E	ZDOK0_DP_N19	D20	D20	F20	ZDOK0_CLK1_N		5-7B																	

P5

A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20

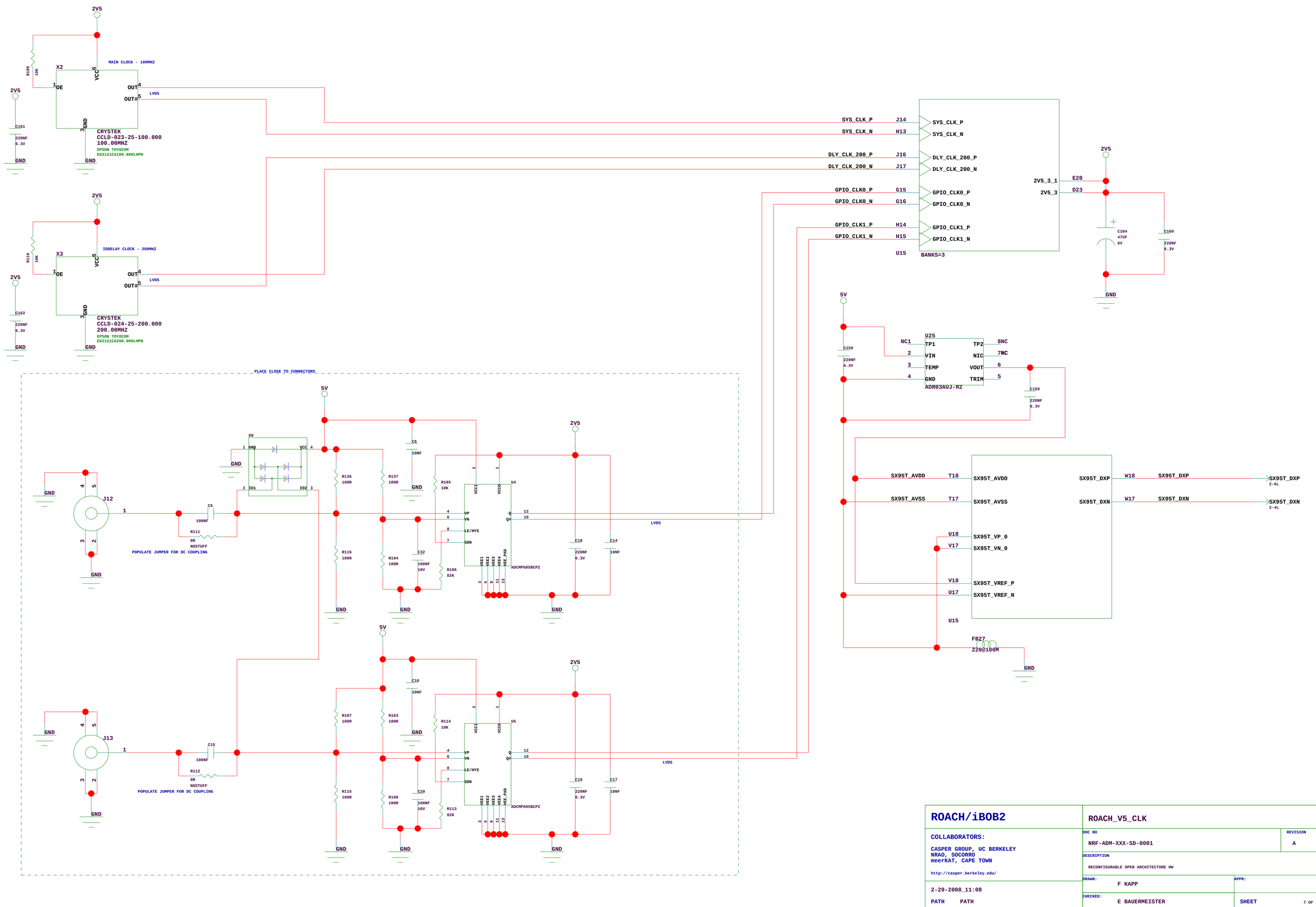
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15 F16 F17 F18 F19 F20

6367550-5

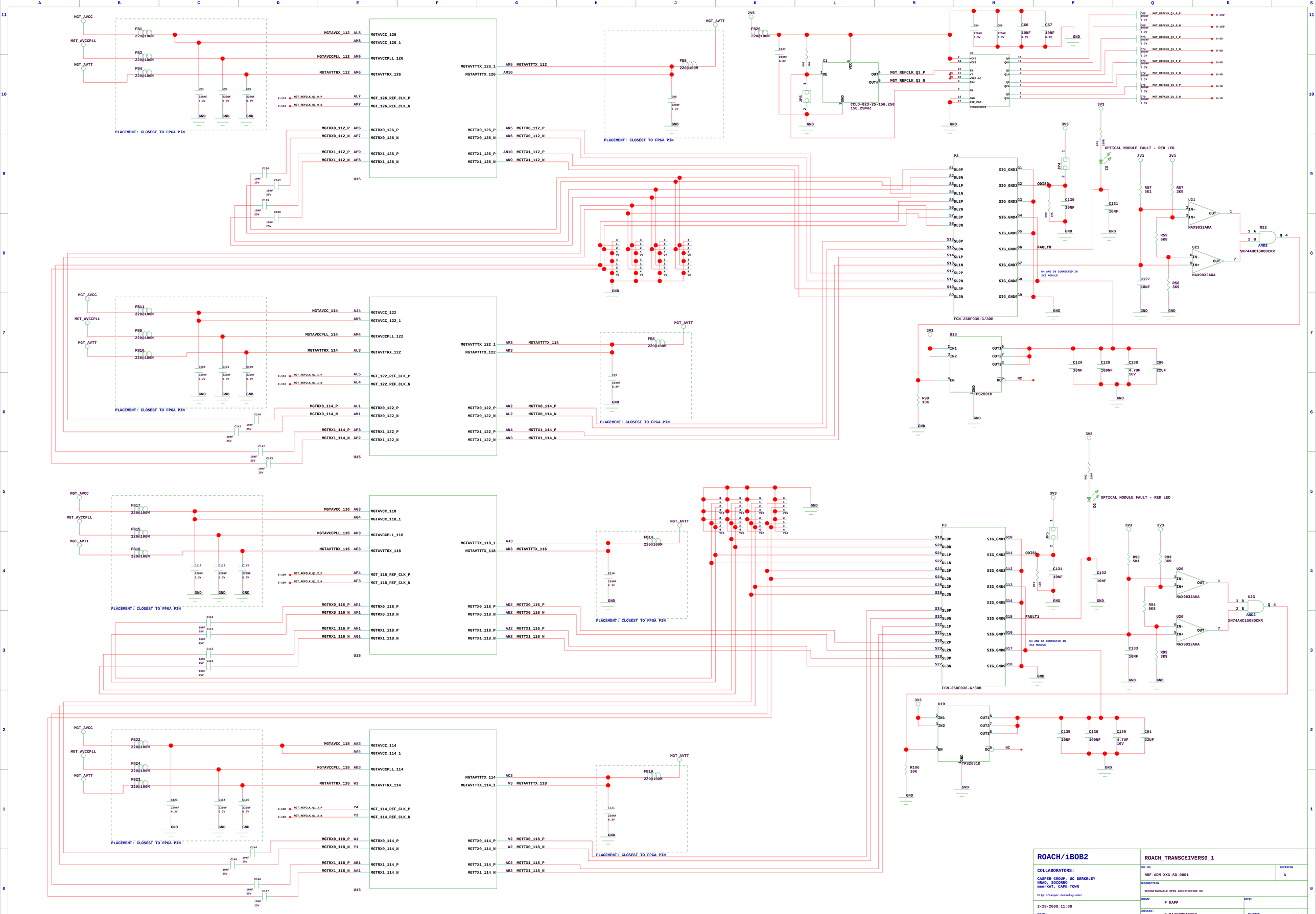
ZDOK40

ROACH/iBOB2	**ROACH_ADC_0**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-29-2008_11:08 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 5 OF 25


ZDOK1_CLK0_P H17
ZDOK1_CLK0_N H18
ZDOK1_CLK1_P K17
ZDOK1_CLK1_N L18
ZDOK1_CLK0_P
ZDOK1_CLK0_N
ZDOK1_CLK1_P
ZDOK1_CLK1_N
ZDOK1_DP_P[37] AD31 ZDOK1_DP_P37
ZDOK1_DP_N[37] AE31 ZDOK1_DP_N37
ZDOK1_DP_P[36] AF33 ZDOK1_DP_P36
ZDOK1_DP_N[36] AE33 ZDOK1_DP_N36
ZDOK1_DP_P[35] AF31 ZDOK1_DP_P35
ZDOK1_DP_N[35] AG31 ZDOK1_DP_N35
ZDOK1_DP_P[34] AG32 ZDOK1_DP_P34
ZDOK1_DP_N[34] AH32 ZDOK1_DP_N34
ZDOK1_DP_P[33] AG28 ZDOK1_DP_P33
ZDOK1_DP_N[33] AH28 ZDOK1_DP_N33
ZDOK1_DP_P[32] AF24 ZDOK1_DP_P32
ZDOK1_DP_N[32] AG25 ZDOK1_DP_N32
ZDOK1_DP_P[31] AJ30 ZDOK1_DP_P31
ZDOK1_DP_N[31] AH30 ZDOK1_DP_N31
ZDOK1_DP_P[30] AK28 ZDOK1_DP_P30
ZDOK1_DP_N[30] AK27 ZDOK1_DP_N30
ZDOK1_DP_P[29] AK26 ZDOK1_DP_P29
ZDOK1_DP_N[29] AJ27 ZDOK1_DP_N29
ZDOK1_DP_P[28] AB27 ZDOK1_DP_P28
ZDOK1_DP_N[28] AC27 ZDOK1_DP_N28
ZDOK1_DP_P[27] AD30 ZDOK1_DP_P27
ZDOK1_DP_N[27] AC29 ZDOK1_DP_N27
ZDOK1_DP_P[26] AE29 ZDOK1_DP_P26
ZDOK1_DP_N[26] AD29 ZDOK1_DP_N26
ZDOK1_DP_P[25] AG33 ZDOK1_DP_P25
ZDOK1_DP_N[25] AH33 ZDOK1_DP_N25
ZDOK1_DP_P[24] AF29 ZDOK1_DP_P24
ZDOK1_DP_N[24] AF30 ZDOK1_DP_N24
ZDOK1_DP_P[23] AG27 ZDOK1_DP_P23
ZDOK1_DP_N[23] AG26 ZDOK1_DP_N23
ZDOK1_DP_P[22] AK34 ZDOK1_DP_P22
ZDOK1_DP_N[22] AK33 ZDOK1_DP_N22
ZDOK1_DP_P[21] AL34 ZDOK1_DP_P21
ZDOK1_DP_N[21] AL33 ZDOK1_DP_N21
ZDOK1_DP_P[20] AJ25 ZDOK1_DP_P20
ZDOK1_DP_N[20] AH25 ZDOK1_DP_N20
ZDOK1_DP_P[19] AB30 ZDOK1_DP_P19
ZDOK1_DP_N[19] AC30 ZDOK1_DP_N19
ZDOK1_DP_P[18] AC28 ZDOK1_DP_P18
ZDOK1_DP_N[18] AD27 ZDOK1_DP_N18
ZDOK1_DP_P[17] AC25 ZDOK1_DP_P17
ZDOK1_DP_N[17] AC24 ZDOK1_DP_N17
ZDOK1_DP_P[16] AE28 ZDOK1_DP_P16
ZDOK1_DP_N[16] AF28 ZDOK1_DP_N16
ZDOK1_DP_P[15] AD24 ZDOK1_DP_P15
ZDOK1_DP_N[15] AE24 ZDOK1_DP_N15
ZDOK1_DP_P[14] AF25 ZDOK1_DP_P14
ZDOK1_DP_N[14] AF26 ZDOK1_DP_N14
ZDOK1_DP_P[13] AH29 ZDOK1_DP_P13
ZDOK1_DP_N[13] AG30 ZDOK1_DP_N13
ZDOK1_DP_P[12] AH27 ZDOK1_DP_P12
ZDOK1_DP_N[12] AJ26 ZDOK1_DP_N12
ZDOK1_DP_P[11] AM33 ZDOK1_DP_P11
ZDOK1_DP_N[11] AM32 ZDOK1_DP_N11
ZDOK1_DP_P[10] AN32 ZDOK1_DP_P10
ZDOK1_DP_N[10] AP32 ZDOK1_DP_N10
ZDOK1_DP_P[9] AC34 ZDOK1_DP_P9
ZDOK1_DP_N[9] AD34 ZDOK1_DP_N9
ZDOK1_DP_P[8] AD32 ZDOK1_DP_P8
ZDOK1_DP_N[8] AE32 ZDOK1_DP_N8
ZDOK1_DP_P[7] AF34 ZDOK1_DP_P7
ZDOK1_DP_N[7] AE34 ZDOK1_DP_N7
ZDOK1_DP_P[6] AD26 ZDOK1_DP_P6
ZDOK1_DP_N[6] AD25 ZDOK1_DP_N6
ZDOK1_DP_P[5] AE27 ZDOK1_DP_P5
ZDOK1_DP_N[5] AE26 ZDOK1_DP_N5
ZDOK1_DP_P[4] AH34 ZDOK1_DP_P4
ZDOK1_DP_N[4] AJ34 ZDOK1_DP_N4
ZDOK1_DP_P[3] AJ32 ZDOK1_DP_P3
ZDOK1_DP_N[3] AK32 ZDOK1_DP_N3
ZDOK1_DP_P[2] AJ31 ZDOK1_DP_P2
ZDOK1_DP_N[2] AK31 ZDOK1_DP_N2
ZDOK1_DP_P[1] AK29 ZDOK1_DP_P1
ZDOK1_DP_N[1] AJ29 ZDOK1_DP_N1
ZDOK1_DP_P[0] AN34 ZDOK1_DP_P0
ZDOK1_DP_N[0] AN33 ZDOK1_DP_N0
U15
BANKS=11, 13, 15, 17, 19, 21
5V
3V3
2V5
1V8
C337 1UF 16V
C336 100NF 10V
C339 1UF 16V
C338 100NF 10V
C340 1UF 16V
C341 100NF 10V
C343 1UF 16V
C342 100NF 10V
P7
W1 X1 Y1 Z1 W2 X2 Y2 Z2 W3 X3 Y3 Z3 W4 X4 Y4 Z4 W5 X5 Y5 Z5 W6 X6 Y6 Z6
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20
E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20
6367550-5
ZDOK40
ZDOK1_DP_P0 A1
ZDOK1_DP_N0 A2
ZDOK1_DP_P1 A3
ZDOK1_DP_N1 A4
ZDOK1_DP_P2 A5
ZDOK1_DP_N2 A6
ZDOK1_DP_P3 A7
ZDOK1_DP_N3 A8
ZDOK1_DP_P4 A9
ZDOK1_DP_N4 A10
ZDOK1_DP_P5 A11
ZDOK1_DP_N5 A12
ZDOK1_DP_P6 A13
ZDOK1_DP_N6 A14
ZDOK1_DP_P7 A15
ZDOK1_DP_N7 A16
ZDOK1_DP_P8 A17
ZDOK1_DP_N8 A18
ZDOK1_DP_P9 A19
ZDOK1_DP_N9 A20
ZDOK1_DP_P10 D1
ZDOK1_DP_N10 D2
ZDOK1_DP_P11 D3
ZDOK1_DP_N11 D4
ZDOK1_DP_P12 D5
ZDOK1_DP_N12 D6
ZDOK1_DP_P13 D7
ZDOK1_DP_N13 D8
ZDOK1_DP_P14 D9
ZDOK1_DP_N14 D10
ZDOK1_DP_P15 D11
ZDOK1_DP_N15 D12
ZDOK1_DP_P16 D13
ZDOK1_DP_N16 D14
ZDOK1_DP_P17 D15
ZDOK1_DP_N17 D16
ZDOK1_DP_P18 D17
ZDOK1_DP_N18 D18
ZDOK1_DP_P19 D19
ZDOK1_DP_N19 D20
P7
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20
C1 ZDOK1_DP_P20
C2 ZDOK1_DP_N20
C3 ZDOK1_DP_P21
C4 ZDOK1_DP_N21
C5 ZDOK1_DP_P22
C6 ZDOK1_DP_N22
C7 ZDOK1_DP_P23
C8 ZDOK1_DP_N23
C9 ZDOK1_DP_P24
C10 ZDOK1_DP_N24
C11 ZDOK1_DP_P25
C12 ZDOK1_DP_N25
C13 ZDOK1_DP_P26
C14 ZDOK1_DP_N26
C15 ZDOK1_DP_P27
C16 ZDOK1_DP_N27
C17 ZDOK1_DP_P28
C18 ZDOK1_DP_N28
C19 ZDOK1_CLK0_P
C20 ZDOK1_CLK0_N
F1 ZDOK1_DP_P29
F2 ZDOK1_DP_N29
F3 ZDOK1_DP_P30
F4 ZDOK1_DP_N30
F5 ZDOK1_DP_P31
F6 ZDOK1_DP_N31
F7 ZDOK1_DP_P32
F8 ZDOK1_DP_N32
F9 ZDOK1_DP_P33
F10 ZDOK1_DP_N33
F11 ZDOK1_DP_P34
F12 ZDOK1_DP_N34
F13 ZDOK1_DP_P35
F14 ZDOK1_DP_N35
F15 ZDOK1_DP_P36
F16 ZDOK1_DP_N36
F17 ZDOK1_DP_P37
F18 ZDOK1_DP_N37
F19 ZDOK1_CLK1_P
F20 ZDOK1_CLK1_N
6367550-5
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
2-29-2008_11:08
PATH PATH
ROACH_ADC_1
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 6 OF 25



ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
2-29-2008_11:08 PATH PATH	


MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB3 220@100M
FB4 220@100M
C84 C93 C92 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_112 AL8 MGTAVCC_126
AM8 MGTAVCC_126_1
MGTAVCCPLL_112 AM9 MGTAVCCPLL_126
MGTAVTTRX_112 AM6 MGTAVTTRX_126
B-11R MGT_REFCLK_Q1_0_P AL7 MGT_126_REF_CLK_P
B-11R MGT_REFCLK_Q1_0_N AM7 MGT_126_REF_CLK_N
MGTRX0_112_P AP6 MGTRX0_126_P
MGTRX0_112_N AP7 MGTRX0_126_N
MGTRX1_112_P AP9 MGTRX1_126_P
MGTRX1_112_N AP8 MGTRX1_126_N
U15
MGTAVTTTX_126_1 AM5 MGTAVTTTX_112
MGTAVTTTX_126 AM10
MGTTX0_126_P AN5 MGTTX0_112_P
MGTTX0_126_N AN6 MGTTX0_112_N
MGTTX1_126_P AN10 MGTTX1_112_P
MGTTX1_126_N AN9 MGTTX1_112_N
MGT_AVTT
FB5 220@100M
C96 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
C106 C107 C109 C108 10NF 25V
V1 V2 V3 V4 V5 V6 V7 V8
2V5
FB26 220@100M
C137 220NF 6.3V
R84 10K
X1 CCLD-023-25-156.250 156.25MHZ
JP6
VCC OE GND OUT OUT*
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
U8 5T89032QMI
C64 C65 C66 C67 220NF 10NF 6.3V
C68 C69 C75 C74 C73 C72 C71 C70 100NF 6.3V
MGT_REFCLK_Q1_0_P B-10D
MGT_REFCLK_Q1_0_N B-10D
MGT_REFCLK_Q1_1_P B-6D
MGT_REFCLK_Q1_1_N B-6D
MGT_REFCLK_Q1_2_P B-4D
MGT_REFCLK_Q1_2_N B-4D
MGT_REFCLK_Q1_3_P B-1D
MGT_REFCLK_Q1_3_N B-1D
3V3
R85 100R
D2 OPTICAL MODULE FAULT - RED LED
P3 FCN-268F036-G/3DB
DL0P DL0N DL1P DL1N DL2P DL2N DL3P DL3N SL0P SL0N SL1P SL1N SL2P SL2N SL3P SL3N
SIG_GND1 SIG_GND2 SIG_GND3 SIG_GND4 SIG_GND5 SIG_GND6 SIG_GND7 SIG_GND8 SIG_GND9
ODIS0 FAULT0
JP4
C130 C131 10NF
R86 10K
R97 5K1 R98 5K1 R93 3K9 R57 3K9 R59 6K8 R58 3K9 R94 6K8 R95 3K9
U21 MAX9032AKA
U22 AND2 SN74AHC1G08DCKR
G4 AND G8 CONNECTED IN 2X2 MODULE
C127 C133 10NF
U18 U19 TPS2031D
R99 10K R100 10K
C129 C135 10NF
C128 C136 100NF
C138 C139 4.7UF 16V
C90 C91 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB11 FB9 FB10 220@100M
C102 C101 C100 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_114 AJ4 MGTAVCC_122
AK5 MGTAVCC_122_1
MGTAVCCPLL_114 AM4 MGTAVCCPLL_122
MGTAVTTRX_114 AL3 MGTAVTTRX_122
B-11R MGT_REFCLK_Q3_1_P AL5 MGT_122_REF_CLK_P
B-11R MGT_REFCLK_Q3_1_N AL4 MGT_122_REF_CLK_N
MGTRX0_114_P AL1 MGTRX0_122_P
MGTRX0_114_N AM1 MGTRX0_122_N
MGTRX1_114_P AP3 MGTRX1_122_P
MGTRX1_114_N AP2 MGTRX1_122_N
U15
MGTAVTTTX_122_1 AM3 MGTAVTTTX_114
MGTAVTTTX_122 AK3
MGTTX0_122_P AK2 MGTTX0_114_P
MGTTX0_122_N AL2 MGTTX0_114_N
MGTTX1_122_P AN4 MGTTX1_114_P
MGTTX1_122_N AN3 MGTTX1_114_N
FB8 220@100M
C99 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C140 C141 C142 C143 10NF 25V
V9 V10 V11 V12 V13 V14 V15 V16
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB17 FB15 FB16 220@100M
C119 C118 C115 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_116 AG3 MGTAVCC_118
AG4 MGTAVCC_118_1
MGTAVCCPLL_116 AH3 MGTAVCCPLL_118
MGTAVTTRX_116 AE3 MGTAVTTRX_118
B-10R MGT_REFCLK_Q3_2_P AF4 MGT_118_REF_CLK_P
B-10R MGT_REFCLK_Q3_2_N AF3 MGT_118_REF_CLK_N
MGTRX0_116_P AE1 MGTRX0_118_P
MGTRX0_116_N AF1 MGTRX0_118_N
MGTRX1_116_P AH1 MGTRX1_118_P
MGTRX1_116_N AG1 MGTRX1_118_N
U15
MGTAVTTTX_118_1 AJ3
MGTAVTTTX_118 AD3 MGTAVTTTX_116
MGTTX0_118_P AD2 MGTTX0_116_P
MGTTX0_118_N AE2 MGTTX0_116_N
MGTTX1_118_P AJ2 MGTTX1_116_P
MGTTX1_118_N AH2 MGTTX1_116_N
FB14 220@100M
C110 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C110 C111 C112 C113 10NF 25V
V17 V18 V19 V20 V21 V22 V23 V24 V25
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB22 FB24 FB23 220@100M
C123 C114 C125 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_118 AA3 MGTAVCC_114
AA4 MGTAVCC_114_1
MGTAVCCPLL_118 AB3 MGTAVCCPLL_114
MGTAVTTRX_118 W3 MGTAVTTRX_114
B-10R MGT_REFCLK_Q3_3_P Y4 MGT_114_REF_CLK_P
B-10R MGT_REFCLK_Q3_3_N Y3 MGT_114_REF_CLK_N
MGTRX0_118_P W1 MGTRX0_114_P
MGTRX0_118_N Y1 MGTRX0_114_N
MGTRX1_118_P AB1 MGTRX1_114_P
MGTRX1_118_N AA1 MGTRX1_114_N
U15
MGTAVTTTX_114 AC3
MGTAVTTTX_114_1 V3 MGTAVTTTX_118
MGTTX0_114_P V2 MGTTX0_118_P
MGTTX0_114_N W2 MGTTX0_118_N
MGTTX1_114_P AC2 MGTTX1_118_P
MGTTX1_114_N AB2 MGTTX1_118_N
FB19 220@100M
C121 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C144 C145 C146 C147 10NF 25V
V26 V27 V28 V29 V30 V31 V32 V33 V34
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
2-29-2008_11:08
PATH
ROACH_TRANSCEIVERS0_1
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE MK
DRAWN: F KAPP
CHECKED: E BAUERMEISTER
APPR:
SHEET 8 OF 25

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

OPTICAL MODULE FAULT - RED LED

G4 AND G8 CONNECTED IN
2X2 MODULE

CCLD-023-25-156.250
156.25MHZ

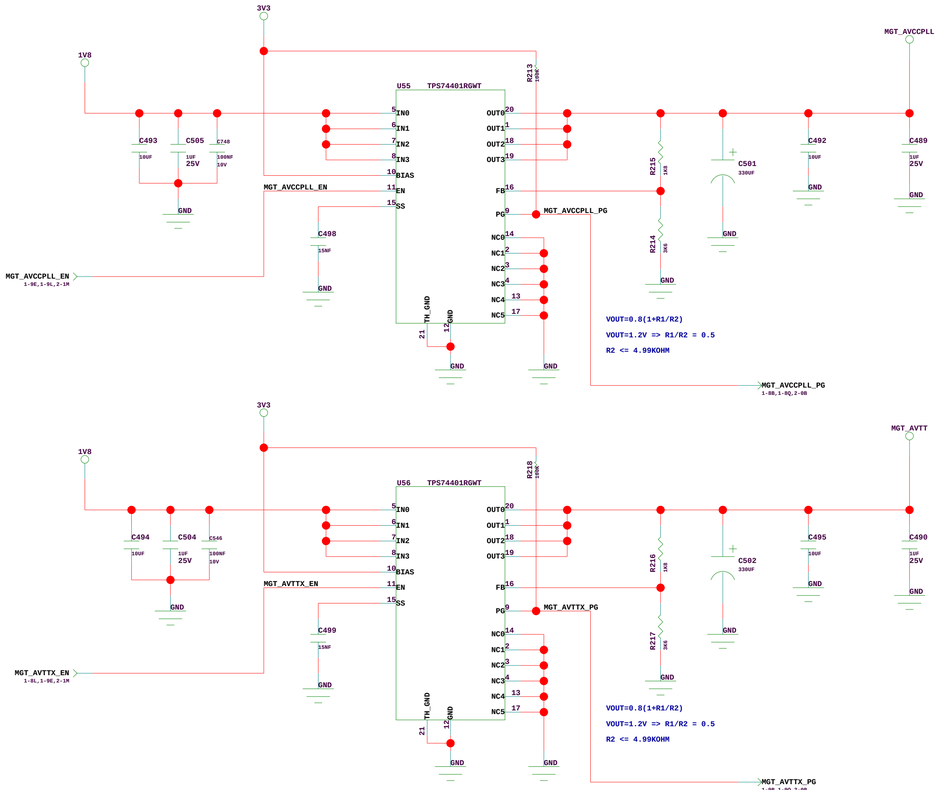
FCN-268F036-G/3DB

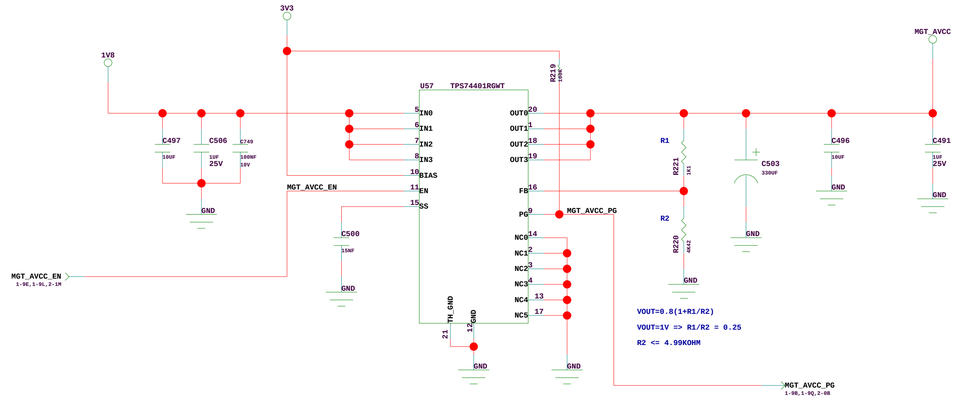
MAX9032AKA

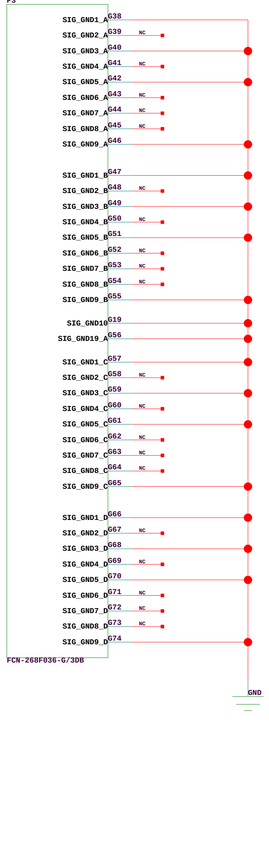
SN74AHC1G08DCKR

TPS2031D

ROACH/iBOB2	**ROACH_TRANSCEIVERS2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-29-2008_11:08	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 9 OF 25







ROACH/iBOB2

ROACH_TRANSCEIVERS_PSU

COLLABORATORS:

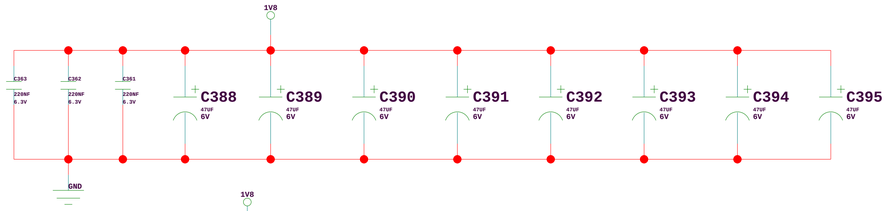
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

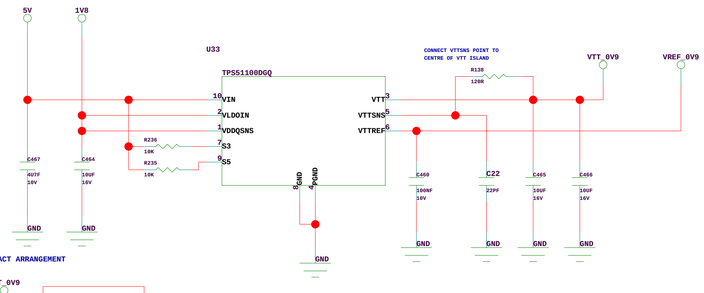
http://casper.berkeley.edu/

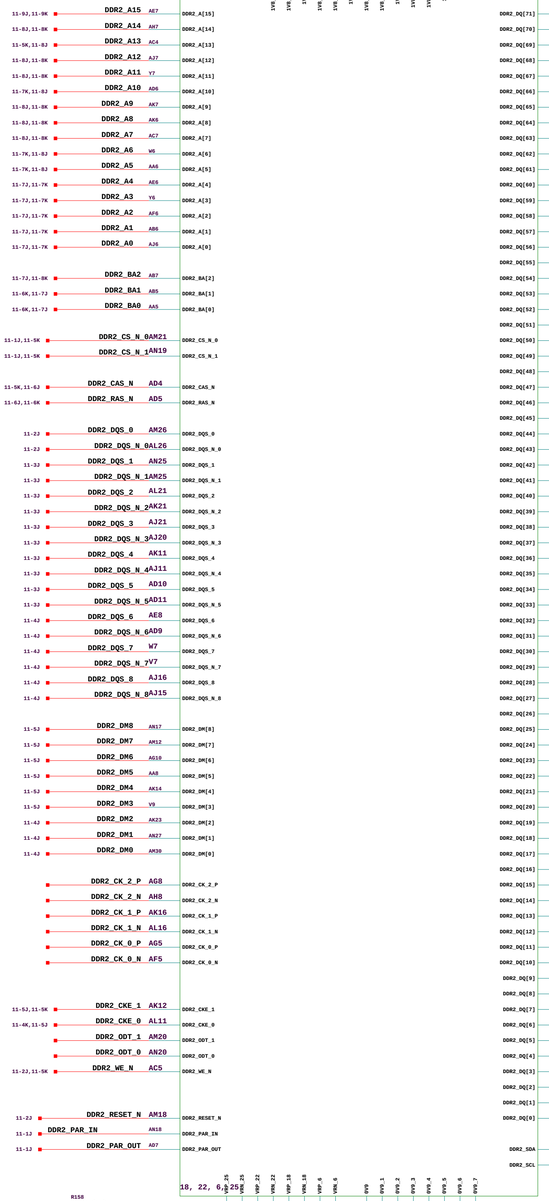
2-29-2008_11:08

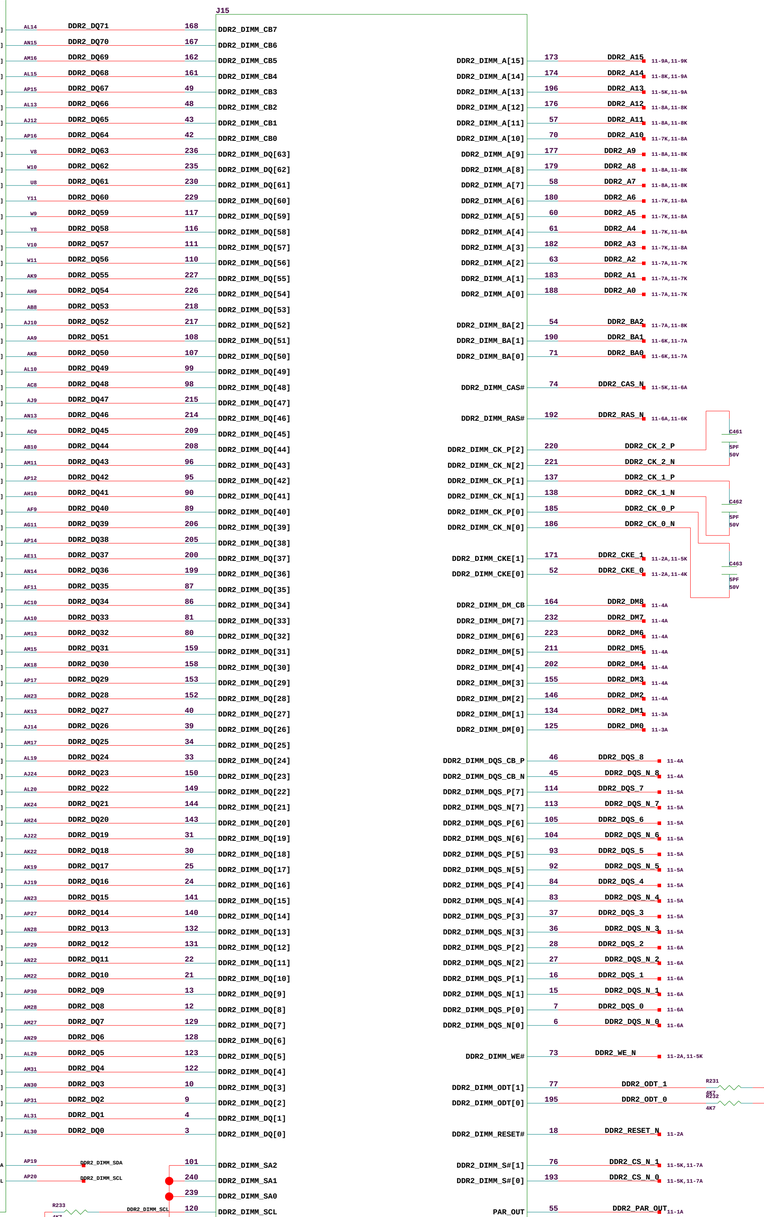
PATH PATH

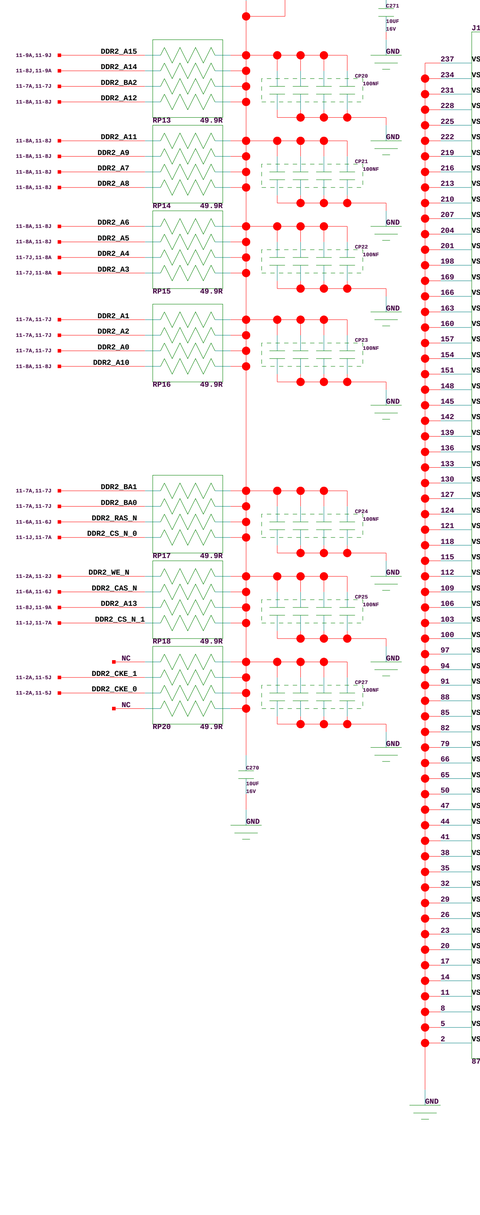
DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	10 OF 25



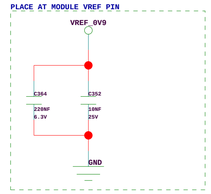


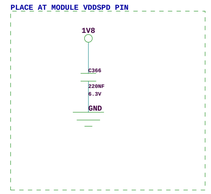


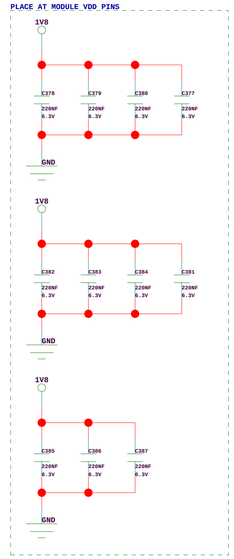


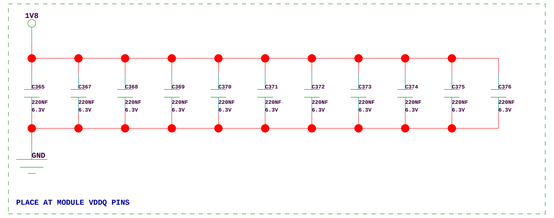


VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
PLACE ONE 10uF CAPACITOR ON EITHER END OF ISLAND

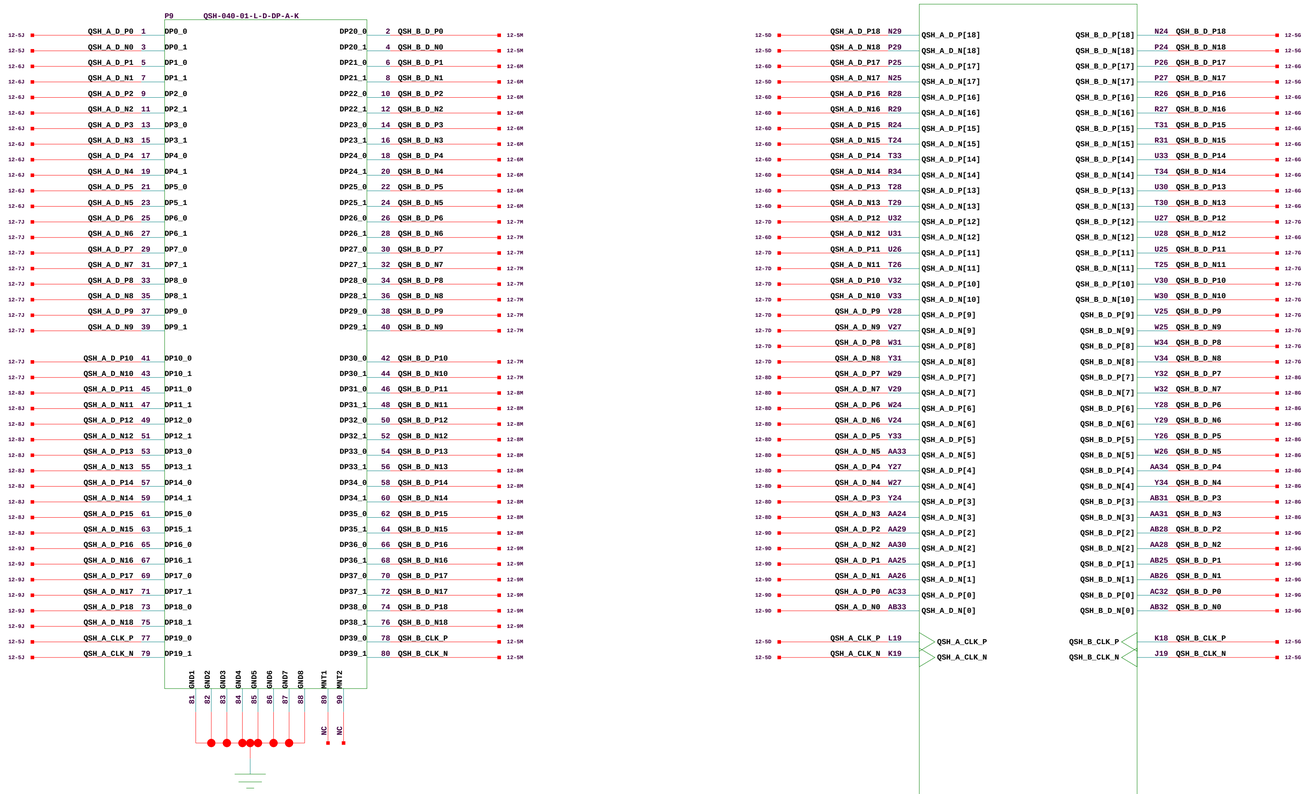








ROACH/iBOB2	ROACH_DDR2_DIMM
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-29-2008_11:08 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 11 OF 25



ROACH/iBOB2		**ROACH_DIFF_GPIO**	
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/		DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
		DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW	
		DRAWN: F KAPP	APPR:
2-29-2008_11:08		CHECKED: E BAUERMEISTER	SHEET 12 OF 25
PATH PATH			

GPIOLVC18[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

GPIOLVC25[0] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

IO VOLTAGE LEVEL SELECT	
1-2: 3.3V	DEFAULT
2-3: 2.5V	

IF CR10 IS ON, CLOCK CAPABLE GPIO'S ARE OUTPUTS

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

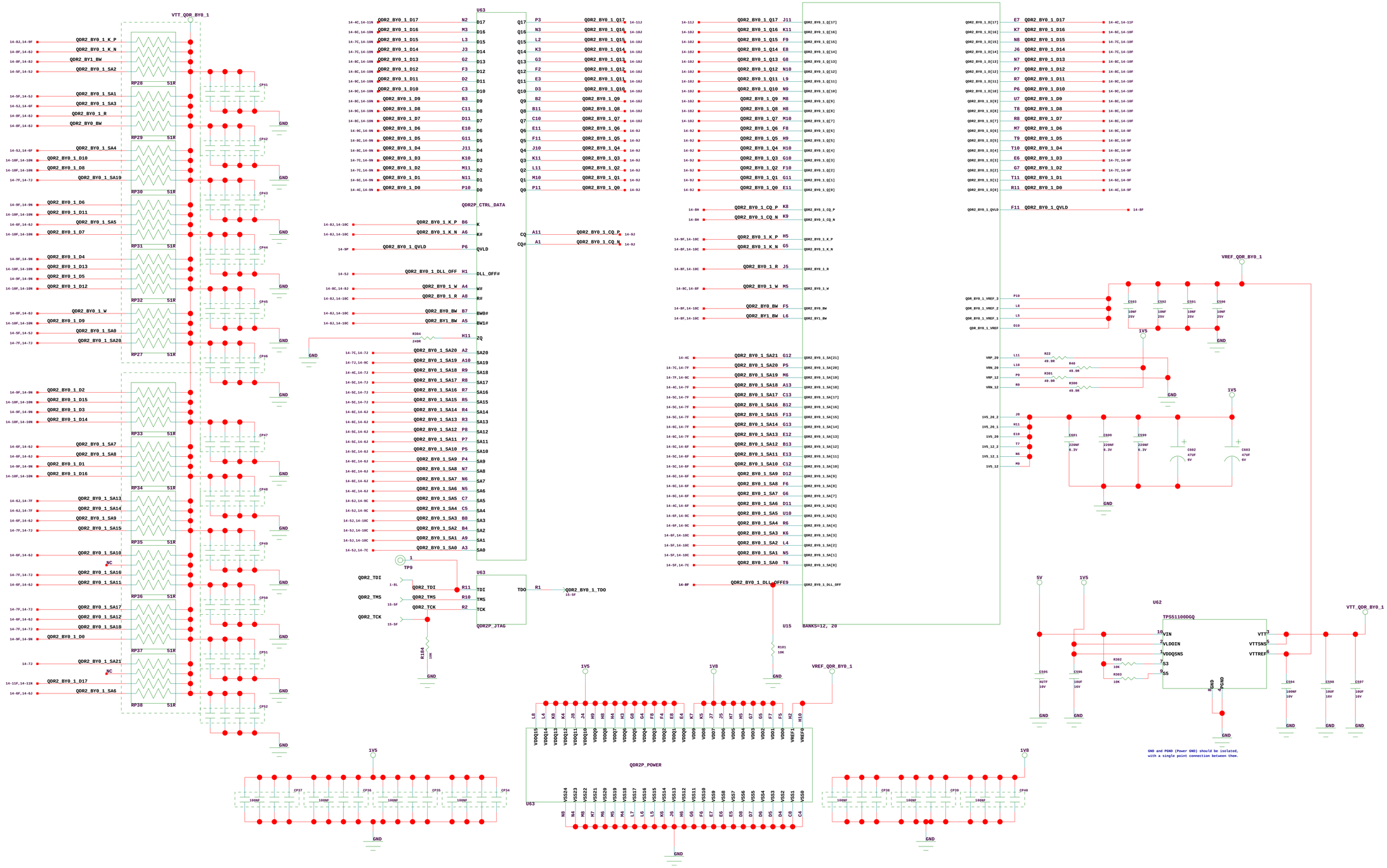
http://casper.berkeley.edu/

2-29-2008_11:08

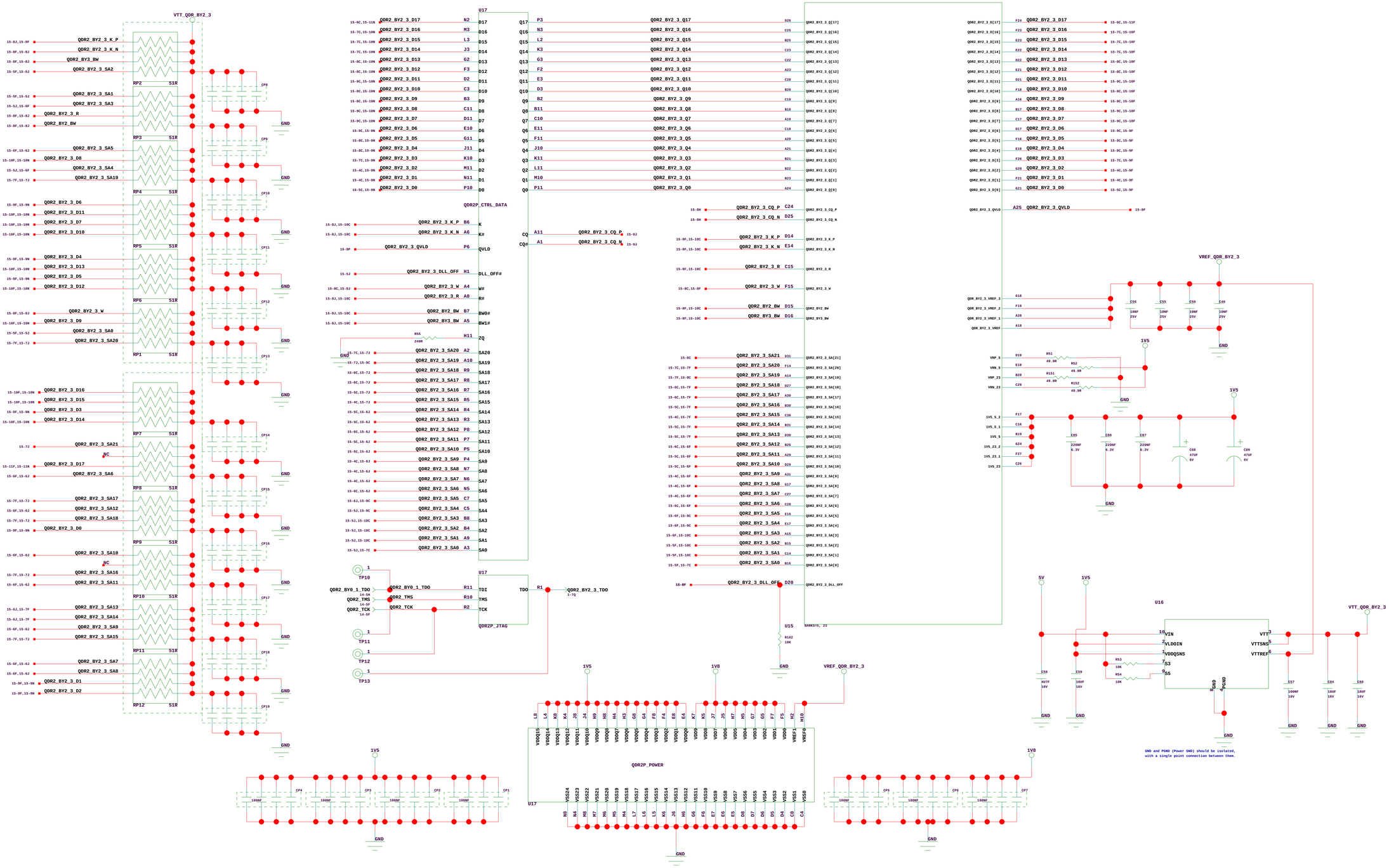
PATH PATH

ROACH_GPIO_MISC

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE MW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	13 OF 25



ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
2-29-2008_11:08 PATH PATH	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
	DRAWN: F KAPP · APPR:
	CHECKED: E BAUERMEISTER · SHEET 14 OF 25

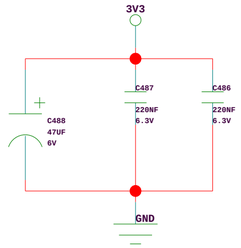


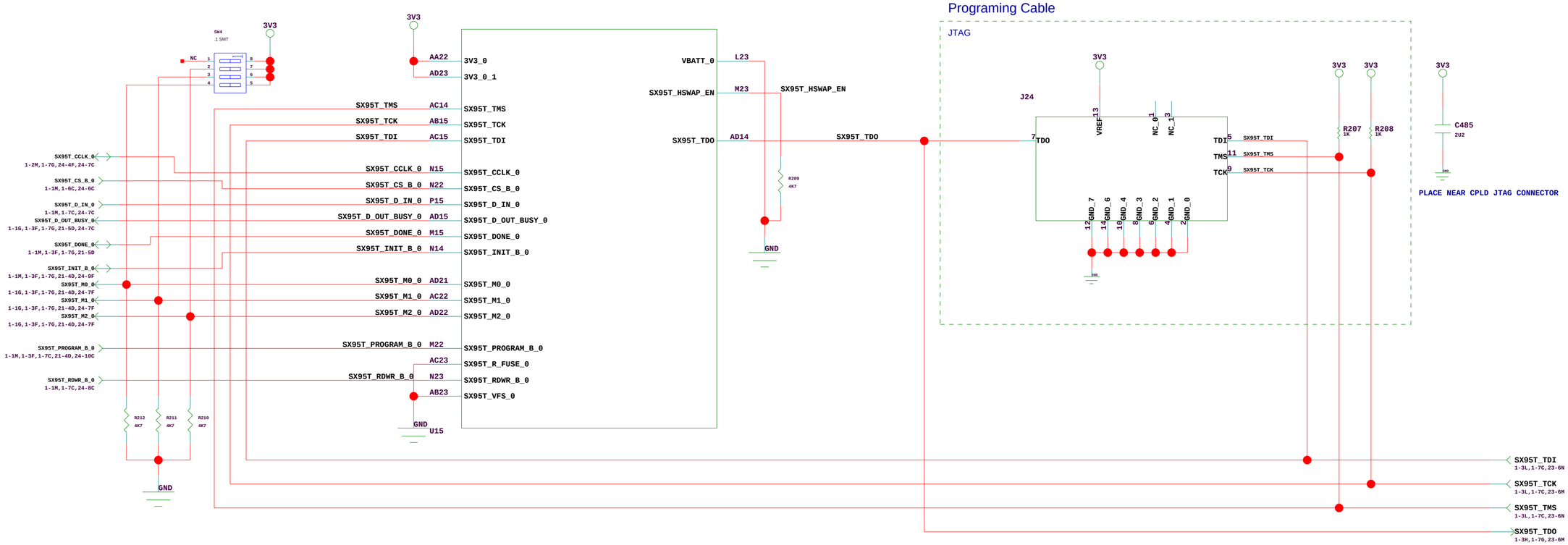
ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-29-2008_11:08	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 15 OF 25

TBD

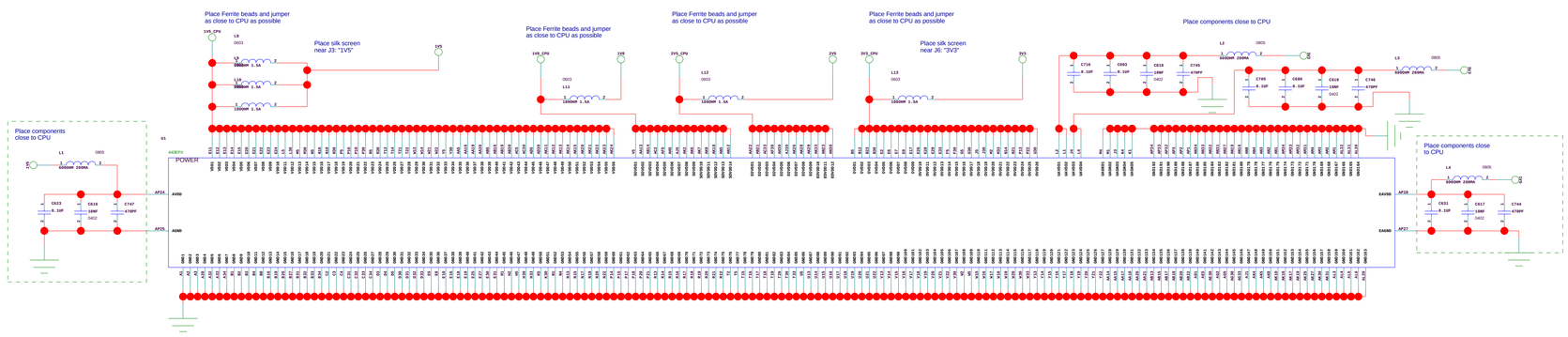
VALID CONFIGURATION MODES

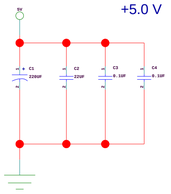
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

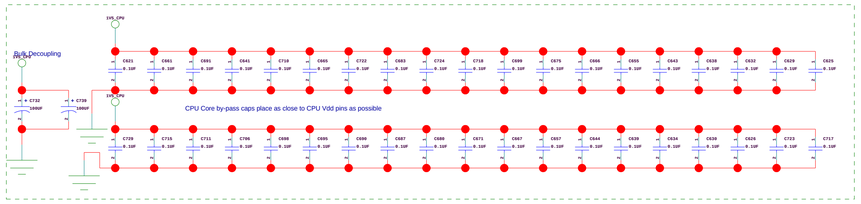


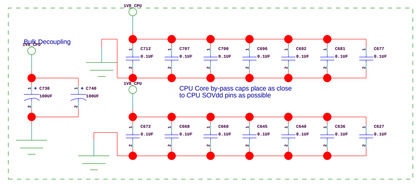


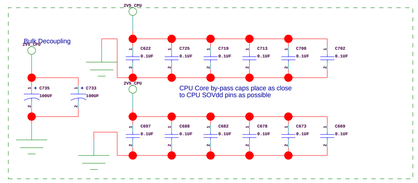
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
2-29-2008_11:08 PATH PATH	

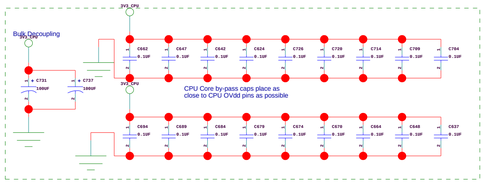


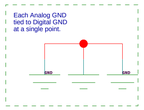










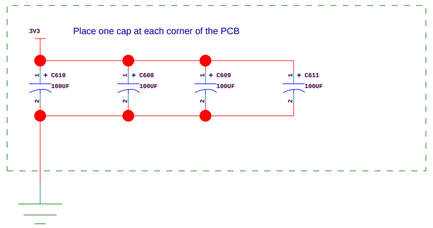


REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: **CASPER GROUP, UC BERKELEY** **NRAO, SOCORRO** **meerKAT, CAPE TOWN** http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 17 OF 25
2-29-2008_11:08 PATH PATH	

REMOVED 3V3 GENERATION



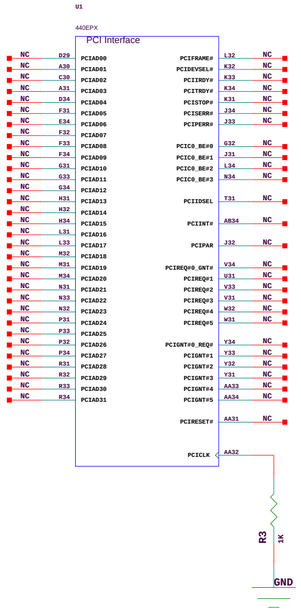
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET: 18 OF 25
2-29-2008_11:08 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-29-2008_11:08 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

Place nearest PHY pin 96

2V5 C533 10NF

Place nearest PHY pin 101

2V5 C534 10NF

Place nearest PHY pin 98

1V8 R233 1R C536 22UF C511 10NF

Place nearest PHY pin 100

1V8 R232 1R C535 22UF C512 10NF

Place as close to PHY CORE VDD power pins as possible

1V8 C526 10NF C527 100NF C525 10NF C528 100NF C530 10NF C529 100NF C531 10NF C532 100NF

Place as close to PHY IO VDD power pins as possible

2V5 C513 10NF C514 100NF C515 10NF C516 100NF C517 10NF C518 100NF C519 10NF C520 100NF C521 10NF C522 100NF C523 10NF C524 100NF

U3 440EP4 Gig-Ethernet RGMII1

UNUSED SECOND ETHERNET MAC

U1 440EP4 Gig-Ethernet RGMII0

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.
Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

ETHERNET Mgt.

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

Place jumpers in line with signals

Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5

NOSTUFF R265 2K2 R264 2K2

Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY

HFJ11-1G02E-L12

C537 22UF GND

DUPLEX LED L10 LED L100 LED

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

ROACH/iBOB2	ROACH_PPC_ETH1
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
2-29-2008_11:08 PATH PATH	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 20 OF 25

U1

USB 2.0 DEVICE

440EPX

USB2CLK — A5 — NC

GPIO28/USB2TXVAL — C6 — NC
USB2TXRDY_REFEN — B6 — NC
USB2RXACT_HOLDREQ_RCVINH — D7 — NC
USB2RXVAL_LEAKTEST2 — C8 — NC
GPIO27/USB2RXERR_EXTREQ# — A4 — SX95T_DONE_0 ↔ SX95T_DONE_0 (1-1M,1-3F,1-7G)
GPIO30/USB2XCVRSEL_EXTACK# — M3 — SX95T_INIT_B_0 ↔ SX95T_INIT_B_0 (1-1M,1-3F,1-7G,24-9F)
GPIO31/USB2TERMSEL_BUSREQ — P4
USB2LS0_DRVINH1 — R2 — NC — SX95T_M0_0 → SX95T_M0_0 (1-1G,1-3F,1-7G,16-3B,24-7F)
USB2LS1_LEAKTEST_HOLDPRI — P1 — NC
GPIO32/USB2OM0 — R3 — SX95T_M1_0 → SX95T_M1_0 (1-1G,1-3F,1-7G,16-3B,24-7F)
GPIO33/USB2OM1 — R4
GPIO29/USB2SUSP_HOLDACK — C5 — SX95T_M2_0 → SX95T_M2_0 (1-1G,1-3F,1-7G,16-3B,24-7F)
SX95T_PROGRAM_B_0 → SX95T_PROGRAM_B_0 (1-1M,1-3F,1-7C,1-3B,24-10C)

NOTE:

USB HOST ONLY

USB 2.0 PHY
HOST/DEVICE

USB2XCVR — J2 — USB2_XCVR_D+
USB2XCVR# — J1 — USB2_XCVR_D-
USB2REXT — L3 — R182 3K4 0402 — GND
USB2XTAL — N2
USB2XTAL# — N3

CLK_USB2_48MHZ (1-3B,1-3L,23-4G) — CLK_USB2_48MHZ

CRITICAL PLACEMENT

Place SP2 very close to P6

SP2 SOT23 PGB102ST23WR

PGB102ST23WR SP2

GND

5V — PTC1 1206L050 500MA — 1 — 2

C614 220UF 10V
C612 100NF 10V
C613 1NF 50V

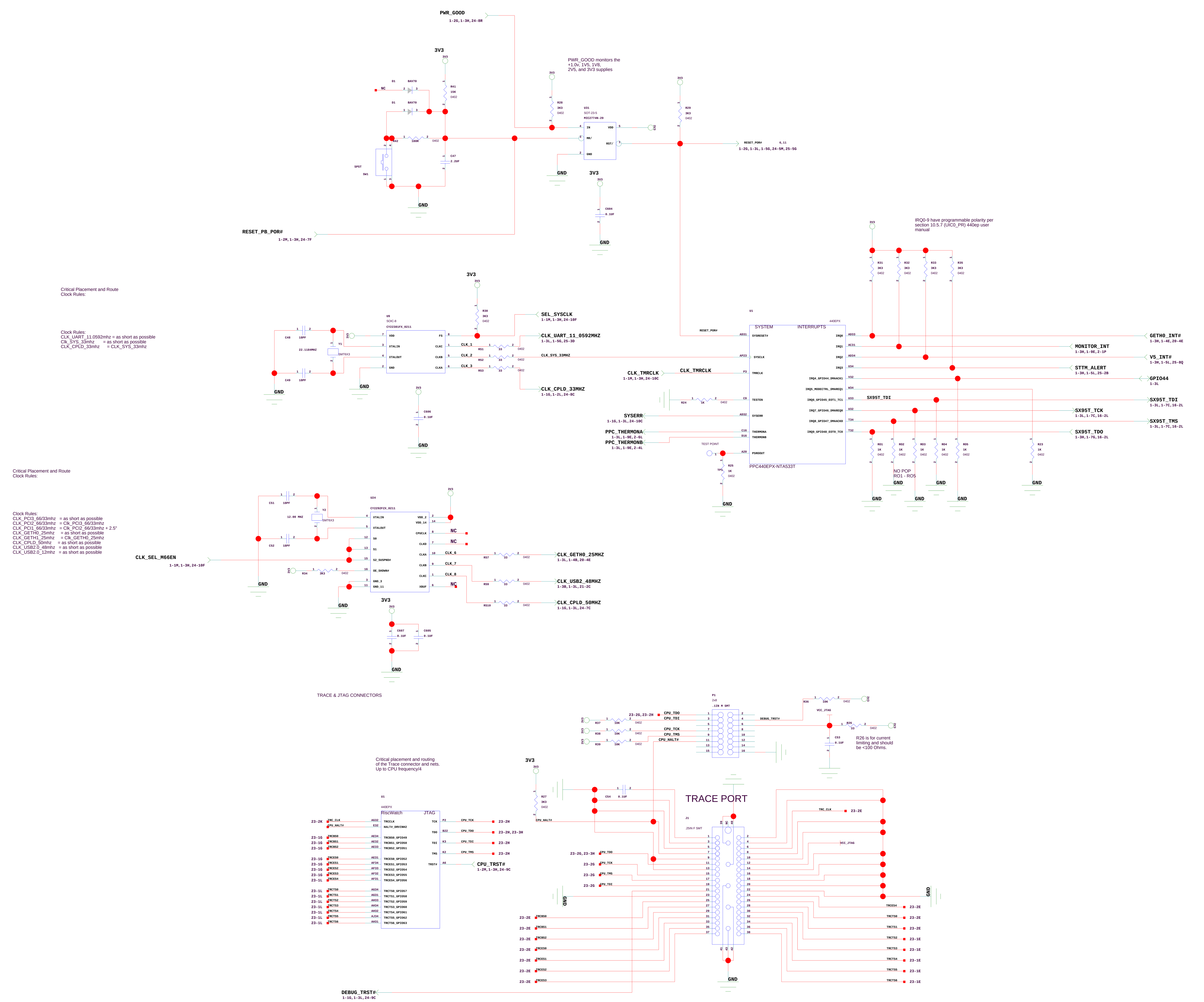
VR4 0603 5.5V 20A

P6 NONE 1X4 USBA
1 VCC
2 D-
3 D+
4 GND
5
6
292303-1

GND

ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET 21 OF 25
2-29-2008_11:08 PATH PATH	

ROACH/iBOB2	ROACH_PPC_DDR2
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-29-2008_11:08	DRAWN: F KAPP — APPR:
PATH: PATH	CHECKED: E BAUERMEISTER — SHEET 22 OF 25



PWR_GOOD
3V3
PWR_GOOD monitors the +1.0v, 1V5, 1V8, 2V5, and 3V3 supplies
RESET_PB_POR#
GND
IRQ0-9 have programmable polarity per section 10.5.7 (UIC0_PR) 440ep user manual
Critical Placement and Route Clock Rules:
Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_SYS_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz
SEL_SYSCLK
CLK_UART_11_0592MHZ
CLK_CPLD_33MHZ
CLK_TMRCLK
SYSERR
PPC_THERMONA
PPC_THERMONB
GETH0_INT#
MONITOR_INT
V5_INT#
STTM_ALERT
GPIO44
SX95T_TDI
SX95T_TCK
SX95T_TMS
SX95T_TDO
NO POP RO1 - RO5
PPC440EPX-NTA533T
Critical Placement and Route Clock Rules:
Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible
CLK_SEL_M66EN
CLK_GETH0_25MHZ
CLK_USB2_48MHZ
CLK_CPLD_50MHZ
TRACE & JTAG CONNECTORS
R26 is for current limiting and should be <100 Ohms.
Critical placement and routing of the Trace connector and nets. Up to CPU frequency/4
CPU_TRST#
TRACE PORT
DEBUG_TRST#

ROACH/iBOB2	ROACH_PPC_TST_CLK_IO	
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO NRF-ADM-XXX-SD-0001	REVISION A
	DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW	
2-29-2008_11:08	DRAWN: F KAPP	APPR:
PATH PATH	CHECKED: E BAUERMEISTER	SHEET 23 OF 25

roach_cpld_XC2C256_7VQ100C_pcb

SD/MMC/MMCPLUS CONNECTOR

J17

SDSR13-A0-0005

RESETS

CPU_TRST# = '1' when JTAG_TRST# = '1' and RESET_PORW = '1' else '0'; see errata sheet

SysErr will be used to drive Status LED (active H)

Boot Configuration

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

Configuration DIP-Swith

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

roach_cpld_XC2C256_7VQ100C_configpins

XC2C256_7VQ144C

Xilinx
Programing Cable

JTAG

PLACE NEAR CPLD JTAG CONNECTOR

ENABLE PER_CLK CONNECTION
TO CONFIGURATION I/F
MUST CO-ORDINATE WITH
SX95T_CCLK_0 AND MODE
TO AVOID CLASH

SN74AHC1G125DCKT

PLACE AT END OF DAISY CHAIN

roach_cpld_XC2C256_7VQ100C_powerpins

PLACE NEAR CPLD POWER PINS

ROACH/iBOB2	ROACH_PPC_CPLD
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-29-2008_11:08 PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 24 OF 25

ROACH/iBOB2	ROACH_PPC_NVM_SERIAL
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-29-2008_11:08	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 25 OF 25