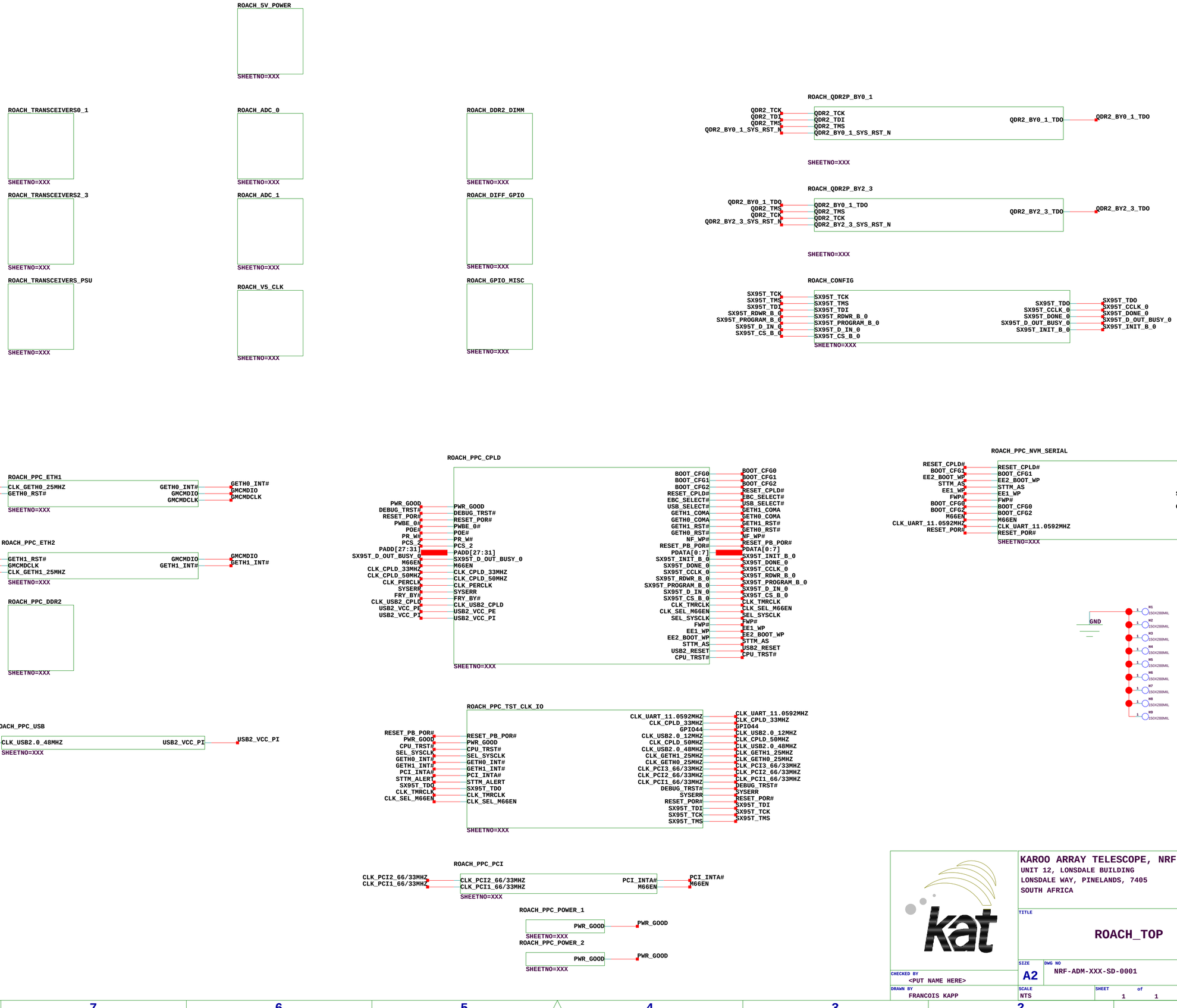


KAROO ARRAY TELESCOPE, NRF
UNIT 12, LONSDALE BUILDING
LONSDALE WAY, PINELANDS, 7405
SOUTH AFRICA

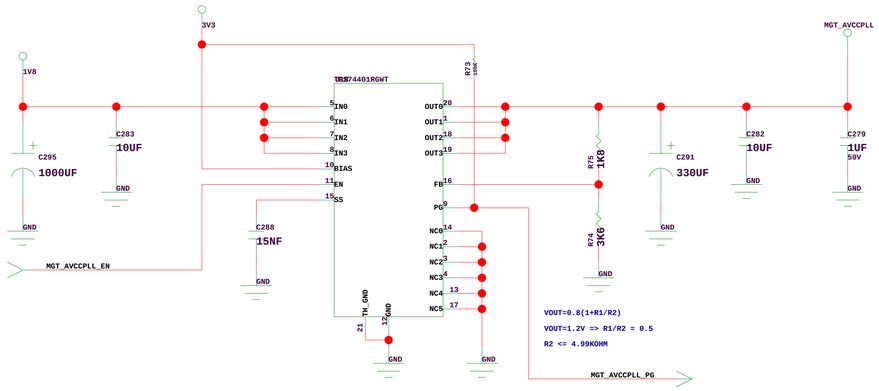
TITLE: ROACH_TOP

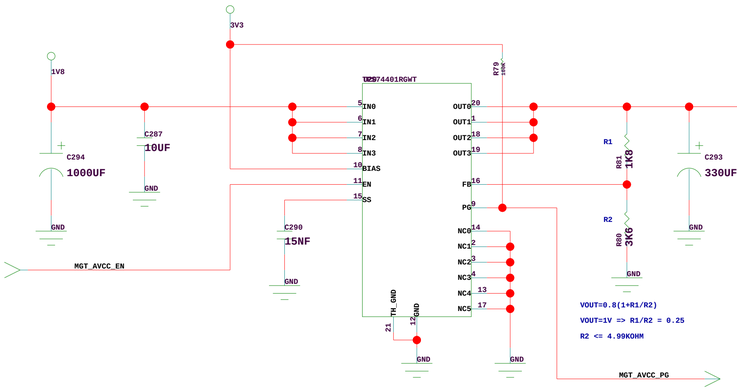
CHECKED BY: <PUT NAME HERE>	SIZE: A2	DWG NO: NRF-ADM-XXX-SD-0001
DRAWN BY: FRANCOIS KAPP	SCALE: NTS	SHEET 1 of 1

REV: A

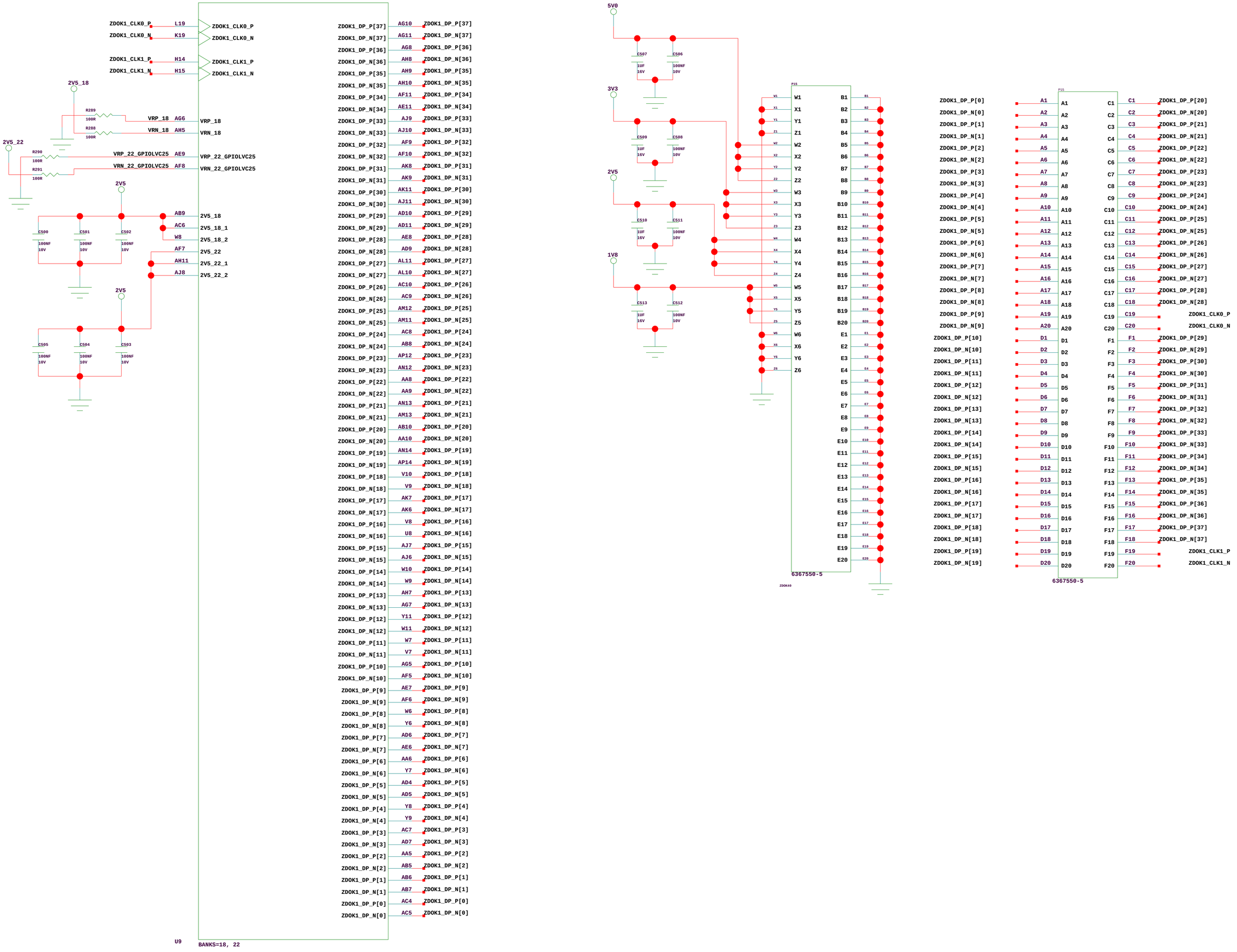
9-19-2007_13:16

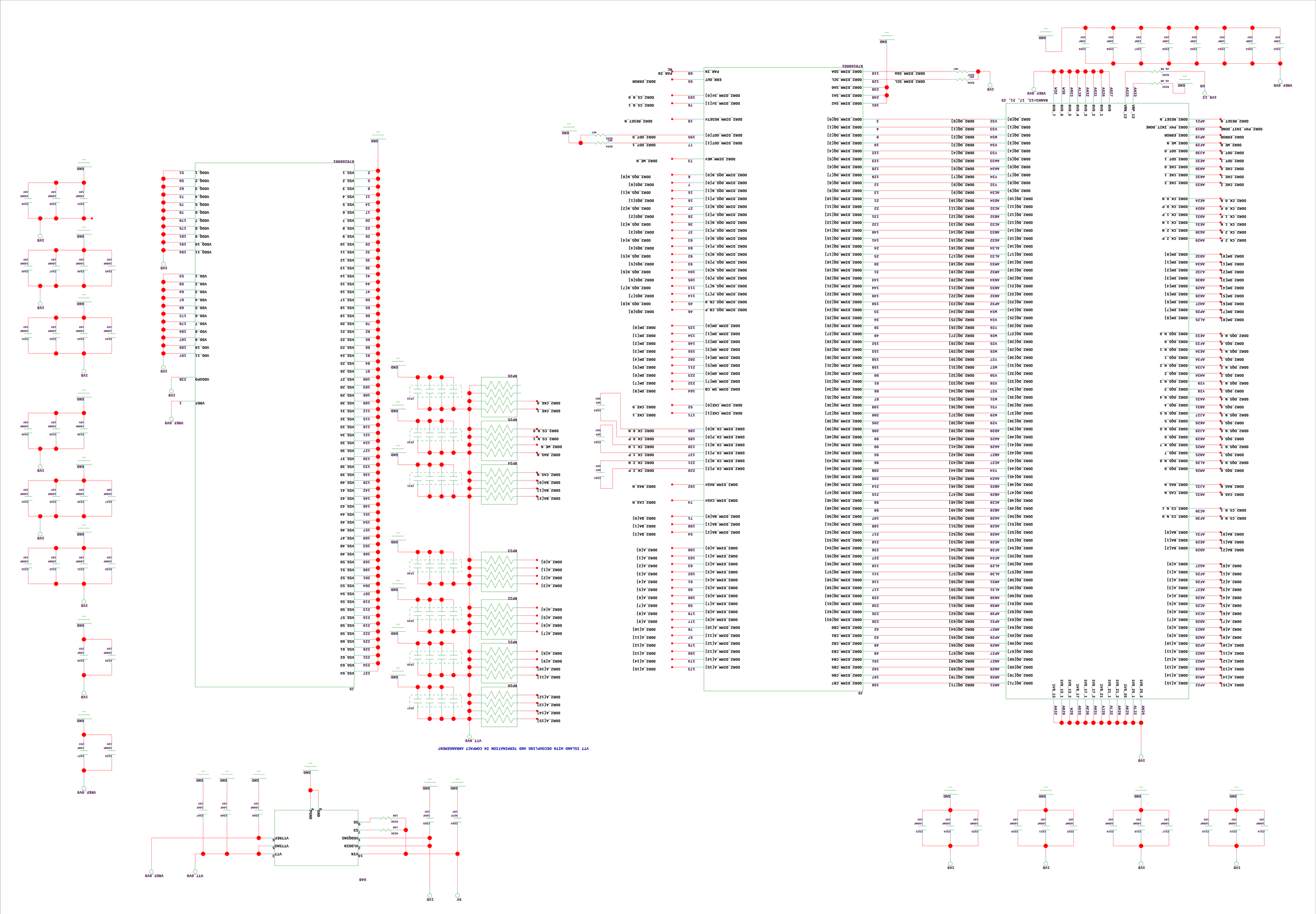
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB2 220@100M
FB3 220@100M
FB4 220@100M
C234 220NF 6.3V
C233 220NF 6.3V
C232 220NF 6.3V
C231 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
2V5
FB26 220@100M
C276 220NF 6.3V
R68 10K
X1
CCLD-023-25-156.250 156.25MHZ
JP4
OE
VCC
OUT
GND
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
C243 10NF 25V
C244 10NF 25V
C245 10NF 25V
C246 10NF 25V
C248 10NF 25V
C247 10NF 25V
MGTAVCC_112 R3
MGTAVCC_112_1 R4
MGTAVCCPLL_112 T3
MGTAVTTRX_112 N3
MGT_112_REF_CLK_P P4
MGT_112_REF_CLK_N P3
MGTRX0_112_P N1
MGTRX0_112_N P1
MGTRX1_112_P T1
MGTRX1_112_N R1
U9
MGTAVCC_112
MGTAVCC_112_1
MGTAVCCPLL_112
MGTAVTTRX_112
MGT_112_REF_CLK_P
MGT_112_REF_CLK_N
MGTRX0_112_P
MGTRX0_112_N
MGTRX1_112_P
MGTRX1_112_N
MGTRREF V4 MGTRREF
MGT_VTRXC V5 MGTAVTTRXC
MGTAVTTTX_112 M3 MGTAVTTTX_112
MGTAVTTTX_112_1 U3 MGTAVTTTX_112_1
MGTTX0_112_P M2 MGTTX0_112_P
MGTTX0_112_N N2 MGTTX0_112_N
MGTTX1_112_P U2 MGTTX1_112_P
MGTTX1_112_N T2 MGTTX1_112_N
MGT_AVTT
R67 49.9R
FB25 220@100M
FB5 220@100M
FB6 220@100M
C265 220NF 6.3V
C236 220NF 6.3V
C235 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
P6
S1 DL0P
S2 DL0N
S3 DL1P
S4 DL1N
S5 DL2P
S6 DL2N
S7 DL3P
S8 DL3N
S10 SL0P
S15 SL0N
S14 SL1P
S13 SL1N
S12 SL2P
S11 SL2N
S16 SL3P
S9 SL3N
MGTRX0_114_P
MGTRX0_114_N
MGTRX1_114_P
MGTRX1_114_N
SIG_GND1 G1
SIG_GND2 G2
SIG_GND3 G3
SIG_GND4 G4
SIG_GND5 G5
SIG_GND6 G6
SIG_GND7 G7
SIG_GND8 G8
SIG_GND9 G9
SIG_GND10 G19
ODIS
FAULT
R62 10K
C269 10NF 6.3V
FCN-268F036-G/3DB
3V3
JP2
OPTICAL MODULE FAULT - RED LED
C270 10NF 6.3V
R69 5K1
R58 3K9
U15
MAX9032AKA
R60 6K8
U14
MAX9032AKA
C266 10NF 6.3V
R59 3K9
U16
AND2
SN74AHC1G08DCKR
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB11 220@100M
FB12 220@100M
FB9 220@100M
FB10 220@100M
C242 220NF 6.3V
C241 220NF 6.3V
C240 220NF 6.3V
C239 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_114 AA3
MGTAVCC_114_1 AA4
MGTAVCCPLL_114 AB3
MGTAVTTRX_114 W3
MGT_114_REF_CLK_P NC Y4
MGT_114_REF_CLK_N NC Y3
MGTRX0_114_P W1
MGTRX0_114_N Y1
MGTRX1_114_P AB1
MGTRX1_114_N AA1
U9
MGTAVCC_114
MGTAVCC_114_1
MGTAVCCPLL_114
MGTAVTTRX_114
MGT_114_REF_CLK_P
MGT_114_REF_CLK_N
MGTRX0_114_P
MGTRX0_114_N
MGTRX1_114_P
MGTRX1_114_N
MGTAVTTTX_114 AC3 MGTAVTTTX_114
MGTAVTTTX_114_1 V3 MGTAVTTTX_114_1
MGTTX0_114_P V2 MGTTX0_114_P
MGTTX0_114_N W2 MGTTX0_114_N
MGTTX1_114_P AC2 MGTTX1_114_P
MGTTX1_114_N AB2 MGTTX1_114_N
MGTTREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT
MGT_AVTT
FB8 220@100M
FB7 220@100M
C237 220NF 6.3V
C238 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
P6
S19 DL0P
S20 DL0N
S21 DL1P
S22 DL1N
S23 DL2P
S24 DL2N
S25 DL3P
S26 DL3N
S34 SL0P
S33 SL0N
S32 SL1P
S31 SL1N
S30 SL2P
S29 SL2N
S28 SL3P
S27 SL3N
MGTRX0_114_P
MGTRX0_114_N
MGTRX1_114_P
MGTRX1_114_N
SIG_GND1 G10
SIG_GND2 G11
SIG_GND3 G12
SIG_GND4 G13
SIG_GND5 G14
SIG_GND6 G15
SIG_GND7 G16
SIG_GND8 G17
SIG_GND9 G18
SIG_GND10 G19
ODIS
FAULT
R63 10K
C273 10NF 6.3V
FCN-268F036-G/3DB
3V3
JP3
OPTICAL MODULE FAULT - RED LED
C271 10NF 6.3V
R70 5K1
R65 3K9
U15
MAX9032AKA
R66 6K8
U14
MAX9032AKA
C272 10NF 6.3V
R67 3K9
U17
AND2
SN74AHC1G08DCKR
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB22 220@100M
FB21 220@100M
FB24 220@100M
FB23 220@100M
C262 220NF 6.3V
C263 220NF 6.3V
C253 220NF 6.3V
C264 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_118 AG3
MGTAVCC_118_1 AG4
MGTAVCCPLL_118 AH3
MGTAVTTRX_118 AE3
MGT_118_REF_CLK_P NC AF4
MGT_118_REF_CLK_N NC AF3
MGTRX0_118_P AE1
MGTRX0_118_N AF1
MGTRX1_118_P AH1
MGTRX1_118_N AG1
U9
MGTAVCC_118
MGTAVCC_118_1
MGTAVCCPLL_118
MGTAVTTRX_118
MGT_118_REF_CLK_P
MGT_118_REF_CLK_N
MGTRX0_118_P
MGTRX0_118_N
MGTRX1_118_P
MGTRX1_118_N
MGTAVTTTX_118_1 AJ3 MGTAVTTTX_118_1
MGTAVTTTX_118 AD3 MGTAVTTTX_118
MGTTX0_118_P AD2 MGTTX0_118_P
MGTTX0_118_N AE2 MGTTX0_118_N
MGTTX1_118_P AJ2 MGTTX1_118_P
MGTTX1_118_N AH2 MGTTX1_118_N
MGT_AVTT
FB19 220@100M
FB20 220@100M
C261 220NF 6.3V
C260 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
P6
S19 DL0P
S20 DL0N
S21 DL1P
S22 DL1N
S23 DL2P
S24 DL2N
S25 DL3P
S26 DL3N
S34 SL0P
S33 SL0N
S32 SL1P
S31 SL1N
S30 SL2P
S29 SL2N
S28 SL3P
S27 SL3N
MGTRX0_116_P
MGTRX0_116_N
MGTRX1_116_P
MGTRX1_116_N
SIG_GND1 G10
SIG_GND2 G11
SIG_GND3 G12
SIG_GND4 G13
SIG_GND5 G14
SIG_GND6 G15
SIG_GND7 G16
SIG_GND8 G17
SIG_GND9 G18
SIG_GND10 G19
ODIS
FAULT
R64 10K
C273 10NF 6.3V
FCN-268F036-G/3DB
3V3
JP3
OPTICAL MODULE FAULT - RED LED
C271 10NF 6.3V
R70 5K1
R65 3K9
U15
MAX9032AKA
R66 6K8
U14
MAX9032AKA
C272 10NF 6.3V
R67 3K9
U17
AND2
SN74AHC1G08DCKR
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB17 220@100M
FB18 220@100M
FB15 220@100M
FB16 220@100M
C259 220NF 6.3V
C258 220NF 6.3V
C257 220NF 6.3V
C254 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
C249 10NF 25V
C250 10NF 25V
C251 10NF 25V
C252 10NF 25V
MGTAVCC_116 J3
MGTAVCC_116_1 J4
MGTAVCCPLL_116 K3
MGTAVTTRX_116 G3
MGT_116_REF_CLK_P NC H4
MGT_116_REF_CLK_N NC H3
MGTRX0_116_P G1
MGTRX0_116_N H1
MGTRX1_116_P K1
MGTRX1_116_N J1
U9
MGTAVCC_116
MGTAVCC_116_1
MGTAVCCPLL_116
MGTAVTTRX_116
MGT_116_REF_CLK_P
MGT_116_REF_CLK_N
MGTRX0_116_P
MGTRX0_116_N
MGTRX1_116_P
MGTRX1_116_N
MGTAVTTTX_116_1 L3 MGTAVTTTX_116_1
MGTAVTTTX_116 F3 MGTAVTTTX_116
MGTTX0_116_P F2 MGTTX0_116_P
MGTTX0_116_N G2 MGTTX0_116_N
MGTTX1_116_P L2 MGTTX1_116_P
MGTTX1_116_N K2 MGTTX1_116_N
MGT_AVTT
FB14 220@100M
FB13 220@100M
C255 220NF 6.3V
C256 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
P6
S19 DL0P
S20 DL0N
S21 DL1P
S22 DL1N
S23 DL2P
S24 DL2N
S25 DL3P
S26 DL3N
S34 SL0P
S33 SL0N
S32 SL1P
S31 SL1N
S30 SL2P
S29 SL2N
S28 SL3P
S27 SL3N
MGTRX0_116_P
MGTRX0_116_N
MGTRX1_116_P
MGTRX1_116_N
SIG_GND1 G10
SIG_GND2 G11
SIG_GND3 G12
SIG_GND4 G13
SIG_GND5 G14
SIG_GND6 G15
SIG_GND7 G16
SIG_GND8 G17
SIG_GND9 G18
SIG_GND10 G19
ODIS
FAULT
R61 10K
C269 10NF 6.3V
FCN-268F036-G/3DB
3V3
JP2
OPTICAL MODULE FAULT - RED LED
C270 10NF 6.3V
R69 5K1
R58 3K9
U15
MAX9032AKA
R60 6K8
U14
MAX9032AKA
C266 10NF 6.3V
R59 3K9
U16
AND2
SN74AHC1G08DCKR
3V3
U12
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
TPS2031D
R71 10K
C268 10NF 6.3V
C267 100NF 6.3V
C277 4.7UF 16V
C229 22UF 16V
3V3
U13
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
TPS2031D
R72 10K
C274 10NF 6.3V
C275 100NF 6.3V
C278 4.7UF 16V
C230 22UF 16V

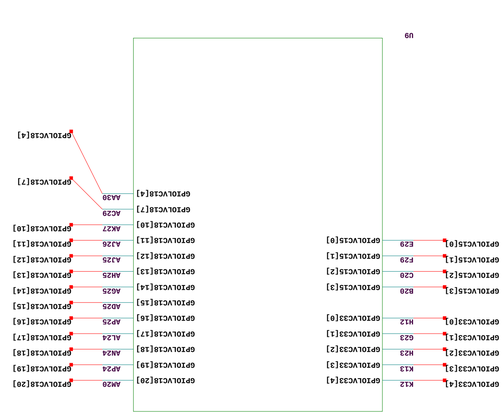

3V3
1V8
MGT_AVCCPLL
U57
TPS74401RGWT
R73
10K
C295
1000UF
C283
10UF
C288
15NF
C291
330UF
C282
10UF
C279
1UF
50V
R75
1K8
R74
3K6
IN0
IN1
IN2
IN3
BIAS
EN
SS
OUT0
OUT1
OUT2
OUT3
FB
PG
NC0
NC1
NC2
NC3
NC4
NC5
TH_GND
GND
MGT_AVCCPLL_EN
MGT_AVCCPLL_PG
VOUT=0.8(1+R1/R2)
VOUT=1.2V => R1/R2 = 0.5
R2 <= 4.99KOHM

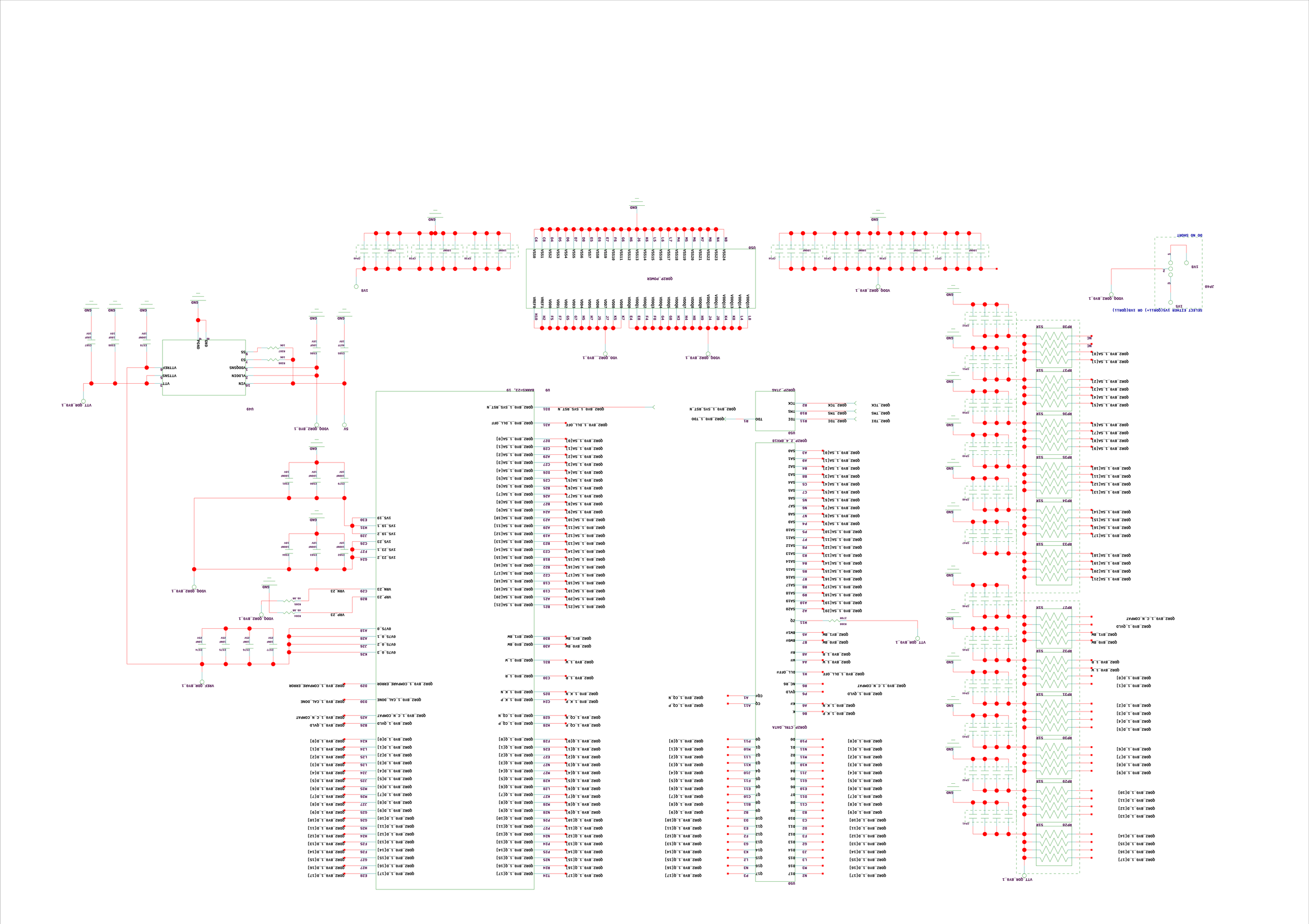

3V3
1V8
MGT_AVCC
U58
TPS74401RGWT
R79
10K
C294
1000UF
C287
10UF
C290
15NF
C293
330UF
C286
10UF
C281
1UF
50V
R1
R81
1K8
R2
R80
3K6
IN0
IN1
IN2
IN3
BIAS
EN
SS
OUT0
OUT1
OUT2
OUT3
FB
PG
NC0
NC1
NC2
NC3
NC4
NC5
TH_GND
GND
MGT_AVCC_EN
MGT_AVCC_PG
VOUT=0.8(1+R1/R2)
VOUT=1V => R1/R2 = 0.25
R2 <= 4.99KOHM

3V3
1V8
MGT_AVTT
U56
TPS74401RGWT
R78
10K
C296
1000UF
C284
10UF
C289
15NF
C292
330UF
C285
10UF
C280
1UF
50V
R76
1K8
R77
3K6
IN0
IN1
IN2
IN3
BIAS
EN
SS
OUT0
OUT1
OUT2
OUT3
FB
PG
NC0
NC1
NC2
NC3
NC4
NC5
TH_GND
GND
MGT_AVTTX_EN
MGT_AVTTX_PG
VOUT=0.8(1+R1/R2)
VOUT=1.2V => R1/R2 = 0.5
R2 <= 4.99KOHM


ZDOK1_CLK0_P L19 ZDOK1_CLK0_P
ZDOK1_CLK0_N K19 ZDOK1_CLK0_N
ZDOK1_CLK1_P H14 ZDOK1_CLK1_P
ZDOK1_CLK1_N H15 ZDOK1_CLK1_N
2V5_18
R289 100R
R288 100R
VRP_18 AG6 VRP_18
VRN_18 AH5 VRN_18
2V5_22
R290 100R
R291 100R
VRP_22_GPIOLVC25 AE9 VRP_22_GPIOLVC25
VRN_22_GPIOLVC25 AF8 VRN_22_GPIOLVC25
2V5
C500 C501 C502 100NF 10V
AB9 2V5_18
AC6 2V5_18_1
W8 2V5_18_2
AF7 2V5_22
AH11 2V5_22_1
AJ8 2V5_22_2
C505 C504 C503 100NF 10V
ZDOK1_DP_P[37] AG10 ZDOK1_DP_P[37]
ZDOK1_DP_N[37] AG11 ZDOK1_DP_N[37]
ZDOK1_DP_P[36] AG8 ZDOK1_DP_P[36]
ZDOK1_DP_N[36] AH8 ZDOK1_DP_N[36]
ZDOK1_DP_P[35] AH9 ZDOK1_DP_P[35]
ZDOK1_DP_N[35] AH10 ZDOK1_DP_N[35]
ZDOK1_DP_P[34] AF11 ZDOK1_DP_P[34]
ZDOK1_DP_N[34] AE11 ZDOK1_DP_N[34]
ZDOK1_DP_P[33] AJ9 ZDOK1_DP_P[33]
ZDOK1_DP_N[33] AJ10 ZDOK1_DP_N[33]
ZDOK1_DP_P[32] AF9 ZDOK1_DP_P[32]
ZDOK1_DP_N[32] AF10 ZDOK1_DP_N[32]
ZDOK1_DP_P[31] AK8 ZDOK1_DP_P[31]
ZDOK1_DP_N[31] AK9 ZDOK1_DP_N[31]
ZDOK1_DP_P[30] AK11 ZDOK1_DP_P[30]
ZDOK1_DP_N[30] AJ11 ZDOK1_DP_N[30]
ZDOK1_DP_P[29] AD10 ZDOK1_DP_P[29]
ZDOK1_DP_N[29] AD11 ZDOK1_DP_N[29]
ZDOK1_DP_P[28] AE8 ZDOK1_DP_P[28]
ZDOK1_DP_N[28] AD9 ZDOK1_DP_N[28]
ZDOK1_DP_P[27] AL11 ZDOK1_DP_P[27]
ZDOK1_DP_N[27] AL10 ZDOK1_DP_N[27]
ZDOK1_DP_P[26] AC10 ZDOK1_DP_P[26]
ZDOK1_DP_N[26] AC9 ZDOK1_DP_N[26]
ZDOK1_DP_P[25] AM12 ZDOK1_DP_P[25]
ZDOK1_DP_N[25] AM11 ZDOK1_DP_N[25]
ZDOK1_DP_P[24] AC8 ZDOK1_DP_P[24]
ZDOK1_DP_N[24] AB8 ZDOK1_DP_N[24]
ZDOK1_DP_P[23] AP12 ZDOK1_DP_P[23]
ZDOK1_DP_N[23] AN12 ZDOK1_DP_N[23]
ZDOK1_DP_P[22] AA8 ZDOK1_DP_P[22]
ZDOK1_DP_N[22] AA9 ZDOK1_DP_N[22]
ZDOK1_DP_P[21] AN13 ZDOK1_DP_P[21]
ZDOK1_DP_N[21] AM13 ZDOK1_DP_N[21]
ZDOK1_DP_P[20] AB10 ZDOK1_DP_P[20]
ZDOK1_DP_N[20] AA10 ZDOK1_DP_N[20]
ZDOK1_DP_P[19] AN14 ZDOK1_DP_P[19]
ZDOK1_DP_N[19] AP14 ZDOK1_DP_N[19]
ZDOK1_DP_P[18] V10 ZDOK1_DP_P[18]
ZDOK1_DP_N[18] V9 ZDOK1_DP_N[18]
ZDOK1_DP_P[17] AK7 ZDOK1_DP_P[17]
ZDOK1_DP_N[17] AK6 ZDOK1_DP_N[17]
ZDOK1_DP_P[16] V8 ZDOK1_DP_P[16]
ZDOK1_DP_N[16] U8 ZDOK1_DP_N[16]
ZDOK1_DP_P[15] AJ7 ZDOK1_DP_P[15]
ZDOK1_DP_N[15] AJ6 ZDOK1_DP_N[15]
ZDOK1_DP_P[14] W10 ZDOK1_DP_P[14]
ZDOK1_DP_N[14] W9 ZDOK1_DP_N[14]
ZDOK1_DP_P[13] AH7 ZDOK1_DP_P[13]
ZDOK1_DP_N[13] AG7 ZDOK1_DP_N[13]
ZDOK1_DP_P[12] Y11 ZDOK1_DP_P[12]
ZDOK1_DP_N[12] W11 ZDOK1_DP_N[12]
ZDOK1_DP_P[11] W7 ZDOK1_DP_P[11]
ZDOK1_DP_N[11] V7 ZDOK1_DP_N[11]
ZDOK1_DP_P[10] AG5 ZDOK1_DP_P[10]
ZDOK1_DP_N[10] AF5 ZDOK1_DP_N[10]
ZDOK1_DP_P[9] AE7 ZDOK1_DP_P[9]
ZDOK1_DP_N[9] AF6 ZDOK1_DP_N[9]
ZDOK1_DP_P[8] W6 ZDOK1_DP_P[8]
ZDOK1_DP_N[8] Y6 ZDOK1_DP_N[8]
ZDOK1_DP_P[7] AD6 ZDOK1_DP_P[7]
ZDOK1_DP_N[7] AE6 ZDOK1_DP_N[7]
ZDOK1_DP_P[6] AA6 ZDOK1_DP_P[6]
ZDOK1_DP_N[6] Y7 ZDOK1_DP_N[6]
ZDOK1_DP_P[5] AD4 ZDOK1_DP_P[5]
ZDOK1_DP_N[5] AD5 ZDOK1_DP_N[5]
ZDOK1_DP_P[4] Y8 ZDOK1_DP_P[4]
ZDOK1_DP_N[4] Y9 ZDOK1_DP_N[4]
ZDOK1_DP_P[3] AC7 ZDOK1_DP_P[3]
ZDOK1_DP_N[3] AD7 ZDOK1_DP_N[3]
ZDOK1_DP_P[2] AA5 ZDOK1_DP_P[2]
ZDOK1_DP_N[2] AB5 ZDOK1_DP_N[2]
ZDOK1_DP_P[1] AB6 ZDOK1_DP_P[1]
ZDOK1_DP_N[1] AB7 ZDOK1_DP_N[1]
ZDOK1_DP_P[0] AC4 ZDOK1_DP_P[0]
ZDOK1_DP_N[0] AC5 ZDOK1_DP_N[0]
U9
BANKS=18, 22
5V0
3V3
2V5
1V8
C507 C506 1UF 16V 100NF 10V
C509 C508 1UF 16V 100NF 10V
C510 C511 1UF 16V 100NF 10V
C513 C512 1UF 16V 100NF 10V
P15
W1 X1 Y1 Z1 W2 X2 Y2 Z2 W3 X3 Y3 Z3 W4 X4 Y4 Z4 W5 X5 Y5 Z5 W6 X6 Y6 Z6
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20
6367550-5
ZDOK40
ZDOK1_DP_P[0] A1 A1 C1 C1 ZDOK1_DP_P[20]
ZDOK1_DP_N[0] A2 A2 C2 C2 ZDOK1_DP_N[20]
ZDOK1_DP_P[1] A3 A3 C3 C3 ZDOK1_DP_P[21]
ZDOK1_DP_N[1] A4 A4 C4 C4 ZDOK1_DP_N[21]
ZDOK1_DP_P[2] A5 A5 C5 C5 ZDOK1_DP_P[22]
ZDOK1_DP_N[2] A6 A6 C6 C6 ZDOK1_DP_N[22]
ZDOK1_DP_P[3] A7 A7 C7 C7 ZDOK1_DP_P[23]
ZDOK1_DP_N[3] A8 A8 C8 C8 ZDOK1_DP_N[23]
ZDOK1_DP_P[4] A9 A9 C9 C9 ZDOK1_DP_P[24]
ZDOK1_DP_N[4] A10 A10 C10 C10 ZDOK1_DP_N[24]
ZDOK1_DP_P[5] A11 A11 C11 C11 ZDOK1_DP_P[25]
ZDOK1_DP_N[5] A12 A12 C12 C12 ZDOK1_DP_N[25]
ZDOK1_DP_P[6] A13 A13 C13 C13 ZDOK1_DP_P[26]
ZDOK1_DP_N[6] A14 A14 C14 C14 ZDOK1_DP_N[26]
ZDOK1_DP_P[7] A15 A15 C15 C15 ZDOK1_DP_P[27]
ZDOK1_DP_N[7] A16 A16 C16 C16 ZDOK1_DP_N[27]
ZDOK1_DP_P[8] A17 A17 C17 C17 ZDOK1_DP_P[28]
ZDOK1_DP_N[8] A18 A18 C18 C18 ZDOK1_DP_N[28]
ZDOK1_DP_P[9] A19 A19 C19 ZDOK1_CLK0_P
ZDOK1_DP_N[9] A20 A20 C20 ZDOK1_CLK0_N
ZDOK1_DP_P[10] D1 D1 F1 ZDOK1_DP_P[29]
ZDOK1_DP_N[10] D2 D2 F2 ZDOK1_DP_N[29]
ZDOK1_DP_P[11] D3 D3 F3 ZDOK1_DP_P[30]
ZDOK1_DP_N[11] D4 D4 F4 ZDOK1_DP_N[30]
ZDOK1_DP_P[12] D5 D5 F5 ZDOK1_DP_P[31]
ZDOK1_DP_N[12] D6 D6 F6 ZDOK1_DP_N[31]
ZDOK1_DP_P[13] D7 D7 F7 ZDOK1_DP_P[32]
ZDOK1_DP_N[13] D8 D8 F8 ZDOK1_DP_N[32]
ZDOK1_DP_P[14] D9 D9 F9 ZDOK1_DP_P[33]
ZDOK1_DP_N[14] D10 D10 F10 ZDOK1_DP_N[33]
ZDOK1_DP_P[15] D11 D11 F11 ZDOK1_DP_P[34]
ZDOK1_DP_N[15] D12 D12 F12 ZDOK1_DP_N[34]
ZDOK1_DP_P[16] D13 D13 F13 ZDOK1_DP_P[35]
ZDOK1_DP_N[16] D14 D14 F14 ZDOK1_DP_N[35]
ZDOK1_DP_P[17] D15 D15 F15 ZDOK1_DP_P[36]
ZDOK1_DP_N[17] D16 D16 F16 ZDOK1_DP_N[36]
ZDOK1_DP_P[18] D17 D17 F17 ZDOK1_DP_P[37]
ZDOK1_DP_N[18] D18 D18 F18 ZDOK1_DP_N[37]
ZDOK1_DP_P[19] D19 D19 F19 ZDOK1_CLK1_P
ZDOK1_DP_N[19] D20 D20 F20 ZDOK1_CLK1_N
P15
6367550-5


VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
BANKS=13, 17, 21, 25
VREF_0V9
VTT_0V9
1V8
GND
5V
U48
J9


U9
GPIOLVC18[4]
GPIOLVC18[7]
AA30
AC29
GPIOLVC18[10]
AK27
GPIOLVC18[11]
AJ26
GPIOLVC18[12]
AJ25
GPIOLVC18[13]
AH25
GPIOLVC18[14]
AG25
GPIOLVC18[15]
AD25
GPIOLVC18[16]
AP25
GPIOLVC18[17]
AL24
GPIOLVC18[18]
AN24
GPIOLVC18[19]
AP24
GPIOLVC18[20]
AM20
GPIOLVC18[4]
GPIOLVC18[7]
GPIOLVC18[10]
GPIOLVC18[11]
GPIOLVC18[12]
GPIOLVC18[13]
GPIOLVC18[14]
GPIOLVC18[15]
GPIOLVC18[16]
GPIOLVC18[17]
GPIOLVC18[18]
GPIOLVC18[19]
GPIOLVC18[20]
GPIOLVC15[0]
E29
GPIOLVC15[1]
F29
GPIOLVC15[2]
C29
GPIOLVC15[3]
B29
GPIOLVC33[0]
M12
GPIOLVC33[1]
G23
GPIOLVC33[2]
H23
GPIOLVC33[3]
K13
GPIOLVC33[4]
K12
GPIOLVC15[0]
GPIOLVC15[1]
GPIOLVC15[2]
GPIOLVC15[3]
GPIOLVC33[0]
GPIOLVC33[1]
GPIOLVC33[2]
GPIOLVC33[3]
GPIOLVC33[4]


DO NOT SHORT
JP40
1V8
SELECT EITHER 1V5(QDR11+) OR 1V8(QDR11)
1V5
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GND
VTT_QDR_BV0_1
QDR2_BV0_1_DQ[0]
QDR2_BV0_1_DQ[1]
QDR2_BV0_1_DQ[2]
QDR2_BV0_1_DQ[3]
QDR2_BV0_1_DQ[4]
QDR2_BV0_1_DQ[5]
QDR2_BV0_1_DQ[6]
QDR2_BV0_1_DQ[7]
QDR2_BV0_1_DQ[8]
QDR2_BV0_1_DQ[9]
QDR2_BV0_1_DQ[10]
QDR2_BV0_1_DQ[11]
QDR2_BV0_1_DQ[12]
QDR2_BV0_1_DQ[13]
QDR2_BV0_1_DQ[14]
QDR2_BV0_1_DQ[15]
QDR2_BV0_1_DQ[16]
QDR2_BV0_1_DQ[17]
QDR2_BV0_1_SA[0]
QDR2_BV0_1_SA[1]
QDR2_BV0_1_SA[2]
QDR2_BV0_1_SA[3]
QDR2_BV0_1_SA[4]
QDR2_BV0_1_SA[5]
QDR2_BV0_1_SA[6]
QDR2_BV0_1_SA[7]
QDR2_BV0_1_SA[8]
QDR2_BV0_1_SA[9]
QDR2_BV0_1_SA[10]
QDR2_BV0_1_SA[11]
QDR2_BV0_1_SA[12]
QDR2_BV0_1_SA[13]
QDR2_BV0_1_SA[14]
QDR2_BV0_1_SA[15]
QDR2_BV0_1_SA[16]
QDR2_BV0_1_SA[17]
QDR2_BV0_1_SA[18]
QDR2_BV0_1_SA[19]
QDR2_BV0_1_SA[20]
QDR2_BV0_1_SA[21]
QDR2_BV0_1_C_N_COMPAT
QDR2_BV0_1_QVLD
QDR2_BV0_1_BW
QDR2_BV0_1_K
QDR2_BV0_1_K_N
QDR2_BV0_1_K_P
QDR2_BV0_1_LD
QDR2_BV0_1_R
QDR2_BV0_1_W
QDR2_BV0_1_DLL_OFF
QDR2_BV0_1_SYS_RST_N
QDR2_TDI
QDR2_TMS
QDR2_TCK
TDO
R1
QDR2_BV0_1_TDO
QDR2P_JTAG
QDR2P_CTRL_DATA
QDR2P_2_4_BWX18
QDR2P_POWER
U50
U9
U49
VDD_QDR2_BV0_1
VDDQ_QDR2_BV0_1
VREF_QDR_BV0_1
VTT_QDR_BV0_1
1V8
1V5
5V
0V75_0
VRP_23
VRN_23
QDR2_BV0_1_COMPARE_ERROR
QDR2_BV0_1_CAL_DONE
QDR2_BV0_1_C_N_COMPAT
QDR2_BV0_1_QVLD
QDR2_BV0_1_D[0]
QDR2_BV0_1_D[1]
QDR2_BV0_1_D[2]
QDR2_BV0_1_D[3]
QDR2_BV0_1_D[4]
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QDR2_BV0_1_D[6]
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QDR2_BV0_1_D[8]
QDR2_BV0_1_D[9]
QDR2_BV0_1_D[10]
QDR2_BV0_1_D[11]
QDR2_BV0_1_D[12]
QDR2_BV0_1_D[13]
QDR2_BV0_1_D[14]
QDR2_BV0_1_D[15]
QDR2_BV0_1_D[16]
QDR2_BV0_1_D[17]
QDR2_BV0_1_Q[0]
QDR2_BV0_1_Q[1]
QDR2_BV0_1_Q[2]
QDR2_BV0_1_Q[3]
QDR2_BV0_1_Q[4]
QDR2_BV0_1_Q[5]
QDR2_BV0_1_Q[6]
QDR2_BV0_1_Q[7]
QDR2_BV0_1_Q[8]
QDR2_BV0_1_Q[9]
QDR2_BV0_1_Q[10]
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QDR2_BV0_1_Q[14]
QDR2_BV0_1_Q[15]
QDR2_BV0_1_Q[16]
QDR2_BV0_1_Q[17]
QDR2_BV0_1_CQ_P
QDR2_BV0_1_CQ_N
QDR2_BV0_1_SYS_RST_N
QDR2_BV0_1_DLL_OFF
QDR2_BV0_1_SA[0]
QDR2_BV0_1_SA[1]
QDR2_BV0_1_SA[2]
QDR2_BV0_1_SA[3]
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QDR2_BV0_1_SA[18]
QDR2_BV0_1_SA[19]
QDR2_BV0_1_SA[20]
QDR2_BV0_1_SA[21]
QDR2_BV0_1_K_P
QDR2_BV0_1_K_N
QDR2_BV0_1_R
QDR2_BV0_1_W
QDR2_BV0_1_BW
QDR2_BV0_1_QVLD
QDR2_BV0_1_C_N_COMPAT
QDR2_BV0_1_COMPARE_ERROR
QDR2_BV0_1_CAL_DONE
VTT_QDR_BV0_1
VDDQ_QDR2_BV0_1
VDD_QDR2_BV0_1
GND
BANKS=23,19
VTT_QDR_BV0_1
VTTSNS
VTTREF
VDDQSNS
VLDOIN
VIN
SS
S3
S2
S1
VRP_23
VRN_23
0V75_0
5V
VDD_QDR2_BV0_1
VDDQ_QDR2_BV0_1
VREF_QDR_BV0_1
1V5_19
1V5_19_1
1V5_19_2
1V5_23
1V5_23_1
1V5_23_2
1V8
GND
VDD_QDR2_BV0_1
VDDQ_QDR2_BV0_1
VTT_QDR_BV0_1
VREF_QDR_BV0_1
SELECT EITHER 1V5(QDR11+) OR 1V8(QDR11)
DO NOT SHORT
JP40
1V5
1V8
VDDQ_QDR2_BV0_1
VDD_QDR2_BV0_1
VTT_QDR_BV0_1
GND
5V
0V75_0
VRP_23
VRN_23
QDR2_BV0_1_COMPARE_ERROR
QDR2_BV0_1_CAL_DONE
QDR2_BV0_1_C_N_COMPAT
QDR2_BV0_1_QVLD
QDR2_BV0_1_D[0]
QDR2_BV0_1_D[1]
QDR2_BV0_1_D[2]
QDR2_BV0_1_D[3]
QDR2_BV0_1_D[4]
QDR2_BV0_1_D[5]
QDR2_BV0_1_D[6]
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QDR2_BV0_1_D[8]
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QDR2_BV0_1_D[16]
QDR2_BV0_1_D[17]
QDR2_BV0_1_Q[0]
QDR2_BV0_1_Q[1]
QDR2_BV0_1_Q[2]
QDR2_BV0_1_Q[3]
QDR2_BV0_1_Q[4]
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QDR2_BV0_1_Q[15]
QDR2_BV0_1_Q[16]
QDR2_BV0_1_Q[17]
QDR2_BV0_1_CQ_P
QDR2_BV0_1_CQ_N
QDR2_BV0_1_SYS_RST_N
QDR2_BV0_1_DLL_OFF
QDR2_BV0_1_SA[0]
QDR2_BV0_1_SA[1]
QDR2_BV0_1_SA[2]
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QDR2_BV0_1_SA[20]
QDR2_BV0_1_SA[21]
QDR2_BV0_1_K_P
QDR2_BV0_1_K_N
QDR2_BV0_1_R
QDR2_BV0_1_W
QDR2_BV0_1_BW
QDR2_BV0_1_QVLD
QDR2_BV0_1_C_N_COMPAT
QDR2_BV0_1_COMPARE_ERROR
QDR2_BV0_1_CAL_DONE
QDR2_TDI
QDR2_TMS
QDR2_TCK
TDO
R1
QDR2_BV0_1_TDO
QDR2_BV0_1_SYS_RST_N
QDR2P_JTAG
QDR2P_CTRL_DATA
QDR2P_2_4_BWX18
QDR2P_POWER
U50
U9
U49
VTT_QDR_BV0_1
VDDQ_QDR2_BV0_1
VDD_QDR2_BV0_1
VREF_QDR_BV0_1
1V8
1V5
5V
0V75_0
VRP_23
VRN_23
VTTSNS
VTTREF
VDDQSNS
VLDOIN
VIN
SS
S3
S2
S1
1V5_19
1V5_19_1
1V5_19_2
1V5_23
1V5_23_1
1V5_23_2
BANKS=23,19
U9
U49
U50
QDR2P_POWER
QDR2P_CTRL_DATA
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QDR2P_2_4_BWX18
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VDDQ_QDR2_BV0_1
VTT_QDR_BV0_1
VREF_QDR_BV0_1
GND
1V8
1V5
5V
0V75_0
VRP_23
VRN_23
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QDR2_BV0_1_CAL_DONE
QDR2_BV0_1_C_N_COMPAT
QDR2_BV0_1_QVLD
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QDR2_BV0_1_D[1]
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QDR2_BV0_1_Q[6]
QDR2_BV0_1_Q[7]
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QDR2_BV0_1_CQ_P
QDR2_BV0_1_CQ_N
QDR2_BV0_1_SYS_RST_N
QDR2_BV0_1_DLL_OFF
QDR2_BV0_1_SA[0]
QDR2_BV0_1_SA[1]
QDR2_BV0_1_SA[2]
QDR2_BV0_1_SA[3]
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QDR2_BV0_1_SA[18]
QDR2_BV0_1_SA[19]
QDR2_BV0_1_SA[20]
QDR2_BV0_1_SA[21]
QDR2_BV0_1_K_P
QDR2_BV0_1_K_N
QDR2_BV0_1_R
QDR2_BV0_1_W
QDR2_BV0_1_BW
QDR2_BV0_1_QVLD
QDR2_BV0_1_C_N_COMPAT
QDR2_TDI
QDR2_TMS
QDR2_TCK
TDO
R1
QDR2_BV0_1_TDO
QDR2_BV0_1_SYS_RST_N
QDR2_BV0_1_DLL_OFF
QDR2_BV0_1_SYS_RST_N
BANKS=23,19
U9
U49
U50
QDR2P_POWER
QDR2P_CTRL_DATA
QDR2P_JTAG
QDR2P_2_4_BWX18
VDD_QDR2_BV0_1
VDDQ_QDR2_BV0_1
VTT_QDR_BV0_1
VREF_QDR_BV0_1
GND
1V8
1V5
5V
0V75_0
VRP_23
VRN_23
VTTSNS
VTTREF
VDDQSNS
VLDOIN
VIN
SS
S3
S2
S1
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1V5_19_2
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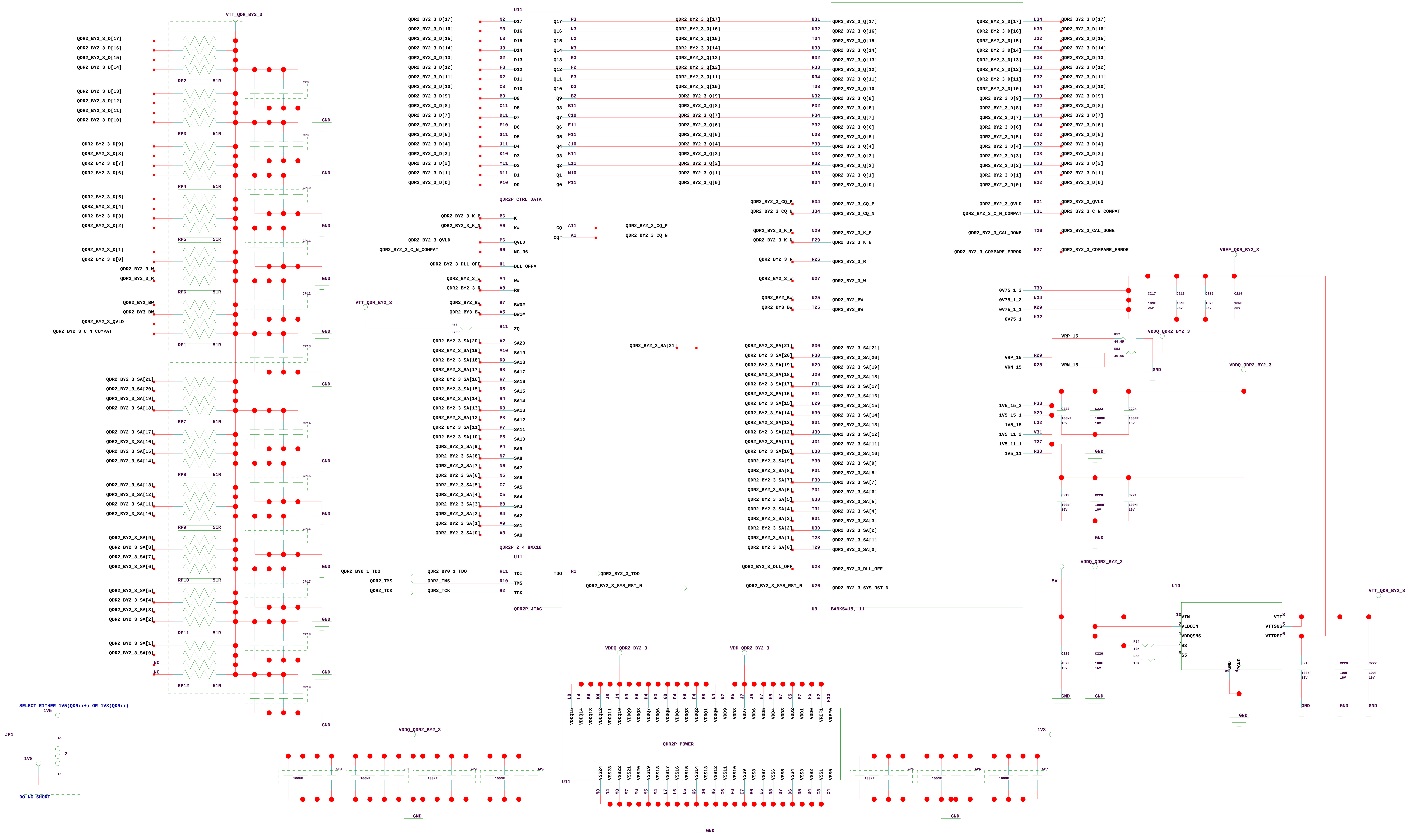

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QDR2_BY2_3_D[16]
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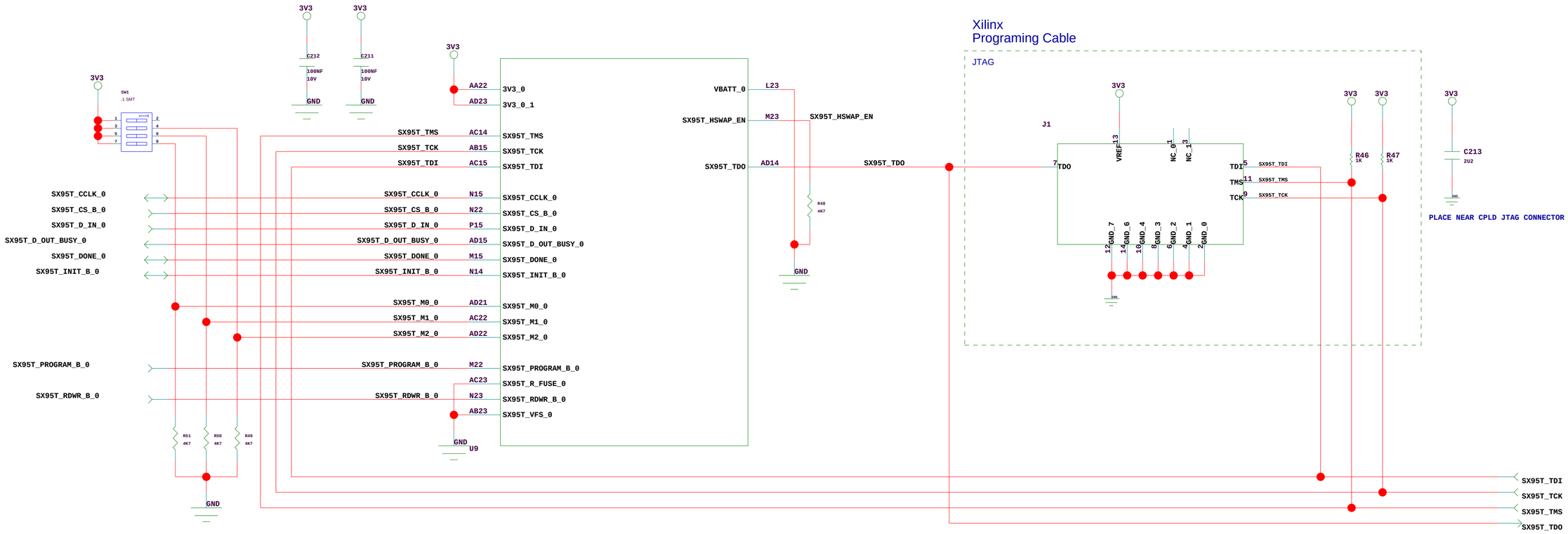
RP3 51R
RP4 51R
RP5 51R
RP6 51R
RP1 51R
RP7 51R
RP8 51R
RP9 51R
RP10 51R
RP11 51R
RP12 51R
QDR2_BY2_3_W
QDR2_BY2_3_R
QDR2_BY2_BW
QDR2_BY3_BW
QDR2_BY2_3_QVLD
QDR2_BY2_3_C_N_COMPAT
NC
GND
U11
QDR2P_CTRL_DATA
QDR2_BY2_3_K_P
QDR2_BY2_3_K_N
QDR2_BY2_3_QVLD
QDR2_BY2_3_C_N_COMPAT
QDR2_BY2_3_DLL_OFF
K
K#
QVLD
NC_R6
DLL_OFF#
W#
R#
BW0#
BW1#
ZQ
R56
270R
VTT_QDR_BY2_3
CQ
CQ#
QDR2_BY2_3_CQ_P
QDR2_BY2_3_CQ_N
QDR2_BY2_3_SA[21]
QDR2P_2_4_8MX18
QDR2_BY0_1_TDO
QDR2_TMS
QDR2_TCK
TDI
TMS
TCK
TDO
QDR2_BY2_3_TDO
QDR2P_JTAG
QDR2_BY2_3_SYS_RST_N
QDR2_BY2_3_DLL_OFF
U9
BANKS=15, 11
QDR2_BY2_3_CAL_DONE
QDR2_BY2_3_COMPARE_ERROR
VREF_QDR_BY2_3
0V75_1_3
0V75_1_2
0V75_1_1
0V75_1
VRP_15
VRN_15
R52 49.9R
R53 49.9R
VDDQ_QDR2_BY2_3
1V5_15_2
1V5_15_1
1V5_15
1V5_11_2
1V5_11_1
1V5_11
100NF 10V
10NF 25V
5V
U10
VIN
VLDOIN
VDDQSNS
S3
S5
VTT
VTTSNS
VTTREF
GND
PGND
R54 10K
R55 10K
47UF 10V
10UF 10V
VTT_QDR_BY2_3
VDDQ_QDR2_BY2_3
VDD_QDR2_BY2_3
QDR2P_POWER
VREF0
VREF1
1V5
1V8
JP1
SELECT EITHER 1V5(QDRii+) OR 1V8(QDRii)
DO NO SHORT
100NF

TBD

VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input



The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups. Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

Place nearest PHY pin 96

Place nearest PHY pin 101

Place nearest PHY pin 98

Place nearest PHY pin 100

Place as close to PHY CORE VDD power pins as possible

Place as close to PHY IO VDD power pins as possible

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5

Place jumers in line with signals

Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

Bottom LED
Green/Toggle = ACTIVITY

HFJ11-1G02E-L12

CHASSIS_GND

ETHERNET Mgt.

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

NOSTUFF

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

DP83865DVH

2V5
C482
10NF
Place nearest PHY pin 96
2V5
C455
10NF
Place nearest PHY pin 101
1V8
R256
1R
C483
22UF/6V
C476
10NF
ETH1_PGM_VDD
Place nearest PHY pin 98
1V8
R257
1R
C484
22UF/6V
C475
10NF
ETH1_1V8_AVDD3
Place nearest PHY pin 100
1V8
C458
10NF
C459
100NF
C457
10NF
C460
100NF
C461
10NF
C479
100NF
C462
10NF
C456
100NF
Place as close to PHY CORE VDD power pins as possible
2V5
C481
10NF
C477
100NF
C480
10NF
C470
100NF
C468
10NF
C469
100NF
C467
10NF
C478
100NF
C465
10NF
C466
100NF
C463
10NF
C464
100NF
Place as close to PHY IO VDD power pins as possible
U1
4408PX
GigE/Ethernet ROM#1
GMC1_TXD0
GMC1_TXD1
GMC1_TXD2
GMC1_TXD3
GMC1_TXCTL
GMC1_TXCLK
GMC1_RXD0
GMC1_RXD1
GMC1_RXD2
GMC1_RXD3
GMC1_RXCTL
GMC1_RXCLK
Place resistors as close to CPU as possible and keep all traces lengths equal
R275 22R
R276 22R
R277 22R
R278 22R
R279 22R
R274 22R
R271 22R
R272 22R
R273 22R
R280 0R
GMCMDCLK
GMCMDIO
Place resistors close to PHY all trace lengths equal
U47
DP83865DVH
GMC1TXD0
GMC1TXD1
GMC1TXD2
GMC1TXD3
GMC1TXCTL
GMC1TXCLK
GMC1RXD0
GMC1RXD1
GMC1RXD2
GMC1RXD3
GMC1RXCTL
GMC1RXCLK
TXD0/TX0
TXD1/TX1
TXD2/TX2
TXD3/TX3
TXD4
TXD5
TXD6
TXD7
TX_EN/TXEN_ER
TX_ER
TX_CLK/RGMII_SEL1
RX_CLK/TCK
CRS/RGMII_SEL0
COL
RXD0/RX0
RXD1/RX1
RXD2/RX2
RXD3/RX3
RXD4
RXD5
RXD6
RXD7
RX_DV/RCK
RX_ER/RXDV_ER
RX_CLK
MDC
MDIO
CLK_TO_MAC
RESETn
INTERRUPTn
CLK_IN
CLK_OUT
TDO
TDI
TCK
TMS
TRSTn
GETH1_RSTn
GETH1_INTn
CLK_GETH1_25MHZ
NC
Place jumers in line with signals
JP39
JP38
Place components as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible.
Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5
MDIA_P
MDIA_N
MDIB_P
MDIB_N
MDIC_P
MDIC_N
MDID_P
MDID_N
MDI1_0P
MDI1_0N
MDI1_1P
MDI1_1N
MDI1_2P
MDI1_2N
MDI1_3P
MDI1_3N
R255 49.9R
R249 49.9R
R251 49.9R
R253 49.9R
R250 49.9R
C474 10NF
C472 10NF
C473 10NF
C471 10NF
VDD_SEL_STRAP
MAC_CLK_EN_STRAP
MDIX_EN_STRAP
MULTI_EN_STRAP
LINK1000_LED/AN_EN_STRAP
LINK100_LED/DUPLEX_STRAP
LINK10_LED/RLED/SPEED1_STRAP
ACTIVITY_LED/SPEED0_STRAP
DUPLEX_LED/PHYAD0B0_STRAP
PHYAD0B1_STRAP
PHYAD0B2_STRAP
PHYAD0B3_STRAP
PHYAD0B4_STRAP
LED1_LINK0
LED1_LINK1
LED1_LINK
LED1_ACT
LED1_DUPLEX
R260 2K2
NOSTUFF
R261 2K2
NOSTUFF
R262 2K2
BG_REF
TX_TCLK
NON_IEEE_STRAP
RESERVED1
RESERVED2
RESERVED
R247 9K76
Ethernet LEDs
Top LED = SPEED/LINK
Green = 1000
Off = 10/100
Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY
J8
VCC
GND
MNT1
MNT2
TD0P
TD0N
TD1P
TD2P
TD2N
TD1N
TD3P
TD3N
CASE1
CASE2
GRN
GRN/ YEL
HFJ11-1G02E-L12
C485 22UF/6V
NC
CHASSIS_GND
STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL
JP35
JP36
DUPLEX LED
JP37
JP24
JP34
JP33
R246 2K2
R245 330R
D10
JP32
JP31
R269 2K2
R267 330R
JP30
JP29
L10 LED
R268 2K2
R244 330R
D11
JP28
JP27
L100 LED
R258 2K2
R243 330R
D9
JP25
JP26
R242 2K2
R241 330R

PLACE NEAREST DDR2 MODULE PINS

DDR_VREF_0V9

1V8

GND

DDR_VTT

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

DDR_PA[15:0]

DDR_PD[63:0]

Place parts as close to CPU as possible

DDR SDRAM

U27

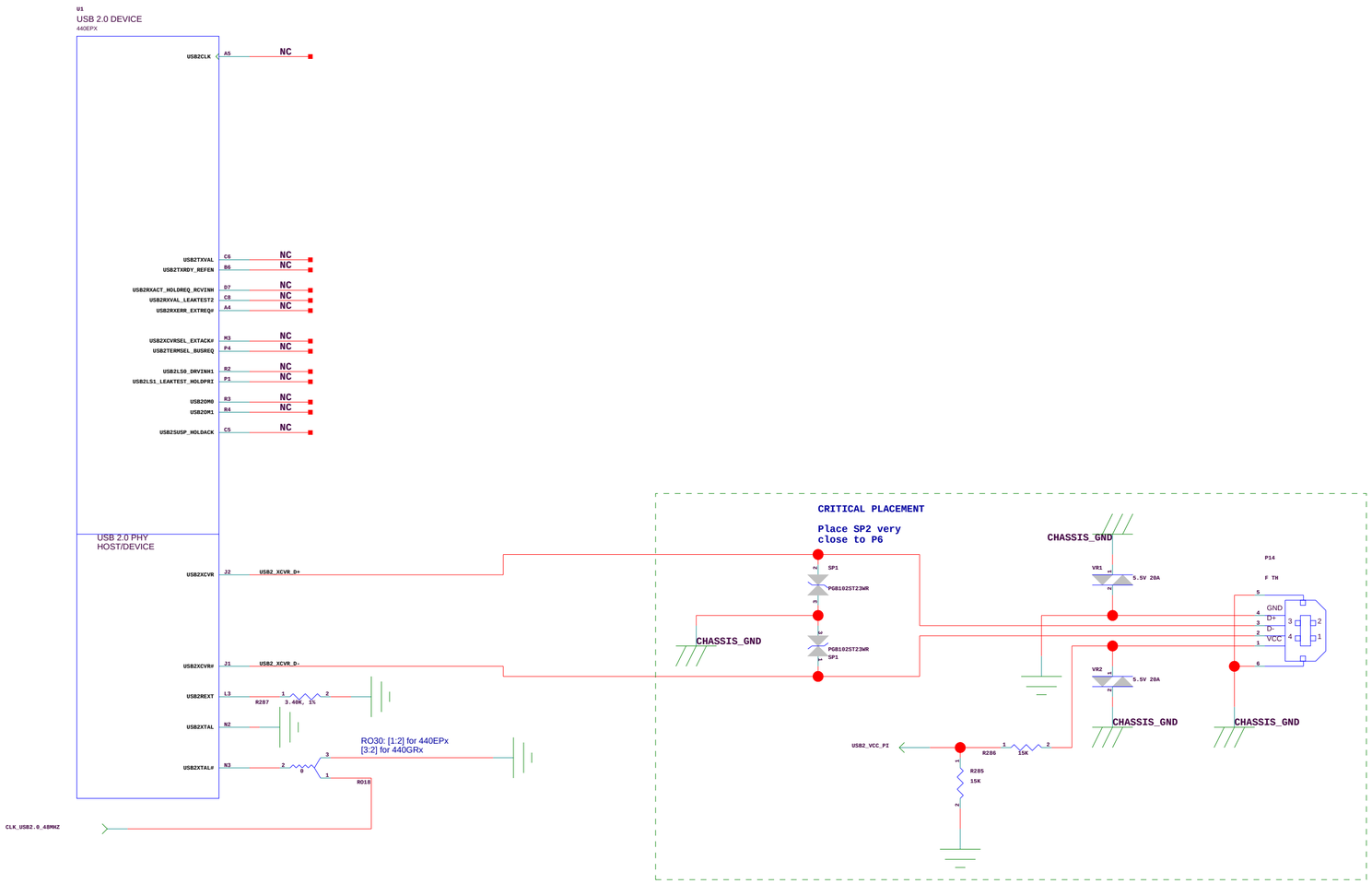
Scope Loop

DDR_CLKOUT0

DDR_CLKOUT

DDR_VTT

5V



KAROO ARRAY TELESCOPE, NRF UNIT 12, LONSDALE BUILDING LONSDALE WAY, PINELANDS, 7405 SOUTH AFRICA			
TITLE: ROACH_PPC_USB			
CHECKED BY: <PUT NAME HERE>	SIZE: A2	DWG NO: <PUT DRAWING NUMBER HERE>	REV: 0
DRAWN BY: <PUT NAME HERE>	SCALE: NTS	SHEET: 1 of 1	9-19-2007_13:16

Memory Bus

PAD0[27..31]

PDATA[0..7]

RESETS

CPU_TRSTn = '1' when JTAG_TRSTn = '1' and RESET_PORn = '1' else '0'; see errata sheet

CLOCKS

STATUS / MISC

SYSERR

FLASH

I2C

USB

Assertion of USB2_RESET may be asynchronous to CLK_USB2_CPLD
De-assertion of USB2_RESET must be synchronous to CLK_USB2_CPLD

NAND FLASH

ETHERNET

USB_EBC_MUX

roach_cpld_XC2C256_7VQ100C_pcb

U22

P4	PAD4	P142	PAD217
P7	PAD8	P140	PAD214
P9	PAD10	P139	PAD213
P10	PAD12	P138	PAD212
P11	PAD15	P137	PAD211
P12	PAD16	P136	PAD208
P13	PAD17	P135	PAD207
P14	PAD18	P134	PAD206
P15	PAD19	P133	PAD204
P16	PAD20	P132	PAD199
P17	PAD21	P131	PAD197
P18	PAD23	P130	PAD196
P19	PAD28	P129	PAD195
P20	PAD29	P128	PAD194
P21	PAD30	P126	PAD192
P22	PAD31	P125	PAD191
P23	PAD32	P124	PAD190
P24	PAD33	P121	PAD187
P25	PAD34	P120	PAD186
P26	PAD35	P119	PAD178
P28	PAD44	P118	PAD177
P30	PAD48	P117	PAD176
P31	PAD49	P116	PAD175
P32	PAD50	P115	PAD173
P33	PAD52	P114	PAD171
P34	PAD54	P113	PAD169
P35	PAD55	P112	PAD168
P38	PAD59	P111	PAD167
P40	PAD64	P110	PAD166
P41	PAD65	P107	PAD163
P42	PAD66	P106	PAD162
P43	PAD67	P105	PAD161
P44	PAD68	P104	PAD160
P45	PAD69	P103	PAD158
P46	PAD70	P102	PAD156
P48	PAD73	P101	PAD154
P49	PAD74	P100	PAD152
P50	PAD75	P98	PAD146
P51	PAD76	P97	PAD145
P52	PAD77	P96	PAD144
P53	PAD81	P95	PAD143
P54	PAD82	P94	PAD142
P56	PAD86	P92	PAD138
P57	PAD87	P91	PAD137
P58	PAD88	P88	PAD134
P59	PAD89	P87	PAD133
P60	PAD90	P86	PAD132
P61	PAD95	P85	PAD131
P64	PAD100	P83	PAD125
P66	PAD102	P82	PAD121
P68	PAD105	P81	PAD120
P69	PAD107	P80	PAD119
P70	PAD108	P79	PAD118
P71	PAD109	P78	PAD117
P74	PAD112	P77	PAD115
P75	PAD113	P76	PAD114

User DIP-Swith

Boot Configuration

Configuration DIP-Swith

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

SysErr will be used to drive Status LED (active H)

J3

GMMC001LEU

roach_cpld_XC2C256_7VQ100C_powerpins

U22

PLACE NEAR CPLD POWER PINS

roach_cpld_XC2C256_7VQ100C_configpins

Xilinx
Programing Cable

JTAG

PLACE NEAR CPLD JTAG CONNECTOR

PWR_GOOD monitors the +1.0v, 1V5, 1V8, 2V5, and 3V3 supplies

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_3V3_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz

IRQ0-9 have programmable polarity per section 10.5.7 (UIC0_PR) 440ep user manual

Critical Placement and Route
Clock Rules:

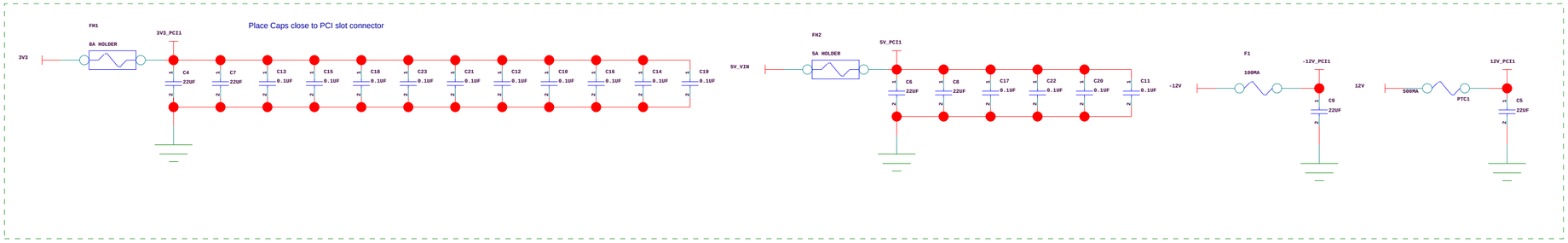
Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible

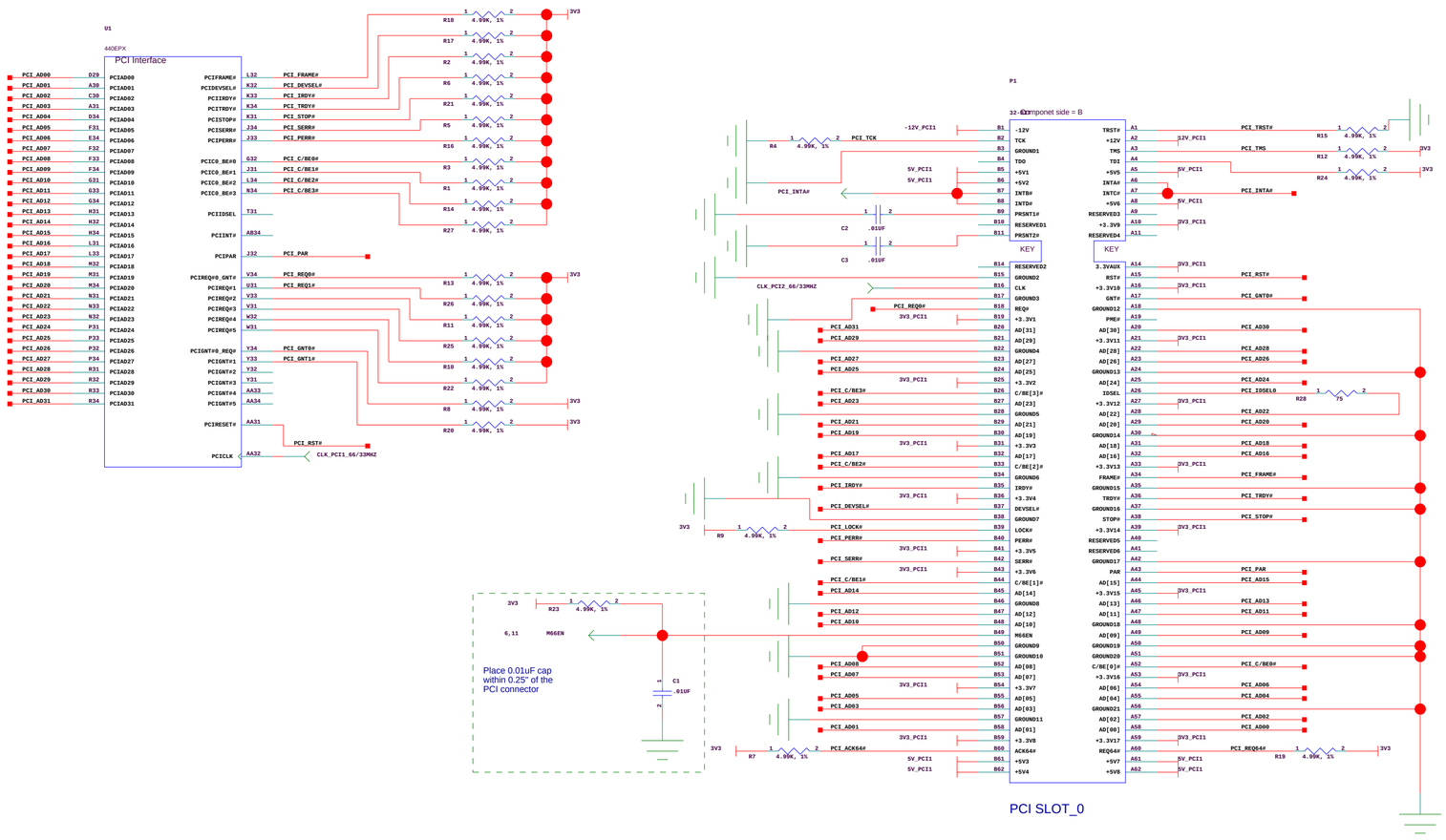
TRACE & JTAG CONNECTORS

Critical placement and routing of the Trace connector and nets. Up to CPU frequency/4

R26 is for current limiting and should be <100 Ohms.

NO POP
RO1 - RO5





PCI SLOT_0

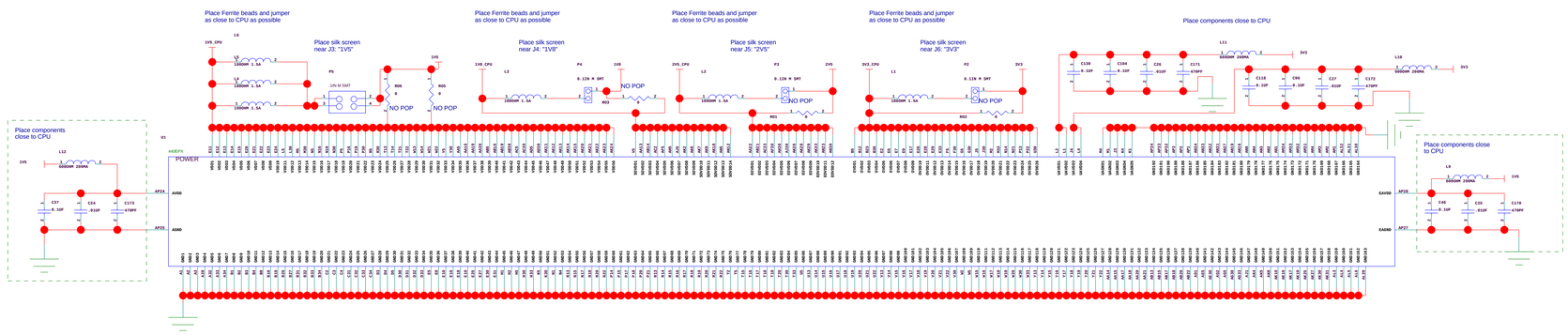
Include silkscreen text:
"SUPPORTS 3V3 IO ONLY"

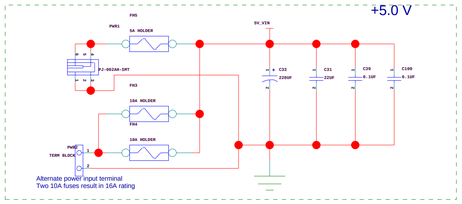
Optional PRSNT signals are not used, max 25W is available		
PRSNT1#	PRSNT2#	Expansion Configuration
Open	Open	No expansion board present
Ground	Open	Expansion board present, 25 W maximum
Open	Ground	Expansion board present, 15 W maximum
Ground	Ground	Expansion board present, 7.5 W maximum

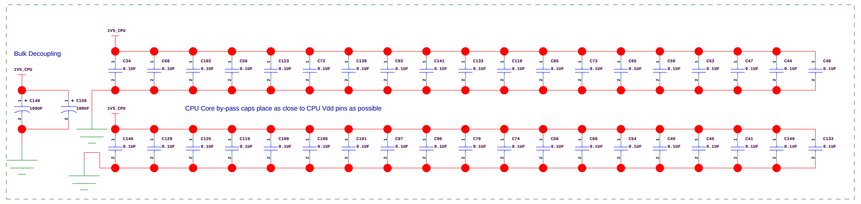
KAROO ARRAY TELESCOPE, NRF
UNIT 12, LONSDALE BUILDING
LONSDALE WAY, PINELANDS, 7405
SOUTH AFRICA

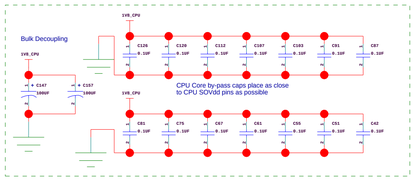
TITLE: ROACH_PPC_PCI

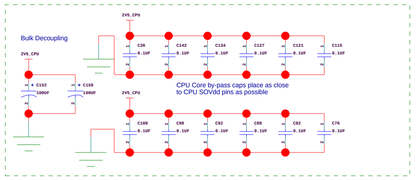
CHECKED BY: <PUT NAME HERE>
DRAWN BY: <PUT NAME HERE>
SIZE: A2
DWG NO: <PUT DRAWING NUMBER HERE>
REV: 0
SCALE: NTS
SHEET: 1 of 1
9-19-2007_13:16

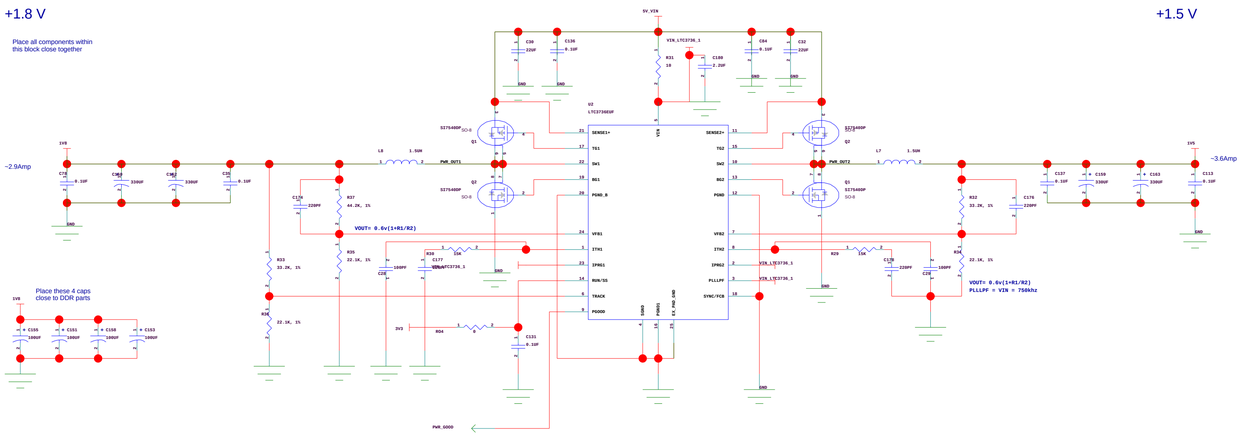

Place Ferrite beads and jumper as close to CPU as possible
Place silk screen near J3: "1V5"
Place Ferrite beads and jumper as close to CPU as possible
Place silk screen near J4: "1V8"
Place Ferrite beads and jumper as close to CPU as possible
Place silk screen near J5: "2V5"
Place Ferrite beads and jumper as close to CPU as possible
Place silk screen near J6: "3V3"
Place components close to CPU
Place components close to CPU
Place components close to CPU
1V5_CPU
1V8_CPU
2V5_CPU
3V3_CPU
1V5
1V8
2V5
3V3
NO POP
POWER
AVSD
ADSD
EAVSD
EADSD

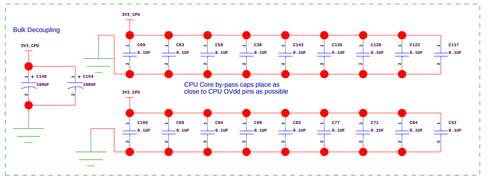

+5.0 V
FH5
FH3
FH4
PWR1
PWR2
5A HOLDER
15A HOLDER
15A HOLDER
TERM BLOCK
5V_VIN
Alternate power input terminal
Two 10A fuses result in 16A rating

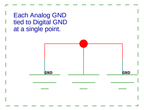

Bulk Decoupling
CPU Core by-pass caps place as close to CPU Vdd pins as possible
1V5_CPU

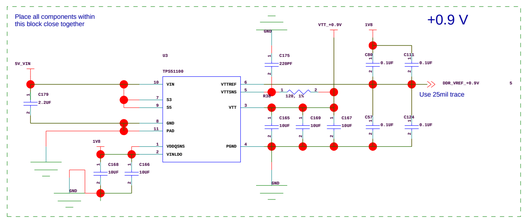

Bulk Decoupling
CPU Core by-pass caps place as close to CPU SOVdd pins as possible
1V8_CPU

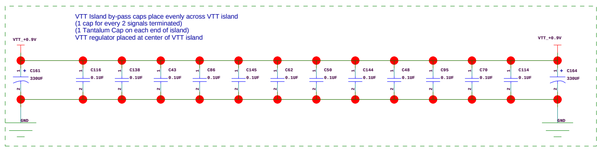

Bulk Decoupling
CPU Core by-pass caps place as close to CPU SOVdd pins as possible
2V5_CPU


+1.8 V
Place all components within this block close together
~2.9Amp
Place these 4 caps close to DDR parts
+1.5 V
~3.6Amp
5V_VIN
VOUT= 0.6v(1+R1/R2)
VOUT= 0.6v(1+R1/R2)
PLLLPF = VIN = 750khz
PWR_GOOD


Bulk Decoupling
CPU Core by-pass caps place as close to CPU OVdd pins as possible
3V3_CPU

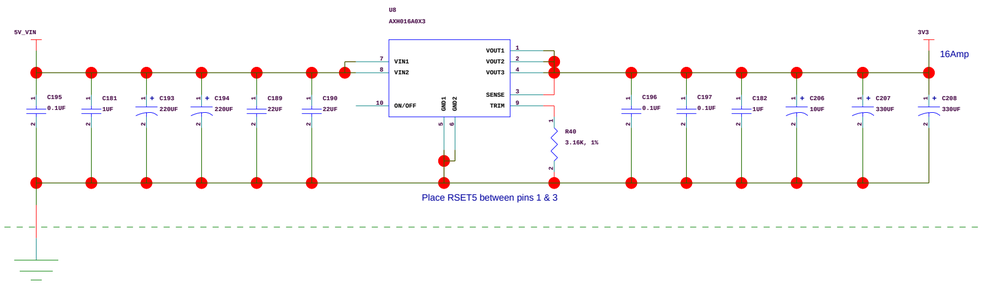

Each Analog GND tied to Digital GND at a single point.
GND


Place all components within this block close together
+0.9 V
U3
TPS51100
VTT_+0.9V
Use 25mil trace
0R0_VREF_+0.9V

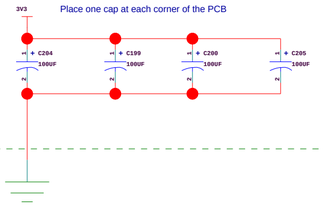

VTT Island by-pass caps place evenly across VTT island
(1 cap for every 2 signals terminated)
(1 Tantalum Cap on each end of island)
VTT regulator placed at center of VTT island
VTT_+0.9V

Place all components within
this block close together

+3.3 V

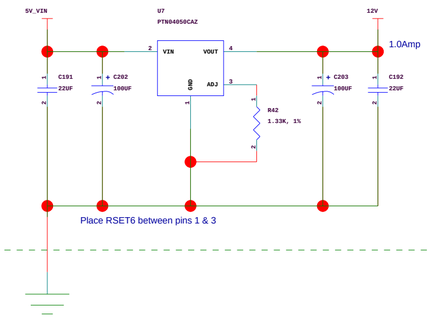


Place one cap at each corner of the PCB



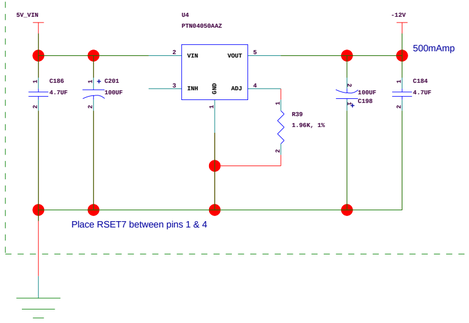
Place all components within
this block close together

+12 V



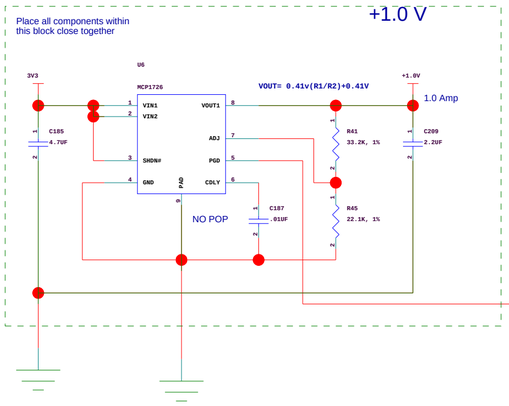
Place all components within
this block close together

-12 V



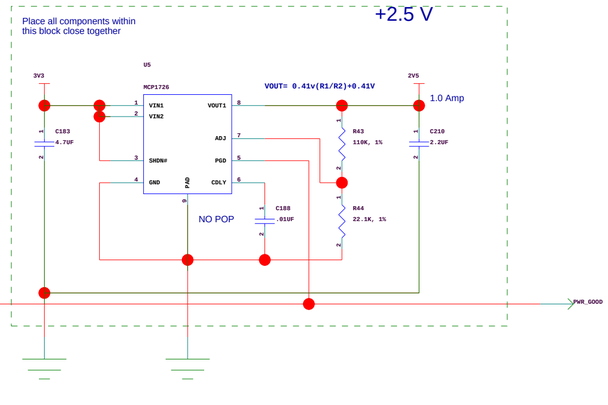
Place all components within
this block close together

+1.0 V



Place all components within
this block close together

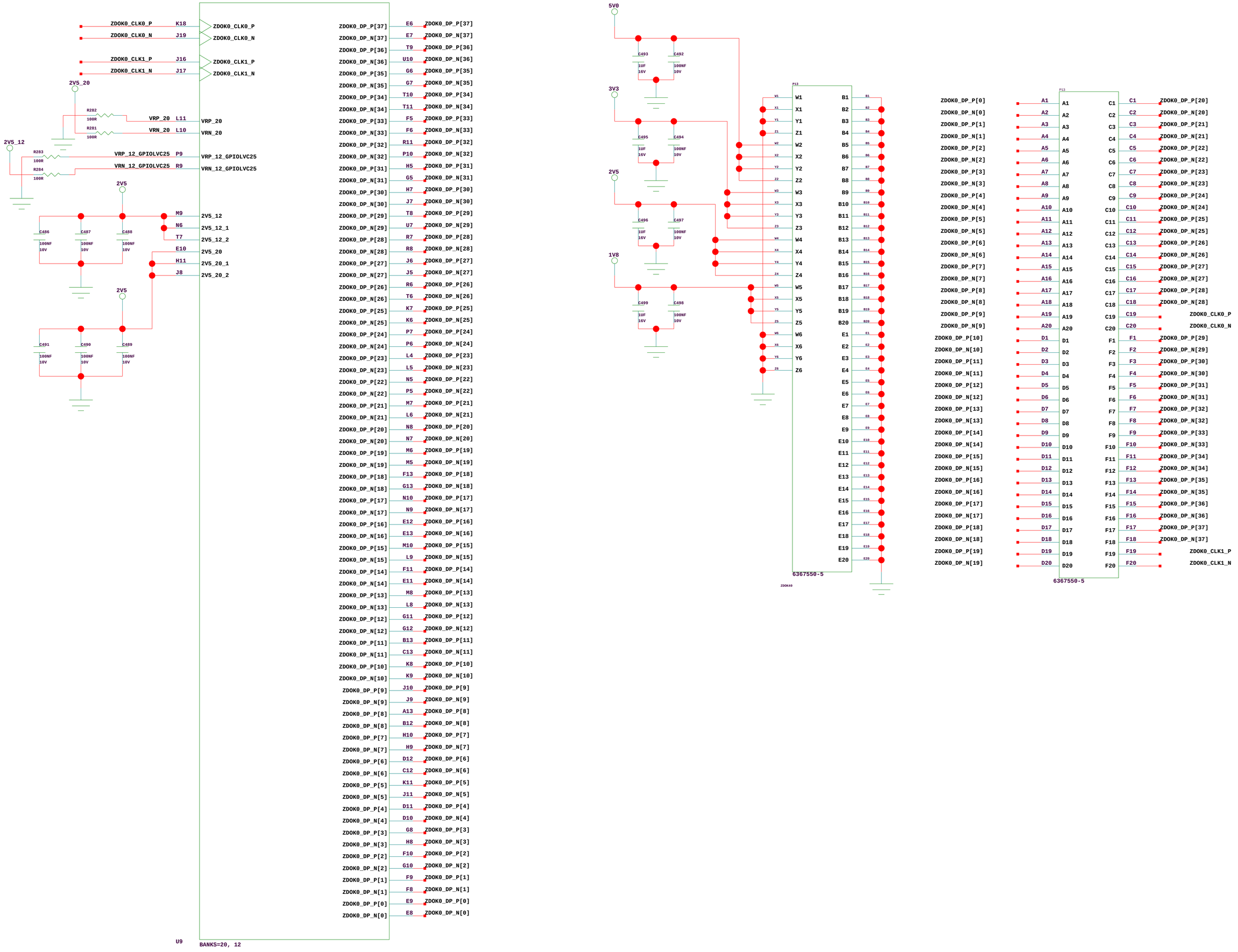
+2.5 V



KAROO ARRAY TELESCOPE, NRF
UNIT 12, LONSDALE BUILDING
LONSDALE WAY, PINELANDS, 7405
SOUTH AFRICA

TITLE: ROACH_PPC_POWER_2

CHECKED BY: <PUT NAME HERE>	SIZE: A2	DWG NO: <PUT DRAWING NUMBER HERE>	REV: 0
DRAWN BY: <PUT NAME HERE>	SCALE: NTS	SHEET: 1 of 1	9-19-2007_13:16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ZDOK0_CLK1_N J17
ZDOK0_CLK0_P
ZDOK0_CLK0_N
ZDOK0_CLK1_P
ZDOK0_CLK1_N
2V5_20
R282 100R
R281 100R
VRP_20 L11
VRN_20 L10
VRP_20
VRN_20
2V5_12
R283 100R
R284 100R
VRP_12_GPIOLVC25 P9
VRN_12_GPIOLVC25 R9
VRP_12_GPIOLVC25
VRN_12_GPIOLVC25
2V5
C486 100NF 10V
C487 100NF 10V
C488 100NF 10V
M9 2V5_12
N6 2V5_12_1
T7 2V5_12_2
E10 2V5_20
H11 2V5_20_1
J8 2V5_20_2
C491 100NF 10V
C490 100NF 10V
C489 100NF 10V
ZDOK0_DP_P[37] E6 ZDOK0_DP_P[37]
ZDOK0_DP_N[37] E7 ZDOK0_DP_N[37]
ZDOK0_DP_P[36] T9 ZDOK0_DP_P[36]
ZDOK0_DP_N[36] U10 ZDOK0_DP_N[36]
ZDOK0_DP_P[35] G6 ZDOK0_DP_P[35]
ZDOK0_DP_N[35] G7 ZDOK0_DP_N[35]
ZDOK0_DP_P[34] T10 ZDOK0_DP_P[34]
ZDOK0_DP_N[34] T11 ZDOK0_DP_N[34]
ZDOK0_DP_P[33] F5 ZDOK0_DP_P[33]
ZDOK0_DP_N[33] F6 ZDOK0_DP_N[33]
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ZDOK0_DP_N[32] P10 ZDOK0_DP_N[32]
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ZDOK0_DP_N[31] G5 ZDOK0_DP_N[31]
ZDOK0_DP_P[30] H7 ZDOK0_DP_P[30]
ZDOK0_DP_N[30] J7 ZDOK0_DP_N[30]
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ZDOK0_DP_P[26] R6 ZDOK0_DP_P[26]
ZDOK0_DP_N[26] T6 ZDOK0_DP_N[26]
ZDOK0_DP_P[25] K7 ZDOK0_DP_P[25]
ZDOK0_DP_N[25] K6 ZDOK0_DP_N[25]
ZDOK0_DP_P[24] P7 ZDOK0_DP_P[24]
ZDOK0_DP_N[24] P6 ZDOK0_DP_N[24]
ZDOK0_DP_P[23] L4 ZDOK0_DP_P[23]
ZDOK0_DP_N[23] L5 ZDOK0_DP_N[23]
ZDOK0_DP_P[22] N5 ZDOK0_DP_P[22]
ZDOK0_DP_N[22] P5 ZDOK0_DP_N[22]
ZDOK0_DP_P[21] M7 ZDOK0_DP_P[21]
ZDOK0_DP_N[21] L6 ZDOK0_DP_N[21]
ZDOK0_DP_P[20] N8 ZDOK0_DP_P[20]
ZDOK0_DP_N[20] N7 ZDOK0_DP_N[20]
ZDOK0_DP_P[19] M6 ZDOK0_DP_P[19]
ZDOK0_DP_N[19] M5 ZDOK0_DP_N[19]
ZDOK0_DP_P[18] F13 ZDOK0_DP_P[18]
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ZDOK0_DP_N[13] L8 ZDOK0_DP_N[13]
ZDOK0_DP_P[12] G11 ZDOK0_DP_P[12]
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ZDOK0_DP_P[8] A13 ZDOK0_DP_P[8]
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2V5
1V8
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C499 1UF 16V
C498 100NF 10V
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B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20
6367550-5
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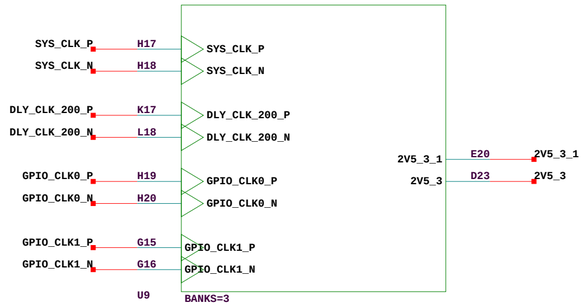
ZDOK0_DP_N[19] D20 D20 F20 ZDOK0_CLK1_N
P13
6367550-5


K10 K15 K20 K25 K30 K4 K5 L13 L17 L22 L27 L7 M12 M14 M16 M18 M20 M24 M34 M4 N11 N13 N17 N19 N21 N26 N31 N4 P12 P14 P16 P18 P2 P20 P22 P28 P8 R10 R13 R15 R17 R19 R2 R21 R23 R25 R5 T12 T14 T16 T20 T22 T32 T4 T5 U11 U13 U15 U19 U21 U23 U29 U34 U6 U9 V12 V14 V16 V20 V22 V26 V6 W13 W15 W19 W21 W23 W33 W4 W5 Y10 Y12 Y14 Y16 Y18 Y2 Y20 Y22 Y25 Y30 Y5
GND_128 GND_129 GND_130 GND_131 GND_132 GND_133 GND_134 GND_135 GND_136 GND_137 GND_138 GND_139 GND_140 GND_141 GND_142 GND_143 GND_144 GND_145 GND_146 GND_147 GND_148 GND_149 GND_150 GND_151 GND_152 GND_153 GND_154 GND_155 GND_156 GND_157 GND_158 GND_159 GND_160 GND_161 GND_162 GND_163 GND_164 GND_165 GND_166 GND_167 GND_168 GND_169 GND_170 GND_171 GND_172 GND_173 GND_174 GND_175 GND_176 GND_177 GND_178 GND_179 GND_180 GND_181 GND_182 GND_183 GND_184 GND_185 GND_186 GND_187 GND_188 GND_189 GND_190 GND_191 GND_192 GND_193 GND_194 GND_195 GND_196 GND_197 GND_198 GND_199 GND_200 GND_201 GND_202 GND_203 GND_204 GND_205 GND_206 GND_207 GND_208 GND_209 GND_210 GND_211 GND_212 GND_213 GND_214 GND_215 GND_216 GND_217 GND_218
A11 A12 A17 A22 A27 A32 AA11 AA13 AA15 AA17 AA19 AA2 AA21 AA23 AA27 AA7 AB12
GND GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16
GND_127 GND_126 GND_125 GND_124 GND_123 GND_122 GND_121 GND_120 GND_119 GND_118 GND_117 GND_116 GND_115 GND_114 GND_113 GND_112 GND_111
J33 J23 J2 J18 J13 H6 H26 H21 H2 H16 G9 G4 G34 G29 G19 F7 F32
GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_25 GND_26 GND_27 GND_28 GND_29 GND_30 GND_31 GND_32 GND_33 GND_34 GND_35 GND_36 GND_37 GND_38 GND_39 GND_40 GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67 GND_68 GND_69 GND_70 GND_71 GND_72 GND_73 GND_74 GND_75 GND_76 GND_77 GND_78 GND_79 GND_80 GND_81 GND_82 GND_83 GND_84 GND_85 GND_86 GND_87 GND_88 GND_89 GND_90 GND_91 GND_92 GND_93 GND_94 GND_95 GND_96 GND_97 GND_98 GND_99 GND_100 GND_101 GND_102 GND_103 GND_104 GND_105 GND_106 GND_107 GND_108 GND_109 GND_110
AB14 AB16 AB18 AB20 AB22 AB24 AB34 AB4 AC11 AC13 AC17 AC19 AC21 AC26 AC31 AD12 AD16 AD18 AD28 AD8 AE10 AE15 AE20 AE25 AE4 AE5 AF12 AF17 AF2 AF22 AF27 AF32 AG19 AG2 AG24 AG29 AG34 AG9 AH16 AH26 AH4 AH6 AJ13 AJ23 AJ33 AJ5 AK10 AK20 AK30 AK4 AL17 AL27 AL6 AL9 AM14 AM2 AM24 AM34 AN1 AN11 AN2 AN21 AN31 AN7 AN8 AP11 AP13 AP18 AP23 AP28 AP33 B1 B11 B14 B2 B24 B29 B34 B7 B8 C11 C2 C21 C31 D18 D28 D33 D6 D9 E15 E25 E5 F12 F22
U9
GND
2V5
AB11 AC12 L12 M11 M21 P11 P23 T23 U24 V11 V23 Y23
2V5_AUX 2V5_AUX_1 2V5_AUX_2 2V5_AUX_3 2V5_AUX_4 2V5_AUX_5 2V5_AUX_6 2V5_AUX_7 2V5_AUX_8 2V5_AUX_9 2V5_AUX_10 2V5_AUX_11
U9
1V0
Y21 Y19 Y17 Y15 Y13 W22 W20 W16 W14 W12 V21 V19 V15 V13 U22 U20 U16 U14 U12 T21 T19 T15 T13 R22 R20 R18 R16 R14 R12 P21 P19 P17 P13 N20 N18 N16 N12 M19 M17 M13 AD17 AD13 AC20 AC18 AC16 AB21 AB19 AB17 AB13 AA20 AA18 AA16 AA14 AA12
1V0_53 1V0_52 1V0_51 1V0_50 1V0_49 1V0_48 1V0_47 1V0_46 1V0_45 1V0_44 1V0_43 1V0_42 1V0_41 1V0_40 1V0_39 1V0_38 1V0_37 1V0_36 1V0_35 1V0_34 1V0_33 1V0_32 1V0_31 1V0_30 1V0_29 1V0_28 1V0_27 1V0_26 1V0_25 1V0_24 1V0_23 1V0_22 1V0_21 1V0_20 1V0_19 1V0_18 1V0_17 1V0_16 1V0_15 1V0_14 1V0_13 1V0_12 1V0_11 1V0_10 1V0_9 1V0_8 1V0_7 1V0_6 1V0_5 1V0_4 1V0_3 1V0_2 1V0_1 1V0
U9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H17
SYS_CLK_N
H18
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K17
DLY_CLK_200_N
L18
GPIO_CLK0_P
H19
GPIO_CLK0_N
H20
GPIO_CLK1_P
G15
GPIO_CLK1_N
G16
U9
SYS_CLK_P
SYS_CLK_N
DLY_CLK_200_P
DLY_CLK_200_N
GPIO_CLK0_P
GPIO_CLK0_N
GPIO_CLK1_P
GPIO_CLK1_N
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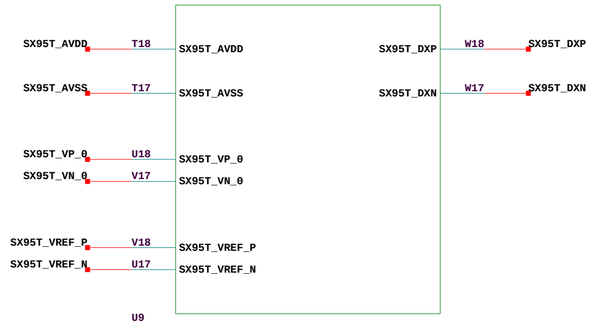
E20
2V5_3
D23
2V5_3_1
2V5_3


SX95T_AVDD
T18
SX95T_AVSS
T17
SX95T_VP_0
U18
SX95T_VN_0
V17
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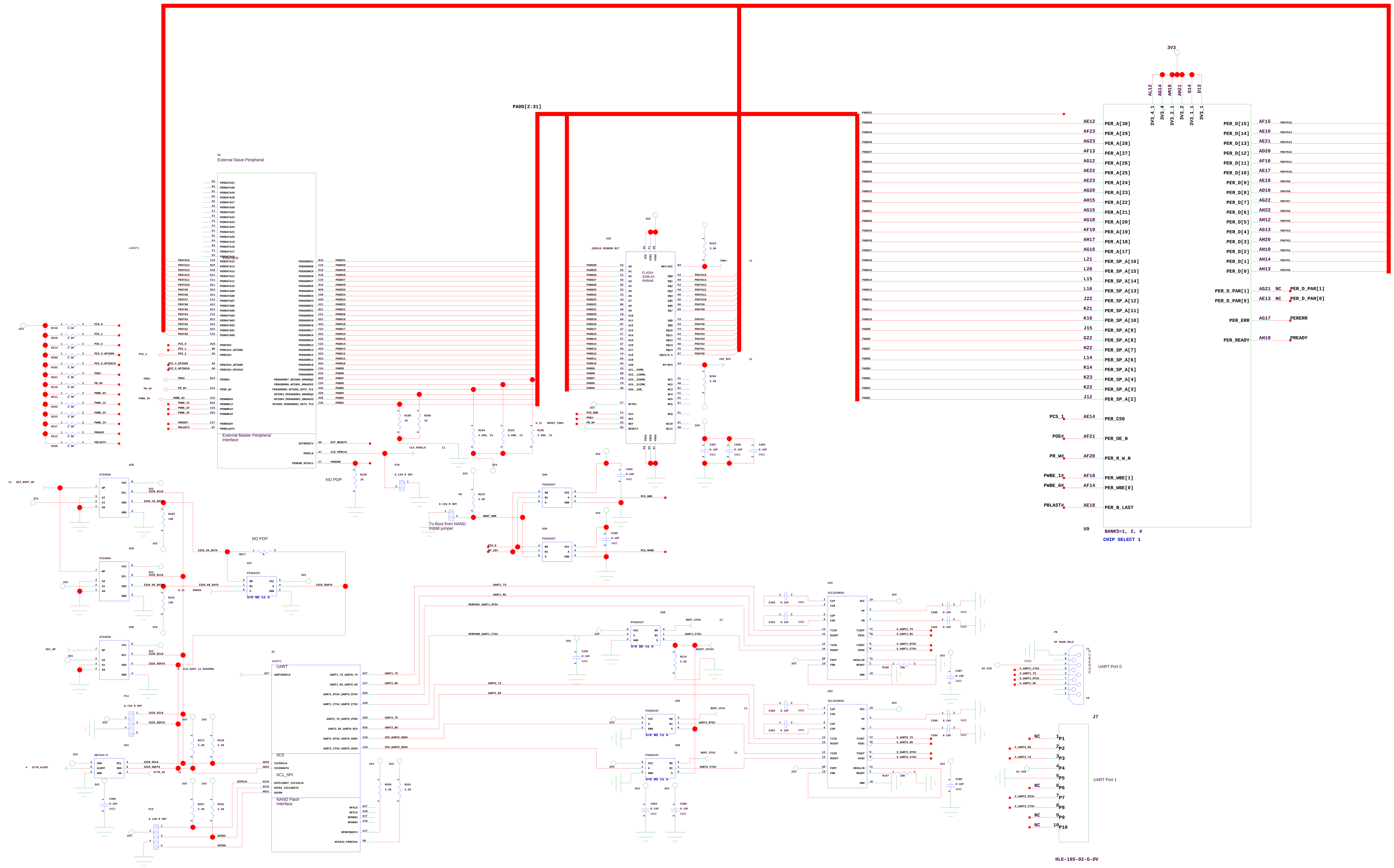
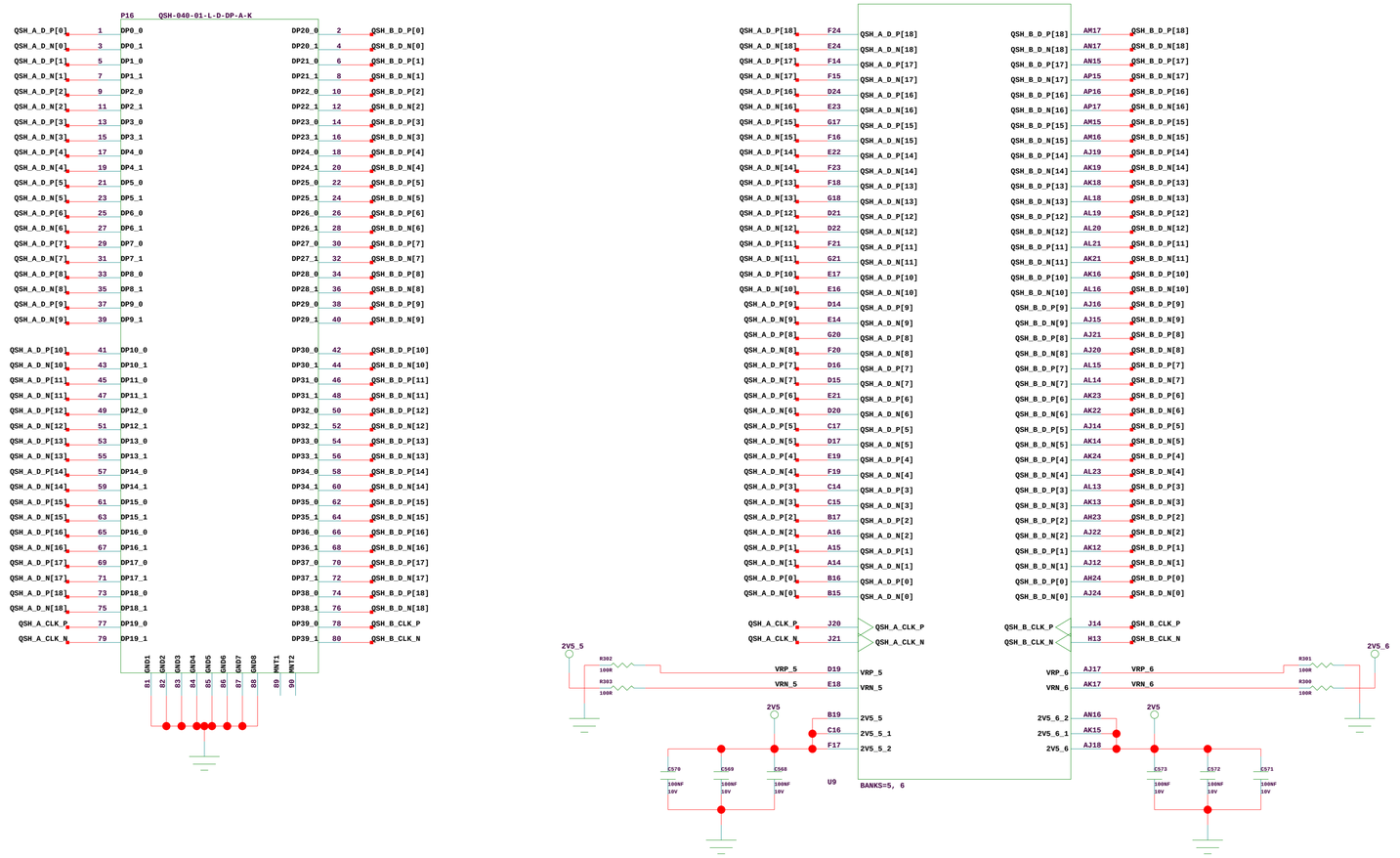
V18
SX95T_VREF_N
U17
U9
SX95T_AVDD
SX95T_AVSS
SX95T_VP_0
SX95T_VN_0
SX95T_VREF_P
SX95T_VREF_N
SX95T_DXP
W18
SX95T_DXN
W17
SX95T_DXP
SX95T_DXN

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB27 220@100M
FB28 220@100M
FB29 220@100M
FB30 220@100M
C413 220NF 6.3V
C412 220NF 6.3V
C411 220NF 6.3V
C410 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
2V5
FB51 220@100M
C454 220NF 6.3V
R238 10K
X2
OE
VCC
OUT+
OUT-
MGT_REFCLK_Q2_P
MGT_REFCLK_Q2_N
JP23 156.25MHZ
CCLD-023-25-156.250
C422 10NF 25V
C423 10NF 25V
C424 10NF 25V
C425 10NF 25V
C427 10NF 25V
C426 10NF 25V
MGTAVCC_120 D5
MGTAVCC_120_1 F4
MGTAVCCPLL_120 D3
MGTAVTTRX_120 C3
MGT_120_REF_CLK_P E4
MGT_120_REF_CLK_N D4
MGTRX0_120_P A3
MGTRX0_120_N A2
MGTRX1_120_P D1
MGTRX1_120_N C1
U9
MGTAVCC_120
MGTAVCC_120_1
MGTAVCCPLL_120
MGTAVTTRX_120
MGT_120_REF_CLK_P
MGT_120_REF_CLK_N
MGTRX0_120_P
MGTRX0_120_N
MGTRX1_120_P
MGTRX1_120_N
MGTAVTTTX_120_1 E3
MGTAVTTTX_120 C4
MGTTX0_120_P B4
MGTTX0_120_N B3
MGTTX1_120_P E2
MGTTX1_120_N D2
MGT_AVTT
FB31 220@100M
FB32 220@100M
C415 220NF 6.3V
C414 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVTTTX_120_1
MGTAVTTTX_120
MGTTX0_120_P
MGTTX0_120_N
MGTTX1_120_P
MGTTX1_120_N
P6
S39 DL0P
S40 DL0N
S41 DL1P
S42 DL1N
S43 DL2P
S44 DL2N
S45 DL3P
S46 DL3N
S54 SL0P
S53 SL0N
S52 SL1P
S51 SL1N
S50 SL2P
S49 SL2N
S48 SL3P
S47 SL3N
FCN-268F036-G/3DB
SIG_GND1 G20
SIG_GND2 G21
SIG_GND3 G22
SIG_GND4 G23
SIG_GND5 G24
SIG_GND6 G25
SIG_GND7 G26
SIG_GND8 G27
SIG_GND9 G28
SIG_GND10 G19
ODIS
FAULT
R239 10K
C446 10NF 6.3V
C448 10NF 6.3V
3V3
R229 150R
OPTICAL MODULE FAULT - RED LED
JP21
R228 5K1
R227 3K9
R226 6K8
R225 3K9
C447 10NF 6.3V
U44 MAX9032AKA
U43 MAX9032AKA
U45 AND2 SN74AHC1G08DCKR
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB37 220@100M
FB38 220@100M
FB35 220@100M
FB36 220@100M
C421 220NF 6.3V
C420 220NF 6.3V
C419 220NF 6.3V
C418 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_122 AJ4
MGTAVCC_122_1 AK5
MGTAVCCPLL_122 AM4
MGTAVTTRX_122 AL3
MGT_122_REF_CLK_P AL5
MGT_122_REF_CLK_N AL4
MGTRX0_122_P AL1
MGTRX0_122_N AM1
MGTRX1_122_P AP3
MGTRX1_122_N AP2
U9
MGTAVCC_122
MGTAVCC_122_1
MGTAVCCPLL_122
MGTAVTTRX_122
MGT_122_REF_CLK_P
MGT_122_REF_CLK_N
MGTRX0_122_P
MGTRX0_122_N
MGTRX1_122_P
MGTRX1_122_N
MGTAVTTTX_122_1 AM3
MGTAVTTTX_122 AK3
MGTTX0_122_P AK2
MGTTX0_122_N AL2
MGTTX1_122_P AN4
MGTTX1_122_N AN3
MGT_AVTT
FB34 220@100M
FB33 220@100M
C416 220NF 6.3V
C417 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVTTTX_122_1
MGTAVTTTX_122
MGTTX0_122_P
MGTTX0_122_N
MGTTX1_122_P
MGTTX1_122_N
U41 TPS2031D
R224 10K
C445 10NF 6.3V
C444 100NF 6.3V
C408 4.7UF 16V
C406 22UF 16V
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB48 220@100M
FB47 220@100M
FB50 220@100M
FB49 220@100M
C441 220NF 6.3V
C442 220NF 6.3V
C432 220NF 6.3V
C443 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_126 AL8
MGTAVCC_126_1 AM8
MGTAVCCPLL_126 AM9
MGTAVTTRX_126 AM6
MGT_126_REF_CLK_P AL7
MGT_126_REF_CLK_N AM7
MGTRX0_126_P AP6
MGTRX0_126_N AP7
MGTRX1_126_P AP9
MGTRX1_126_N AP8
U9
MGTAVCC_126
MGTAVCC_126_1
MGTAVCCPLL_126
MGTAVTTRX_126
MGT_126_REF_CLK_P
MGT_126_REF_CLK_N
MGTRX0_126_P
MGTRX0_126_N
MGTRX1_126_P
MGTRX1_126_N
MGTAVTTTX_126_1 AM5
MGTAVTTTX_126 AM10
MGTTX0_126_P AN5
MGTTX0_126_N AN6
MGTTX1_126_P AN10
MGTTX1_126_N AN9
MGT_AVTT
FB45 220@100M
FB46 220@100M
C440 220NF 6.3V
C439 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVTTTX_126_1
MGTAVTTTX_126
MGTTX0_126_P
MGTTX0_126_N
MGTTX1_126_P
MGTTX1_126_N
P6
S57 DL0P
S58 DL0N
S59 DL1P
S60 DL1N
S61 DL2P
S62 DL2N
S63 DL3P
S64 DL3N
S72 SL0P
S71 SL0N
S70 SL1P
S69 SL1N
S68 SL2P
S67 SL2N
S66 SL3P
S65 SL3N
FCN-268F036-G/3DB
SIG_GND1 G29
SIG_GND2 G30
SIG_GND3 G31
SIG_GND4 G32
SIG_GND5 G33
SIG_GND6 G34
SIG_GND7 G35
SIG_GND8 G36
SIG_GND9 G37
SIG_GND10 G19
ODIS
FAULT
R233 10K
C451 10NF 6.3V
C449 10NF 6.3V
3V3
R232 150R
OPTICAL MODULE FAULT - RED LED
JP22
R233 5K1
R234 3K9
R235 6K8
R236 3K9
C450 10NF 6.3V
U44 MAX9032AKA
U43 MAX9032AKA
U46 AND2 SN74AHC1G08DCKR
U42 TPS2031D
R237 10K
C452 10NF 6.3V
C453 100NF 6.3V
C409 4.7UF 16V
C407 22UF 16V


PADD[2:31]
3V3
External Slave Peripheral
External Master Peripheral Interface
NO POP
To Boot from NAND, install jumper
UART
IIC0
IIC1_SPI
NAND Flash Interface
BANKS=1, 2, 4
CHIP SELECT 1
U9
UART Port 0
J7
UART Port 1
HLE-105-02-G-DV


P16 QSH-040-01-L-D-DP-A-K
QSH_A_D_P[0] 1 DP0_0
QSH_A_D_N[0] 3 DP0_1
QSH_A_D_P[1] 5 DP1_0
QSH_A_D_N[1] 7 DP1_1
QSH_A_D_P[2] 9 DP2_0
QSH_A_D_N[2] 11 DP2_1
QSH_A_D_P[3] 13 DP3_0
QSH_A_D_N[3] 15 DP3_1
QSH_A_D_P[4] 17 DP4_0
QSH_A_D_N[4] 19 DP4_1
QSH_A_D_P[5] 21 DP5_0
QSH_A_D_N[5] 23 DP5_1
QSH_A_D_P[6] 25 DP6_0
QSH_A_D_N[6] 27 DP6_1
QSH_A_D_P[7] 29 DP7_0
QSH_A_D_N[7] 31 DP7_1
QSH_A_D_P[8] 33 DP8_0
QSH_A_D_N[8] 35 DP8_1
QSH_A_D_P[9] 37 DP9_0
QSH_A_D_N[9] 39 DP9_1
QSH_A_D_P[10] 41 DP10_0
QSH_A_D_N[10] 43 DP10_1
QSH_A_D_P[11] 45 DP11_0
QSH_A_D_N[11] 47 DP11_1
QSH_A_D_P[12] 49 DP12_0
QSH_A_D_N[12] 51 DP12_1
QSH_A_D_P[13] 53 DP13_0
QSH_A_D_N[13] 55 DP13_1
QSH_A_D_P[14] 57 DP14_0
QSH_A_D_N[14] 59 DP14_1
QSH_A_D_P[15] 61 DP15_0
QSH_A_D_N[15] 63 DP15_1
QSH_A_D_P[16] 65 DP16_0
QSH_A_D_N[16] 67 DP16_1
QSH_A_D_P[17] 69 DP17_0
QSH_A_D_N[17] 71 DP17_1
QSH_A_D_P[18] 73 DP18_0
QSH_A_D_N[18] 75 DP18_1
QSH_A_CLK_P 77 DP19_0
QSH_A_CLK_N 79 DP19_1
DP20_0 2 QSH_B_D_P[0]
DP20_1 4 QSH_B_D_N[0]
DP21_0 6 QSH_B_D_P[1]
DP21_1 8 QSH_B_D_N[1]
DP22_0 10 QSH_B_D_P[2]
DP22_1 12 QSH_B_D_N[2]
DP23_0 14 QSH_B_D_P[3]
DP23_1 16 QSH_B_D_N[3]
DP24_0 18 QSH_B_D_P[4]
DP24_1 20 QSH_B_D_N[4]
DP25_0 22 QSH_B_D_P[5]
DP25_1 24 QSH_B_D_N[5]
DP26_0 26 QSH_B_D_P[6]
DP26_1 28 QSH_B_D_N[6]
DP27_0 30 QSH_B_D_P[7]
DP27_1 32 QSH_B_D_N[7]
DP28_0 34 QSH_B_D_P[8]
DP28_1 36 QSH_B_D_N[8]
DP29_0 38 QSH_B_D_P[9]
DP29_1 40 QSH_B_D_N[9]
DP30_0 42 QSH_B_D_P[10]
DP30_1 44 QSH_B_D_N[10]
DP31_0 46 QSH_B_D_P[11]
DP31_1 48 QSH_B_D_N[11]
DP32_0 50 QSH_B_D_P[12]
DP32_1 52 QSH_B_D_N[12]
DP33_0 54 QSH_B_D_P[13]
DP33_1 56 QSH_B_D_N[13]
DP34_0 58 QSH_B_D_P[14]
DP34_1 60 QSH_B_D_N[14]
DP35_0 62 QSH_B_D_P[15]
DP35_1 64 QSH_B_D_N[15]
DP36_0 66 QSH_B_D_P[16]
DP36_1 68 QSH_B_D_N[16]
DP37_0 70 QSH_B_D_P[17]
DP37_1 72 QSH_B_D_N[17]
DP38_0 74 QSH_B_D_P[18]
DP38_1 76 QSH_B_D_N[18]
DP39_0 78 QSH_B_CLK_P
DP39_1 80 QSH_B_CLK_N
GND1 81
GND2 82
GND3 83
GND4 84
GND5 85
GND6 86
GND7 87
GND8 88
MNT1 89
MNT2 90
QSH_A_D_P[18] F24 QSH_A_D_P[18]
QSH_A_D_N[18] E24 QSH_A_D_N[18]
QSH_A_D_P[17] F14 QSH_A_D_P[17]
QSH_A_D_N[17] F15 QSH_A_D_N[17]
QSH_A_D_P[16] D24 QSH_A_D_P[16]
QSH_A_D_N[16] E23 QSH_A_D_N[16]
QSH_A_D_P[15] G17 QSH_A_D_P[15]
QSH_A_D_N[15] F16 QSH_A_D_N[15]
QSH_A_D_P[14] E22 QSH_A_D_P[14]
QSH_A_D_N[14] F23 QSH_A_D_N[14]
QSH_A_D_P[13] F18 QSH_A_D_P[13]
QSH_A_D_N[13] G18 QSH_A_D_N[13]
QSH_A_D_P[12] D21 QSH_A_D_P[12]
QSH_A_D_N[12] D22 QSH_A_D_N[12]
QSH_A_D_P[11] F21 QSH_A_D_P[11]
QSH_A_D_N[11] G21 QSH_A_D_N[11]
QSH_A_D_P[10] E17 QSH_A_D_P[10]
QSH_A_D_N[10] E16 QSH_A_D_N[10]
QSH_A_D_P[9] D14 QSH_A_D_P[9]
QSH_A_D_N[9] E14 QSH_A_D_N[9]
QSH_A_D_P[8] G20 QSH_A_D_P[8]
QSH_A_D_N[8] F20 QSH_A_D_N[8]
QSH_A_D_P[7] D16 QSH_A_D_P[7]
QSH_A_D_N[7] D15 QSH_A_D_N[7]
QSH_A_D_P[6] E21 QSH_A_D_P[6]
QSH_A_D_N[6] D20 QSH_A_D_N[6]
QSH_A_D_P[5] C17 QSH_A_D_P[5]
QSH_A_D_N[5] D17 QSH_A_D_N[5]
QSH_A_D_P[4] E19 QSH_A_D_P[4]
QSH_A_D_N[4] F19 QSH_A_D_N[4]
QSH_A_D_P[3] C14 QSH_A_D_P[3]
QSH_A_D_N[3] C15 QSH_A_D_N[3]
QSH_A_D_P[2] B17 QSH_A_D_P[2]
QSH_A_D_N[2] A16 QSH_A_D_N[2]
QSH_A_D_P[1] A15 QSH_A_D_P[1]
QSH_A_D_N[1] A14 QSH_A_D_N[1]
QSH_A_D_P[0] B16 QSH_A_D_P[0]
QSH_A_D_N[0] B15 QSH_A_D_N[0]
QSH_A_CLK_P J20 QSH_A_CLK_P
QSH_A_CLK_N J21 QSH_A_CLK_N
2V5_5
R302 100R
R303 100R
VRP_5 D19 VRP_5
VRN_5 E18 VRN_5
2V5
B19 2V5_5
C16 2V5_5_1
F17 2V5_5_2
C570 100NF 10V
C569 100NF 10V
C568 100NF 10V
U9
BANKS=5, 6
QSH_B_D_P[18] AM17 QSH_B_D_P[18]
QSH_B_D_N[18] AN17 QSH_B_D_N[18]
QSH_B_D_P[17] AN15 QSH_B_D_P[17]
QSH_B_D_N[17] AP15 QSH_B_D_N[17]
QSH_B_D_P[16] AP16 QSH_B_D_P[16]
QSH_B_D_N[16] AP17 QSH_B_D_N[16]
QSH_B_D_P[15] AM15 QSH_B_D_P[15]
QSH_B_D_N[15] AM16 QSH_B_D_N[15]
QSH_B_D_P[14] AJ19 QSH_B_D_P[14]
QSH_B_D_N[14] AK19 QSH_B_D_N[14]
QSH_B_D_P[13] AK18 QSH_B_D_P[13]
QSH_B_D_N[13] AL18 QSH_B_D_N[13]
QSH_B_D_P[12] AL19 QSH_B_D_P[12]
QSH_B_D_N[12] AL20 QSH_B_D_N[12]
QSH_B_D_P[11] AL21 QSH_B_D_P[11]
QSH_B_D_N[11] AK21 QSH_B_D_N[11]
QSH_B_D_P[10] AK16 QSH_B_D_P[10]
QSH_B_D_N[10] AL16 QSH_B_D_N[10]
QSH_B_D_P[9] AJ16 QSH_B_D_P[9]
QSH_B_D_N[9] AJ15 QSH_B_D_N[9]
QSH_B_D_P[8] AJ21 QSH_B_D_P[8]
QSH_B_D_N[8] AJ20 QSH_B_D_N[8]
QSH_B_D_P[7] AL15 QSH_B_D_P[7]
QSH_B_D_N[7] AL14 QSH_B_D_N[7]
QSH_B_D_P[6] AK23 QSH_B_D_P[6]
QSH_B_D_N[6] AK22 QSH_B_D_N[6]
QSH_B_D_P[5] AJ14 QSH_B_D_P[5]
QSH_B_D_N[5] AK14 QSH_B_D_N[5]
QSH_B_D_P[4] AK24 QSH_B_D_P[4]
QSH_B_D_N[4] AL23 QSH_B_D_N[4]
QSH_B_D_P[3] AL13 QSH_B_D_P[3]
QSH_B_D_N[3] AK13 QSH_B_D_N[3]
QSH_B_D_P[2] AH23 QSH_B_D_P[2]
QSH_B_D_N[2] AJ22 QSH_B_D_N[2]
QSH_B_D_P[1] AK12 QSH_B_D_P[1]
QSH_B_D_N[1] AJ12 QSH_B_D_N[1]
QSH_B_D_P[0] AH24 QSH_B_D_P[0]
QSH_B_D_N[0] AJ24 QSH_B_D_N[0]
QSH_B_CLK_P J14 QSH_B_CLK_P
QSH_B_CLK_N H13 QSH_B_CLK_N
2V5_6
R301 100R
R300 100R
VRP_6 AJ17 VRP_6
VRN_6 AK17 VRN_6
2V5
AN16 2V5_6_2
AK15 2V5_6_1
AJ18 2V5_6
C573 100NF 10V
C572 100NF 10V
C571 100NF 10V