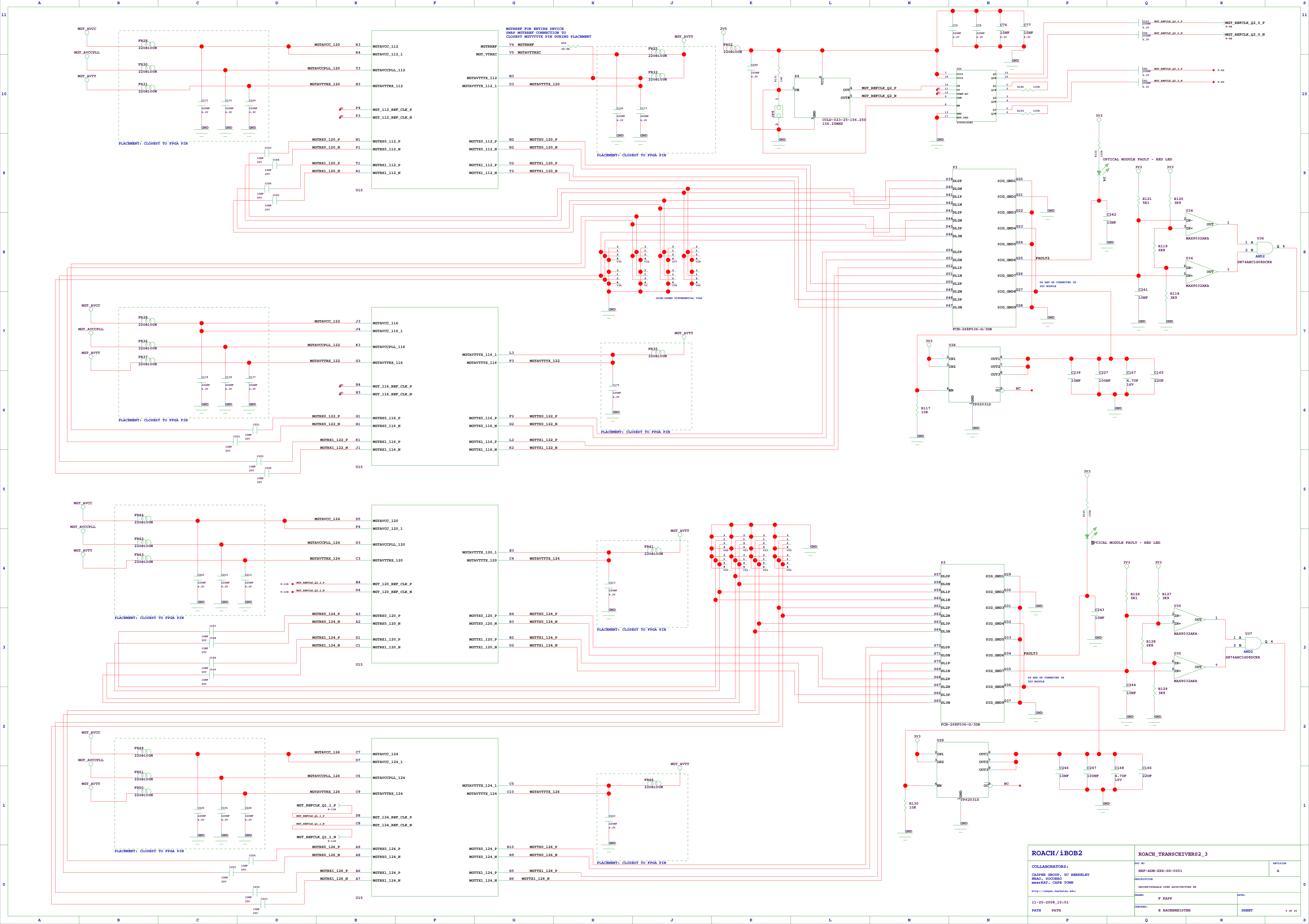
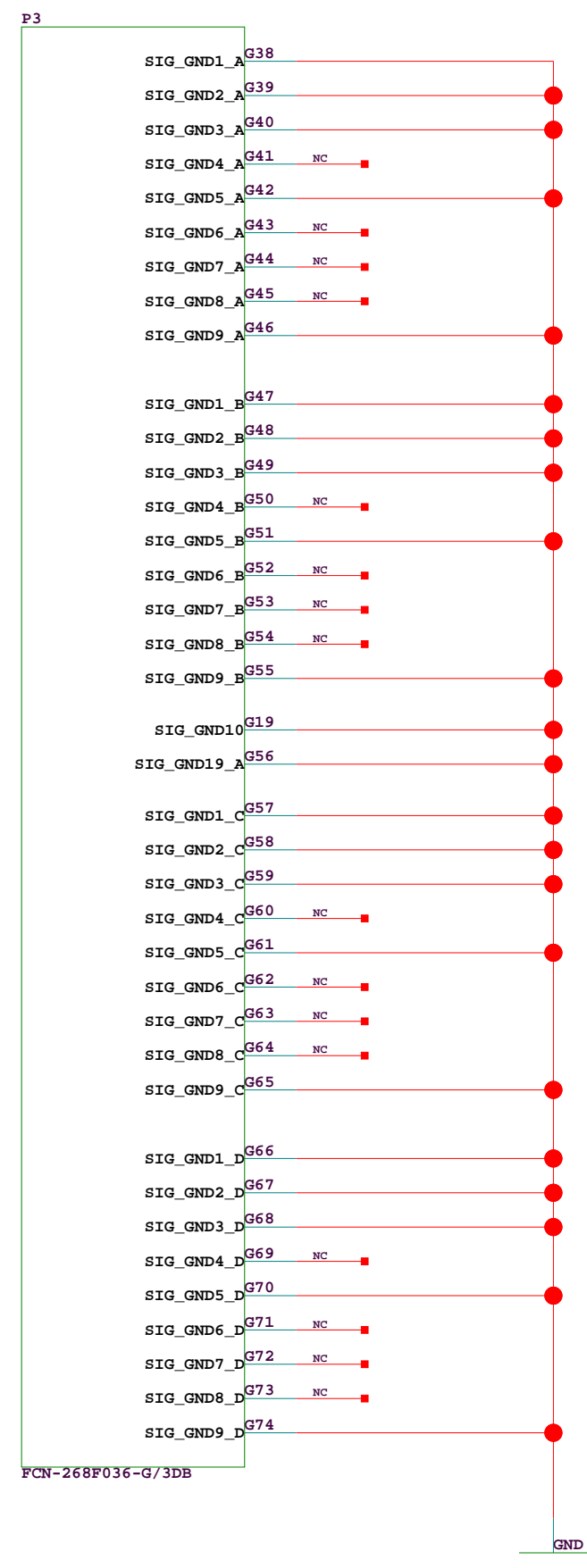
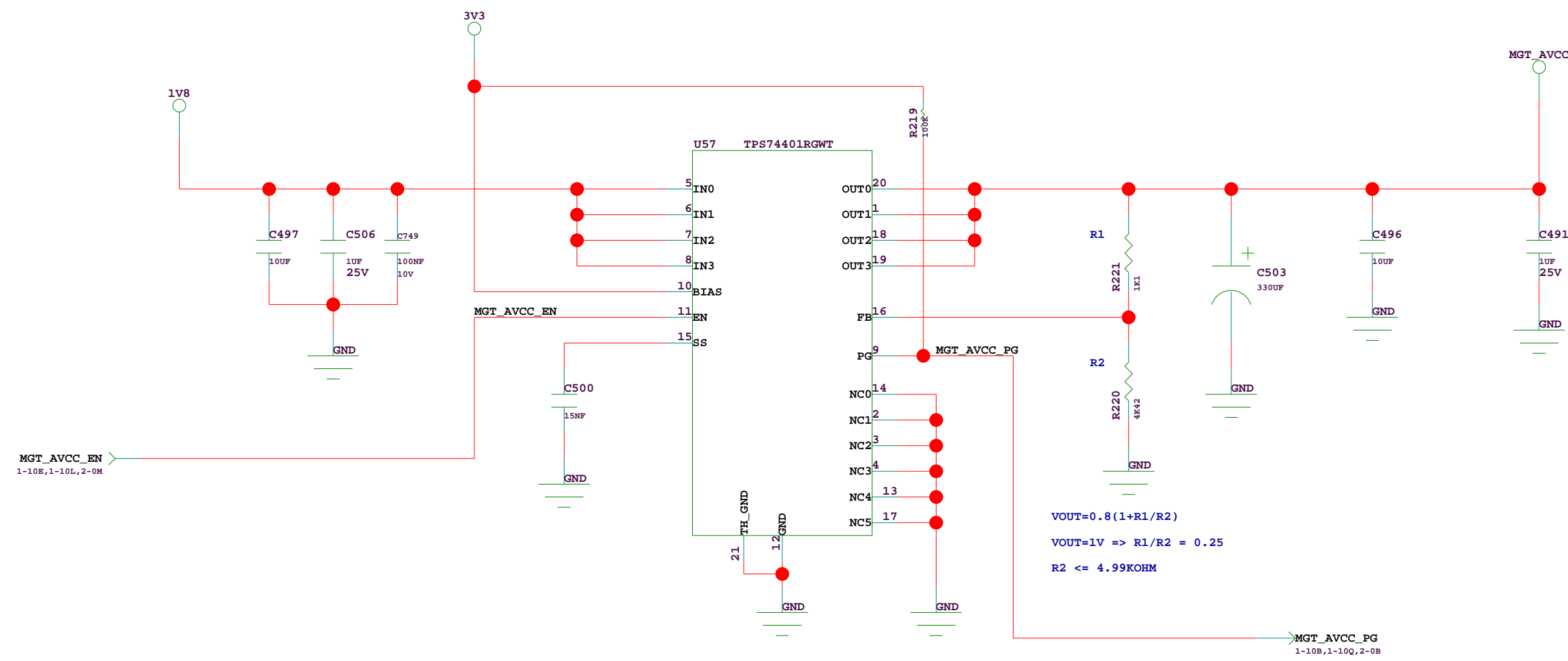
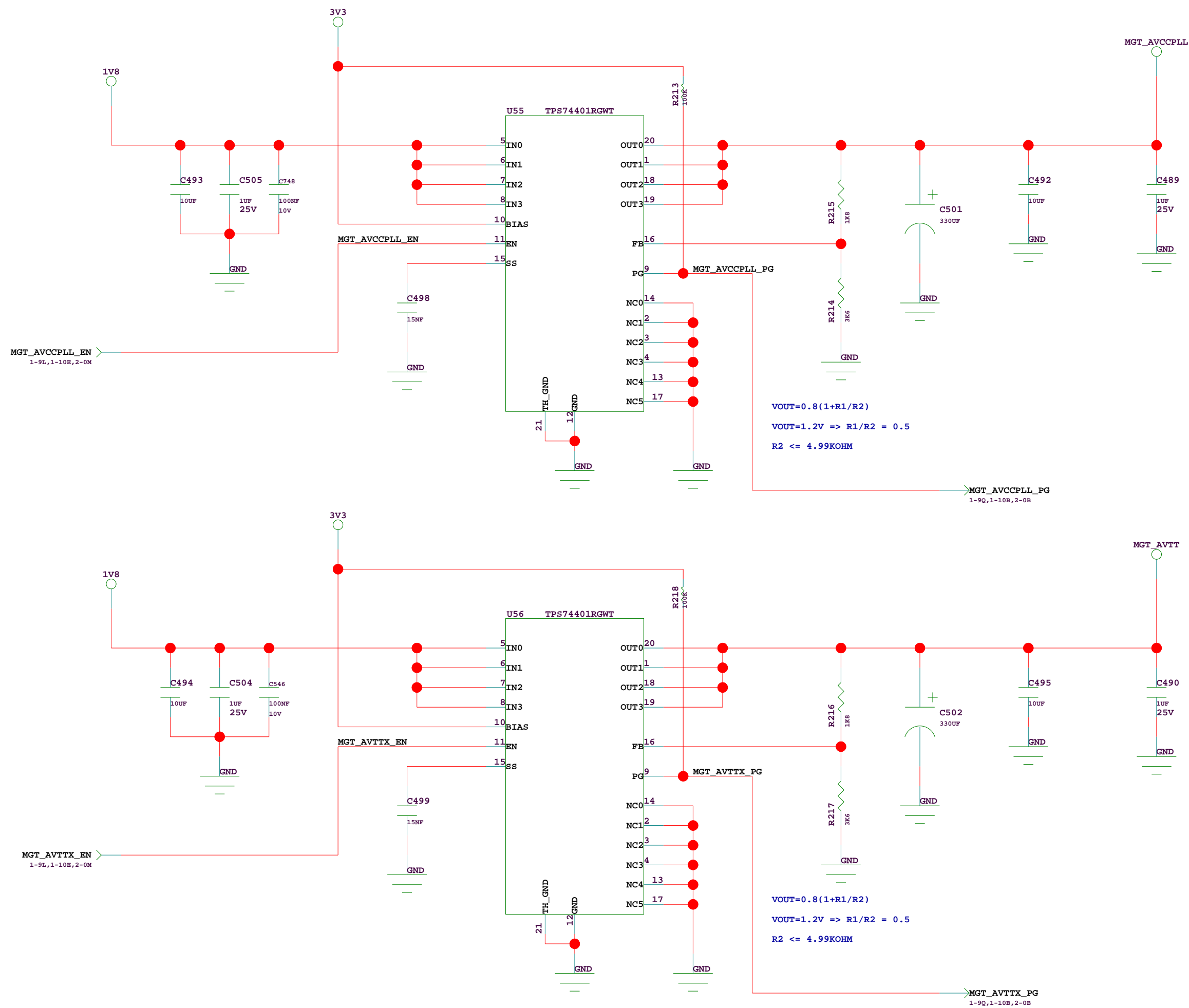
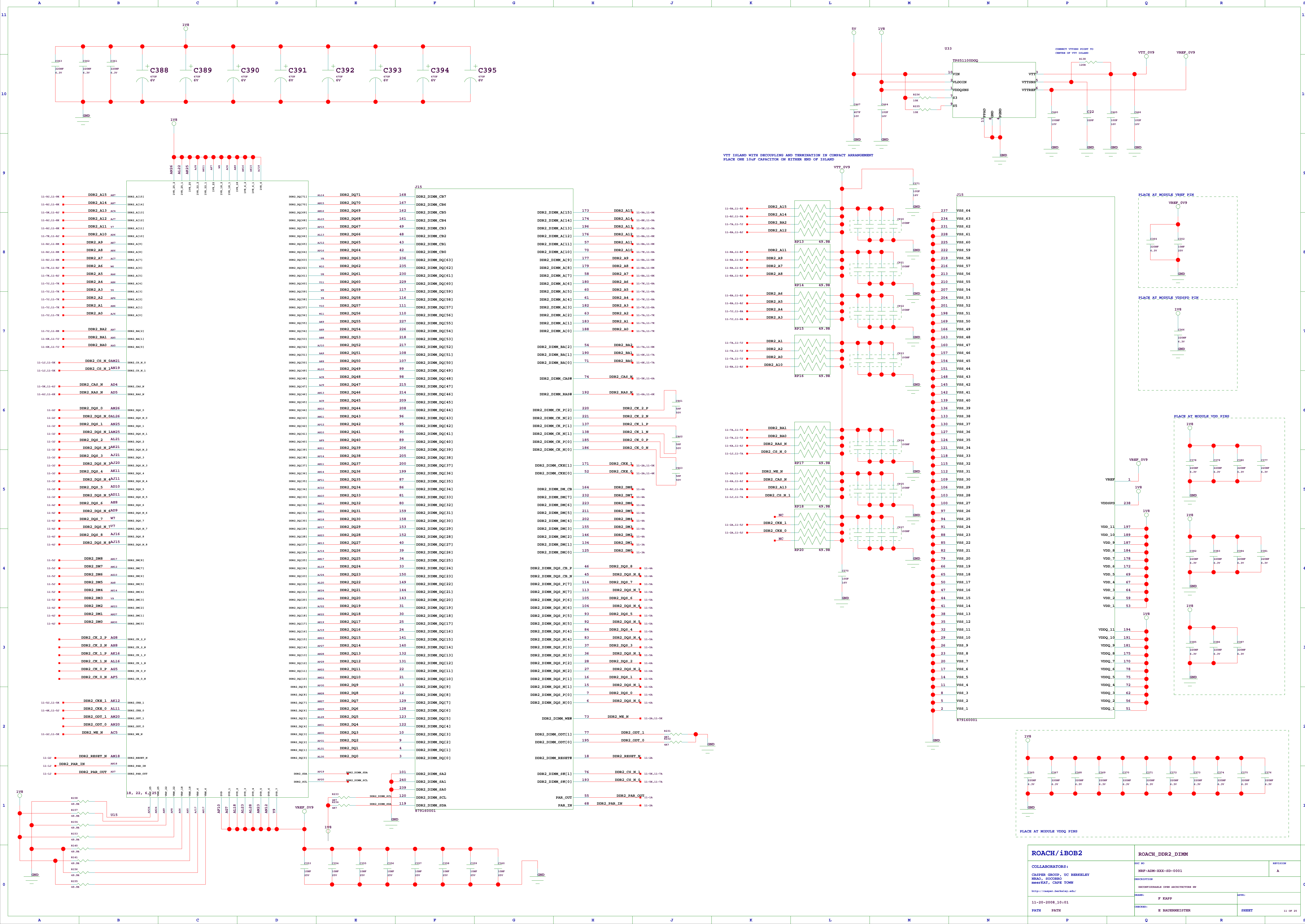


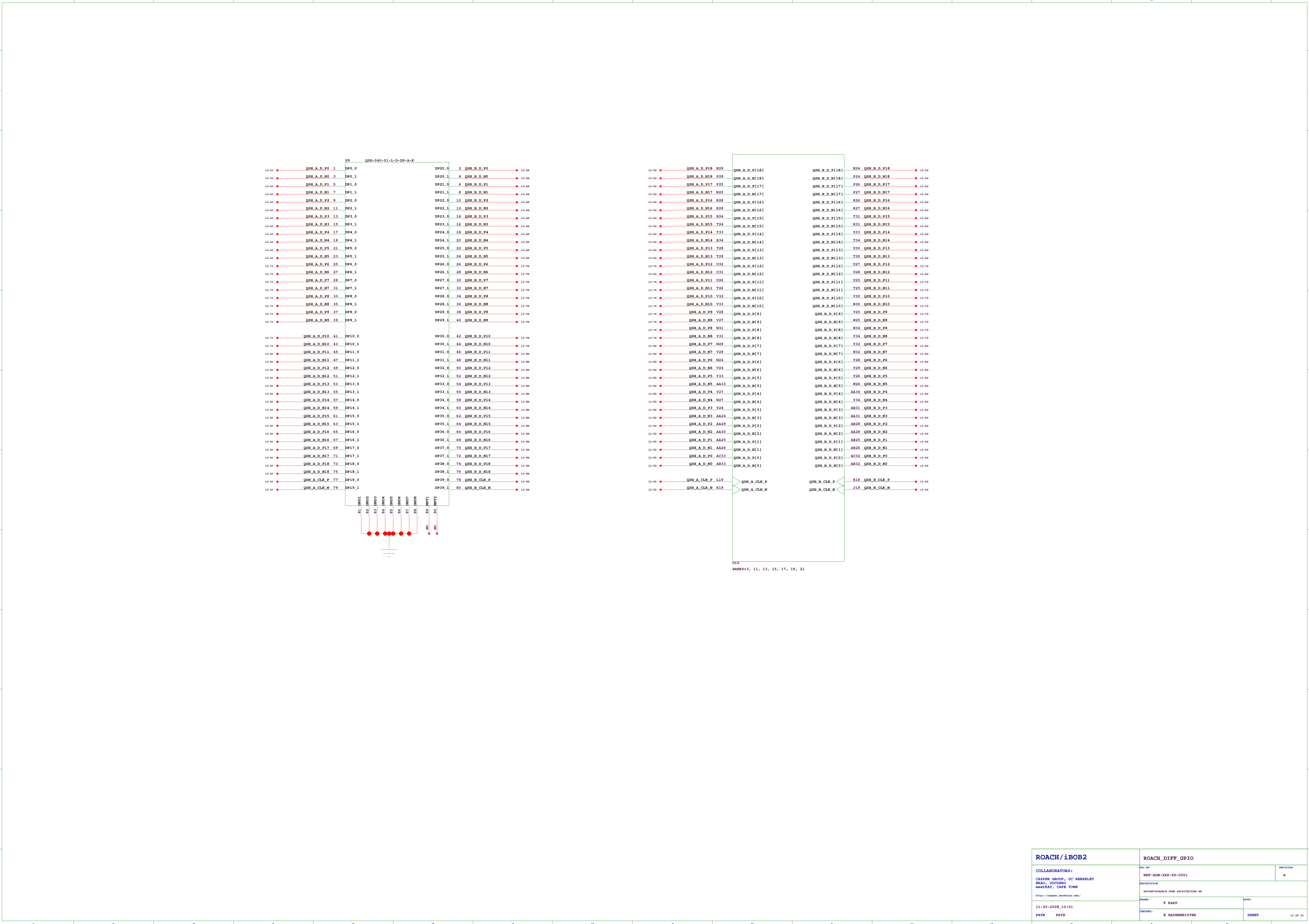
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COLLABORATORS:			DOC NO	REV/ISSN	
CASPER GROUP, UC BERKELEY			NRF-ADM-XXX-BD-0001	A	
NRAO, SOCCORRO			DESCRIPTION		
MesaCAT, CAPE TOWN			RECONFIGURABLE OPEN ARCHITECTURE HW		
http://casper.berkeley.edu/			ISSN:	ISSN:	
11-20-2008_10:01			F KAPP		
PATH			CHECKED:	R BAUERMEISTER	
				SHEET	



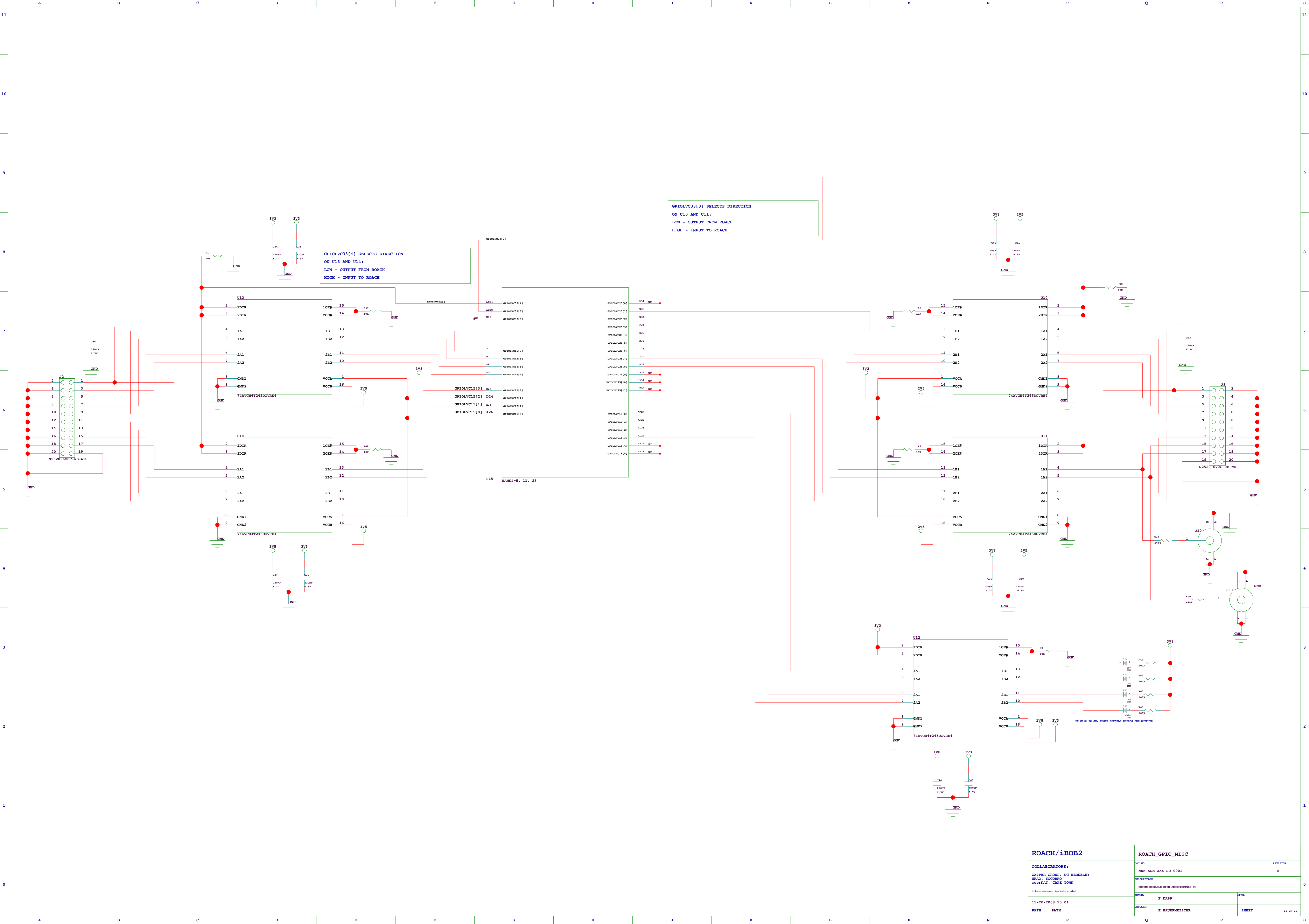


ROACH/iBOE2		ROACH_TRANSCEIVERS_PSU	
COLLABORATORS:		DOC NO:	REVISION:
CASPER GROUP, UC BERKELEY		NRF-ADM-XXX-SD-0001	A
NRAO, SOCORRO		DESCRIPTION:	
BANKAT, CAPE TOWN		RECONFIGURABLE OPEN ARCHITECTURE HW	
http://casper.berkeley.edu/		DRAWN:	APPD:
11-20-2008_10.01		F KAPP	
PATH	PATH	CHECKED:	SHEET
P	Q	E BAUERMEISTER	10 OF 25

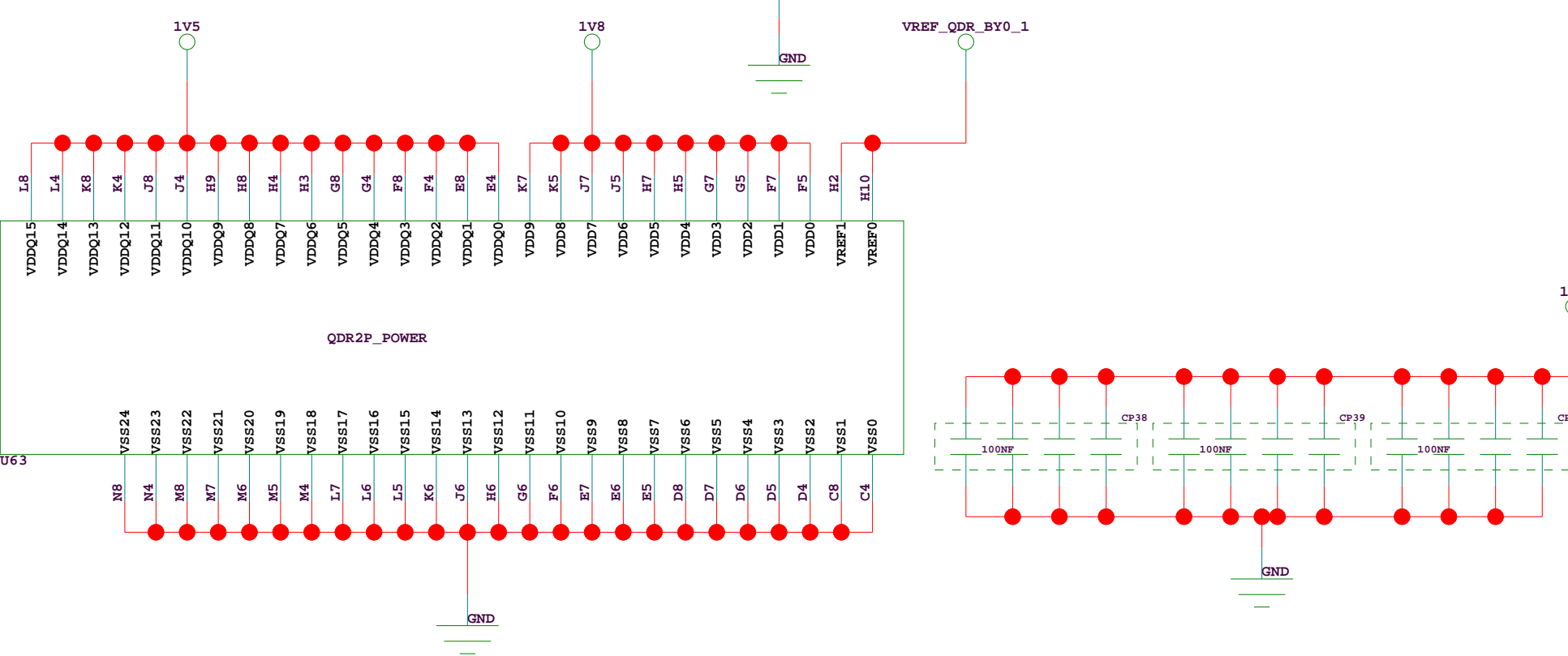
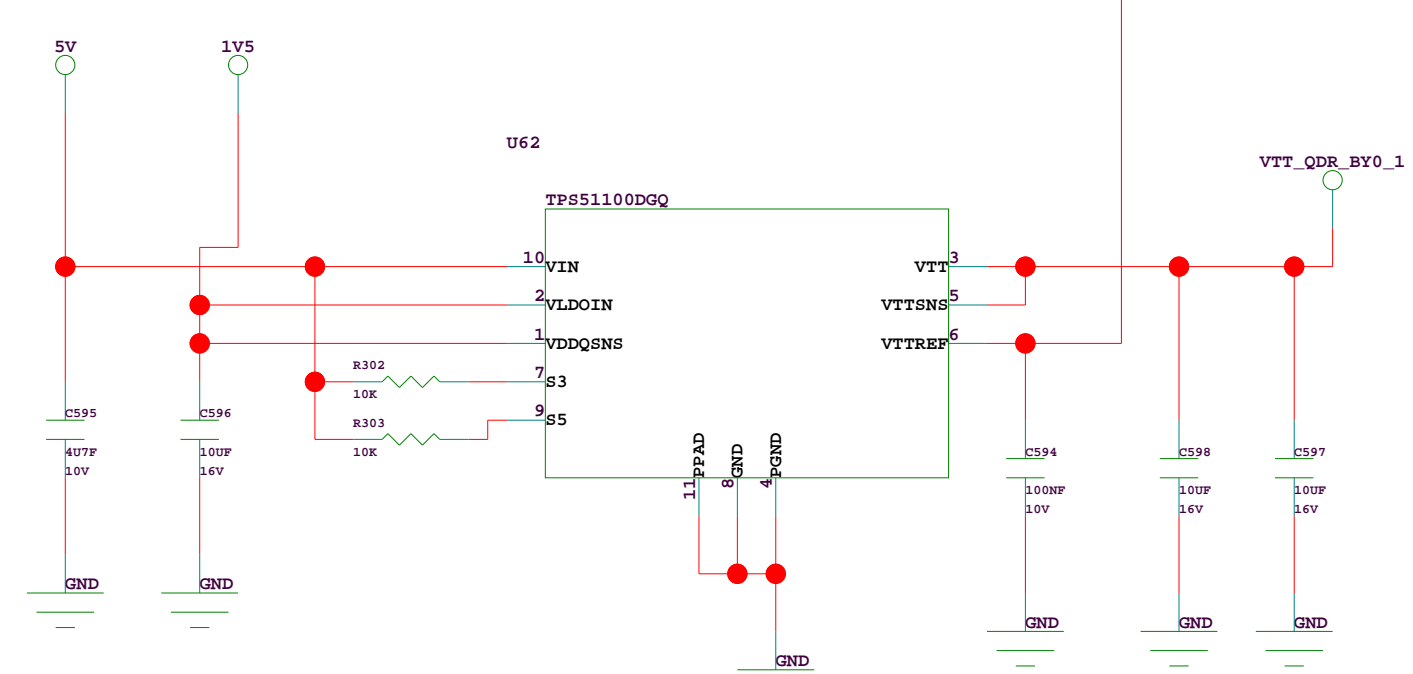
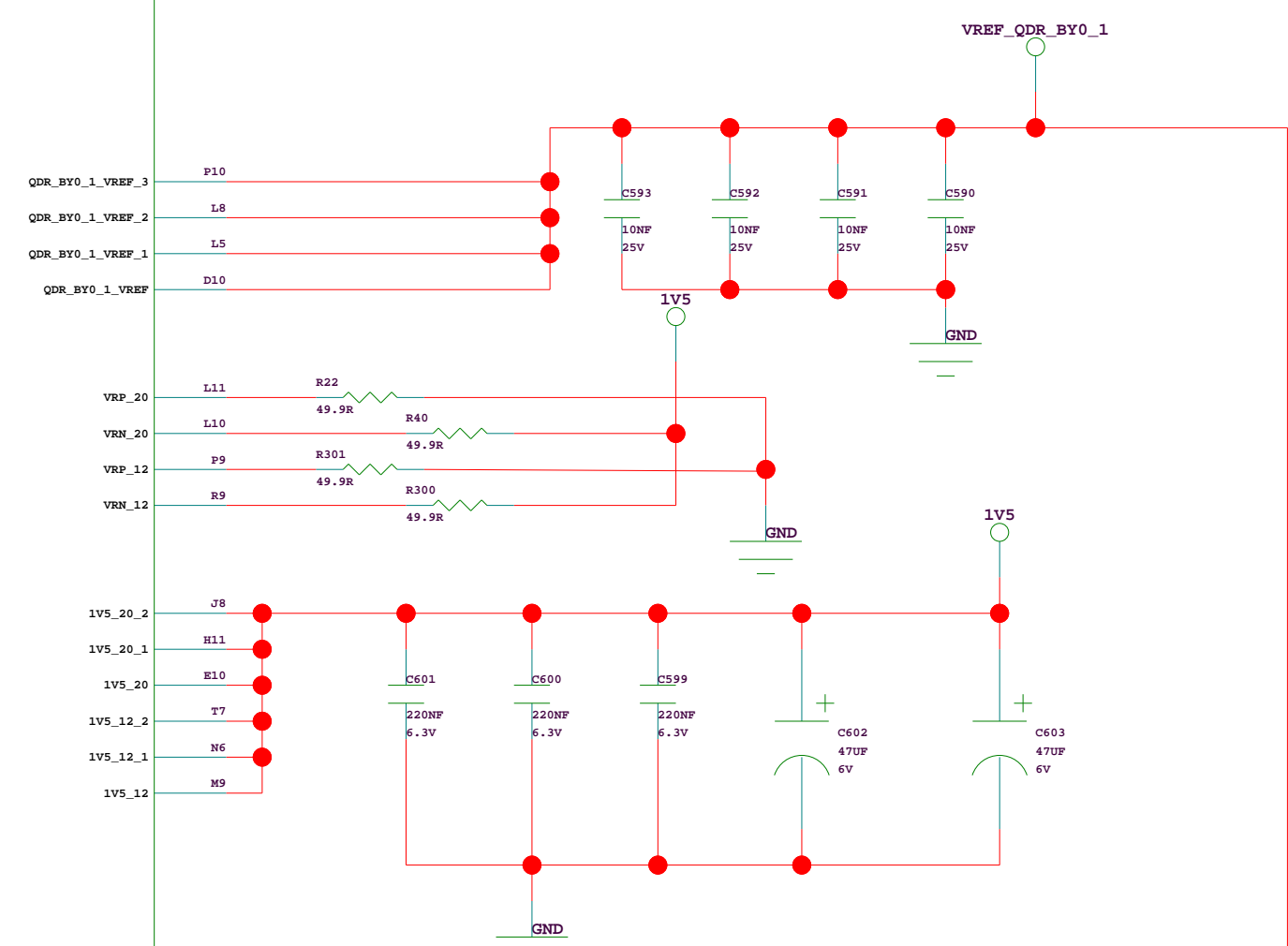
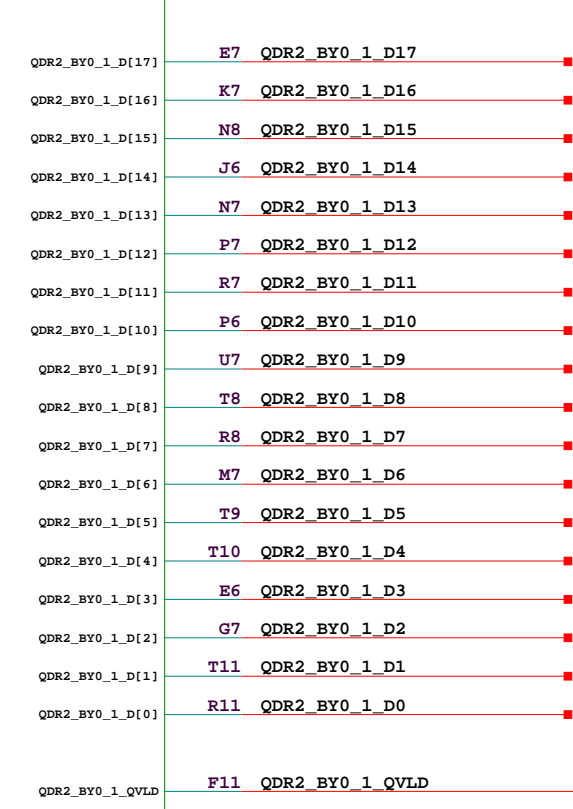
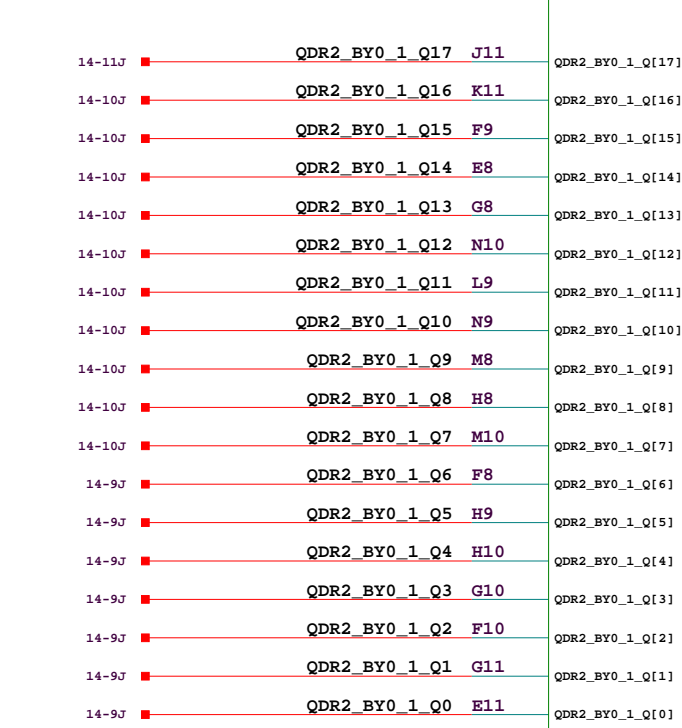
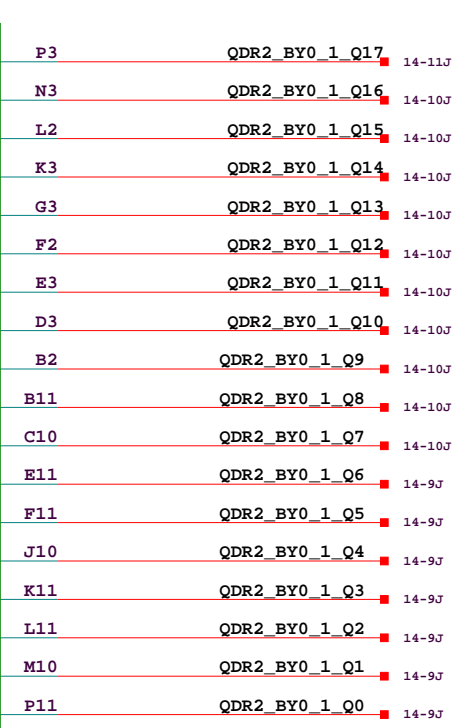
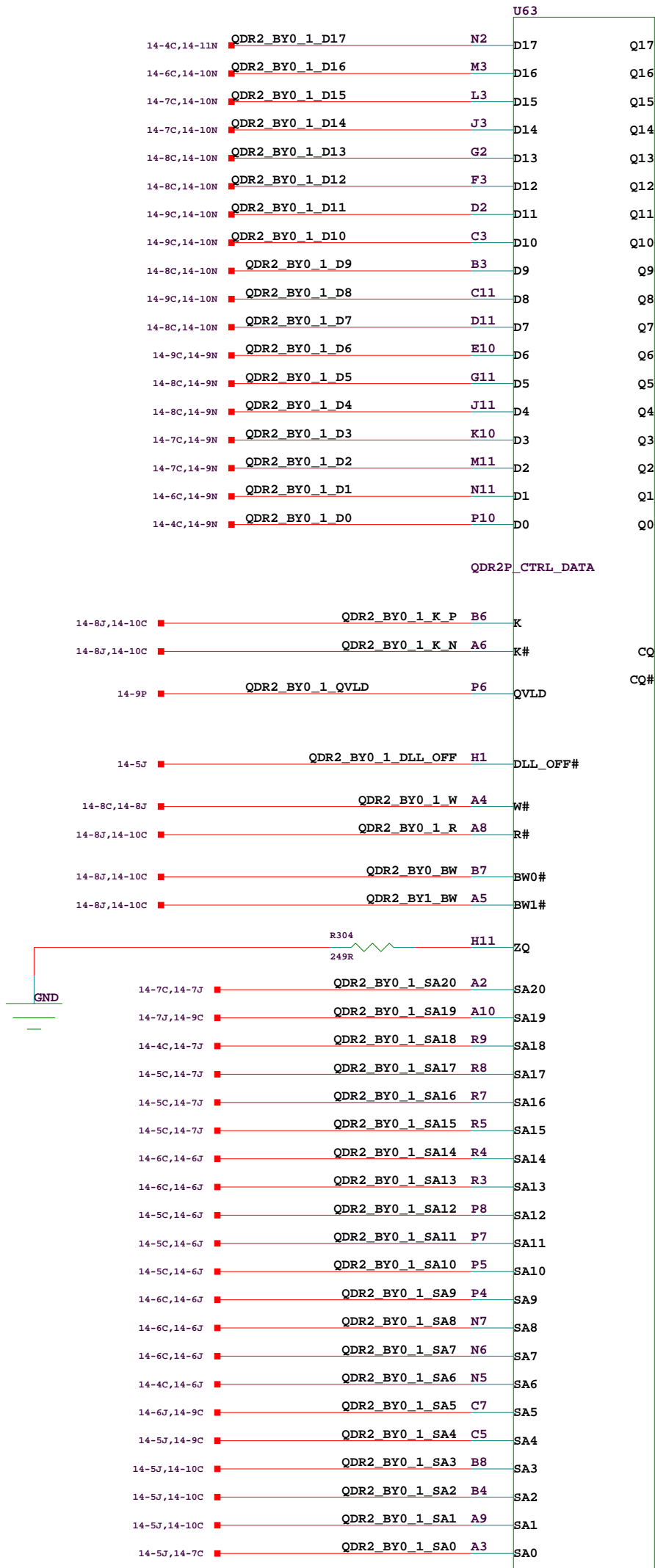
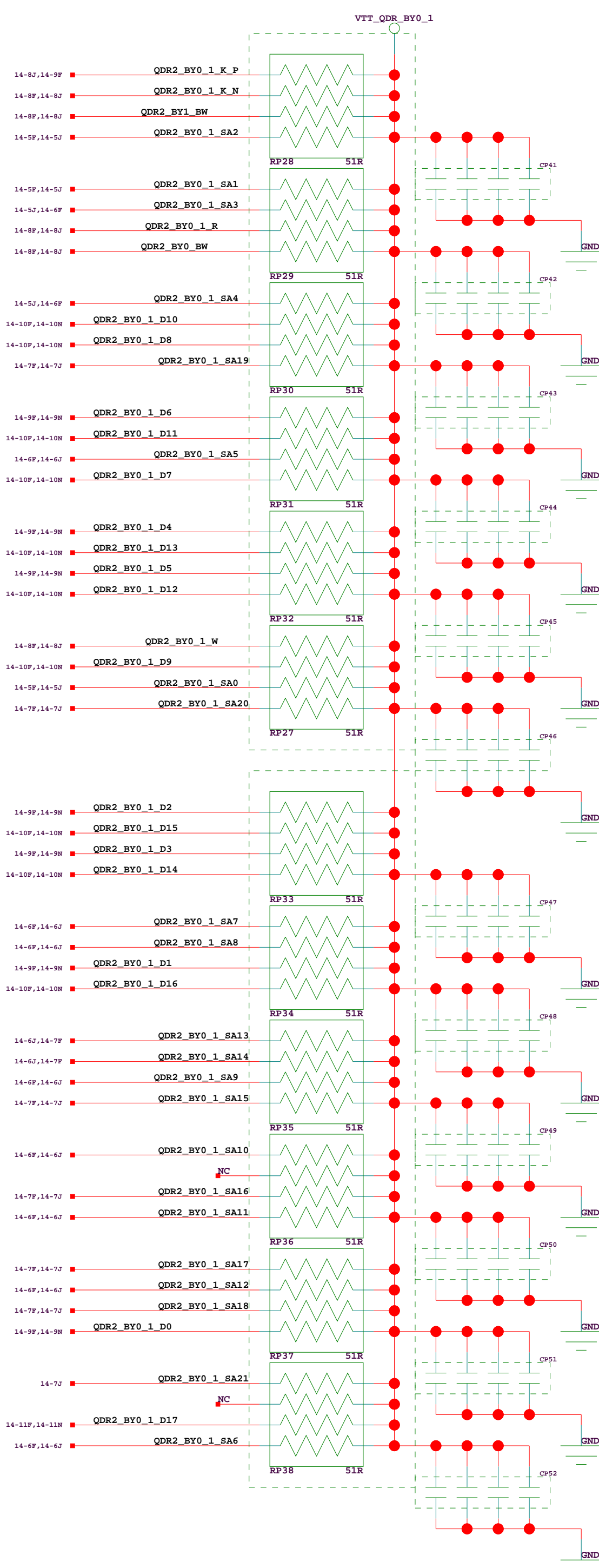




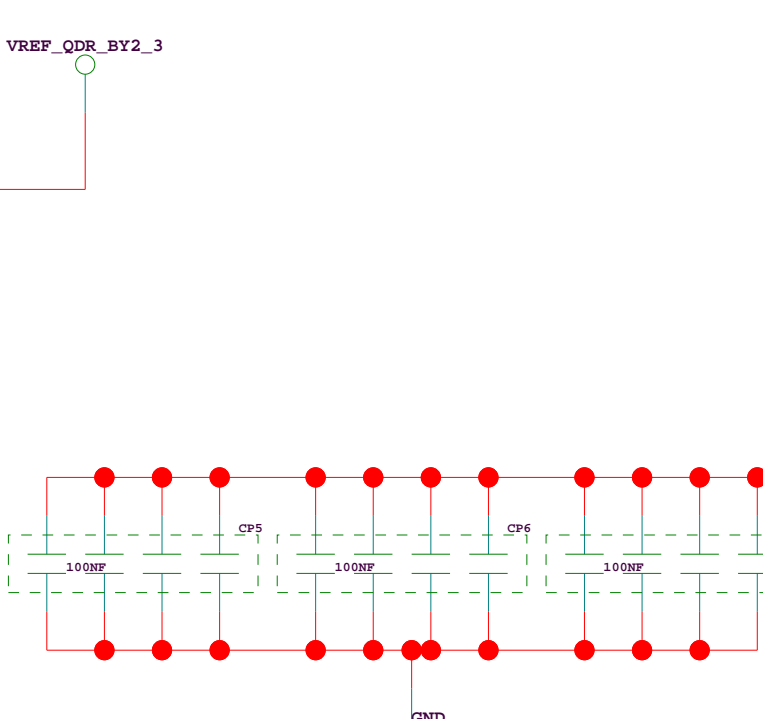
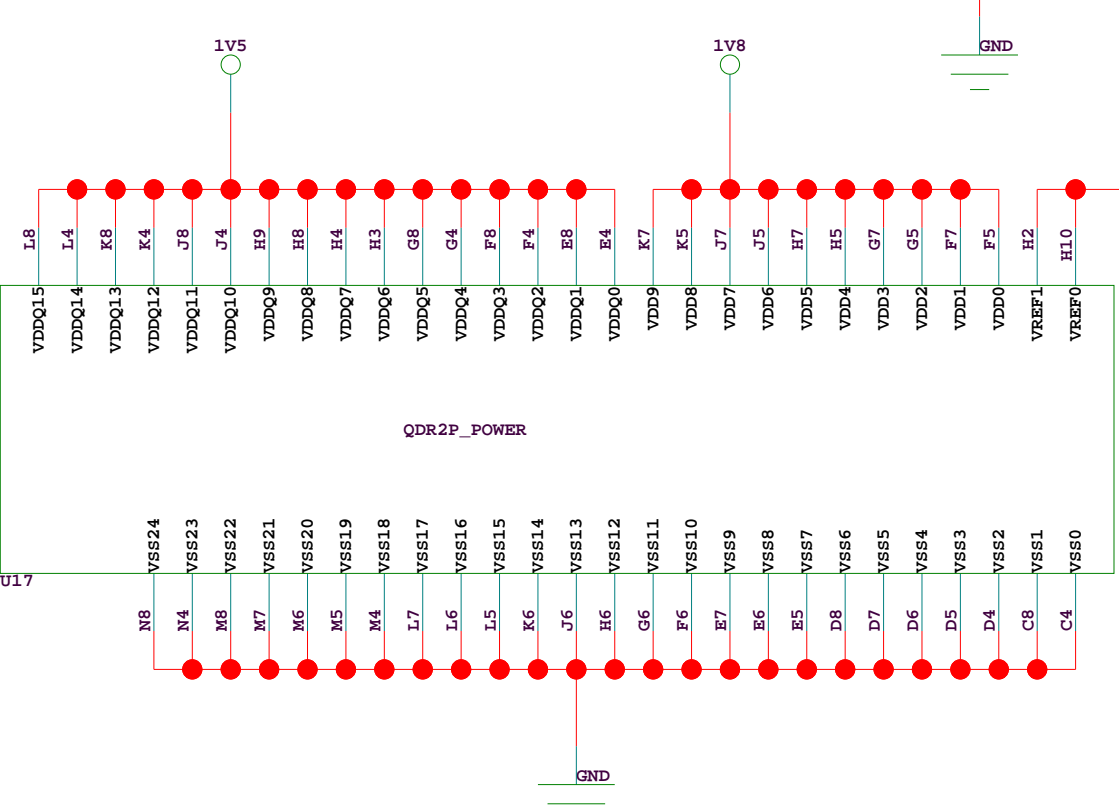
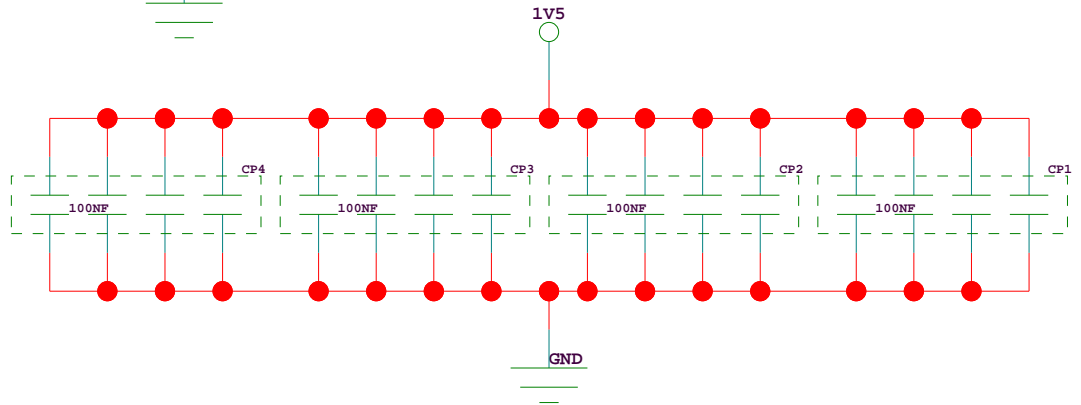
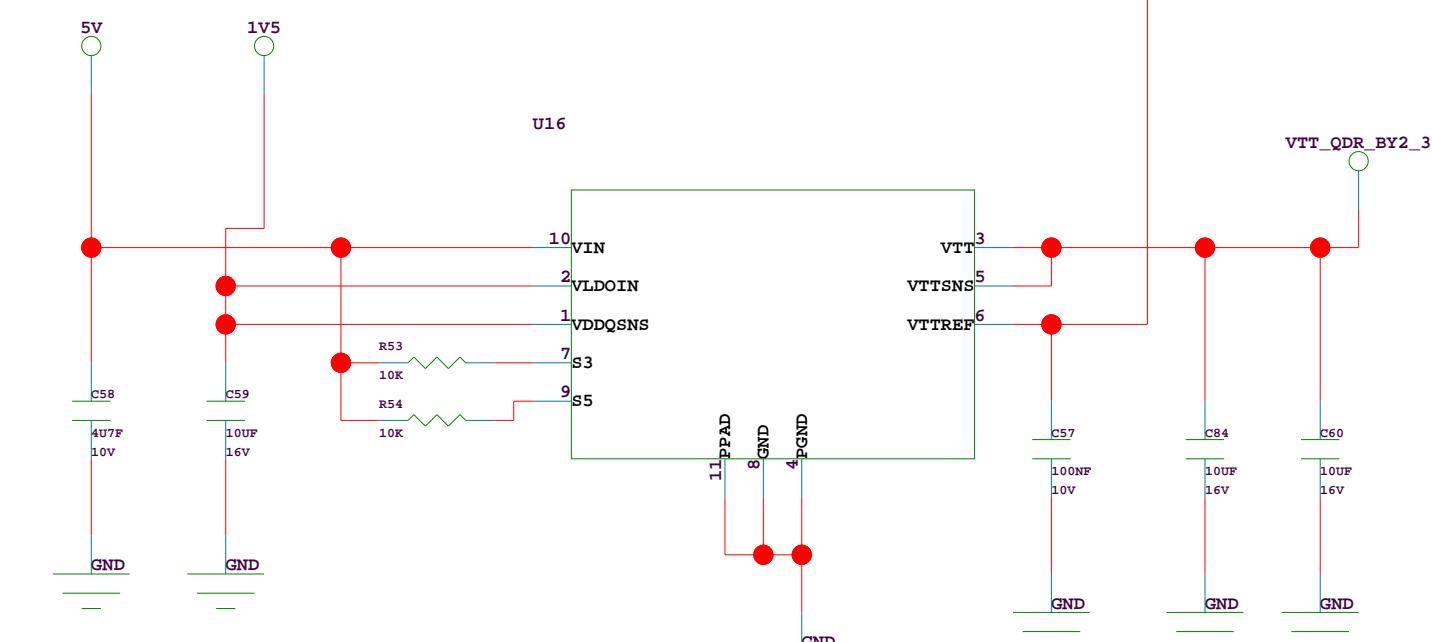
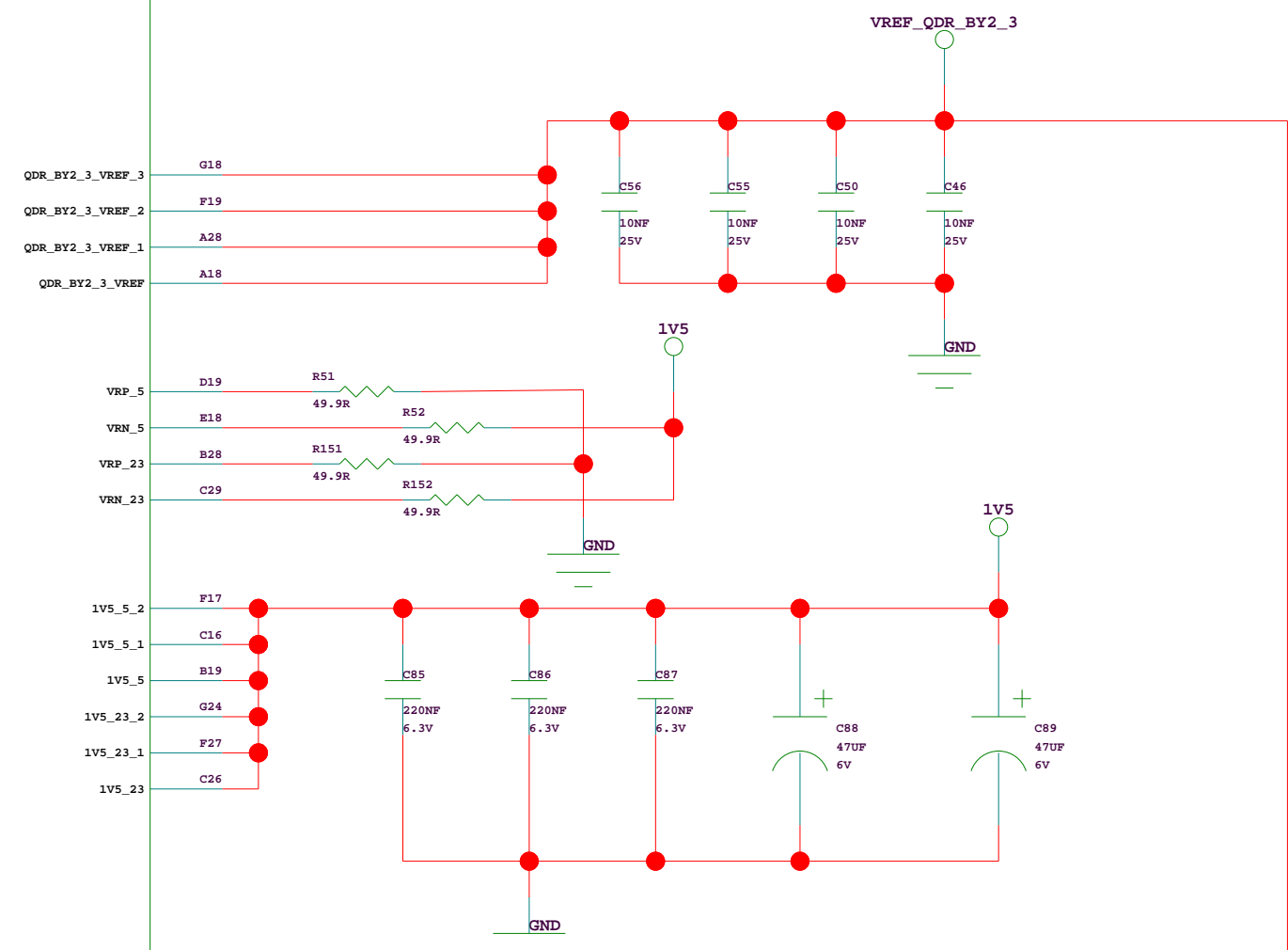
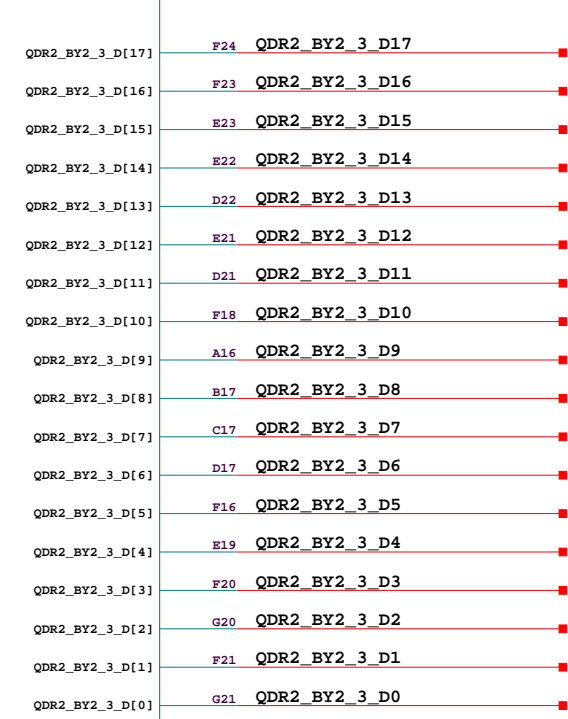
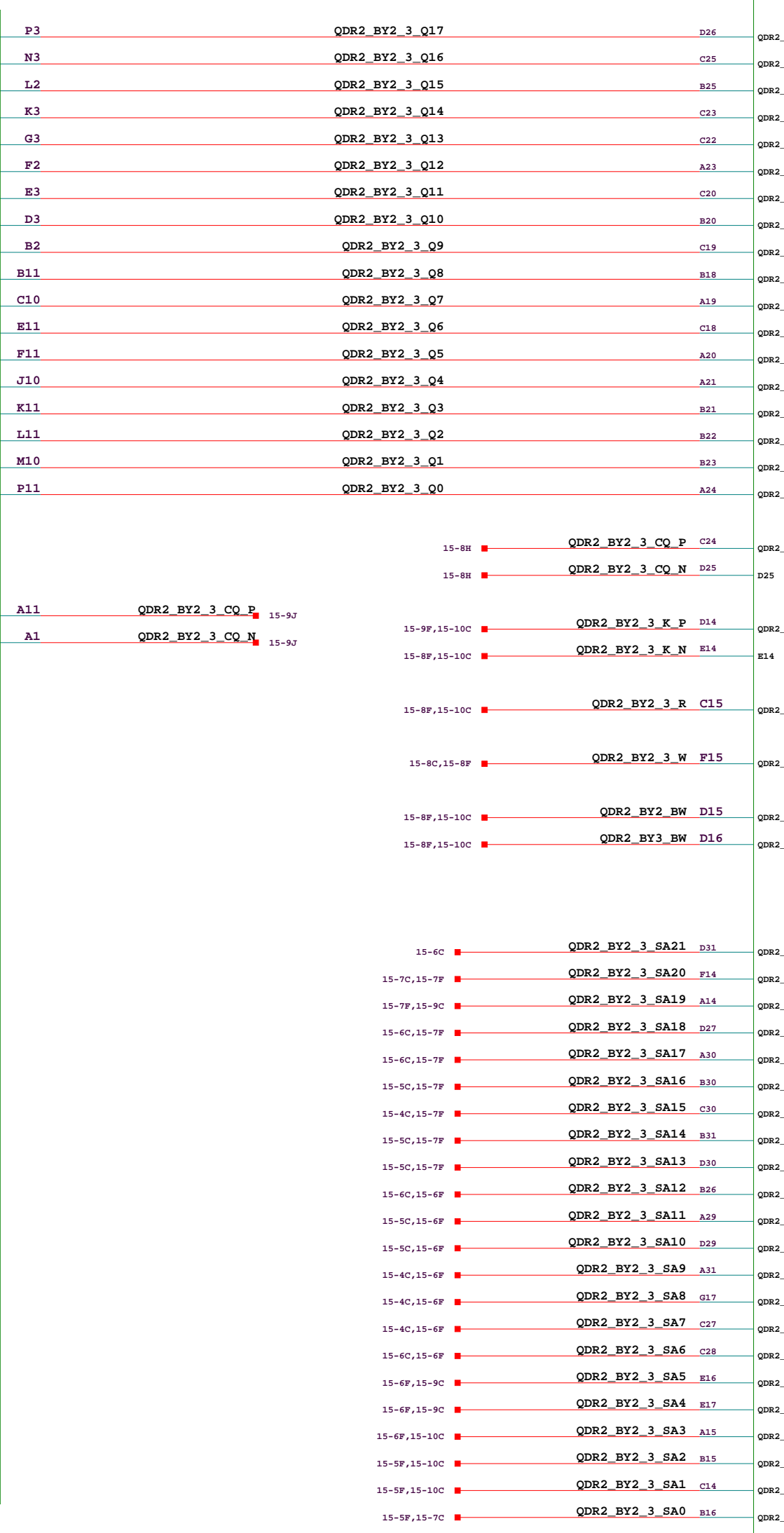
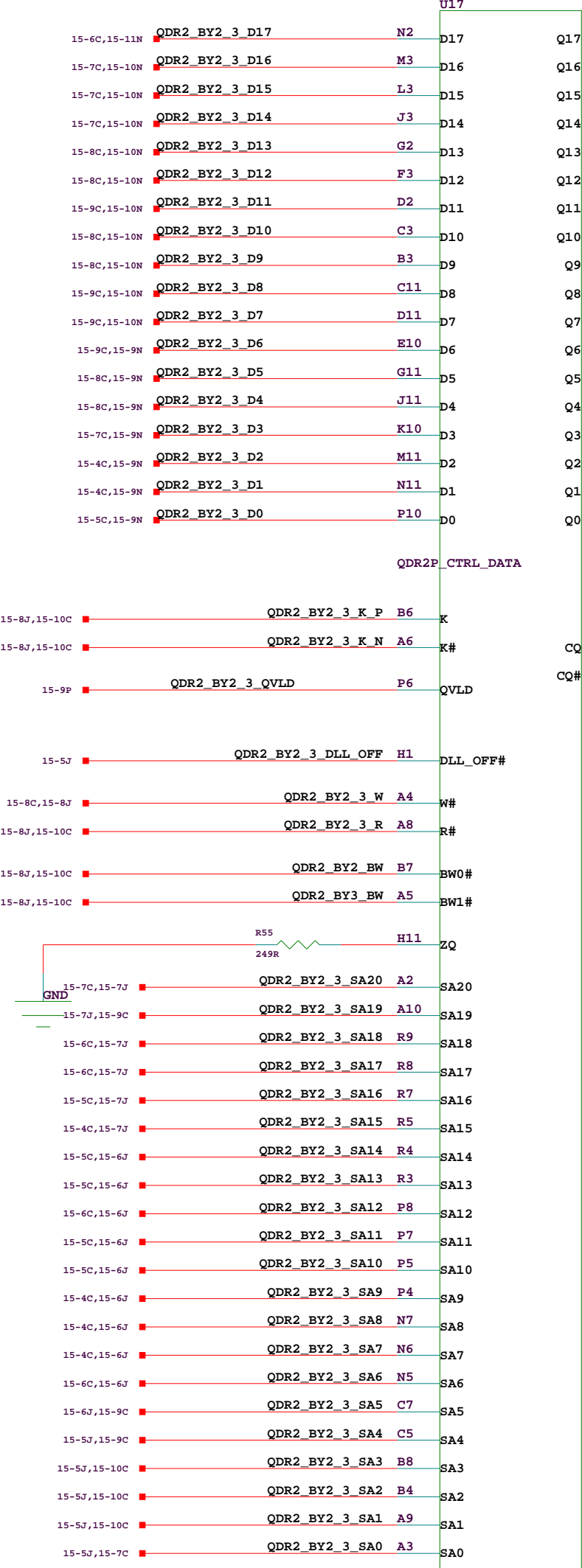
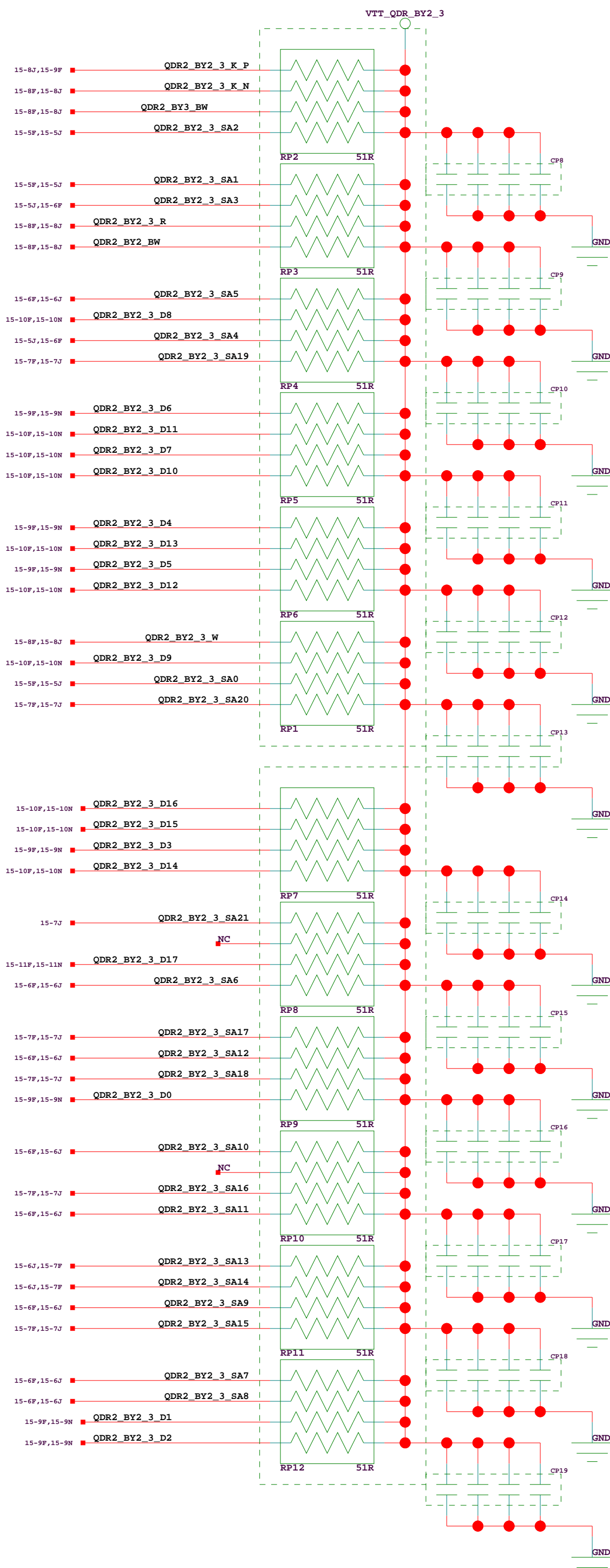
ROACH/iBOB2				ROACH_DIFF_GPIO			
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOONERO BARKAT, CAPE TOWN http://casper.berkeley.edu/				DOC NO:		REVISION	
				NRF-ADM-XXX-SD-0001		A	
				DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW			
DATE:				F KAPP		APPR:	
11-20-2008_10:01				CHECKED:		SHEET	
PATH				E BAUERMEISTER		12 OF 25	



ROACH/iBOE2		ROACH_GPIO_MISC	
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCCORRO MARCAT, CAPE TOWN http://casper.berkeley.edu/		DOC NO: NRF-ADM-XXX-BD-0001	SUBVISION: A
11-20-2008_10:01		DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
PATH	PATH	DESIGNER: F KAPP	APPR: R BAUERMISTROT
		CHECKED:	SHEET



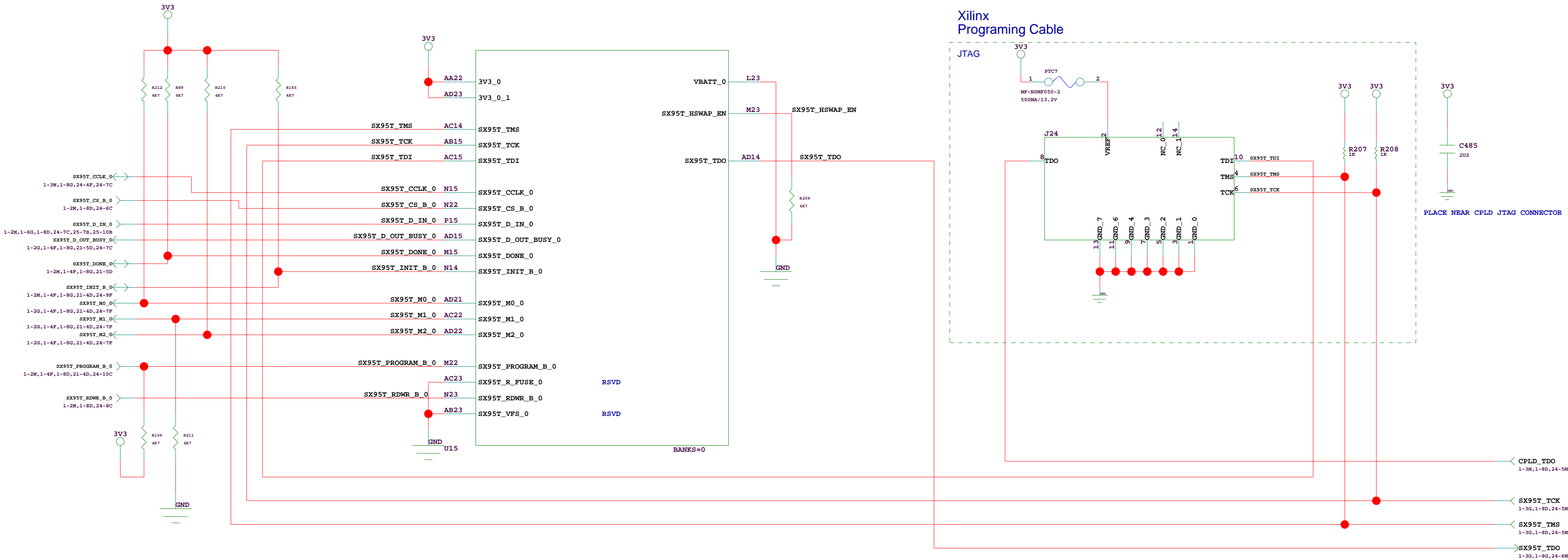
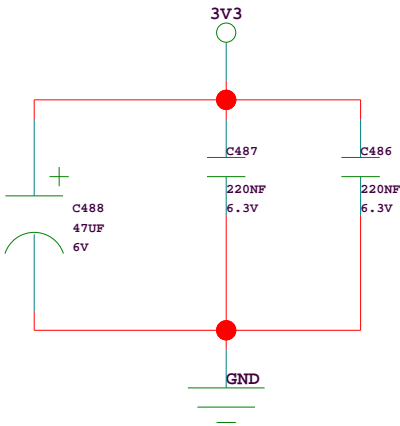
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COLLABORATORS:		DOC NO	REVISION
CASPER GROUP, UC BERKELEY NBAO, SOCORRO meerCAT, CARKO TOWN		NRF-ADM-XXX-SD-0001	A
DESCRIPTION		RECONFIGURABLE OPEN ARCHITECTURE IM	
http://casper.berkeley.edu/		BRAND:	APP:
11-20-2008_10:01		F KAPP	
PATH PATH		CHECKED:	SHEET 14 OF 25
		E BAUERKRITTER	



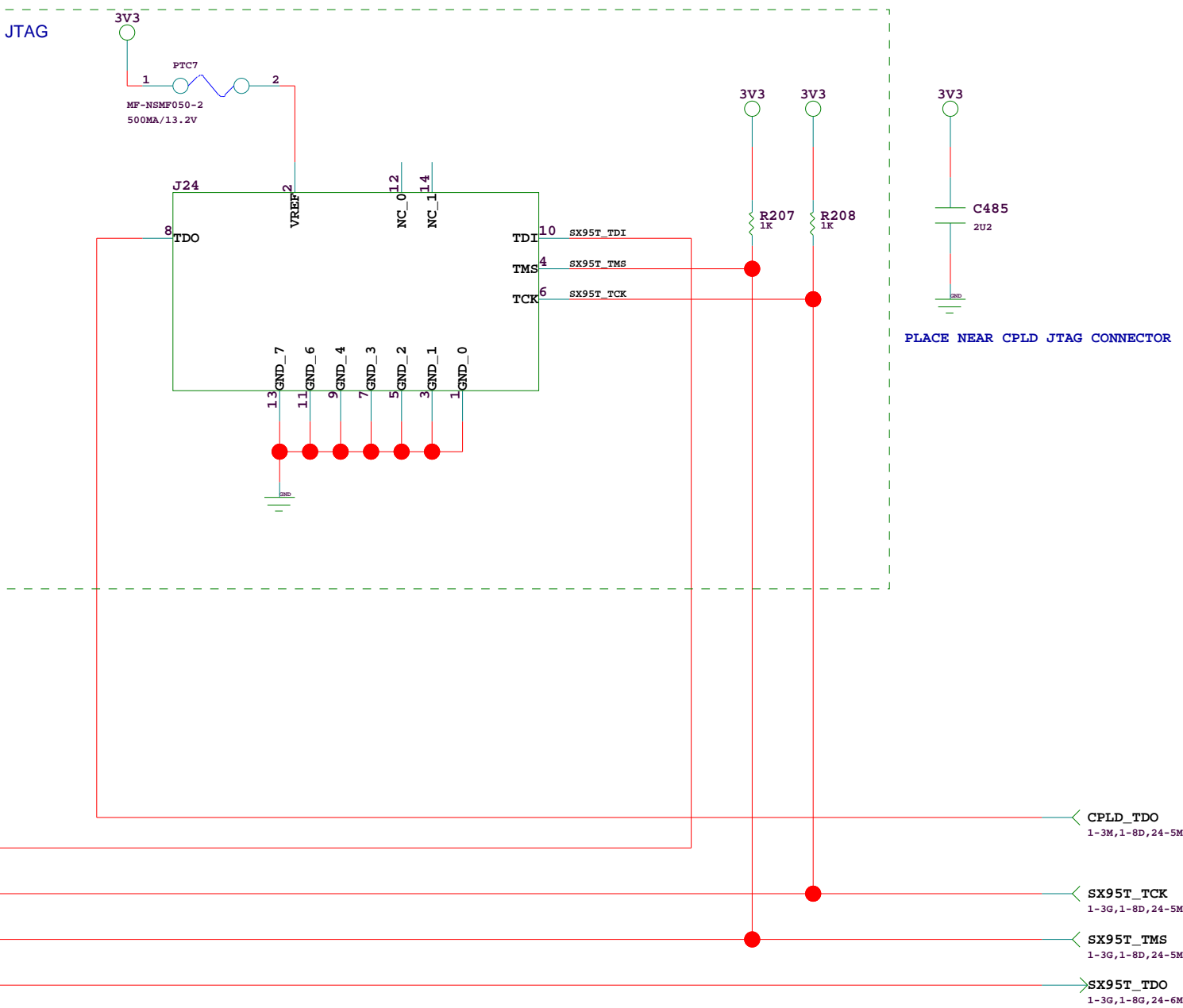
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CASPER GROUP, UC BERKELEY		NRF-ADM-XXX-SD-0001	A
NRAO, SOONERO		DESCRIPTION	
MesaCAT, CAPE TOWN		RECONFIGURABLE OPEN ARCHITECTURE HW	
http://casper.berkeley.edu/		DATE:	APPR:
11-20-2008_10:01		F KAPP	
PATH	PATH	R BAUERMEISTER	SHEET

TBD

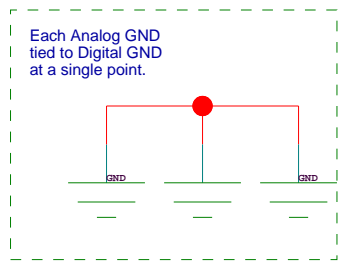
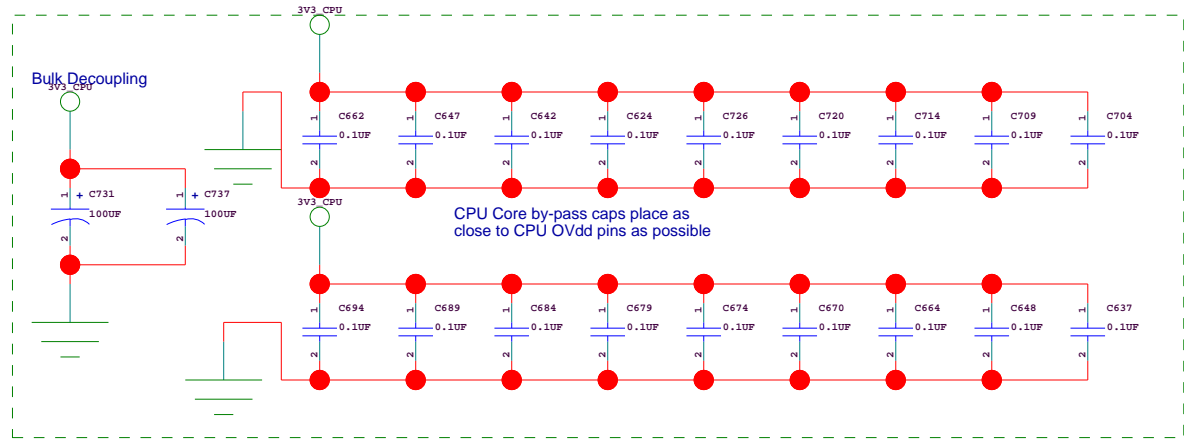
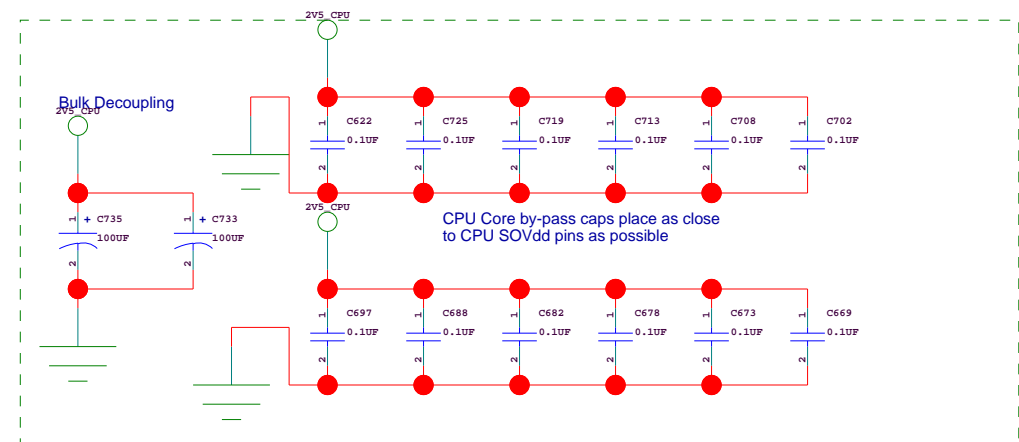
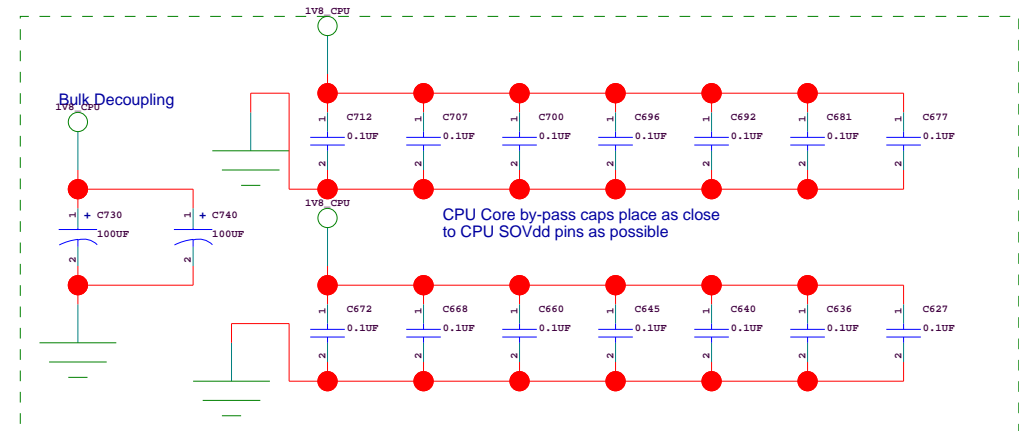
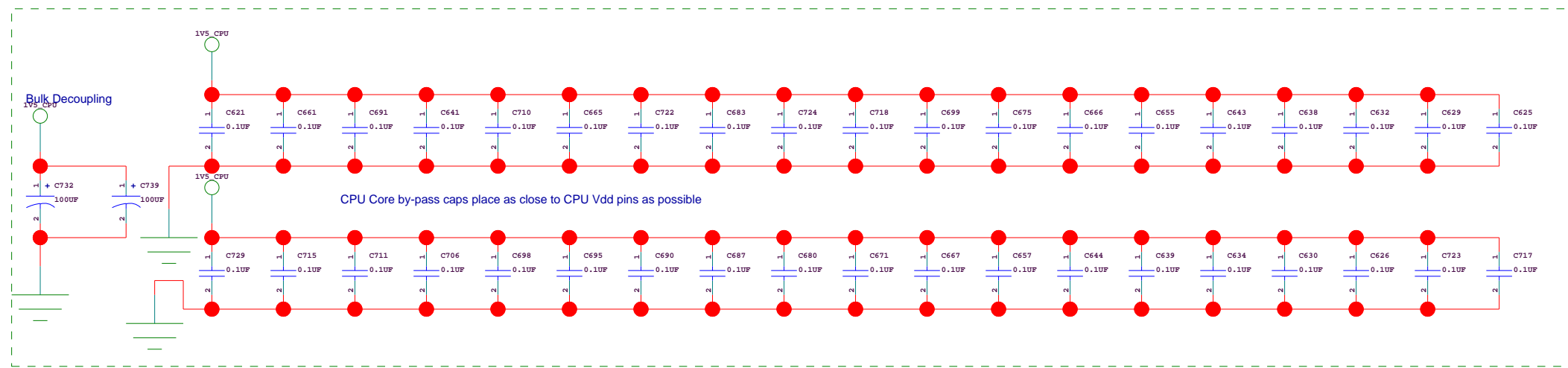
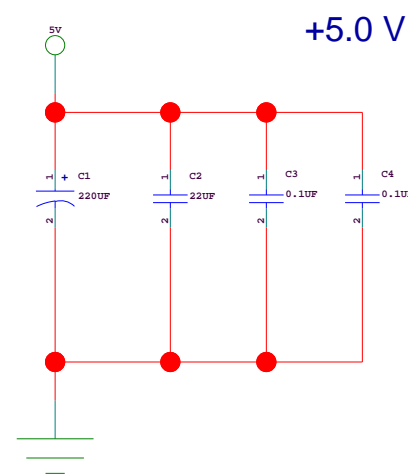
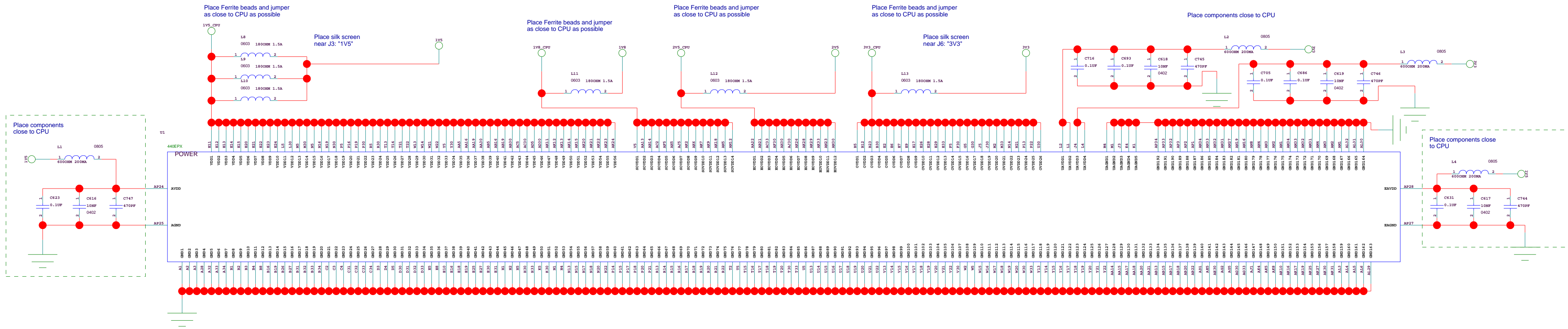
VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input



Xilinx
Programming Cable



ROACH/iBOB2		ROACH_CONFIG	
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO NRF-ADM-XXX-SD-0001		REVISION A
	DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW		
	11-20-2008_10:01	DRAWN: F KAPP	APPR:
PATH	PATH	CHECKED: E BAUERMEISTER	SHEET 16 OF 25



REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOE2

COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOONRO
BAAERAT, CAPE TOWN
<http://casper.berkeley.edu/>

11-20-2008_10:01

PATH PATH

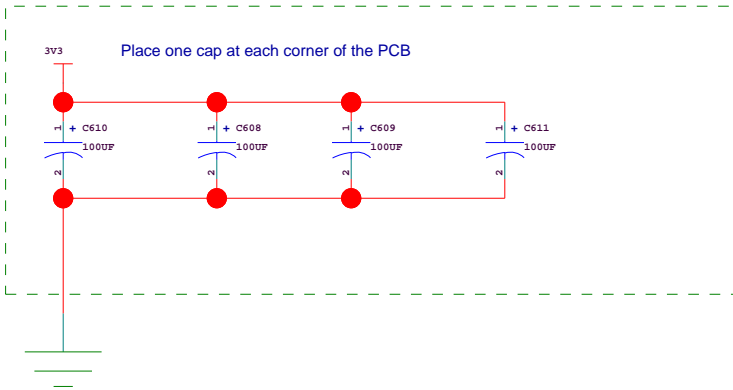
ROACH_PPC_POWER_1

DCC NO: NRP-ADM-XXX-SD-0001
SUBVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

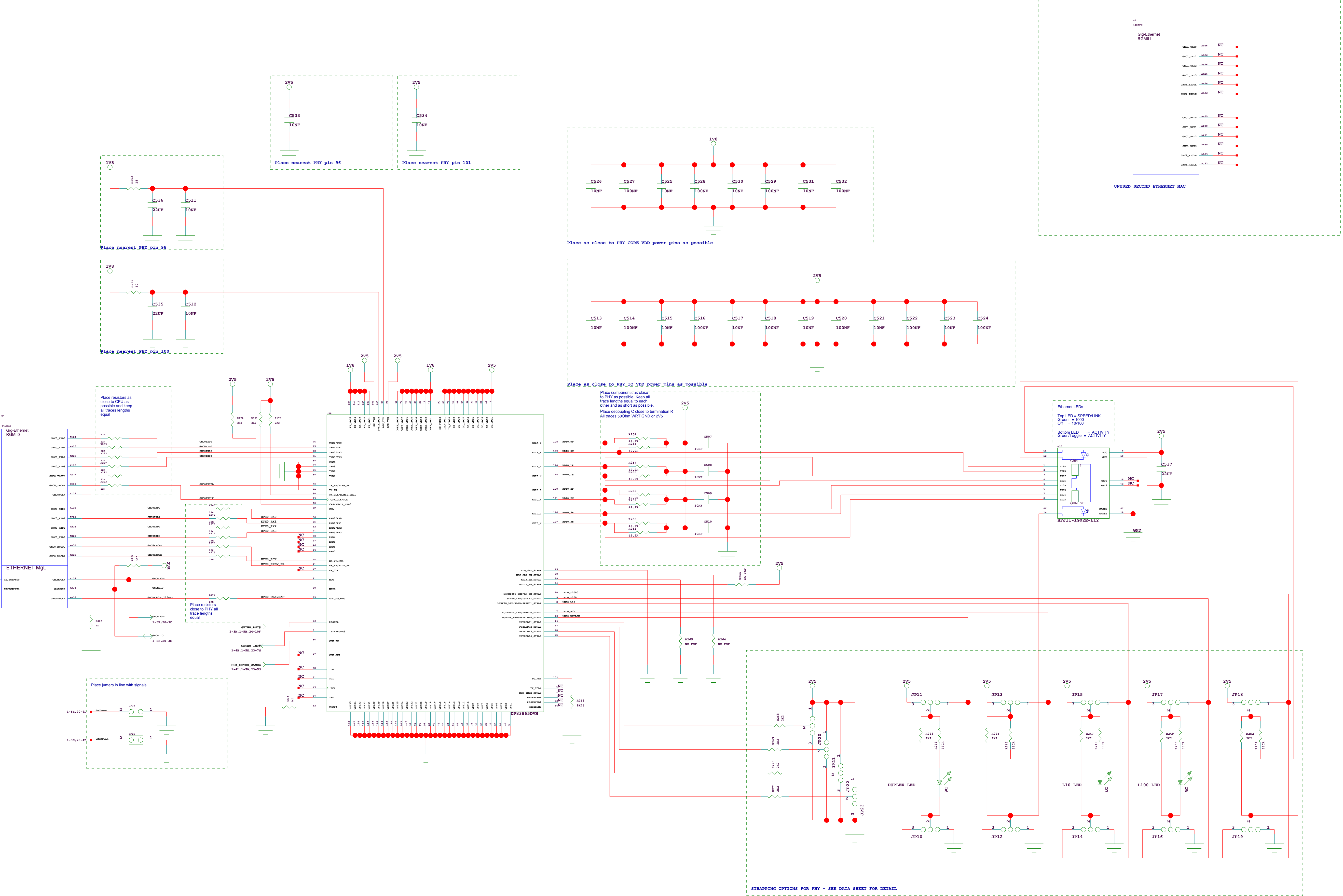
DESIGN: F KAPP
CHECKED: R BAUERMEISTER

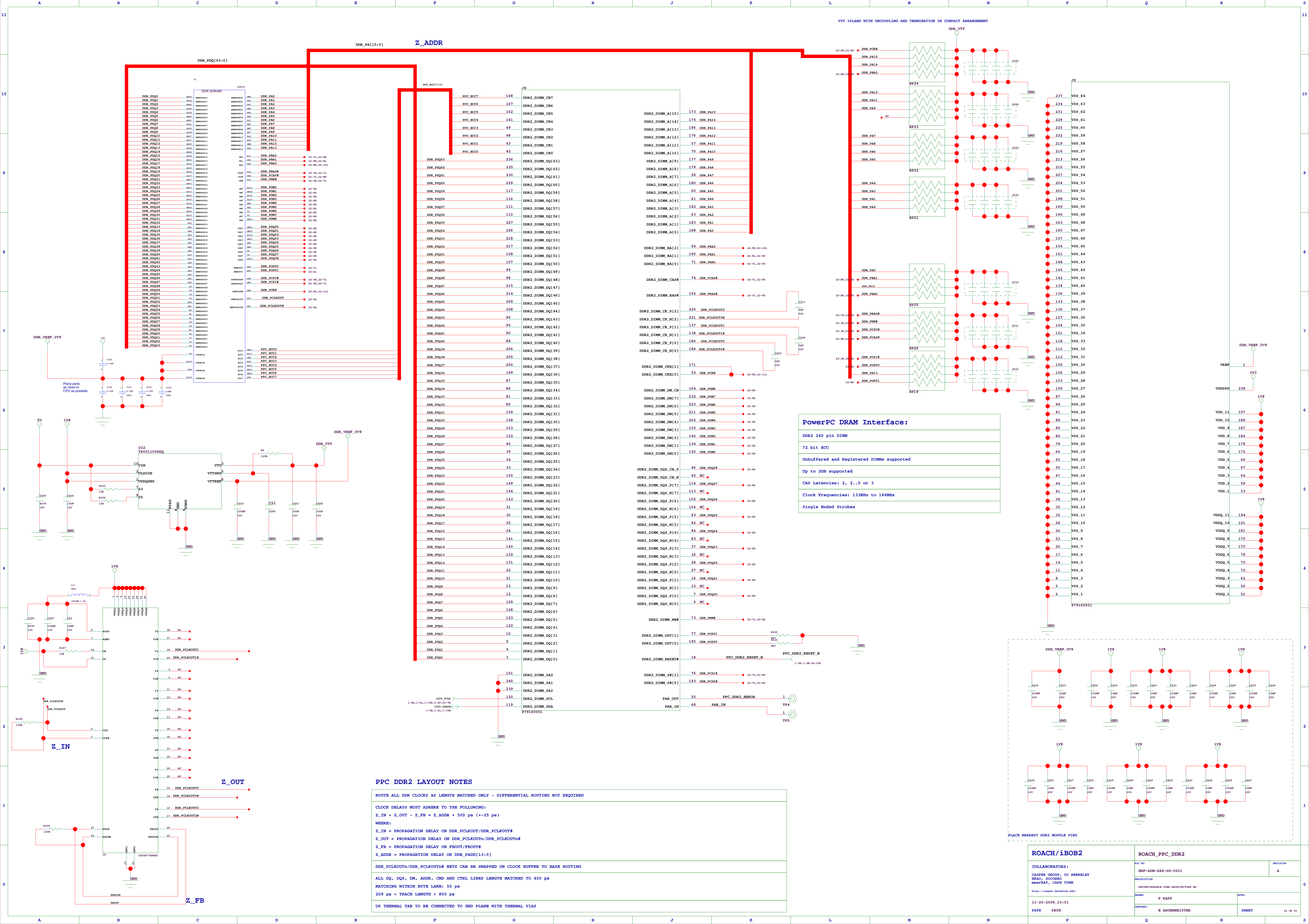
11-20-2008_10:01
SHEET 17 OF 25

A	B	C	D	E	F	G	H	J	K	L	M																						
7											7																						
6	<div>REMOVED 3V3 GENERATION</div> <div></div>										6																						
5											5																						
4	<div>REMOVED +12V GENERATION</div> <div>REMOVED -12V GENERATION</div>										4																						
3											3																						
2											2																						
1	<div>REMOVED +1V GENERATION</div> <div>REMOVED +2V5 GENERATION</div>										1																						
0	<table><tr><td colspan="2">ROACH/iBOB2</td><td colspan="2">ROACH_PPC_POWER_2</td></tr><tr><td rowspan="3">COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/</td><td colspan="2">DOC NO NRF-ADM-XXX-SD-0001</td><td>REVISION A</td></tr><tr><td colspan="3">DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW</td></tr><tr><td colspan="2">DRAWN: F KAPP</td><td>APPR:</td></tr><tr><td>11-20-2008_10:01</td><td colspan="2">CHECKED: E BAUERMEISTER</td><td>SHEET 18 OF 25</td></tr><tr><td>PATH</td><td>PATH</td><td colspan="2"></td></tr></table>										ROACH/iBOB2		ROACH_PPC_POWER_2		COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO NRF-ADM-XXX-SD-0001		REVISION A	DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW			DRAWN: F KAPP		APPR:	11-20-2008_10:01	CHECKED: E BAUERMEISTER		SHEET 18 OF 25	PATH	PATH			0
ROACH/iBOB2		ROACH_PPC_POWER_2																															
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO NRF-ADM-XXX-SD-0001		REVISION A																														
	DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW																																
	DRAWN: F KAPP		APPR:																														
11-20-2008_10:01	CHECKED: E BAUERMEISTER		SHEET 18 OF 25																														
PATH	PATH																																
A	B	C	D	E	F	G	H	J	K	L	M																						

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.
The Tx and the Rx side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.
Minimize the number of vias on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30





Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11_0592MHz = as short as possible
CLK_SYS_33MHz = as short as possible
CLK_CPLD_33MHz = CLK_SYS_33MHz

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PC13_6633MHz = as short as possible
CLK_PC12_6633MHz = CLK_PC13_6633MHz
CLK_PC11_6633MHz = CLK_PC12_6633MHz + 2.5°
CLK_GETH0_25MHz = as short as possible
CLK_GETH1_25MHz = CLK_GETH0_25MHz
CLK_CPLD_50MHz = as short as possible
CLK_USB2_0_48MHz = as short as possible
CLK_USB2_0_12MHz = as short as possible

TRACE & JTAG CONNECTORS

Critical placement and routing
of the Trace connector and nets.
Up to CPU frequency!

TRACE PORT

ROACH/iBOE2

ROACH_PPC_TST_CLK_IO

COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCCORO
MesaCAT, CAPE TOWN
<http://casper.berkeley.edu/>

DOC NO
NRF-ADM-XXX-BD-0001

REVISION
A

11-20-2008_10:01

DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DESIGN:
F KAPP

PPPS:

PATH

CHECKED:
R BAUERMEISTER

SHEET

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