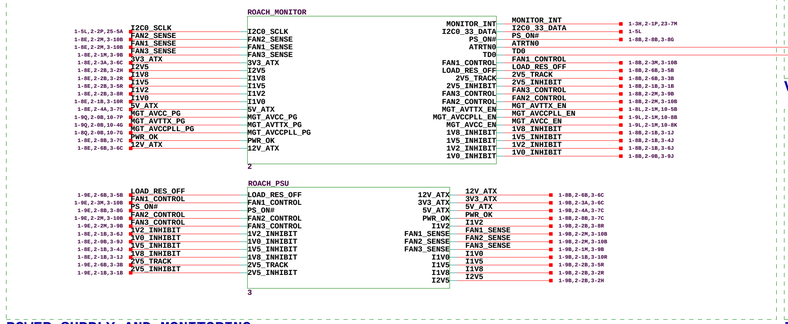
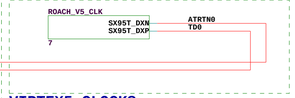
VIRTEX5

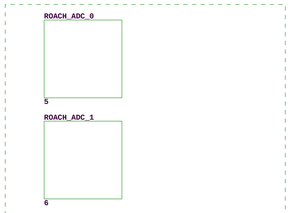
POWER SUPPLY AND MONITORING



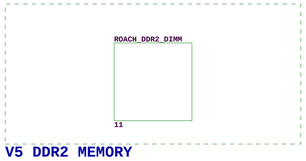
VIRTEX5 CLOCKS



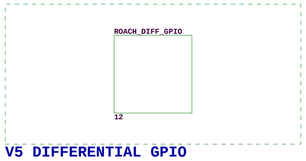
ZDOK/ADC INTERFACE



V5 DDR2 MEMORY

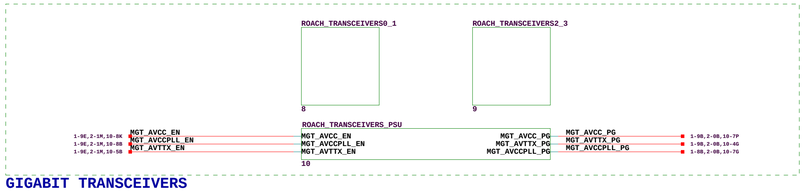


V5 DIFFERENTIAL GPIO

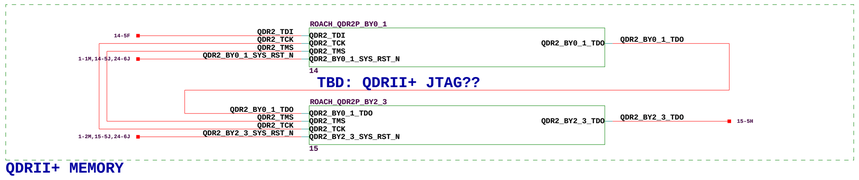


V5 SE GPIO & MISCELLANEOUS

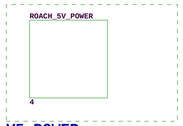
GIGABIT TRANSCEIVERS



QDRII+ MEMORY

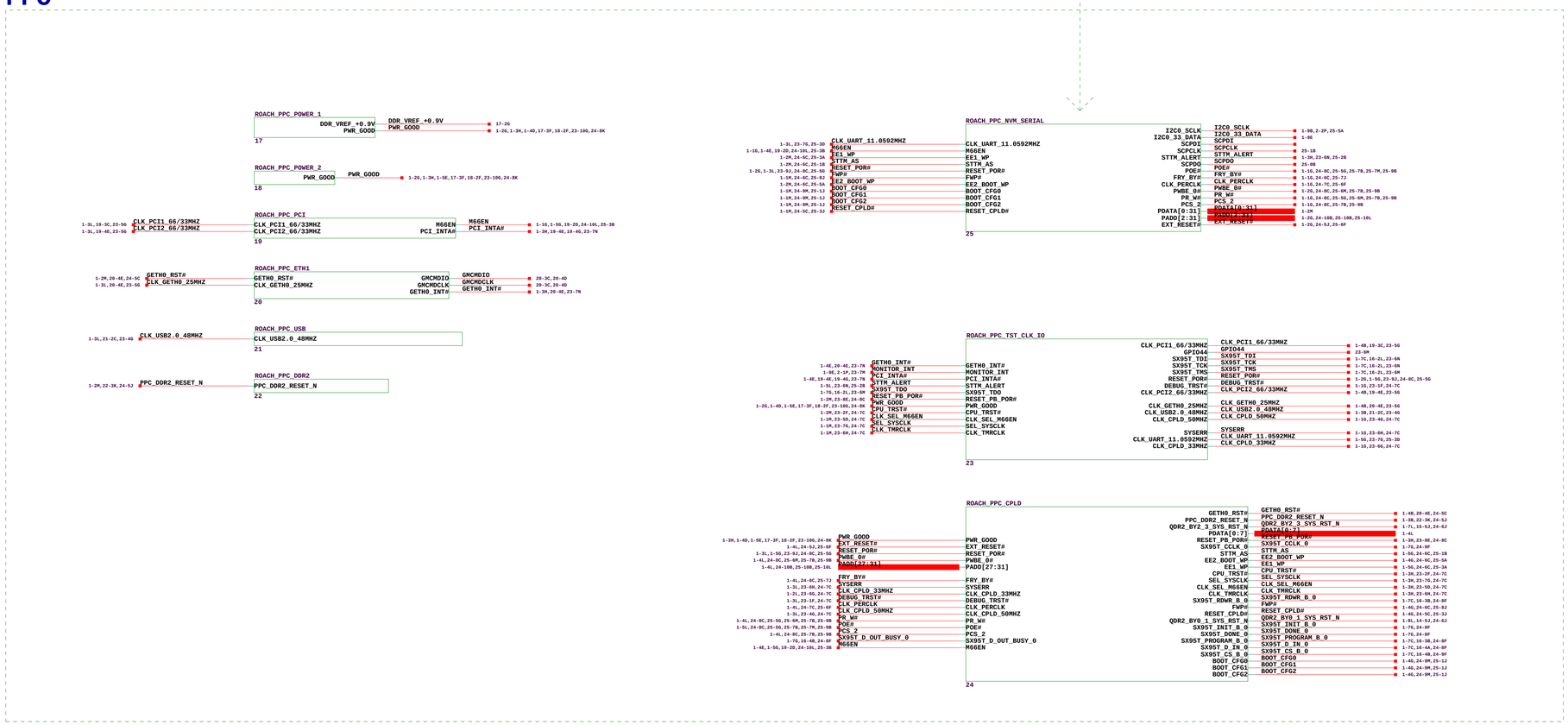


V5 POWER

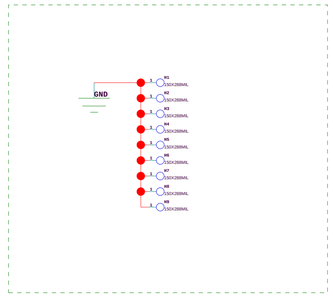


VIRTEX5 CONFIGURATION

PPC



MECHANICAL



CONTRIBUTORS

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MIKE REVNELL
HAYDEN SO
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ROACH/iBOB2	**ROACH_TOP**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-8-2007_14:44	DRAWN: F KAPP · APPR:
PATH PATH	CHECKED: E BAUERMEISTER · SHEET 1 OF 25

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

TIE TO GROUND IF PLL'S ARE NOT USED

PLACE AT ACTEL 3V3 POWER PINS

PLACE AT ACTEL 1V5 POWER PINS

roach_AFS600_powerpins

roach_AFS600_configpins

roach_AFS600_pcb

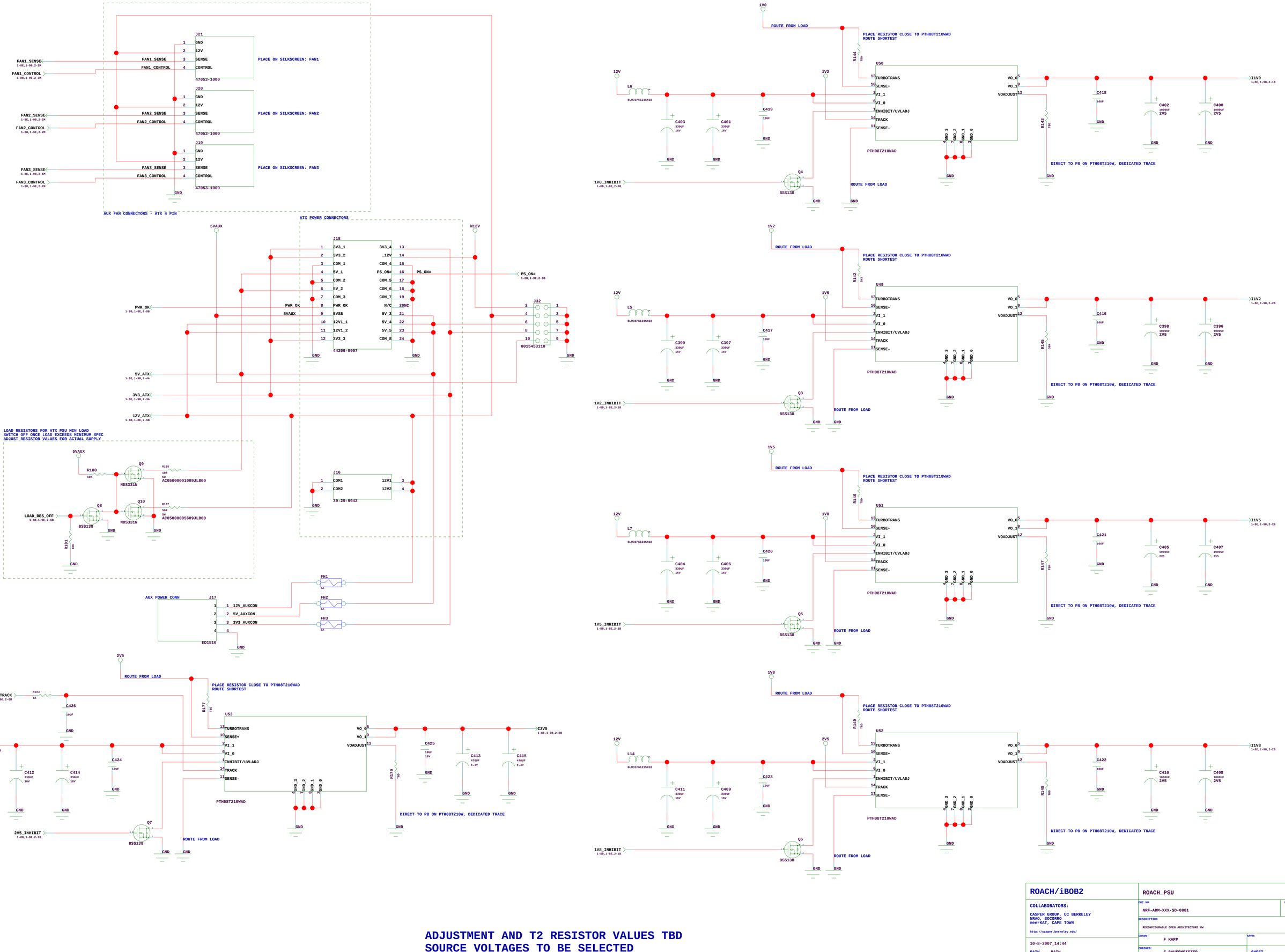
PUSH BUTTON POWER SWITCH

XPORT - PLACE IN REAR I/O REGION

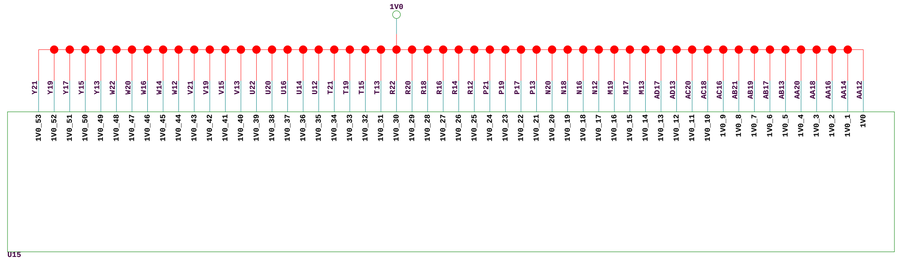
TEMPERATURE DIODE HEADER

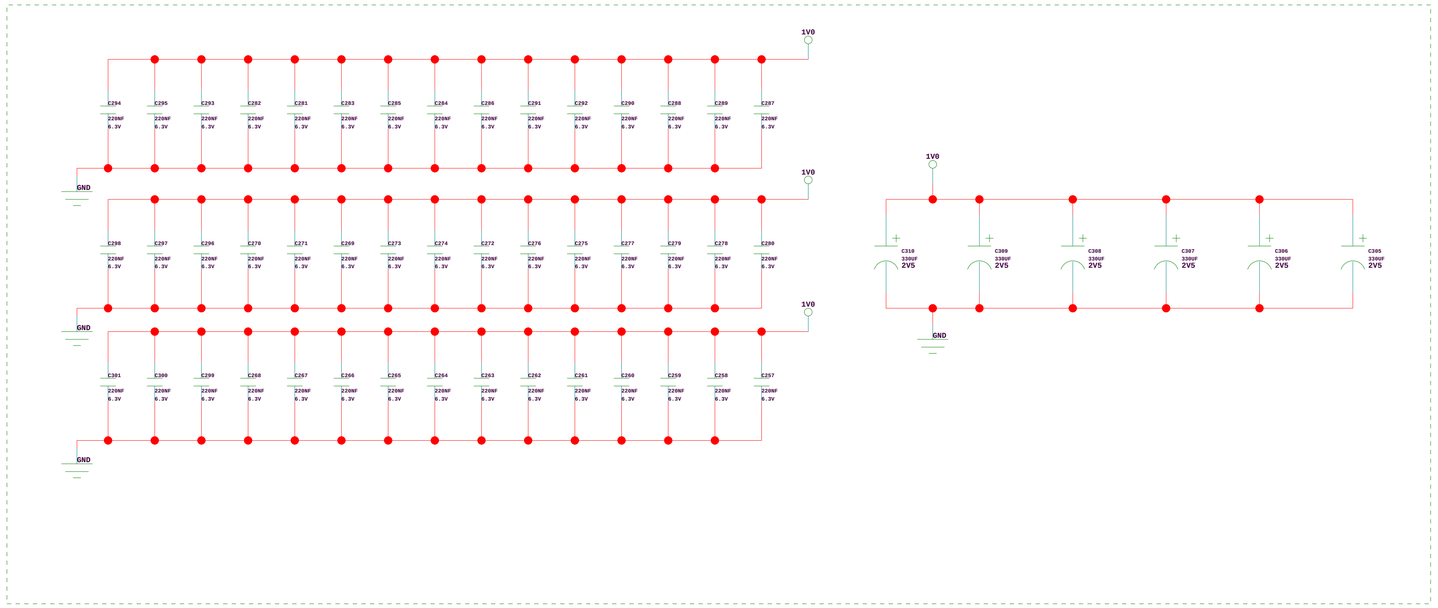
ACTEL JTAG CONNECTOR

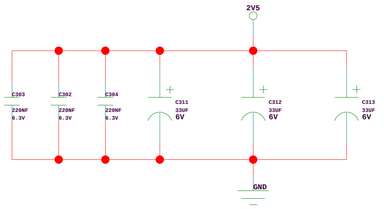
ROACH/iBOB2	ROACH_MONITOR
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-8-2007_14:44	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 2 OF 25

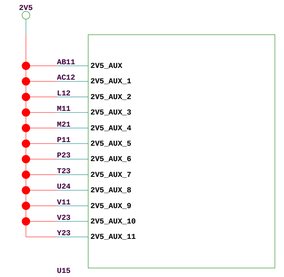


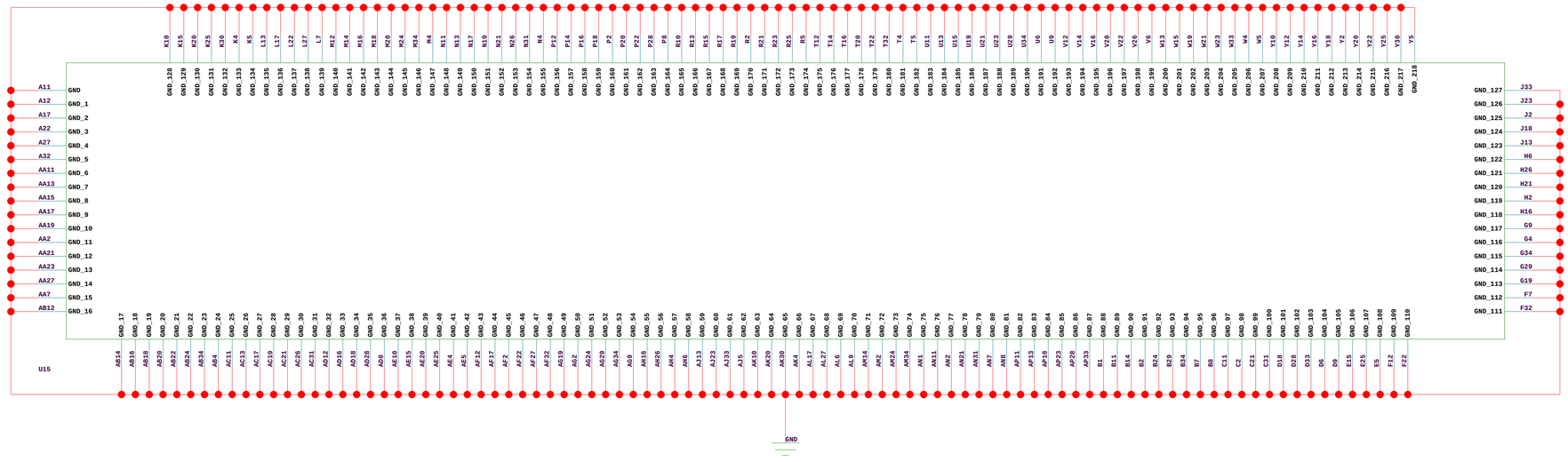
ROACH/iBOB2	ROACH_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE RW
10-8-2007_14:44 PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET: 3 OF 25











ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
10-8-2007_14:44 PATH PATH	

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

10-8-2007_14:44

PATH PATH

ROACH_ADC_0

DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 5 OF 25

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

10-8-2007_14:44

PATH PATH

ROACH_ADC_1

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

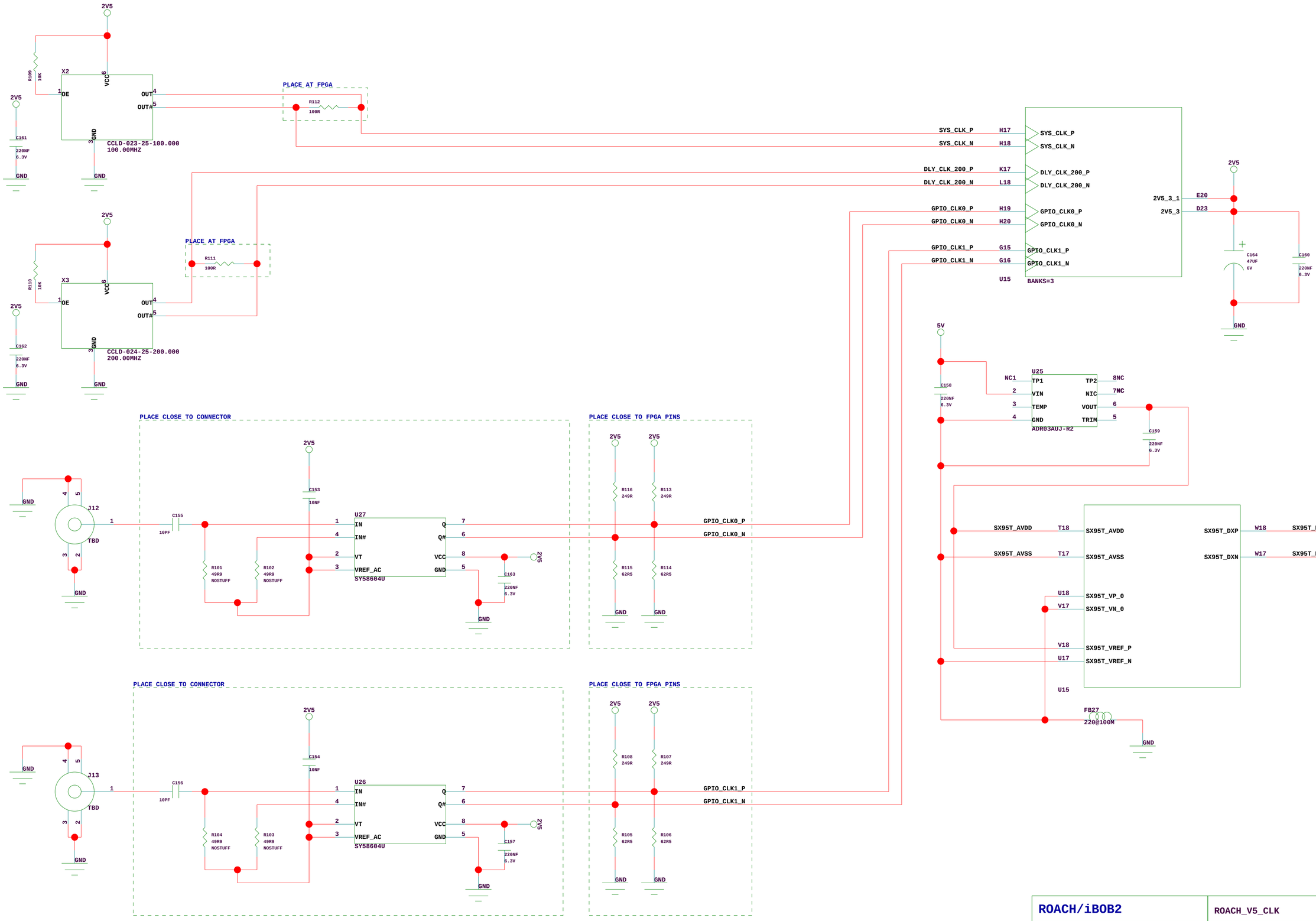
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

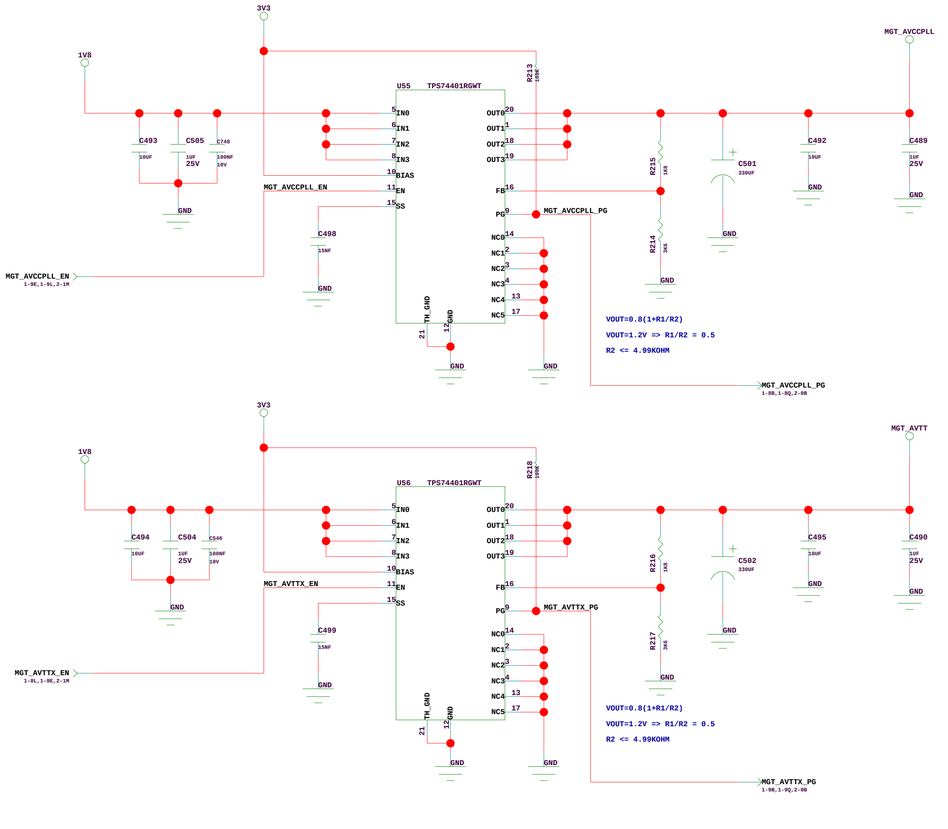
SHEET 6 OF 25

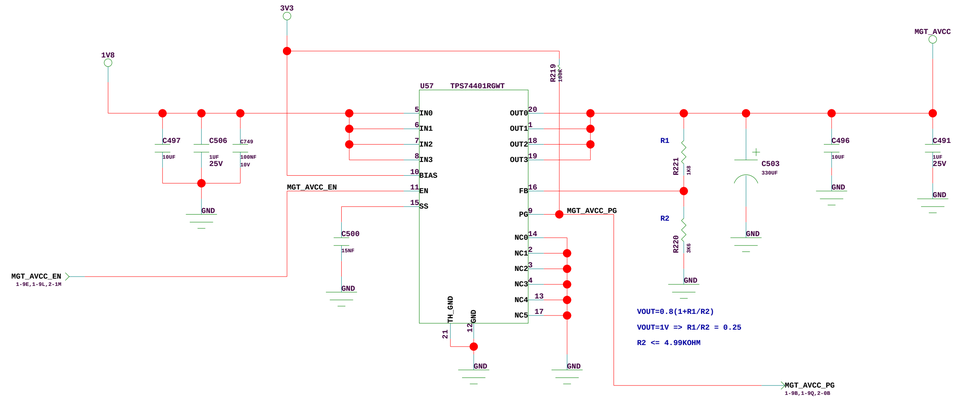


ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
10-8-2007_14:44 PATH PATH	

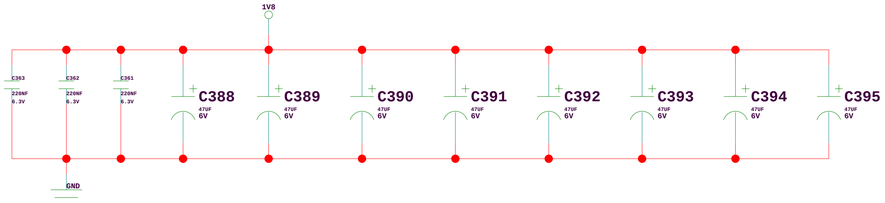
ROACH/iBOB2	**ROACH_TRANSCEIVERS0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP CHECKED: E BAUERMEISTER APPR:
10-8-2007_14:44	SHEET 8 OF 25
PATH PATH	

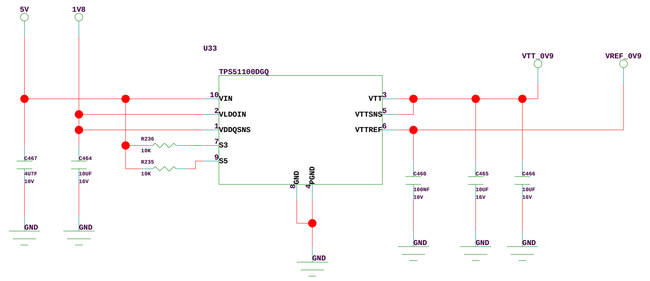
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB28 220@100M
FB29 220@100M
FB30 220@100M
FB31 220@100M
C172 C171 C170 C169 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
2V5
FB52 220@100M
C248 220NF 6.3V
R131 10K
X4
OE
VCC
OUT
OUT
CCLD-023-25-156.250 156.25MHZ
JP9
MGT_REFCLK_Q2_P
MGT_REFCLK_Q2_N
C181 C182 C183 C184 C186 C185 10NF 25V
MGTAVCC_120 D5 MGTAVCC_120
MGTAVCC_120_1 F4 MGTAVCC_120_1
MGTAVCCPLL_120 D3 MGTAVCCPLL_120
MGTAVTTRX_120 C3 MGTAVTTRX_120
MGT_120_REF_CLK_P E4 MGT_120_REF_CLK_P
MGT_120_REF_CLK_N D4 MGT_120_REF_CLK_N
MGTRX0_120_P A3 MGTRX0_120_P
MGTRX0_120_N A2 MGTRX0_120_N
MGTRX1_120_P D1 MGTRX1_120_P
MGTRX1_120_N C1 MGTRX1_120_N
U15
MGTAVTTTX_120_1 E3 MGTAVTTTX_120_1
MGTAVTTTX_120 C4 MGTAVTTTX_120
MGTTX0_120_P B4 MGTTX0_120_P
MGTTX0_120_N B3 MGTTX0_120_N
MGTTX1_120_P E2 MGTTX1_120_P
MGTTX1_120_N D2 MGTTX1_120_N
FB32 220@100M
FB33 220@100M
C174 C173 220NF 6.3V
P3
S39 DL0P
S40 DL0N
S41 DL1P
S42 DL1N
S43 DL2P
S44 DL2N
S45 DL3P
S46 DL3N
S54 SL0P
S53 SL0N
S52 SL1P
S51 SL1N
S50 SL2P
S49 SL2N
S48 SL3P
S47 SL3N
SIG_GND1 G20
SIG_GND2 G21
SIG_GND3 G22
SIG_GND4 G23
SIG_GND5 G24
SIG_GND6 G25
SIG_GND7 G26
SIG_GND8 G27
SIG_GND9 G28
SIG_GND10 G19
FCN-268F036-G/3DB
JP7
ODIS
FAULT
R123 10K
C240 10NF
C242 10NF
3V3
R132 150R
OPTICAL MODULE FAULT - RED LED
R121 5K1
R120 3K9
R119 6K8
R118 3K9
C241 10NF
U34 MAX9032AKA
U30 MAX9032AKA
U36 AND2 SN74AHC1G08DCKR
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB38 220@100M
FB39 220@100M
FB36 220@100M
FB37 220@100M
C180 C179 C178 C177 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_122 AJ4 MGTAVCC_122
MGTAVCC_122_1 AK5 MGTAVCC_122_1
MGTAVCCPLL_122 AM4 MGTAVCCPLL_122
MGTAVTTRX_122 AL3 MGTAVTTRX_122
MGT_122_REF_CLK_P NC AL5 MGT_122_REF_CLK_P
MGT_122_REF_CLK_N NC AL4 MGT_122_REF_CLK_N
MGTRX0_122_P AL1 MGTRX0_122_P
MGTRX0_122_N AM1 MGTRX0_122_N
MGTRX1_122_P AP3 MGTRX1_122_P
MGTRX1_122_N AP2 MGTRX1_122_N
U15
C251 C252 C250 C249 10NF 25V
MGTAVTTTX_122_1 AM3 MGTAVTTTX_122_1
MGTAVTTTX_122 AK3 MGTAVTTTX_122
MGTTX0_122_P AK2 MGTTX0_122_P
MGTTX0_122_N AL2 MGTTX0_122_N
MGTTX1_122_P AN4 MGTTX1_122_P
MGTTX1_122_N AN3 MGTTX1_122_N
FB35 220@100M
FB34 220@100M
C175 C176 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
U28 TPS2031D
R130 10K
C246 10NF
C247 100NF
C168 4.7UF 16V
C166 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB49 220@100M
FB48 220@100M
FB51 220@100M
FB50 220@100M
C224 C225 C191 C226 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_126 AL8 MGTAVCC_126
MGTAVCC_126_1 AM8 MGTAVCC_126_1
MGTAVCCPLL_126 AM9 MGTAVCCPLL_126
MGTAVTTRX_126 AM6 MGTAVTTRX_126
MGT_126_REF_CLK_P NC AL7 MGT_126_REF_CLK_P
MGT_126_REF_CLK_N NC AM7 MGT_126_REF_CLK_N
MGTRX0_126_P AP6 MGTRX0_126_P
MGTRX0_126_N AP7 MGTRX0_126_N
MGTRX1_126_P AP9 MGTRX1_126_P
MGTRX1_126_N AP8 MGTRX1_126_N
U15
C255 C256 C254 C253 10NF 25V
MGTAVTTTX_126_1 AM5 MGTAVTTTX_126_1
MGTAVTTTX_126 AM10 MGTAVTTTX_126
MGTTX0_126_P AN5 MGTTX0_126_P
MGTTX0_126_N AN6 MGTTX0_126_N
MGTTX1_126_P AN10 MGTTX1_126_P
MGTTX1_126_N AN9 MGTTX1_126_N
FB46 220@100M
FB47 220@100M
C223 C222 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB44 220@100M
FB45 220@100M
FB42 220@100M
FB43 220@100M
C221 C220 C215 C212 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_124 C7 MGTAVCC_124
MGTAVCC_124_1 D7 MGTAVCC_124_1
MGTAVCCPLL_124 C6 MGTAVCCPLL_124
MGTAVTTRX_124 C9 MGTAVTTRX_124
MGT_124_REF_CLK_P NC D8 MGT_124_REF_CLK_P
MGT_124_REF_CLK_N NC C8 MGT_124_REF_CLK_N
MGTRX0_124_P A9 MGTRX0_124_P
MGTRX0_124_N A8 MGTRX0_124_N
MGTRX1_124_P A6 MGTRX1_124_P
MGTRX1_124_N A7 MGTRX1_124_N
U15
C187 C188 C189 C190 10NF 25V
MGTAVTTTX_124_1 C5 MGTAVTTTX_124_1
MGTAVTTTX_124 C10 MGTAVTTTX_124
MGTTX0_124_P B10 MGTTX0_124_P
MGTTX0_124_N B9 MGTTX0_124_N
MGTTX1_124_P B5 MGTTX1_124_P
MGTTX1_124_N B6 MGTTX1_124_N
FB41 220@100M
FB40 220@100M
C213 C214 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
P3
S57 DL0P
S58 DL0N
S59 DL1P
S60 DL1N
S61 DL2P
S62 DL2N
S63 DL3P
S64 DL3N
S72 SL0P
S71 SL0N
S70 SL1P
S69 SL1N
S68 SL2P
S67 SL2N
S66 SL3P
S65 SL3N
SIG_GND1 G29
SIG_GND2 G30
SIG_GND3 G31
SIG_GND4 G32
SIG_GND5 G33
SIG_GND6 G34
SIG_GND7 G35
SIG_GND8 G36
SIG_GND9 G37
SIG_GND10 G19
FCN-268F036-G/3DB
JP8
ODIS
FAULT
R124 10K
C245 10NF
C243 10NF
R126 5K1
R127 3K9
R128 6K8
R129 3K9
C244 10NF
U37 AND2 SN74AHC1G08DCKR
U29 TPS2031D
R117 10K
C239 10NF
C227 100NF
C167 4.7UF 16V
C165 22UF
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
10-8-2007_14:44
PATH PATH
ROACH_TRANSCEIVERS2_3
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 9 OF 25

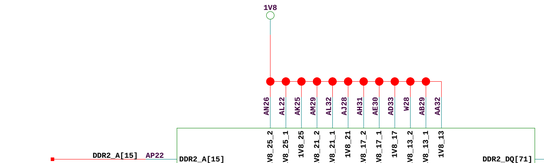


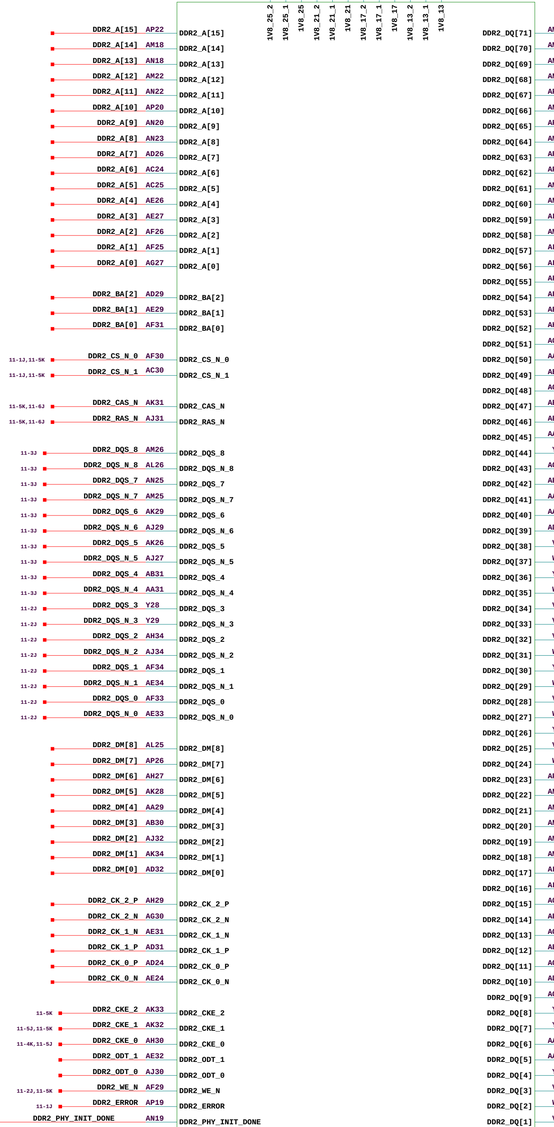


ROACH/iBOB2	**ROACH_TRANSCEIVERS_PSU**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-8-2007_14:44 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 10 OF 25

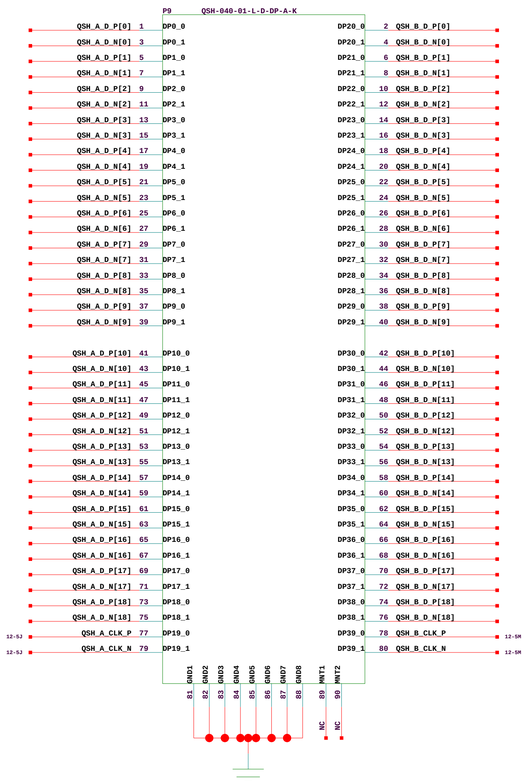


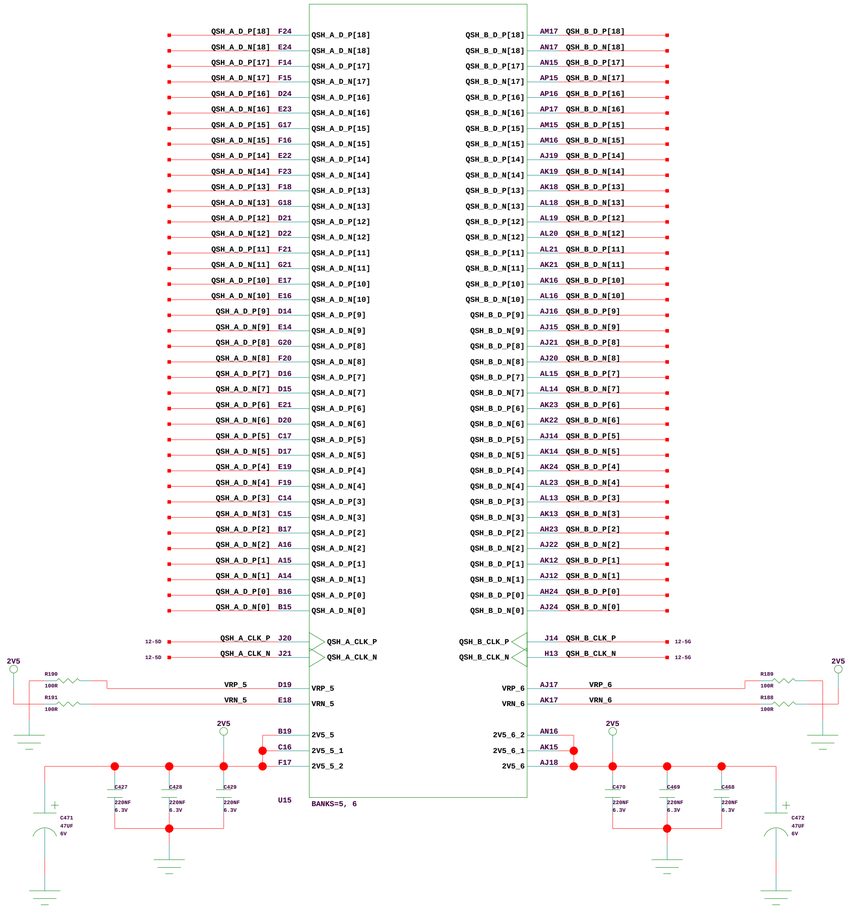






ROACH/iBOB2	**ROACH_DDR2_DIMM**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-8-2007_14:44 PATH PATH	DRAWN: F KAPP APPR:
	CHECKED: E BAUERMEISTER SHEET 11 OF 25





ROACH/iBOB2	**ROACH_DIFF_GPIO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-8-2007_14:44 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 12 OF 25

GPIOLVC33[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

GPIOLVC18[20] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

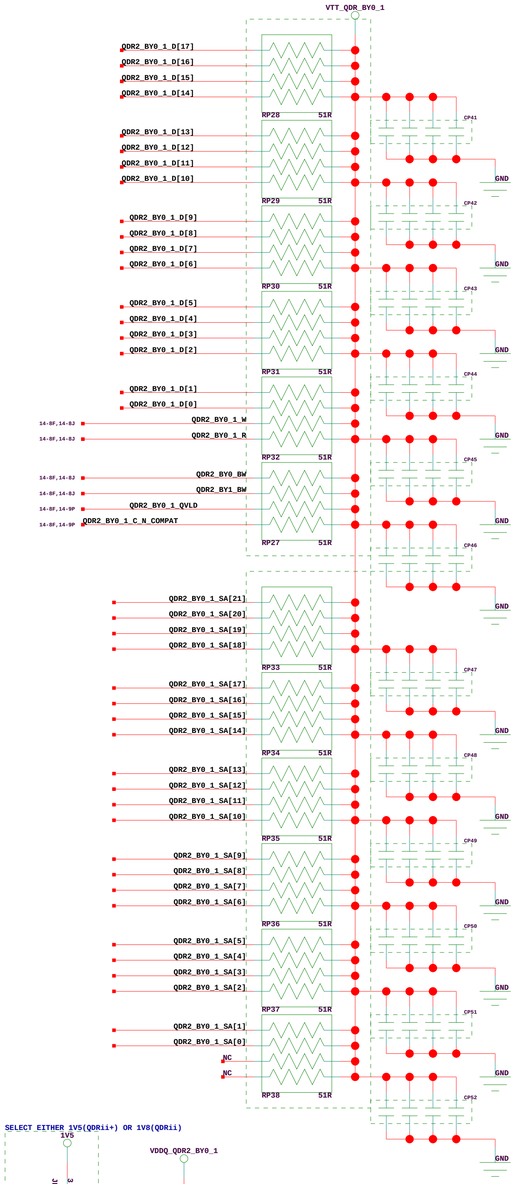
IO VOLTAGE LEVEL SELECT
1-2: 3.3V
2-3: 2.5V

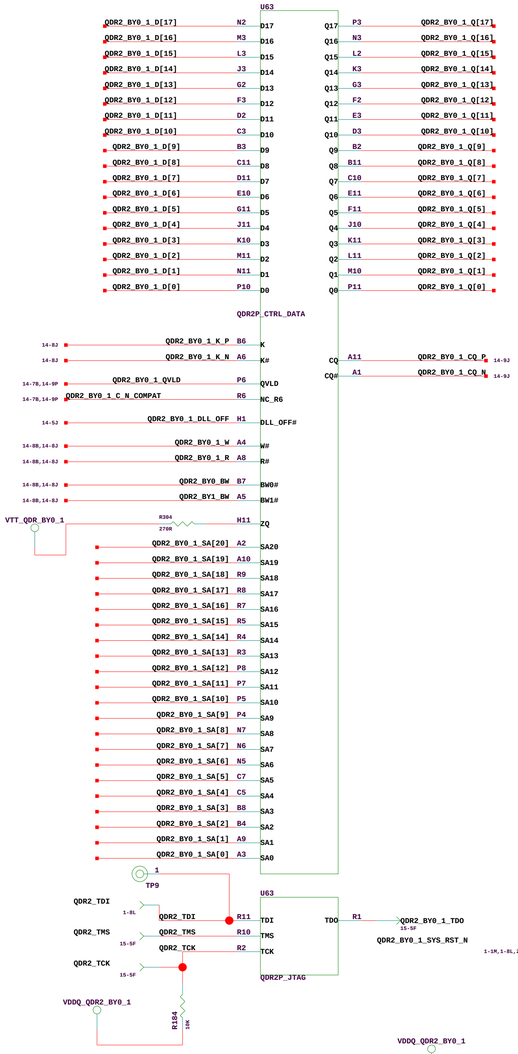
HLE-105-02-G-DV

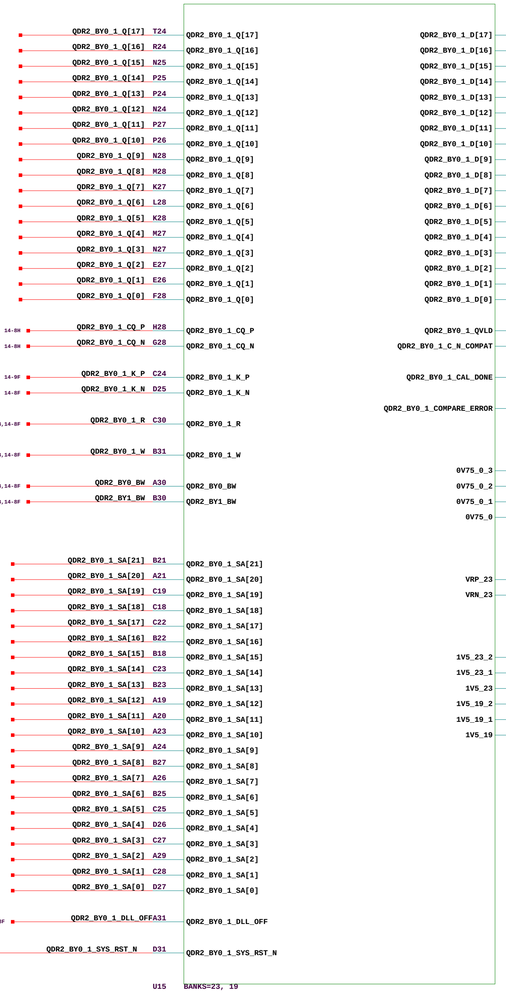
74AVCH4T245DGVRE4

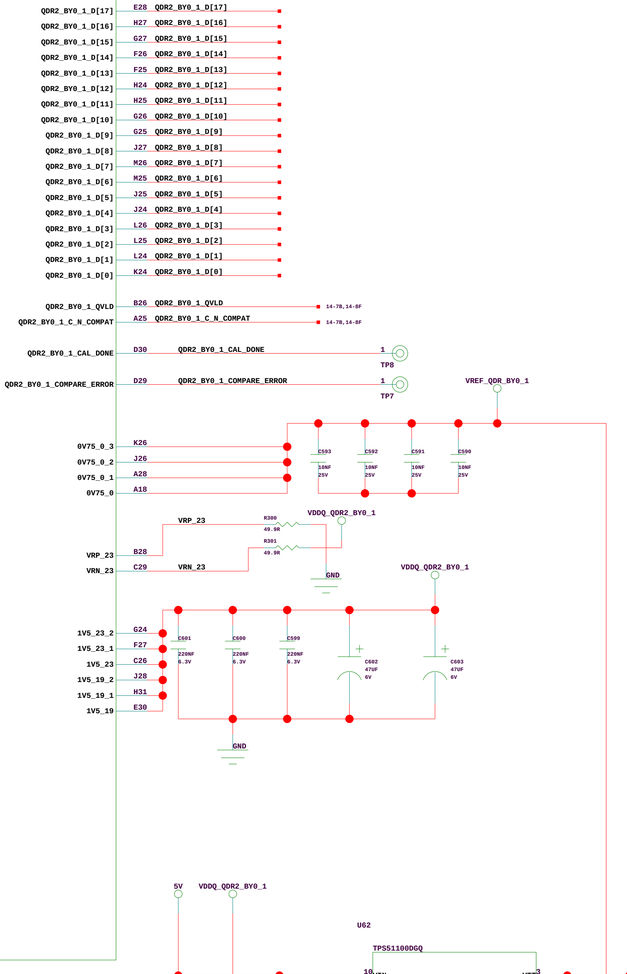
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
10-8-2007_14:44
PATH PATH

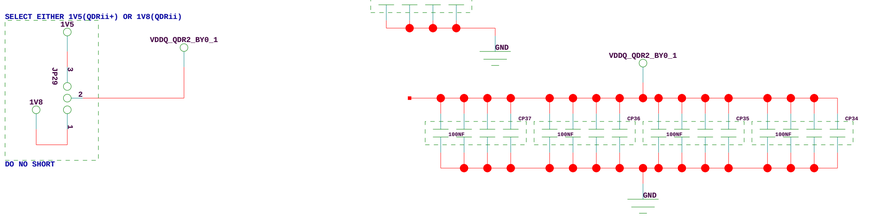
ROACH_GPIO_MISC
DOC NO: NRF-ADM-XXX-SD-0001
REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
CHECKED: E BAUERMEISTER
APPR:
SHEET 13 OF 25

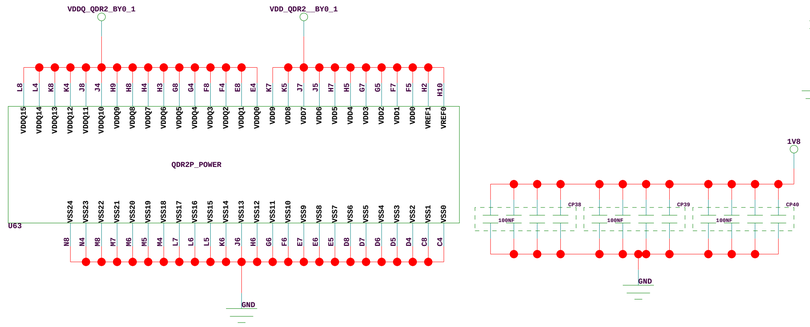


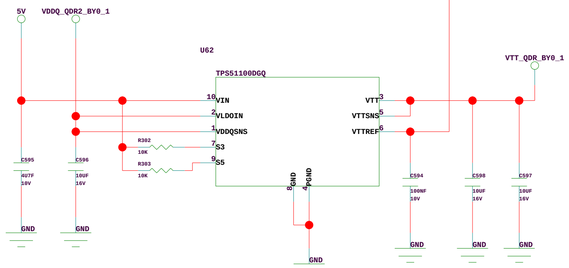




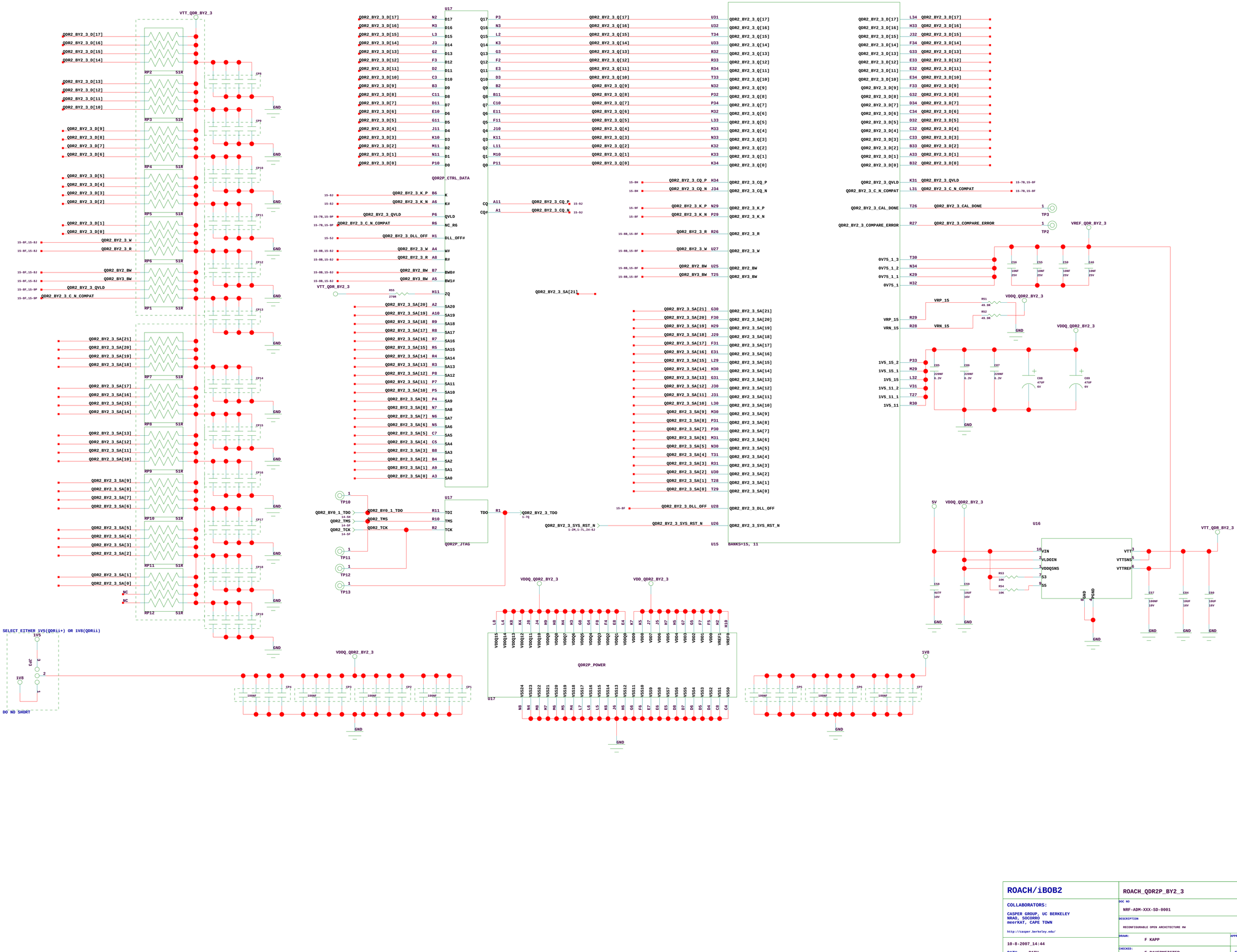








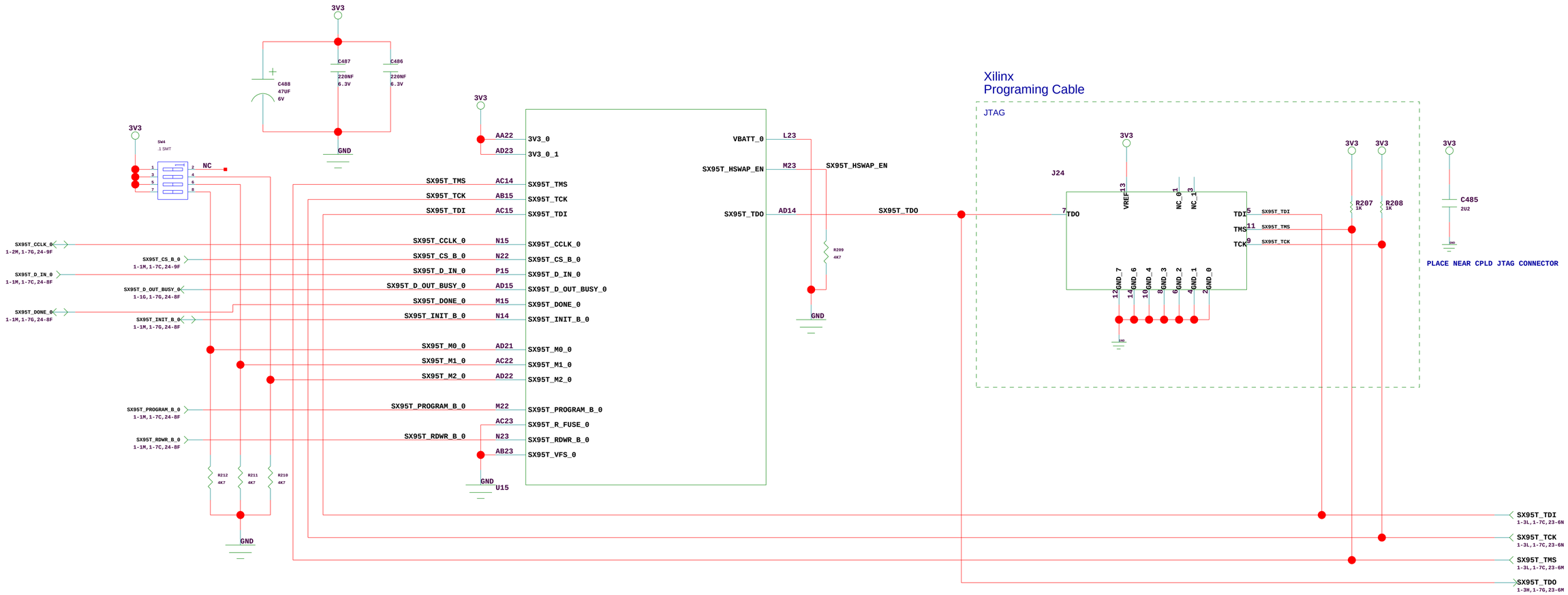
ROACH/iBOB2		**ROACH_QDR2P_BY0_1**	
COLLABORATORS:		DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/		DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
10-8-2007_14:44		DRAWN: F KAPP	APPR:
PATH PATH		CHECKED: E BAUERMEISTER	SHEET 14 OF 25



ROACH/iBOB2	ROACH_QDR2P_BY2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-8-2007_14:44	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 15 OF 25

TBD

VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input



ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
10-8-2007_14:44 PATH PATH	

Place components close to CPU

Place components close to CPU

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J3: "1V5"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J4: "1V8"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J5: "2V5"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J6: "3V3"

Place components close to CPU

Place components close to CPU

Alternate power input terminal
Two 10A fuses result in 16A rating

+5.0 V

Bulk Decoupling

CPU Core by-pass caps place as close to CPU Vdd pins as possible

Bulk Decoupling

CPU Core by-pass caps place as close to CPU SOVdd pins as possible

Bulk Decoupling

CPU Core by-pass caps place as close to CPU DVdd pins as possible

+1.8 V

Place all components within this block close together

~2.9Amp

~3.6Amp

Place these 4 caps close to DDR parts

VOUT= 0.6v(1+R1/R2)

PWR_GOOD

1-2G,1-3H,1-4D,1-5E,18-2F,23-19G,24-8K

+1.5 V

VOUT= 0.6v(1+R1/R2)
PLLLPF = VIN = 750khz

Each Analog GND tied to Digital GND at a single point.

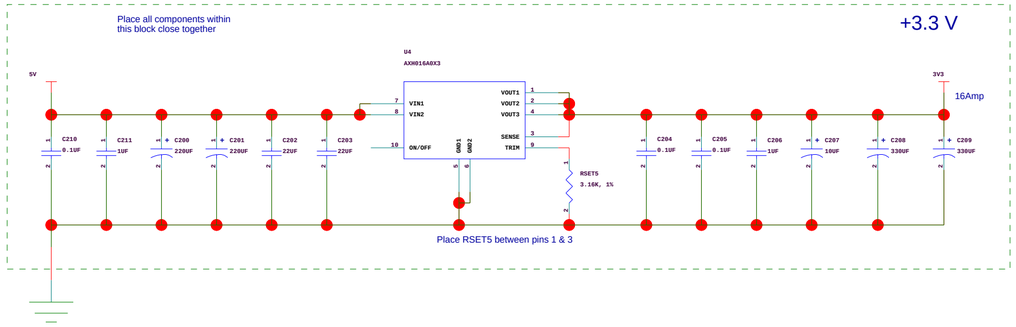
Place all components within this block close together

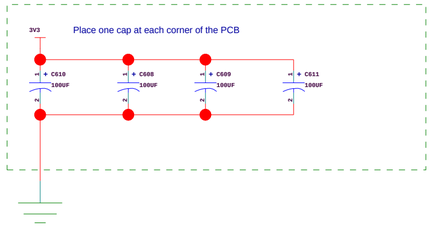
+0.9 V

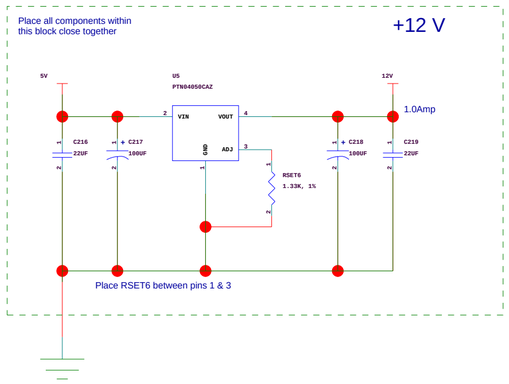
Use 25mil trace

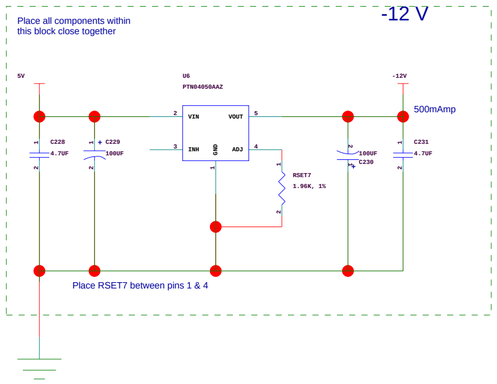
VTT island by-pass caps place evenly across VTT island
(1 cap for every 2 signals terminated)
(1 Tantalum Cap on each end of island)
VTT regulator placed at center of VTT island

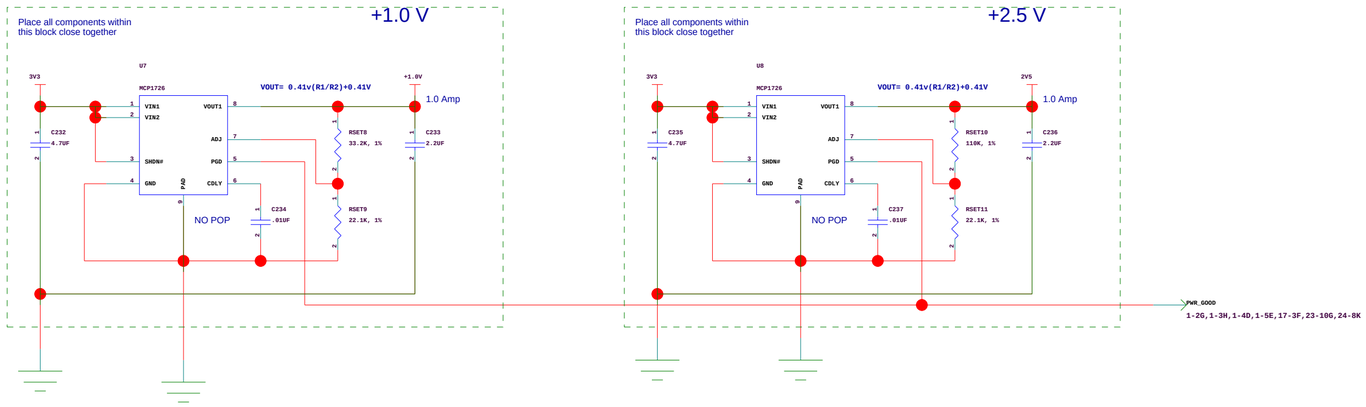
ROACH/iBOB2	ROACH_PPC_POWER_1
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-8-2007_14:44	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 17 OF 25



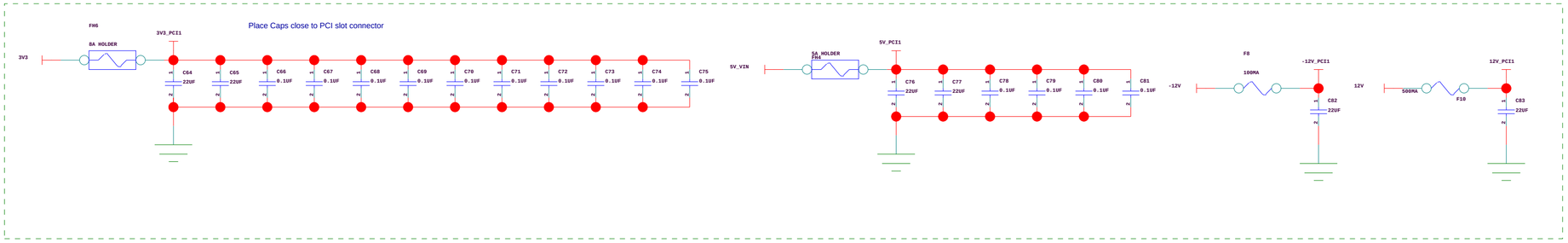


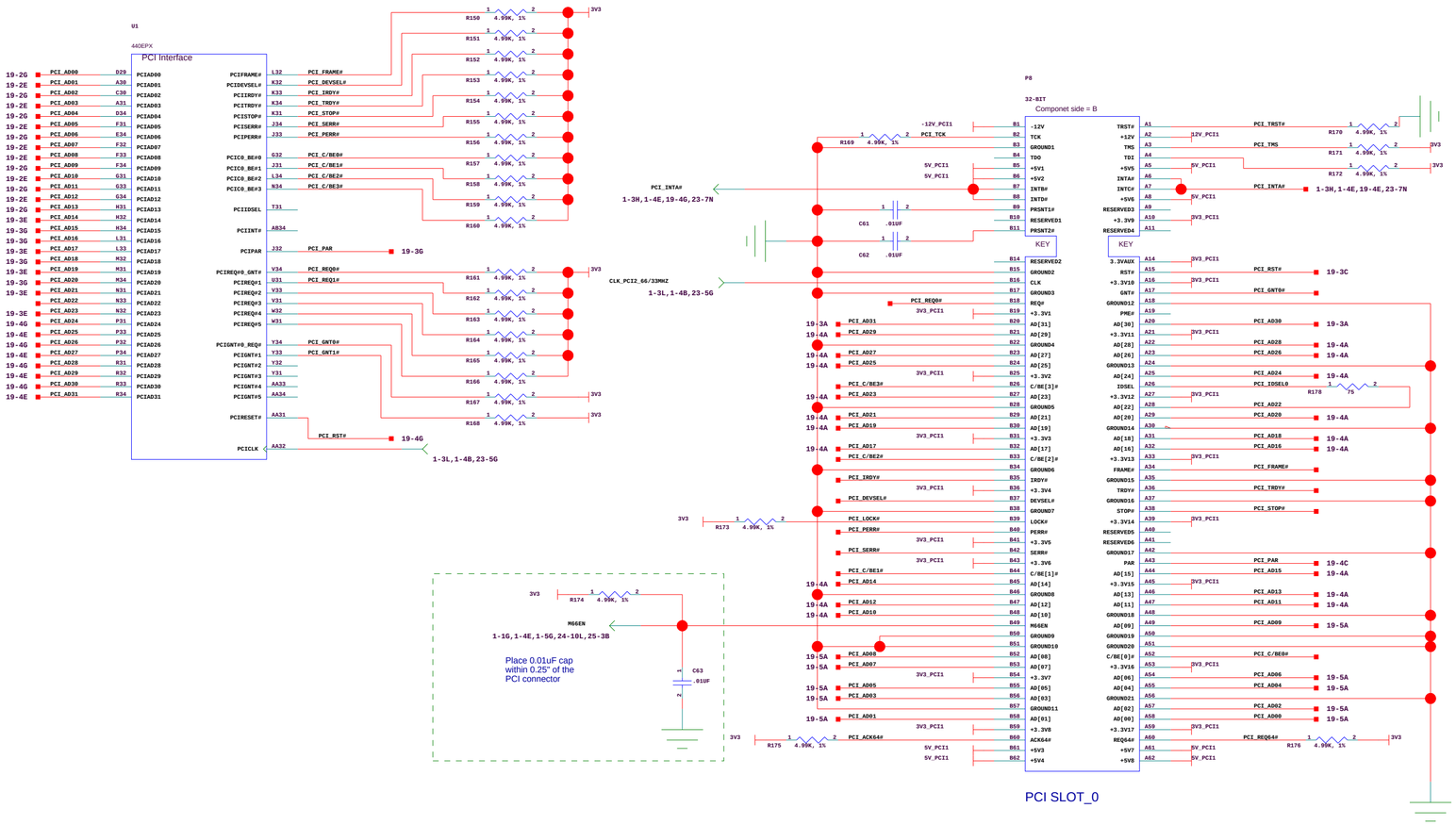






ROACH/iBOB2	**ROACH_PPC_POWER_2**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 18 OF 25
10-8-2007_14:44 PATH PATH	




U1
440EPX
PCI Interface
PCI_AD00 D29 PCIAD00
PCI_AD01 A30 PCIAD01
PCI_AD02 C30 PCIAD02
PCI_AD03 A31 PCIAD03
PCI_AD04 D34 PCIAD04
PCI_AD05 F31 PCIAD05
PCI_AD06 E34 PCIAD06
PCI_AD07 F32 PCIAD07
PCI_AD08 F33 PCIAD08
PCI_AD09 F34 PCIAD09
PCI_AD10 G31 PCIAD10
PCI_AD11 G33 PCIAD11
PCI_AD12 G34 PCIAD12
PCI_AD13 H31 PCIAD13
PCI_AD14 H32 PCIAD14
PCI_AD15 H34 PCIAD15
PCI_AD16 L31 PCIAD16
PCI_AD17 L33 PCIAD17
PCI_AD18 M32 PCIAD18
PCI_AD19 M31 PCIAD19
PCI_AD20 M34 PCIAD20
PCI_AD21 N31 PCIAD21
PCI_AD22 N33 PCIAD22
PCI_AD23 N32 PCIAD23
PCI_AD24 P31 PCIAD24
PCI_AD25 P33 PCIAD25
PCI_AD26 P32 PCIAD26
PCI_AD27 P34 PCIAD27
PCI_AD28 R31 PCIAD28
PCI_AD29 R32 PCIAD29
PCI_AD30 R33 PCIAD30
PCI_AD31 R34 PCIAD31
PCIFRAME# L32 PCI_FRAME#
PCIDEVSEL# K32 PCI_DEVSEL#
PCIIRDY# K33 PCI_IRDY#
PCITRDY# K34 PCI_TRDY#
PCISTOP# K31 PCI_STOP#
PCISERR# J34 PCI_SERR#
PCIPERR# J33 PCI_PERR#
PCICO_BE#0 G32 PCI_C/BE0#
PCICO_BE#1 J31 PCI_C/BE1#
PCICO_BE#2 L34 PCI_C/BE2#
PCICO_BE#3 N34 PCI_C/BE3#
PCIIDSEL T31
PCIINT# AB34
PCIPAR J32 PCI_PAR
PCIREQ#0_GNT# V34 PCI_REQ0#
PCIREQ#1 V31 PCI_REQ1#
PCIREQ#2 V33
PCIREQ#3 V31
PCIREQ#4 W32
PCIREQ#5 W31
PCIGNT#0_REQ# Y34 PCI_GNT0#
PCIGNT#1 Y33 PCI_GNT1#
PCIGNT#2 Y32
PCIGNT#3 Y31
PCIGNT#4 AA33
PCIGNT#5 AA34
PCIRESET# AA31
PCI_RST#
PCICLK AA32
19-3G
19-2E
19-2G
19-2E
19-2E
19-2G
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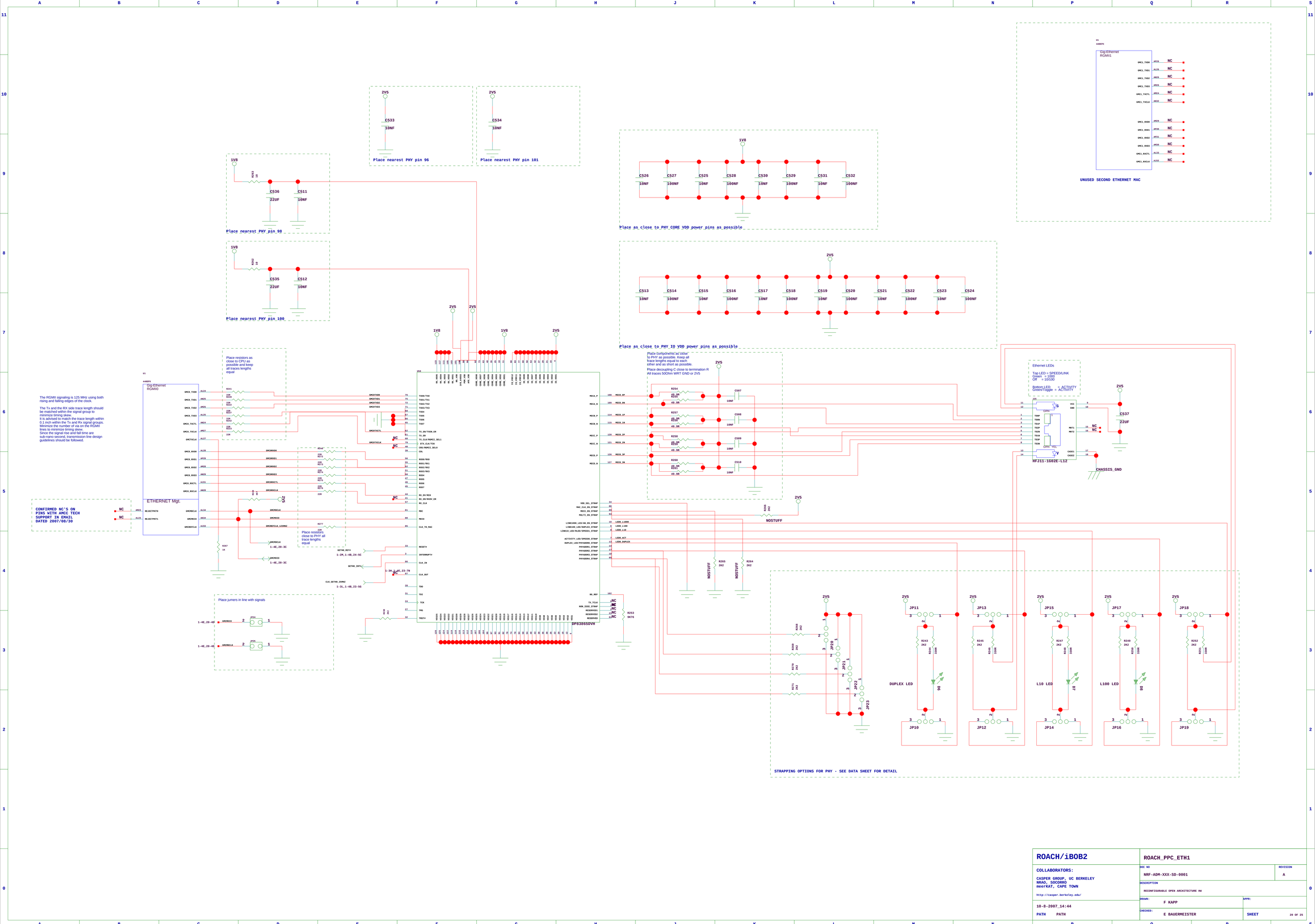
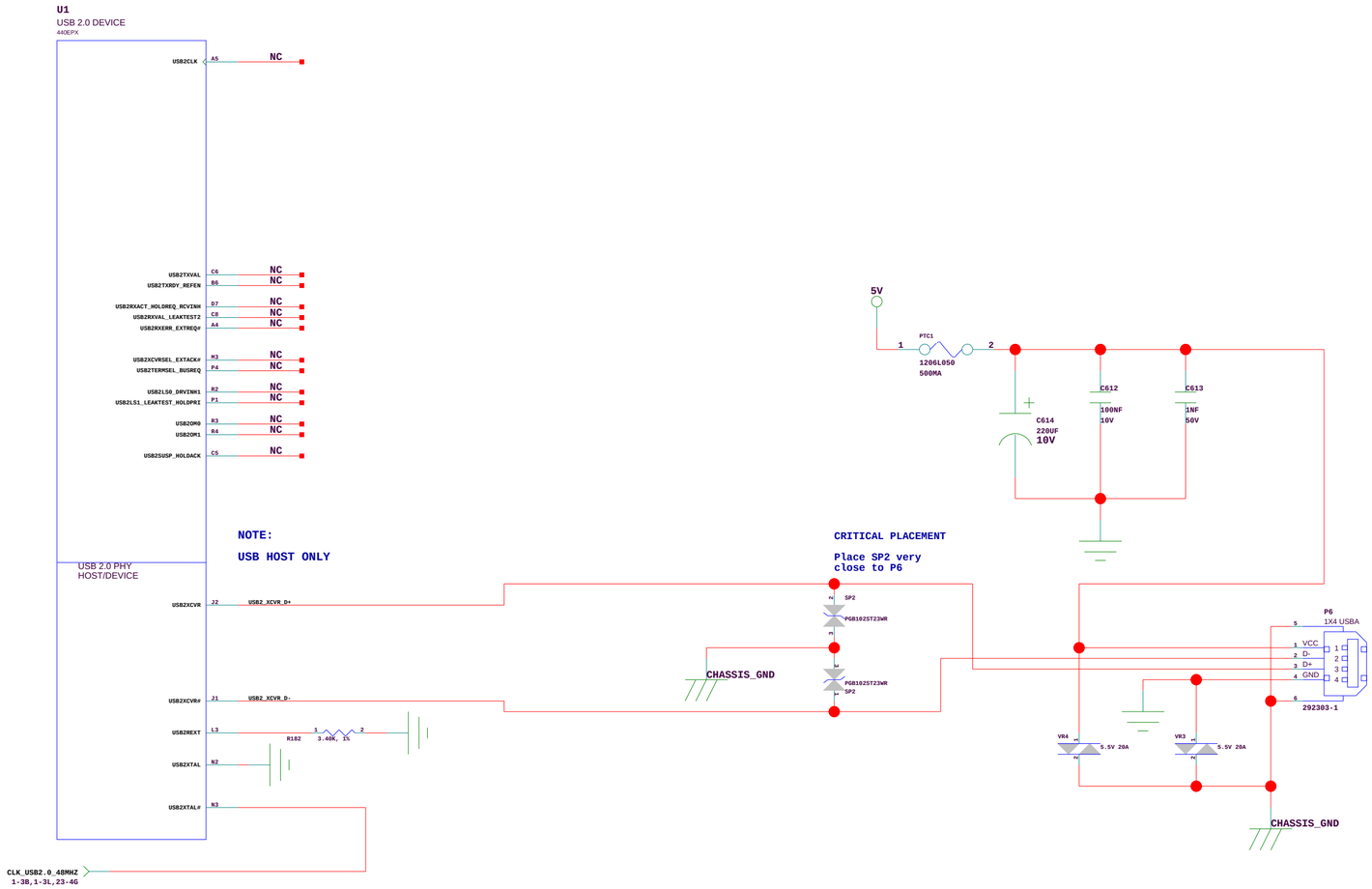


ROACH/iBOB2	**ROACH_PPC_ETH1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-8-2007_14:44 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 20 OF 25



ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR:
10-8-2007_14:44 PATH PATH	CHECKED: E BAUERMEISTER SHEET 21 OF 25

DDR_PA[15:0]

DDR_PD0[63:0]

U1

DDR SDRAM

64DEPX

DDR_PD0	AB2	MEMDATA00	MEMADDR00
DDR_PD1	AF2	MEMDATA01	MEMADDR01
DDR_PD2	AK5	MEMDATA02	MEMADDR02
DDR_PD3	AL28	MEMDATA03	MEMADDR03
DDR_PD4	AL22	MEMDATA04	MEMADDR04
DDR_PD5	AK2	MEMDATA05	MEMADDR05
DDR_PD6	AK1	MEMDATA06	MEMADDR06
DDR_PD7	AP21	MEMDATA07	MEMADDR07
DDR_PD8	AP28	MEMDATA08	MEMADDR08
DDR_PD9	AL18	MEMDATA09	MEMADDR09
DDR_PD10	AK17	MEMDATA10	MEMADDR10
DDR_PD11	AF17	MEMDATA11	MEMADDR11
DDR_PD12	AK26	MEMDATA12	MEMADDR12
DDR_PD13	AF18	MEMDATA13	MEMADDR13
DDR_PD14	AK18	MEMDATA14	
DDR_PD15	AF16	MEMDATA15	
DDR_PD16	AK16	MEMDATA16	
DDR_PD17	AF15	MEMDATA17	
DDR_PD18	AL15	MEMDATA18	
DDR_PD19	AF14	MEMDATA19	
DDR_PD20	AL17	MEMDATA20	
DDR_PD21	AK17	MEMDATA21	
DDR_PD22	AK15	MEMDATA22	
DDR_PD23	AK15	MEMDATA23	
DDR_PD24	AF13	MEMDATA24	
DDR_PD25	AK13	MEMDATA25	
DDR_PD26	AF12	MEMDATA26	
DDR_PD27	AL12	MEMDATA27	
DDR_PD28	AK14	MEMDATA28	
DDR_PD29	AK14	MEMDATA29	
DDR_PD30	AL13	MEMDATA30	
DDR_PD31	AK12	MEMDATA31	
DDR_PD32	AF3	MEMDATA32	
DDR_PD33	AF1	MEMDATA33	
DDR_PD34	AD4	MEMDATA34	
DDR_PD35	AD3	MEMDATA35	
DDR_PD36	AB3	MEMDATA36	
DDR_PD37	AF2	MEMDATA37	
DDR_PD38	AE2	MEMDATA38	
DDR_PD39	AE1	MEMDATA39	
DDR_PD40	AC3	MEMDATA40	
DDR_PD41	AC1	MEMDATA41	
DDR_PD42	AA4	MEMDATA42	
DDR_PD43	AA3	MEMDATA43	
DDR_PD44	AD2	MEMDATA44	
DDR_PD45	AC4	MEMDATA45	
DDR_PD46	AB1	MEMDATA46	
DDR_PD47	AB2	MEMDATA47	
DDR_PD48	Y3	MEMDATA48	
DDR_PD49	Y2	MEMDATA49	
DDR_PD50	Y4	MEMDATA50	
DDR_PD51	V3	MEMDATA51	
DDR_PD52	AA2	MEMDATA52	
DDR_PD53	AA1	MEMDATA53	
DDR_PD54	W3	MEMDATA54	
DDR_PD55	W1	MEMDATA55	
DDR_PD56	V1	MEMDATA56	
DDR_PD57	U2	MEMDATA57	
DDR_PD58	T4	MEMDATA58	
DDR_PD59	R1	MEMDATA59	
DDR_PD60	V3	MEMDATA60	
DDR_PD61	V1	MEMDATA61	
DDR_PD62	T3	MEMDATA62	
DDR_PD63	T1	MEMDATA63	

DDR_PA0	AM5	MEMADDR00	
DDR_PA1	AP4	MEMADDR01	
DDR_PA2	AP5	MEMADDR02	
DDR_PA3	AM6	MEMADDR03	
DDR_PA4	AP6	MEMADDR04	
DDR_PA5	AM4	MEMADDR05	
DDR_PA6	AL7	MEMADDR06	
DDR_PA7	AN7	MEMADDR07	
DDR_PA8	AN8	MEMADDR08	
DDR_PA9	AP7	MEMADDR09	
DDR_PA10	AL2	MEMADDR10	
DDR_PA11	AL8	MEMADDR11	
DDR_PA12	AN3	MEMADDR12	
DDR_PA13	AN4	MEMADDR13	
DDR_PBA0	AJ1	BA0	
DDR_PBA1	AN3	BA1	
DDR_PBA2	AP8	BA2	
DDR_PRAS#	AJ4	RAS#	
DDR_PCAS#	AN4	CAS#	
DDR_PWE#	AJ2	WE#	
DDR_PDM0	AL21	DM0	
DDR_PDM1	AP18	DM1	
DDR_PDM2	AP15	DM2	
DDR_PDM3	AL14	DM3	
DDR_PDM4	AD4	DM4	
DDR_PDM5	AB3	DM5	
DDR_PDM6	Y3	DM6	
DDR_PDM7	V3	DM7	
DDR_PDM8	AN18	DM8	
DDR_PDQS0	AM21	DQS0	
DDR_PDQS1	AM19	DQS1	
DDR_PDQS2	AL16	DQS2	
DDR_PDQS3	AM13	DQS3	
DDR_PDQS4	AB3	DQS4	
DDR_PDQS5	AB4	DQS5	
DDR_PDQS6	W3	DQS6	
DDR_PDQS7	Y3	DQS7	
DDR_PDQS8	AP10	DQS8	
DDR_PODT0	AN3	MEMODT0	
DDR_PODT1	AG1	MEMODT1	
DDR_PCS0#	AN2	BANKSELA0	
DDR_PCS1#	AM1	BANKSELA1	
DDR_PCKE	AN9	MEMCKE0	
DDR_CLKOUT	AL1	MEMCLKOUT	
DDR_CLKOUT#	AM1	MEMCLKOUT#	

PPC_ECC0	AM11	ECC0	22-9F
PPC_ECC1	AL11	ECC1	22-9F
PPC_ECC2	AN9	ECC2	22-9F
PPC_ECC3	AL9	ECC3	22-10F
PPC_ECC4	AM11	ECC4	22-10F
PPC_ECC5	AN11	ECC5	22-10F
PPC_ECC6	AM10	ECC6	22-10F
PPC_ECC7	AP9	ECC7	22-10F

	AM8	SVREF1A	
	AL10	SVREF1B	
	AF4	SVREF2A	
	AL19	SVREF2B	

R212 1 2

R213 1 2

500ps Loop

DDR_CLKOUT

DDR_CLKOUT#

DDR_VREF_0V9

1V8

C158 0.10F

C148 0.10F

C151 0.10F 0402

C152 0.10F 0402

C148 0.01UF

Place parts as close to CPU as possible

5V

1V8

U32

VIN 10

VLDOIN 2

VDDQSNS 1

S3 7

S5 9

VTT 3

VTTSNS 5

VTTREF 6

GND 8

PGND 4

R230 10K

R229 10K

C459 4U7F 10V

C456 10UF 16V

C453 100NF 10V

C457 10UF 16V

C458 10UF 16V

DDR_VTT

DDR_VREF_0V9

GND

J8

22-6D	PPC_ECC7	168	DDR2_DIMM_CB7
22-6D	PPC_ECC6	167	DDR2_DIMM_CB6
22-7D	PPC_ECC5	162	DDR2_DIMM_CB5
22-7D	PPC_ECC4	161	DDR2_DIMM_CB4
22-7D	PPC_ECC3	49	DDR2_DIMM_CB3
22-7D	PPC_ECC2	48	DDR2_DIMM_CB2
22-7D	PPC_ECC1	43	DDR2_DIMM_CB1
22-7D	PPC_ECC0	42	DDR2_DIMM_CB0
DDR_PDQ63		236	DDR2_DIMM_DQ[63]
DDR_PDQ62		235	DDR2_DIMM_DQ[62]
DDR_PDQ61		230	DDR2_DIMM_DQ[61]
DDR_PDQ60		229	DDR2_DIMM_DQ[60]
DDR_PDQ59		117	DDR2_DIMM_DQ[59]
DDR_PDQ58		116	DDR2_DIMM_DQ[58]
DDR_PDQ57		111	DDR2_DIMM_DQ[57]
DDR_PDQ56		110	DDR2_DIMM_DQ[56]
DDR_PDQ55		227	DDR2_DIMM_DQ[55]
DDR_PDQ54		226	DDR2_DIMM_DQ[54]
DDR_PDQ53		218	DDR2_DIMM_DQ[53]
DDR_PDQ52		217	DDR2_DIMM_DQ[52]
DDR_PDQ51		108	DDR2_DIMM_DQ[51]
DDR_PDQ50		107	DDR2_DIMM_DQ[50]
DDR_PDQ49		99	DDR2_DIMM_DQ[49]
DDR_PDQ48		98	DDR2_DIMM_DQ[48]
DDR_PDQ47		215	DDR2_DIMM_DQ[47]
DDR_PDQ46		214	DDR2_DIMM_DQ[46]
DDR_PDQ45		209	DDR2_DIMM_DQ[45]
DDR_PDQ44		208	DDR2_DIMM_DQ[44]
DDR_PDQ43		96	DDR2_DIMM_DQ[43]
DDR_PDQ42		95	DDR2_DIMM_DQ[42]
DDR_PDQ41		90	DDR2_DIMM_DQ[41]
DDR_PDQ40		89	DDR2_DIMM_DQ[40]
DDR_PDQ39		206	DDR2_DIMM_DQ[39]
DDR_PDQ38		205	DDR2_DIMM_DQ[38]
DDR_PDQ37		200	DDR2_DIMM_DQ[37]
DDR_PDQ36		199	DDR2_DIMM_DQ[36]
DDR_PDQ35		87	DDR2_DIMM_DQ[35]
DDR_PDQ34		86	DDR2_DIMM_DQ[34]
DDR_PDQ33		81	DDR2_DIMM_DQ[33]
DDR_PDQ32		80	DDR2_DIMM_DQ[32]
DDR_PDQ31		159	DDR2_DIMM_DQ[31]
DDR_PDQ30		158	DDR2_DIMM_DQ[30]
DDR_PDQ29		153	DDR2_DIMM_DQ[29]
DDR_PDQ28		152	DDR2_DIMM_DQ[28]
DDR_PDQ27		40	DDR2_DIMM_DQ[27]
DDR_PDQ26		39	DDR2_DIMM_DQ[26]
DDR_PDQ25		34	DDR2_DIMM_DQ[25]
DDR_PDQ24		33	DDR2_DIMM_DQ[24]
DDR_PDQ23		150	DDR2_DIMM_DQ[23]
DDR_PDQ22		149	DDR2_DIMM_DQ[22]
DDR_PDQ21		144	DDR2_DIMM_DQ[21]
DDR_PDQ20		143	DDR2_DIMM_DQ[20]
DDR_PDQ19		31	DDR2_DIMM_DQ[19]
DDR_PDQ18		30	DDR2_DIMM_DQ[18]
DDR_PDQ17		25	DDR2_DIMM_DQ[17]
DDR_PDQ16		24	DDR2_DIMM_DQ[16]
DDR_PDQ15		141	DDR2_DIMM_DQ[15]
DDR_PDQ14		140	DDR2_DIMM_DQ[14]
DDR_PDQ13		132	DDR2_DIMM_DQ[13]
DDR_PDQ12		131	DDR2_DIMM_DQ[12]
DDR_PDQ11		22	DDR2_DIMM_DQ[11]
DDR_PDQ10		21	DDR2_DIMM_DQ[10]
DDR_PDQ9		13	DDR2_DIMM_DQ[9]
DDR_PDQ8		12	DDR2_DIMM_DQ[8]
DDR_PDQ7		129	DDR2_DIMM_DQ[7]
DDR_PDQ6		128	DDR2_DIMM_DQ[6]
DDR_PDQ5		123	DDR2_DIMM_DQ[5]
DDR_PDQ4		122	DDR2_DIMM_DQ[4]
DDR_PDQ3		10	DDR2_DIMM_DQ[3]
DDR_PDQ2		9	DDR2_DIMM_DQ[2]
DDR_PDQ1		4	DDR2_DIMM_DQ[1]
DDR_PDQ0		3	DDR2_DIMM_DQ[0]
		101	DDR2_DIMM_SA2
		240	DDR2_DIMM_SA1
		239	DDR2_DIMM_SA0
		120	DDR2_DIMM_SCL
		119	DDR2_DIMM_SDA

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1V8

R228 4K7

R227 4K7

PPC_DDR2_DIMM_SCL

PPC_DDR2_DIMM_SDA

GND

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA1	22-8L,22-9D
DDR2_DIMM_BA[1]	190	DDR_PBA2	22-8L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-8L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	NC	
DDR2_DIMM_CK_N[2]	221	NC	
DDR2_DIMM_CK_P[1]	137	NC	
DDR2_DIMM_CK_N[1]	138	NC	
DDR2_DIMM_CK_P[0]	185	DDR_CLKOUT	
DDR2_DIMM_CK_N[0]	186	DDR_CLKOUT#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-7L,22-8D
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-9D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D
ERR_OUT	55	PPC_DDR2_ERROR	
PAR_IN	68	PAR_IN	

R226 4K7

PPC_DDR2_RESET_N

1-2M,1-3B,24-5J

C455 5PF 50V

1

TP4

TP5

DDR_VTT

DDR_PA15
DDR_PA14
DDR_PA13
DDR_PA12

RP24

DDR_PA11
DDR_PA10
DDR_PA9
DDR_PA8

RP23

DDR_PA7
DDR_PA6
DDR_PA5
DDR_PA4

RP22

DDR_PA3
DDR_PA2
DDR_PA1
DDR_PA0

RP21

CP26 CP28 CP29 CP30

GND

22-8K,22-9D DDR_PBA1
22-8K,22-9D DDR_PBA2
22-8K,22-9D DDR_PBA0
22-8K,22-9D DDR_PCAS#

RP25

22-7K,22-9D DDR_PRAS#
22-6K,22-8D DDR_PCKE
22-3K,22-9D DDR_PWE#
22-3K,22-8D DDR_PCS0#

RP26

22-3K,22-8D DDR_PCS1#
22-8D DDR_PODT0
22-8D DDR_PODT1

NC

RP19

CP32 CP31 CP33

J8

	237	VSS_64	
	234	VSS_63	
	231	VSS_62	
	228	VSS_61	
	225	VSS_60	
	222	VSS_59	
	219	VSS_58	
	216	VSS_57	
	213	VSS_56	
	210	VSS_55	
	207	VSS_54	
	204	VSS_53	
	201	VSS_52	
	198	VSS_51	
	169	VSS_50	
	166	VSS_49	
	163	VSS_48	
	160	VSS_47	
	157	VSS_46	
	154	VSS_45	
	151	VSS_44	
	148	VSS_43	
	145	VSS_42	
	142	VSS_41	
	139	VSS_40	
	136	VSS_39	
	133	VSS_38	
	130	VSS_37	
	127	VSS_36	
	124	VSS_35	
	121	VSS_34	
	118	VSS_33	
	115	VSS_32	
	112	VSS_31	
	109	VSS_30	
	106	VSS_29	
	103	VSS_28	
	100	VSS_27	
	97	VSS_26	
	94	VSS_25	
	91	VSS_24	
	88	VSS_23	
	85	VSS_22	
	82	VSS_21	
	79	VSS_20	
	66	VSS_19	
	65	VSS_18	
	50	VSS_17	
	47	VSS_16	
	44	VSS_15	
	41	VSS_14	
	38	VSS_13	
	35	VSS_12	
	32	VSS_11	
	29	VSS_10	
	26	VSS_9	
	23	VSS_8	
	20	VSS_7	
	17	VSS_6	
	14	VSS_5	
	11	VSS_4	
	8	VSS_3	
	5	VSS_2	
	2	VSS_1	

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DDR_VREF_0V9

VREF 1

1V8

VDDSPD 238

1V8

VDD_11	197	
VDD_10	189	
VDD_9	187	
VDD_8	184	
VDD_7	178	
VDD_6	172	
VDD_5	69	
VDD_4	67	
VDD_3	64	
VDD_2	59	
VDD_1	53	

1V8

VDDQ_11	194	
VDDQ_10	191	
VDDQ_9	181	
VDDQ_8	175	
VDDQ_7	170	
VDDQ_6	78	
VDDQ_5	75	
VDDQ_4	72	
VDDQ_3	62	
VDDQ_2	56	
VDDQ_1	51	

GND

DDR_VREF_0V9

1V8

C432 100NF 10V

C433 10NF 25V

C454 100NF 10V

C434 10NF 25V

C430 100NF 10V

C443 10NF 25V

C431 100NF 10V

C444 10NF 25V

C436 100NF 10V

C445 10NF 25V

C435 100NF 10V

C446 10NF 25V

C438 100NF 10V

C451 10NF 25V

C437 100NF 10V

C452 10NF 25V

C439 100NF 10V

C449 10NF 25V

C440 100NF 10V

C450 10NF 25V

C441 100NF 10V

C448 10NF 25V

C442 100NF 10V

C447 10NF 25V

PLACE NEAREST DDR2 MODULE PINS

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

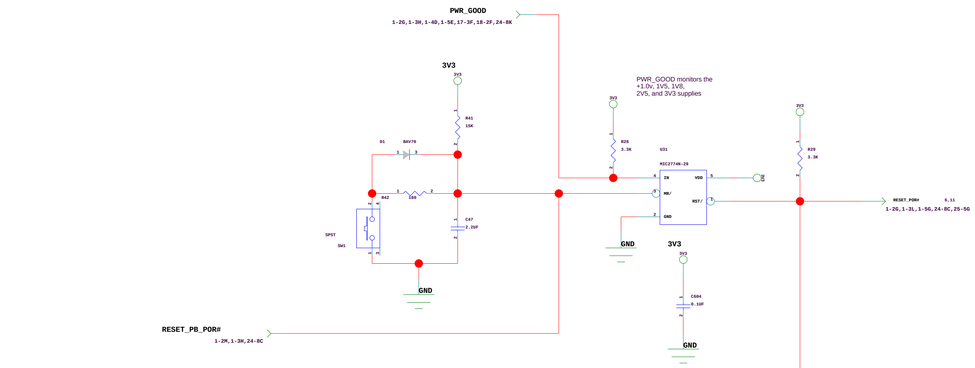
http://casper.berkeley.edu/

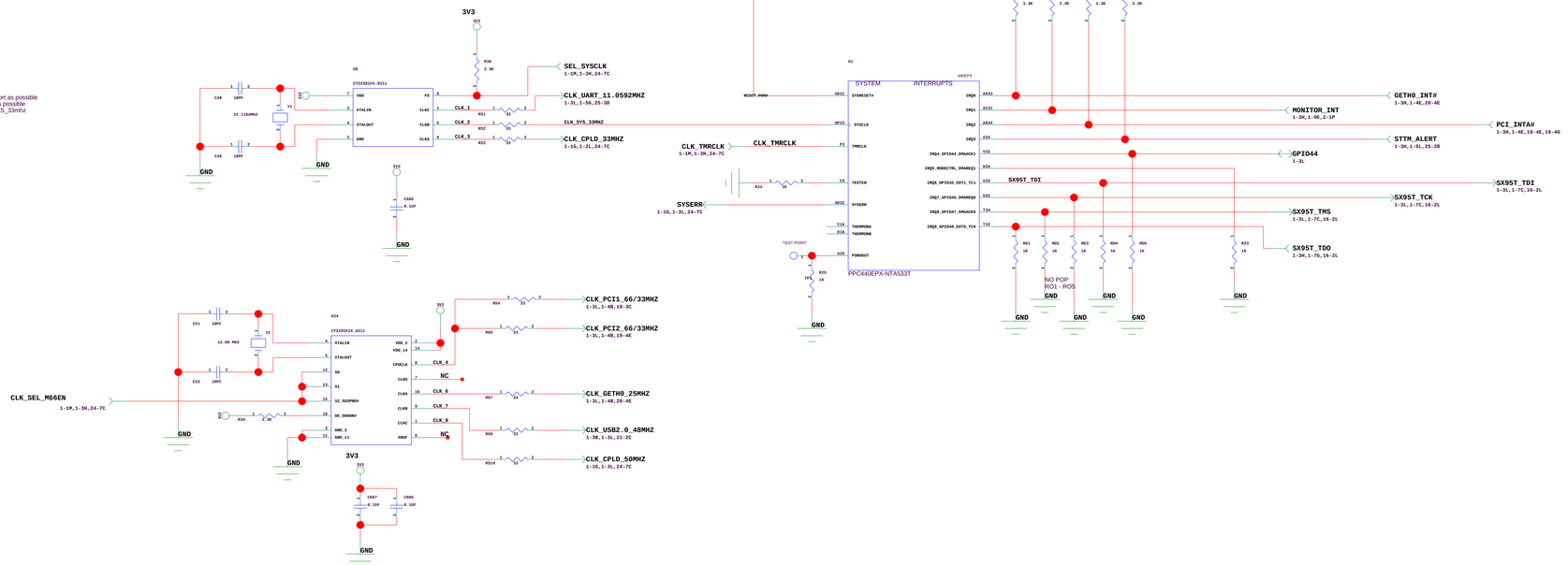
10-8-2007_14:44

PATH PATH

ROACH_PPC_DDR2

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	22 OF 25





ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

10-8-2007_14:44

PATH PATH

ROACH_PPC_TST_CLK_IO

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

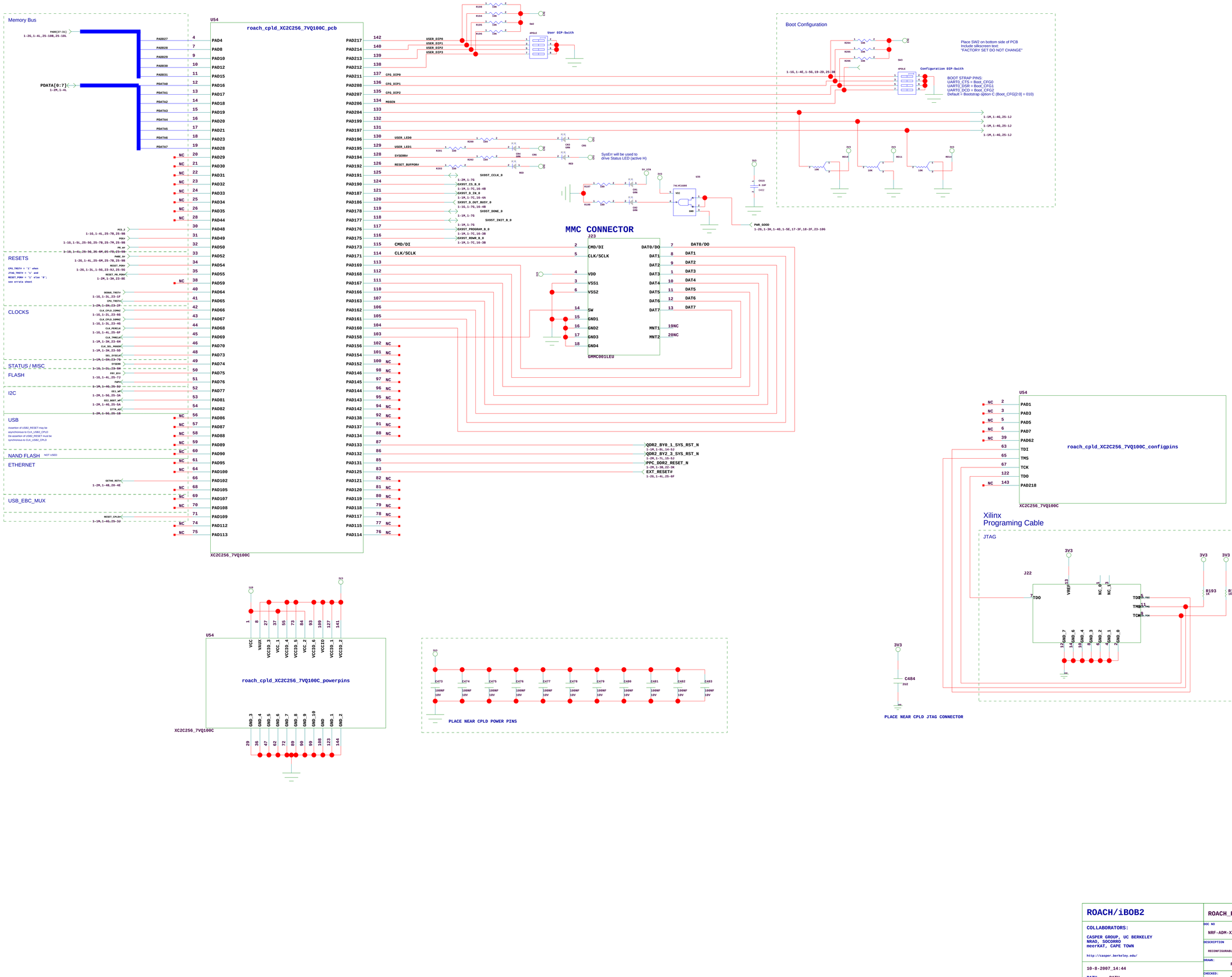
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 23 OF 25



ROACH/iBOB2	**ROACH_PPC_CPLD**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-8-2007_14:44 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 24 OF 25

PDATA[0:31]
1-2M,1-4L

PADD[2:31]

1-2G,1-4L,24-16B,25-10B,25-19L

PCS_0
PCS_1
PCS_2
PCS_4_GPIO09
PCS_5_GPIO010
PDEV
PB_WP
PWBE_0#
PWBE_1#
PWBE_2#
PWBE_3#
PREADY
PBLASTF#

25-5G,25-8C
25-7C,25-7M
1-1G,1-4L,24-8C,25-7B
25-7C
25-7C
1-1G,1-5L,24-8C,25-5G,25-7B,25-7M
1-1G,1-4L,24-8C,25-5M,25-7B
1-2G,1-4L,24-8C,25-6M,25-7B
25-6M,25-7C
25-7C
25-7C
25-7C,25-8Q

U1
External Slave Peripheral
AXEEPX

PERDATA31
PERDATA30
PERDATA29
PERDATA28
PERDATA27
PERDATA26
PERDATA25
PERDATA24
PERDATA23
PERDATA22
PERDATA21
PERDATA20
PERDATA19
PERDATA18
PERDATA17
PERDATA16
PERDATA15
PERDATA14
PERDATA13
PERDATA12
PERDATA11
PERDATA10
PERDATA9
PERDATA8
PERDATA7
PERDATA6
PERDATA5
PERDATA4
PERDATA3
PERDATA2
PERDATA1
PERDATA0

PERADDR31
PERADDR30
PERADDR29
PERADDR28
PERADDR27
PERADDR26
PERADDR25
PERADDR24
PERADDR23
PERADDR22
PERADDR21
PERADDR20
PERADDR19
PERADDR18
PERADDR17
PERADDR16
PERADDR15
PERADDR14
PERADDR13
PERADDR12
PERADDR11
PERADDR10
PERADDR9
PERADDR8
PERADDR7
PERADDR6
PERADDR5
PERADDR4
PERADDR3
PERADDR2

PA031
PA030
PA029
PA028
PA027
PA026
PA025
PA024
PA023
PA022
PA021
PA020
PA019
PA018
PA017
PA016
PA015
PA014
PA013
PA012
PA011
PA010
PA009
PA008
PA007
PA006
PA005
PA004
PA003
PA002

PERCS0#
PERCS1#_GPIO06
PERCS4#_GPIO09
PERCS5#_GPIO10
PERRDY
PERM_WP
PERWBE0#
PERWBE1#
PERWBE2#
PERWBE3#
PERREADY
PERBLAST#

PERADDR07_GPIO08_DMAREQ3
PERADDR06_GPIO01_DMAACK3
PERADDR05_GPIO02_EOT2_TC2
GPIO03_PERADDR04_DMAREQ2
GPIO04_PERADDR03_DMAACK2
GPIO05_PERADDR02_EOT1_TC1

External Master Peripheral Interface

EXTRESET#2
PERCLK
PERERR_GPIO11

CLK_PERCLK
Z5-8Q
NO POP
R85 1K
J7 0.1in x 0.1in
EXT_RESET#
1-2G,1-4L,24-5J
CLK_PERCLK
1-1G,1-4L,24-7C

R84 1K
R83 1K
R86 4.99K, 1%
R87 4.99K, 1%
R88 4.99K, 1%

3V3

U42
32MX16 MIRROR BIT
FLASH 32Mx16 4Mx8

PA0030
PA0029
PA0028
PA0027
PA0026
PA0025
PA0024
PA0023
PA0022
PA0021
PA0020
PA0019
PA0018
PA0017
PA0016
PA0015
PA0014
PA0013
PA0012
PA0011
PA0010
PA0009
PA0008
PA0007
PA0006
PA0005

A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21_A0MB_
A22_128MB_
A23_256MB_
A24_512MB_
A25_1GB_

BYTE#
CE#
OE#
WE#
RESET#

WP#/ACC
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15/A-1
RY/BY#
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11

R89 3.3K
R90 3.3K
R91 3.3K
PWP#
1-1M,1-4G,24-6C
RY_BY#
1-1G,1-4L,24-6C

PA031
PA030
PA029
PA028
PA027
PA026
PA025
PA024
PA023
PA022
PA021
PA020
PA019
PA018
PA017
PA016
PA015
PA014
PA013
PA012
PA011
PA010
PA009
PA008
PA007
PA006
PA005
PA004
PA003
PA002

1-2G,1-4L,24-16B,25-10B

AE12 PER_A[30]
AF23 PER_A[29]
AG23 PER_A[28]
AF13 PER_A[27]
AG12 PER_A[26]
AE22 PER_A[25]
AE23 PER_A[24]
AG20 PER_A[23]
AH15 PER_A[22]
AG15 PER_A[21]
AG18 PER_A[20]
AF19 PER_A[19]
AH17 PER_A[18]
AG16 PER_A[17]
L21 PER_SP_A[16]
L20 PER_SP_A[15]
L15 PER_SP_A[14]
L16 PER_SP_A[13]
J22 PER_SP_A[12]
K21 PER_SP_A[11]
K16 PER_SP_A[10]
J15 PER_SP_A[9]
G22 PER_SP_A[8]
H22 PER_SP_A[7]
L14 PER_SP_A[6]
K14 PER_SP_A[5]
K23 PER_SP_A[4]
K22 PER_SP_A[3]
J12 PER_SP_A[2]

3V3
3V3_4_1 AL12
3V3_4_2 AG14
3V3_3_1 AH19
3V3_3_2 AH21
3V3_2_1 G14
3V3_1_1 D13

PCS_1 AE14 PER_CS0
25-7C,25-10B
POE# AF21 PER_OE_N
1-1G,1-5L,24-8C,25-5G,25-7B,25-9B
PR_W# AF20 PER_R_W_N
1-1G,1-4L,24-8C,25-5G,25-7B,25-9B
PWBE_1# AF18 PER_WBE[1]
25-7C,25-9B
PWBE_0# AF14 PER_WBE[0]
1-2G,1-4L,24-8C,25-7B,25-9B
PBLAST# AE18 PER_B_LAST
25-7C,25-8B

U15
BANKS=1, 2, 4
CHIP SELECT 1

PER_D[15] AF15 PDATA15
PER_D[14] AE16 PDATA14
PER_D[13] AE21 PDATA13
PER_D[12] AD20 PDATA12
PER_D[11] AF16 PDATA11
PER_D[10] AE17 PDATA10
PER_D[9] AE19 PDATA9
PER_D[8] AD19 PDATA8
PER_D[7] AG22 PDATA7
PER_D[6] AH22 PDATA6
PER_D[5] AH12 PDATA5
PER_D[4] AG13 PDATA4
PER_D[3] AH20 PDATA3
PER_D[2] AH19 PDATA2
PER_D[1] AH14 PDATA1
PER_D[0] AH13 PDATA0

PER_D_PAR[1] AG21 NC
PER_D_PAR[0] AE13 NC
PER_D_PAR[1]
PER_D_PAR[0]

PER_ERR AG17 PERERR
25-6E

PER_READY AH18 PREADY
25-7C,25-9B

C334 470F 6V
C335 470F 6V
C330 220NF 0.3V
C331 220NF 0.3V
C332 220NF 0.3V
C333 220NF 0.3V
GND

I2C0_SCLK
1-5L,1-9B,2-2P
I2C0_33_DATA
1-5L,1-9E

EE2_BOOT_WP
1-2M,1-4G,24-6C

A7140B8
VCC
WP
SCL
SDA
A2
A1
A0
GND
I2C0_SCLK
I2C0_33_DATA
R88 15K

NO POP
R59
I2C0_33_DATA
I2C0_SDATA
U47
PI5A3157
S/B GO TO A

I2C0_66_DATA
R89 15K

MGGEN
1-1G,1-4E,1-5G,19-2D,24-10L

EE1_WP
1-2M,1-5G,24-6C

CLK_UART_11.0592MHZ
1-1L,1-5G,23-7G

U1
4XEEPX
UART
UARTSERCLK

UART1_TX_UART0_TX
UART1_RX_UART0_RX
UART1_RTS#_UART0_RTS#
UART1_CTS#_UART0_CTS#
UART2_TX_UART0_DTR#
UART2_RX_UART0_RI#
UART2_RTS#_UART0_DSR#
UART2_CTS#_UART0_DCD#

UART1_TX
UART1_RX
UART2_TX
UART2_RX
CPU_UART0_DSR#
CPU_UART0_DCD#

IIC0
IIC0SCLK
IIC0SDATA

IIC1_SPI
SCPCLKOUT_IIC1SCLK
SCPDI_IIC1SDATA
SCPDO

NAND Flash Interface
NOT USED

NFALE
NFCLE
NFREN#
NFWEN#
NFRDYBUSY#
NFCE3#_PERCS3#

U41
ADT7414-B
VDD
ALERT
GND
SCL
SDA
A0
I2C0_SCLK
I2C0_SDATA
STTM_ALERT
1-3M,1-5L,23-6N

P11
0.12k H SMT
P4
0.12k H SMT

R72 3.3K
R74 3.3K
R75 3.3K
R76 3.3K
R77 3.3K
R78 3.3K

SCPCLK
SCPDI
SCPDO
SCPCLK
1-5L
SCPDI
1-5L
SCPDO
1-5L

STTM_AS
1-2M,1-5G,24-6C

C651 0.1UF 0402

PCS_0
1-1G,1-5L,24-8C,25-7M,25-9B
PDEV
1-1G,1-5L,24-8C,25-5G,25-7M,25-9B
PB_WP
1-1G,1-4L,24-8C,25-5G,25-6M,25-9B
PWBE_0#
1-2G,1-4L,24-8C,25-6M,25-9B
PWBE_1#
PWBE_2#
PWBE_3#
PREADY
PBLAST#
25-5G,25-10B
25-7M,25-10B
25-9B
25-9B
25-6M,25-9B
25-9B
25-9B
25-8Q,25-9B
25-6M,25-8B

Z5-8C,25-10B
PCS_0
1-1G,1-5L,24-8C,25-7B,25-7M,25-9B
PDEV
1-1G,1-4L,24-8C,25-6M,25-7B,25-9B
PB_WP
RESET_PORb
1-2G,1-3L,1-5G,23-9J,24-8C

U44
U43
ICL3225ECA
C1P
C1N
C2P
C2N
VCC
VP
VN
T1IN
R1OUT
T2IN
R2OUT
FORCEOFF
FORCEON
INVALID
READY
GND
C192 0.1UF 0402
C194 0.1UF 0402
C193 0.1UF 0402
C195 0.1UF 0402
C196 0.1UF 0402
C198 0.1UF 0402
C197 0.1UF 0402
C199 0.1UF 0402
C648 0.1UF 0402
C653 0.1UF 0402
R85 10K
R87 10K
X_UART1_TX
X_UART1_RX
X_UART1_RTS#
X_UART1_CTS#
X_UART2_TX
X_UART2_RX
X_UART2_RTS#
X_UART2_CTS#

5V_VIN
P2
9P DSUB MALE
CTS#1
UART Port 0

J14
HLE-105-02-G-DV
UART Port 1

C652 0.1UF 0402
C658 0.1UF 0402
C659 0.1UF 0402
C654 0.1UF 0402
C655 0.1UF 0402
C650 0.1UF 0402

U48
U45
U46
PI5A3157
S/B GO TO A
UART1_CTS#
UART2_RTS#
UART2_CTS#
R82 3.3K

RESET_CPLD#
1-1M,1-4G,24-5C

BOOT_CFG2
1-1M,1-4G,24-9M
BOOT_CFG1
1-1M,1-4G,24-9M
BOOT_CFG0
1-1M,1-4G,24-9M

ROACH/iBOB2	ROACH_PPC_NVM_SERIAL
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-8-2007_14:44 PATH PATH	DRAWN: F KAPP APPR:
	CHECKED: E BAUERMEISTER SHEET 25 OF 25