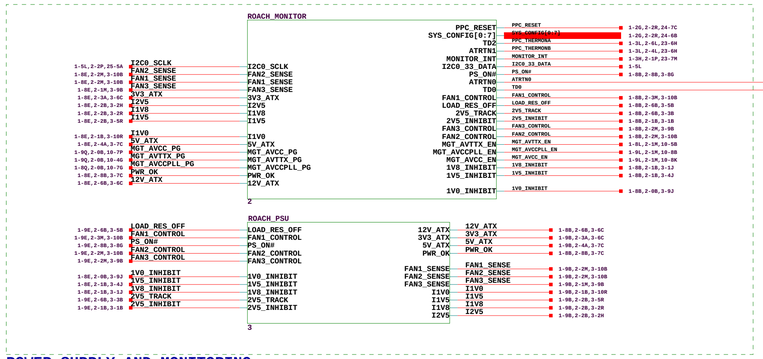
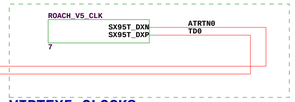
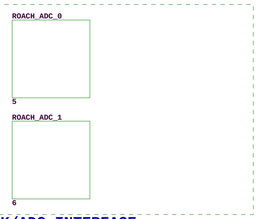
VIRTEX5

POWER SUPPLY AND MONITORING



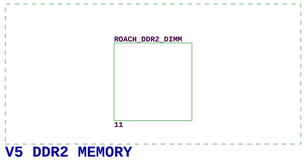
VIRTEX5 CLOCKS



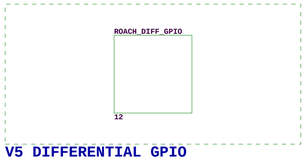


ZDOK/ADC INTERFACE

V5 DDR2 MEMORY

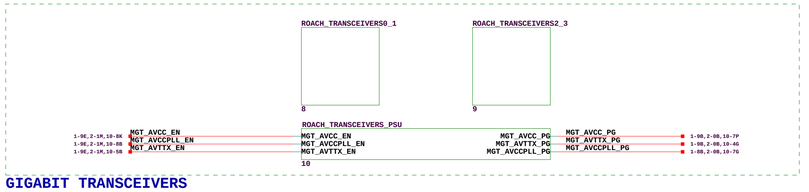


V5 DIFFERENTIAL GPIO

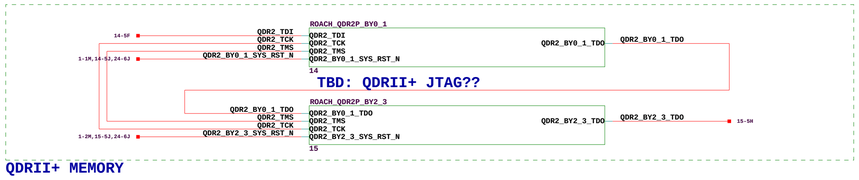


V5 SE GPIO & MISCELLANEOUS

GIGABIT TRANSCEIVERS



QDRII+ MEMORY



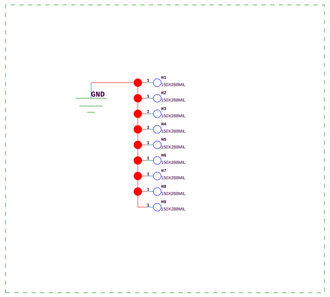
V5 POWER

VIRTEX5 CONFIGURATION

V5 SE GPIO & MISCELLANEOUS

PPC

MECHANICAL



CONTRIBUTORS

ETIENNE BAUERMEISTER
HENRY CHEN
STEVE DURAND
FRANCOIS KAPP
ALAN LANDMAN
GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2	**ROACH_TOP**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-25-2007_12:29 · PATH PATH	DRAWN: F KAPP · APPR: · CHECKED: E BAUERMEISTER · SHEET 1 OF 25

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

TIE TO GROUND IF PLL'S ARE NOT USED

PLACE AT ACTEL 3V3 POWER PINS

PLACE AT ACTEL 1V5 POWER PINS

roach_AFS600_powerpins

roach_AFS600_pcb

roach_AFS600_configpins

PB POWER SWITCH

KEY - REMOVE PIN

MONITOR RESET

XPORT - PLACE IN REAR I/O REGION

ACTEL JTAG CONNECTOR

ROACH/iBOB2	ROACH_MONITOR
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-25-2007_12:29	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 2 OF 25

PSU INPUT SUMMARY (5V)

VOLTAGE	5.0V +- 10%
CURRENT (MAX)	6.0A

PSU RAIL SUMMARY (1V0)

VOLTAGE	1.0V +- 5%
SUPPLIES	FPGA CORE
CURRENT (QUIESCENT)	1.5A
CURRENT (ACTIVE)	26.8A
LOAD STEP	25.3A

PSU INPUT SUMMARY (1V5)

VOLTAGE	12V +- 10%
CURRENT (MAX)	0.8A

PSU RAIL SUMMARY (1V5)

VOLTAGE	1.5V +- 5%
SUPPLIES	FPGA IO, QDR, PPC
CURRENT (QUIESCENT)	0.25A
CURRENT (ACTIVE)	6.8A
LOAD STEP	6.55A

PSU INPUT SUMMARY (1V8)

VOLTAGE	12V +- 10%
CURRENT (MAX)	1.8A

PSU RAIL SUMMARY (1V8)

VOLTAGE	1.8V +- 5%
SUPPLIES	FPGA IO, DDR2 x 2
CURRENT (QUIESCENT)	1A
CURRENT (ACTIVE)	12.9A
LOAD STEP	11.9A

PSU INPUT SUMMARY (2V5)

VOLTAGE	12V +- 10%
CURRENT (MAX)	0.8A

PSU RAIL SUMMARY (2V5)

VOLTAGE	2.5V +- 5%
SUPPLIES	FPGA, ZDOK PPC, PHY
CURRENT (QUIESCENT)	0.1A
CURRENT (ACTIVE)	3.6A
LOAD STEP	3.5A

ROACH/iBOB2

ROACH_PSU

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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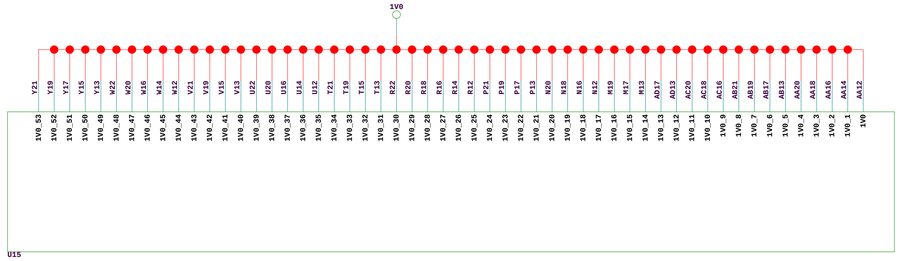
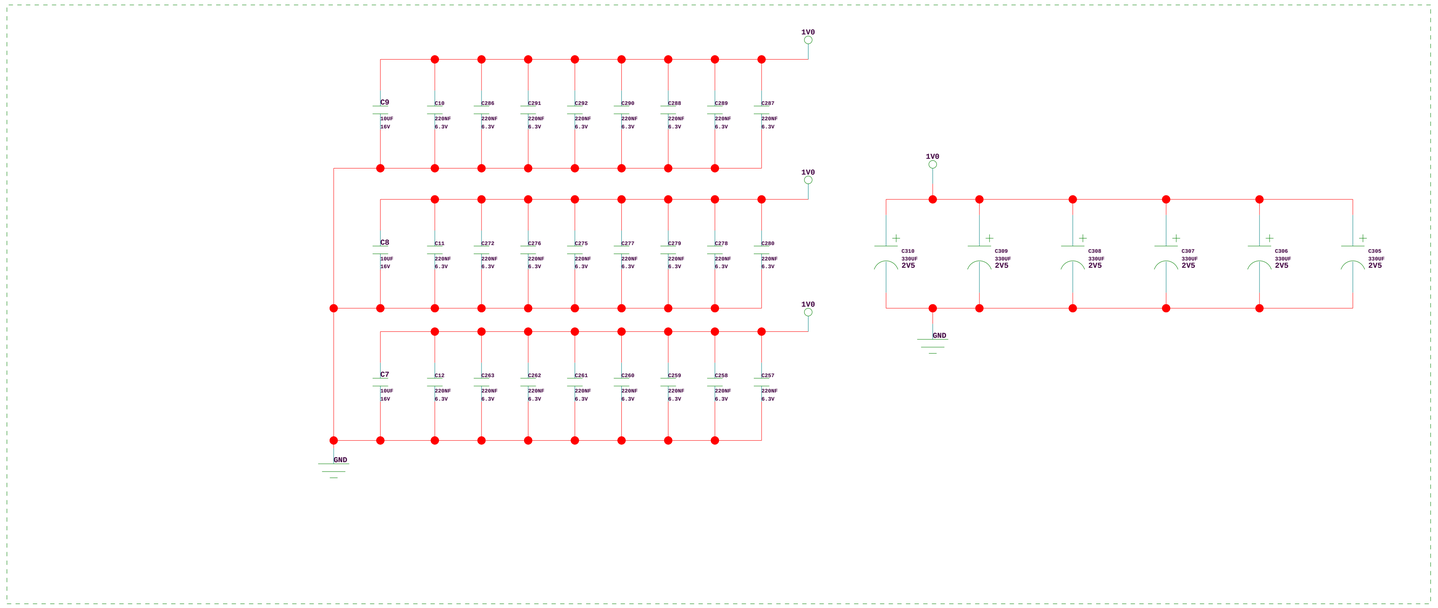
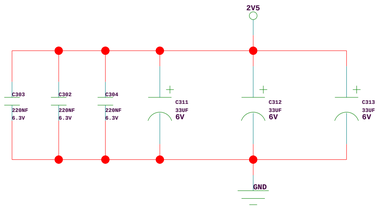
10-25-2007_12:29

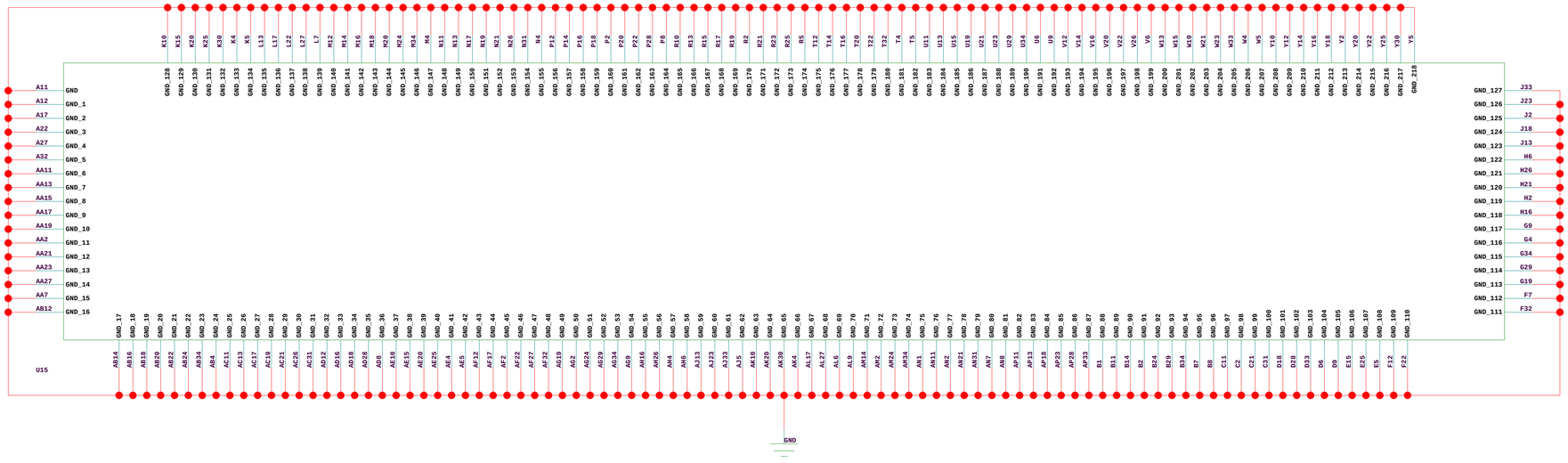
PATH PATH

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	3 OF 25









ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
10-25-2007_12:29 PATH PATH	

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

10-25-2007_12:29

PATH PATH

ROACH_ADC_0

DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 5 OF 25

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
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10-25-2007_12:29

PATH PATH

ROACH_ADC_1

DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET: 6 OF 25

MAIN CLOCK - 100MHZ

CRYSTEK
CCLD-023-25-100.000
100.00MHZ
EPSON TOYOCOM
EG2121CA100.000LHPN

IODELAY CLOCK - 200MHZ

CRYSTEK
CCLD-024-25-200.000
200.00MHZ
EPSON TOYOCOM
EG2121CA200.000LHPN

PLACE CLOSE TO CONNECTORS

POPULATE JUMPER FOR DC COUPLING

POPULATE JUMPER FOR DC COUPLING

ADCMP605BCPZ

ADCMP605BCPZ

BANKS=3

ADR03AUJ-R2

ROACH/iBOB2	ROACH_V5_CLK
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
10-25-2007_12:29 PATH PATH	

ROACH/iBOB2

ROACH_TRANSCEIVERS0_1

COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

10-25-2007_12:29

PATH PATH

SHEET 8 OF 25

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

OPTICAL MODULE FAULT - RED LED

G4 AND G8 CONNECTED IN
ZX2 MODULE

CCLD-023-25-156.250
156.25MHZ

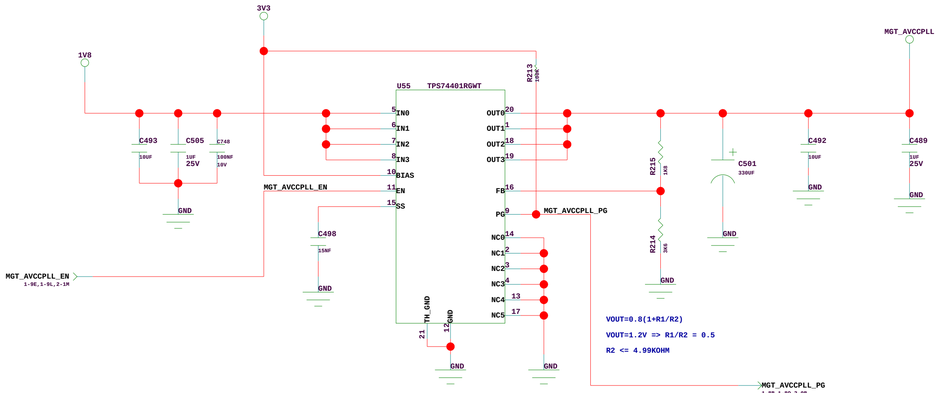
FCN-268F036-G/3DB

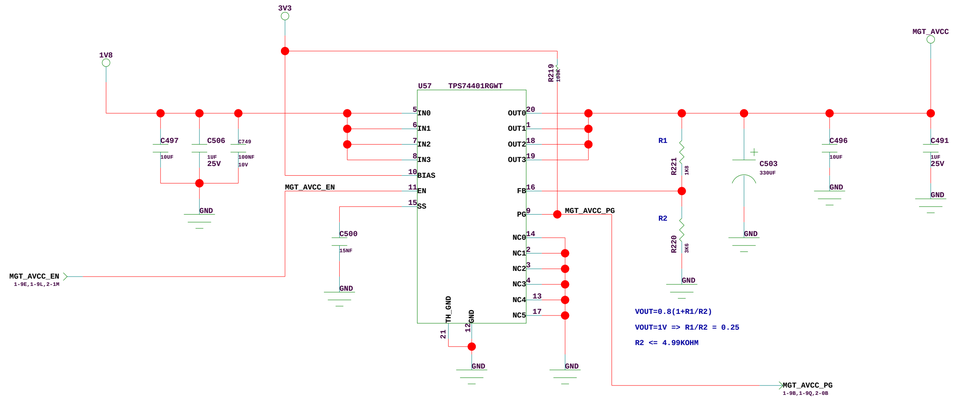
TPS2031D

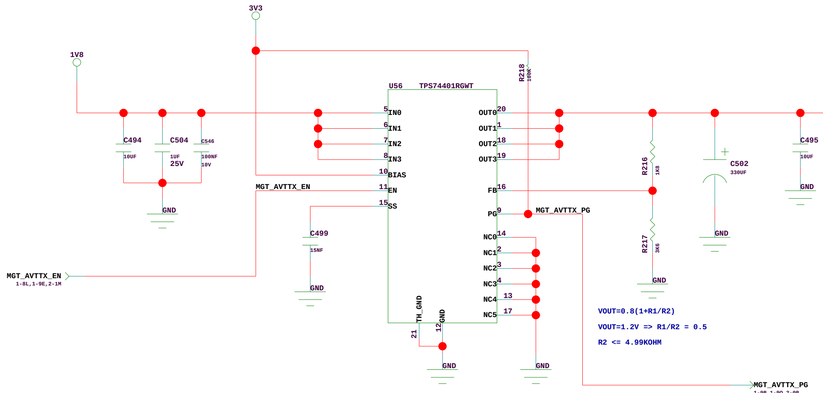
MAX9032AKA

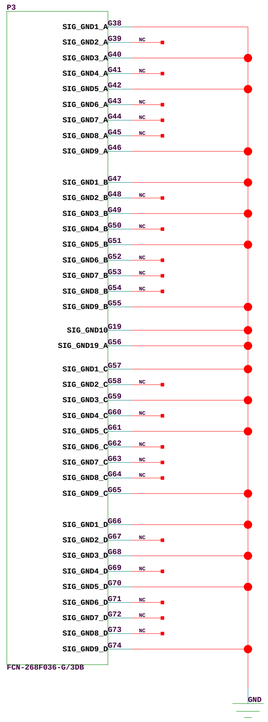
SN74AHC1G08DCKR

ROACH/iBOB2	ROACH_TRANSCEIVERS2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-25-2007_12:29	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 9 OF 25

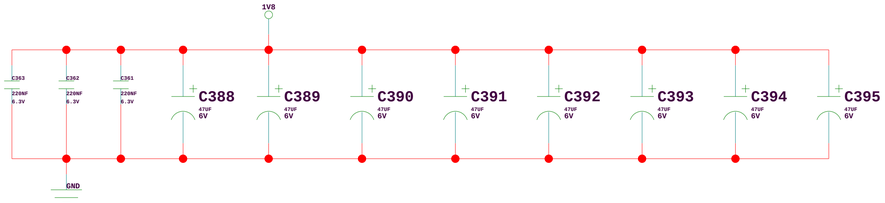


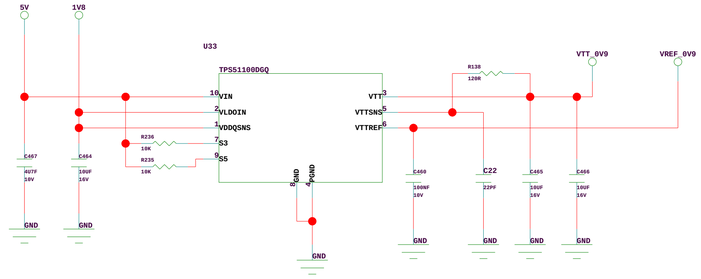


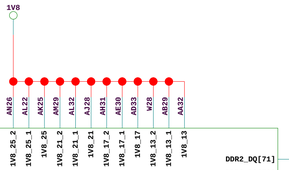


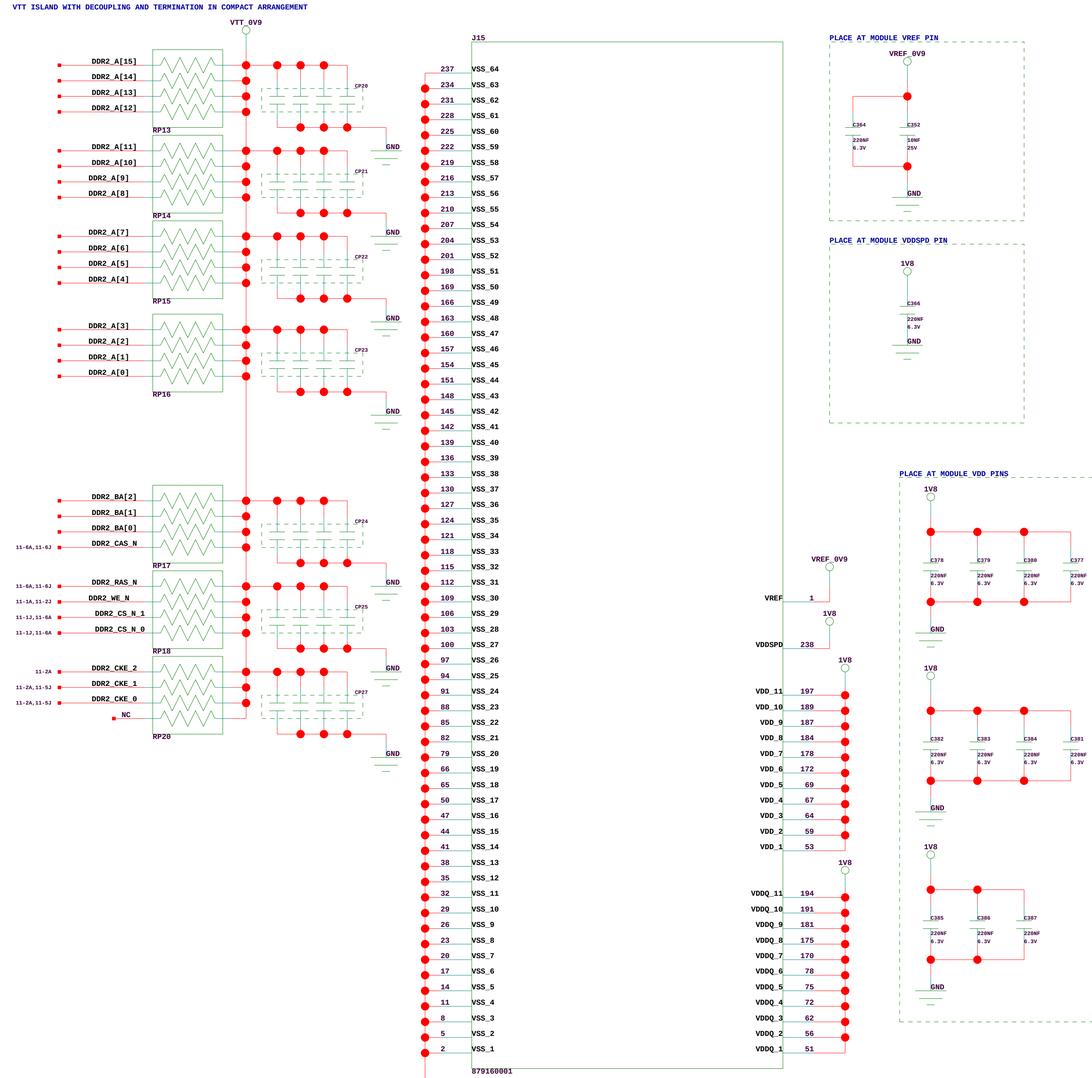


ROACH/iBOB2	ROACH_TRANSCEIVERS_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-25-2007_12:29	DRAWN: F KAPP · APPR:
PATH PATH	CHECKED: E BAUERMEISTER · SHEET 10 OF 25









ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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10-25-2007_12:29

PATH PATH

ROACH_DDR2_DIMM

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

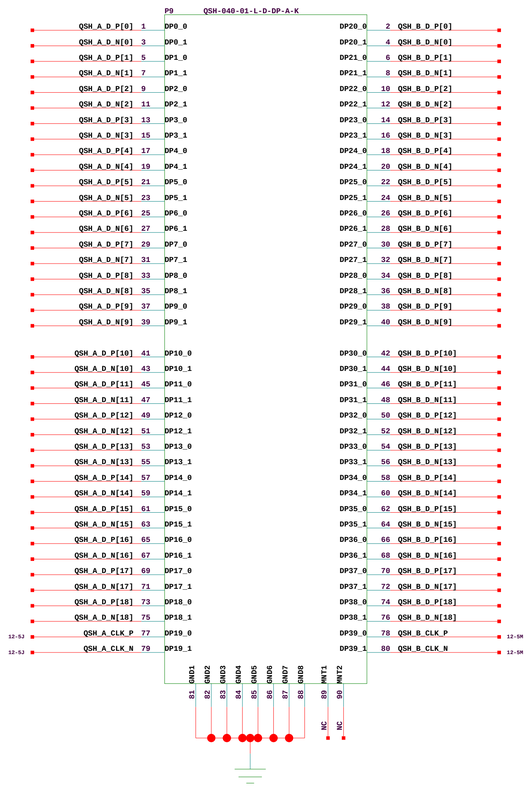
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

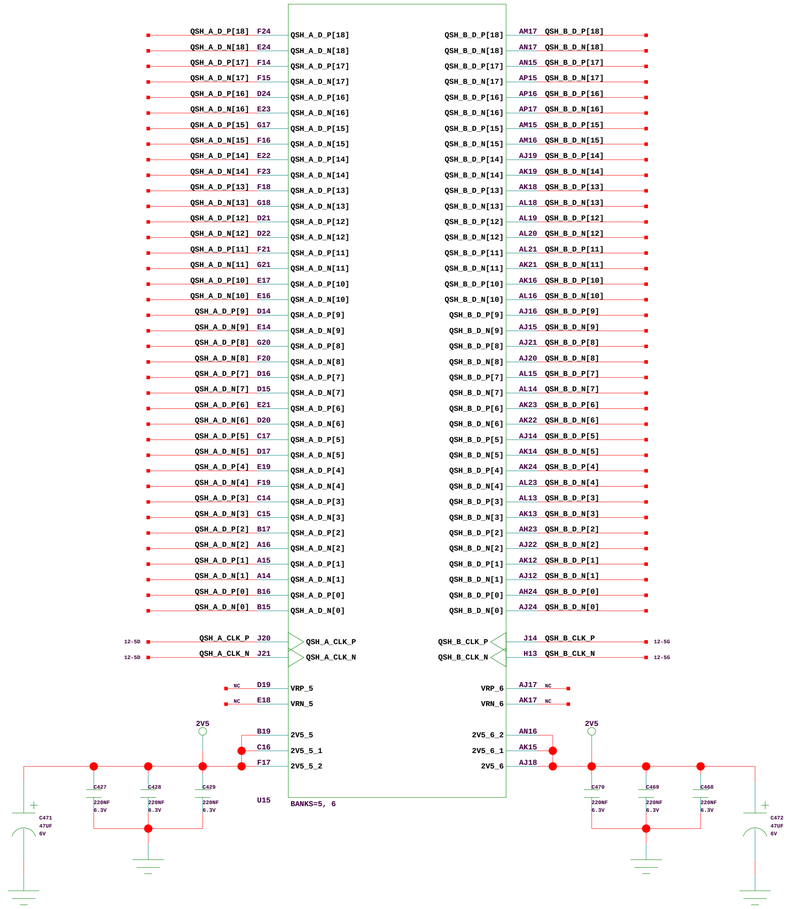
DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 11 OF 25





ROACH/iBOB2

ROACH_DIFF_GPIO

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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PATH PATH

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 12 OF 25

GPIOLVC18[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

GPIOLVC18[20] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

IO VOLTAGE LEVEL SELECT	
1-2: 3.3V	DEFAULT
2-3: 2.5V	

GPIOLVC18[4] IS DUAL FUNCTION:
1. DRIVES LED
2. CONTROLS DIRECTION ON GPIOLVC33[1-4]

IF CR18 IS ON, CLOCK CAPABLE GPIO'S ARE OUTPUTS

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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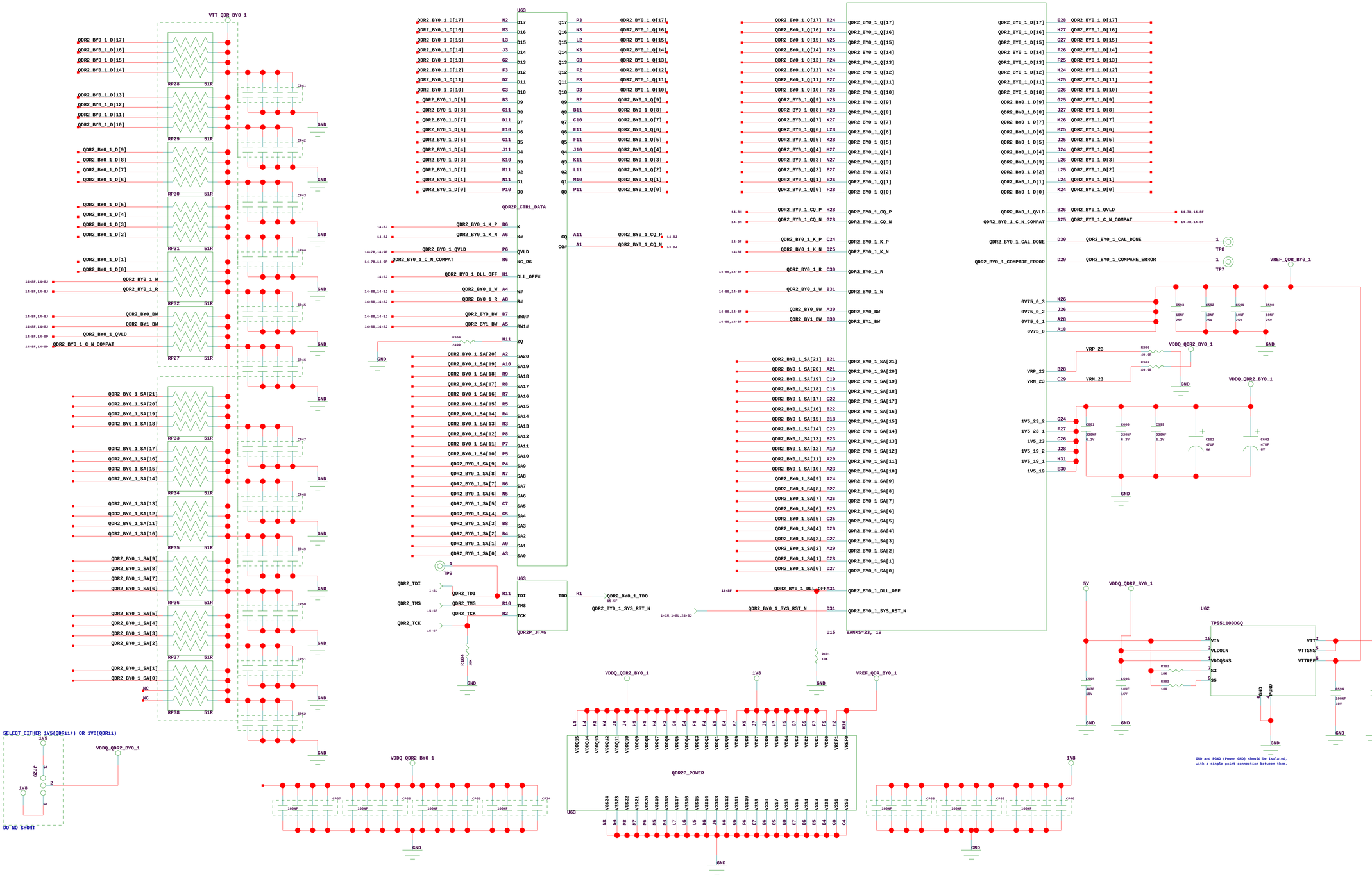
10-25-2007_12:29

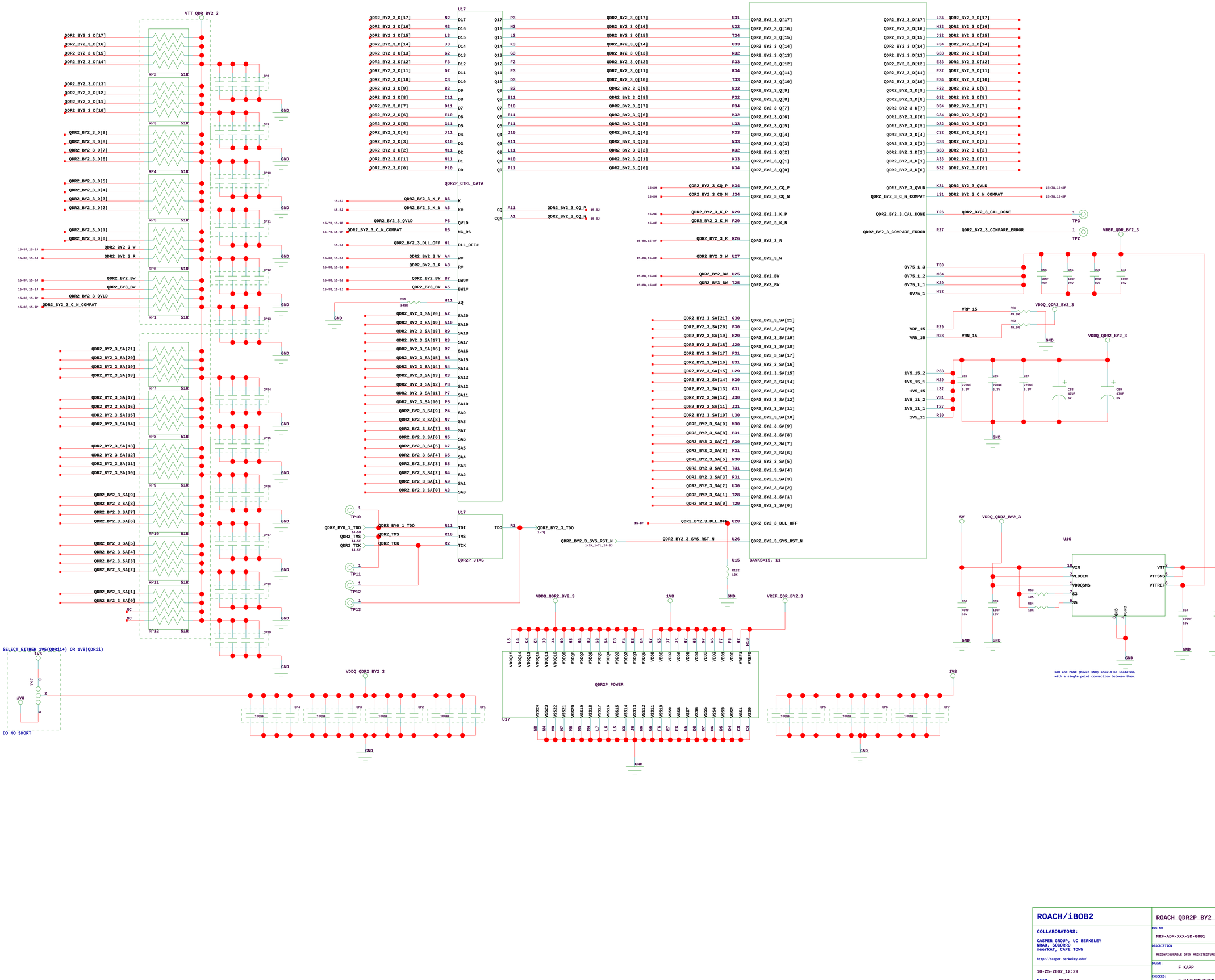
PATH PATH

ROACH_GPIO_MISC

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE MM
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	13 OF 25



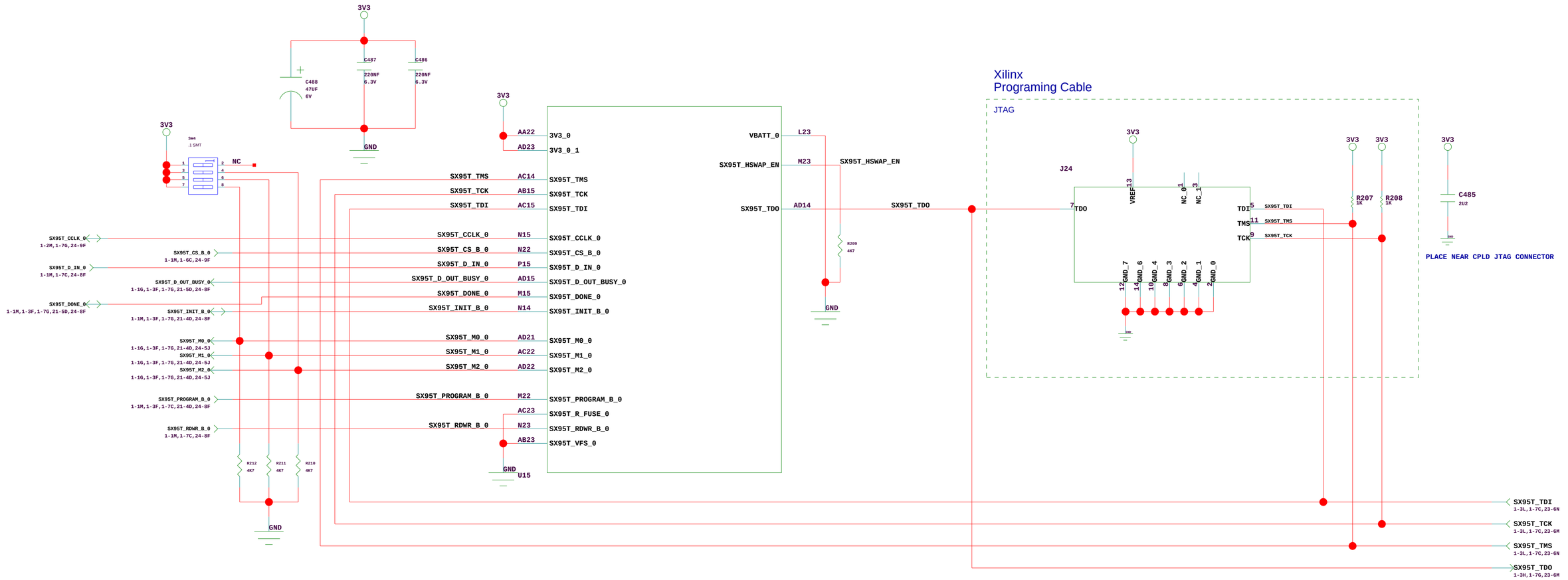
ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
10-25-2007_12:29	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
PATH PATH	DRAWN: F KAPP
	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 14 OF 25



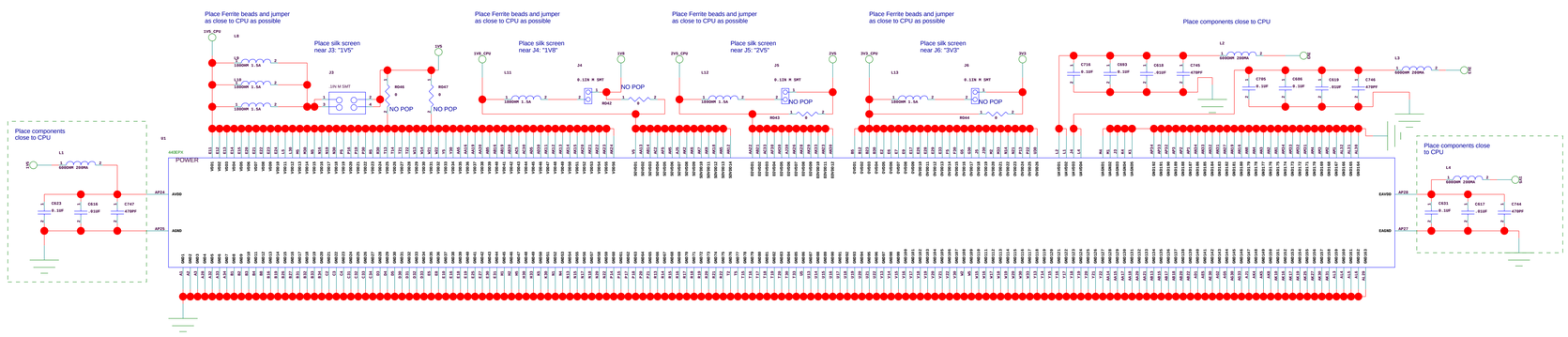
ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET: 15 OF 25
10-25-2007_12:29	
PATH PATH	

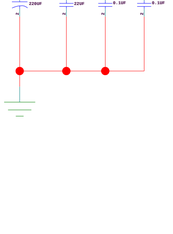
TBD

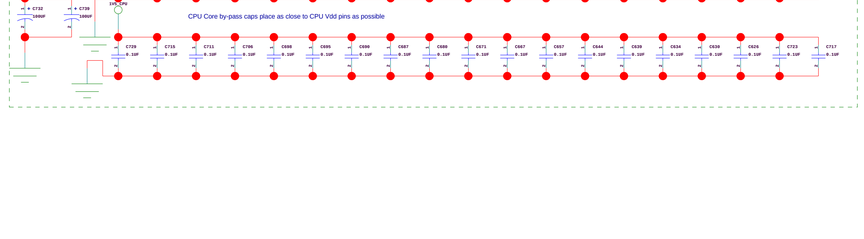
VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

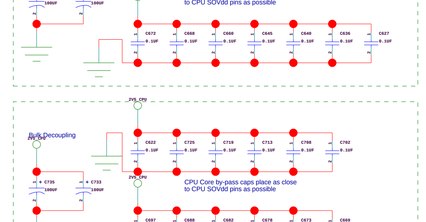


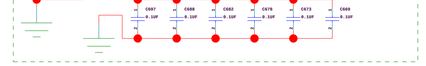
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
10-25-2007_12:29 PATH PATH	

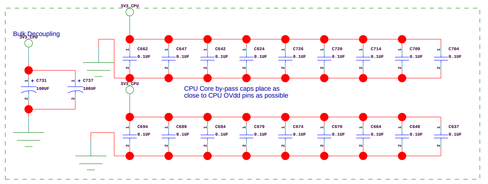


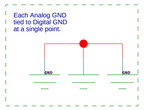










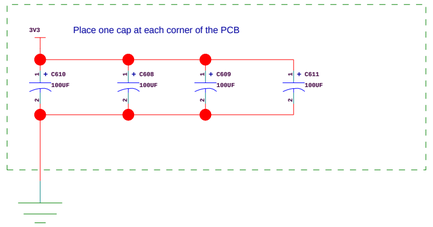


REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: **CASPER GROUP, UC BERKELEY** **NRAO, SOCORRO** **meerKAT, CAPE TOWN** http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 17 OF 25
10-25-2007_12:29 PATH PATH	

REMOVED 3V3 GENERATION



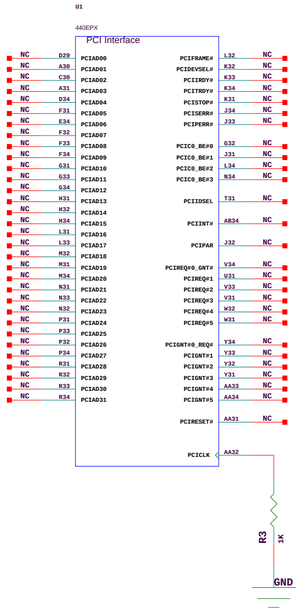
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET 18 OF 25
10-25-2007_12:29 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-25-2007_12:29 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

ROACH/iBOB2

ROACH_PPC_ETH1

COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

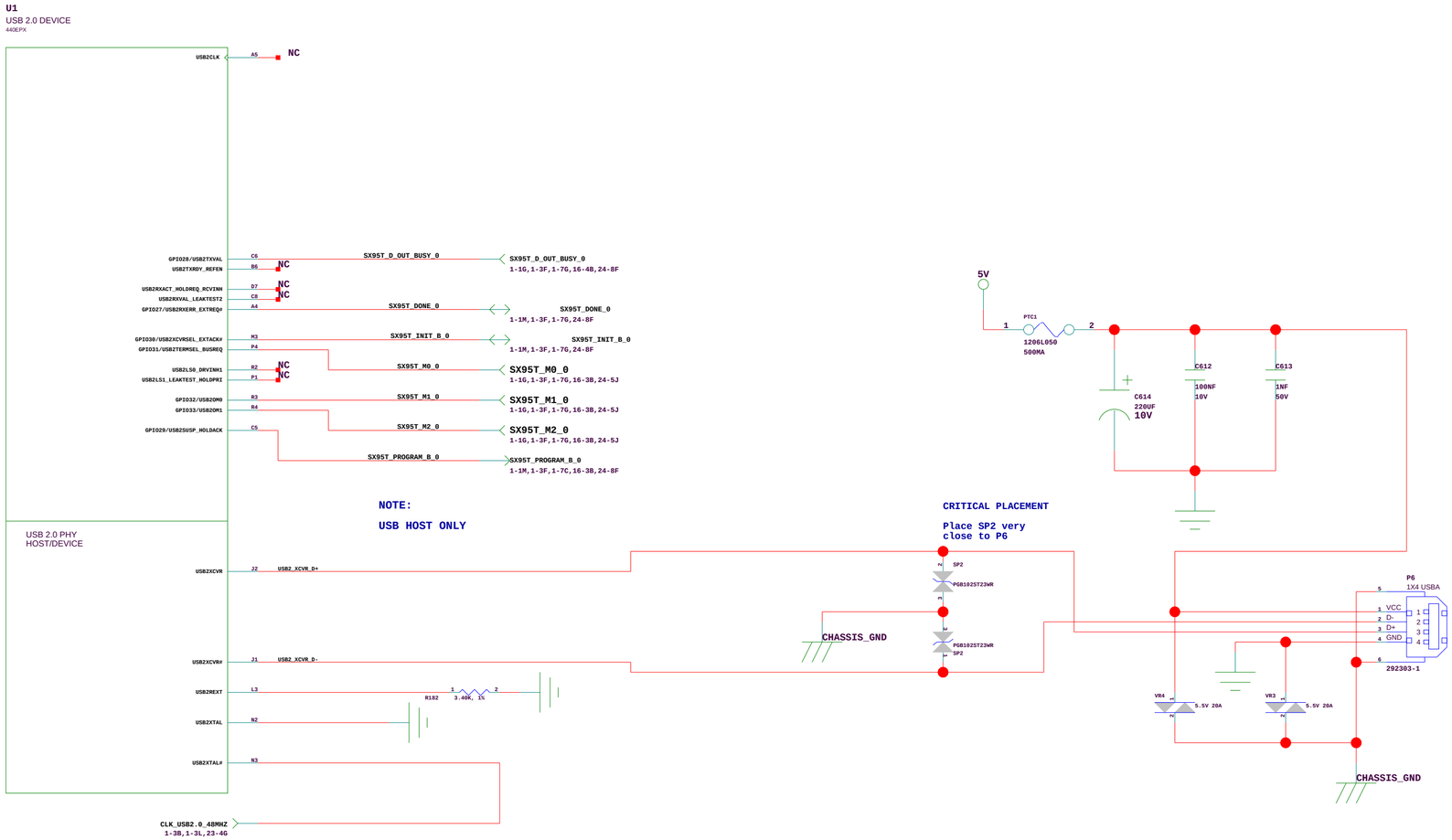
CHECKED: E BAUERMEISTER

APPR:

10-25-2007_12:29

PATH PATH

SHEET 20 OF 25



ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25
10-25-2007_12:29 PATH PATH	

DDR_PA[15:0]

DDR_PD0[63:0]

U1

DDR SDRAM

64DEPX

DDR_PD0	MEMDATA00	MEMADDR00	DDR_PA0
DDR_PD1	MEMDATA01	MEMADDR01	DDR_PA1
DDR_PD2	MEMDATA02	MEMADDR02	DDR_PA2
DDR_PD3	MEMDATA03	MEMADDR03	DDR_PA3
DDR_PD4	MEMDATA04	MEMADDR04	DDR_PA4
DDR_PD5	MEMDATA05	MEMADDR05	DDR_PA5
DDR_PD6	MEMDATA06	MEMADDR06	DDR_PA6
DDR_PD7	MEMDATA07	MEMADDR07	DDR_PA7
DDR_PD8	MEMDATA08	MEMADDR08	DDR_PA8
DDR_PD9	MEMDATA09	MEMADDR09	DDR_PA9
DDR_PD10	MEMDATA10	MEMADDR10	DDR_PA10
DDR_PD11	MEMDATA11	MEMADDR11	DDR_PA11
DDR_PD12	MEMDATA12	MEMADDR12	DDR_PA12
DDR_PD13	MEMDATA13	MEMADDR13	DDR_PA13
DDR_PD14	MEMDATA14		
DDR_PD15	MEMDATA15	BA0	DDR_PBA0
DDR_PD16	MEMDATA16	BA1	DDR_PBA1
DDR_PD17	MEMDATA17	BA2	DDR_PBA2
DDR_PD18	MEMDATA18		
DDR_PD19	MEMDATA19	RAS#	DDR_PRAS#
DDR_PD20	MEMDATA20	CAS#	DDR_PCAS#
DDR_PD21	MEMDATA21	WE#	DDR_PWE#
DDR_PD22	MEMDATA22		
DDR_PD23	MEMDATA23	DM0	DDR_PDM0
DDR_PD24	MEMDATA24	DM1	DDR_PDM1
DDR_PD25	MEMDATA25	DM2	DDR_PDM2
DDR_PD26	MEMDATA26	DM3	DDR_PDM3
DDR_PD27	MEMDATA27	DM4	DDR_PDM4
DDR_PD28	MEMDATA28	DM5	DDR_PDM5
DDR_PD29	MEMDATA29	DM6	DDR_PDM6
DDR_PD30	MEMDATA30	DM7	DDR_PDM7
DDR_PD31	MEMDATA31	DM8	DDR_PDM8
DDR_PD32	MEMDATA32		
DDR_PD33	MEMDATA33	DQS0	DDR_PDQS0
DDR_PD34	MEMDATA34	DQS1	DDR_PDQS1
DDR_PD35	MEMDATA35	DQS2	DDR_PDQS2
DDR_PD36	MEMDATA36	DQS3	DDR_PDQS3
DDR_PD37	MEMDATA37	DQS4	DDR_PDQS4
DDR_PD38	MEMDATA38	DQS5	DDR_PDQS5
DDR_PD39	MEMDATA39	DQS6	DDR_PDQS6
DDR_PD40	MEMDATA40	DQS7	DDR_PDQS7
DDR_PD41	MEMDATA41	DQS8	DDR_PDQS8
DDR_PD42	MEMDATA42		
DDR_PD43	MEMDATA43	MEMODT0	DDR_PODT0
DDR_PD44	MEMDATA44	MEMODT1	DDR_PODT1
DDR_PD45	MEMDATA45		
DDR_PD46	MEMDATA46	BANKSEL#0	DDR_PCS0#
DDR_PD47	MEMDATA47	BANKSEL#1	DDR_PCS1#
DDR_PD48	MEMDATA48		
DDR_PD49	MEMDATA49	MEMCLKEN	DDR_PCKE
DDR_PD50	MEMDATA50		
DDR_PD51	MEMDATA51	MEMCLKOUT	DDR_CLKOUT
DDR_PD52	MEMDATA52		
DDR_PD53	MEMDATA53	MEMCLKOUT#	DDR_CLKOUT#
DDR_PD54	MEMDATA54		
DDR_PD55	MEMDATA55		
DDR_PD56	MEMDATA56		
DDR_PD57	MEMDATA57		
DDR_PD58	MEMDATA58		
DDR_PD59	MEMDATA59		
DDR_PD60	MEMDATA60		
DDR_PD61	MEMDATA61		
DDR_PD62	MEMDATA62		
DDR_PD63	MEMDATA63		

ECC0	SVREF1A	PPC_ECC0
ECC1	SVREF1B	PPC_ECC1
ECC2	SVREF2A	PPC_ECC2
ECC3	SVREF2B	PPC_ECC3
ECC4		PPC_ECC4
ECC5		PPC_ECC5
ECC6		PPC_ECC6
ECC7		PPC_ECC7

22-9F, 22-9F, 22-9F, 22-10F, 22-10F, 22-10F, 22-10F, 22-10F

DDR_CLKOUT

DDR_CLKOUT#

R813 1 2 500ps Loop

DDR_VREF_0V9

1V8

Place parts as close to CPU as possible

C158 0.10F

C148 0.10F

C151 0.10F 0402

C152 0.10F 0402

C148 0.01F

5V

1V8

U32

TPS51100DGQ

VIN	10	5V, 1V8
VLDOIN	2	1V8
VDDQSNS	1	DDR_VREF_0V9
S3	7	DDR_VTT
S5	9	DDR_VTT
VTT	3	DDR_VTT
VTTSNS	5	DDR_VTT
VTTREF	6	DDR_VREF_0V9
GND	8	GND
PGND	4	GND

R230 10K

R229 10K

R6 120R

C459 .01UF 10V

C456 .10UF 10V

C453 .100NF 10V

C21 22PF

C457 .10UF 10V

C458 .10UF 10V

GND

J8

22-6D	PPC_ECC7	168
22-6D	PPC_ECC6	167
22-7D	PPC_ECC5	162
22-7D	PPC_ECC4	161
22-7D	PPC_ECC3	49
22-7D	PPC_ECC2	48
22-7D	PPC_ECC1	43
22-7D	PPC_ECC0	42
DDR_PDQ63		236
DDR_PDQ62		235
DDR_PDQ61		230
DDR_PDQ60		229
DDR_PDQ59		117
DDR_PDQ58		116
DDR_PDQ57		111
DDR_PDQ56		110
DDR_PDQ55		227
DDR_PDQ54		226
DDR_PDQ53		218
DDR_PDQ52		217
DDR_PDQ51		108
DDR_PDQ50		107
DDR_PDQ49		99
DDR_PDQ48		98
DDR_PDQ47		215
DDR_PDQ46		214
DDR_PDQ45		209
DDR_PDQ44		208
DDR_PDQ43		96
DDR_PDQ42		95
DDR_PDQ41		90
DDR_PDQ40		89
DDR_PDQ39		206
DDR_PDQ38		205
DDR_PDQ37		200
DDR_PDQ36		199
DDR_PDQ35		87
DDR_PDQ34		86
DDR_PDQ33		81
DDR_PDQ32		80
DDR_PDQ31		159
DDR_PDQ30		158
DDR_PDQ29		153
DDR_PDQ28		152
DDR_PDQ27		40
DDR_PDQ26		39
DDR_PDQ25		34
DDR_PDQ24		33
DDR_PDQ23		150
DDR_PDQ22		149
DDR_PDQ21		144
DDR_PDQ20		143
DDR_PDQ19		31
DDR_PDQ18		30
DDR_PDQ17		25
DDR_PDQ16		24
DDR_PDQ15		141
DDR_PDQ14		140
DDR_PDQ13		132
DDR_PDQ12		131
DDR_PDQ11		22
DDR_PDQ10		21
DDR_PDQ9		13
DDR_PDQ8		12
DDR_PDQ7		129
DDR_PDQ6		128
DDR_PDQ5		123
DDR_PDQ4		122
DDR_PDQ3		10
DDR_PDQ2		9
DDR_PDQ1		4
DDR_PDQ0		3
DDR2_DIMM_CB7		
DDR2_DIMM_CB6		
DDR2_DIMM_CB5		
DDR2_DIMM_CB4		
DDR2_DIMM_CB3		
DDR2_DIMM_CB2		
DDR2_DIMM_CB1		
DDR2_DIMM_CB0		
DDR2_DIMM_DQ[63]		
DDR2_DIMM_DQ[62]		
DDR2_DIMM_DQ[61]		
DDR2_DIMM_DQ[60]		
DDR2_DIMM_DQ[59]		
DDR2_DIMM_DQ[58]		
DDR2_DIMM_DQ[57]		
DDR2_DIMM_DQ[56]		
DDR2_DIMM_DQ[55]		
DDR2_DIMM_DQ[54]		
DDR2_DIMM_DQ[53]		
DDR2_DIMM_DQ[52]		
DDR2_DIMM_DQ[51]		
DDR2_DIMM_DQ[50]		
DDR2_DIMM_DQ[49]		
DDR2_DIMM_DQ[48]		
DDR2_DIMM_DQ[47]		
DDR2_DIMM_DQ[46]		
DDR2_DIMM_DQ[45]		
DDR2_DIMM_DQ[44]		
DDR2_DIMM_DQ[43]		
DDR2_DIMM_DQ[42]		
DDR2_DIMM_DQ[41]		
DDR2_DIMM_DQ[40]		
DDR2_DIMM_DQ[39]		
DDR2_DIMM_DQ[38]		
DDR2_DIMM_DQ[37]		
DDR2_DIMM_DQ[36]		
DDR2_DIMM_DQ[35]		
DDR2_DIMM_DQ[34]		
DDR2_DIMM_DQ[33]		
DDR2_DIMM_DQ[32]		
DDR2_DIMM_DQ[31]		
DDR2_DIMM_DQ[30]		
DDR2_DIMM_DQ[29]		
DDR2_DIMM_DQ[28]		
DDR2_DIMM_DQ[27]		
DDR2_DIMM_DQ[26]		
DDR2_DIMM_DQ[25]		
DDR2_DIMM_DQ[24]		
DDR2_DIMM_DQ[23]		
DDR2_DIMM_DQ[22]		
DDR2_DIMM_DQ[21]		
DDR2_DIMM_DQ[20]		
DDR2_DIMM_DQ[19]		
DDR2_DIMM_DQ[18]		
DDR2_DIMM_DQ[17]		
DDR2_DIMM_DQ[16]		
DDR2_DIMM_DQ[15]		
DDR2_DIMM_DQ[14]		
DDR2_DIMM_DQ[13]		
DDR2_DIMM_DQ[12]		
DDR2_DIMM_DQ[11]		
DDR2_DIMM_DQ[10]		
DDR2_DIMM_DQ[9]		
DDR2_DIMM_DQ[8]		
DDR2_DIMM_DQ[7]		
DDR2_DIMM_DQ[6]		
DDR2_DIMM_DQ[5]		
DDR2_DIMM_DQ[4]		
DDR2_DIMM_DQ[3]		
DDR2_DIMM_DQ[2]		
DDR2_DIMM_DQ[1]		
DDR2_DIMM_DQ[0]		
DDR2_DIMM_SA2		101
DDR2_DIMM_SA1		240
DDR2_DIMM_SA0		239
DDR2_DIMM_SCL		120
DDR2_DIMM_SDA		119

879160001

1V8

R228 4K7

R227 4K7

PPC_DDR2_DIMM_SCL

PPC_DDR2_DIMM_SDA

GND

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA1	22-8L,22-9D
DDR2_DIMM_BA[1]	190	DDR_PBA2	22-8L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-8L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	NC	
DDR2_DIMM_CK_N[2]	221	NC	
DDR2_DIMM_CK_P[1]	137	NC	
DDR2_DIMM_CK_N[1]	138	NC	
DDR2_DIMM_CK_P[0]	185	DDR_CLKOUT	
DDR2_DIMM_CK_N[0]	186	DDR_CLKOUT#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-7L,22-8D
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-9D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D
ERR_OUT	55	PPC_DDR2_ERROR	1 TP4
PAR_IN	68	PAR_IN	1 TP5

R226 4K7

PPC_DDR2_RESET_N

1-2B,1-2M,24-5J

C455 .5PF 50V

GND

DDR_VTT

RP24 DDR_PA15 DDR_PA14 DDR_PA13 DDR_PA12

RP23 DDR_PA11 DDR_PA10 DDR_PA9 DDR_PA8

RP22 DDR_PA7 DDR_PA6 DDR_PA5 DDR_PA4

RP21 DDR_PA3 DDR_PA2 DDR_PA1 DDR_PA0

RP25 22-8K,22-9D DDR_PBA1; 22-8K,22-9D DDR_PBA2; 22-8K,22-9D DDR_PBA0; 22-8K,22-9D DDR_PCAS#

RP26 22-7K,22-9D DDR_PRAS#; 22-6K,22-8D DDR_PCKE; 22-3K,22-9D DDR_PWE#; 22-3K,22-8D DDR_PCS0#

RP19 22-3K,22-8D DDR_PCS1#; 22-8D DDR_PODT0; 22-8D DDR_PODT1; NC

CP26 CP28 CP29 CP30 CP32 CP31 CP33

GND

J8

237	VSS_64	
234	VSS_63	
231	VSS_62	
228	VSS_61	
225	VSS_60	
222	VSS_59	
219	VSS_58	
216	VSS_57	
213	VSS_56	
210	VSS_55	
207	VSS_54	
204	VSS_53	
201	VSS_52	
198	VSS_51	
169	VSS_50	
166	VSS_49	
163	VSS_48	
160	VSS_47	
157	VSS_46	
154	VSS_45	
151	VSS_44	
148	VSS_43	
145	VSS_42	
142	VSS_41	
139	VSS_40	
136	VSS_39	
133	VSS_38	
130	VSS_37	
127	VSS_36	
124	VSS_35	
121	VSS_34	
118	VSS_33	
115	VSS_32	
112	VSS_31	
109	VSS_30	
106	VSS_29	
103	VSS_28	
100	VSS_27	
97	VSS_26	
94	VSS_25	
91	VSS_24	
88	VSS_23	
85	VSS_22	
82	VSS_21	
79	VSS_20	
66	VSS_19	
65	VSS_18	
50	VSS_17	
47	VSS_16	
44	VSS_15	
41	VSS_14	
38	VSS_13	
35	VSS_12	
32	VSS_11	
29	VSS_10	
26	VSS_9	
23	VSS_8	
20	VSS_7	
17	VSS_6	
14	VSS_5	
11	VSS_4	
8	VSS_3	
5	VSS_2	
2	VSS_1	

879160001

GND

DDR_VREF_0V9

VREF 1

1V8

VDDSPD 238

1V8

VDD_11	197	
VDD_10	189	
VDD_9	187	
VDD_8	184	
VDD_7	178	
VDD_6	172	
VDD_5	69	
VDD_4	67	
VDD_3	64	
VDD_2	59	
VDD_1	53	

1V8

VDDQ_11	194	
VDDQ_10	191	
VDDQ_9	181	
VDDQ_8	175	
VDDQ_7	170	
VDDQ_6	78	
VDDQ_5	75	
VDDQ_4	72	
VDDQ_3	62	
VDDQ_2	56	
VDDQ_1	51	

DDR_VREF_0V9

1V8

C432 .100NF 10V

C433 .10NF 25V

C454 .100NF 10V

C434 .10NF 25V

C430 .100NF 10V

C443 .10NF 25V

C431 .100NF 10V

C444 .10NF 25V

C436 .100NF 10V

C445 .10NF 25V

C435 .100NF 10V

C446 .10NF 25V

GND

1V8

C438 .100NF 10V

C451 .10NF 25V

C437 .100NF 10V

C452 .10NF 25V

C439 .100NF 10V

C449 .10NF 25V

C440 .100NF 10V

C450 .10NF 25V

C441 .100NF 10V

C448 .10NF 25V

C442 .100NF 10V

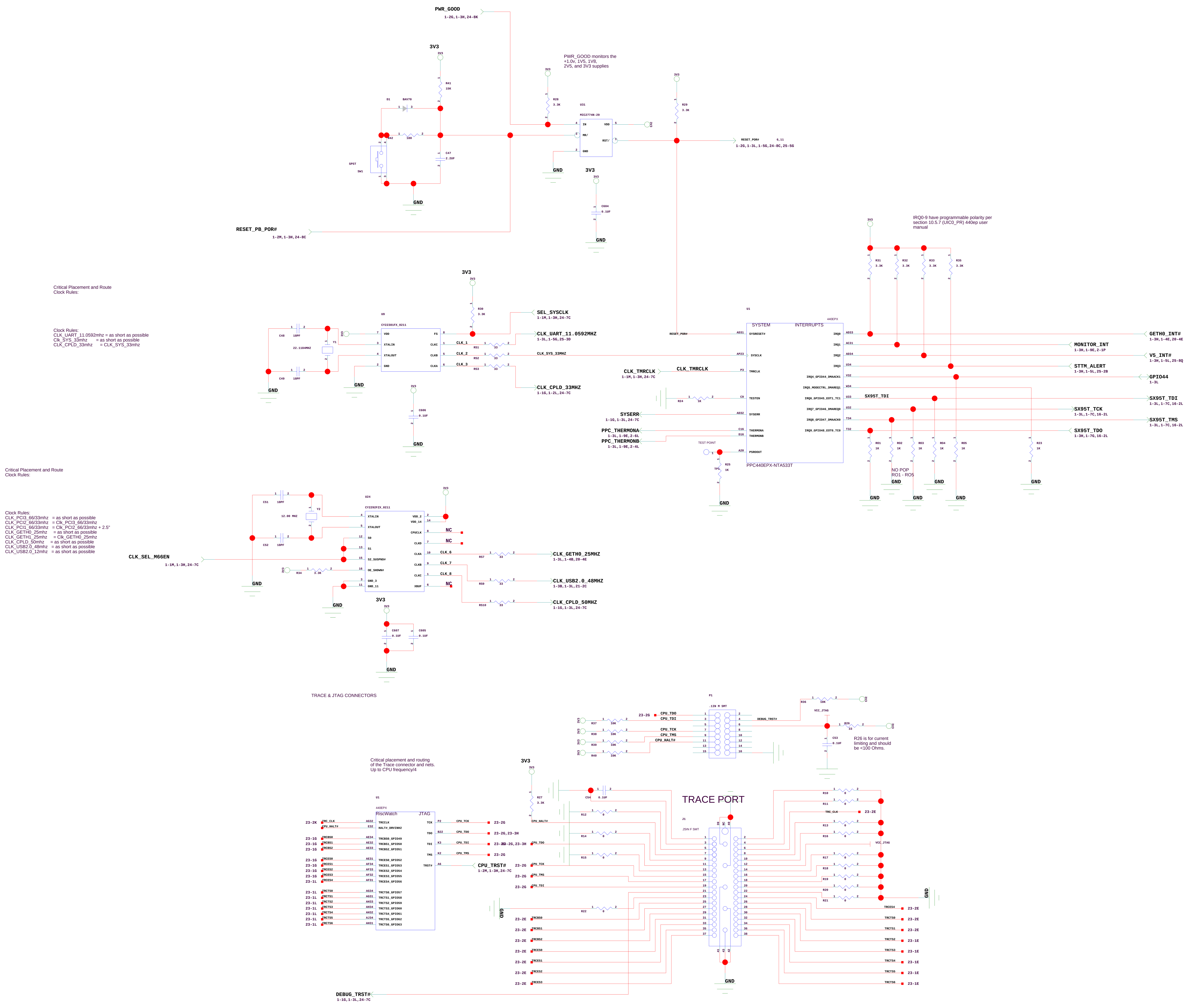
C447 .10NF 25V

GND

PLACE NEAREST DDR2 MODULE PINS

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

ROACH/iBOB2	ROACH_PPC_DDR2
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-25-2007_12:29	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 22 OF 25


PWR_GOOD
PWR_GOOD monitors the +1.0v, 1V5, 1V8, 2V5, and 3V3 supplies
RESET_PB_POR#
RESET_POR#
IRQ0-9 have programmable polarity per section 10.5.7 (UIC0_PR) 440ep user manual
Critical Placement and Route Clock Rules:
Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_SYS_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz
SEL_SYSCLK
CLK_UART_11.0592MHZ
CLK_SYS_33MHZ
CLK_CPLD_33MHZ
CLK_TMRCLK
SYSERR
PPC_THERMONA
PPC_THERMONB
GETH0_INT#
MONITOR_INT
V5_INT#
STTM_ALERT
GPIO44
SX95T_TDI
SX95T_TCK
SX95T_TMS
SX95T_TDO
PPC440EPX-NTA533T
NO POP RO1 - RO5
Critical Placement and Route Clock Rules:
Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible
CLK_SEL_M66EN
CLK_GETH0_25MHZ
CLK_USB2.0_48MHZ
CLK_CPLD_50MHZ
TRACE & JTAG CONNECTORS
R26 is for current limiting and should be <100 Ohms.
Critical placement and routing of the Trace connector and nets. Up to CPU frequency/4
TRACE PORT
RiscWatch
JTAG
CPU_TRST#
DEBUG_TRST#
GND
3V3

ROACH/iBOB2

ROACH_PPC_TST_CLK_IO

COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

10-25-2007_12:29

PATH PATH

SHEET 23 OF 25

Memory Bus

PA0R[27:31]
1-2G,1-4L,25-10B

PA0D27 4 PAD4
PA0D28 7 PAD8
PA0D29 9 PAD10
PA0D30 10 PAD12
PA0D31 11 PAD15

PDATA[0:7]
1-2M,1-4L

PDATA0 12 PAD16
PDATA1 13 PAD17
PDATA2 14 PAD18
PDATA3 15 PAD19
PDATA4 16 PAD20
PDATA5 17 PAD21
PDATA6 18 PAD23
PDATA7 19 PAD28

NC 20 PAD29
NC 21 PAD30
NC 22 PAD31
NC 23 PAD32
NC 24 PAD33
NC 25 PAD34
NC 26 PAD35

28 PAD44

SELECTMAP_CS
1-2G,1-5L,25-7B
PCS_2
1-1G,1-4L,25-7B
PERR
1-1G,1-5L,25-5G,25-7B,25-7M,25-10B
PR_WU
3-1G,3-4L;29-5G,28-6M,@5-7B;@5-9B

30 PAD48
31 PAD49
32 PAD50

RESETS

PWRE_B#
1-2G,1-4L,25-6M,25-7B,25-9B
RESET_PDN#
1-2G,1-3L,1-5G,23-9J,25-5G
RESET_PB_PDN#
1-2M,1-3H,23-8E
PPC_RESET
1-2G,1-9E,2-2R
DEBUG_TRST#
1-1G,1-3L,23-1F
CPU_TRST#

33 PAD52
34 PAD54
35 PAD55
38 PAD59
40 PAD64
41 PAD65

CPU_TRSTN = '1' when
JTAG_TRSTN = '1' and
RESET_PDN# = '1' else '0';
see errata sheet

CLOCKS

1-2M,1-3M,23-2F
CLK_CPLD_33MHZ
1-1G,1-2L,23-6G
CLK_CPLD_50MHZ
1-1G,1-3L,23-4G
CLK_PCICLK
1-1G,1-4L,25-6F
CLK_TMCLK
1-1M,1-3M,23-6H
CLK_SEL_MODE
1-1M,1-3M,23-5D
SEL_SYSCLK

42 PAD66
43 PAD67
44 PAD68
45 PAD69
46 PAD70
48 PAD73

STATUS / MISC

1-1M,1-3N,23-7G
SYSERR
3-1G,3-3L,23-8H

49 PAD74

FLASH

FPF_BSY
1-1G,1-4L,25-7J
FWP#
3-1M,3-4G,25-BJ

50 PAD75
51 PAD76

I2C

EE1_WP
1-2M,1-5L,25-1A
EE2_BOOT_WP
1-2M,1-4G,25-5A
ETTM_A1C
1-2M,1-5G,25-1B

52 PAD77
53 PAD81
54 PAD82
56 PAD86

SYS_CONFIG[0:7]
1-2G,1-9E,2-2R

SYS_CONFIG[0:3]

SYS_CONFIG0 57 PAD87
SYS_CONFIG1 58 PAD88
SYS_CONFIG2 59 PAD89
SYS_CONFIG3 60 PAD90
SYS_CONFIG4 61 PAD95
SYS_CONFIG5 64 PAD100
SYS_CONFIG6 66 PAD102
SYS_CONFIG7 68 PAD105

ETHERNET

GETH0_RST#
1-2M,1-4B,20-4E

NC 69 PAD107
NC 70 PAD108

RESET_CPLD#
1-1M,1-4G,25-3J

71 PAD109
NC 74 PAD112
75 PAD113

PER_CCLK_ENF

U54

roach_cpld_XC2C256_7VQ100C_pcb

XC2C256_7VQ100C

142 PAD217
140 PAD214
139 PAD213
138 PAD212
137 PAD211
136 PAD208
135 PAD207
134 PAD206
133 PAD204
132 PAD199
131 PAD197
130 PAD196
129 PAD195
128 PAD194
126 PAD192
125 PAD191
124 PAD190
121 PAD187
120 PAD186
119 PAD178
118 PAD177
117 PAD176
116 PAD175
115 PAD173
114 PAD171
113 PAD169
112 PAD168
111 PAD167
110 PAD166
107 PAD163
106 PAD162
105 PAD161
104 PAD160
103 PAD158
102 PAD156
101 NC PAD154
100 NC PAD152
98 NC PAD146
97 NC PAD145
96 NC PAD144
95 NC PAD143
94 NC PAD142
92 NC PAD138
91 NC PAD137
88 NC PAD134
87 PAD133
86 PAD132
85 PAD131
83 PAD125
82 NC PAD121
81 NC PAD120
80 NC PAD119
79 NC PAD118
78 PAD117
77 PAD115
76 PAD114

USER_DIP0
USER_DIP1
USER_DIP2
USER_DIP3

R198 10K
R194 10K
R195 10K
R196 10K
SW2
4POLE
User DIP-Swith

CFG_DIP0
CFG_DIP1
CFG_DIP2
M66EN

USER_LED0
USER_LED1
SYSERR#
RESET_BUFPOR#

R200 180
R201 180
R202 180
R203 10K
CR2 GRN
CR3 GRN
CR4 GRN
CR5 RED
CR6 GRN
CR7 RED

SysErr will be used to drive Status LED (active H)

SX95T_CCLK_0
1-2M,1-7G
SX95T_CS_B_0
1-1M,1-9C,16-4B
SX95T_D_IN_0
1-1M,1-7C,16-4A
SX95T_D_OUT_BUSY_0
1-1G,1-3F,1-7G,16-4B,21-5D
SX95T_DONE_0
1-1M,1-3F,1-7G,21-5D
SX95T_INIT_B_0
1-1M,1-3F,1-7G,21-4D
SX95T_PROGRAM_B_0
1-1M,1-3F,1-7C,16-3B,21-4D
SX95T_RDWR_B_0
1-1M,1-7C,16-3B

R197 180
R199 180
CR1 GRN
CR2 GRN
3V_STB
3V3
74LVC1G66
U35
VCC
GND
C615 0.1UF
GND2
PWR_GOOD
1-2G,1-3H,23-10G

CMD/DI
CLK/SCLK

J17

10 CMD/DI
6 CLK/SCLK
7 VDD
8 VSS1
4 VSS2
14 SD_CD_COM
15 SD_WP_COM

GMC050064SEU

DAT0/DO 2 DAT0/DO
DAT1 1 DAT1
DAT2 13 DAT2
DAT3 12 DAT3
DAT4 11 DAT4
DAT5 9 DAT5
DAT6 5 DAT6
DAT7 3 DAT7
MNT1 16 NC
MNT2 17 NC

SD/MMC/MMCPLUS CONNECTOR

QDR2_BY0_1_SYS_RST_N
1-1M,1-8L,14-5J
QDR2_BY2_3_SYS_RST_N
1-2M,1-7L,15-5J
PPC_DDR2_RESET_N
1-2G,1-2M,22-2B
EXT_RESET#
1-2G,1-4L,25-6F

SX95T_M0_0
1-1G,1-3F,1-7G,16-3B,21-4D
SX95T_M1_0
1-1G,1-3F,1-7G,16-3B,21-4D
SX95T_M2_0
1-1G,1-3F,1-7G,16-3B,21-4D

Boot Configuration

R204 10K
R205 10K
R206 10K
SW3
4POLE
Configuration DIP-Swith

1-1G,1-5G,25-3B

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

BOOT_CFG0
1-1M,1-4G,25-1J
BOOT_CFG1
1-1M,1-4G,25-1J
BOOT_CFG2
1-1M,1-4G,25-1J

RD10 10K
RD11 10K
RD14 10K

Xilinx Programing Cable

JTAG

J22

3V3
TDO
VREF
NC_0
NC_1
TDI
TMS
TCK
GND_7
GND_6
GND_4
GND_3
GND_2
GND_1
GND_0
R193 1K
R192 1K

C484 .01UF

PLACE NEAR CPLD JTAG CONNECTOR

U54

roach_cpld_XC2C256_7VQ100C_configpins

XC2C256_7VQ100C

NC 2 PAD1
NC 3 PAD3
NC 5 PAD5
NC 6 PAD7
NC 39 PAD62
63 TDI
65 TMS
67 TCK
122 TDO
NC 143 PAD218

ENABLE PER_CLK CONNECTION TO CONFIGURATION I/F MUST CO-ORDINATE WITH SX95T_CCLK_0 AND MODE TO AVOID CLASH

PER_CCLK_ENF
CLK_PERCLK

SN74AHC1G125DCKT
U2
DE#
A
GND
VCC
Y
SX95T_CCLK_0

R135 10K
C13 100NF 10V

U54

roach_cpld_XC2C256_7VQ100C_powerpins

XC2C256_7VQ100C

VCC 1
VAUX 8
VCCIO_3 27
VCC_1 37
VCCIO_4 55
VCCIO_5 73
VCC_2 84
VCCIO_6 93
VCCIO 109
VCCIO_1 127
VCCIO_2 141

GND_3 29
GND_4 36
GND_5 47
GND_6 62
GND_7 72
GND_8 89
GND_9 99
GND_10 108
GND 123
GND_1 144
GND_2

C473 100NF 10V
C474 100NF 10V
C475 100NF 10V
C476 100NF 10V
C477 100NF 10V
C478 100NF 10V
C479 100NF 10V
C480 100NF 10V
C481 100NF 10V
C482 100NF 10V
C483 100NF 10V

PLACE NEAR CPLD POWER PINS

ROACH/iBOB2	**ROACH_PPC_CPLD**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 24 OF 25
10-25-2007_12:29 PATH PATH	

PDATA[0:31]
PADD[2:31]
PADD30 IS THE LSB FOR 16 BIT WIDE BUS TRANSFERS
NOTE: DMA SIGNALS IN GREEN TEXT
PADD2 IS THE MSB
External Slave Peripheral
External Master Peripheral Interface
FLASH 32Mx16 /64Mx8
EPB RESET OUTPUT
EXT_RESET#
CLK_PERCLK
RESET_POR#
U15
BANKS=1, 2, 4
CHIP SELECT 1
3V3
GND
NO POP
AT24C64N-10SU-1.8
UART
IIC0
IIC1_SPI
NAND Flash Interface
NOT USED
UART Port 0
UART Port 1
J14
HLE-105-02-G-DV
STTM_ALERT
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
ROACH_PPC_NVM_SERIAL
DOC NO
NRF-ADM-XXX-SD-0001
REVISION
A
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
CHECKED: E BAUERMEISTER
10-25-2007_12:29
PATH PATH
SHEET 25 OF 25