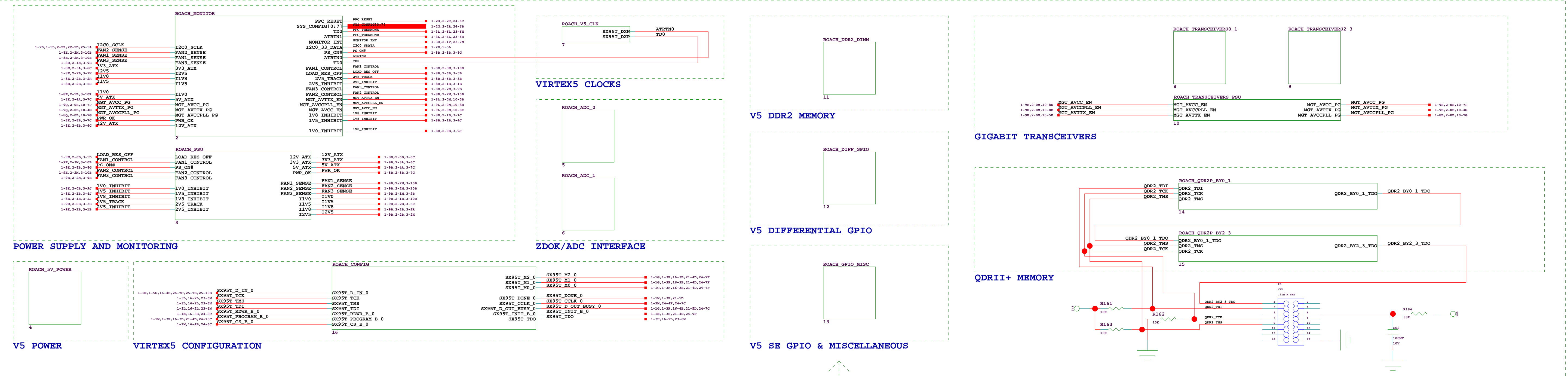
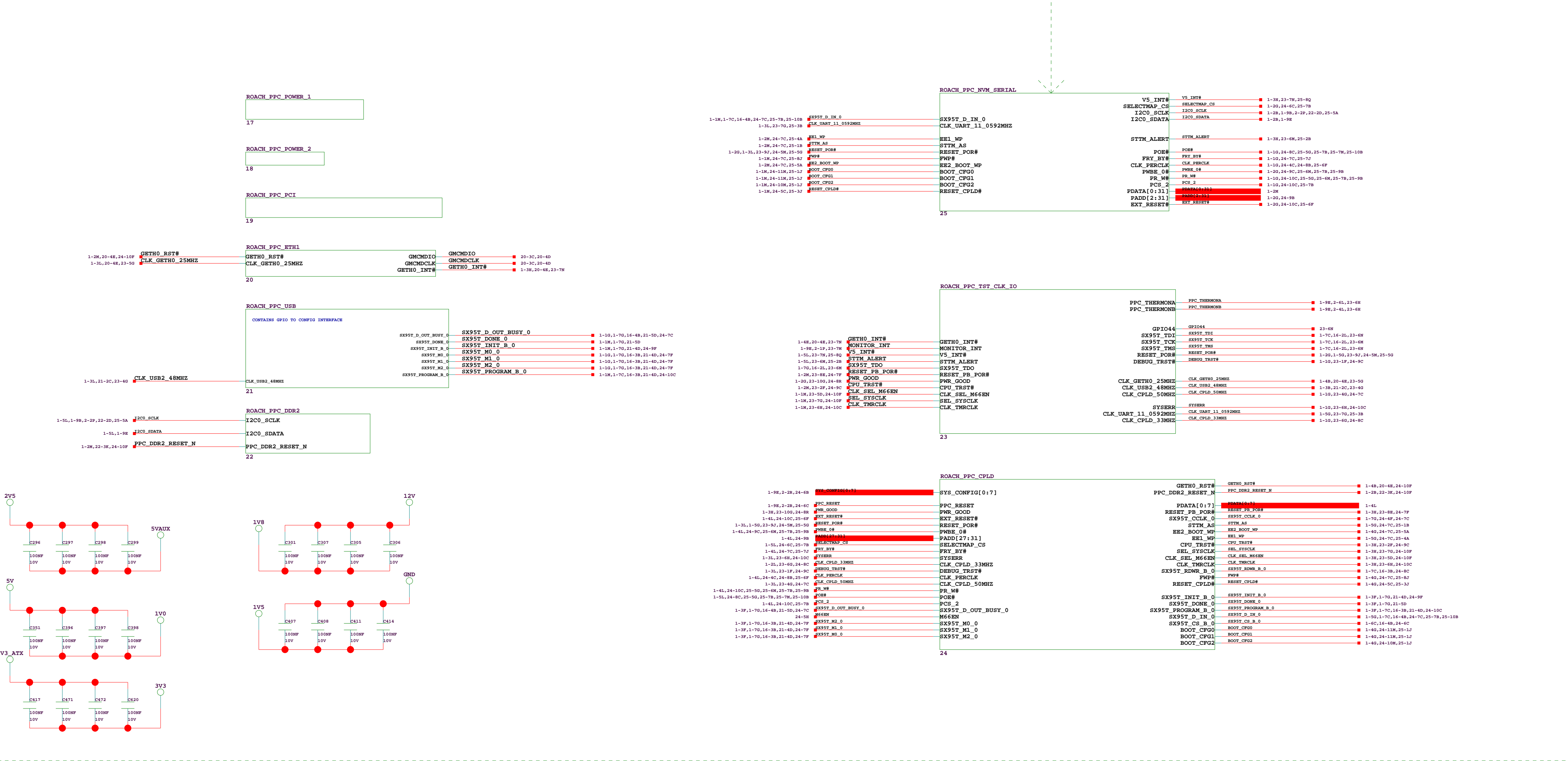


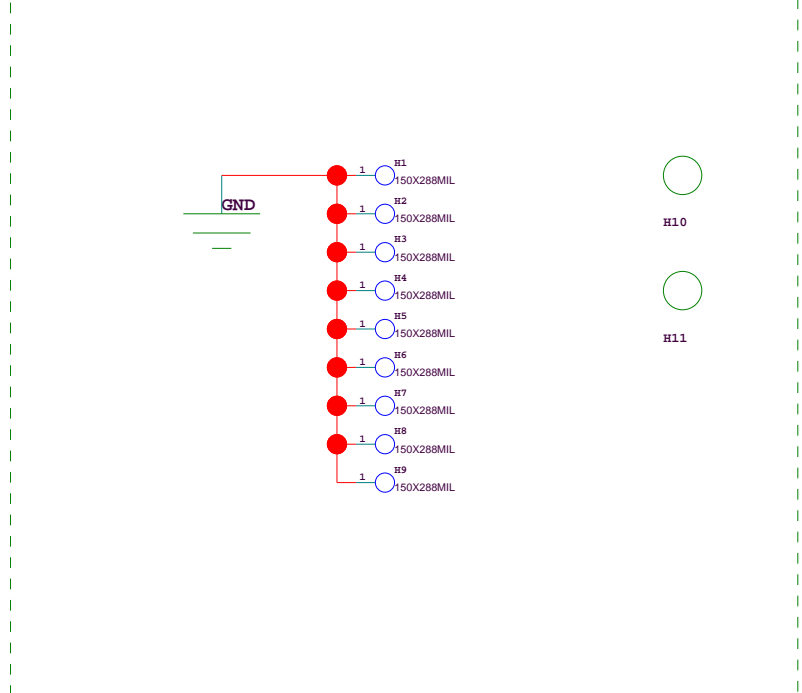
VIRTEX5



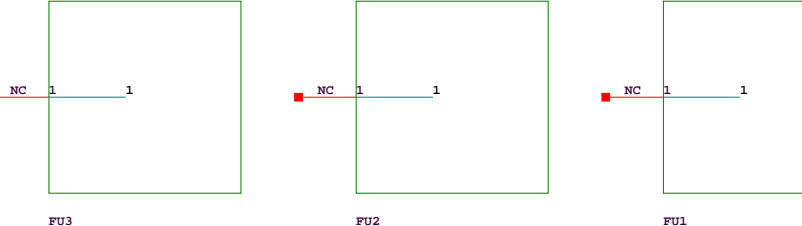
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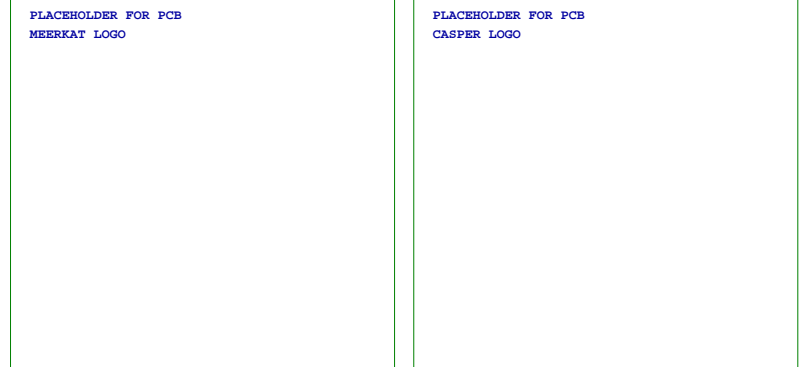
MECHANICAL



BOARD FIDUCIALS



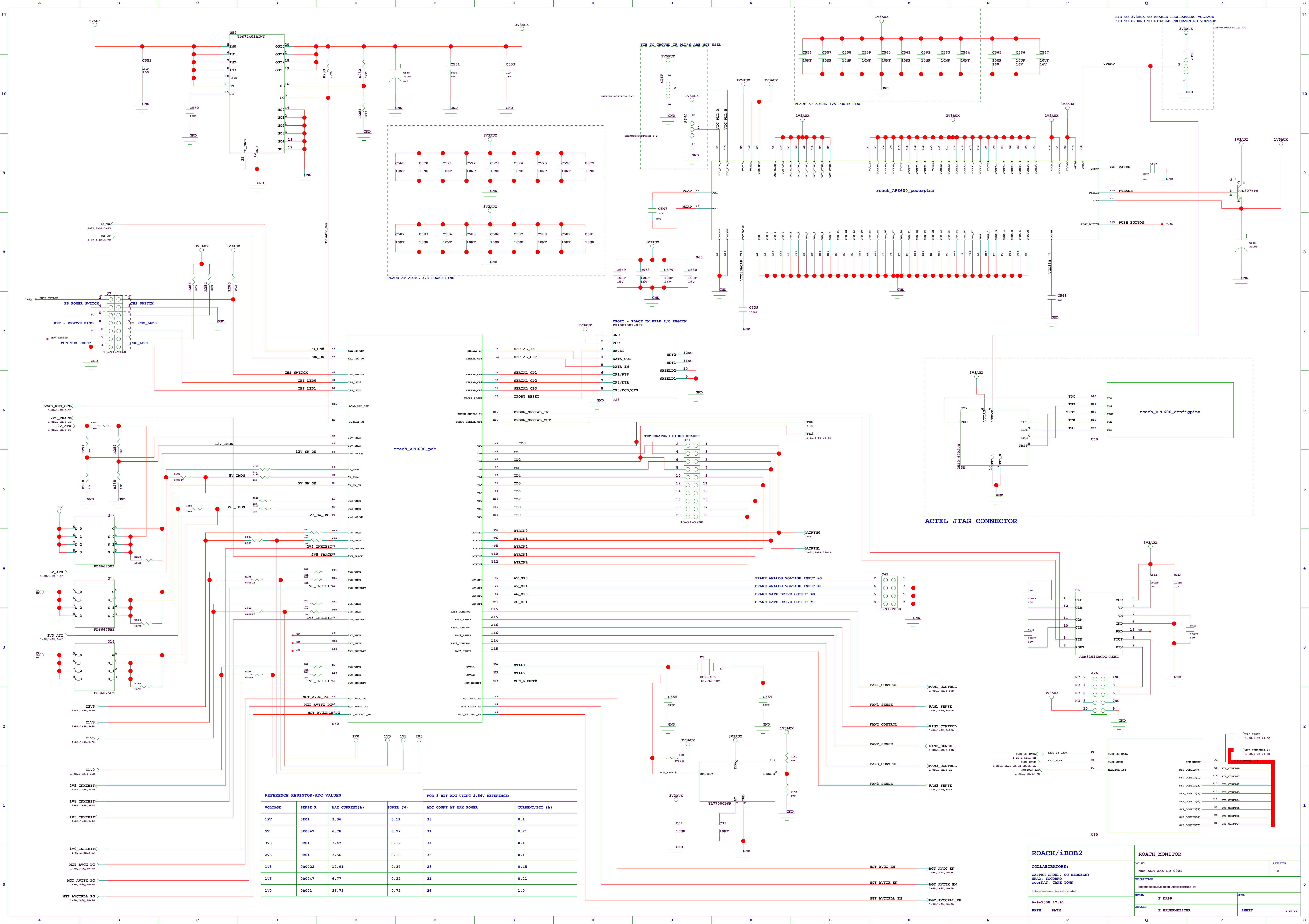
LOGO'S



CONTRIBUTORS

STEVEN BAUMGARTNER
FRANCIS KAPP
ALAN LAMANN
GORDON PECK
MIKE RYAN
DAN NEUBERGER

ROACH/iBOB2		ROACH_TOP	
COLLABORATORS:		DOC NO	REVISION
CASPER GROUP, UC BERKELEY		NRF-ADM-XXX-SD-0001	A
DESCRIPTION		RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN:		DATE:	APPROVED:
6-4-2008 17:41		F KAPP	
PATH		R BAUMGARTNER	
		SHEET	
		1 OF 25	



REFERENCE RESISTOR/ADC VALUES				FOR 8 BIT ADC USING 2.56V REFERENCE:	
VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)	ADC COUNT AT MAX POWER	CURRENT/BIT (A)
12V	0R01	3.36	0.11	33	0.1
5V	0R0047	6.78	0.22	31	0.21
3V3	0R01	3.47	0.12	34	0.1
2V5	0R01	3.56	0.13	35	0.1
1V8	0R0022	12.91	0.37	28	0.45
1V5	0R0047	6.77	0.22	31	0.21
1V0	0R001	26.79	0.72	26	1.0

ROACH/iBOE2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCCORRO
BaeKAT, CAPE TOWN
<http://casper.berkeley.edu/>

6-4-2008_17:41

PATH

PATH

ROACH_MONITOR

DOC NO

NRF-ADM-XXX-SD-0001

DESCRIPTION

RECONFIGURABLE OPEN ARCHITECTURE HW

6-4-2008_17:41

6-4-2008_17:41

REVISION

A

DESIGNER

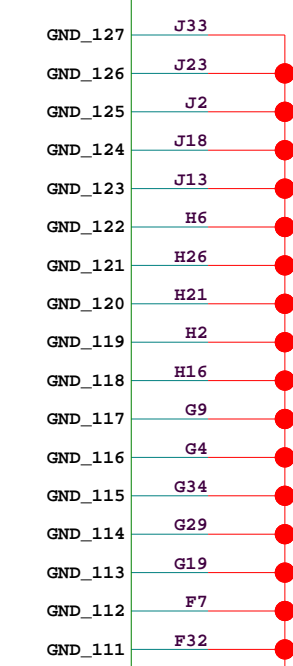
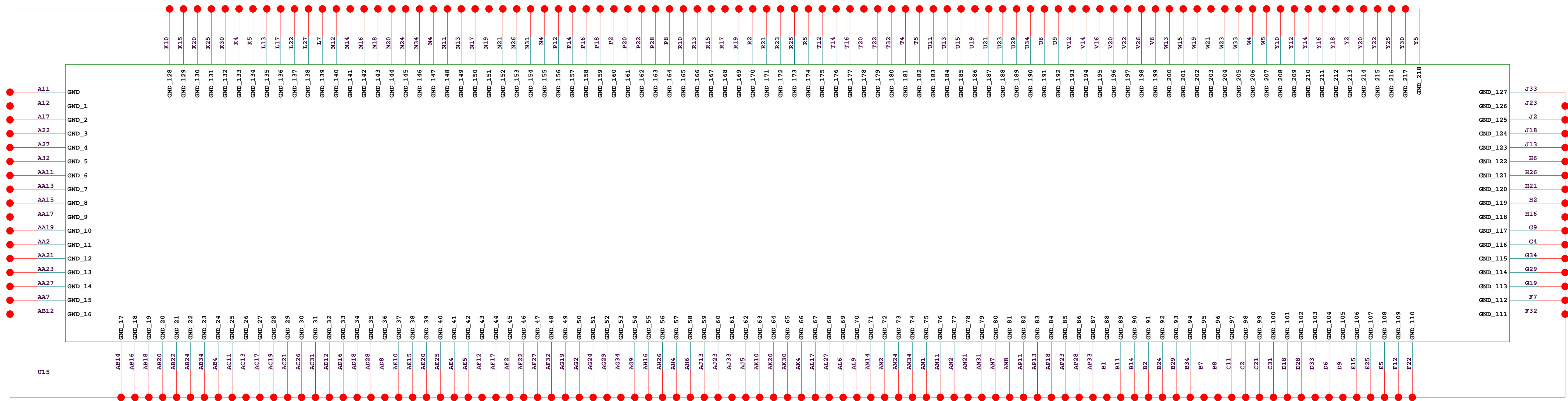
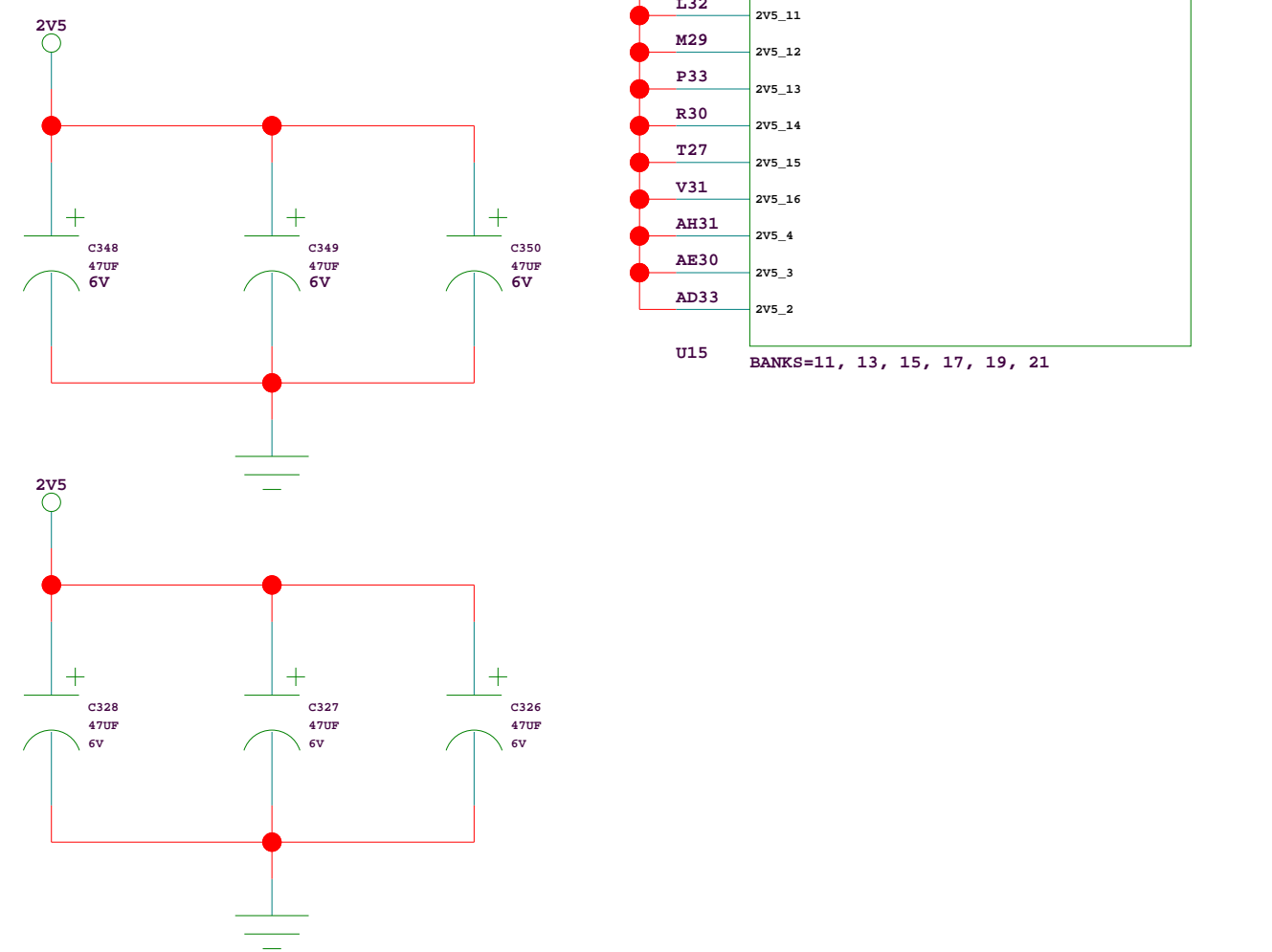
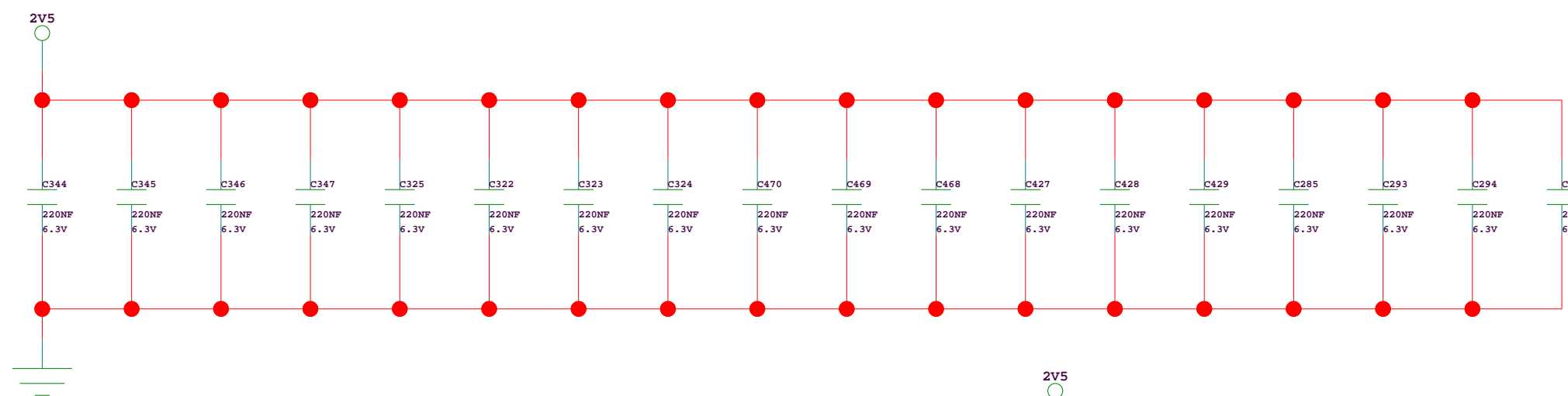
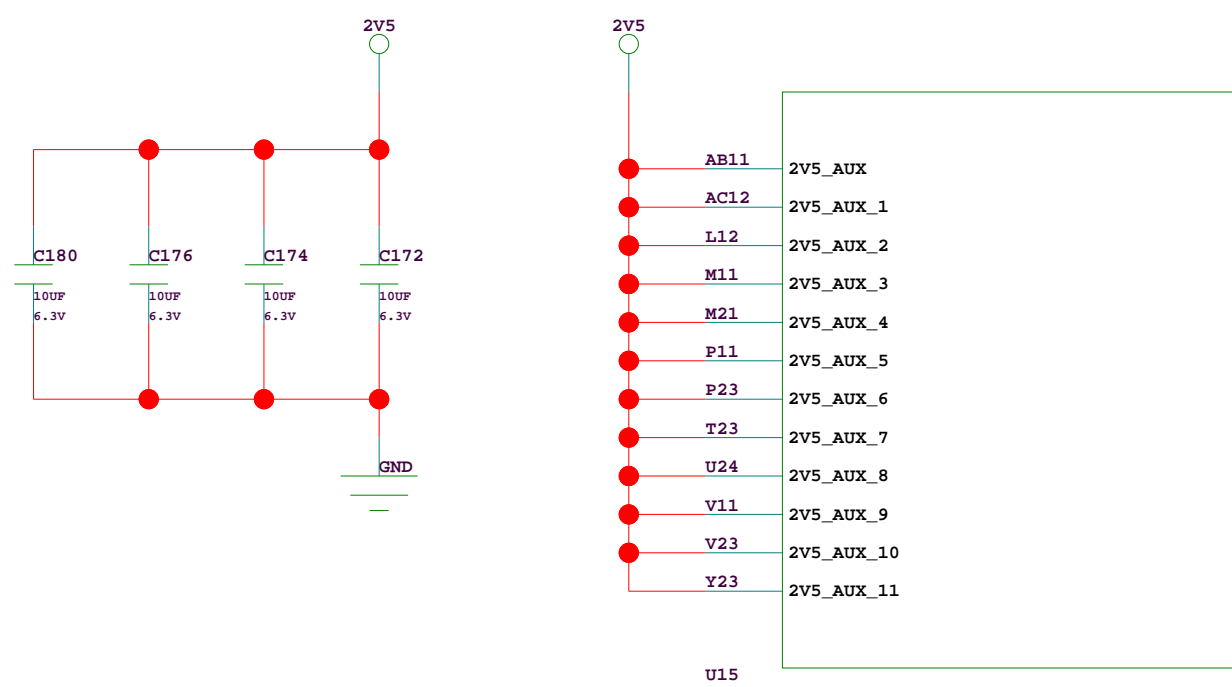
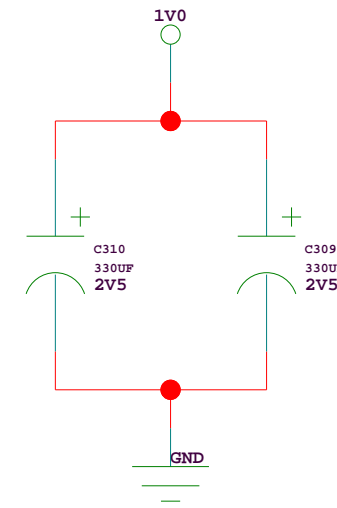
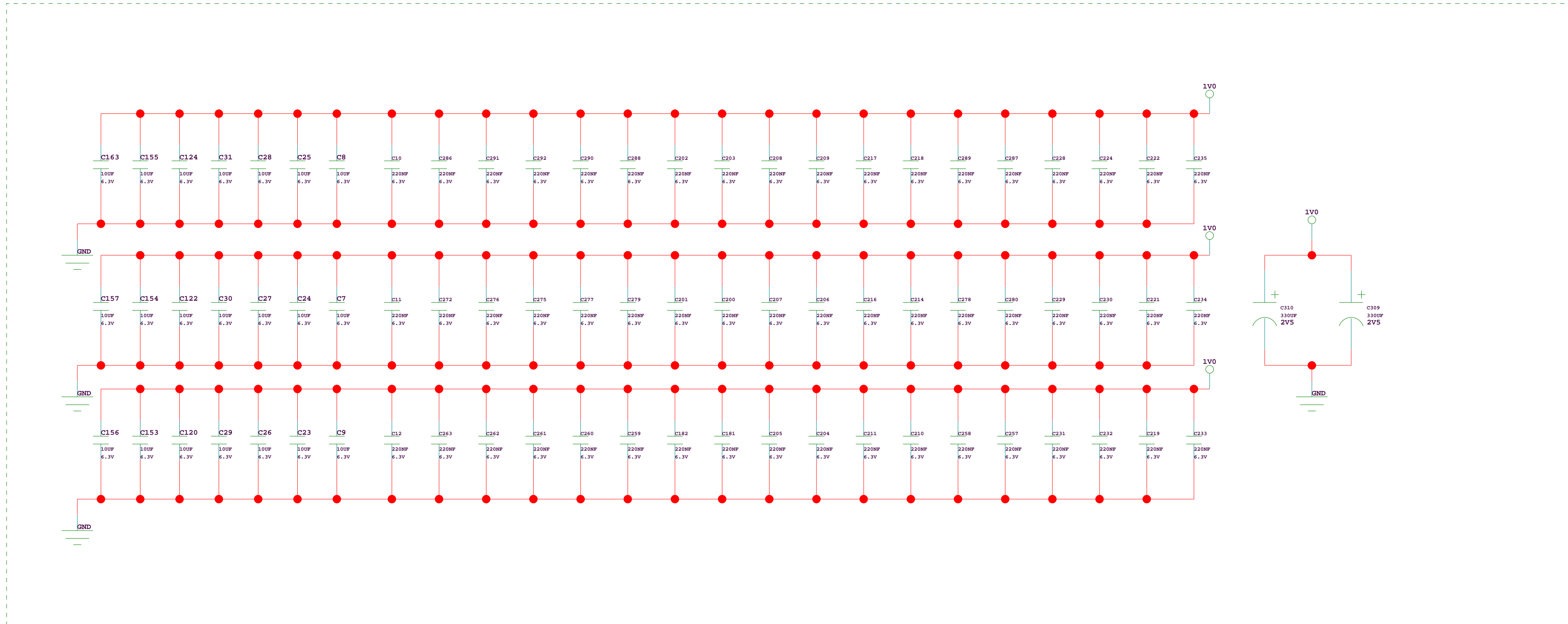
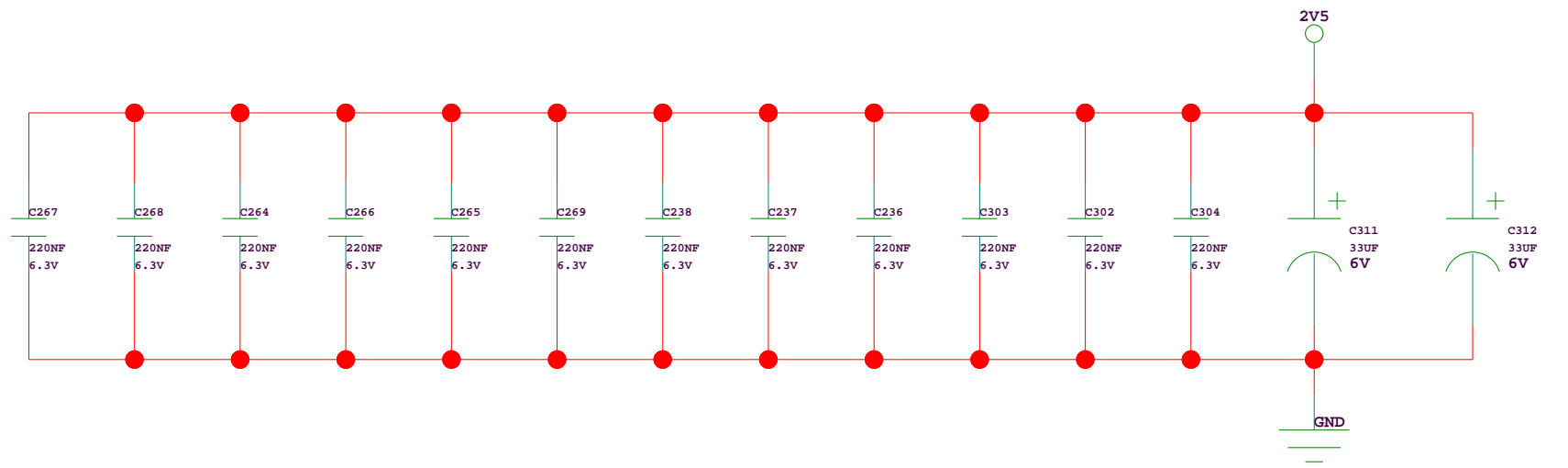
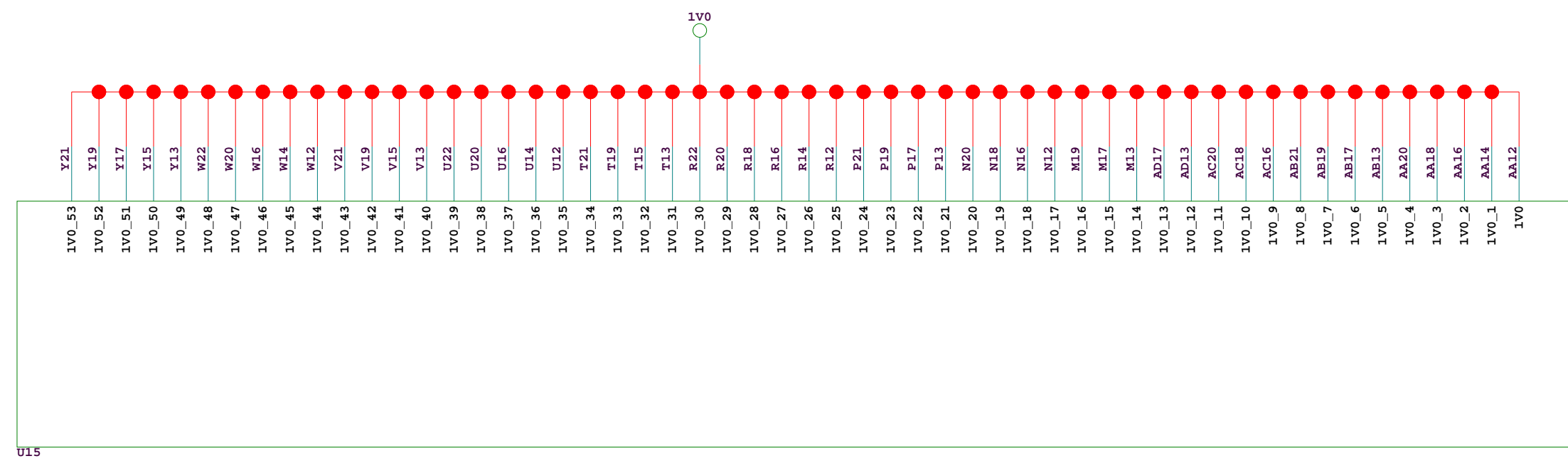
F KAPP

CHECKED

R BAUERMEISTER

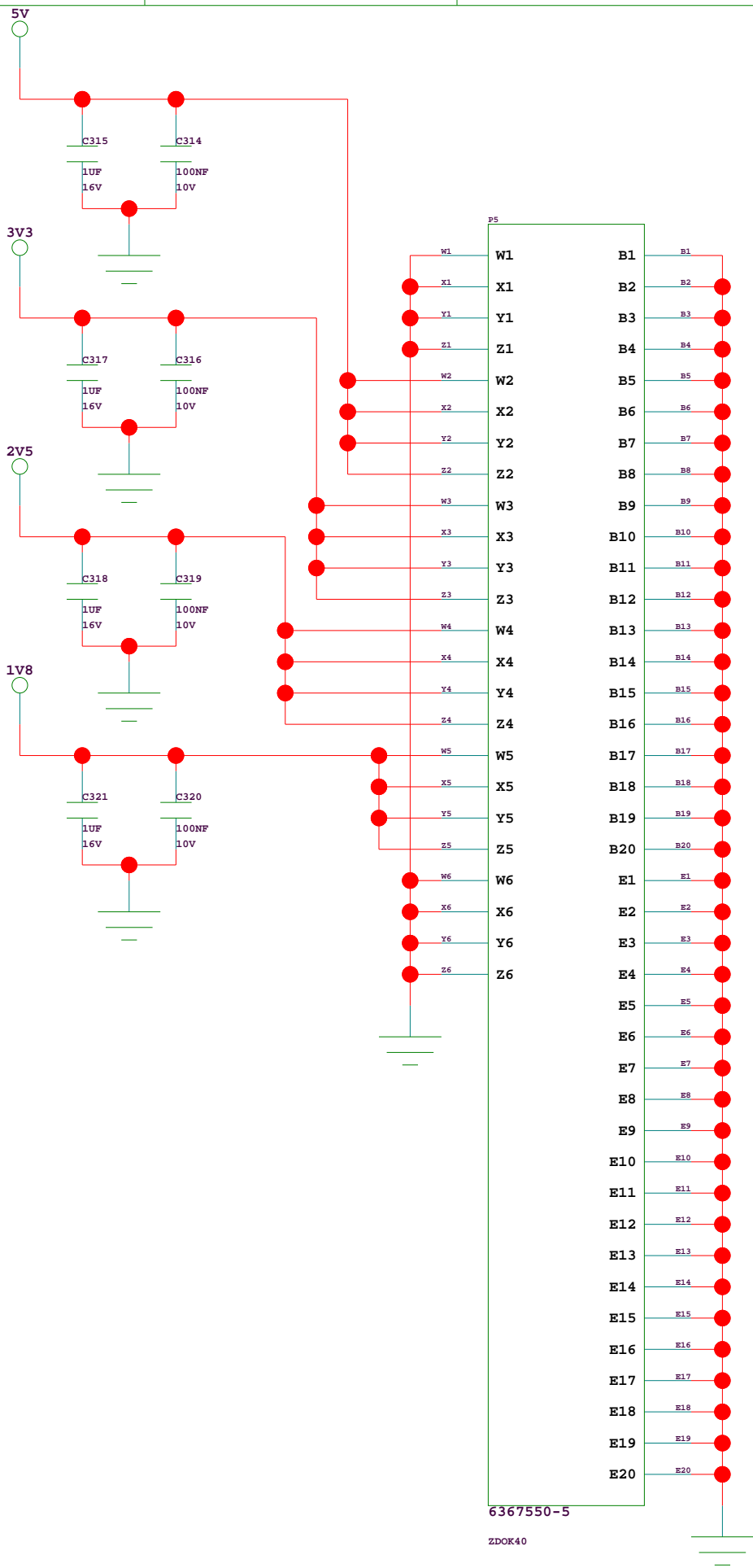
SHEET

2 OF 25

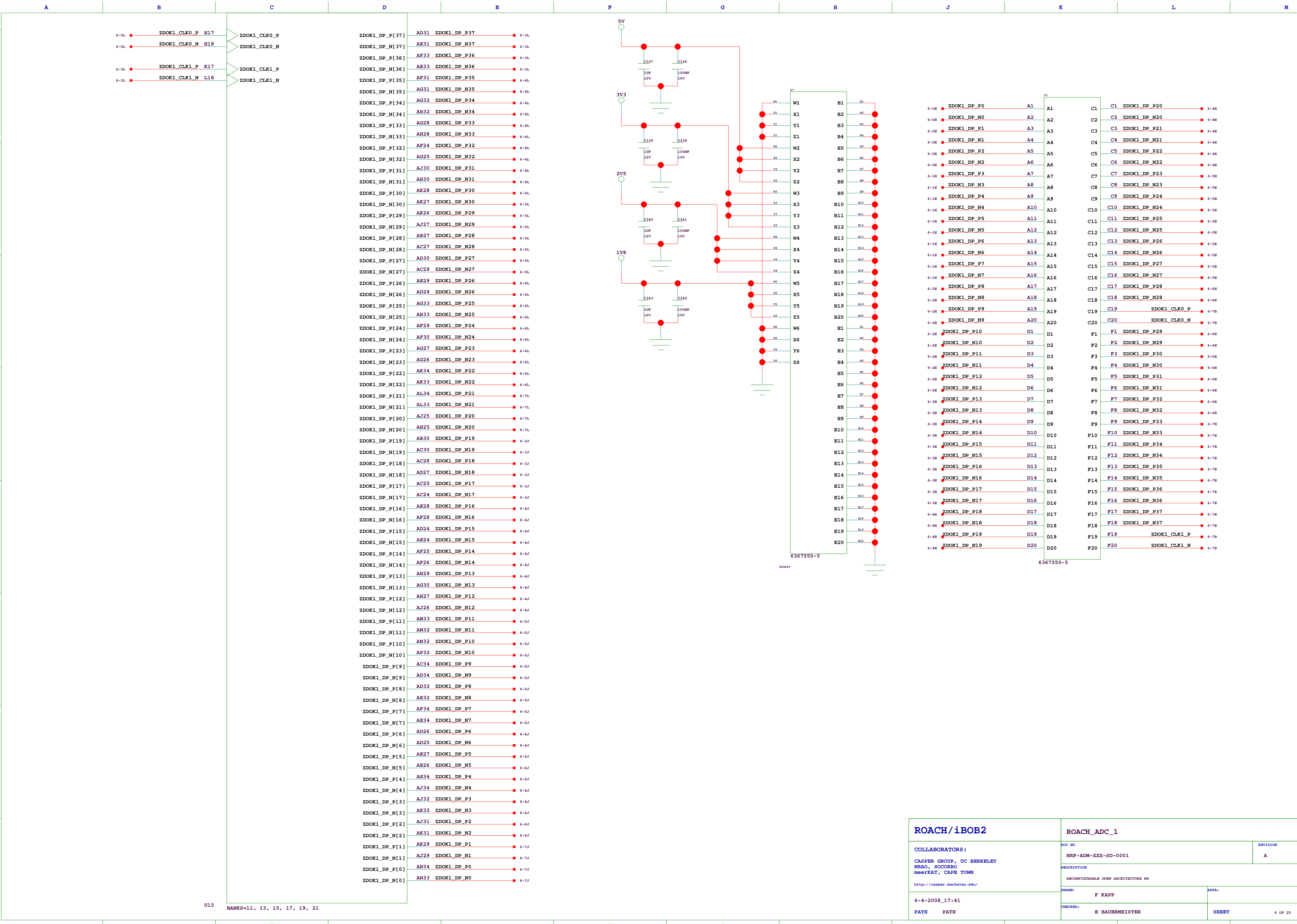


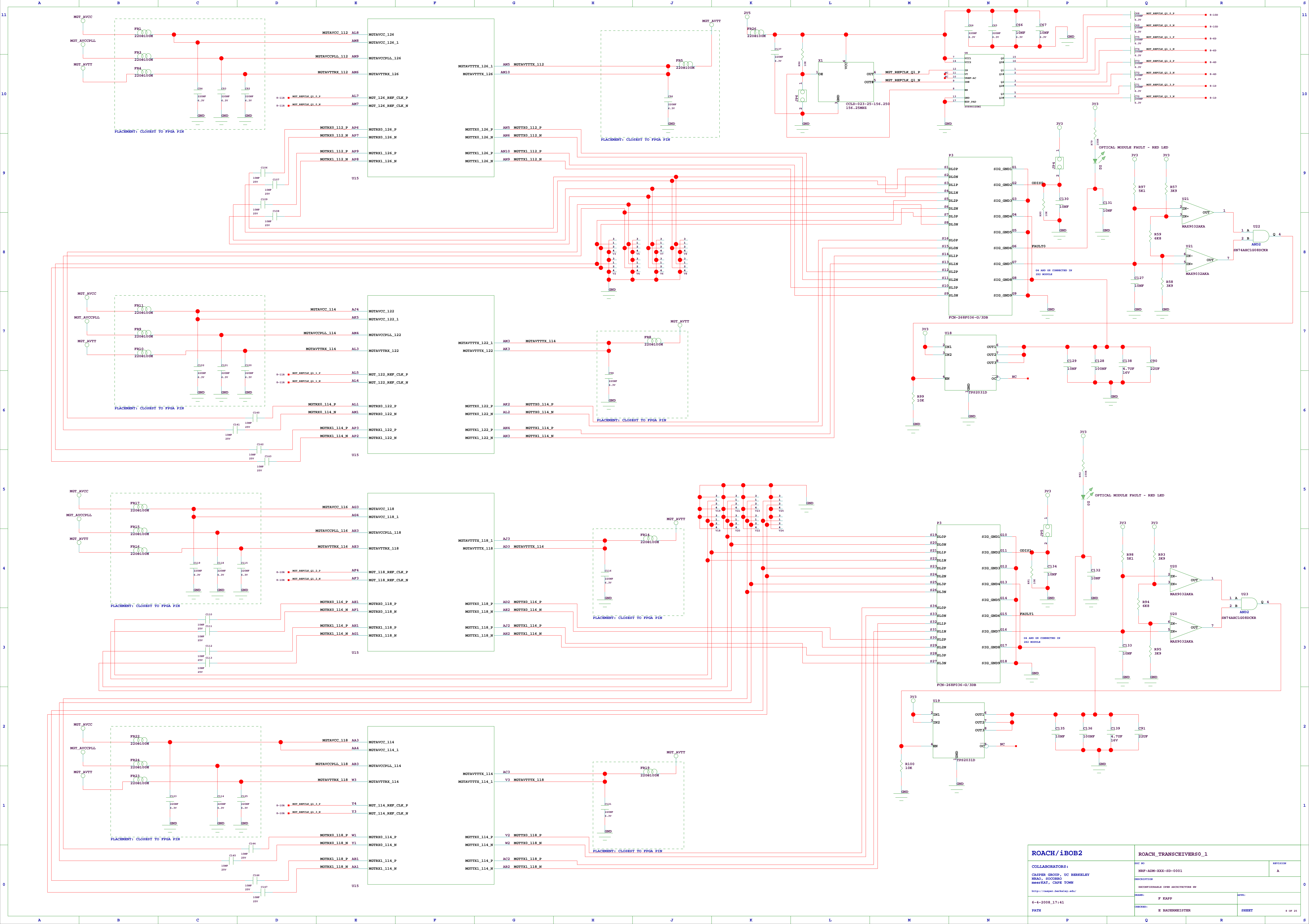
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COLLABORATORS: CAPSER GROUP, UC BERKELEY WANG, SPOONER mae@CAT, CAPS TOWN http://casper.berkeley.edu/		SOC NO NRP-ADM-XXX-ED-0001 DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE IN	REVISION A
6-4-2008_17:41		NAME: F KAPP	APP:
PATH PATH		CHECKED: F BAUMHOMISTER	SHEET 4 OF 2

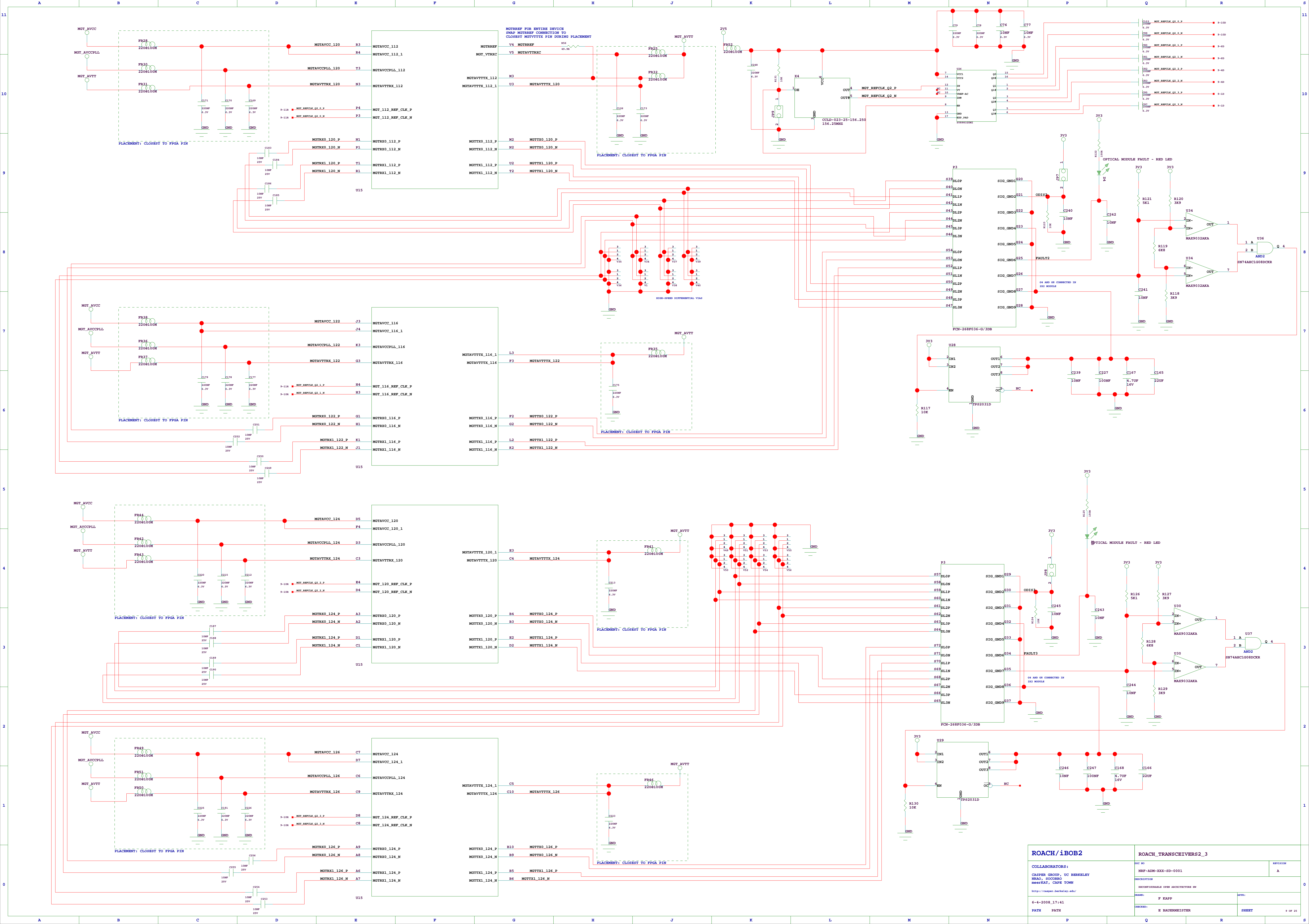
ROACH/iBOB2		ROACH_ADC_0	
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/		DOC NO	REVISION
		NRF-ADM-XXX-SD-0001	A
		DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW	
6-4-2008_17:41		DRAWN: F KAPP	APPR:
PATH PATH		CHECKED: E BAUERMEISTER	SHEET 5 OF 25

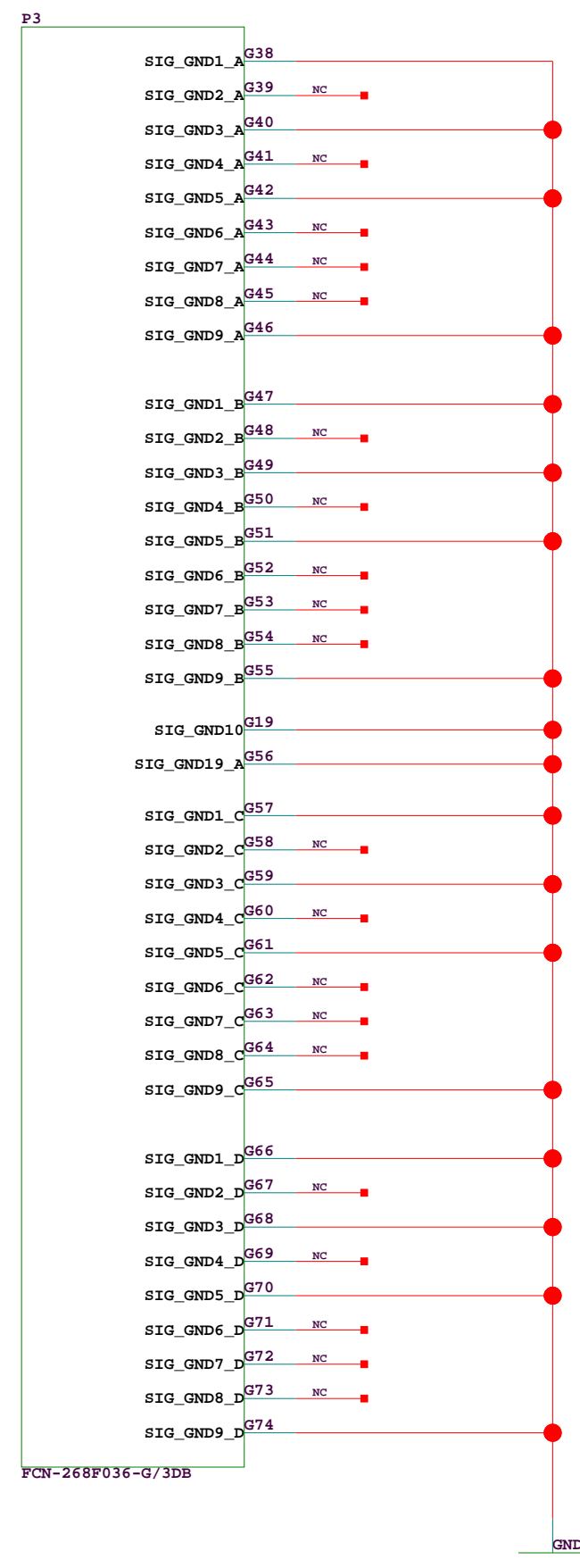
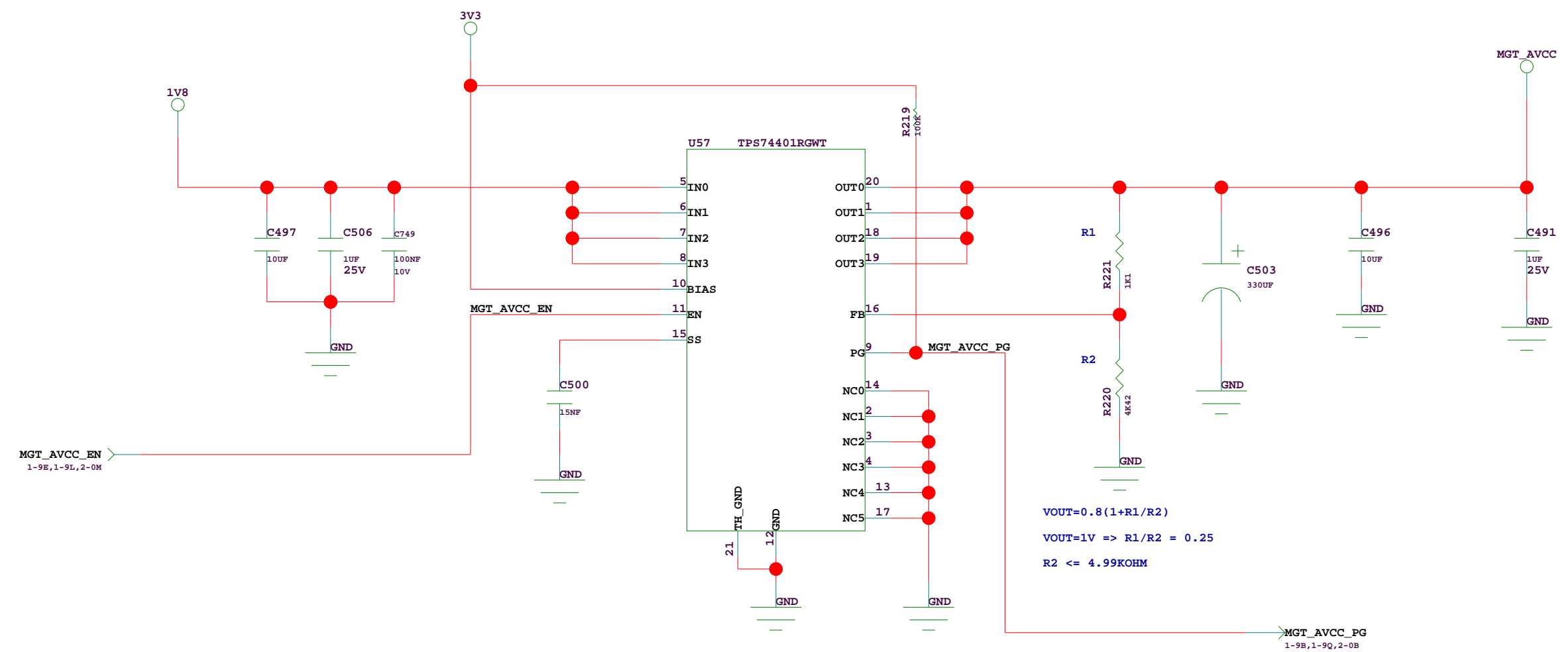
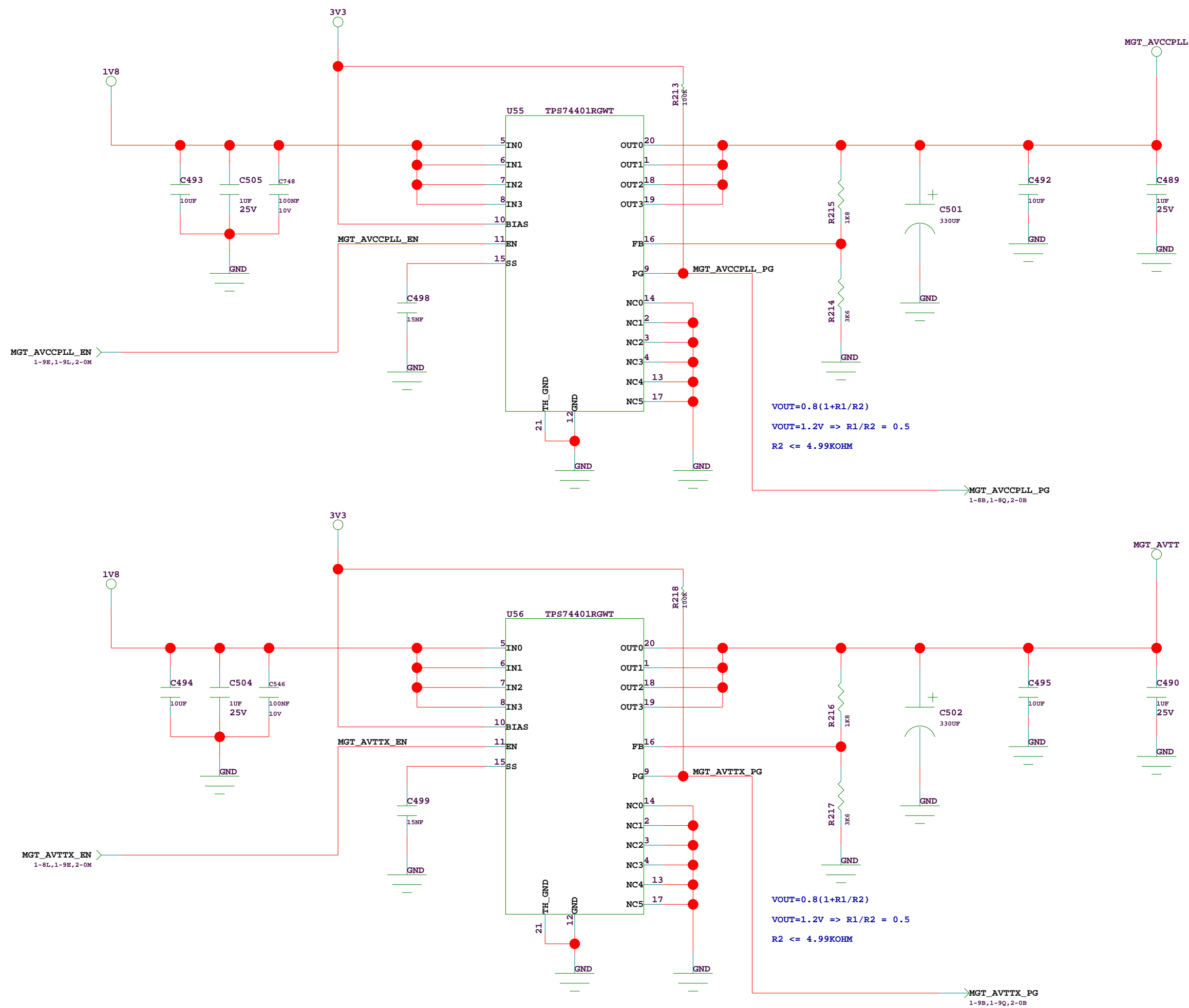


U15 BANKS=11, 13, 15, 17, 19, 21

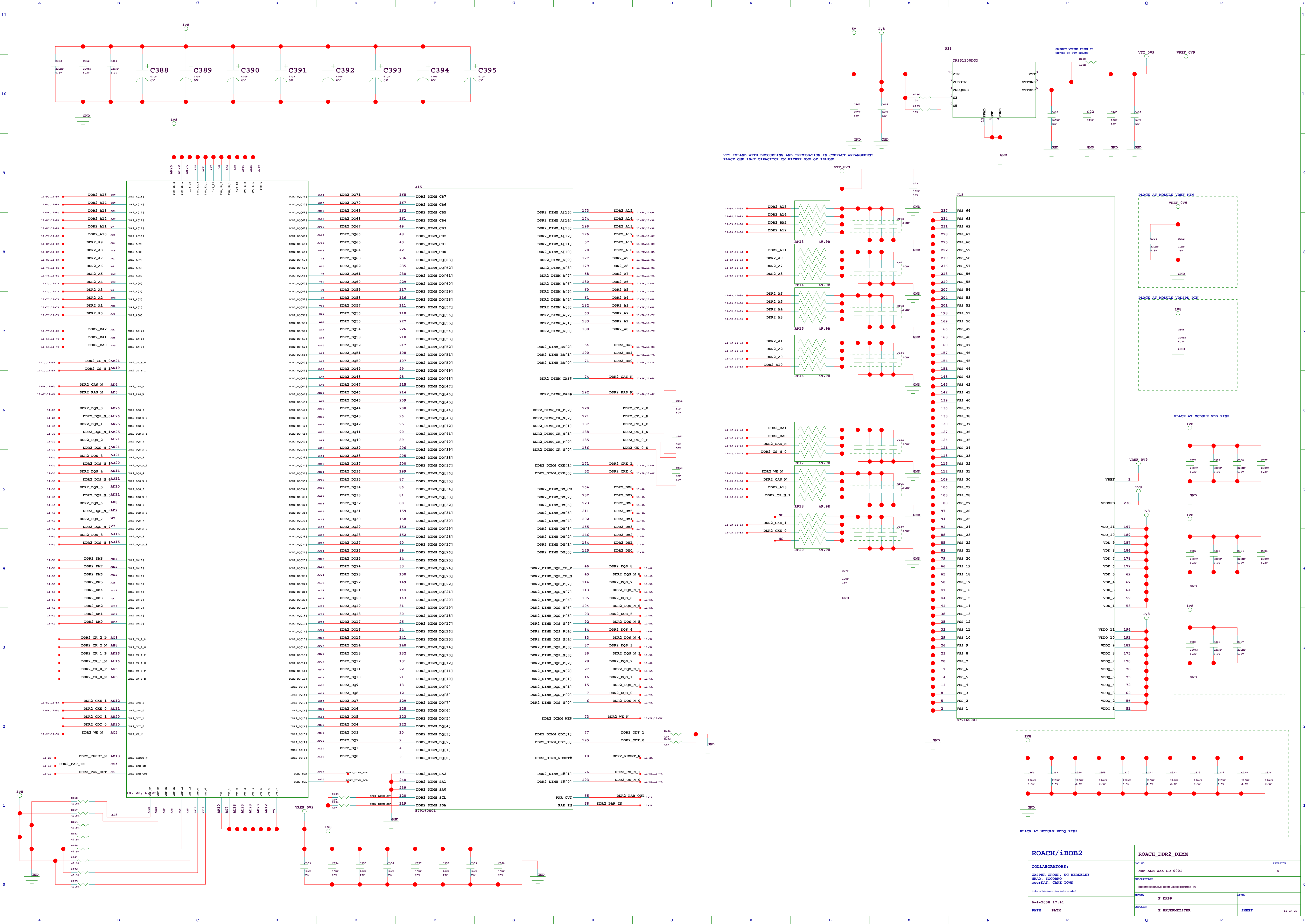


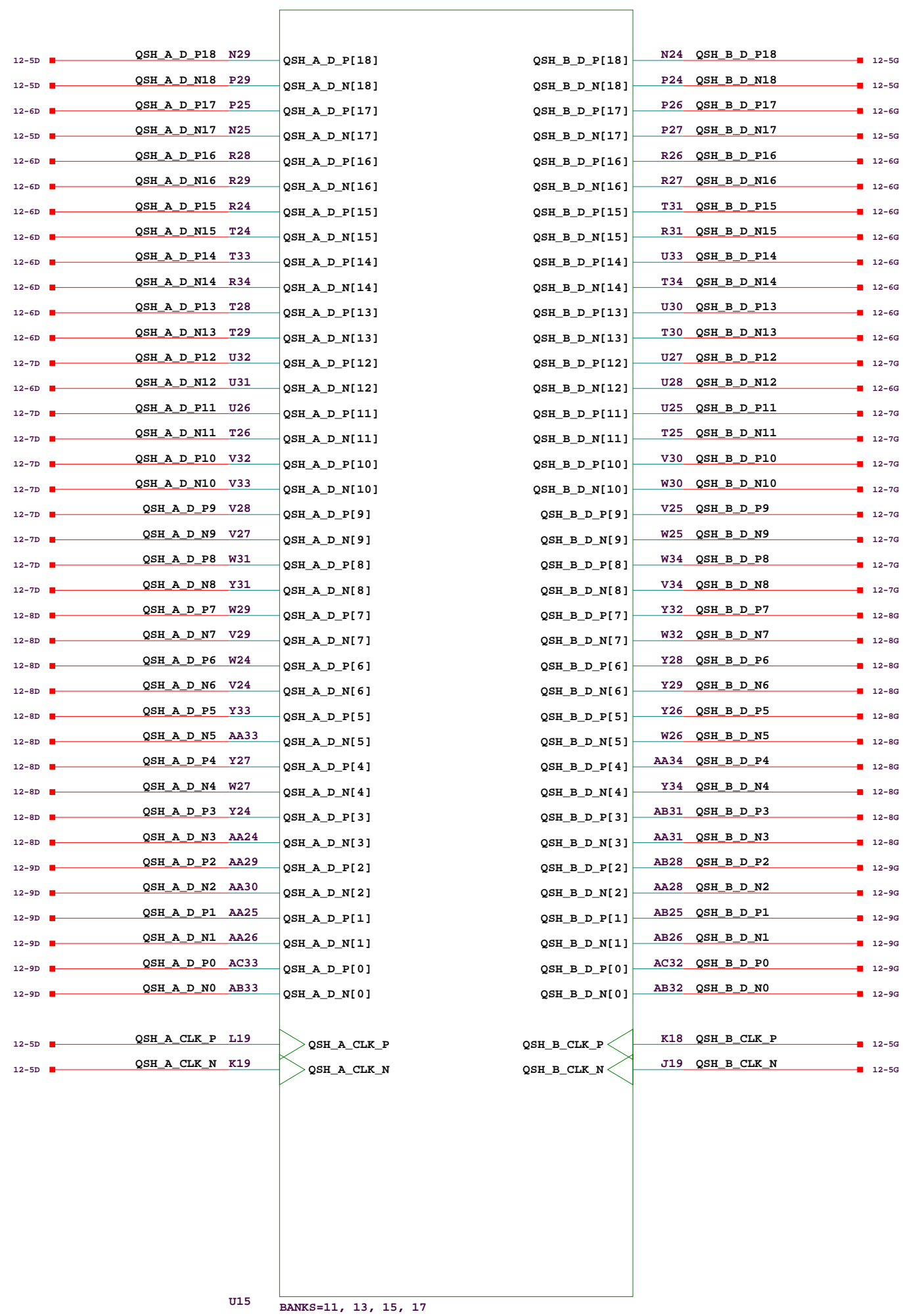
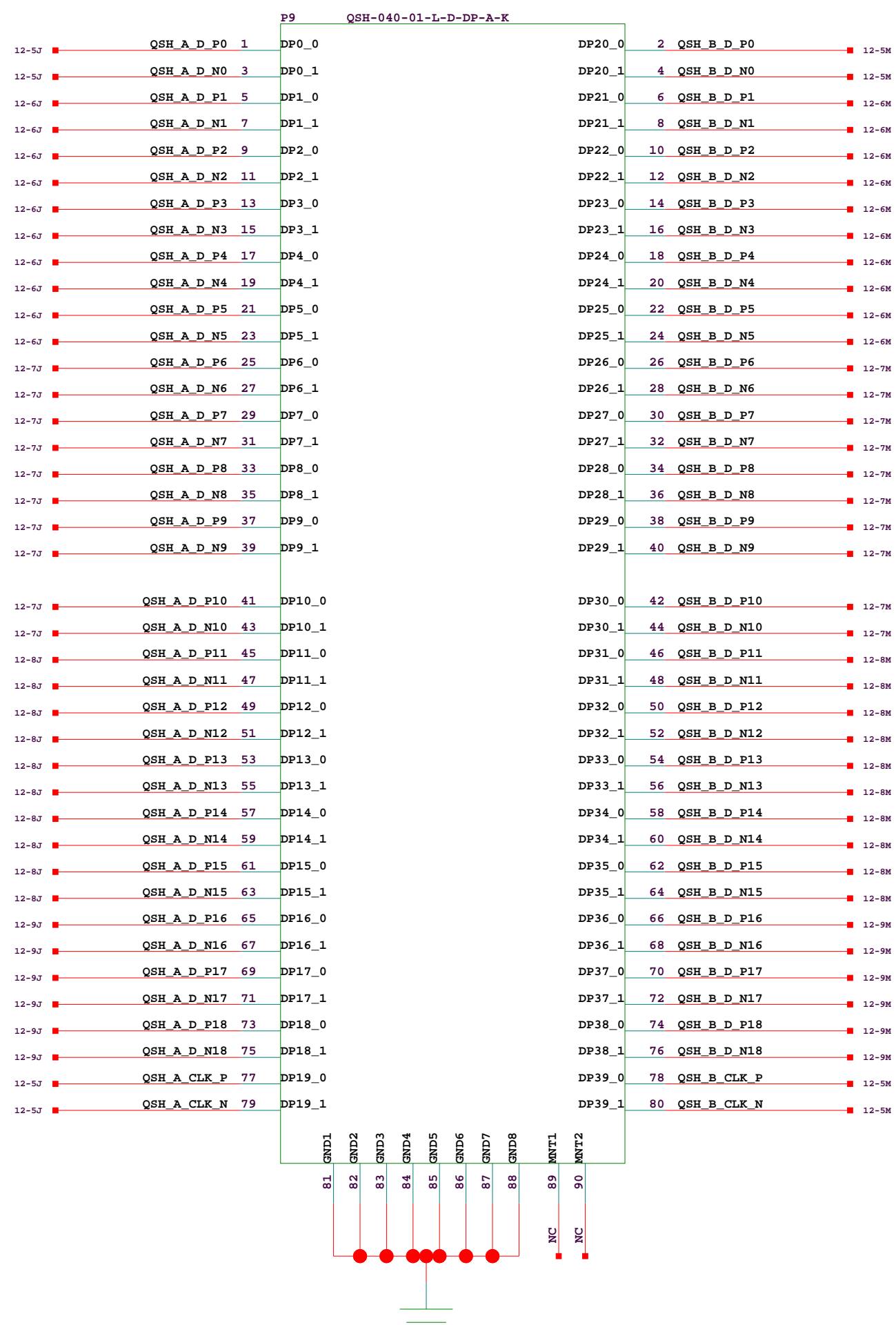




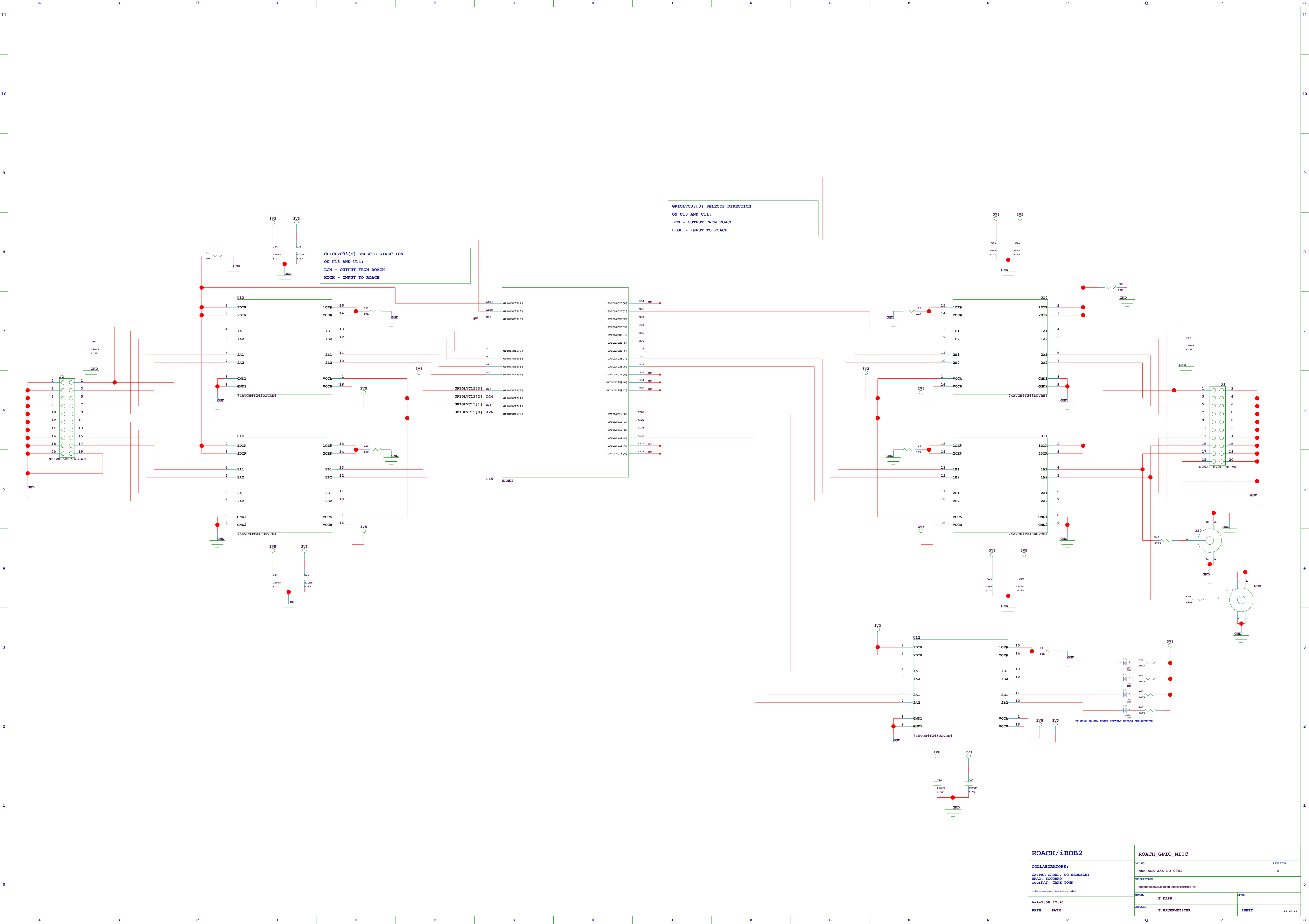


ROACH/iBOE2		ROACH_TRANSCEIVERS_PSU	
COLLABORATORS:		DOC NO:	REVISION:
CASPER GROUP, UC BERKELEY		NRF-ADM-XXX-SD-0001	A
MESA, SOCORRO		DESCRIPTION:	
MesaEAT, CAPE TOWN		RECONFIGURABLE OPEN ARCHITECTURE HW	
http://casper.berkeley.edu/		DRAWN:	APPD:
6-4-2008 17:41		F KAPP	
PATH PATH		CHECKED:	SHEET
		E BAUERMEISTER	10 OF 2

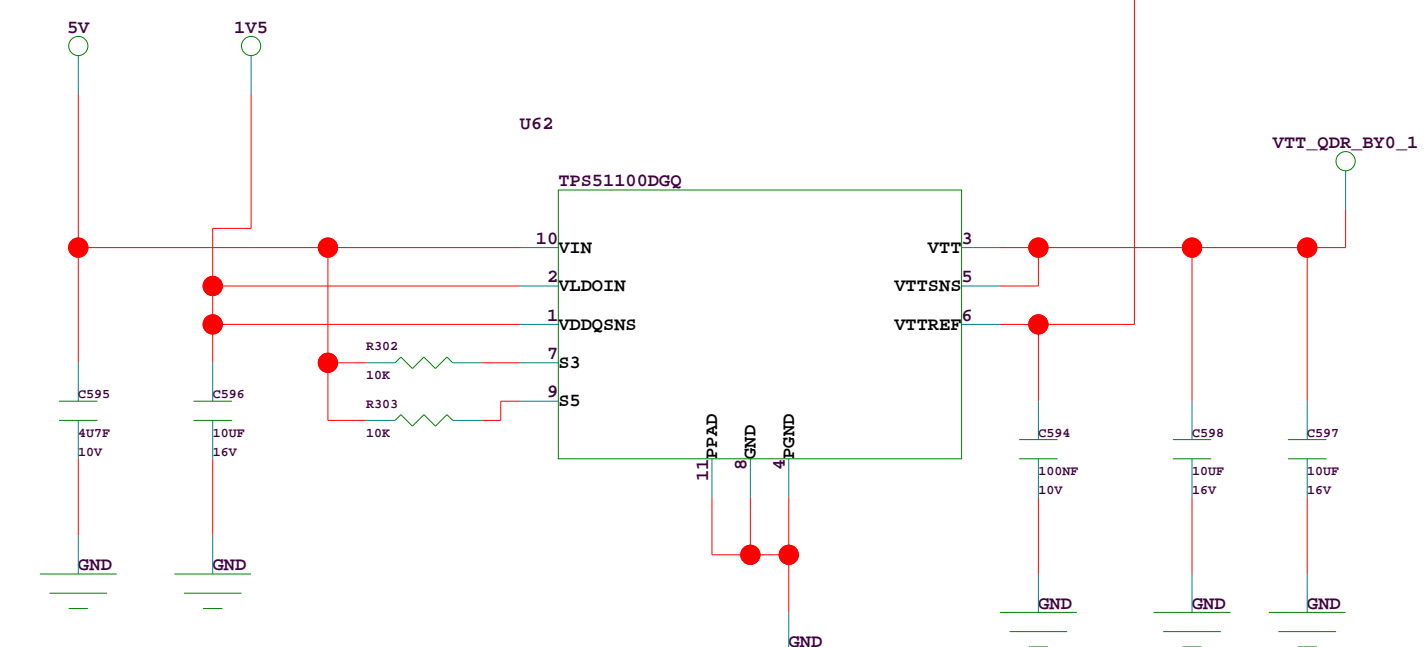
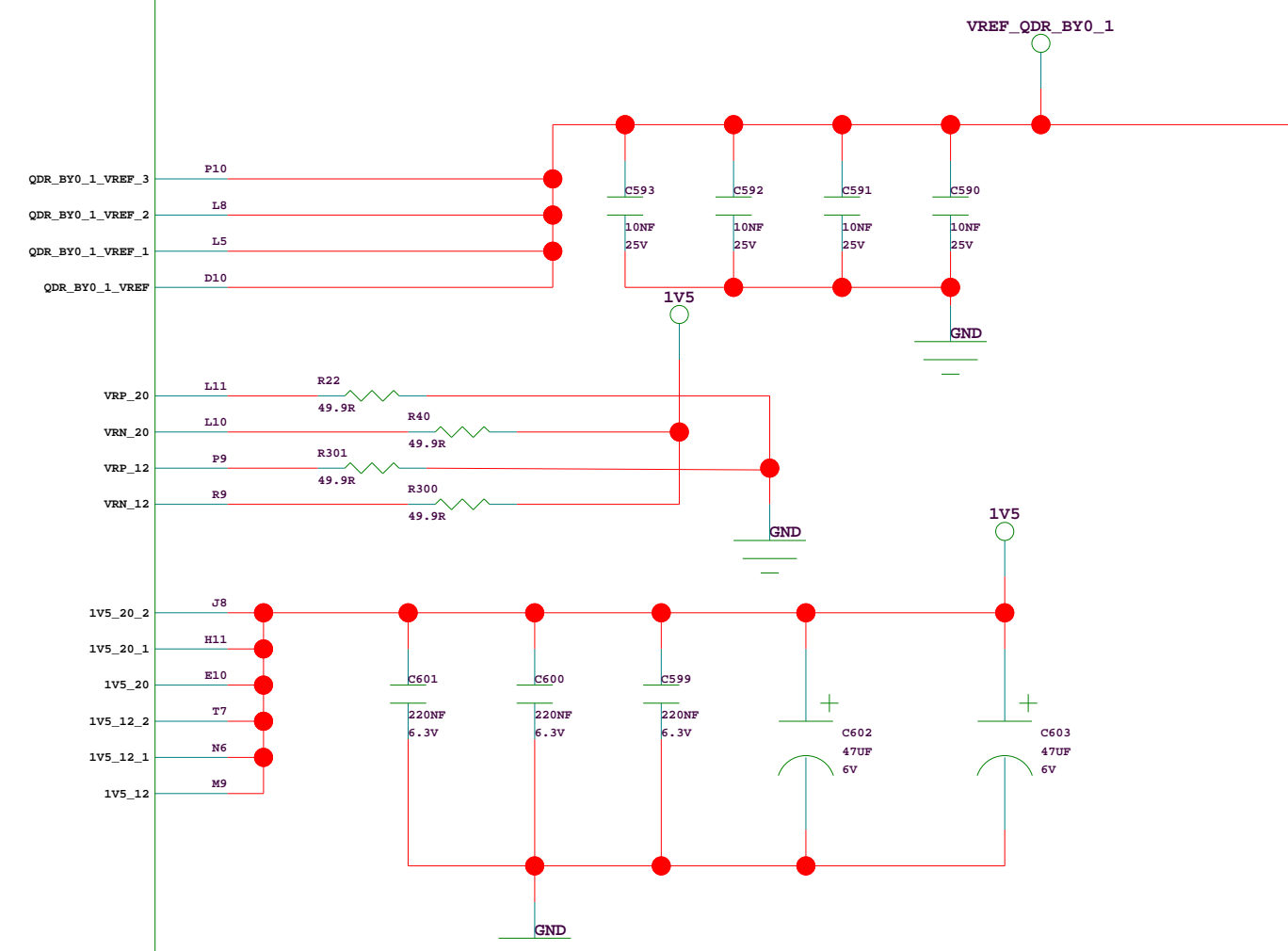
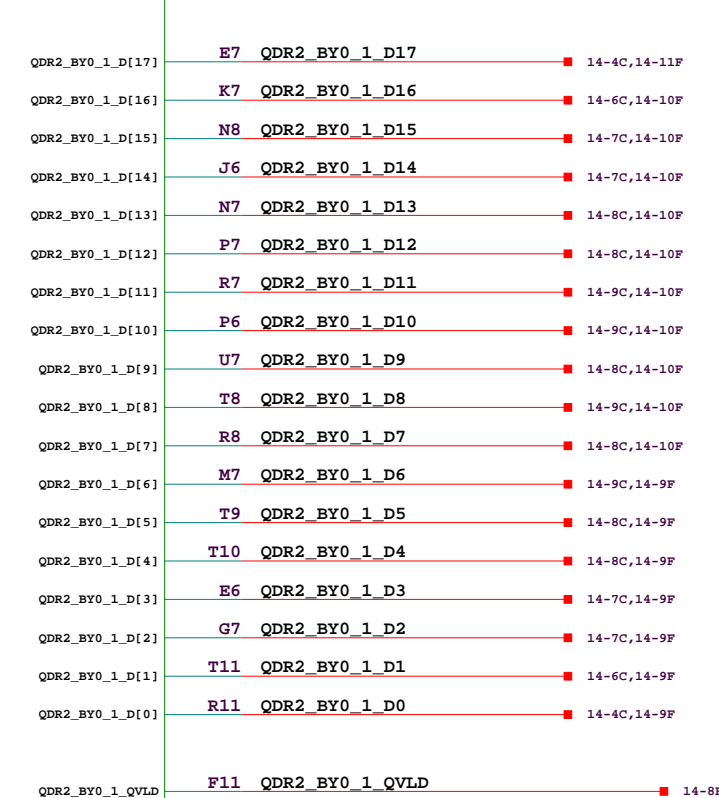
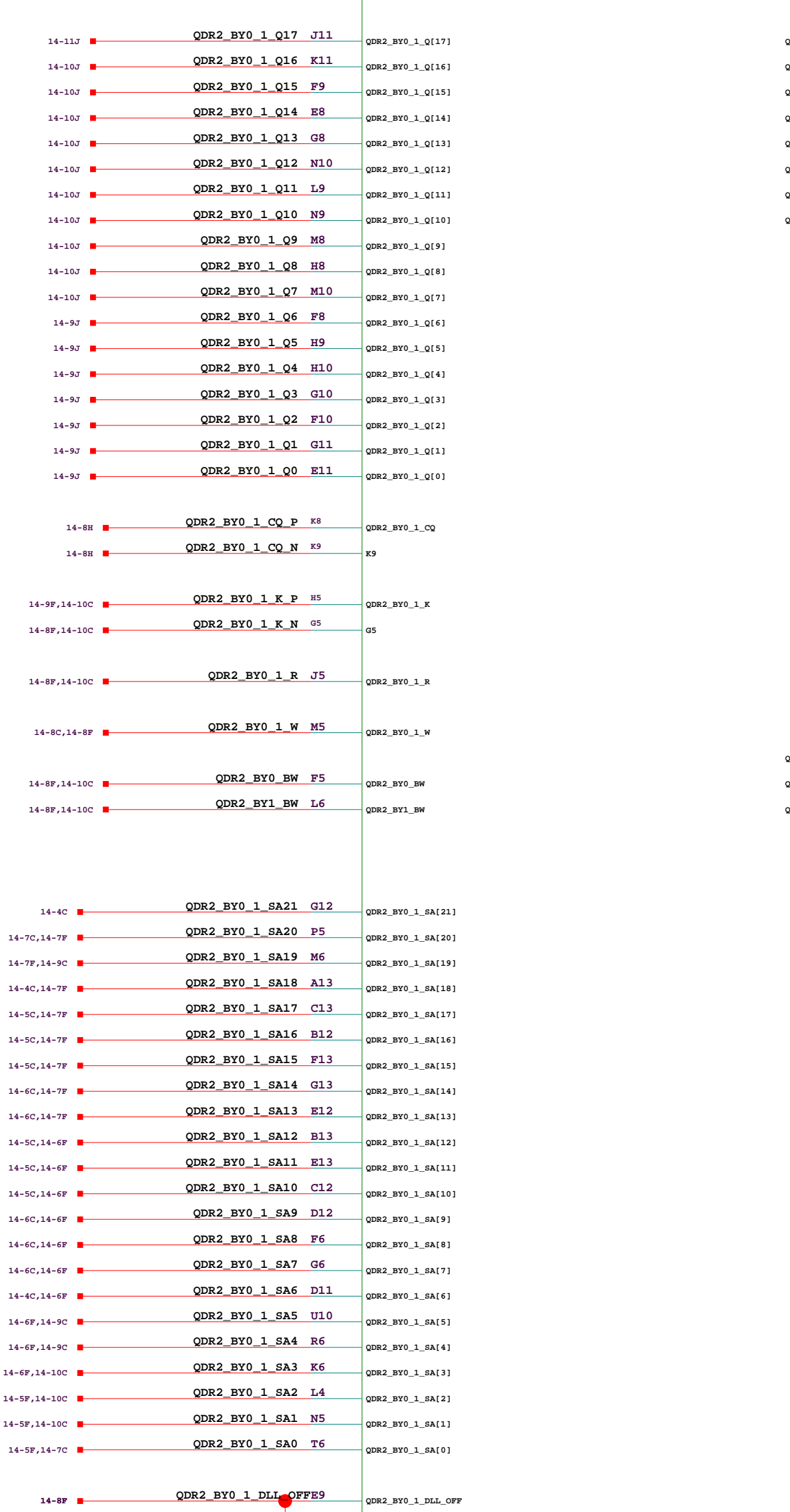
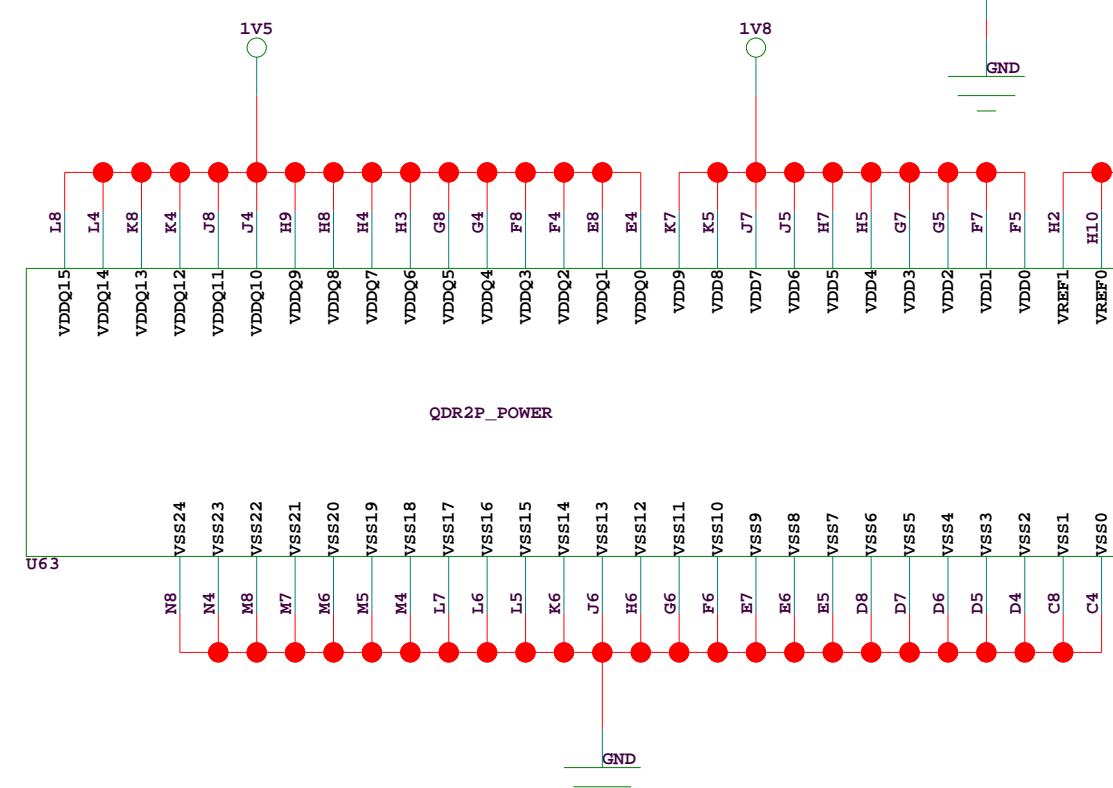
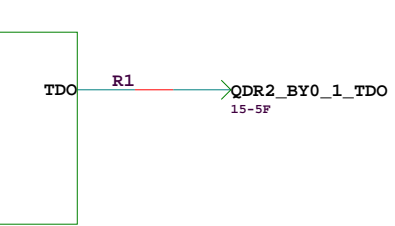
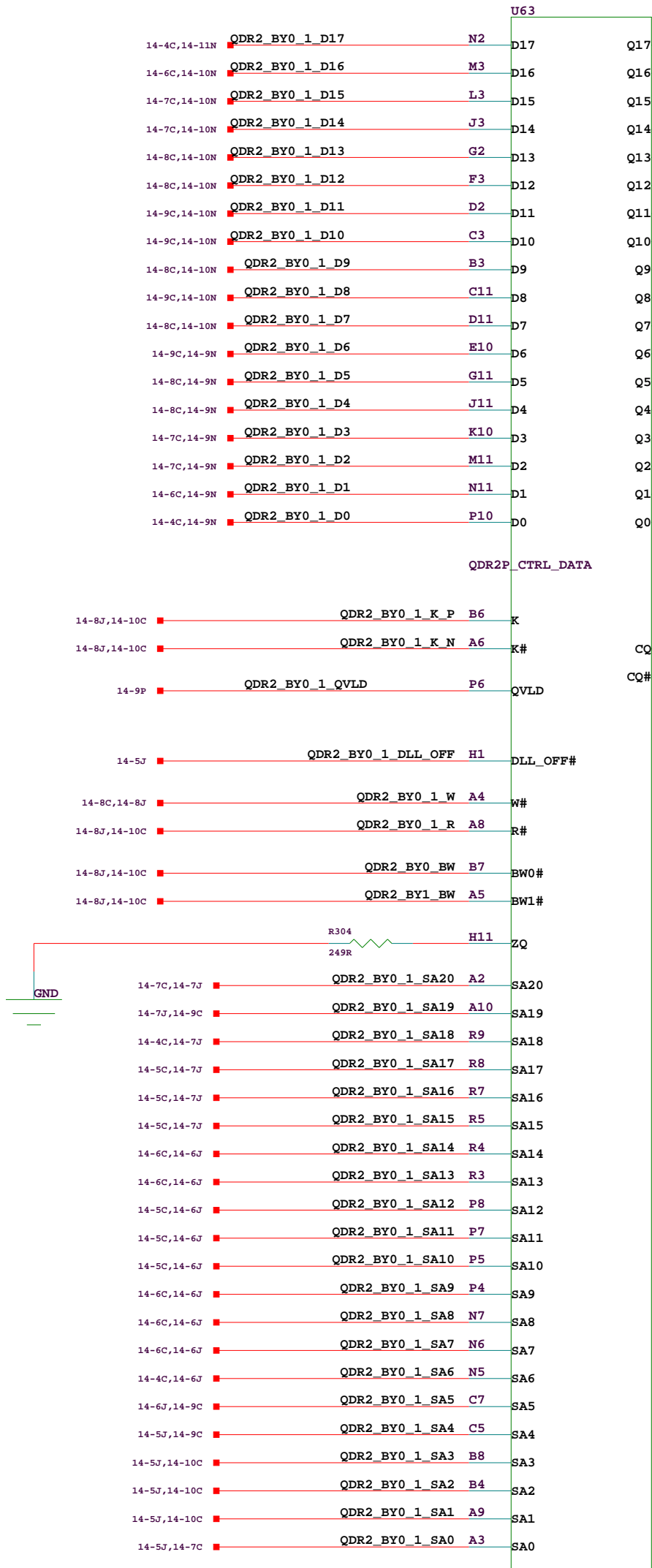
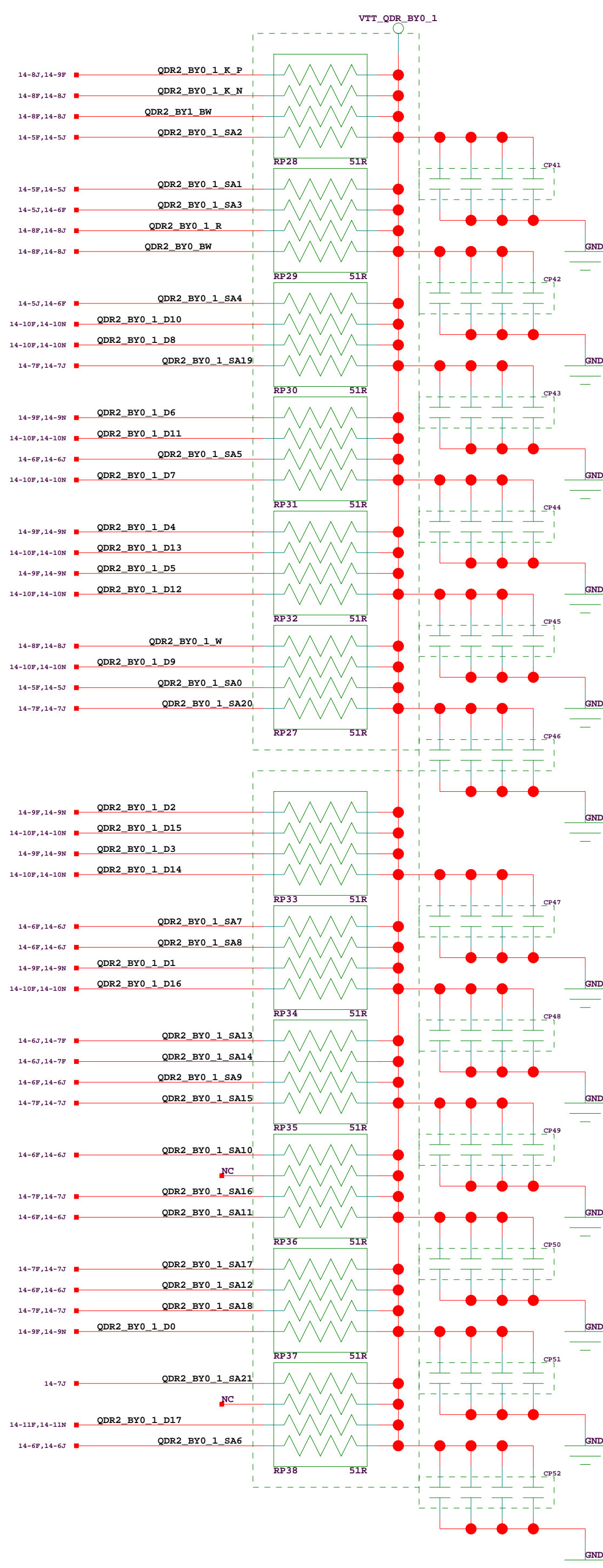




ROACH/iBOE2		ROACH_DIFF_GPIO		REVISION	
COLLABORATORS:		DOC NO		A	
CASPER GROUP, UC BERKELEY		NEP-ADM-XXX-ED-0001			
MAD, SPOCCO		DESCRIPTION			
MEERKAT, CAPE TOWN		RECONFIGURABLE OVER ARCHITECTURE RM			
http://casper.berkeley.edu/		NAME:		APP:	
6-4-2008 17:41		F KAPP			
PATH PATH		CHECKED:		SHEET	
		E BAUERMEISTER		12 OF 2	

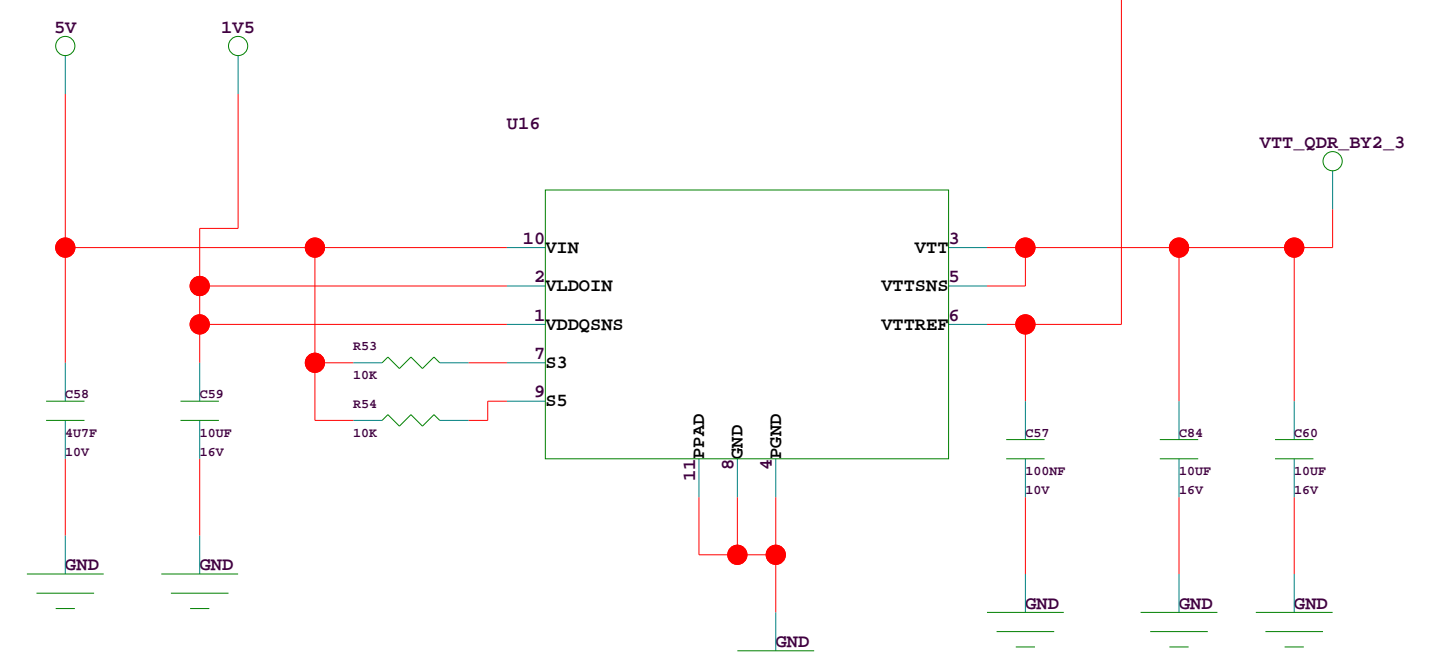
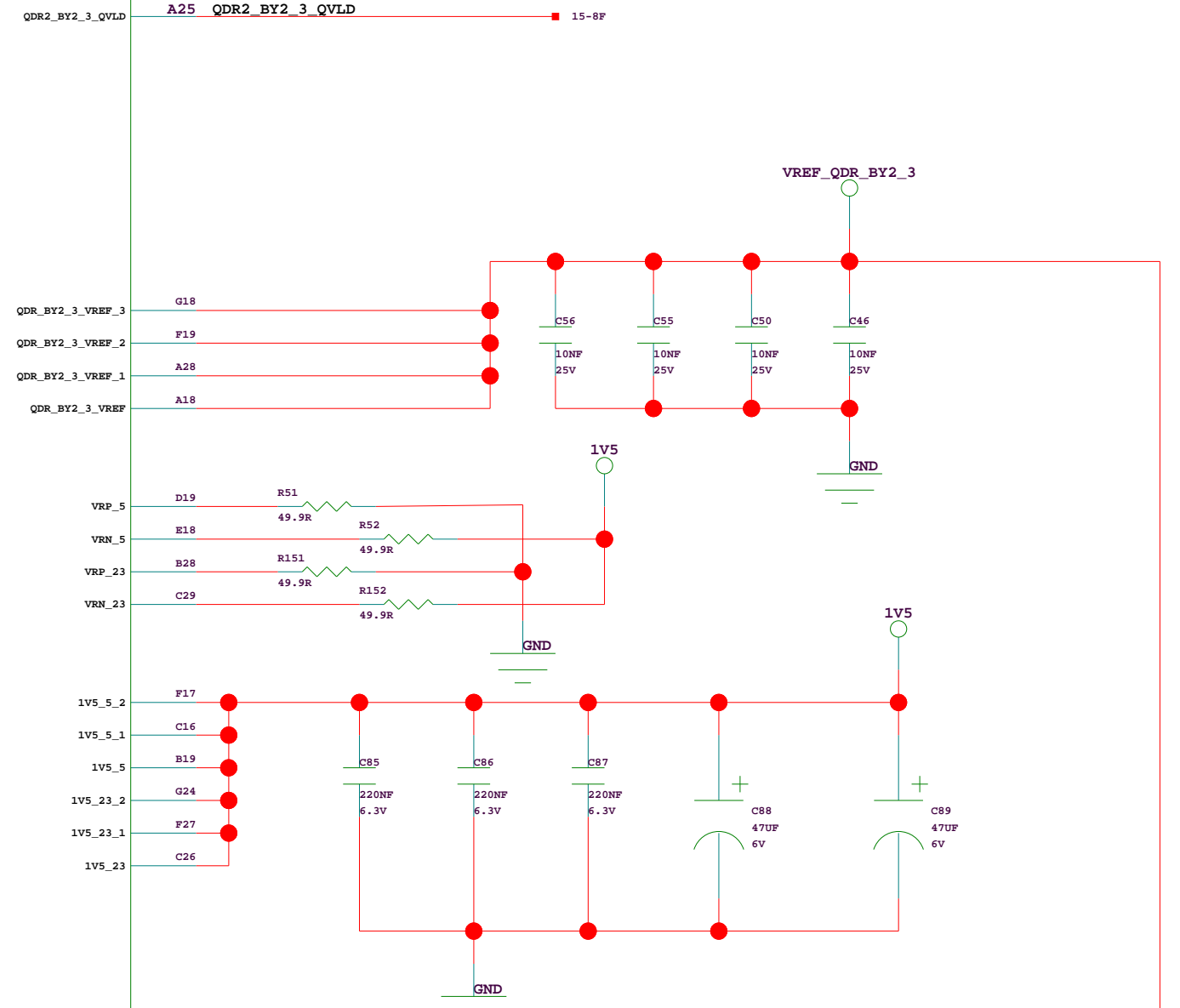
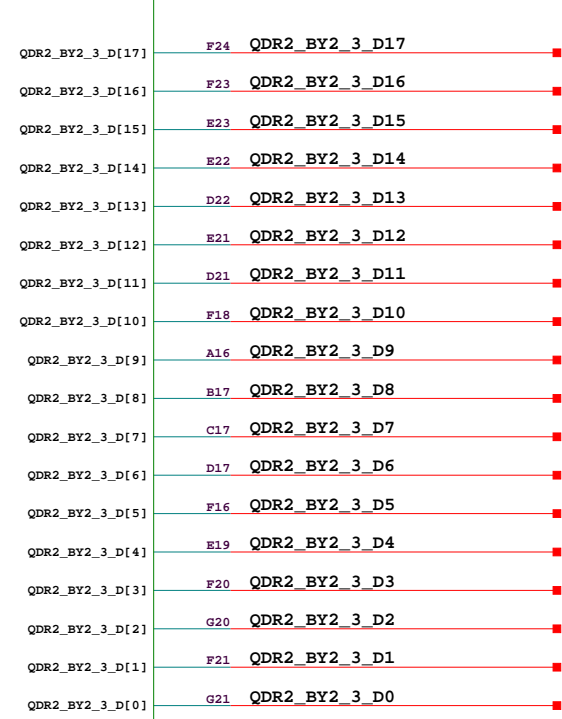
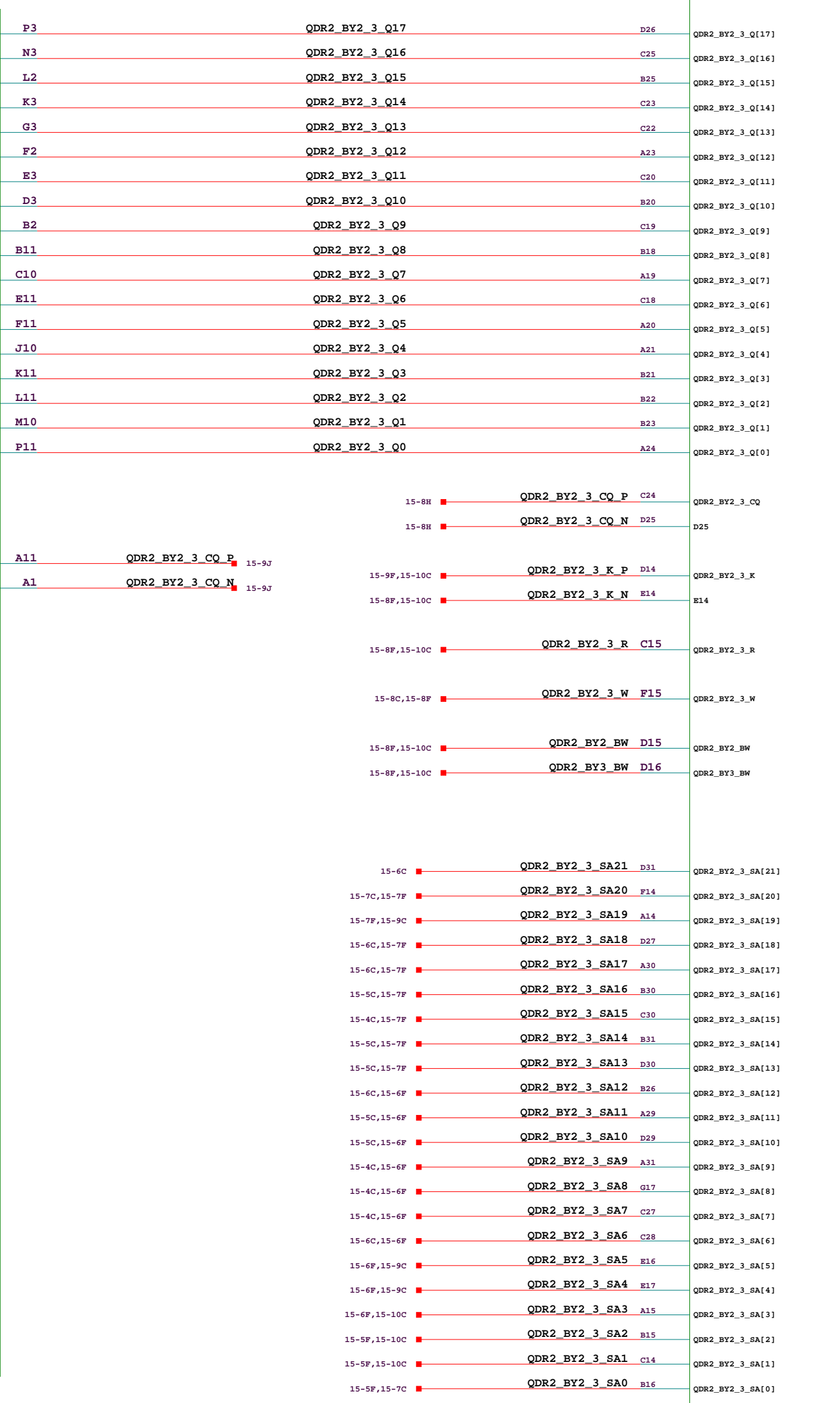
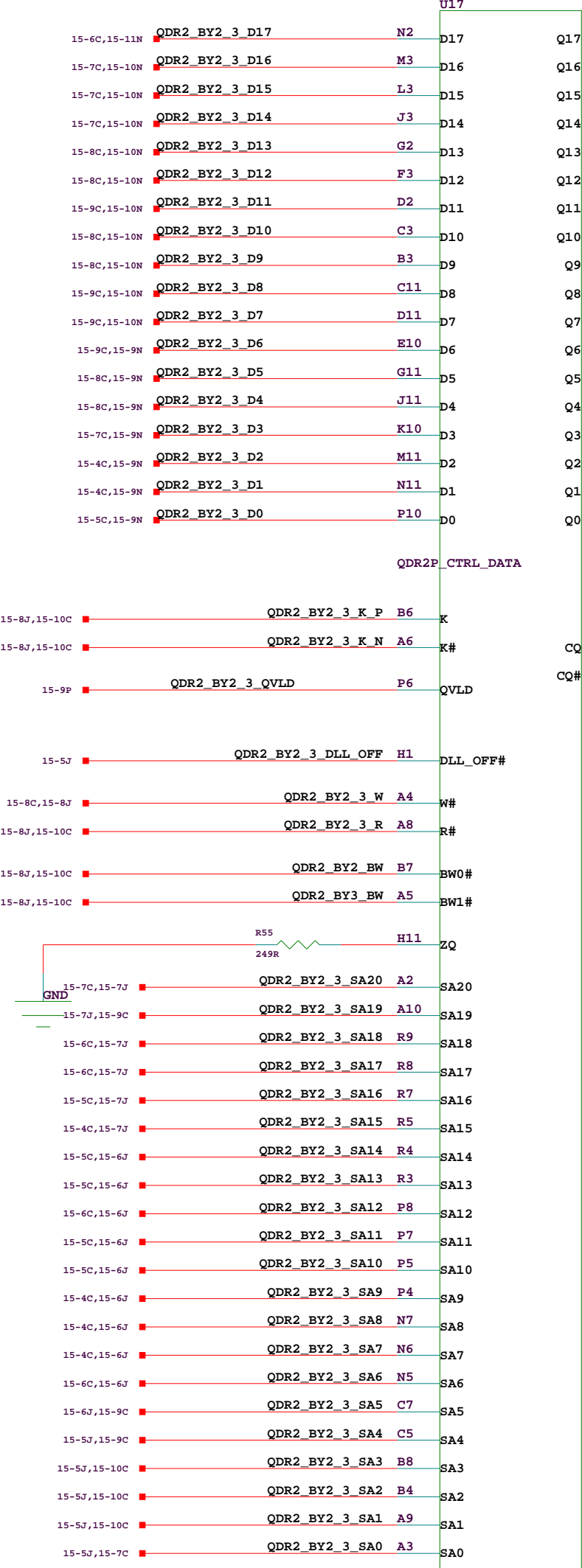
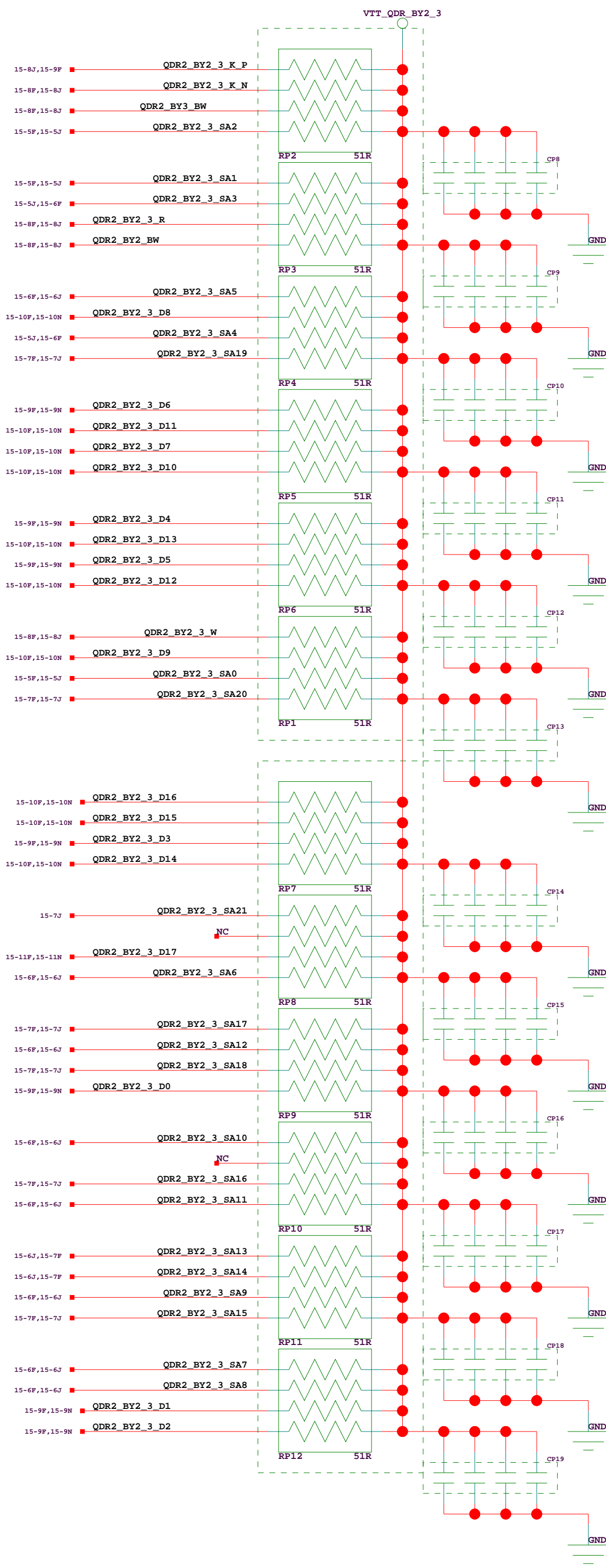


ROACH/iBOE2		ROACH_GPIO_MISC	
COLLABORATORS:		DCC NO	REVISION
CASPER GROUP, UC BERKELEY		NRF-ADM-XXX-BD-0001	A
DESCRIPTION		RECONFIGURABLE OPEN ARCHITECTURE HW	
http://casper.berkeley.edu/		DESIGNER	APPD
6-4-2008_17:41		F KAPP	
PATH	PATH	DESIGNED BY	SHEET
		R BAUERMISTROT	13 OF 25



GND and PGND (Power GND) should be isolated, with a single point connection between them.

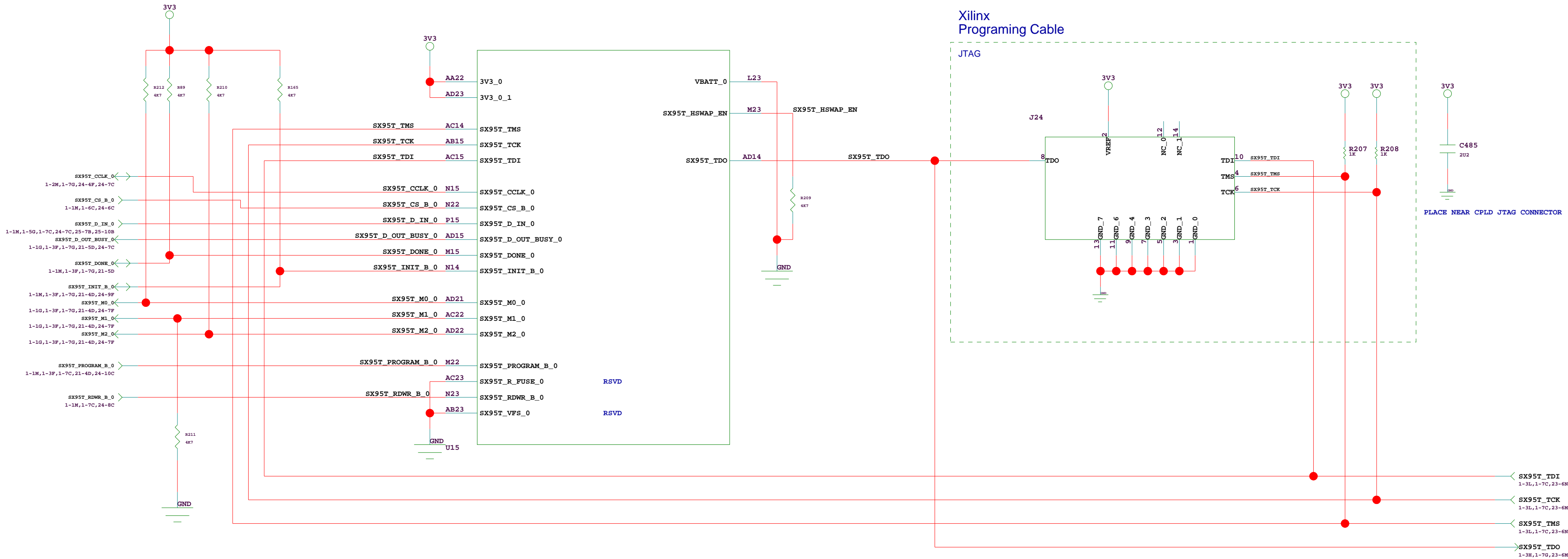
ROACH/iBOB2		ROACH_QDR2P_BY0_1	
COLLABORATORS: CAPSER GROUP, UC BERKELEY WANG, SCORROD mae@CAT, CAPS TOWN http://capers.berkeley.edu/		DOC NO NRC-ADM-XXX-ED-0001 DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE MM	
6-4-2008 17:41		NAME: F KAPP	APPR:
PATH PATH		CHECKED: F BAUMHOMISTER	SHEET 14 OF 2



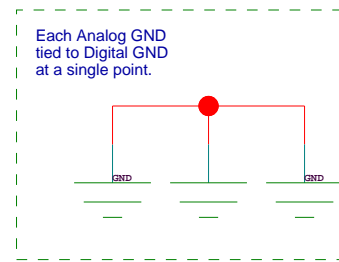
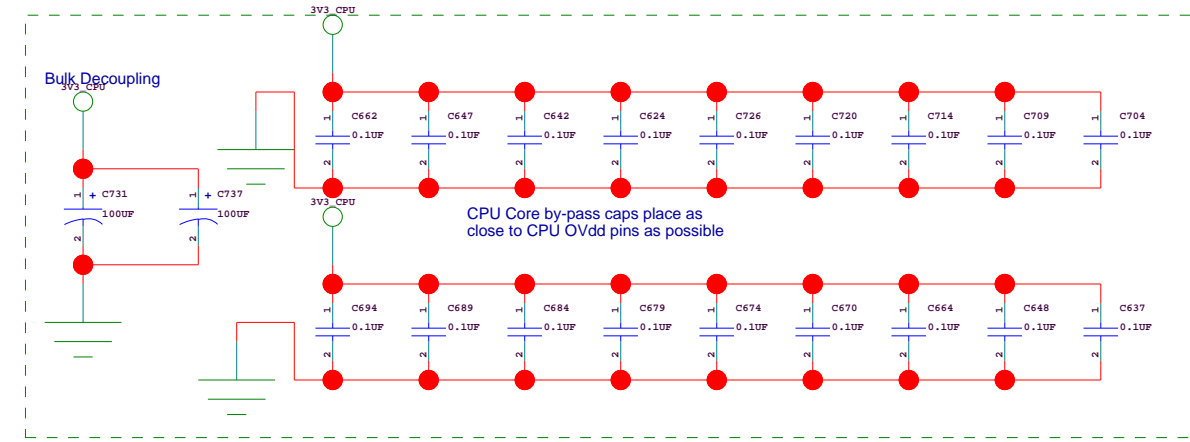
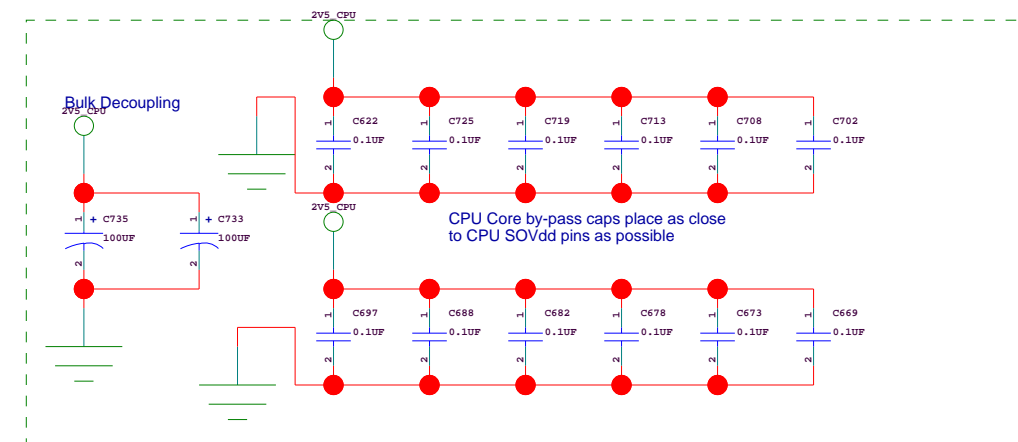
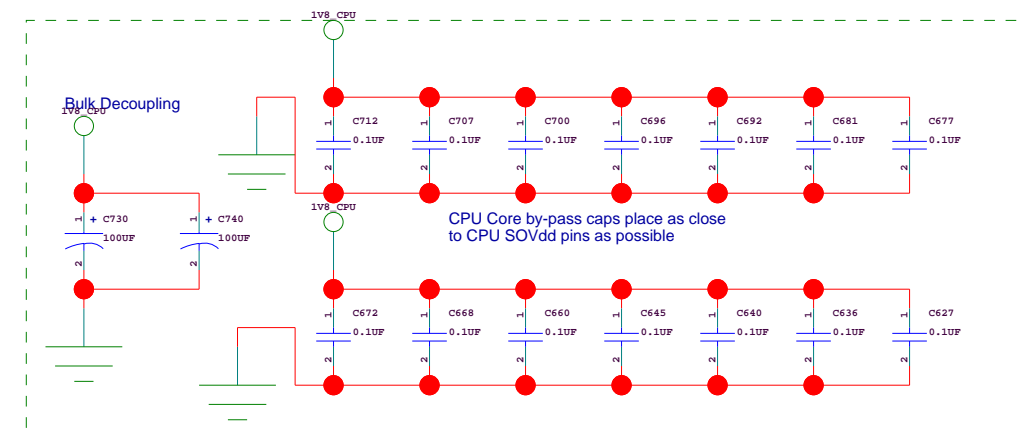
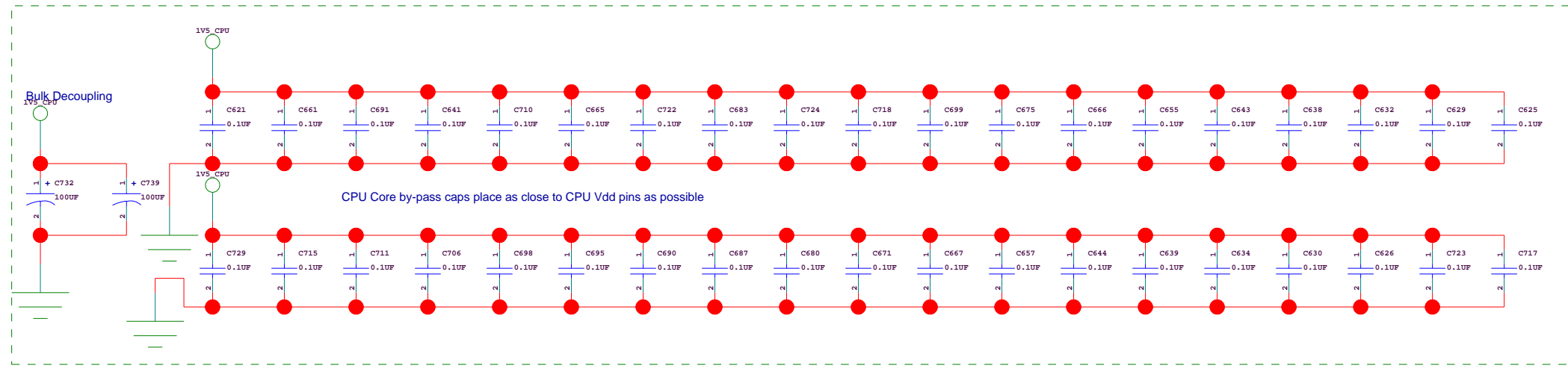
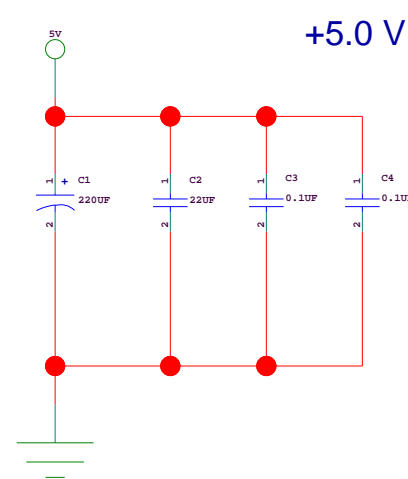
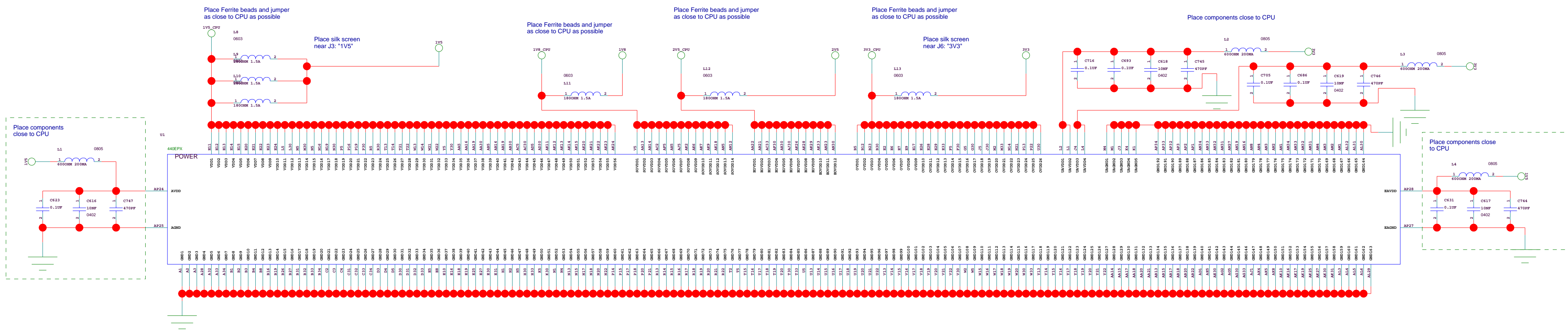
GND and PWRD (Power GND) should be isolated, with a single point connection between them.

ROACH/iBOB2		ROACH_QDR2P_BY2_3	
COLLABORATORS:		DOC NO	REVISION
CASPER GROUP, UC BERKELEY		NRF-ADM-XXX-SD-0001	A
NRAO, SOONERO		DESCRIPTION	
MesaCAT, CAPE TOWN		RECONFIGURABLE OPEN ARCHITECTURE HW	
http://casper.berkeley.edu/		DATE:	APP:
6-4-2008 17:41		F KAPP	
PATH PATH		R BAUERNBIESTER	SHEET

VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input



ROACH/iBOB2		ROACH_CONFIG	
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/		DOC NO	REVISION
		NRF-ADM-XXX-SD-0001	A
		DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW	
6-4-2008_17:41 PATH PATH		SRAM: F KAPP	APPR:
		CHECKED: E BAUERMEISTER	SHEET 16 OF 25



REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOE2

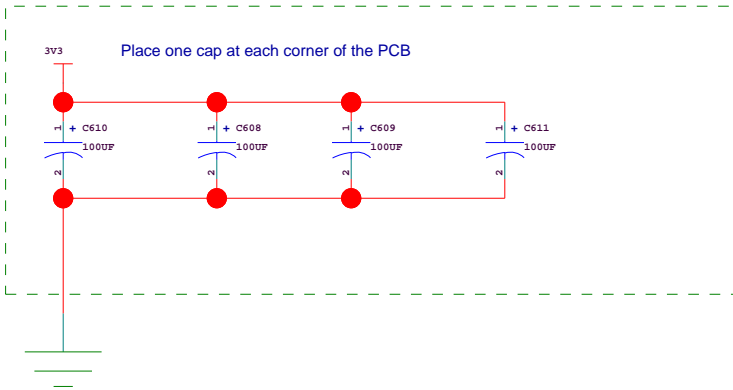
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOONERO
BeeKAT, CAPE TOWN
<http://casper.berkeley.edu/>

6-4-2008_17:41

PATH PATH

ROACH_PPC_POWER_1

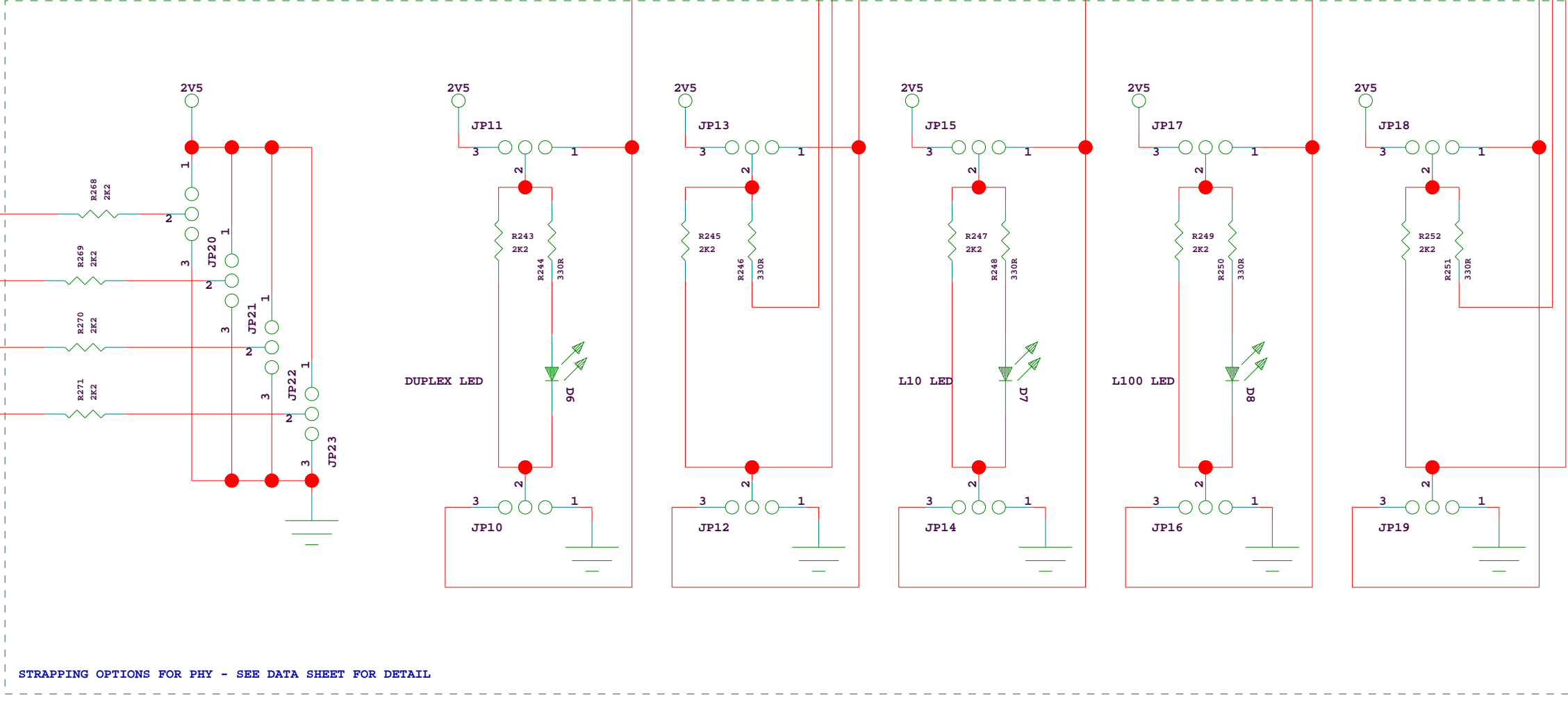
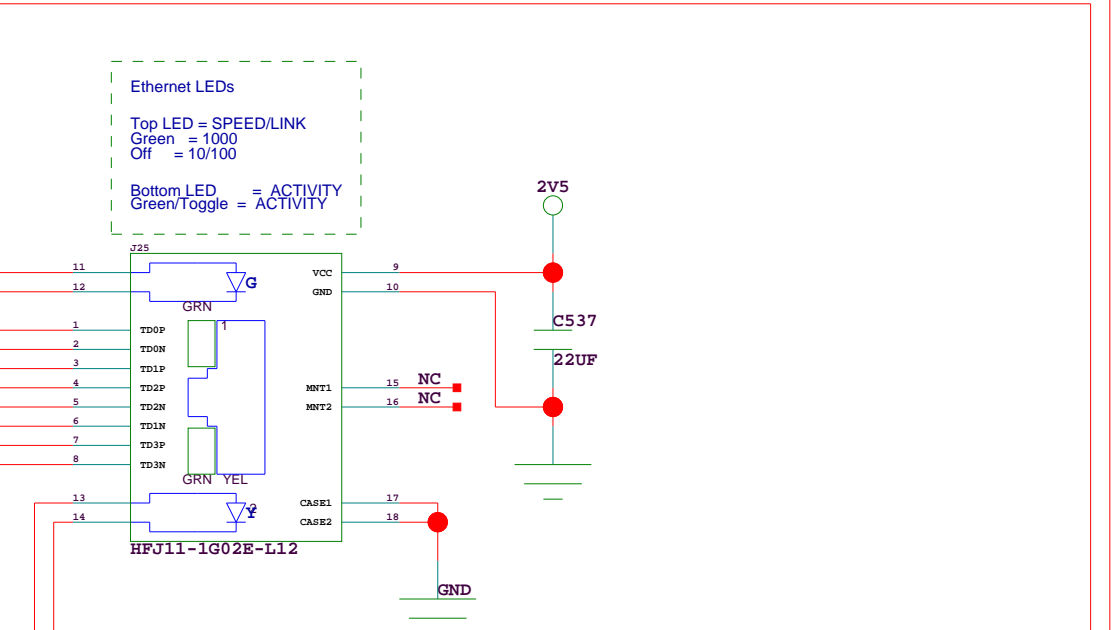
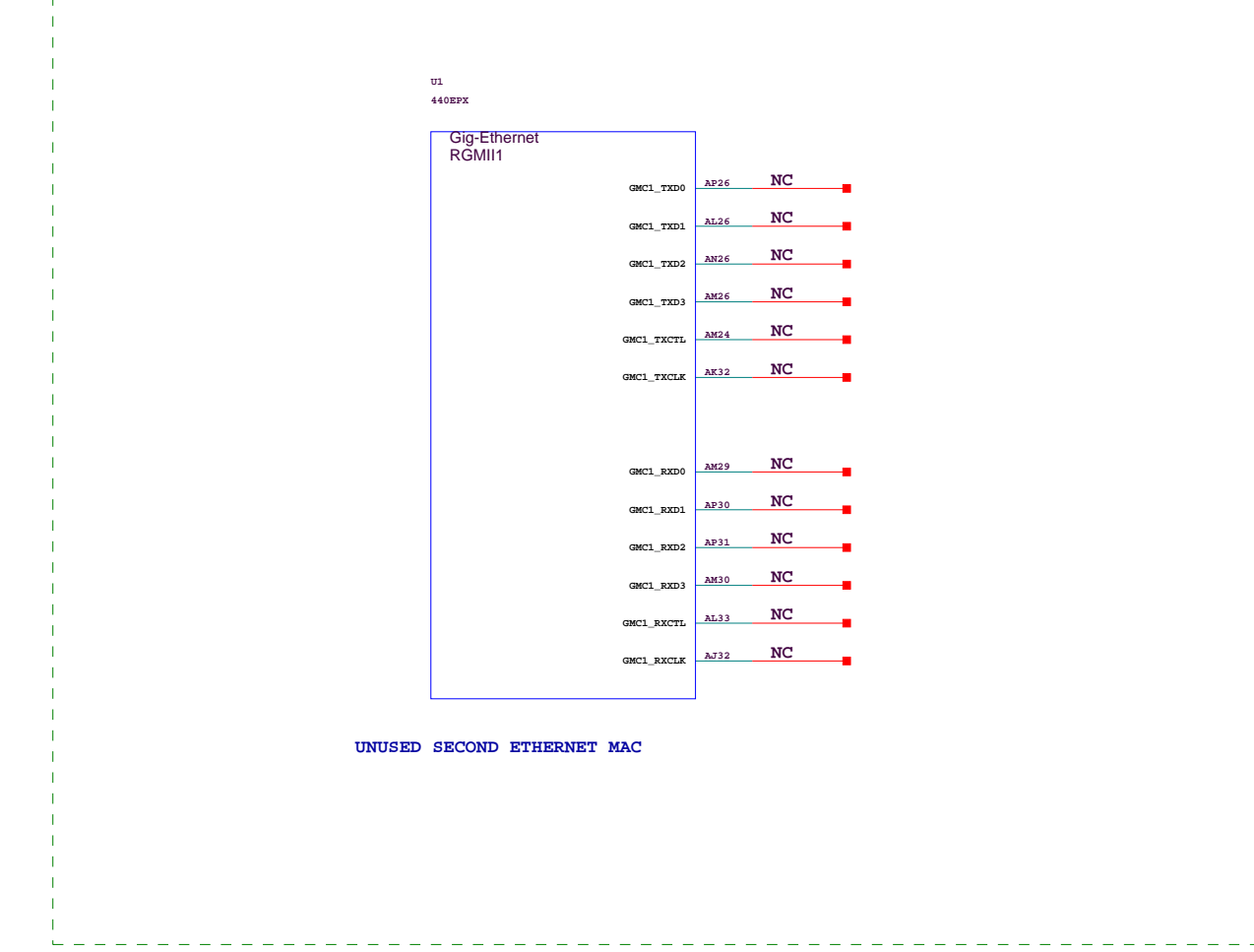
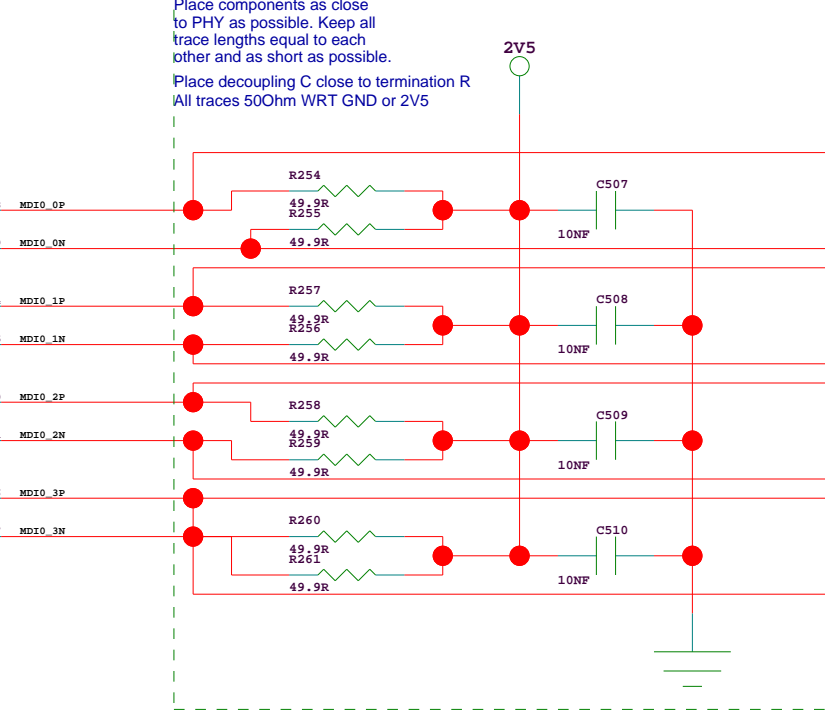
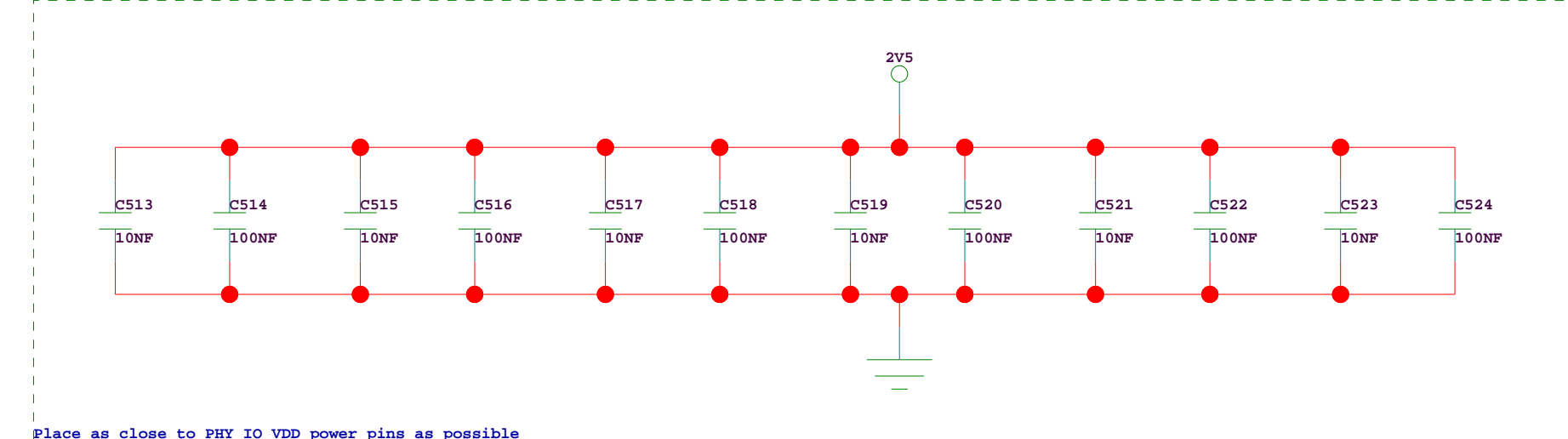
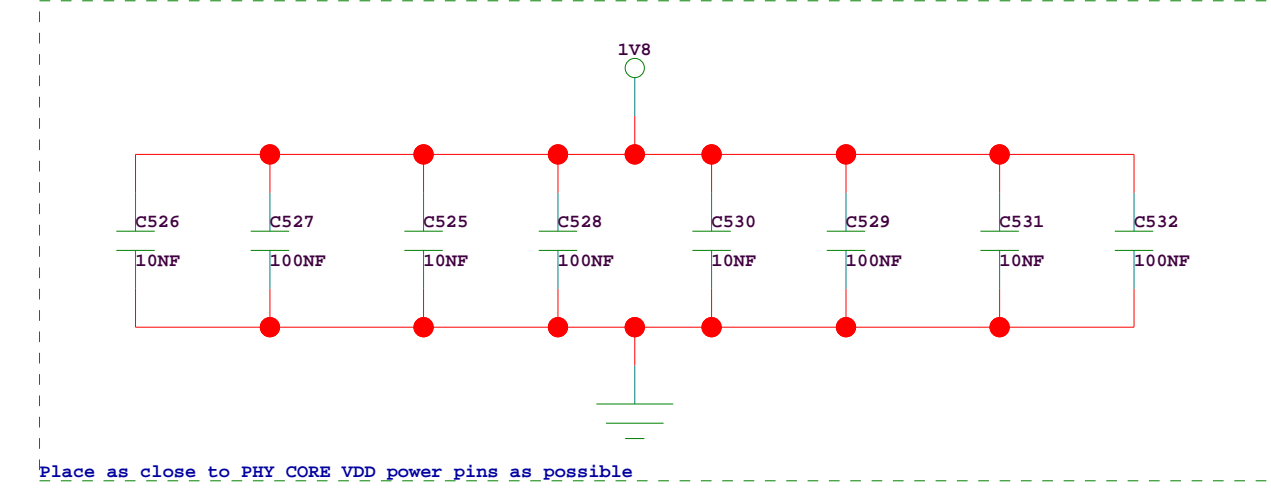
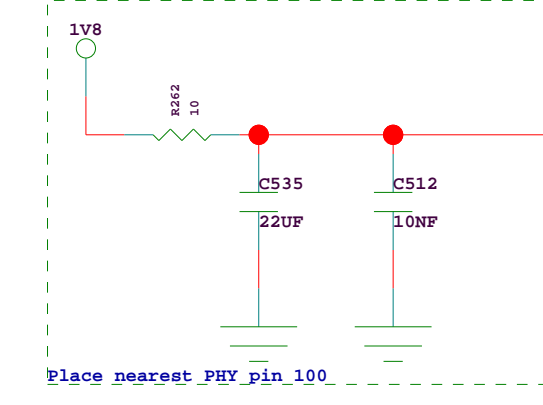
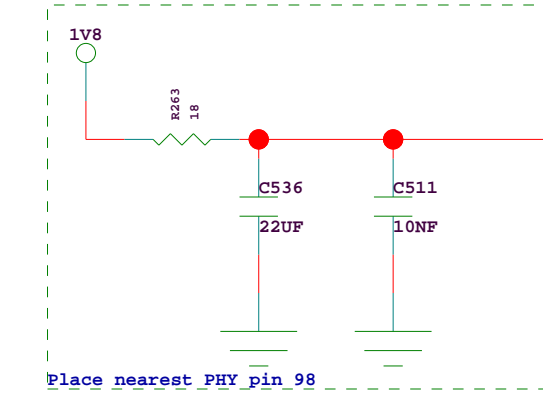
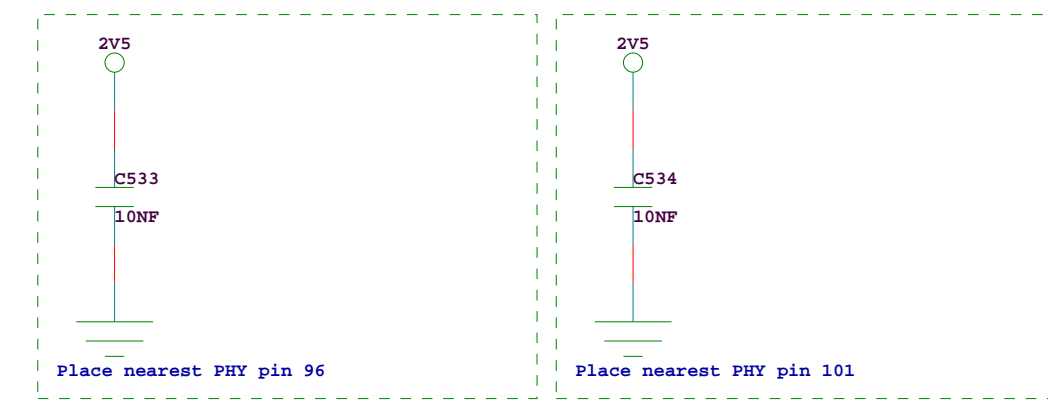
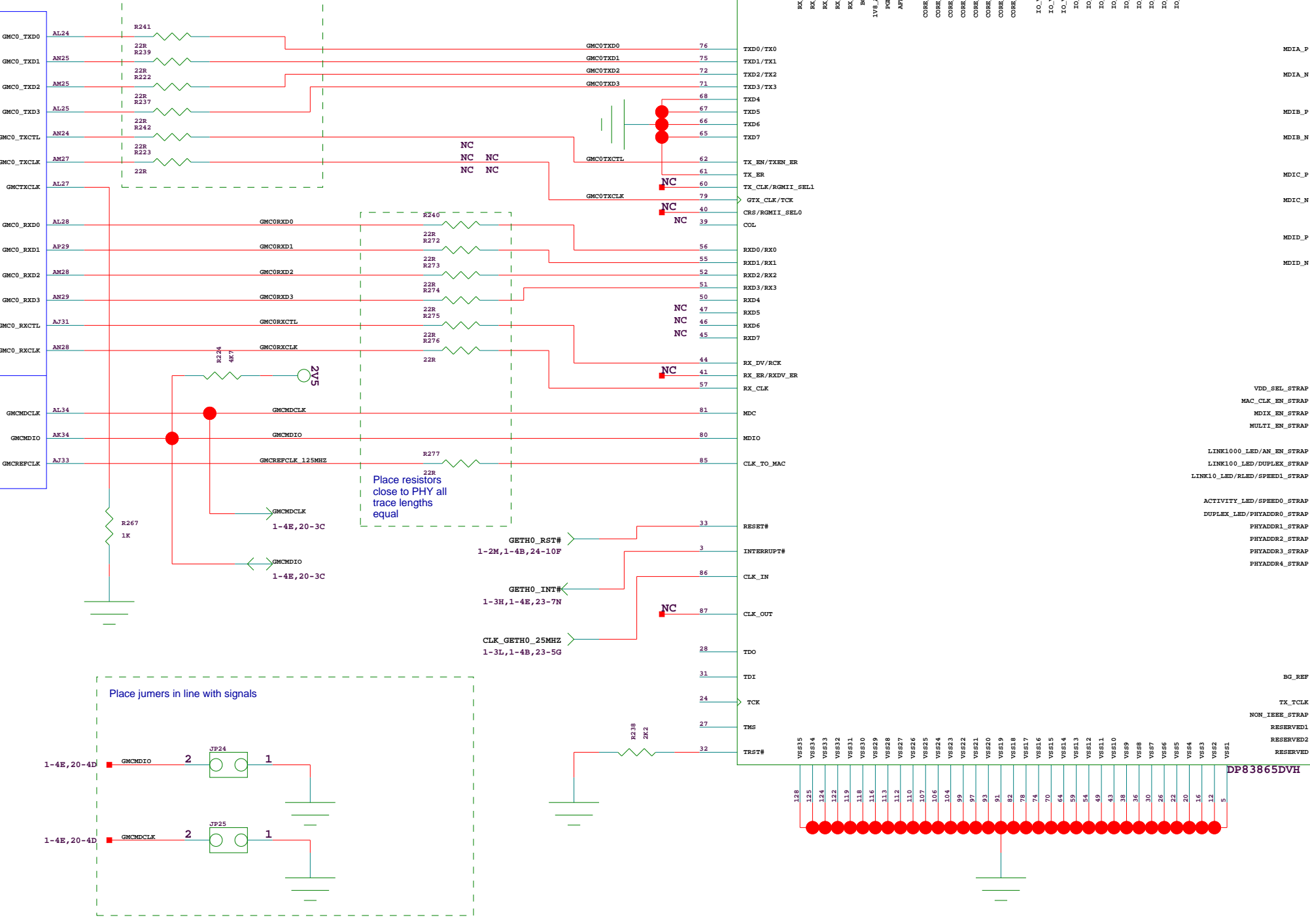
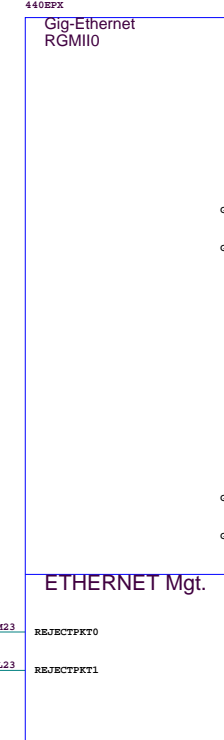
DOC NO	REVISION
NRF-ADM-XXX-SD-0001	A
DESCRIPTION	
RECONFIGURABLE OPEN ARCHITECTURE HW	
DESIGNER	APPR
F KAPP	
CHECKED	SHEET
R BAUERMEISTER	17 OF 25

A	B	C	D	E	F	G	H	J	K	L	M																		
7											7																		
6	<div>REMOVED 3V3 GENERATION</div> <div></div>										6																		
5											5																		
4	<div>REMOVED +12V GENERATION</div> <div>REMOVED -12V GENERATION</div>										4																		
3											3																		
2											2																		
1	<div>REMOVED +1V GENERATION</div> <div>REMOVED +2V5 GENERATION</div>										1																		
0	<table><tr><td colspan="2">ROACH/iBOB2</td><td colspan="2">ROACH_PPC_POWER_2</td></tr><tr><td colspan="2" rowspan="2">COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/</td><td>DOC NO NRF-ADM-XXX-SD-0001</td><td>REVISION A</td></tr><tr><td colspan="2">DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW</td></tr><tr><td colspan="2">6-4-2008_17:41</td><td>DRAWN: F KAPP</td><td>APPR: </td></tr><tr><td>PATH</td><td>PATH</td><td>CHECKED: E BAUERMEISTER</td><td>SHEET 18 OF 25</td></tr></table>										ROACH/iBOB2		ROACH_PPC_POWER_2		COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/		DOC NO NRF-ADM-XXX-SD-0001	REVISION A	DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW		6-4-2008_17:41		DRAWN: F KAPP	APPR: 	PATH	PATH	CHECKED: E BAUERMEISTER	SHEET 18 OF 25	0
ROACH/iBOB2		ROACH_PPC_POWER_2																											
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/		DOC NO NRF-ADM-XXX-SD-0001	REVISION A																										
		DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW																											
6-4-2008_17:41		DRAWN: F KAPP	APPR: 																										
PATH	PATH	CHECKED: E BAUERMEISTER	SHEET 18 OF 25																										
A	B	C	D	E	F	G	H	J	K	L	M																		

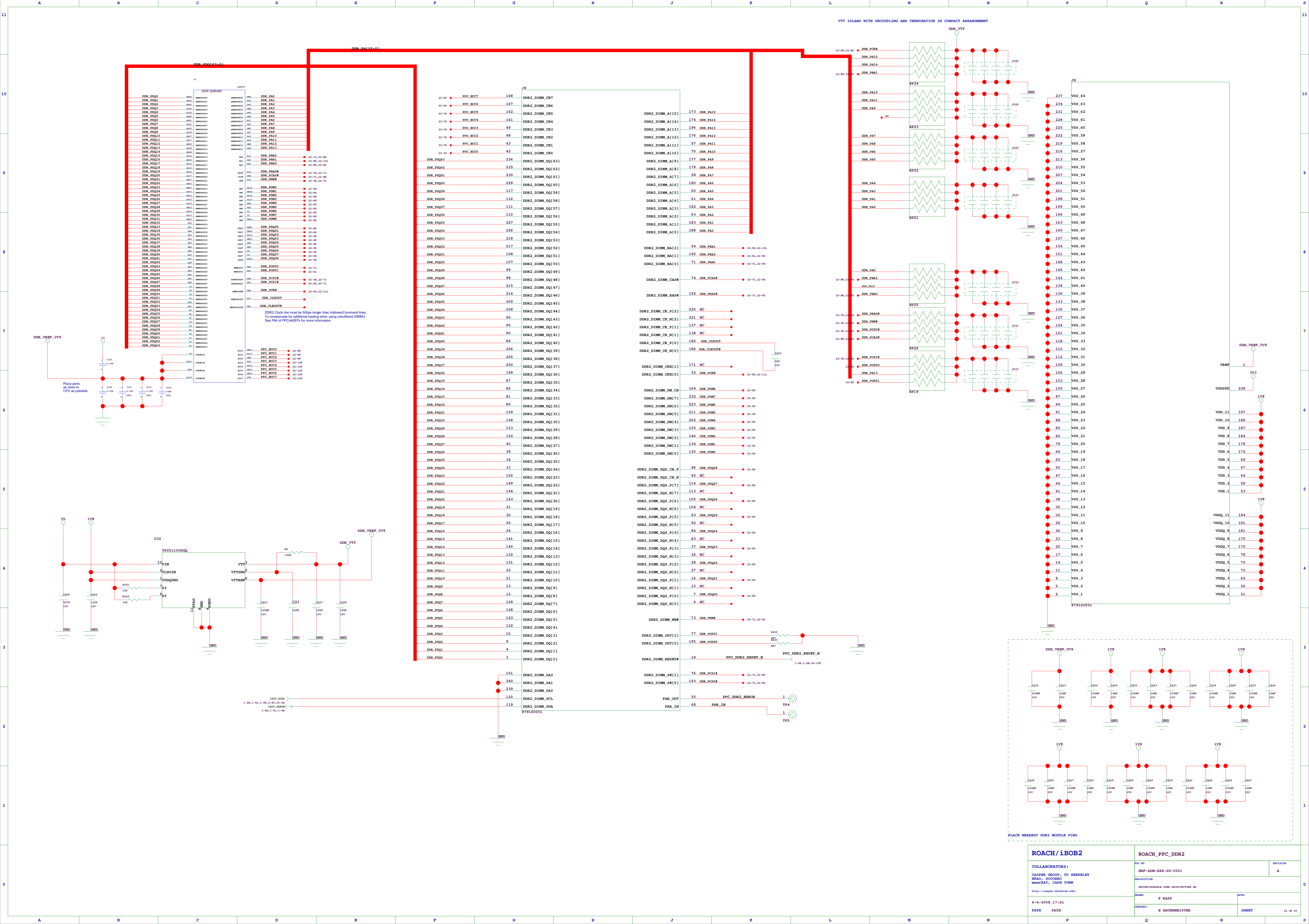
The RGMII signaling is 125 MHz using both rising and falling edges of the clock.
The Tx and the Rx side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.
Minimize the number of vias on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

U1



ROACH/iBOB2			ROACH_PPC_ETH1		
COLLABORATORS:			DOC NO	REVISION	
CASPER GROUP, UC BERKELEY NRAO, SOONERO MASCAT, CAPE TOWN			NRF-ADM-XXX-SD-0001	A	
http://casper.berkeley.edu/			DESCRIPTION		
6-4-2008_17:41			RECONFIGURABLE OPEN ARCHITECTURE HW		
PATH			NAME:	J KAPP	APP:
PATH			CHECKED:	K BAUERMEISTER	SHEET
			20 OF 25		



Critical Placement and Route
Clock Rules:

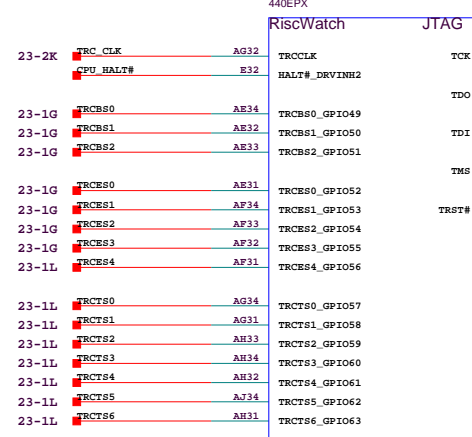
Clock Rules:
CLK_UART_11_0592MHz = as short as possible
CLK_SYS_33MHz = as short as possible
CLK_CPLD_33MHz = CLK_SYS_33MHz

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PC13_6633MHz = as short as possible
CLK_PC12_6633MHz = CLK_PC13_6633MHz
CLK_PC11_6633MHz = CLK_PC12_6633MHz + 2.5°
CLK_GETH0_25MHz = as short as possible
CLK_GETH1_25MHz = CLK_GETH0_25MHz
CLK_CPLD_50MHz = as short as possible
CLK_USB2_0_48MHz = as short as possible
CLK_USB2_0_12MHz = as short as possible

TRACE & JTAG CONNECTORS

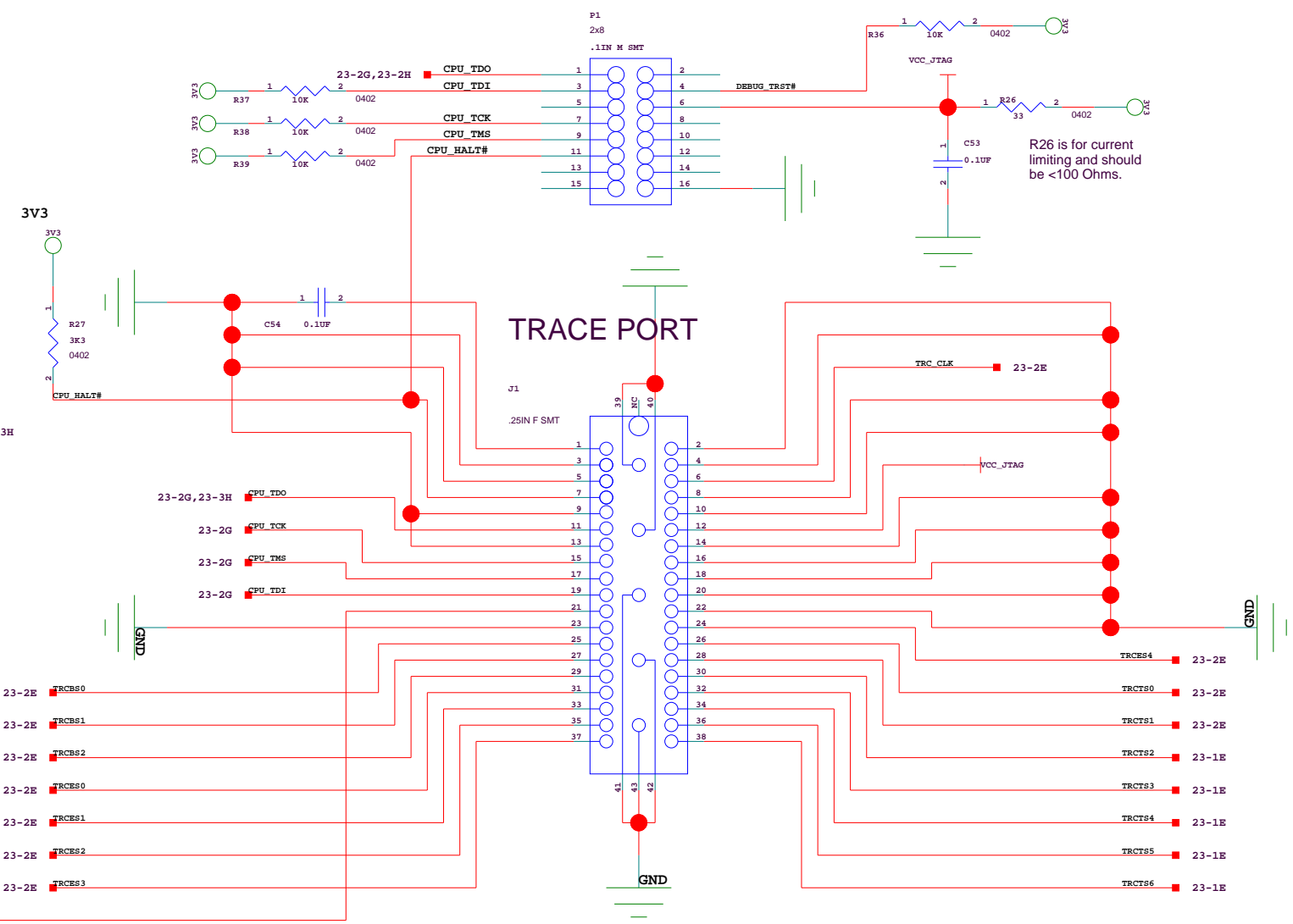
Critical placement and routing
of the Trace connector and nets.
Up to CPU frequency!



DEBUG_TRST#

1-10,1-10,10-10

TRACE PORT



ROACH/iBOE2

ROACH_PPC_TST_CLK_IO

COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOONERO
MASCAT, CAPE TOWN
<http://casper.berkeley.edu/>

DOC NO: NRP-ADM-XXX-SD-0001
REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
AUTHOR: F KAPP
CHECKED: R BAUERMEISTER
DATE: 6-4-2008 17:41
SHEET: 23 OF 25

