1.0MM PITCH DDR2
22.5 DEGREES THRU-HOLE SOCKET

(SERIES #: 87916)

Multi-Line Model Documentation

ALL DATA CONTAINED IN THIS REPORT IS **SIMULATED**. THE ACTUAL PERFORMANCE OF THE FINAL PRODUCT MAY DIFFER FROM THE INFORMATION STATED IN THIS REPORT.

HSPICE MODEL OF THE CONNECTOR; GENERATED FROM S-PARAMETER MODEL, WAS USED IN GENERATING ALL DATA REFLECTED IN THIS REPORT.

ALL EVALUATION OF THE MODEL SHOULD BE CONDUCTED AT 200ps RISETIME [10%~90%] OR SLOWER.

THE CONNECTOR MODEL IN THIS REPORT REPRESENTS A “PRODUCTION” QUALITY DESIGN WITH MOTHER BOARD AND MODULE CARD EFFECTS.

ALL INFORMATION IN THIS REPORT IS CONSIDERED MOLEX PROPRIETARY AND CONFIDENTIAL.

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Revisions

Tested / Written by : C.M. WONG
Date : 02 October 2006

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Date : 02 October 2006

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Objective

Document the high-speed electrical characteristics of 1.0 mm pitch DDR2 22.5 degrees thru-hole socket for:

- Time Domain Transmission (TDT)
  - Propagation delay
- Time Domain Reflectometry (TDR)
- Multi-line crosstalk

Conclusions

At stipulated risetime of 500ps and slower, TDR impedance of the mated interconnect system falls within 50Ω±10%, and multi-line crosstalk values are expected to stay within 10%.

Test summary of high speed electrical performance

Time domain parameter	Designated risetime [10%~90%]	Row	Connector pin no.	Simulated results		Unit
Propagation delay [10%~10%]	300ps	Lower	21	101.8		ps
			22	96.0		
		Upper	140	118.6		
			141	133.6		
	500ps	Lower	21	103.1		
			22	96.8		
		Upper	140	120.8		
			141	136.3		
TDR impedance (Z_o)				Min.	Max.	Ω
	300ps	Lower	21	48.8	50.5	
			22	48.5 (nominal)		
		Upper	140	48.8	52.6	
			141	48.9	56.2	
	500ps	Lower	21	49.3 (nominal)		
			22	49.1 (nominal)		
		Upper	140	49.6	51.0	
			141	49.6	53.1	

Time domain parameter		Designated risetime [10%~90%]	Row	Connector pin no.	Simulated results	Unit
Multi-line crosstalk (7 driven lines, 1 victim line)	NEXT	300ps	Lower	22	2.5	%
			Upper	141	16.3	
		500ps	Lower	22	1.6	
			Upper	141	10.6	
	FEXT	300ps	Lower	22	-2.0	
			Upper	141	-10.1	
		500ps	Lower	22	-1.3	
			Upper	141	-6.6	

Notes:

- All analytical tests were performed in a single ended 50Ω environment.
- All data were obtained using Piecewise Linear Source with designated risetimes of 300ps and 500ps [10%~90%].
- Signal-to-ground ratio is 2:1.
- Connector pin numbers with reference to Figure 1.

Discussion

Model Information

Molex Series Name :	1.0mm pitch DDR2 22.5 degrees thru-hole socket
HSPICE Model Filename :	mlm87916_int_revA.sp
Terminal Material :	Copper alloy
Housing Material :	High temperature thermoplastic, UL 94V-0
Modeled Pin Fields :	2 rows x 14 columns pin matrix for each model
Motherboard and Module Card Material :	FR4
Motherboard Stack Up :	Ground plane thickness = 0.03302mm PCB stack height = 0.254mm (10 mils)
Module Card Stack Up :	Ground plane thickness = 0.03302mm PCB stack height = 0.1mm (4 mils) Module pad size = 2.34mm x 0.80mm

HSPICE model node map

	Model Input		Model Output	
Connector Pin	**Node Number**	**Pin Name**	**Node Number**	**Pin Name**
16	Commoned within model			
17				
18	1	LPort1	17	LPort17
19	2	LPort2	18	LPort18
20	Commoned within model			
21	3	LPort3	19	LPort19
22	4	LPort4	20	LPort20
23	Commoned within model			
24	5	LPort5	21	LPort21
25	6	LPort6	22	LPort22
26	Commoned within model			
27	7	LPort7	23	LPort23
28	8	LPort8	24	LPort24
29	Commoned within model			
136				
137	9	LPort9	25	LPort25
138	10	LPort10	26	LPort26
139	Commoned within model			
140	11	LPort11	27	LPort27
141	12	LPort12	28	LPort28
142	Commoned within model			
143	13	LPort13	29	LPort29
144	14	LPort14	30	LPort30
145	Commoned within model			
146	15	LPort15	31	LPort31
147	16	LPort16	32	LPort32
148	Commoned within model			
149				

Notes:

- The signal configuration of the above model is $GS^{+}S^{-}$.
- All unused nodes are to be terminated with 50Ω resistors and returned to ground. Leaving the pins either open circuited or shorted to ground can result in simulation convergence issues.

Connector model

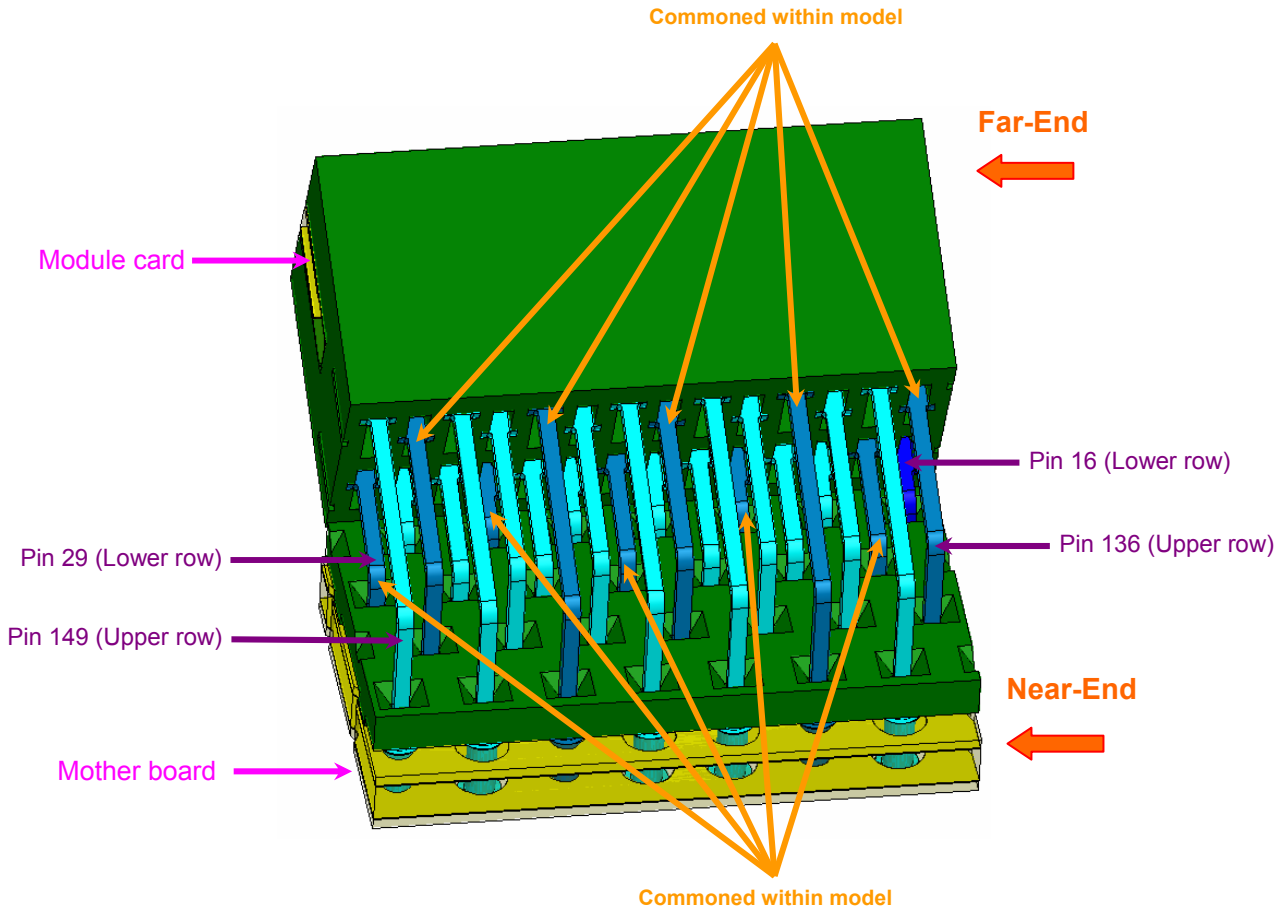

Figure 1: 3D connector model used for SPICE extraction

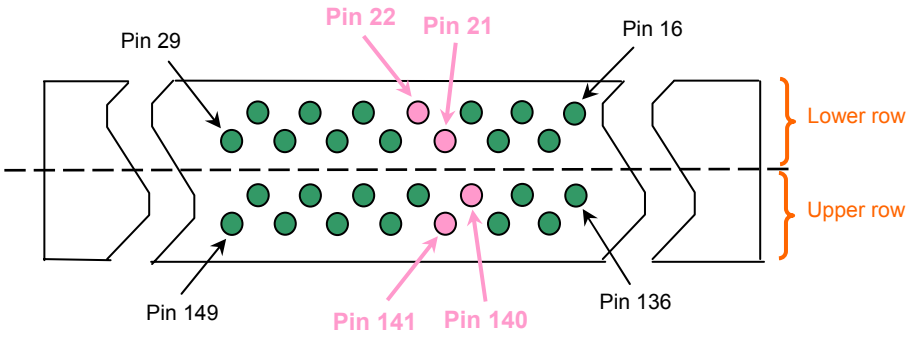

Figure 2: Connector footprint

Simulation setup

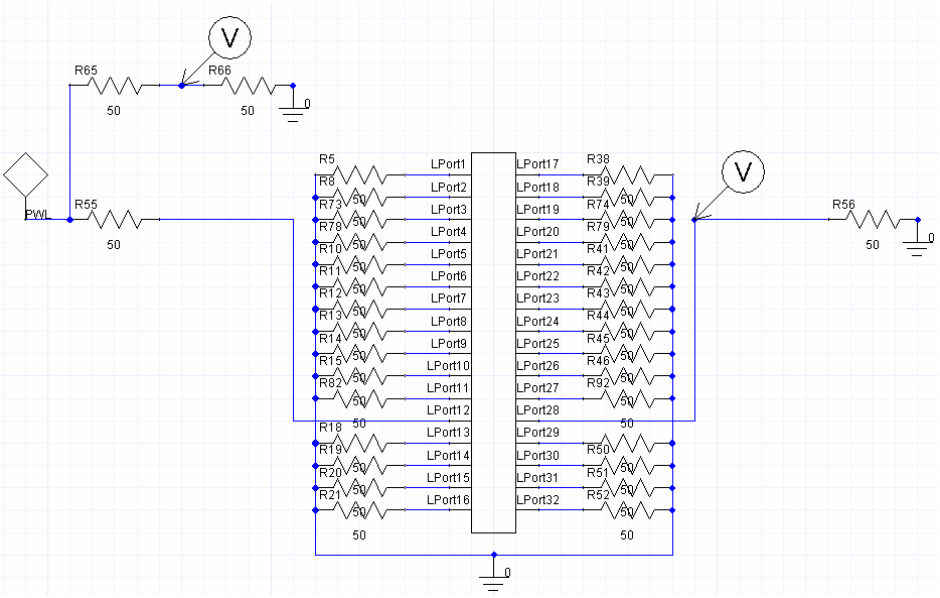

Figure 3: TDT simulation setup

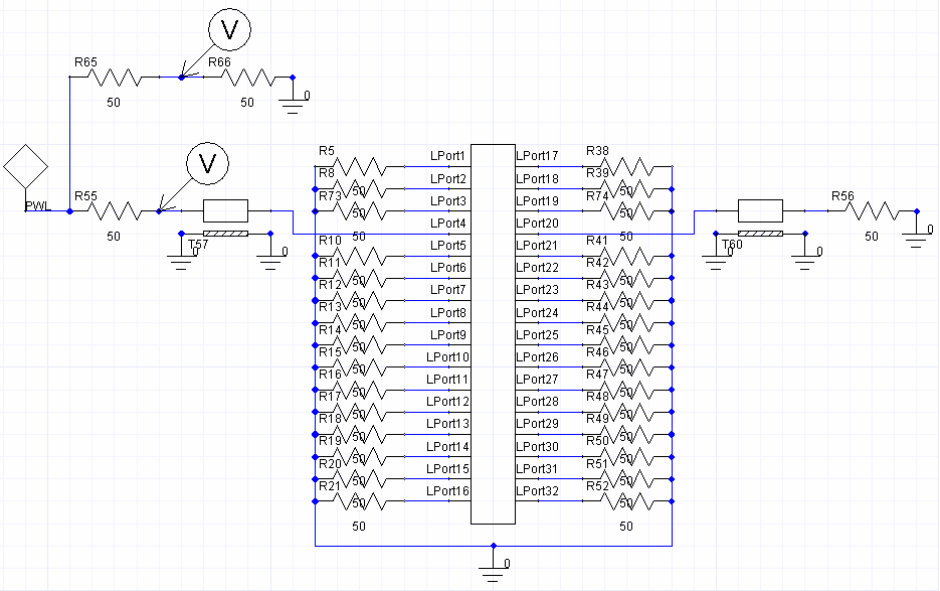

Figure 4: TDR impedance simulation setup

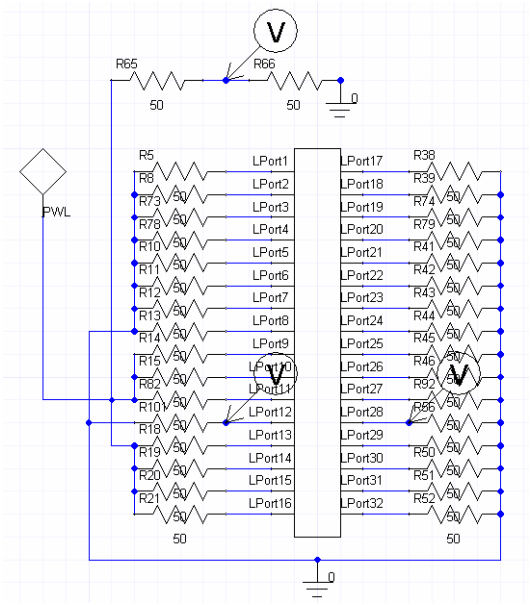

Figure 5: Multi-line crosstalk simulation setup

Time domain results

The overall high-speed electrical performance of the mated connector has been observed to improve with a slower risetime.

Due to the geometry of the connector, lower row of the connector has shorter pins than the upper row. This could be the main reason for the better high-speed performance. Compensation introduced within the system could help to further enhance the high-speed electrical performance of the interconnect solution.

Time domain charts

Propagation delay charts

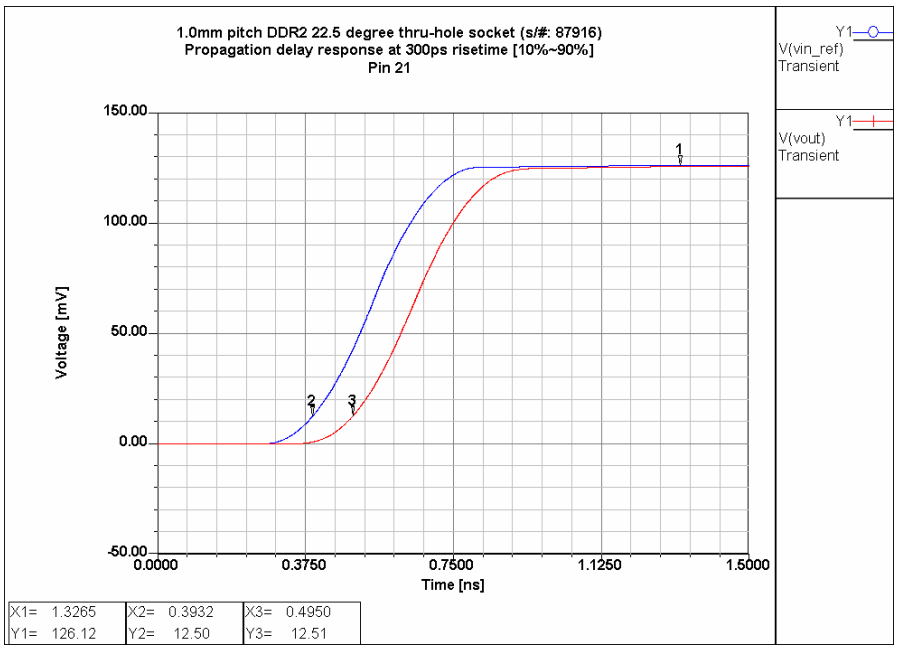

Chart 1: Propagation delay response of Pin 21 at 300ps risetime [10%~90%]

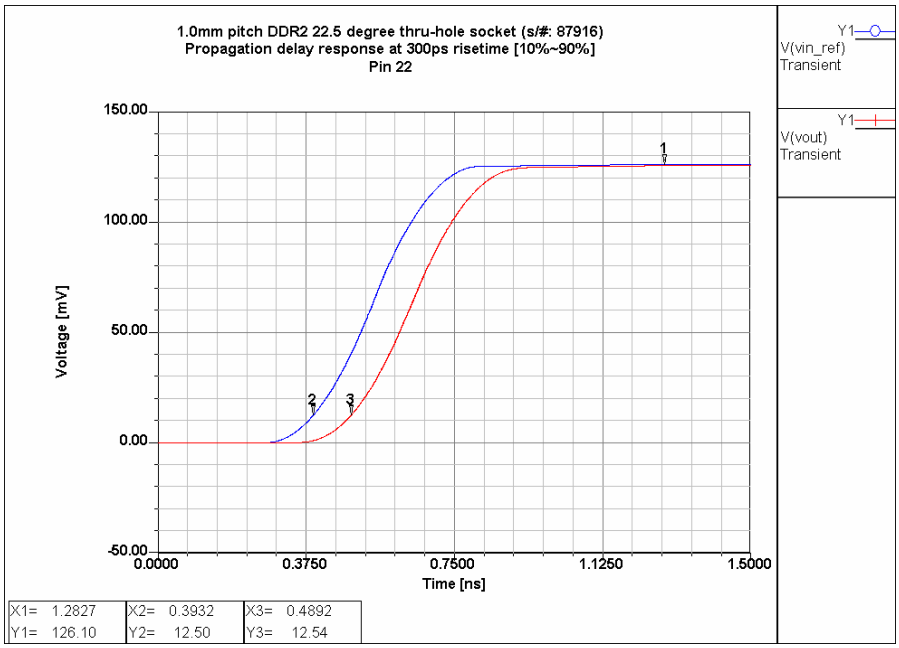

Chart 2: Propagation delay response of Pin 22 at 300ps risetime [10%~90%]

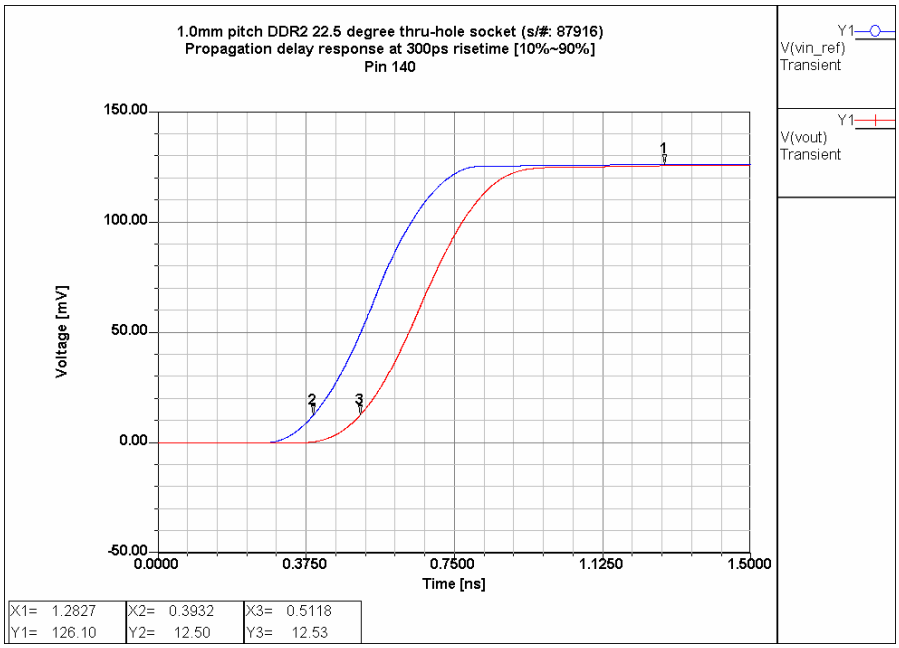

Chart 3: Propagation delay response of Pin 140 at 300ps risetime [10%~90%]

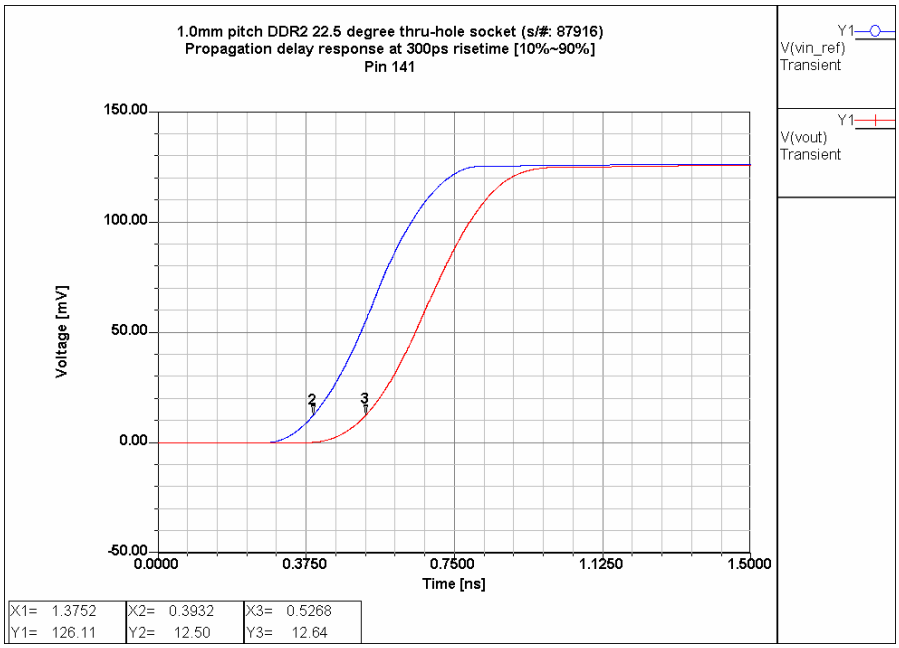

Chart 4: Propagation delay response of Pin 141 at 300ps risetime [10%~90%]

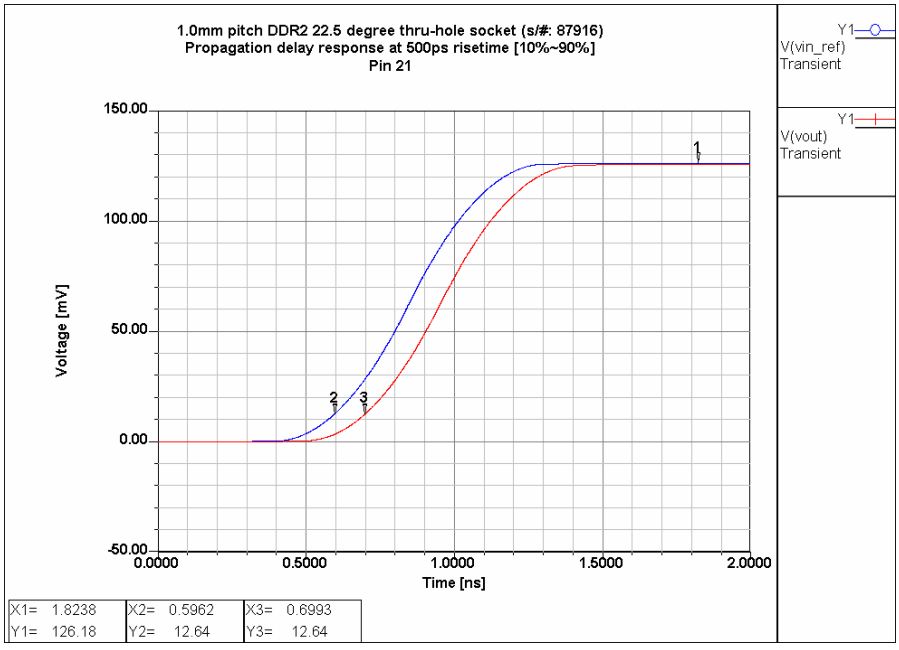

Chart 5: Propagation delay response of Pin 21 at 500ps risetime [10%~90%]

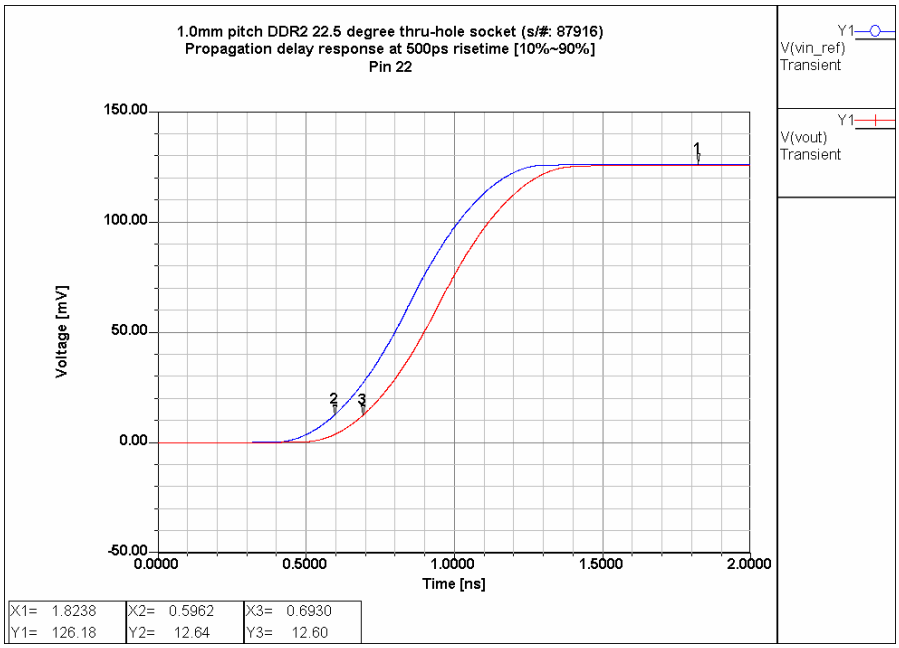

Chart 6: Propagation delay response of Pin 22 at 500ps risetime [10%~90%]

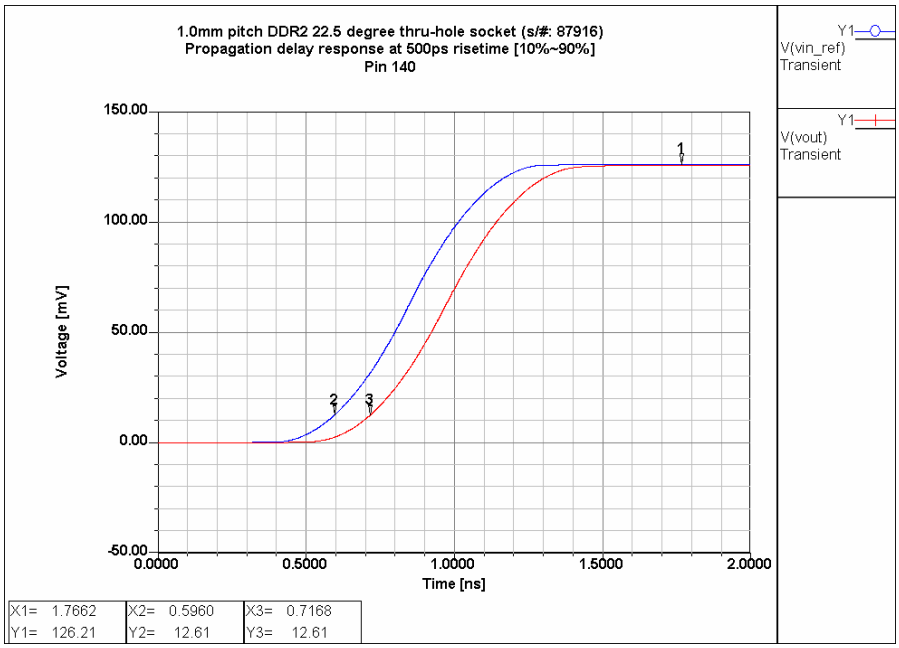

Chart 7: Propagation delay response of Pin 140 at 500ps risetime [10%~90%]

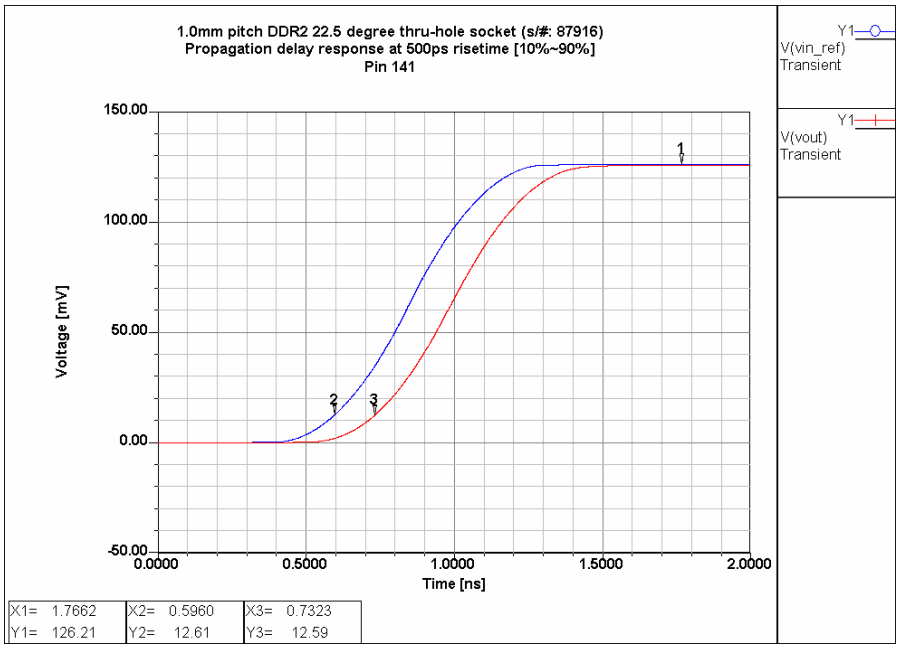

Chart 8: Propagation delay response of Pin 141 at 500ps risetime [10%~90%]

TDR impedance charts

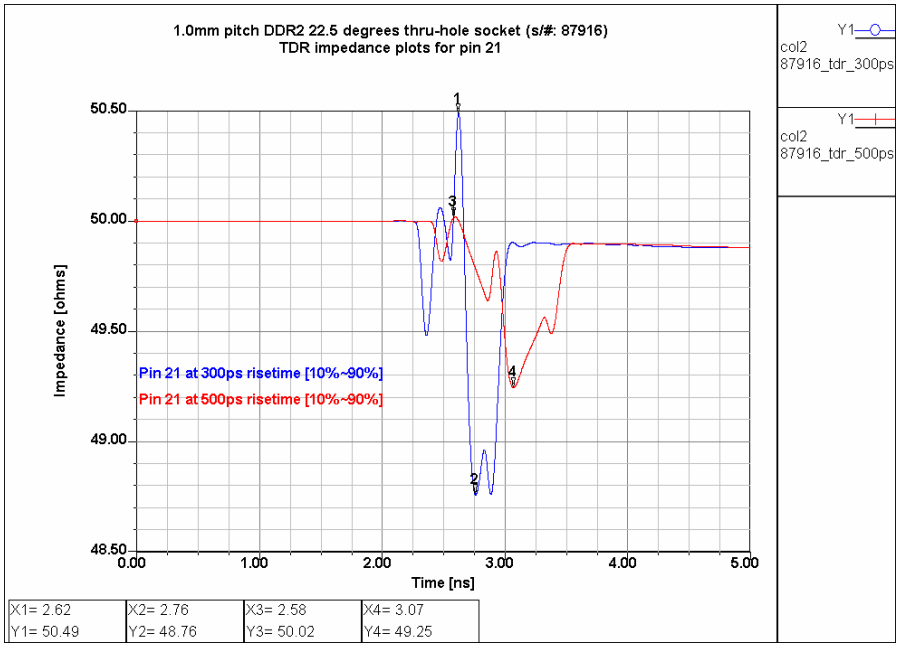

Chart 9: TDR impedance of pin 21

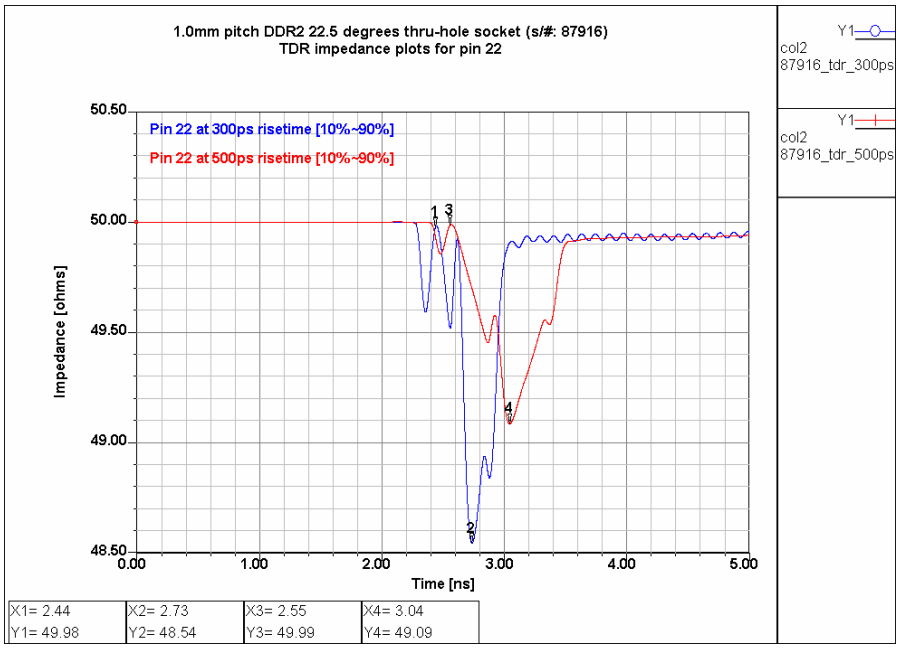

Chart 10: TDR impedance of pin 22

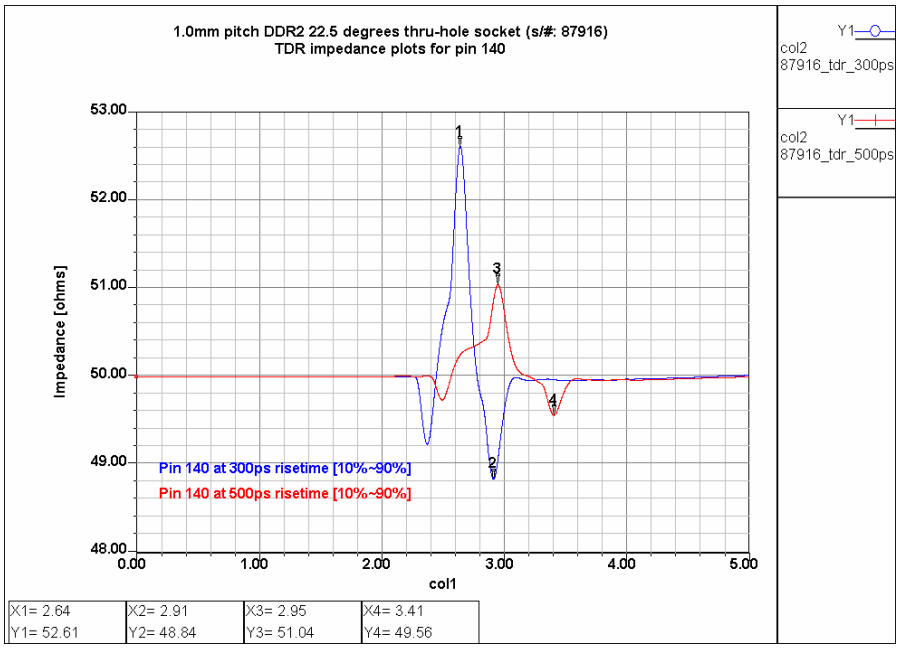

Chart 11: TDR impedance of pin 140

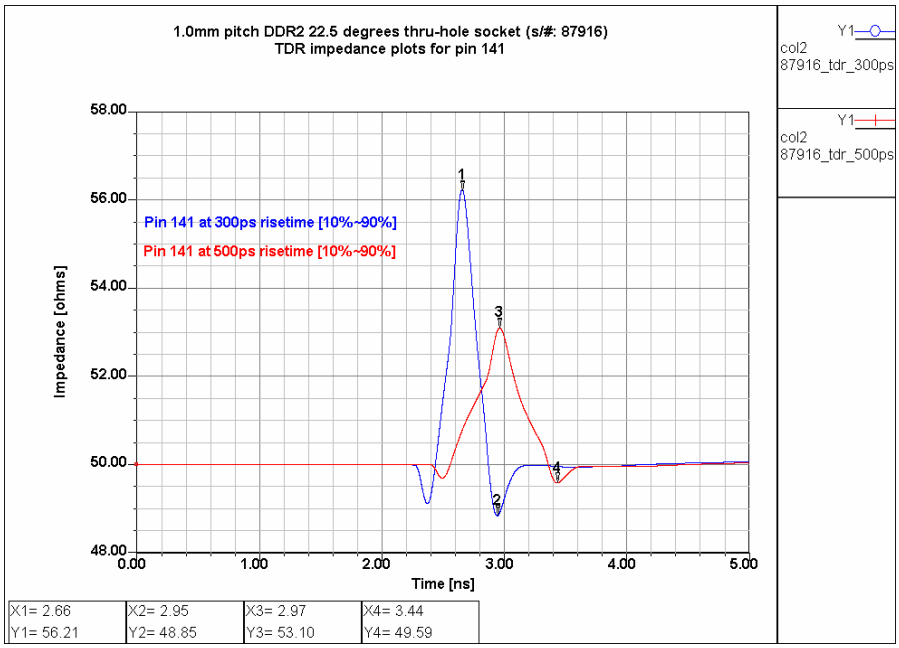

Chart 12: TDR impedance of pin 141

Multi-line crosstalk chart

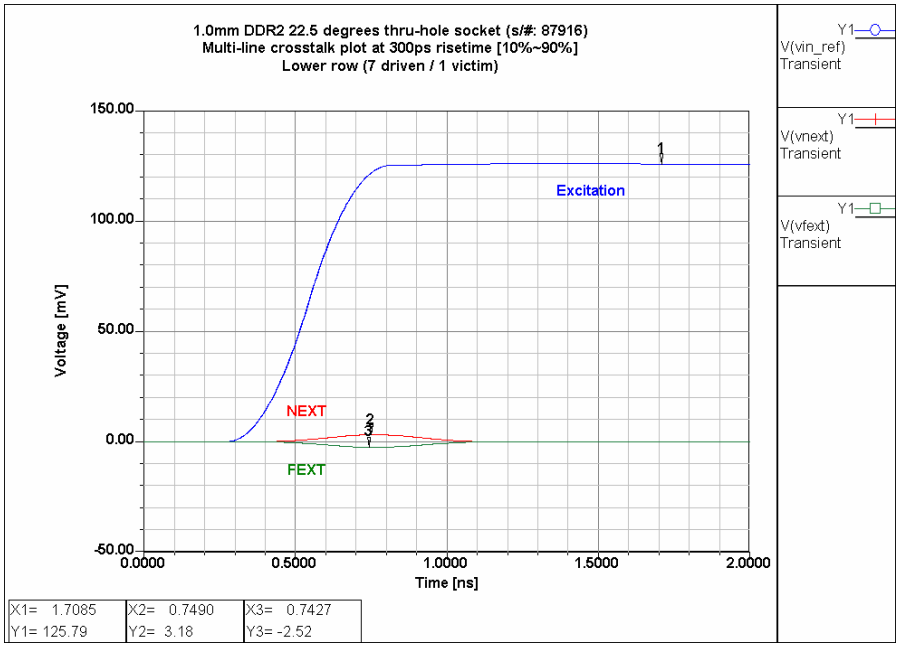

Chart 13: Multi-line crosstalk performance of lower row at 300ps risetime [10%~90%]

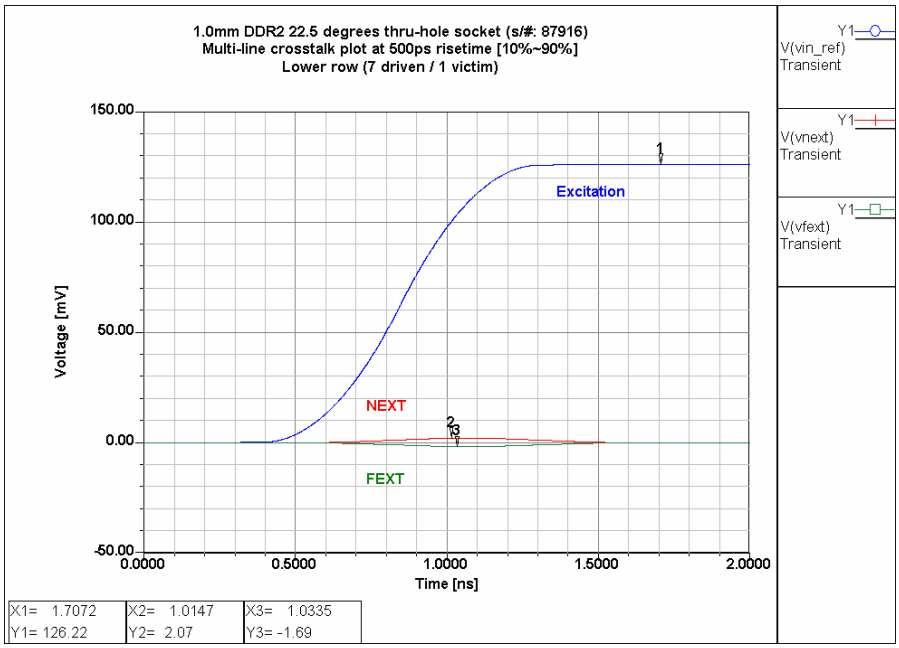

Chart 14: Multi-line crosstalk performance of lower row at 500ps risetime [10%~90%]

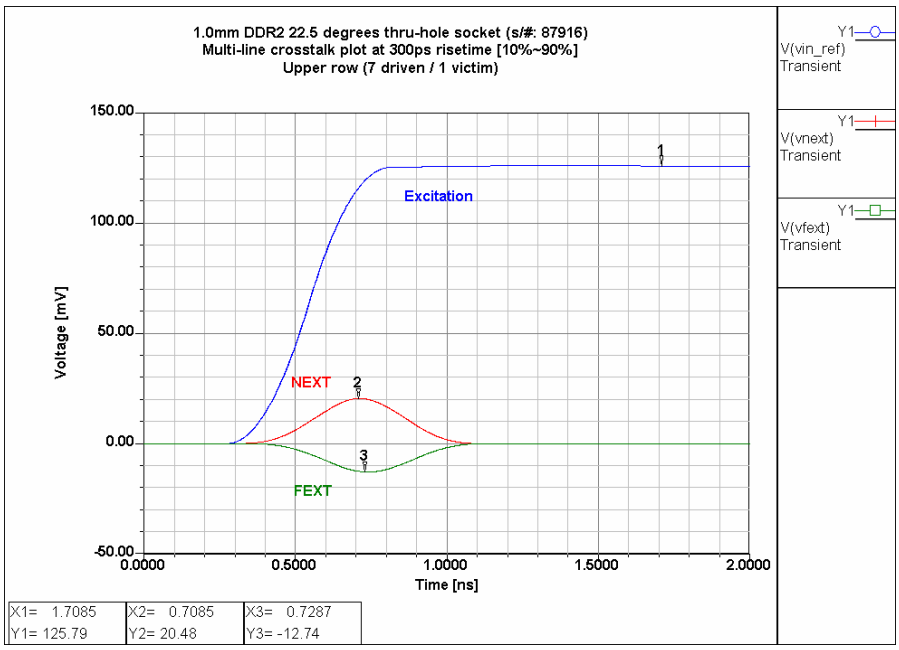

Chart 15: Multi-line crosstalk performance of upper row at 300ps risetime [10%~90%]

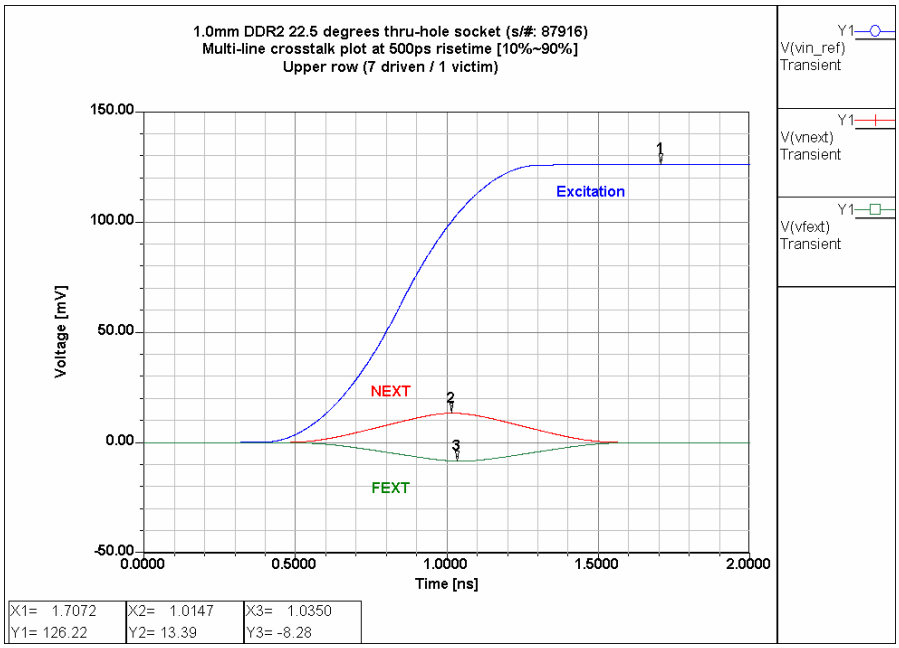

Chart 16: Multi-line crosstalk performance of upper row at 500ps risetime [10%~90%]