VIRTEX5

POWER SUPPLY AND MONITORING

ROACH_MONITOR

PPC_RESET
SYS_CONFIG[0:7]
TDI
ATRTN1
MONITOR_INT
I2C0_33_DATA
PS_ON#
ATRTN0
TDO
FAN1_CONTROL
LOAD_RES_OFF
2V5_TRACK
2V5_INHIBIT
FAN3_CONTROL
FAN2_CONTROL
MGT_AVTTX_EN
MGT_AVCCPLL_EN
MGT_AVCC_EN
1V0_INHIBIT
1V5_INHIBIT
1V0_INHIBIT

I2C0_SCLK
FAN2_SENSE
FAN1_SENSE
FAN3_SENSE
3V3_ATX
I2V5
I1V8
I1V5
I1V0
5V_ATX
MGT_AVCC_PG
MGT_AVTTX_PG
MGT_AVCCPLL_PG
PWR_OK
12V_ATX

ROACH_PSU

LOAD_RES_OFF
FAN1_CONTROL
PS_ON#
FAN2_CONTROL
FAN3_CONTROL
1V0_INHIBIT
1V5_INHIBIT
1V8_INHIBIT
2V5_TRACK
2V5_INHIBIT

12V_ATX
3V3_ATX
5V_ATX
PWR_OK
FAN1_SENSE
FAN2_SENSE
FAN3_SENSE
I1V0
I1V5
I1V8
I2V5

ROACH_5V_POWER

V5 POWER

VIRTEX5 CONFIGURATION

ROACH_CONFIG

SX95T_D_IN_0
SX95T_TCK
SX95T_TMS
CPLD_TDO
SX95T_RDWR_B_0
SX95T_PROGRAM_B_0
SX95T_CS_B_0

SX95T_M2_0
SX95T_M1_0
SX95T_M0_0
SX95T_DONE_0
SX95T_CCLK_0
SX95T_D_OUT_BUSY_0
SX95T_INIT_B_0
SX95T_TDO

ZDOK/ADC INTERFACE

ROACH_ADC_0

ROACH_ADC_1

VIRTEX5 CLOCKS

ROACH_V5_CLK

SX95T_DXN
SX95T_DXP
ATRTN0
TDO

V5 DDR2 MEMORY

ROACH_DDR2_DIMM

V5 DIFFERENTIAL GPIO

ROACH_DIFF_GPIO

V5 SE GPIO & MISCELLANEOUS

ROACH_GPIO_MISC

GIGABIT TRANSCEIVERS

ROACH_TRANSCEIVERS0_1

MGT_REFCLK_Q1_1_P
MGT_REFCLK_Q1_1_N
MGT_REFCLK_Q2_0_P
MGT_REFCLK_Q2_0_N

ROACH_TRANSCEIVERS2_3

MGT_REFCLK_Q1_1_P
MGT_REFCLK_Q1_1_N
MGT_REFCLK_Q2_0_P
MGT_REFCLK_Q2_0_N

ROACH_TRANSCEIVERS_PSU

MGT_AVCC_EN
MGT_AVCCPLL_EN
MGT_AVTTX_EN
MGT_AVCC_PG
MGT_AVTTX_PG
MGT_AVCCPLL_PG

QDRII+ MEMORY

ROACH_QDR2P_BY0_1

QDR2_TDI
QDR2_TCK
QDR2_TMS
QDR2_BY0_1_TDO

ROACH_QDR2P_BY2_3

QDR2_BY0_1_TDO
QDR2_TMS
QDR2_TCK
QDR2_BY2_3_TDO

R161 10K
R162 10K
R163 10K
R164 33R
C62 100NF 10V

PPC

ROACH_PPC_POWER_1

ROACH_PPC_POWER_2

ROACH_PPC_PCI

ROACH_PPC_ETH1

GETH0_RST#
CLK_GETH0_25MHZ
GMCMDIO
GMCMDCLK
GETH0_INT#

ROACH_PPC_USB

CONTAINS GPIO TO CONFIG INTERFACE

SX95T_D_OUT_BUSY_0
SX95T_DONE_0
SX95T_INIT_B_0
SX95T_M0_0
SX95T_M1_0
SX95T_M2_0
SX95T_PROGRAM_B_0

CLK_USB2_48MHZ

ROACH_PPC_DDR2

I2C0_SCLK
I2C0_SDATA
PPC_DDR2_RESET_N

PLACE OVER PLANE SPLIT AT BOTTOM OF PCB NEAR ADC CONNECTORS

2V5 C296 C297 C298 C299 100NF 10V
5VAUX
5V C351 C396 C397 C398 100NF 10V
1V0
3V3_ATX C417 C471 C472 C620 100NF 10V
3V3
1V8 C391 C397 C395 C394 100NF 10V
12V
1V5 C497 C498 C411 C414 100NF 10V
GND

ROACH_PPC_NVM_SERIAL

SX95T_D_IN_0
CLK_UART_11_0592MHZ
EE1_WP
STTM_AS
RESET_POR#
FWP#
EE2_BOOT_WP
BOOT_CFG0
BOOT_CFG1
BOOT_CFG2
RESET_CPLD#
PREADY

V5_INT#
SELECTMAP_CS
I2C0_SCLK
I2C0_SDATA
STTM_ALERT
POE#
FRY_BY#
CLK_PERCLK
PWBE_0#
PR_W#
PCS_2
PDATA[0:31]
PADD[2:31]
EXT_RESET#

ROACH_PPC_TST_CLK_IO

CPLD_INT
GETH0_INT#
MONITOR_INT
V5_INT#
STTM_ALERT
RESET_PB_POR#
PWR_GOOD
CPU_TRST#
CLK_SEL_M66EN
SEL_SYSCLK
CLK_TMRCLK

PPC_THERMONA
PPC_THERMONB
GPIO44
RESET_POR#
DEBUG_TRST#
CLK_GETH0_25MHZ
CLK_USB2_48MHZ
CLK_CPLD_50MHZ
SYSERR
CLK_UART_11_0592MHZ
CLK_CPLD_33MHZ

ROACH_PPC_CPLD

SX95T_TMS
SX95T_TCK
SX95T_TDO
SYS_CONFIG[0:7]
PPC_RESET
PWR_GOOD
EXT_RESET#
RESET_POR#
PWBE_0#
PADD[27:31]
SELECTMAP_CS
FRY_BY#
SYSERR
CLK_CPLD_33MHZ
DEBUG_TRST#
CLK_PERCLK
CLK_CPLD_50MHZ
PR_W#
POE#
PCS_2
SX95T_D_OUT_BUSY_0
M66EN
SX95T_M0_0
SX95T_M1_0
SX95T_M2_0

CPLD_TDO
GETH0_RST#
PPC_DDR2_RESET_N
CPLD_INT
PDATA[0:7]
RESET_PB_POR#
SX95T_CCLK_0
STTM_AS
EE2_BOOT_WP
EE1_WP
CPU_TRST#
SEL_SYSCLK
CLK_SEL_M66EN
CLK_TMRCLK
SX95T_RDWR_B_0
FWP#
RESET_CPLD#
PREADY
SX95T_INIT_B_0
SX95T_DONE_0
SX95T_PROGRAM_B_0
SX95T_D_IN_0
SX95T_CS_B_0
BOOT_CFG0
BOOT_CFG1
BOOT_CFG2

MECHANICAL

GND
H9 H10 H11

BOARD FIDUCIALS

PLACE TOP
PLACE BOTTOM
PLACE TOP ON BORDER TAB
PLACE BOTTOM ON BORDER TAB

FU1 FU2 FU3 FU4 FU5 FU6 FU7 FU8 FU9 FU10 FU11 FU12

LOGO'S

PLACEHOLDER FOR PCB MEERKAT LOGO

PLACEHOLDER FOR PCB CASPER LOGO

PLACEHOLDER FOR PCB ROACH LOGO

PLACEHOLDER FOR PCB NRAO LOGO

BOARD SERIAL NUMBER

CONTRIBUTORS

ETIENNE BAUERMEISTER
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FRANCOIS KAPP
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GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2	ROACH_TOP
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: ROACH; REVISION: 1.0.2; DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45 PATH PATH	DRAWN: F KAPP; APPR: ; CHECKED: E BAUERMEISTER; SHEET 1 OF 25

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

TIE TO GROUND IF PLL'S ARE NOT USED

PLACE AT ACTEL 1V5 POWER PINS

PLACE AT ACTEL 3V3 POWER PINS

roach_AFS600_powerpins

roach_AFS600_configpins

roach_AFS600_pcb

PB POWER SWITCH

KEY - REMOVE PIN

MONITOR RESET

XPORT - PLACE IN REAR I/O REGION

TEMPERATURE DIODE HEADER

ACTEL JTAG CONNECTOR

REFERENCE RESISTOR/ADC VALUES

VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)	FOR 8 BIT ADC USING 2.56V REFERENCE: ADC COUNT AT MAX POWER	CURRENT/BIT (A)
12V	0R01	3.36	0.11	33	0.1
5V	0R0047	6.78	0.22	31	0.21
3V3	0R01	3.47	0.12	34	0.1
2V5	0R01	3.56	0.13	35	0.1
1V8	0R0022	12.91	0.37	28	0.45
1V5	0R0047	6.77	0.22	31	0.21
1V0	0R001	26.79	0.72	26	1.0

ROACH/iBOB2	ROACH_MONITOR
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A; DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45; PATH PATH	DRAWN: F KAPP; APPR:; CHECKED: E BAUERMEISTER; SHEET 2 OF 25

AUX FAN CONNECTORS - ATX 4 PIN

FAN1_SENSE 1-9E,1-10B,2-3R
FAN1_CONTROL 1-9B,1-10E,2-3R
FAN2_SENSE 1-9E,1-10B,2-3R
FAN2_CONTROL 1-9B,1-10E,2-3J
FAN3_SENSE 1-9E,1-10B,2-3R
FAN3_CONTROL 1-9B,1-10E,2-3J

U64 U7 U52 U39 U49 U47 — OC BUF SN74LVC1G07DBVT

R175 R174 R173 4K7

PTC4 PTC3 PTC2 MF-NSMF050-2 500MA/13.2V

J21 J20 J19 — 47053-1000 — PLACE ON SILKSCREEN: FAN1 / FAN2 / FAN3

1 GND, 2 12V, 3 SENSE, 4 CONTROL

3V3AUX

R192 R191 R190 4K7

D12 D11 D10 BZX84C3V3LT1 3V3

ATX POWER CONNECTORS

J18 — 44206-0007

1	3V3_1	3V3_4	13
2	3V3_2	_12V	14
3	COM_1	COM_4	15
4	5V_1	PS_ON#	16
5	COM_2	COM_5	17
6	5V_2	COM_6	18
7	COM_3	COM_7	19
8	PWR_OK	N/C	20NC
9	5VSB	5V_3	21
10	12V1_1	5V_4	22
11	12V1_2	5V_5	23
12	3V3_3	COM_8	24

PS_ON# 1-9B,1-10E,2-8B

J32 — 8510-4500PL

PWR_OK 1-9B,1-9E,2-8B

5VAUX

5V_ATX 1-9E,1-10B,2-4A

3V3_ATX 1-9E,1-10B,2-3A

12V_ATX 1-9B,1-9E,2-6B

N12V

BOARD LAYOUT NOTE
SEPARATE GROUND RETURN CURRENTS FROM MAIN BOARD GROUND PLANES
BETWEEN POWER INPUT CONNECTORS AND REGULATOR AREA ON BOARD.

LOAD RESISTORS FOR ATX PSU MIN LOAD
SWITCH OFF ONCE LOAD EXCEEDS MINIMUM SPEC
ADJUST RESISTOR VALUES FOR ACTUAL SUPPLY

5VAUX — R180 10R — Q9 NDS331N — R185 10R 5W AC05000001009JLB00

LOAD_RES_OFF 1-9B,1-10E,2-6B — Q8 BSS138 — R181 10K

Q10 NDS331N — R187 56R 5W AC05000005609JLB00

GND

PSU INPUT SUMMARY

VOLTAGE	5.0V +- 10%
CURRENT (MAX)	6.0A

5V

L6 L5 L16 BLM31PG121SN1B

C403 330UF 16V — C401 330UF 16V — C419 22UF 16V

1V0 — ROUTE FROM LOAD — R144 68

PLACE RESISTOR CLOSE TO U50
ROUTE SHORTEST

U50 — 30A SMPS MODULE — PTH05T210WAD

TURBOTRANS, SENSE+, VI_1, VI_0, INHIBIT/UVLADJ, TRACK, SENSE-

GND_3, GND_2, GND_1, GND_0

VO_0, VO_1 — I1V0 1-9E,1-10B,2-1B

VOADJUST — R143 634K — DIRECT TO P8 ON U50, DEDICATED TRACE

C418 10UF — C117 10UF — C402 100UF 2V5 — C400 100UF 2V5 — C104 100UF 2V5 — C105 100UF 2V5

1V0_INHIBIT 1-9B,1-9E,2-6B — Q4 BSS138 — ROUTE FROM LOAD

PSU RAIL SUMMARY

VOLTAGE	1.0V +- 5%
SUPPLIES	FPGA CORE
CURRENT (QUIESCENT)	1.5A
CURRENT (ACTIVE)	26.8A
LOAD STEP	25.3A

1.2V SUPPLY DELETED - NOT REQUIRED

PSU INPUT SUMMARY

VOLTAGE	12V +- 10%
CURRENT (MAX)	0.8A

12V — L7 BLM31PG121SN1B — C404 330UF 16V — C420 22UF 16V

1V8 — ROUTE FROM LOAD — R146 24K9

PLACE RESISTOR CLOSE TO US1
ROUTE SHORTEST

U51 — 16A SMPS MODULE — PTH08T240WAD

TURBOTRANS, SENSE+, VI, INHIBIT/UVLADJ, TRACK, SENSE-, SMARTSYNC

GND_1, GND_0

VO — I1V5 1-9E,1-10B,2-2B

VOADJUST — R147 649R — DIRECT TO P8 ON US1, DEDICATED TRACE

C421 10UF — C405 1000UF 2V5

1V5_INHIBIT 1-9B,1-9E,2-1B — Q5 BSS138 — ROUTE FROM LOAD

PSU RAIL SUMMARY

VOLTAGE	1.5V +- 5%
SUPPLIES	FPGA IO, QDR, FPC
CURRENT (QUIESCENT)	0.25A
CURRENT (ACTIVE)	6.8A
LOAD STEP	6.55A

2V5 — ROUTE FROM LOAD — R10 22R

PLACE RESISTOR CLOSE TO U53
ROUTE SHORTEST

2V5_TRACK 1-9B,1-10B,2-6B — R183 1K — R177 845R

C426 10UF — C424 22UF 16V — C412 330UF 16V — L15 BLM31PG121SN1B

U53 — PTH08T230WAD

TURBOTRANS, SENSE+, VI, INHIBIT/UVLADJ, TRACK, SENSE-, SMARTSYNC

GND_0

VO — I2V5 1-9E,1-10B,2-2B

VOADJUST — R179 2K87 — DIRECT TO P8 ON U53, DEDICATED TRACE

C425 10UF 16V — C413 680UF 4V

2V5_INHIBIT 1-9B,1-10E,2-1B — Q7 BSS138 — ROUTE FROM LOAD

PSU INPUT SUMMARY

VOLTAGE	12V +- 10%
CURRENT (MAX)	1.8A

12V — L14 BLM31PG121SN1B — C409 330UF 16V — C423 22UF 16V

1V8 — ROUTE FROM LOAD — R149 24K9

PLACE RESISTOR CLOSE TO US2
ROUTE SHORTEST

U27 — 16A SMPS MODULE — PTH08T220WAD

TURBOTRANS, SENSE+, VI, INHIBIT/UVLADJ, TRACK, SENSE-, SMARTSYNC

GND_1, GND_0

VO — I1V8 1-9E,1-10B,2-2B

VOADJUST — R148 487R — DIRECT TO P8 ON PTH08T210W, DEDICATED TRACE

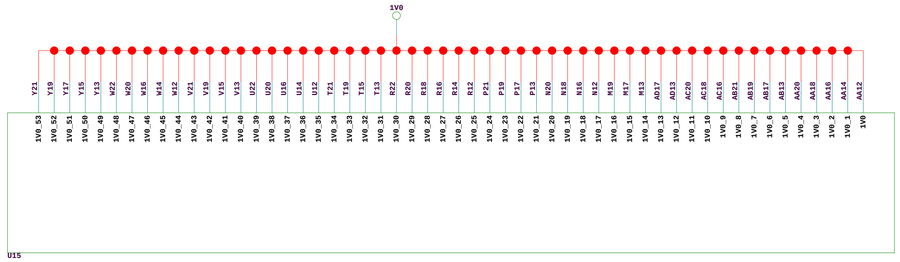
C422 10UF — C410 1000UF 2V5

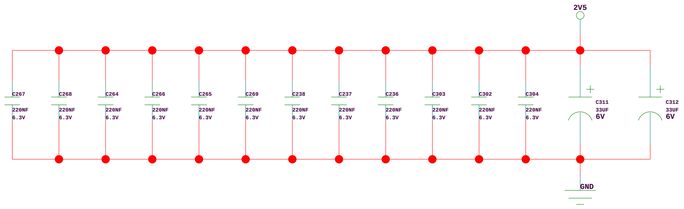
1V8_INHIBIT 1-9B,1-10E,2-1B — Q6 BSS138 — ROUTE FROM LOAD

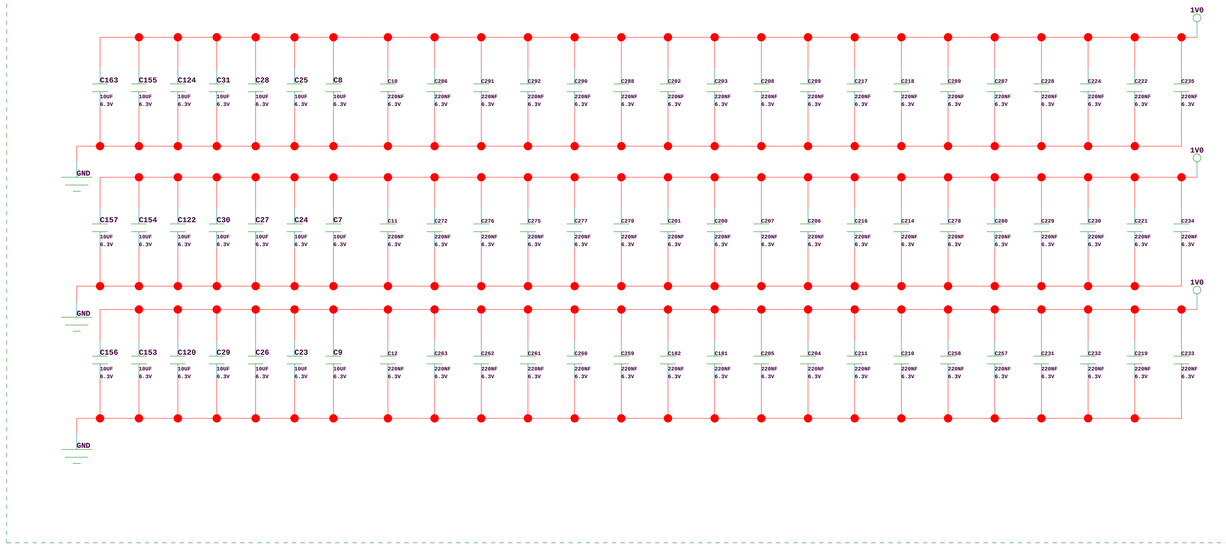
PSU RAIL SUMMARY

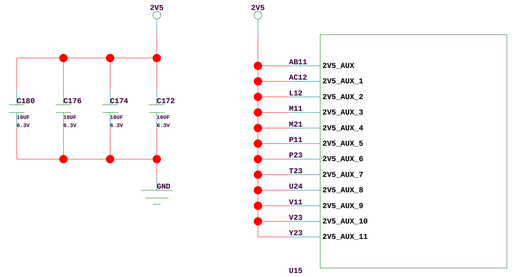
VOLTAGE	1.8V +- 5%
SUPPLIES	FPGA IO, DDR2 x 2
CURRENT (QUIESCENT)	1A
CURRENT (ACTIVE)	12.9A
LOAD STEP	11.9A

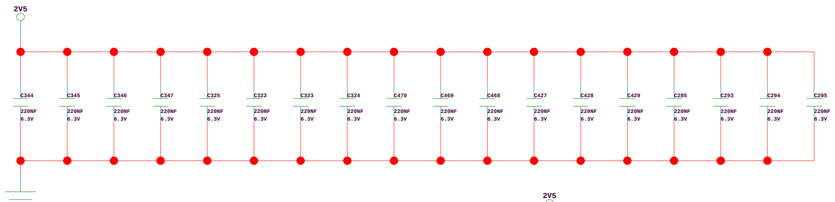
ROACH/iBOB2	ROACH_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 3 OF 25

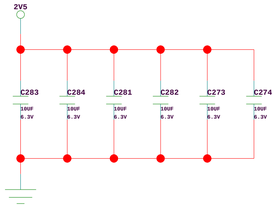


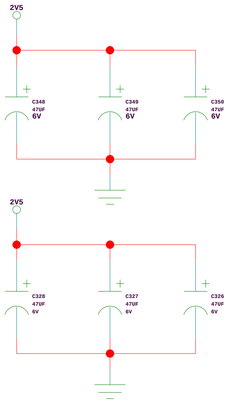


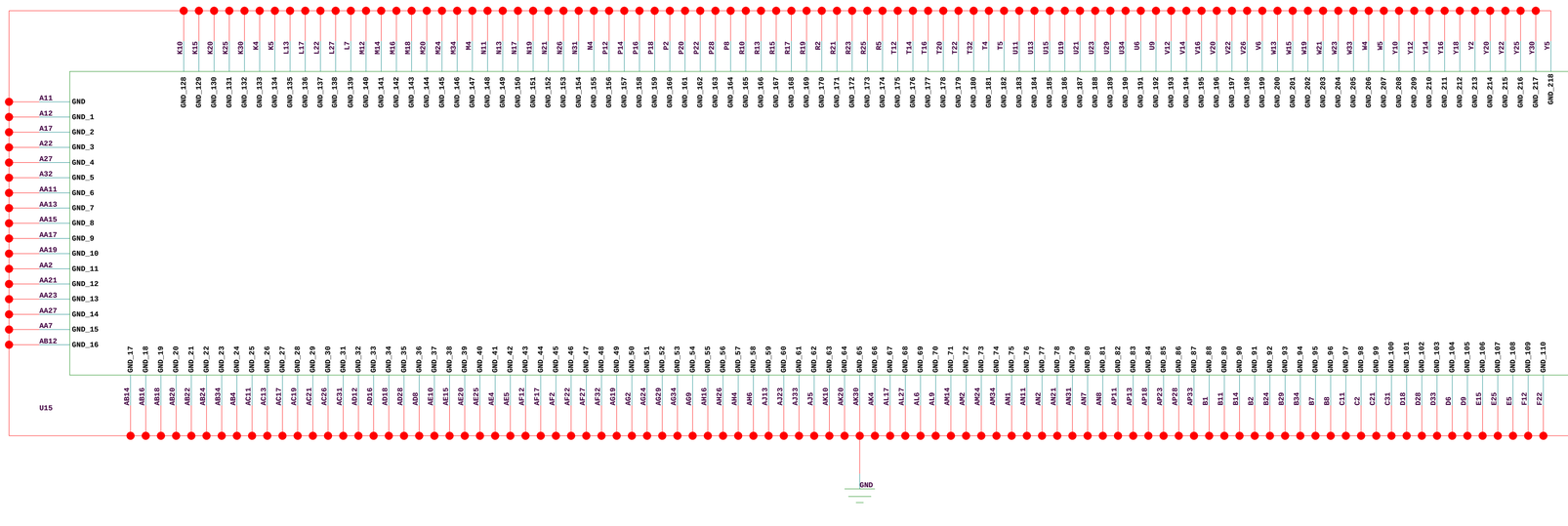












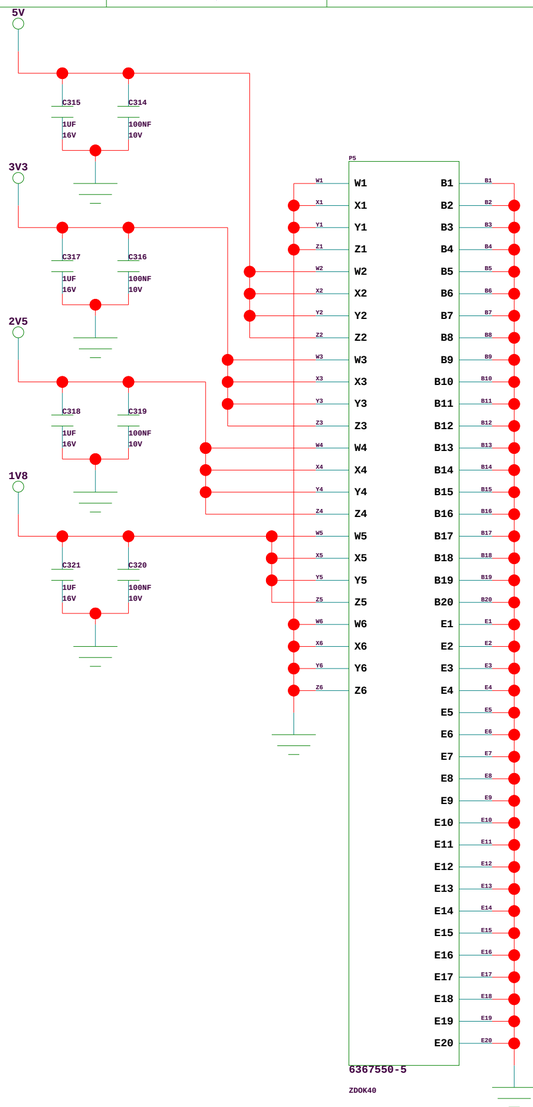
ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
11-27-2008_13:45 PATH PATH	

5-5L	ZDOK0_CLK0_P	J20	ZDOK0_CLK0_P
5-5L	ZDOK0_CLK0_N	J21	ZDOK0_CLK0_N
5-3L	ZDOK0_CLK1_P	H19	ZDOK0_CLK1_P
5-3L	ZDOK0_CLK1_N	H20	ZDOK0_CLK1_N

ZDOK0_DP_P[37]	B33	ZDOK0_DP_P37	5-3L
ZDOK0_DP_N[37]	C33	ZDOK0_DP_N37	5-3L
ZDOK0_DP_P[36]	F25	ZDOK0_DP_P36	5-3L
ZDOK0_DP_N[36]	F26	ZDOK0_DP_N36	5-3L
ZDOK0_DP_P[35]	E32	ZDOK0_DP_P35	5-4L
ZDOK0_DP_N[35]	E33	ZDOK0_DP_N35	5-4L
ZDOK0_DP_P[34]	F33	ZDOK0_DP_P34	5-4L
ZDOK0_DP_N[34]	E34	ZDOK0_DP_N34	5-4L
ZDOK0_DP_P[33]	G32	ZDOK0_DP_P33	5-4L
ZDOK0_DP_N[33]	H32	ZDOK0_DP_N33	5-4L
ZDOK0_DP_P[32]	J27	ZDOK0_DP_P32	5-4L
ZDOK0_DP_N[32]	J26	ZDOK0_DP_N32	5-4L
ZDOK0_DP_P[31]	H34	ZDOK0_DP_P31	5-4L
ZDOK0_DP_N[31]	J34	ZDOK0_DP_N31	5-4L
ZDOK0_DP_P[30]	K31	ZDOK0_DP_P30	5-5L
ZDOK0_DP_N[30]	L31	ZDOK0_DP_N30	5-5L
ZDOK0_DP_P[29]	L30	ZDOK0_DP_P29	5-5L
ZDOK0_DP_N[29]	M30	ZDOK0_DP_N29	5-5L
ZDOK0_DP_P[28]	C34	ZDOK0_DP_P28	5-5L
ZDOK0_DP_N[28]	D34	ZDOK0_DP_N28	5-5L
ZDOK0_DP_P[27]	E29	ZDOK0_DP_P27	5-5L
ZDOK0_DP_N[27]	F29	ZDOK0_DP_N27	5-5L
ZDOK0_DP_P[26]	H25	ZDOK0_DP_P26	5-6L
ZDOK0_DP_N[26]	H24	ZDOK0_DP_N26	5-6L
ZDOK0_DP_P[25]	G30	ZDOK0_DP_P25	5-6L
ZDOK0_DP_N[25]	F30	ZDOK0_DP_N25	5-6L
ZDOK0_DP_P[24]	G33	ZDOK0_DP_P24	5-6L
ZDOK0_DP_N[24]	F34	ZDOK0_DP_N24	5-6L
ZDOK0_DP_P[23]	J30	ZDOK0_DP_P23	5-6L
ZDOK0_DP_N[23]	J31	ZDOK0_DP_N23	5-6L
ZDOK0_DP_P[22]	L25	ZDOK0_DP_P22	5-6L
ZDOK0_DP_N[22]	L26	ZDOK0_DP_N22	5-6L
ZDOK0_DP_P[21]	L29	ZDOK0_DP_P21	5-7L
ZDOK0_DP_N[21]	K29	ZDOK0_DP_N21	5-7L
ZDOK0_DP_P[20]	N27	ZDOK0_DP_P20	5-7L
ZDOK0_DP_N[20]	M27	ZDOK0_DP_N20	5-7L
ZDOK0_DP_P[19]	B32	ZDOK0_DP_P19	5-3J
ZDOK0_DP_N[19]	A33	ZDOK0_DP_N19	5-3J
ZDOK0_DP_P[18]	E26	ZDOK0_DP_P18	5-3J
ZDOK0_DP_N[18]	E27	ZDOK0_DP_N18	5-3J
ZDOK0_DP_P[17]	G25	ZDOK0_DP_P17	5-3J
ZDOK0_DP_N[17]	G26	ZDOK0_DP_N17	5-3J
ZDOK0_DP_P[16]	G27	ZDOK0_DP_P16	5-4J
ZDOK0_DP_N[16]	H27	ZDOK0_DP_N16	5-4J
ZDOK0_DP_P[15]	J24	ZDOK0_DP_P15	5-4J
ZDOK0_DP_N[15]	J25	ZDOK0_DP_N15	5-4J
ZDOK0_DP_P[14]	H30	ZDOK0_DP_P14	5-4J
ZDOK0_DP_N[14]	G31	ZDOK0_DP_N14	5-4J
ZDOK0_DP_P[13]	K27	ZDOK0_DP_P13	5-4J
ZDOK0_DP_N[13]	K26	ZDOK0_DP_N13	5-4J
ZDOK0_DP_P[12]	J32	ZDOK0_DP_P12	5-4J
ZDOK0_DP_N[12]	H33	ZDOK0_DP_N12	5-4J
ZDOK0_DP_P[11]	K33	ZDOK0_DP_P11	5-5J
ZDOK0_DP_N[11]	K32	ZDOK0_DP_N11	5-5J
ZDOK0_DP_P[10]	L34	ZDOK0_DP_P10	5-5J
ZDOK0_DP_N[10]	K34	ZDOK0_DP_N10	5-5J
ZDOK0_DP_P[9]	C32	ZDOK0_DP_P9	5-5J
ZDOK0_DP_N[9]	D32	ZDOK0_DP_N9	5-5J
ZDOK0_DP_P[8]	E28	ZDOK0_DP_P8	5-5J
ZDOK0_DP_N[8]	F28	ZDOK0_DP_N8	5-5J
ZDOK0_DP_P[7]	F31	ZDOK0_DP_P7	5-5J
ZDOK0_DP_N[7]	E31	ZDOK0_DP_N7	5-5J
ZDOK0_DP_P[6]	H28	ZDOK0_DP_P6	5-6J
ZDOK0_DP_N[6]	G28	ZDOK0_DP_N6	5-6J
ZDOK0_DP_P[5]	H29	ZDOK0_DP_P5	5-6J
ZDOK0_DP_N[5]	J29	ZDOK0_DP_N5	5-6J
ZDOK0_DP_P[4]	K24	ZDOK0_DP_P4	5-6J
ZDOK0_DP_N[4]	L24	ZDOK0_DP_N4	5-6J
ZDOK0_DP_P[3]	K28	ZDOK0_DP_P3	5-6J
ZDOK0_DP_N[3]	L28	ZDOK0_DP_N3	5-6J
ZDOK0_DP_P[2]	M25	ZDOK0_DP_P2	5-6J
ZDOK0_DP_N[2]	M26	ZDOK0_DP_N2	5-6J
ZDOK0_DP_P[1]	M28	ZDOK0_DP_P1	5-7J
ZDOK0_DP_N[1]	N28	ZDOK0_DP_N1	5-7J
ZDOK0_DP_P[0]	M31	ZDOK0_DP_P0	5-7J
ZDOK0_DP_N[0]	N30	ZDOK0_DP_N0	5-7J

U15

BANKS=3, 11, 15, 19



5-0E	ZDOK0_DP_P0	A1	A1
5-0E	ZDOK0_DP_N0	A2	A2
5-0E	ZDOK0_DP_P1	A3	A3
5-0E	ZDOK0_DP_N1	A4	A4
5-0E	ZDOK0_DP_P2	A5	A5
5-0E	ZDOK0_DP_N2	A6	A6
5-1E	ZDOK0_DP_P3	A7	A7
5-1E	ZDOK0_DP_N3	A8	A8
5-1E	ZDOK0_DP_P4	A9	A9
5-1E	ZDOK0_DP_N4	A10	A10
5-1E	ZDOK0_DP_P5	A11	A11
5-1E	ZDOK0_DP_N5	A12	A12
5-1E	ZDOK0_DP_P6	A13	A13
5-1E	ZDOK0_DP_N6	A14	A14
5-1E	ZDOK0_DP_P7	A15	A15
5-1E	ZDOK0_DP_N7	A16	A16
5-2E	ZDOK0_DP_P8	A17	A17
5-2E	ZDOK0_DP_N8	A18	A18
5-2E	ZDOK0_DP_P9	A19	A19
5-2E	ZDOK0_DP_N9	A20	A20
5-2E	ZDOK0_DP_P10	D1	D1
5-2E	ZDOK0_DP_N10	D2	D2
5-2E	ZDOK0_DP_P11	D3	D3
5-2E	ZDOK0_DP_N11	D4	D4
5-2E	ZDOK0_DP_P12	D5	D5
5-2E	ZDOK0_DP_N12	D6	D6
5-3E	ZDOK0_DP_P13	D7	D7
5-3E	ZDOK0_DP_N13	D8	D8
5-3E	ZDOK0_DP_P14	D9	D9
5-3E	ZDOK0_DP_N14	D10	D10
5-3E	ZDOK0_DP_P15	D11	D11
5-3E	ZDOK0_DP_N15	D12	D12
5-3E	ZDOK0_DP_P16	D13	D13
5-3E	ZDOK0_DP_N16	D14	D14
5-3E	ZDOK0_DP_P17	D15	D15
5-3E	ZDOK0_DP_N17	D16	D16
5-4E	ZDOK0_DP_P18	D17	D17
5-4E	ZDOK0_DP_N18	D18	D18
5-4E	ZDOK0_DP_P19	D19	D19
5-4E	ZDOK0_DP_N19	D20	D20

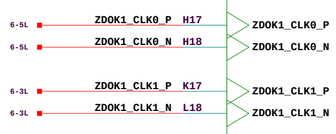
P5
6367550-5
ZDOK40

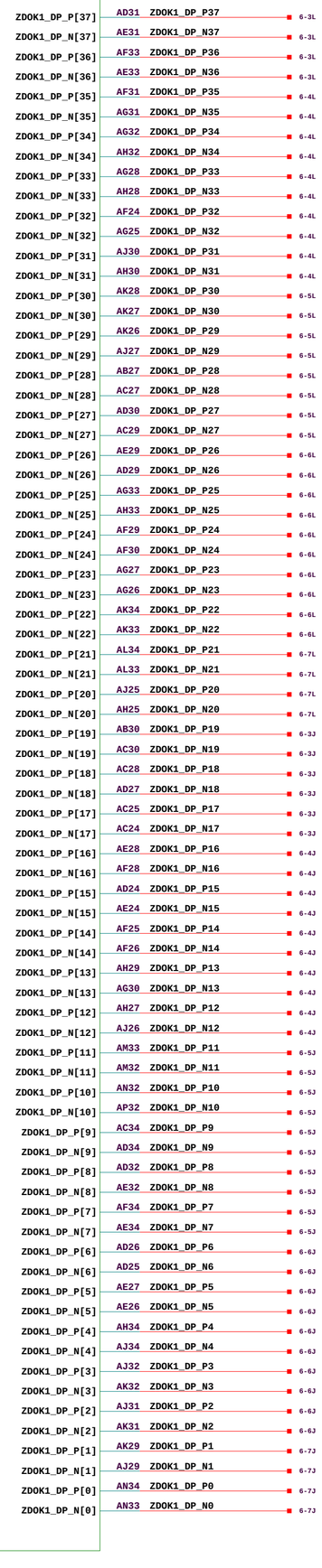
C1	C1	ZDOK0_DP_P20	5-4E
C2	C2	ZDOK0_DP_N20	5-4E
C3	C3	ZDOK0_DP_P21	5-4E
C4	C4	ZDOK0_DP_N21	5-4E
C5	C5	ZDOK0_DP_P22	5-4E
C6	C6	ZDOK0_DP_N22	5-4E
C7	C7	ZDOK0_DP_P23	5-5E
C8	C8	ZDOK0_DP_N23	5-5E
C9	C9	ZDOK0_DP_P24	5-5E
C10	C10	ZDOK0_DP_N24	5-5E
C11	C11	ZDOK0_DP_P25	5-5E
C12	C12	ZDOK0_DP_N25	5-5E
C13	C13	ZDOK0_DP_P26	5-5E
C14	C14	ZDOK0_DP_N26	5-5E
C15	C15	ZDOK0_DP_P27	5-5E
C16	C16	ZDOK0_DP_N27	5-5E
C17	C17	ZDOK0_DP_P28	5-6E
C18	C18	ZDOK0_DP_N28	5-6E
C19		ZDOK0_CLK0_P	5-7B
C20		ZDOK0_CLK0_N	5-7B
F1	F1	ZDOK0_DP_P29	5-6E
F2	F2	ZDOK0_DP_N29	5-6E
F3	F3	ZDOK0_DP_P30	5-6E
F4	F4	ZDOK0_DP_N30	5-6E
F5	F5	ZDOK0_DP_P31	5-6E
F6	F6	ZDOK0_DP_N31	5-6E
F7	F7	ZDOK0_DP_P32	5-6E
F8	F8	ZDOK0_DP_N32	5-6E
F9	F9	ZDOK0_DP_P33	5-7E
F10	F10	ZDOK0_DP_N33	5-7E
F11	F11	ZDOK0_DP_P34	5-7E
F12	F12	ZDOK0_DP_N34	5-7E
F13	F13	ZDOK0_DP_P35	5-7E
F14	F14	ZDOK0_DP_N35	5-7E
F15	F15	ZDOK0_DP_P36	5-7E
F16	F16	ZDOK0_DP_N36	5-7E
F17	F17	ZDOK0_DP_P37	5-7E
F18	F18	ZDOK0_DP_N37	5-7E
F19		ZDOK0_CLK1_P	5-7B
F20		ZDOK0_CLK1_N	5-7B

P5
6367550-5
ZDOK40

PLACE TEXT ON PCB: ZDOK0

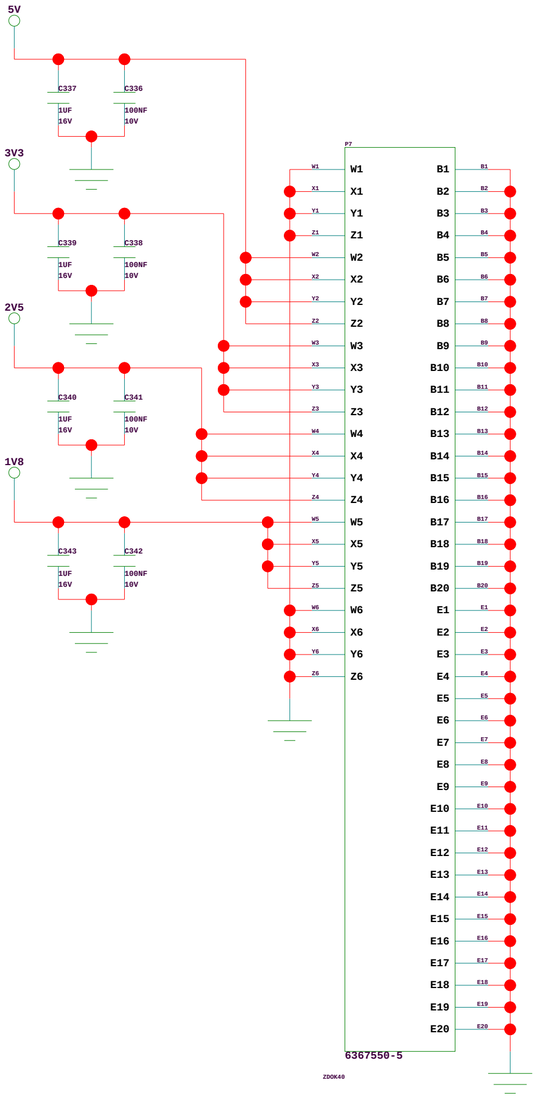
ROACH/iBOB2	**ROACH_ADC_0**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 5 OF 25

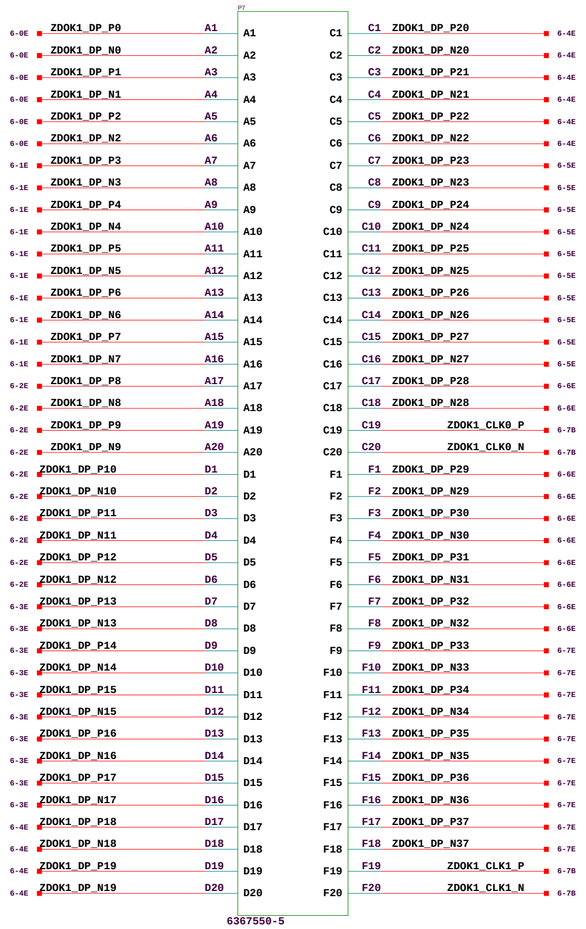




U15

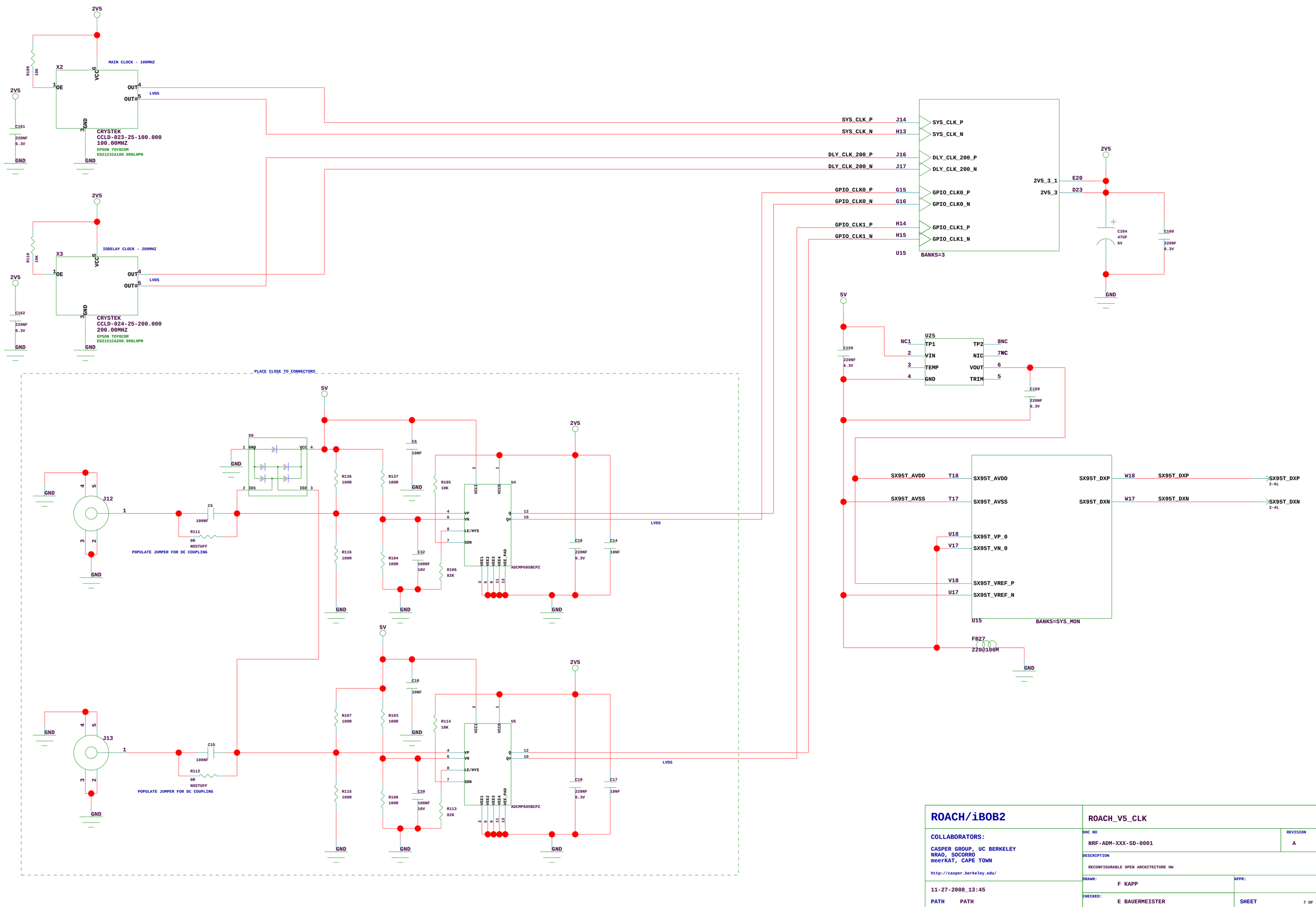
BANKS=3, 13, 17, 21





PLACE TEXT ON PCB: ZDOK1

ROACH/iBOB2	**ROACH_ADC_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 6 OF 25



ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
11-27-2008_13:45 PATH PATH	

ROACH/iBOB2	**ROACH_TRANSCEIVERS0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45 PATH	DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET: 8 OF 25

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

OPTICAL MODULE FAULT - RED LED

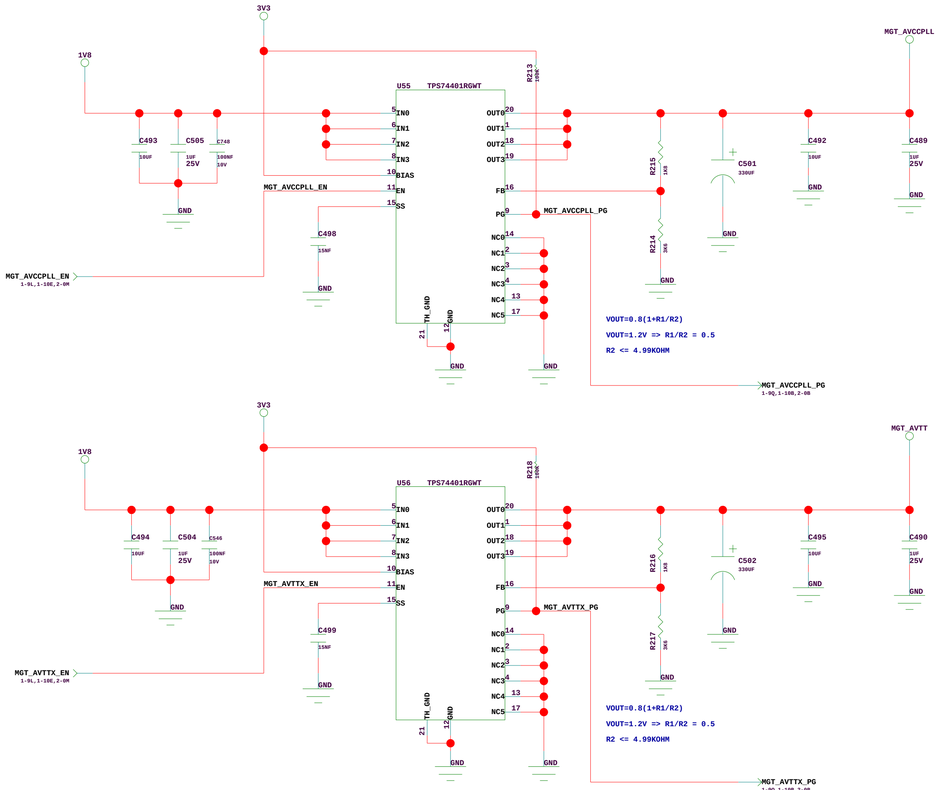
G4 AND G8 CONNECTED IN
2X2 MODULE

HIGH-SPEED DIFFERENTIAL VIAS

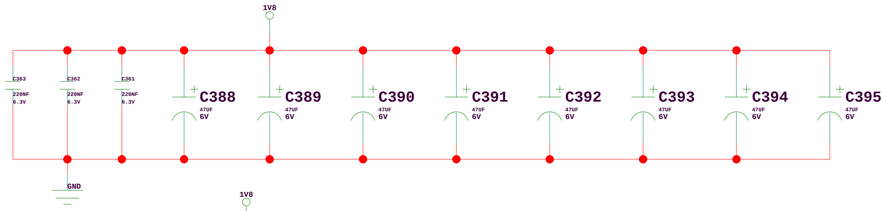
FCN-268F036-G/3DB

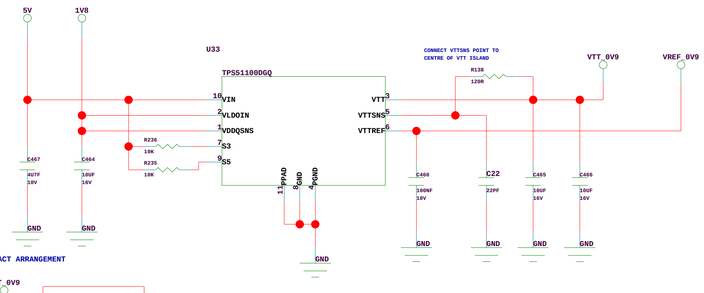
CCLD-023-25-156.250
156.25MHZ

ROACH/iBOB2	ROACH_TRANSCEIVERS2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
11-27-2008_13:45	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 9 OF 25

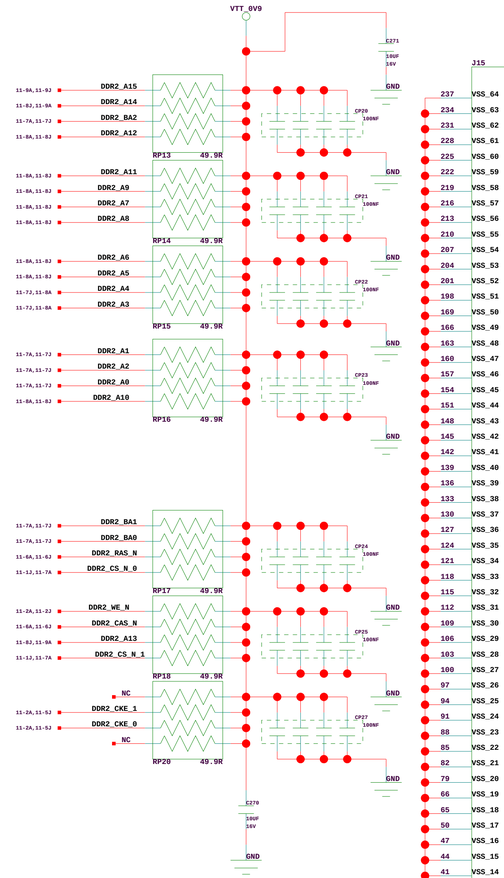


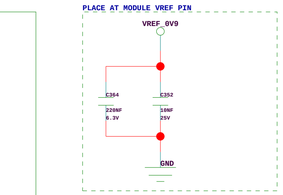
ROACH/iBOB2	**ROACH_TRANSCEIVERS_PSU**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 10 OF 25

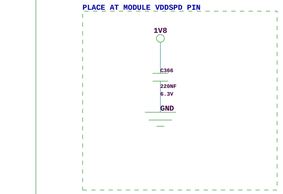


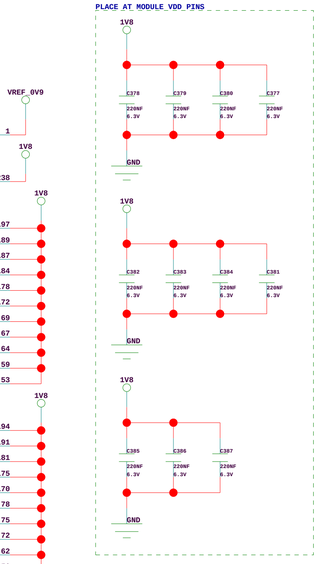


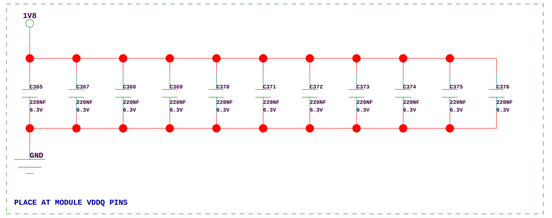
VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
PLACE ONE 10uF CAPACITOR ON EITHER END OF ISLAND











ROACH/iBOB2	ROACH_DDR2_DIMM
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
11-27-2008_13:45	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 11 OF 25

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

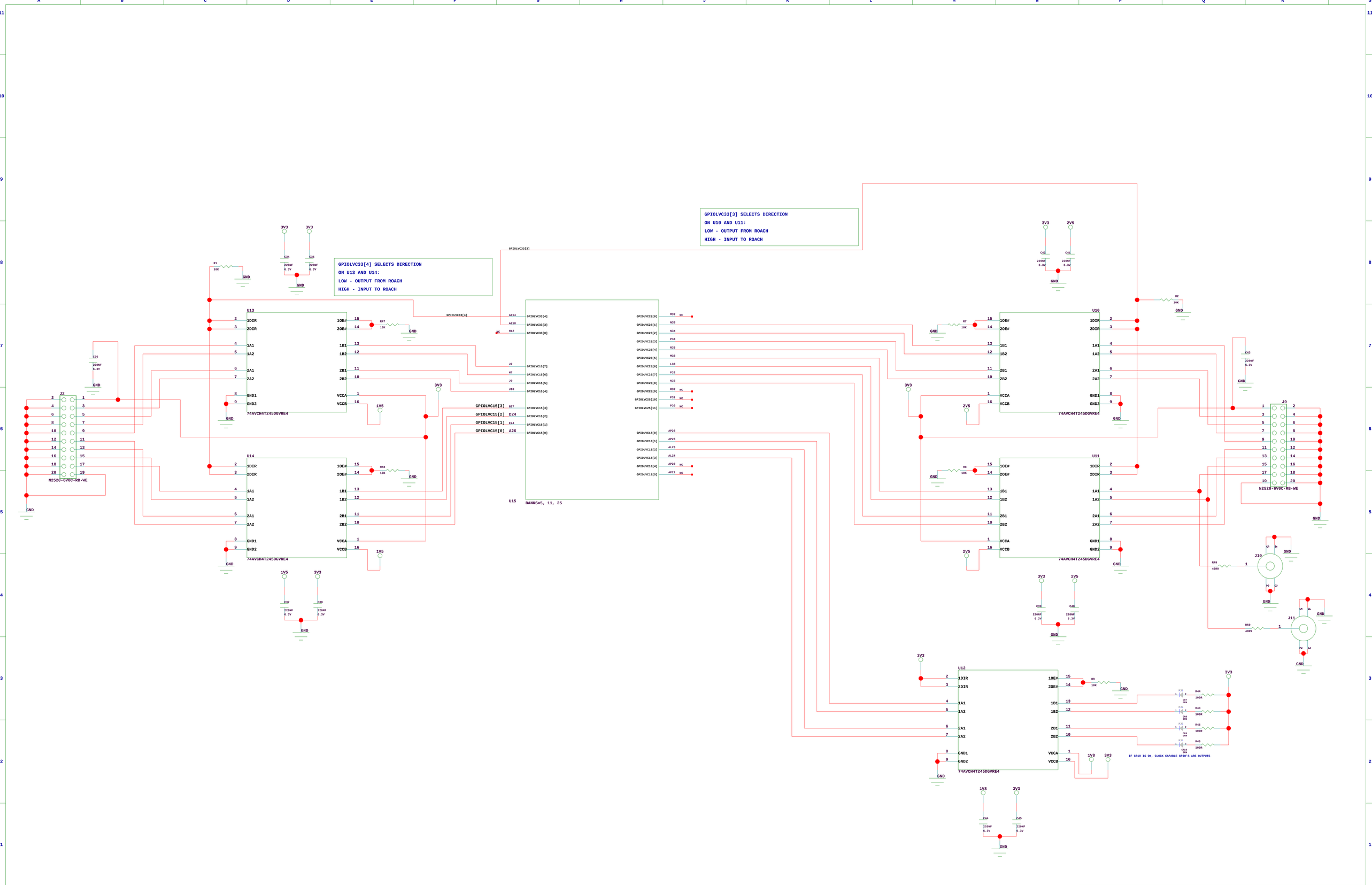
http://casper.berkeley.edu/

11-27-2008_13:45

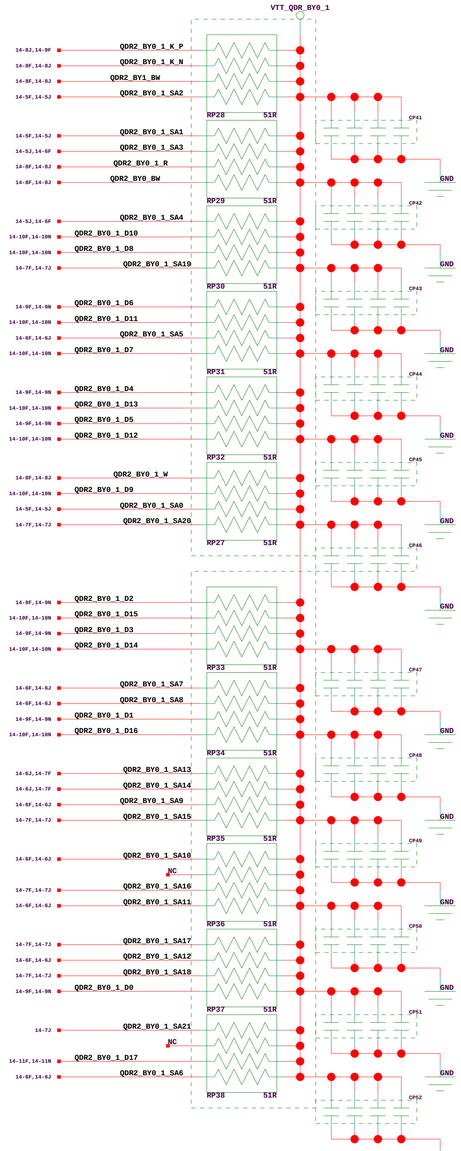
PATH PATH

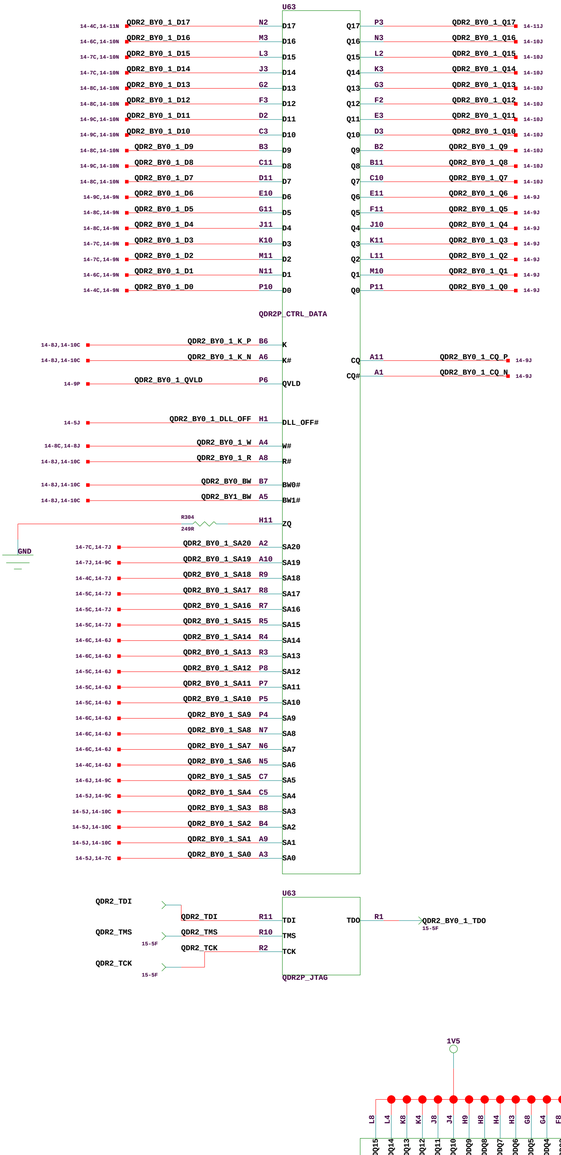
ROACH_DIFF_GPIO

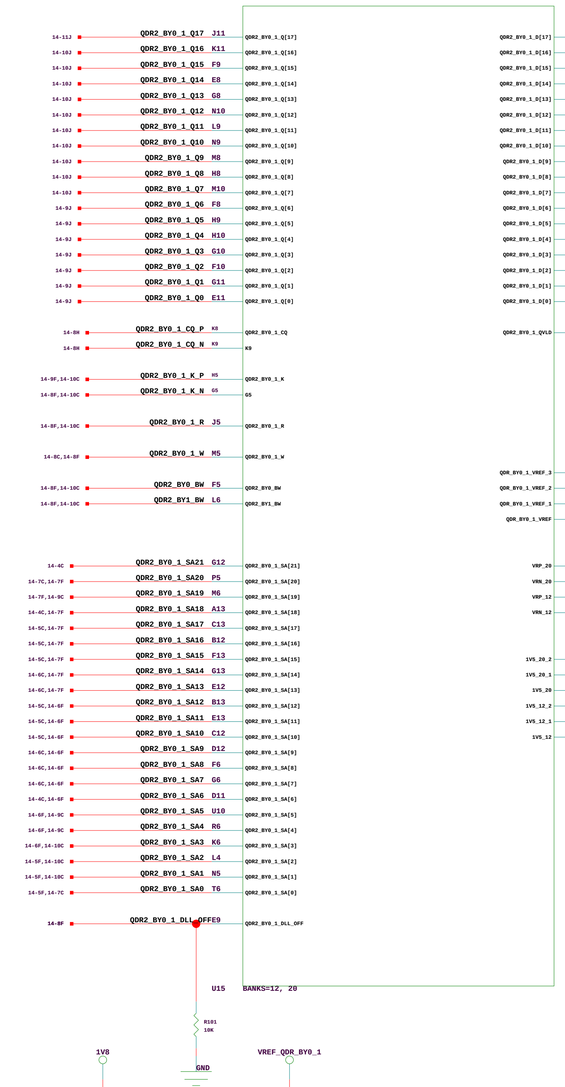
DOC NO: NRF-ADM-XXX-SD-0001
REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 12 OF 25

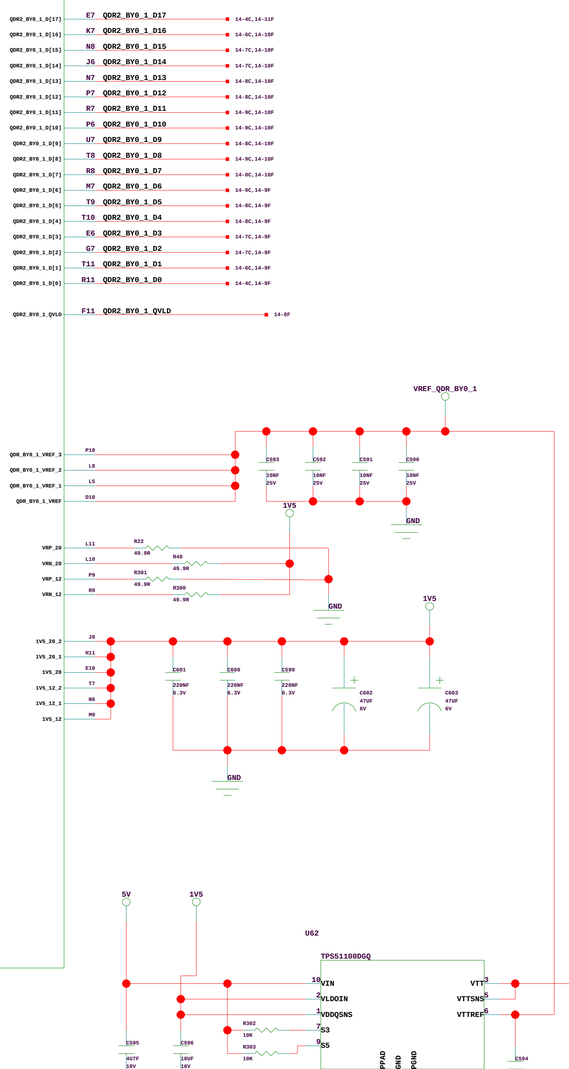


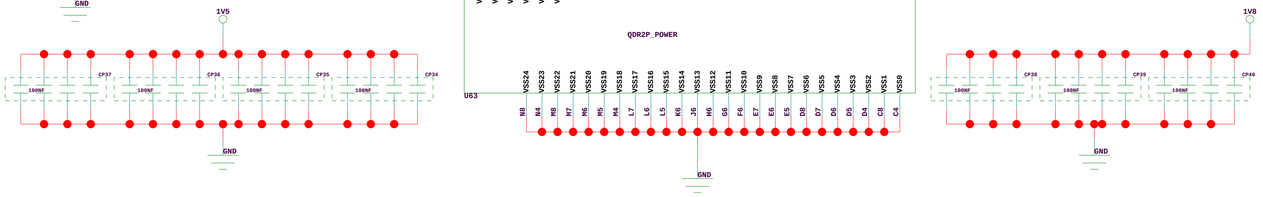
ROACH/iBOB2	**ROACH_GPIO_MISC**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 13 OF 25











ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 14 OF 25
11-27-2008_13:45 PATH PATH	

VTT_QDR_BY2_3

RP1 51R
RP2 51R
RP3 51R
RP4 51R
RP5 51R
RP6 51R
RP7 51R
RP8 51R
RP9 51R
RP10 51R
RP11 51R
RP12 51R

15-8J,15-9F QDR2_BY2_3_K_P
15-8F,15-8J QDR2_BY2_3_K_N
15-8F,15-8J QDR2_BY3_BW
15-5F,15-5J QDR2_BY2_3_SA2
15-5F,15-5J QDR2_BY2_3_SA1
15-5J,15-6F QDR2_BY2_3_SA3
15-8F,15-8J QDR2_BY2_3_R
15-8F,15-8J QDR2_BY2_BW
15-6F,15-6J QDR2_BY2_3_SA5
15-10F,15-10N QDR2_BY2_3_D8
15-5J,15-6F QDR2_BY2_3_SA4
15-7F,15-7J QDR2_BY2_3_SA19
15-9F,15-9N QDR2_BY2_3_D6
15-10F,15-10N QDR2_BY2_3_D11
15-10F,15-10N QDR2_BY2_3_D7
15-10F,15-10N QDR2_BY2_3_D10
15-9F,15-9N QDR2_BY2_3_D4
15-10F,15-10N QDR2_BY2_3_D13
15-9F,15-9N QDR2_BY2_3_D5
15-10F,15-10N QDR2_BY2_3_D12
15-8F,15-8J QDR2_BY2_3_W
15-10F,15-10N QDR2_BY2_3_D9
15-5F,15-5J QDR2_BY2_3_SA0
15-7F,15-7J QDR2_BY2_3_SA20
15-10F,15-10N QDR2_BY2_3_D16
15-10F,15-10N QDR2_BY2_3_D15
15-9F,15-9N QDR2_BY2_3_D3
15-10F,15-10N QDR2_BY2_3_D14
15-7J QDR2_BY2_3_SA21
NC
15-11F,15-11N QDR2_BY2_3_D17
15-6F,15-6J QDR2_BY2_3_SA6
15-7F,15-7J QDR2_BY2_3_SA17
15-6F,15-6J QDR2_BY2_3_SA12
15-7F,15-7J QDR2_BY2_3_SA18
15-9F,15-9N QDR2_BY2_3_D0
15-6F,15-6J QDR2_BY2_3_SA10
NC
15-7F,15-7J QDR2_BY2_3_SA16
15-6F,15-6J QDR2_BY2_3_SA11
15-6J,15-7F QDR2_BY2_3_SA13
15-6J,15-7F QDR2_BY2_3_SA14
15-6F,15-6J QDR2_BY2_3_SA9
15-7F,15-7J QDR2_BY2_3_SA15
15-6F,15-6J QDR2_BY2_3_SA7
15-6F,15-6J QDR2_BY2_3_SA8
15-9F,15-9N QDR2_BY2_3_D1
15-9F,15-9N QDR2_BY2_3_D2

CP1 100NF
CP2 100NF
CP3 100NF
CP4 100NF
CP5 100NF
CP6 100NF
CP7 100NF
CP8
CP9
CP10
CP11
CP12
CP13
CP14
CP15
CP16
CP17
CP18
CP19

GND

1V5

U17

15-6C,15-11N QDR2_BY2_3_D17 N2 D17
15-7C,15-10N QDR2_BY2_3_D16 M3 D16
15-7C,15-10N QDR2_BY2_3_D15 L3 D15
15-7C,15-10N QDR2_BY2_3_D14 J3 D14
15-8C,15-10N QDR2_BY2_3_D13 G2 D13
15-8C,15-10N QDR2_BY2_3_D12 F3 D12
15-9C,15-10N QDR2_BY2_3_D11 D2 D11
15-8C,15-10N QDR2_BY2_3_D10 C3 D10
15-8C,15-10N QDR2_BY2_3_D9 B3 D9
15-9C,15-10N QDR2_BY2_3_D8 C11 D8
15-9C,15-10N QDR2_BY2_3_D7 D11 D7
15-9C,15-9N QDR2_BY2_3_D6 E10 D6
15-8C,15-9N QDR2_BY2_3_D5 G11 D5
15-8C,15-9N QDR2_BY2_3_D4 J11 D4
15-7C,15-9N QDR2_BY2_3_D3 K10 D3
15-4C,15-9N QDR2_BY2_3_D2 M11 D2
15-4C,15-9N QDR2_BY2_3_D1 N11 D1
15-5C,15-9N QDR2_BY2_3_D0 P10 D0

QDR2P_CTRL_DATA

15-8J,15-10C QDR2_BY2_3_K_P B6 K
15-8J,15-10C QDR2_BY2_3_K_N A6 K#
15-9P QDR2_BY2_3_QVLD P6 QVLD
15-5J QDR2_BY2_3_DLL_OFF H1 DLL_OFF#
15-8C,15-8J QDR2_BY2_3_W A4 W#
15-8J,15-10C QDR2_BY2_3_R A8 R#
15-8J,15-10C QDR2_BY2_BW B7 BW0#
15-8J,15-10C QDR2_BY3_BW A5 BW1#
R55 240R
H11 ZQ
15-7C,15-7J GND
15-7J,15-9C QDR2_BY2_3_SA20 A2 SA20
15-6C,15-7J QDR2_BY2_3_SA19 A10 SA19
15-6C,15-7J QDR2_BY2_3_SA18 R9 SA18
15-6C,15-7J QDR2_BY2_3_SA17 R8 SA17
15-5C,15-7J QDR2_BY2_3_SA16 R7 SA16
15-4C,15-7J QDR2_BY2_3_SA15 R5 SA15
15-5C,15-6J QDR2_BY2_3_SA14 R4 SA14
15-5C,15-6J QDR2_BY2_3_SA13 R3 SA13
15-6C,15-6J QDR2_BY2_3_SA12 P8 SA12
15-5C,15-6J QDR2_BY2_3_SA11 P7 SA11
15-5C,15-6J QDR2_BY2_3_SA10 P5 SA10
15-4C,15-6J QDR2_BY2_3_SA9 P4 SA9
15-4C,15-6J QDR2_BY2_3_SA8 N7 SA8
15-4C,15-6J QDR2_BY2_3_SA7 N6 SA7
15-6C,15-6J QDR2_BY2_3_SA6 N5 SA6
15-6J,15-9C QDR2_BY2_3_SA5 C7 SA5
15-5J,15-9C QDR2_BY2_3_SA4 C5 SA4
15-5J,15-10C QDR2_BY2_3_SA3 B8 SA3
15-5J,15-10C QDR2_BY2_3_SA2 B4 SA2
15-5J,15-10C QDR2_BY2_3_SA1 A9 SA1
15-5J,15-7C QDR2_BY2_3_SA0 A3 SA0

Q17 P3 QDR2_BY2_3_Q17 D26 QDR2_BY2_3_Q[17]
Q16 N3 QDR2_BY2_3_Q16 C25 QDR2_BY2_3_Q[16]
Q15 L2 QDR2_BY2_3_Q15 B25 QDR2_BY2_3_Q[15]
Q14 K3 QDR2_BY2_3_Q14 C23 QDR2_BY2_3_Q[14]
Q13 G3 QDR2_BY2_3_Q13 C22 QDR2_BY2_3_Q[13]
Q12 F2 QDR2_BY2_3_Q12 A23 QDR2_BY2_3_Q[12]
Q11 E3 QDR2_BY2_3_Q11 C20 QDR2_BY2_3_Q[11]
Q10 D3 QDR2_BY2_3_Q10 B20 QDR2_BY2_3_Q[10]
Q9 B2 QDR2_BY2_3_Q9 C19 QDR2_BY2_3_Q[9]
Q8 B11 QDR2_BY2_3_Q8 B18 QDR2_BY2_3_Q[8]
Q7 C10 QDR2_BY2_3_Q7 A19 QDR2_BY2_3_Q[7]
Q6 E11 QDR2_BY2_3_Q6 C18 QDR2_BY2_3_Q[6]
Q5 F11 QDR2_BY2_3_Q5 A20 QDR2_BY2_3_Q[5]
Q4 J10 QDR2_BY2_3_Q4 A21 QDR2_BY2_3_Q[4]
Q3 K11 QDR2_BY2_3_Q3 B21 QDR2_BY2_3_Q[3]
Q2 L11 QDR2_BY2_3_Q2 B22 QDR2_BY2_3_Q[2]
Q1 M10 QDR2_BY2_3_Q1 B23 QDR2_BY2_3_Q[1]
Q0 P11 QDR2_BY2_3_Q0 A24 QDR2_BY2_3_Q[0]

CQ A11 QDR2_BY2_3_CQ_P 15-9J
CQ# A1 QDR2_BY2_3_CQ_N 15-9J

15-8N QDR2_BY2_3_CQ_P C24 QDR2_BY2_3_CQ
15-8N QDR2_BY2_3_CQ_N D25 D25
15-9F,15-10C QDR2_BY2_3_K_P D14 QDR2_BY2_3_K
15-8F,15-10C QDR2_BY2_3_K_N E14 E14
15-8F,15-10C QDR2_BY2_3_R C15 QDR2_BY2_3_R
15-8C,15-8F QDR2_BY2_3_W F15 QDR2_BY2_3_W
15-8F,15-10C QDR2_BY2_BW D15 QDR2_BY2_BW
15-8F,15-10C QDR2_BY3_BW D16 QDR2_BY3_BW

15-6C QDR2_BY2_3_SA21 D31 QDR2_BY2_3_SA[21]
15-7C,15-7F QDR2_BY2_3_SA20 F14 QDR2_BY2_3_SA[20]
15-7F,15-9C QDR2_BY2_3_SA19 A14 QDR2_BY2_3_SA[19]
15-6C,15-7F QDR2_BY2_3_SA18 D27 QDR2_BY2_3_SA[18]
15-6C,15-7F QDR2_BY2_3_SA17 A30 QDR2_BY2_3_SA[17]
15-5C,15-7F QDR2_BY2_3_SA16 B30 QDR2_BY2_3_SA[16]
15-4C,15-7F QDR2_BY2_3_SA15 C30 QDR2_BY2_3_SA[15]
15-5C,15-7F QDR2_BY2_3_SA14 B31 QDR2_BY2_3_SA[14]
15-5C,15-7F QDR2_BY2_3_SA13 D30 QDR2_BY2_3_SA[13]
15-6C,15-6F QDR2_BY2_3_SA12 B26 QDR2_BY2_3_SA[12]
15-5C,15-6F QDR2_BY2_3_SA11 A29 QDR2_BY2_3_SA[11]
15-5C,15-6F QDR2_BY2_3_SA10 D29 QDR2_BY2_3_SA[10]
15-4C,15-6F QDR2_BY2_3_SA9 A31 QDR2_BY2_3_SA[9]
15-4C,15-6F QDR2_BY2_3_SA8 G17 QDR2_BY2_3_SA[8]
15-4C,15-6F QDR2_BY2_3_SA7 C27 QDR2_BY2_3_SA[7]
15-6C,15-6F QDR2_BY2_3_SA6 C28 QDR2_BY2_3_SA[6]
15-6F,15-9C QDR2_BY2_3_SA5 E16 QDR2_BY2_3_SA[5]
15-6F,15-9C QDR2_BY2_3_SA4 E17 QDR2_BY2_3_SA[4]
15-6F,15-10C QDR2_BY2_3_SA3 A15 QDR2_BY2_3_SA[3]
15-5F,15-10C QDR2_BY2_3_SA2 B15 QDR2_BY2_3_SA[2]
15-5F,15-10C QDR2_BY2_3_SA1 C14 QDR2_BY2_3_SA[1]
15-5F,15-7C QDR2_BY2_3_SA0 B16 QDR2_BY2_3_SA[0]
15-8F QDR2_BY2_3_DLL_OFF D20 QDR2_BY2_3_DLL_OFF

BANKS=5, 23

U15
R102 10K

QDR2_BY0_1_TDO 14-5H QDR2_BY0_1_TDO R11 TDI
QDR2_TMS 14-5K QDR2_TMS R10 TMS
QDR2_TCK 14-5F QDR2_TCK R2 TCK
TDO R1 QDR2_BY2_3_TDO
QDR2P_JTAG

QDR2_BY2_3_D[17] F24 QDR2_BY2_3_D17 15-6C,15-11F
QDR2_BY2_3_D[16] F23 QDR2_BY2_3_D16 15-7C,15-10F
QDR2_BY2_3_D[15] E23 QDR2_BY2_3_D15 15-7C,15-10F
QDR2_BY2_3_D[14] E22 QDR2_BY2_3_D14 15-7C,15-10F
QDR2_BY2_3_D[13] D22 QDR2_BY2_3_D13 15-8C,15-10F
QDR2_BY2_3_D[12] E21 QDR2_BY2_3_D12 15-8C,15-10F
QDR2_BY2_3_D[11] D21 QDR2_BY2_3_D11 15-9C,15-10F
QDR2_BY2_3_D[10] F18 QDR2_BY2_3_D10 15-8C,15-10F
QDR2_BY2_3_D[9] A16 QDR2_BY2_3_D9 15-8C,15-10F
QDR2_BY2_3_D[8] B17 QDR2_BY2_3_D8 15-9C,15-10F
QDR2_BY2_3_D[7] C17 QDR2_BY2_3_D7 15-9C,15-10F
QDR2_BY2_3_D[6] D17 QDR2_BY2_3_D6 15-9C,15-9F
QDR2_BY2_3_D[5] F16 QDR2_BY2_3_D5 15-8C,15-9F
QDR2_BY2_3_D[4] E19 QDR2_BY2_3_D4 15-8C,15-9F
QDR2_BY2_3_D[3] F20 QDR2_BY2_3_D3 15-7C,15-9F
QDR2_BY2_3_D[2] G20 QDR2_BY2_3_D2 15-4C,15-9F
QDR2_BY2_3_D[1] F21 QDR2_BY2_3_D1 15-4C,15-9F
QDR2_BY2_3_D[0] G21 QDR2_BY2_3_D0 15-5C,15-9F

QDR2_BY2_3_QVLD A25 QDR2_BY2_3_QVLD 15-8F

VREF_QDR_BY2_3

QDR_BY2_3_VREF_3 G18
QDR_BY2_3_VREF_2 F19
QDR_BY2_3_VREF_1 A28
QDR_BY2_3_VREF A18

C56 10NF 25V
C55 10NF 25V
C50 10NF 25V
C46 10NF 25V

VRP_5 D19 RS1 49.9R
VRN_5 E18 RS2 49.9R
VRP_23 B28 R151 49.9R
VRN_23 C29 R152 49.9R

1V5_5_2 F17
1V5_5_1 C16
1V5_5 B19
1V5_23_2 G24
1V5_23_1 F27
1V5_23 C26

C85 220NF 6.3V
C86 220NF 6.3V
C87 220NF 6.3V
C88 470F 6V
C89 470F 6V

5V
1V5

U16

VIN 10
VLDOIN 2
VDDQSNS 1
S3 7
S5 9
PPAD 11
GND 8
PGND 4
VTT 3
VTTSNS 5
VTTREF 6

R53 10K
R54 10K

C58 4U7F 10V
C59 10UF 16V
C57 100NF 10V
C84 10UF 16V
C69 10UF 16V

VTT_QDR_BY2_3

GND and PGND (Power GND) should be isolated, with a single point connection between them.

1V8

VDDQ15 L8
VDDQ14 L4
VDDQ13 K8
VDDQ12 K4
VDDQ11 J8
VDDQ10 J4
VDDQ9 H9
VDDQ8 H8
VDDQ7 H4
VDDQ6 H3
VDDQ5 G8
VDDQ4 G4
VDDQ3 F9
VDDQ2 F4
VDDQ1 E8
VDDQ0 E4
VDD9 K7
VDD8 J7
VDD7 J5
VDD6 H7
VDD5 H5
VDD4 G7
VDD3 G5
VDD2 F7
VDD1 F5
VDD0 H2
VREF1 H10
VREF0

QDR2P_POWER

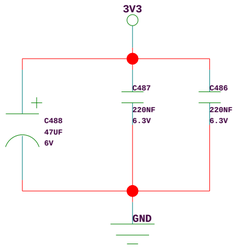
U17

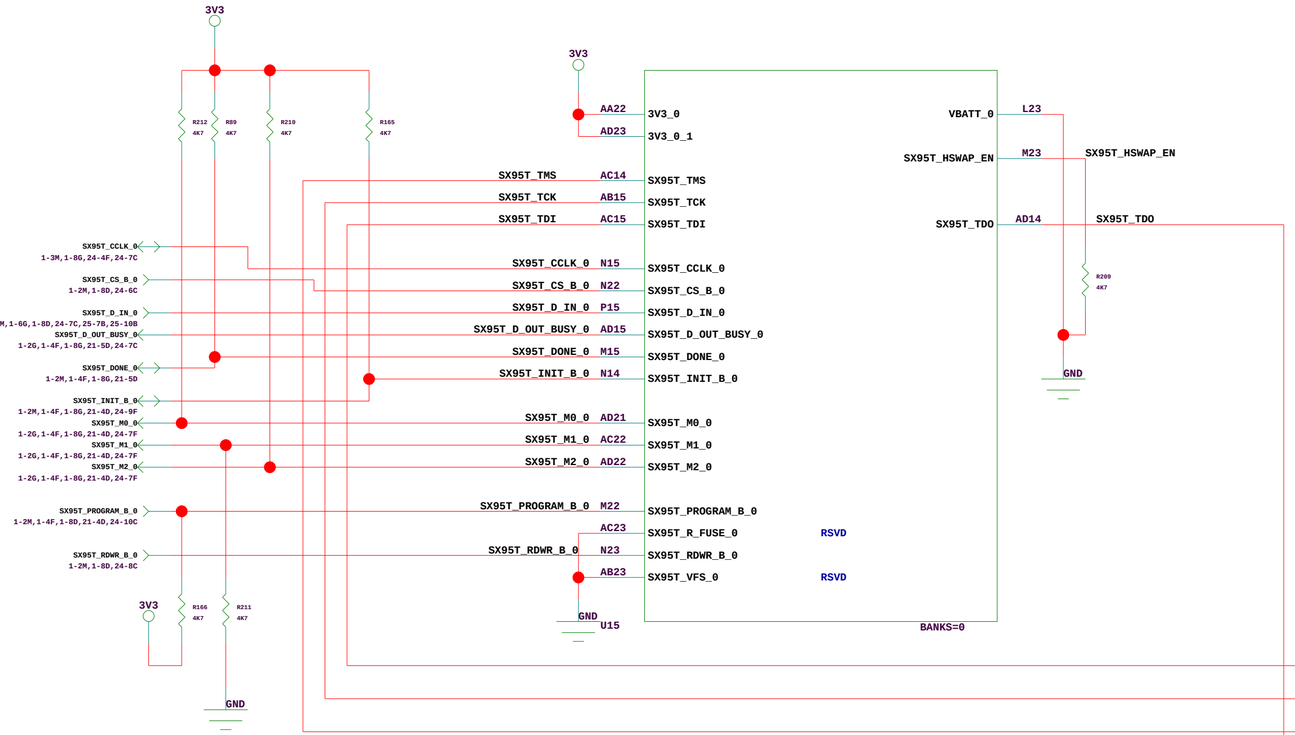
VSS24 N8
VSS23 N4
VSS22 M8
VSS21 M7
VSS20 M6
VSS19 M5
VSS18 M4
VSS17 L7
VSS16 L6
VSS15 L5
VSS14 K6
VSS13 J6
VSS12 H6
VSS11 G6
VSS10 F8
VSS9 F6
VSS8 E7
VSS7 E6
VSS6 E5
VSS5 D8
VSS4 D7
VSS3 D6
VSS2 D5
VSS1 D4
VSS0 C8
C4

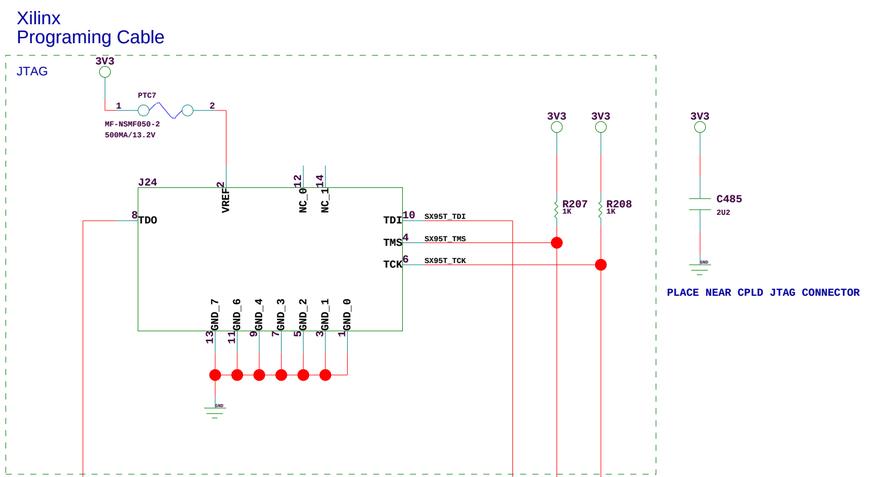
TBD

VALID CONFIGURATION MODES

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

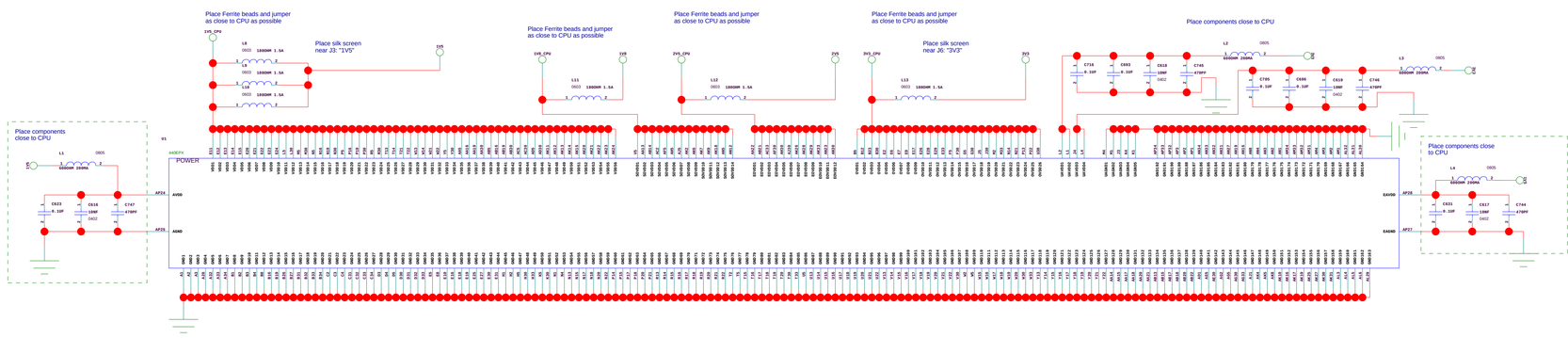


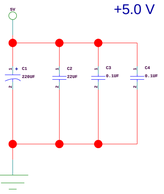


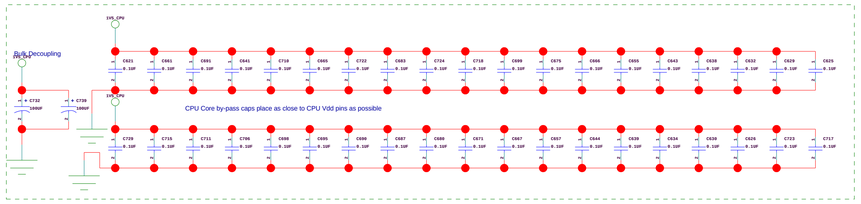


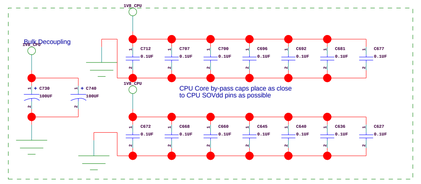
PLACE NEAR CPLD JTAG CONNECTOR

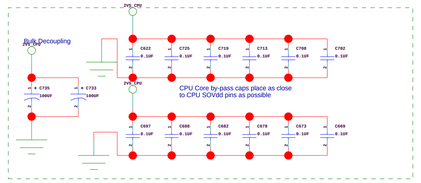
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
11-27-2008_13:45 PATH PATH	

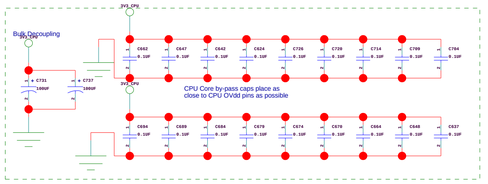


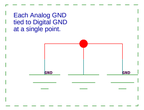










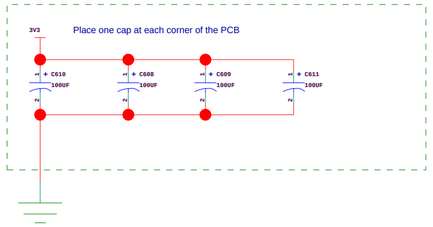


REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW DRAWN: F KAPP APPR:
11-27-2008_13:45 PATH PATH	CHECKED: E BAUERMEISTER SHEET 17 OF 25

REMOVED 3V3 GENERATION



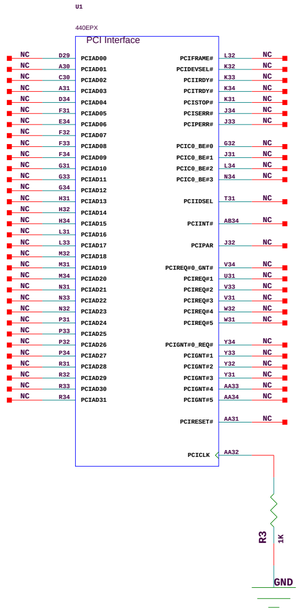
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET: 18 OF 25
11-27-2008_13:45 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

Place nearest PHY pin 96

Place nearest PHY pin 101

Place nearest PHY pin 98

Place nearest PHY pin 100

Place as close to PHY CORE VDD power pins as possible

Place as close to PHY IO VDD power pins as possible

UNUSED SECOND ETHERNET MAC

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups. Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place jumers in line with signals

Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5

Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY

HFJ11-1G02E-L12

ETHERNET Mgt.

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

JUMPER DEFAULTS

JP10, JP11	2 - 3	PHY ADD0 = 1
JP12, JP13	1 - 2	Adertised Modes 1000BASE-T, 100BASE-TX, 10BASE-T
JP14, JP15	1 - 2	
JP16, JP17	2 - 3	FULL DUPLEX
JP18, JP19	2 - 3	AUTO NEGOTIATION ENABLED
JP20-23	1 - 2	PHY ADD4:1 = 1111

ROACH/iBOB2	ROACH_PPC_ETH1
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 20 OF 25
11-27-2008_13:45	
PATH PATH	

U1

USB 2.0 DEVICE

440EPX

USB2CLK — A5 — NC

SECOND USB INTERFACE NOT IMPLEMENTED

NOTE:

SX95T_D_IN_0 ON SHEET 25, GPIO10

GPIO28/USB2TXVAL	C6	SX95T_D_OUT_BUSY_0	SX95T_D_OUT_BUSY_0	1-2G,1-4F,1-8G,16-4B,24-7C
USB2TXRDY_REFEN	B6	NC		
USB2RXACT_HOLDREQ_RCVINH	D7	NC		
USB2RXVAL_LEAKTEST2	C8	NC		
GPIO27/USB2RXERR_EXTREQ#	A4	SX95T_DONE_0	SX95T_DONE_0	1-2M,1-4F,1-8G
GPIO30/USB2XCVRSEL_EXTACK#	M3	SX95T_INIT_B_0	SX95T_INIT_B_0	1-2M,1-4F,1-8G,24-9F
GPIO31/USB2TERMSEL_BUSREQ	P4			
USB2LS0_DRVINH1	R2	SX95T_M0_0	SX95T_M0_0	1-2G,1-4F,1-8G,16-3B,24-7F
USB2LS1_LEAKTEST_HOLDPRI	P1	NC		
GPIO32/USB2OM0	R3	SX95T_M1_0	SX95T_M1_0	1-2G,1-4F,1-8G,16-3B,24-7F
GPIO33/USB2OM1	R4			
GPIO29/USB2SUSP_HOLDACK	C5	SX95T_M2_0	SX95T_M2_0	1-2G,1-4F,1-8G,16-3B,24-7F
		SX95T_PROGRAM_B_0	SX95T_PROGRAM_B_0	1-2M,1-4F,1-8D,16-3B,24-10C

NOTE:

USB HOST ONLY

USB 2.0 PHY
HOST/DEVICE

USB2XCVR — J2 — USB2_XCVR_D+

USB2XCVR# — J1 — USB2_XCVR_D-

USB2REXT — L3 — R182 3K4 0402 — GND

USB2XTAL — N2

USB2XTAL# — N3

CLK_USB2_48MHZ — CLK_USB2_48MHZ
1-4B,1-4L,23-4G

CRITICAL PLACEMENT

Place SP2 very close to P6

SP2 — SOT23 — PGB102ST23WR

SP2 — SOT23 — PGB102ST23WR

GND

5V — PTC1 1206L050 500MA — C614 220UF 10V — C612 100NF 10V — C613 1NF 50V

VR4 0603 5.5V 20A

P6 1X4 USBA
1 VCC
2 D-
3 D+
4 GND
5
6
89485-8001

GND

ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25

Z_ADDR

DDR_PA[15:0]

DDR_PDQ[63:0]

PPC_ECC[7:0]

DDR SDRAM

U1 — 64DEPX

DDR_PDQ0	AB2	MEMDATA00	
DDR_PDQ1	AF22	MEMDATA01	
DDR_PDQ2	AK26	MEMDATA02	
DDR_PDQ3	AL28	MEMDATA03	
DDR_PDQ4	AL22	MEMDATA04	
DDR_PDQ5	AK22	MEMDATA05	
DDR_PDQ6	AK21	MEMDATA06	
DDR_PDQ7	AF21	MEMDATA07	
DDR_PDQ8	AF28	MEMDATA08	
DDR_PDQ9	AL18	MEMDATA09	
DDR_PDQ10	AK17	MEMDATA10	
DDR_PDQ11	AF17	MEMDATA11	
DDR_PDQ12	AK29	MEMDATA12	
DDR_PDQ13	AF18	MEMDATA13	
DDR_PDQ14	AK18	MEMDATA14	
DDR_PDQ15	AF16	MEMDATA15	
DDR_PDQ16	AK16	MEMDATA16	
DDR_PDQ17	AF15	MEMDATA17	
DDR_PDQ18	AF14	MEMDATA18	
DDR_PDQ19	AL14	MEMDATA19	
DDR_PDQ20	AL17	MEMDATA20	
DDR_PDQ21	AK17	MEMDATA21	
DDR_PDQ22	AK15	MEMDATA22	
DDR_PDQ23	AK15	MEMDATA23	
DDR_PDQ24	AF13	MEMDATA24	
DDR_PDQ25	AK13	MEMDATA25	
DDR_PDQ26	AF12	MEMDATA26	
DDR_PDQ27	AL12	MEMDATA27	
DDR_PDQ28	AK14	MEMDATA28	
DDR_PDQ29	AK14	MEMDATA29	
DDR_PDQ30	AL13	MEMDATA30	
DDR_PDQ31	AK12	MEMDATA31	
DDR_PDQ32	AF3	MEMDATA32	
DDR_PDQ33	AF1	MEMDATA33	
DDR_PDQ34	AD4	MEMDATA34	
DDR_PDQ35	AD3	MEMDATA35	
DDR_PDQ36	AD1	MEMDATA36	
DDR_PDQ37	AF2	MEMDATA37	
DDR_PDQ38	AE2	MEMDATA38	
DDR_PDQ39	AE1	MEMDATA39	
DDR_PDQ40	AC3	MEMDATA40	
DDR_PDQ41	AC1	MEMDATA41	
DDR_PDQ42	AA4	MEMDATA42	
DDR_PDQ43	AA3	MEMDATA43	
DDR_PDQ44	AD2	MEMDATA44	
DDR_PDQ45	AC4	MEMDATA45	
DDR_PDQ46	AB1	MEMDATA46	
DDR_PDQ47	AB2	MEMDATA47	
DDR_PDQ48	Y3	MEMDATA48	
DDR_PDQ49	Y2	MEMDATA49	
DDR_PDQ50	Y4	MEMDATA50	
DDR_PDQ51	Y1	MEMDATA51	
DDR_PDQ52	AA2	MEMDATA52	
DDR_PDQ53	AA1	MEMDATA53	
DDR_PDQ54	W3	MEMDATA54	
DDR_PDQ55	W1	MEMDATA55	
DDR_PDQ56	V1	MEMDATA56	
DDR_PDQ57	U2	MEMDATA57	
DDR_PDQ58	W2	MEMDATA58	
DDR_PDQ59	Y4	MEMDATA59	
DDR_PDQ60	R1	MEMDATA60	
DDR_PDQ61	V3	MEMDATA61	
DDR_PDQ62	T1	MEMDATA62	
DDR_PDQ63	T3	MEMDATA63	

DDR_PA0	AM5	MEMADDR00	
DDR_PA1	AP4	MEMADDR01	
DDR_PA2	AM5	MEMADDR02	
DDR_PA3	AM6	MEMADDR03	
DDR_PA4	AP6	MEMADDR04	
DDR_PA5	AN6	MEMADDR05	
DDR_PA6	AL7	MEMADDR06	
DDR_PA7	AN7	MEMADDR07	
DDR_PA8	AM7	MEMADDR08	
DDR_PA9	AP7	MEMADDR09	
DDR_PA10	AL2	MEMADDR10	
DDR_PA11	AL8	MEMADDR11	
DDR_PA12	AN8	MEMADDR12	
DDR_PA13	AN4	MEMADDR13	
DDR_PBA0	AJ3	BA0	
DDR_PBA1	AK3	BA1	
DDR_PBA2	AP8	BA2	
DDR_PRAS#	AJ4	RAS#	
DDR_PCAS#	AN4	CAS#	
DDR_PWE#	AJ2	WE#	

DDR_PDM0	AL21	DM0	
DDR_PDM1	AP18	DM1	
DDR_PDM2	AP15	DM2	
DDR_PDM3	AL14	DM3	
DDR_PDM4	AD4	DM4	
DDR_PDM5	AN3	DM5	
DDR_PDM6	Y3	DM6	
DDR_PDM7	U3	DM7	
DDR_PDM8	AN18	DM8	

DDR_PDQS0	AM21	DQS0	
DDR_PDQS1	AM19	DQS1	
DDR_PDQS2	AL15	DQS2	
DDR_PDQS3	AM13	DQS3	
DDR_PDQS4	AE3	DQS4	
DDR_PDQS5	AN4	DQS5	
DDR_PDQS6	W4	DQS6	
DDR_PDQS7	T4	DQS7	
DDR_PDQS8	AP10	DQS8	

DDR_PODT0	AN3	MEMODT0	
DDR_PODT1	AG1	MEMODT1	
DDR_PCS0#	AN2	BANKSELA0	
DDR_PCS1#	AM1	BANKSELA1	
DDR_PCKE	AN9	MEMCKE0	
DDR_PCLKOUT	AL1	MEMCLKOUT	
DDR_PCLKOUT#	AK1	MEMCLKOUT#	

PPC_ECC0	AM11	ECC0	
PPC_ECC1	AL11	ECC1	
PPC_ECC2	AN9	ECC2	
PPC_ECC3	AL9	ECC3	
PPC_ECC4	AM11	ECC4	
PPC_ECC5	AN11	ECC5	
PPC_ECC6	AM10	ECC6	
PPC_ECC7	AP9	ECC7	

DDR_PDQ63	AJ1	DQ63	
DDR_PDQ62	AJ5	DQ62	
DDR_PDQ61	AJ6	DQ61	
DDR_PDQ60	AJ7	DQ60	
DDR_PDQ59	AH7	DQ59	
DDR_PDQ58	AH8	DQ58	
DDR_PDQ57	AH5	DQ57	
DDR_PDQ56	AH6	DQ56	
DDR_PDQ55	AG6	DQ55	
DDR_PDQ54	AG4	DQ54	
DDR_PDQ53	AG3	DQ53	
DDR_PDQ52	AF7	DQ52	
DDR_PDQ51	AE5	DQ51	
DDR_PDQ50	AE6	DQ50	
DDR_PDQ49	AD6	DQ49	
DDR_PDQ48	AD8	DQ48	
DDR_PDQ47	AC7	DQ47	
DDR_PDQ46	AC8	DQ46	
DDR_PDQ45	AB5	DQ45	
DDR_PDQ44	AB6	DQ44	
DDR_PDQ43	AB8	DQ43	
DDR_PDQ42	AA7	DQ42	
DDR_PDQ41	AA8	DQ41	
DDR_PDQ40	AA9	DQ40	
DDR_PDQ39	AB10	DQ39	
DDR_PDQ38	AB11	DQ38	
DDR_PDQ37	AA11	DQ37	
DDR_PDQ36	AA12	DQ36	
DDR_PDQ35	AB13	DQ35	
DDR_PDQ34	AB14	DQ34	
DDR_PDQ33	AA14	DQ33	
DDR_PDQ32	AA15	DQ32	
DDR_PDQ31	AB16	DQ31	
DDR_PDQ30	AB17	DQ30	
DDR_PDQ29	AA17	DQ29	
DDR_PDQ28	AA18	DQ28	
DDR_PDQ27	AB19	DQ27	
DDR_PDQ26	AB20	DQ26	
DDR_PDQ25	AA20	DQ25	
DDR_PDQ24	AA21	DQ24	
DDR_PDQ23	AB22	DQ23	
DDR_PDQ22	AB23	DQ22	
DDR_PDQ21	AA23	DQ21	
DDR_PDQ20	AA24	DQ20	
DDR_PDQ19	AB25	DQ19	
DDR_PDQ18	AB26	DQ18	
DDR_PDQ17	AA26	DQ17	
DDR_PDQ16	AA27	DQ16	
DDR_PDQ15	AB28	DQ15	
DDR_PDQ14	AA29	DQ14	
DDR_PDQ13	AA30	DQ13	
DDR_PDQ12	AB31	DQ12	
DDR_PDQ11	AB32	DQ11	
DDR_PDQ10	AA32	DQ10	
DDR_PDQ9	AA33	DQ9	
DDR_PDQ8	AB34	DQ8	
DDR_PDQ7	AB35	DQ7	
DDR_PDQ6	AB36	DQ6	
DDR_PDQ5	AA36	DQ5	
DDR_PDQ4	AA35	DQ4	
DDR_PDQ3	AA34	DQ3	
DDR_PDQ2	AA31	DQ2	
DDR_PDQ1	AA30	DQ1	
DDR_PDQ0	AA29	DQ0	

J8

DDR2_DIMM_CB7	168	PPC_ECC7
DDR2_DIMM_CB6	167	PPC_ECC6
DDR2_DIMM_CB5	162	PPC_ECC5
DDR2_DIMM_CB4	161	PPC_ECC4
DDR2_DIMM_CB3	49	PPC_ECC3
DDR2_DIMM_CB2	48	PPC_ECC2
DDR2_DIMM_CB1	43	PPC_ECC1
DDR2_DIMM_CB0	42	PPC_ECC0
DDR2_DIMM_DQ[63]	236	DDR_PDQ63
DDR2_DIMM_DQ[62]	235	DDR_PDQ62
DDR2_DIMM_DQ[61]	230	DDR_PDQ61
DDR2_DIMM_DQ[60]	229	DDR_PDQ60
DDR2_DIMM_DQ[59]	117	DDR_PDQ59
DDR2_DIMM_DQ[58]	116	DDR_PDQ58
DDR2_DIMM_DQ[57]	111	DDR_PDQ57
DDR2_DIMM_DQ[56]	110	DDR_PDQ56
DDR2_DIMM_DQ[55]	227	DDR_PDQ55
DDR2_DIMM_DQ[54]	226	DDR_PDQ54
DDR2_DIMM_DQ[53]	218	DDR_PDQ53
DDR2_DIMM_DQ[52]	217	DDR_PDQ52
DDR2_DIMM_DQ[51]	108	DDR_PDQ51
DDR2_DIMM_DQ[50]	107	DDR_PDQ50
DDR2_DIMM_DQ[49]	99	DDR_PDQ49
DDR2_DIMM_DQ[48]	98	DDR_PDQ48
DDR2_DIMM_DQ[47]	215	DDR_PDQ47
DDR2_DIMM_DQ[46]	214	DDR_PDQ46
DDR2_DIMM_DQ[45]	209	DDR_PDQ45
DDR2_DIMM_DQ[44]	208	DDR_PDQ44
DDR2_DIMM_DQ[43]	96	DDR_PDQ43
DDR2_DIMM_DQ[42]	95	DDR_PDQ42
DDR2_DIMM_DQ[41]	90	DDR_PDQ41
DDR2_DIMM_DQ[40]	89	DDR_PDQ40
DDR2_DIMM_DQ[39]	206	DDR_PDQ39
DDR2_DIMM_DQ[38]	205	DDR_PDQ38
DDR2_DIMM_DQ[37]	200	DDR_PDQ37
DDR2_DIMM_DQ[36]	199	DDR_PDQ36
DDR2_DIMM_DQ[35]	87	DDR_PDQ35
DDR2_DIMM_DQ[34]	86	DDR_PDQ34
DDR2_DIMM_DQ[33]	81	DDR_PDQ33
DDR2_DIMM_DQ[32]	80	DDR_PDQ32
DDR2_DIMM_DQ[31]	159	DDR_PDQ31
DDR2_DIMM_DQ[30]	158	DDR_PDQ30
DDR2_DIMM_DQ[29]	153	DDR_PDQ29
DDR2_DIMM_DQ[28]	152	DDR_PDQ28
DDR2_DIMM_DQ[27]	40	DDR_PDQ27
DDR2_DIMM_DQ[26]	39	DDR_PDQ26
DDR2_DIMM_DQ[25]	34	DDR_PDQ25
DDR2_DIMM_DQ[24]	33	DDR_PDQ24
DDR2_DIMM_DQ[23]	150	DDR_PDQ23
DDR2_DIMM_DQ[22]	149	DDR_PDQ22
DDR2_DIMM_DQ[21]	144	DDR_PDQ21
DDR2_DIMM_DQ[20]	143	DDR_PDQ20
DDR2_DIMM_DQ[19]	31	DDR_PDQ19
DDR2_DIMM_DQ[18]	30	DDR_PDQ18
DDR2_DIMM_DQ[17]	25	DDR_PDQ17
DDR2_DIMM_DQ[16]	24	DDR_PDQ16
DDR2_DIMM_DQ[15]	141	DDR_PDQ15
DDR2_DIMM_DQ[14]	140	DDR_PDQ14
DDR2_DIMM_DQ[13]	132	DDR_PDQ13
DDR2_DIMM_DQ[12]	131	DDR_PDQ12
DDR2_DIMM_DQ[11]	22	DDR_PDQ11
DDR2_DIMM_DQ[10]	21	DDR_PDQ10
DDR2_DIMM_DQ[9]	13	DDR_PDQ9
DDR2_DIMM_DQ[8]	12	DDR_PDQ8
DDR2_DIMM_DQ[7]	129	DDR_PDQ7
DDR2_DIMM_DQ[6]	128	DDR_PDQ6
DDR2_DIMM_DQ[5]	123	DDR_PDQ5
DDR2_DIMM_DQ[4]	122	DDR_PDQ4
DDR2_DIMM_DQ[3]	10	DDR_PDQ3
DDR2_DIMM_DQ[2]	9	DDR_PDQ2
DDR2_DIMM_DQ[1]	4	DDR_PDQ1
DDR2_DIMM_DQ[0]	3	DDR_PDQ0
DDR2_DIMM_SA2	101	
DDR2_DIMM_SA1	240	
DDR2_DIMM_SA0	239	
DDR2_DIMM_SCL	120	I2C0_SCLK 1-48,1-61,1-108,2-2P,25-SB
DDR2_DIMM_SDA	119	I2C0_SDATA 1-38,1-61,1-10E

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DDR2_DIMM_A[15]	173	DDR_PA15
DDR2_DIMM_A[14]	174	DDR_PA14
DDR2_DIMM_A[13]	196	DDR_PA13
DDR2_DIMM_A[12]	176	DDR_PA12
DDR2_DIMM_A[11]	57	DDR_PA11
DDR2_DIMM_A[10]	70	DDR_PA10
DDR2_DIMM_A[9]	177	DDR_PA9
DDR2_DIMM_A[8]	179	DDR_PA8
DDR2_DIMM_A[7]	58	DDR_PA7
DDR2_DIMM_A[6]	180	DDR_PA6
DDR2_DIMM_A[5]	60	DDR_PA5
DDR2_DIMM_A[4]	61	DDR_PA4
DDR2_DIMM_A[3]	182	DDR_PA3
DDR2_DIMM_A[2]	63	DDR_PA2
DDR2_DIMM_A[1]	183	DDR_PA1
DDR2_DIMM_A[0]	188	DDR_PA0
DDR2_DIMM_BA[2]	54	DDR_PBA2 — 22-9D,22-10L
DDR2_DIMM_BA[1]	190	DDR_PBA1 — 22-8L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0 — 22-7L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS# — 22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS# — 22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	DDR_PCLKOUT2
DDR2_DIMM_CK_N[2]	221	DDR_PCLKOUT2#
DDR2_DIMM_CK_P[1]	137	DDR_PCLKOUT1
DDR2_DIMM_CK_N[1]	138	DDR_PCLKOUT1#
DDR2_DIMM_CK_P[0]	185	DDR_PCLKOUT0
DDR2_DIMM_CK_N[0]	186	DDR_PCLKOUT0#
DDR2_DIMM_CKE[1]	171	
DDR2_DIMM_CKE[0]	52	DDR_PCKE — 22-8D,22-11L
DDR2_DIMM_DM_CB	164	DDR_PDM8 — 22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7 — 22-9D
DDR2_DIMM_DM[6]	223	DDR_PDM6 — 22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5 — 22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4 — 22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3 — 22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2 — 22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1 — 22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0 — 22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8 — 22-8D
DDR2_DIMM_DQS_CB_N	45	NC
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7 — 22-8D
DDR2_DIMM_DQS_N[7]	113	NC
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6 — 22-8D
DDR2_DIMM_DQS_N[6]	104	NC
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5 — 22-8D
DDR2_DIMM_DQS_N[5]	92	NC
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4 — 22-8D
DDR2_DIMM_DQS_N[4]	83	NC
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3 — 22-8D
DDR2_DIMM_DQS_N[3]	36	NC
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2 — 22-8D
DDR2_DIMM_DQS_N[2]	27	NC
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1 — 22-8D
DDR2_DIMM_DQS_N[1]	15	NC
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0 — 22-8D
DDR2_DIMM_DQS_N[0]	6	NC
DDR2_DIMM_WE#	73	DDR_PWE# — 22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1
DDR2_DIMM_ODT[0]	195	DDR_PODT0
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N — 1-38,1-3M,24-10F
DDR2_DIMM_S#[1]	76	DDR_PCS1# — 22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0# — 22-7L,22-8D
PAR_OUT	55	PPC_DDR2_ERROR — 1 TP4
PAR_IN	68	PAR_IN — 1 TP5

C313, C308: 5PF 50V; C455: 5PF 50V

R226: 4K7 — PPC_DDR2_RESET_N

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

DDR_VTT

RP24: DDR_PCKE, DDR_PA15, DDR_PA14, DDR_PBA2 — 22-8K,22-8D
RP23: DDR_PA12, DDR_PA11, DDR_PA9 — NC
RP22: DDR_PA7, DDR_PA8, DDR_PA6, DDR_PA5
RP21: DDR_PA4, DDR_PA3, DDR_PA1, DDR_PA2
RP25: DDR_PA0, DDR_PBA1, DDR_PA10, DDR_PBA0 — 22-8K,22-9D
RP26: DDR_PRAS#, DDR_PWE#, DDR_PCS0#, DDR_PCAS# — 22-7K,22-9D; 22-3K,22-9D; 22-8K,22-9D
RP19: DDR_PCS1#, DDR_PODT0, DDR_PA13, DDR_PODT1 — 22-3K,22-9D; 22-8D

CP26, CP28, CP29, CP30, CP32, CP31, CP33; GND

J8

VSS_64	237	VDD_DDR_0V9
VSS_63	234	VREF 1
VSS_62	231	3V3
VSS_61	228	VDDSPD 238
VSS_60	225	1V8
VSS_59	222	VDD_11 197
VSS_58	219	VDD_10 189
VSS_57	216	VDD_9 187
VSS_56	213	VDD_8 184
VSS_55	210	VDD_7 178
VSS_54	207	VDD_6 172
VSS_53	204	VDD_5 69
VSS_52	201	VDD_4 67
VSS_51	198	VDD_3 64
VSS_50	169	VDD_2 59
VSS_49	166	VDD_1 53
VSS_48	163	
VSS_47	160	VDDQ_11 194
VSS_46	157	VDDQ_10 191
VSS_45	154	VDDQ_9 181
VSS_44	151	VDDQ_8 175
VSS_43	148	VDDQ_7 170
VSS_42	145	VDDQ_6 78
VSS_41	142	VDDQ_5 75
VSS_40	139	VDDQ_4 72
VSS_39	136	VDDQ_3 62
VSS_38	133	VDDQ_2 56
VSS_37	130	VDDQ_1 51
VSS_36	127	
VSS_35	124	
VSS_34	121	
VSS_33	118	
VSS_32	115	
VSS_31	112	
VSS_30	109	
VSS_29	106	
VSS_28	103	
VSS_27	100	
VSS_26	97	
VSS_25	94	
VSS_24	91	
VSS_23	88	
VSS_22	85	
VSS_21	82	
VSS_20	79	
VSS_19	76	
VSS_18	65	
VSS_17	50	
VSS_16	47	
VSS_15	44	
VSS_14	41	
VSS_13	38	
VSS_12	35	
VSS_11	32	
VSS_10	29	
VSS_9	26	
VSS_8	23	
VSS_7	20	
VSS_6	17	
VSS_5	14	
VSS_4	11	
VSS_3	8	
VSS_2	5	
VSS_1	2	

879160001

GND

DECOUPLING

DDR_VREF_0V9: C432, C433 — 100NF 10V; 10NF 25V
1V8: C454, C434, C439, C443, C431, C444, C436, C445, C435, C446 — 100NF 10V; 10NF 25V
1V8: C438, C451, C437, C452, C439, C449, C440, C450, C441, C448, C442, C447 — 100NF 10V; 10NF 25V

PLACE NEAREST DDR2 MODULE PINS

POWER

5V, 1V8

C150: 0.1UF
C148: 0.1UF; C151: 0.1UF 0402; C152: 0.1UF 0402; C149: 10UF 10V 0402

Place parts as close to CPU as possible

U32 TPS51100DGQ
VIN 10, VLDOIN 2, VDDQSNS 1, S3 7, S5 8, PPAD 11, GND 9, PGND 4
VTT 3, VTTSNS 5, VTTREF 6
R230 10K, R229 10K
C459 4U7F 10V, C456 10UF 10V, C453 100NF 10V, C21 22PF, C457 10UF 10V, C458 10UF 10V
R6 120R
DDR_VREF_0V9, DDR_VTT

L17 0603 1000HM 1.5A
C329 4U7F 10V, C300 100NF 10V, C63 10NF 25V
R167 10K
AVDD 8, AGND 7, OE 22, OS 21

DDR_PCLKOUT0 … DDR_PCLKOUT3 → Y0 … Y8 (38, 37, 39, 40, 3, 2, 11, 12, 14, 13, 34, 35, 33, 32, 29, 30, 19, 18, 16, 17)

DDR_PCLKOUT
R168 120R
CLK 4, CLK# 5

R169 120R
FBIN 27, FBIN# 26, FBOUT 24, FBOUT# 25
U6 CDCU877ARHAT; GND1 10, GND2 41

Z_IN
Z_OUT
Z_FB
FBOUT#
FBOUT

PPC DDR2 LAYOUT NOTES

ROUTE ALL DDR CLOCKS AS LENGTH MATCHED ONLY - DIFFERENTIAL ROUTING NOT REQUIRED

CLOCK DELAYS MUST ADHERE TO THE FOLLOWING:
Z_IN + Z_OUT - Z_FB = Z_ADDR + 500 ps (+-25 ps)
WHERE:
Z_IN = PROPAGATION DELAY ON DDR_PCLKOUT/DDR_PCLKOUT#
Z_OUT = PROPAGATION DELAY ON DDR_PCLKOUTn/DDR_PCLKOUTn#
Z_FB = PROPAGATION DELAY ON FBOUT/FBOUT#
Z_ADDR = PROPAGATION DELAY ON DDR_PADD[13:0]

DDR_PCLKOUTn/DDR_PCLKOUTn# NETS CAN BE SWAPPED ON CLOCK BUFFER TO EASE ROUTING

ALL DQ, DQS, DM, ADDR, CMD AND CTRL LINES LENGTH MATCHED TO 400 ps
MATCHING WITHIN BYTE LANE: 50 ps
209 ps < TRACE LENGTH < 800 ps

U6 THERMAL TAB TO BE CONNECTED TO GND PLANE WITH THERMAL VIAS

PowerPC DRAM Interface:

DDR2 240 pin DIMM
72 bit ECC
Unbuffered and Registered DIMMs supported
Up to 2GB supported
CAS Latencies: 2, 2.5 or 3
Clock Frequencies: 133MHz to 166MHz
Single Ended Strobes

ROACH/iBOB2	ROACH_PPC_DDR2
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 22 OF 25

PWR_GOOD
1-3G,1-4H,24-8R

3V3

PWR_GOOD monitors the +1.0v, 1V5, 1V8, 2V5, and 3V3 supplies

RESET_PB_POR#
1-3M,1-4H,24-7F

RESET_PORH
1-3G,1-4L,1-6G,24-5M,25-5G

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_3V3_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz

PLACE NEAR U9

SEL_SYSCLK
1-3M,1-4H,24-10F

CLK_UART_11_0592MHZ
1-4L,1-6G,25-3B

UART:11.0592MHZ

SYSTEM:33MHZ

CLK_CPLD_33MHZ
1-2G,1-4L,24-8C

CPLD:33MHZ

CLK_SYS_33MHZ

CLK_TMRCLK
1-2M,1-4H,24-10C

SYSERR
1-2G,1-4L,24-10C

PPC_THERMONA
1-4L,1-10E,2-6L

PPC_THERMONB
1-4L,1-10E,2-4L

PPC440EPX-NTA533T

IRQ0-9 have programmable polarity per section 10.5.7 (UIC0_PR) 440ep user manual

GETH0_INT#
1-4H,1-5E,20-4E

MONITOR_INT
1-4H,1-10E,2-2F

VS_INT#
1-4H,1-6L,25-8Q

STTM_ALERT
1-4H,1-6L,25-2B

GPIO44
1-4L

CPLD_INT
1-3M,1-4H,24-6C

NO POP
RO1 - RO5

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz * 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible

CLK_SEL_M66EN
1-2M,1-4H,24-10F

PLACE NEAR U24

CLK_GETH0_25MHZ
1-4L,1-5B,20-4E

CLK_USB2_48MHZ
1-4B,1-4L,21-2C

CLK_CPLD_50MHZ
1-2G,1-4L,24-7C

TRACE & JTAG CONNECTORS

Critical placement and routing of the Trace connector and nets. Up to CPU frequency/4

TRACE PORT

CPU_TRST#
1-3M,1-4H,24-9C

DEBUG_TRST#
1-2G,1-4L,24-9C

R26 is for current limiting and should be <100 Ohms.

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

11-27-2008_13:45

PATH PATH

ROACH_PPC_TST_CLK_IO

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 23 OF 25

roach_cpld_XC2C256_7VQ100C_pcb

CLK_TMCLK	4	PAD4	PAD217 142 NC
SYSERR	7	PAD8	PAD214 140 NC
EXT_RESET#	9	PAD10	PAD213 139 GETH0_RST#
SX95T_PROGRAM_B_0	10	PAD12	PAD212 138 PPC_DDR2_RESET_N
SX95T_DONE_0	11	PAD15	PAD211 137 CLK_SEL_MGGEN
PCS_2	12	PAD16	PAD208 136 SEL_SYSCLK
PB_WE	13	PAD17	PAD207 135 NC
DEBUG_TRST#	14	PAD18	PAD206 134 NC
CPU_TRST#/	15	PAD19	PAD204 133 NC
FWBE_0#	16	PAD20	PAD199 132 NC
PADATA[27]	17	PAD21	PAD197 131 SX95T_INIT_B_0
PADATA[28]	18	PAD23	PAD196 130 NC
PADATA[29]	19	PAD28	PAD195 129
PADATA[30]	20	PAD29	PAD194 128
PADATA[31]	21	PAD30	PAD192 126
PDATA0	22	PAD31	PAD191 125 NC
PDATA1	23	PAD32	PAD190 124 NC
PDATA2	24	PAD33	PAD187 121 MMC_WP
PDATA3	25	PAD34	PAD186 120 DAT1
PDATA4	26	PAD35	PAD178 119 DAT0_DO
PDATA7	28	PAD44	PAD177 118 DAT7
CLK_CPLD_33MHZ	30	PAD48	PAD176 117 DAT6
PDATA6	31	PAD49	PAD175 116 CLK_SCLK
CLK_PERCLK	32	PAD50	PAD173 115 DAT5
PDATA5	33	PAD52	PAD171 114 DAT4
PDEX	34	PAD54	PAD169 113 CMD_DI
SX95T_RDWR_B_0	35	PAD55	PAD168 112 DAT3
CLK_CPLD_50MHZ	38	PAD59	PAD167 111 DAT2
SX95T_D_IN_0	40	PAD64	PAD166 110 MMC_CD
SX95T_D_OUT_BUSY_0	41	PAD65	PAD163 107 SX95T_M0_0
PER_CCLK_ENa	42	PAD66	PAD162 106 SX95T_M1_0
SX95T_CCLK_0	43	PAD67	PAD161 105 SX95T_M2_0
FRY_BY#	44	PAD68	PAD160 104 NC
FWP#	45	PAD69	PAD158 103 RESET_PB_POR#
EE1_WP#	46	PAD70	PAD156 102 USER_LED0
EE2_BOOT_WP#	48	PAD73	PAD154 101 USER_LED1
STTM_AS#	49	PAD74	PAD152 100 SYSERR#
SELECTMAP_CS	50	PAD75	PAD146 98 RESET_BUFPOR#
PMEADY	51	PAD76	PAD145 97
SX95T_CS_B_0	52	PAD77	PAD144 96 USER_DIP0
CPLD_INT	53	PAD81	PAD143 95 USER_DIP1
PPC_RESET	54	PAD82	PAD142 94 USER_DIP2
SYS_CONFIG0	56	PAD86	PAD138 92 USER_DIP3
SYS_CONFIG1	57	PAD87	PAD137 91
SYS_CONFIG2	58	PAD88	PAD134 88
SYS_CONFIG3	59	PAD89	PAD133 87
SYS_CONFIG4	60	PAD90	PAD132 86 NC
SYS_CONFIG5	61	PAD95	PAD131 85 NC
SYS_CONFIG6	64	PAD100	PAD125 83 NC
SYS_CONFIG7	66	PAD102	PAD121 82 NC
NC	68	PAD105	PAD120 81 NC
NC	69	PAD107	PAD119 80 NC
NC	70	PAD108	PAD118 79 NC
RESET_CPLD#	71	PAD109	PAD117 78 NC
NC	74	PAD112	PAD115 77 NC
NC	75	PAD113	PAD114 76 NC

SYS_CONFIG[6:7] 1-3G,1-10E,2-2R

PDATA[0:7] 1-3M,1-5L

PADATA[27:31] 1-3G,1-5L

U54 XC2C256_7VQ144C

BOOT_CFG0 1-2M,1-5G,25-1J
BOOT_CFG1 1-2M,1-5G,25-1J
BOOT_CFG2 1-2M,1-5G,25-1J

R010 R011 R014 — 0402 — NO POP — 3V3

SD/MMC/MMCPLUS CONNECTOR

J17 — SDSR13-A0-0005

4	CMD/DI	DAT0/DO	13
9	CLK/SCLK	DAT1	14
		DAT2	1
8	VDD	DAT3	2
7	VSS1	DAT4	3
11	VSS2	DAT5	5
		DAT6	10
6	SD_CD_COM	DAT7	12
15	SD_WP_COM		
		MNT1	16
		MNT2	17

3V3

R197 R199 — 330R — 0402 — IC1 — 74LVC1G08 — U35 SC70-5 — VCC GND — 3V3 — C615 0.01UF 0402 — PWR_GOOD 1-3G,1-4R,23-1DG

RESETS

CPU_TRST# = '1' when JTAG_TRST# = '1' and RESET_PORT = '1' else '0'; see errata sheet

RESET_PB_POR# 1-2M 1-4G 23-8E
USER_LED0
USER_LED1 — R201 R202 R203 — 1500 — 0402 — LED0 LED1 LED2 — CR3 CR4 CR5 — CR6
SYSERR#
RESET_BUFPOR#

SysErr will be used to drive Status LED (active H)

R194 R195 R196 — 10K — 0402 — SW2 — APEX4 — User DIP-Switch

USER_DIP0
USER_DIP1
USER_DIP2
USER_DIP3

Boot Configuration

R204 R205 R206 — 10K — 0402 — SW3 — APEX4 — Configuration DIP-Switch

CFG_DIP0
CFG_DIP1
CFG_DIP2
MGGEN

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

roach_cpld_XC2C256_7VQ100C_configpins

U54 XC2C256_7VQ144C

NC	2	PAD1	
NC	3	PAD3	
NC	5	PAD5	
NC	6	PAD7	
NC	39	PAD62	
SX95T_TDO	63	TDI	
SX95T_TMS	65	TMS	
SX95T_TCK	67	TCK	
CPLD_TDO	122	TDO	
RESET_PORB	143	PAD218	

1-3G,1-8G,16-2L
1-3G,1-8D,16-2L
1-3G,1-8D,16-2L
1-3M,1-8D,16-2L
1-3G,1-6G,23-9J,25-9G

ENABLE PER_CLK CONNECTION TO CONFIGURATION I/F MUST CO-ORDINATE WITH SX95T_CCLK_0 AND MODE TO AVOID CLASH

R135 10K — PER_CCLK_ENa
R305 330R — R306 240R — CLK_PERCLK 1-2G,1-5L,24-8B,25-6F
SN74AHC1G125DCKT — U2 — DE# A GND VCC Y — C13 100NF 10V — SX95T_CCLK_0 1-3M,1-8G,24-7C

PLACE AT END OF DAISY CHAIN

roach_cpld_XC2C256_7VQ100C_powerpins

U54 XC2C256_7VQ144C

VCC	VAUX	VCCIO_3	VCC_1	VCCIO_4	VCCIO_5	VCC_2	VCCIO_6	VCCIO	VCCIO_1	VCCIO_2
1	8	27	37	55	73	84	93	109	127	141

GND_3	GND_4	GND_5	GND_6	GND_7	GND_8	GND_9	GND_10	GND	GND_1	GND_2
29	36	47	62	72	89	99	99	108	123	144

PLACE NEAR CPLD POWER PINS

C473 C474 C475 C476 C477 C478 C479 C480 C481 C482 C483 — 100NF 10V

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

11-27-2008_13:45

PATH PATH

ROACH_PPC_CPLD

DOC NO: NRF-ADM-XXX-SD-0001
REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 24 OF 25

PDATA[0:31]
1-3M,1-5L

PADD[2:31]

PADD[2:31]
1-3G,1-5L,24-9B

PADD30 IS THE LSB FOR 16 BIT WIDE BUS TRANSFERS

**NOTE:
DMA SIGNALS
IN GREEN TEXT**

PADD2 IS THE MSB

CHIP SELECTS CONFIG

CS0	NOR FLASH - U42
CS1	FPGA - U15
CS2	CPLD - U54
CS3	FPGA - U15
CS4	SELECTMAP_CS
CS5	GPIO - SX95_D_IN

SX95T_D_IN_0 — 1-2M,1-6G,1-8D,16-4B,24-7C,25-7B
POE# — 1-2G,1-6L,24-8C,25-5G,25-7B,25-7M
PB_WE — 1-2G,1-5L,24-10C,25-5G,25-6M,25-7B
PWBE_0# — 1-3G,1-5L,24-9C,25-6M,25-7B
PWBE_1# — 25-6M,25-7C
PWBE_2# — 25-7C
PWBE_3# — 25-7C
PREADY — 1-2M,1-5G,24-6C,25-7B,25-9B
PBLAST# — 25-6M,25-7C
PCS_0 — 1-2G,1-5L,24-10C
PCS_1
PCS_2
SELECTMAP_CS — 1-3G,1-6L,24-6C
SELECTMAP_CS — SX95T_D_IN_0

External Slave Peripheral

U1 — AX82FPX

PERDATA[31:0] — PERADDR[31:0] — PA0031:PA0000
PERCS0# — PCS_0 — PCS0
PERCS1#_GPIO06 — PCS_1 — PCS1
PERCS2# — PCS_2 — PCS2
PERCS4#_GPIO09 — SELECTMAP_CS — PCS4
PERCS5#_GPIO10 — SX95T_D_IN_0 — PCS5
PERDE# — PDE# — PDE
PERWR_WF — PB_WF — PWE
PERBE0#_PWBE_0#
PERBE1#_PWBE_1#
PERBE2#_PWBE_2#
PERBE3#_PWBE_3#
PEREADY — PREADY — PREADY
PERBLAST# — PBLAST# — PBLAST
PERADDR27_GPIO08_DMAREQ2 — PA0027 — DMAREQ2
PERADDR06_GPIO01_DMAACK2 — PA0006 — DMAACK2 — EDT2/TC2
PERADDR05_GPIO02_EDT2_TC2 — PA0005 — DMAREQ3 — EDT3/TC3
GPIO03_PERADDR04_DMAREQ3 — PA0004 — DMAACK3
GPIO04_PERADDR03_DMAACK3 — PA0003
GPIO05_PERADDR02_EDT3_TC3 — PA0002

EXTRESET2 — R6 — CLK_PERCLK — PERCLK — PERERR_GPIO11

R134 R133 R132 R84 R83 R5 3K3 — 3V3

EXT_RESET# — EPB RESET OUTPUT — 1-3G,1-5L,24-10C
CLK_PERCLK — 1-2G,1-5L,24-4C,24-8B

External Master Peripheral Interface

NOT USED
NFALE — NC
NFCLE — NC
NFRENB — NC
NFWENB — NC
NFRDYBUSY#
NFCE3#_PERCS3# — PCS_3

FLASH 32Mx16 (64MB)

U42 — FBGA64 — 32Mx16 MIRROR BIT
PADD30:PA0030 … PADD0:PA0000
WP#/ACC — R4 — PWP# — 1-2M,1-5G,24-7C
DQ15/A-1 — R4 — RY_BY# — 1-3G,1-6L,24-7C
BYTE# — R81 3K3
RESET# — R85 3K3 — 3V3
PCS_0 — PCS0
PDATA15:PDATA0

U44 / U43 — ISL3225ECA

U44 — C192 C194 0.1UF — C193 C195 0.1UF — X_UART1_TX X_UART1_RX X_UART1_RTS# X_UART1_CTS# — R86 10K — RESET_CPLD# — 1-2M,1-5G,24-5C
U43 — C196 C198 0.1UF — C197 C199 0.1UF — X_UART2_TX X_UART2_RX X_UART2_RTS# X_UART2_CTS# — R87 10K — BOOT_CFG2 — 1-2M,1-5G,24-10M — BOOT_CFG1 — 1-2M,1-5G,24-11M — BOOT_CFG0 — 1-2M,1-5G,24-11M

U40 / U45 / U46 — P3SA3157 — TDFN_ZA-6

U40 — C652 0.1UF — UART1_CTS# — R82 3K3 — SX9 BD TO A
U45 — C651 0.1UF — UART2_RTS# — R81 3K3 — SX9 BD TO A
U46 — C650 0.1UF — UART2_CTS# — R80 3K3 — SX9 BD TO A

UART

U1 — UARTSERCLK — CLK_UART_11_0592MHZ — 1-4L,1-6G,23-7G
UART1_TX_UART0_TX — UART1_TX — UART1_TX
UART1_RX_UART0_RX — UART1_RX — UART1_RX
UART1_RTS#_UART0_RTS# — PERPARB_UART1_RTS#
UART1_CTS#_UART0_CTS# — PERPARB_UART1_CTS#
UART2_TX_UART0_DTR# — UART2_TX — UART2_TX
UART2_RX_UART0_RI# — UART2_RX — UART2_RX
UART2_RTS#_UART0_DSR# — CPU_UART0_DSR# — UART2_RTS#
UART2_CTS#_UART0_DCD# — CPU_UART0_DCD# — UART2_CTS#

IIC0 / IIC1_SPI

IIC0SCLK — I2C0_SCLK — 1-4B,1-6L,1-10B,2-2P,22-2F
IIC0SDATA — I2C0_SDATA — 1-3B,1-6L,1-10E
SCPCLKOUT_IIC1SCLK — SCPCLK
SCPDI_IIC1SDATA — SCPDE
SCPDO — SCPDO

I2C0_SCLK / I2C0_SDATA

AT24MAC602 — EE2_BOOT_WP — 1-3M,1-5G,24-7C
EE1_WP — 1-3M,1-6G,24-7C
R88 10K — R89 10K — 3V3

P11 / P4 — 1x5 VT — 0.12A M SMT

PTC6 — MF-NSMF050-2 — 500MA/13.2V — I2C0_SCLK — I2C0_SDATA
PTC5 — MF-NSMF050-2 — 500MA/13.2V — SCPDE — SCPDO
U41 — AD7414-0 — STTM_ALERT — 1-4B,1-6L,23-6M — STTM_AS — 1-3M,1-6G,24-7C
R73 R74 R75 R76 R77 R78 3K3 — SCPCLK

P2 — 3314FDDE 15B-HDCE — SF DSUB MALE

PTC8 — MF-NSMF050-2 — 500MA/13.2V — UART Port 0
C648 0.1UF — J14 — UART Port 1 — HLE-105-02-G-DV
P1 P2 P3 P4 P5 P6 P7 P8 P9 P10 — NC

PADD30:PA0030 … PADD0:PA0000 — PDATA15:PDATA0

PADD30	AE23	PER_A[30]	PER_D[15] AG22 PDATA7
PADD29	AE22	PER_A[29]	PER_D[14] AH22 PDATA6
PADD28	AG18	PER_A[28]	PER_D[13] AH12 PDATA5
PADD27	AG12	PER_A[27]	PER_D[12] AG13 PDATA4
PADD26	AG15	PER_A[26]	PER_D[11] AH20 PDATA3
PADD25	AG23	PER_A[25]	PER_D[10] AH19 PDATA2
PADD24	AF19	PER_A[24]	PER_D[9] AH14 PDATA1
PADD23	AE12	PER_A[23]	PER_D[8] AH13 PDATA0
PADD22	AG16	PER_A[22]	PER_D[7] AF15 PDATA15
PADD21	AF13	PER_A[21]	PER_D[6] AE16 PDATA14
PADD20	AG20	PER_A[20]	PER_D[5] AE21 PDATA13
PADD19	AF23	PER_A[19]	PER_D[4] AD20 PDATA12
PADD18	AH17	PER_A[18]	PER_D[3] AF16 PDATA11
PADD17	AH15	PER_A[17]	PER_D[2] AE17 PDATA10
PADD16	L20	PER_SP_A[16]	PER_D[1] AE19 PDATA9
PADD15	J22	PER_SP_A[15]	PER_D[0] AD19 PDATA8
PADD14	H22	PER_SP_A[14]	
PADD13	L15	PER_SP_A[13]	PER_D_PAR[1] AG21 NC
PADD12	L16	PER_SP_A[12]	PER_D_PAR[0] AE13 NC
PADD11	K22	PER_SP_A[11]	
PADD10	K21	PER_SP_A[10]	PER_INT G23 VS_INT# — 1-4H,1-6L,23-7K
PADD9	K16	PER_SP_A[9]	
PADD8	J15	PER_SP_A[8]	PER_READY K12 PREADY — 1-2M,1-5G,24-6C,25-7B,25-9B
PADD7 DMAREQ2	L21	PER_SP_A[7]	
PADD6 DMAACK2	G22	PER_SP_A[6]	PER_CLK AH18 CLK_PERCLK
PADD5 EDT2/TC2	K23	PER_SP_A[5]	
PADD4 DMAREQ3	K14	PER_SP_A[4]	
PADD3 DMAACK3	L14	PER_SP_A[3]	
PADD2 EDT3/TC3	J12	PER_SP_A[2]	
PCS_1	K13	PER_CS0	
PCS_2	AG17	PER_CS1	
POE# — 1-2G,1-6L,24-8C,25-5G,25-7B,25-10B	AF21	PER_OE_N	
PR_W# — 1-2G,1-5L,24-10C,25-5G,25-7B,25-9B	AF20	PER_R_W_N	
PWBE_1# — 25-7C,25-9B	AF14	PER_WBE[1]	
PWBE_0# — 1-3G,1-5L,24-9C,25-7B,25-9B	AF18	PER_WBE[0]	
PBLAST# — 25-7C,25-9B	H23	PER_B_LAST	

U15 — BANKS=1, 2, 4 — CHIP SELECT 1

3V3_4_1 AL12 — 3V3_4_2 AG14 — 3V3_2 AM19 — 3V3_1_1 AM21 — 3V3_1 G14 — 3V3 D13

C334 470F 6V — C335 470F 6V — C330 220NF 6.3V — C331 220NF 6.3V — C332 220NF 6.3V — C333 220NF 6.3V — GND

Cross-sheet references

1-2G,1-6L,24-8C,25-7B,25-7M,25-10B — PDE#
1-2G,1-5L,24-10C,25-6M,25-7B,25-9B — PB_WE
RESET_PORB# — 1-3G,1-4L,1-6G,23-B3,24-5M

ROUTE AS DAISY CHAIN - U1 - U15 - U2 - U54 - TERMINATION
KEEP STUBS AS SHORT AS POSSIBLE

CLK_UART_11_0592MHZ — 1-4L,1-6G,23-7G

ROACH/iBOB2	ROACH_PPC_NVM_SERIAL
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45 — PATH PATH	DRAWN: F KAPP — APPR:
	CHECKED: E BAUERMEISTER — SHEET 25 OF 25