VIRTEX5

POWER SUPPLY AND MONITORING

ROACH_MONITOR

I2C0_SCLK
FAN2_SENSE
FAN1_SENSE
FAN3_SENSE
3V3_ATX
I2V5
I1V8
I1V5
I1V0
5V_ATX
MGT_AVCC_PG
MGT_AVTTX_PG
MGT_AVCCPLL_PG
PWR_OK
I2V_ATX

PPC_RESET
SYS_CONFIG[0:7]
TDZ
ATRTN1
MONITOR_INT
I2C0_33_DATA
PS_ONB
ATRTN0
TDO
FAN1_CONTROL
LOAD_RES_OFF
2V5_TRACK
2V5_INHIBIT
FAN3_CONTROL
FAN2_CONTROL
MGT_AVTTX_EN
MGT_AVCCPLL_EN
MGT_AVCC_EN
1V8_INHIBIT
1V5_INHIBIT
1V0_INHIBIT

ROACH_PSU

LOAD_RES_OFF
FAN1_CONTROL
PS_ONB
FAN2_CONTROL
FAN3_CONTROL
1V0_INHIBIT
1V5_INHIBIT
1V8_INHIBIT
2V5_TRACK
2V5_INHIBIT

12V_ATX
3V3_ATX
5V_ATX
PWR_OK
FAN1_SENSE
FAN2_SENSE
FAN3_SENSE
I1V0
I1V5
I1V8
I2V5

VIRTEX5 CLOCKS

ROACH_V5_CLK

SX95T_DXN
SX95T_DXP
ATRTN0
TDO

V5 DDR2 MEMORY

ROACH_DDR2_DIMM

GIGABIT TRANSCEIVERS

ROACH_TRANSCEIVERS0_1

ROACH_TRANSCEIVERS2_3

ROACH_TRANSCEIVERS_PSU

MGT_AVCC_EN
MGT_AVCCPLL_EN
MGT_AVTTX_EN
MGT_AVCC_PG
MGT_AVTTX_PG
MGT_AVCCPLL_PG

ZDOK/ADC INTERFACE

ROACH_ADC_0

ROACH_ADC_1

V5 DIFFERENTIAL GPIO

ROACH_DIFF_GPIO

QDRII+ MEMORY

ROACH_QDR2P_BY0_1

QDR2_TDI
QDR2_TCK
QDR2_TMS
QDR2_BY0_1_TDO

ROACH_QDR2P_BY2_3

QDR2_BY2_3_TDO

V5 POWER

ROACH_5V_POWER

VIRTEX5 CONFIGURATION

ROACH_CONFIG

SX95T_D_IN_0
SX95T_TCK
SX95T_TMS
SX95T_TDI
SX95T_RDWR_B_0
SX95T_PROGRAM_B_0
SX95T_CS_B_0

SX95T_M2_0
SX95T_M1_0
SX95T_M0_0
SX95T_DONE_0
SX95T_CCLK_0
SX95T_D_OUT_BUSY_0
SX95T_INIT_B_0
SX95T_TDO

V5 SE GPIO & MISCELLANEOUS

ROACH_GPIO_MISC

PPC

ROACH_PPC_POWER_1

ROACH_PPC_POWER_2

ROACH_PPC_PCI

ROACH_PPC_ETH1

GETH0_RST#
CLK_GETH0_25MHZ
GMCMDIO
GMCMDCLK
GETH0_INT#

ROACH_PPC_USB

CONTAINS GPIO TO CONFIG INTERFACE

CLK_USB2_48MHZ

ROACH_PPC_DDR2

PPC_DDR2_RESET_N

ROACH_PPC_NVM_SERIAL

CLK_UART_11_0592MHZ
M66EN
EE1_WP
STTM_AS
PORT_POR#
FWP#
EE2_BOOT_WP
BOOT_CFG0
BOOT_CFG1
BOOT_CFG2
RESET_CPLD#

VS_INT#
SELECTMAP_CS
I2C0_SCLK
I2C0_33_DATA
SCPDI
SCPCLK
STTM_ALERT
SCPDO
POE#
FRY_BY#
CLK_PERCLK
PWBE_0#
PR_WE#
PCS_2
PDATA[8:31]
PADD[2:31]
EXT_RESET#

ROACH_PPC_TST_CLK_IO

GETH0_INT#
MONITOR_INT
VS_INT#
STTM_ALERT
SX95T_TDO
RESET_PB_POR#
PWR_GOOD
CPU_TRST#
CLK_SEL_M66EN
SEL_SYSCLK
CLK_TMRCLK

PPC_THERMONA
PPC_THERMONB
GPIO44
SX95T_TDI
SX95T_TCK
SX95T_TMS
RESET_POR#
DEBUG_TRST#
CLK_GETH0_25MHZ
CLK_USB2_48MHZ
CLK_CPLD_50MHZ
SYSERR
CLK_UART_11_0592MHZ
CLK_CPLD_33MHZ

ROACH_PPC_CPLD

SYS_CONFIG[0:7]
PPC_RESET
PWR_GOOD
EXT_RESET#
RESET_POR#
PWBE_0#
PADD[27:31]
SELECTMAP_CS
FRY_BY#
SYSERR
CLK_CPLD_33MHZ
DEBUG_TRST#
CLK_PERCLK
CLK_CPLD_50MHZ
PR_WE#
POE#
PCS_2
SX95T_D_OUT_BUSY_0
M66EN
SX95T_M0_0
SX95T_M1_0
SX95T_M2_0

GETH0_RST#
PPC_DDR2_RESET_N
PDATA[0:7]
RESET_PB_POR#
SX95T_CCLK_0
STTM_AS
EE2_BOOT_WP
EE1_WP
CPU_TRST#
SEL_SYSCLK
CLK_SEL_M66EN
CLK_TMRCLK
SX95T_RDWR_B_0
FWP#
RESET_CPLD#
SX95T_INIT_B_0
SX95T_DONE_0
SX95T_PROGRAM_B_0
SX95T_D_IN_0
SX95T_CS_B_0
BOOT_CFG0
BOOT_CFG1
BOOT_CFG2

MECHANICAL

GND

U3

U49

PLACEHOLDER FOR PCB
MEERKAT LOGO

PLACEHOLDER FOR PCB
CASPER LOGO

PLACEHOLDER FOR PCB
NRAO LOGO

BOARD SERIAL NUMBER

CONTRIBUTORS

ETIENNE BAUERMEISTER
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FRANCOIS KAPP
ALAN LANDMAN
GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

2-22-2008_13:23

PATH PATH

ROACH_TOP

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 1 OF 25

roach_AFS600_pcb

TIE TO GROUND IF PLL'S ARE NOT USED

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

PLACE AT ACTEL 1V5 POWER PINS

PLACE AT ACTEL 3V3 POWER PINS

roach_AFS600_powerpins

roach_AFS600_configpins

PB POWER SWITCH

KEY - REMOVE PIN

MONITOR RESET

XPORT - PLACE IN REAR I/O REGION
XP1001001-03R

TEMPERATURE DIODE HEADER

ACTEL JTAG CONNECTOR

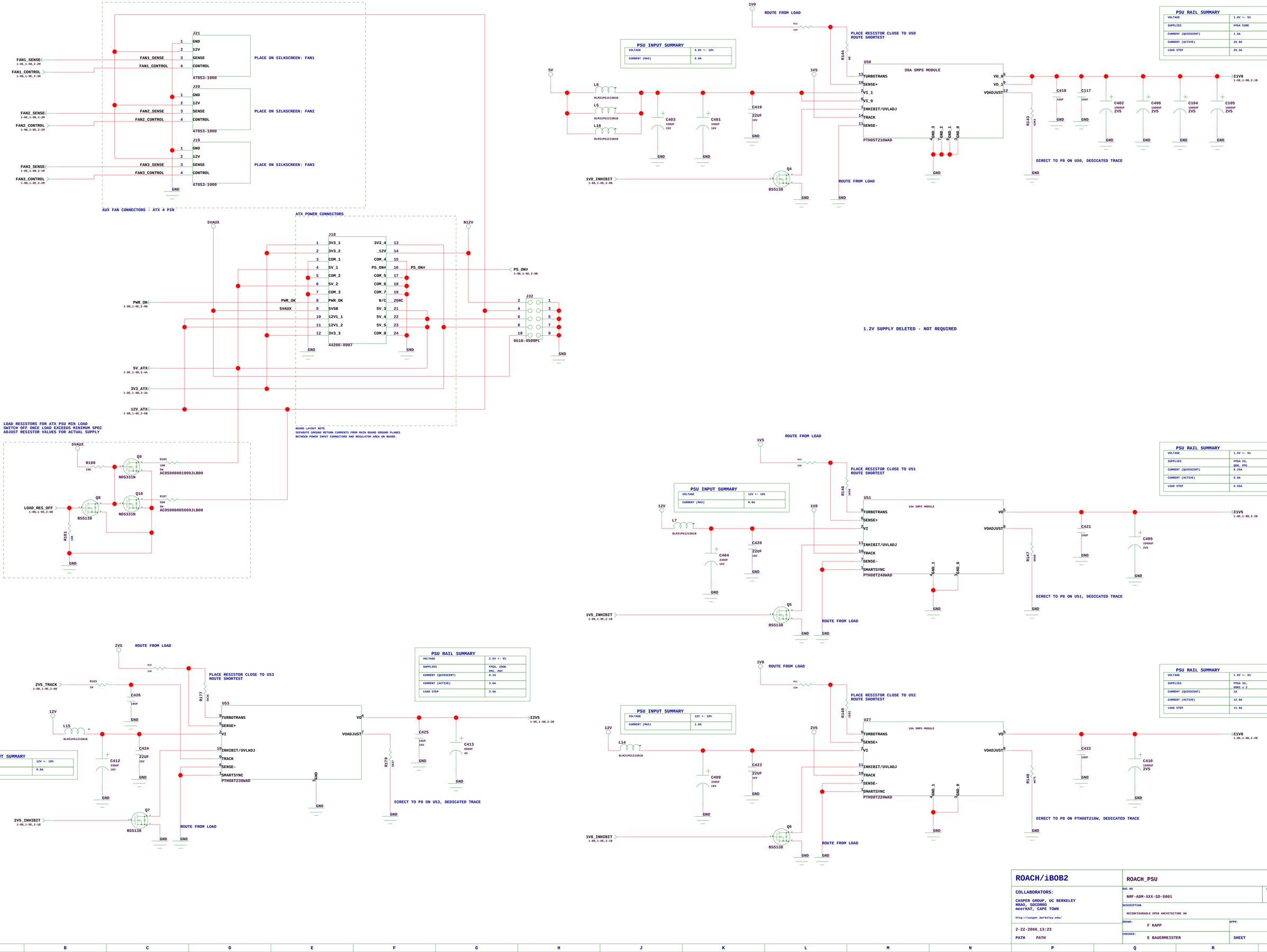
REFERENCE RESISTOR/ADC VALUES

VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)
12V	0R01	3.36	0.11
5V	0R0047	6.78	0.22
3V3	0R01	3.47	0.12
2V5	0R01	3.56	0.13
1V8	0R0022	12.91	0.37
1V5	0R0047	6.77	0.22
1V0	0R001	26.79	0.72

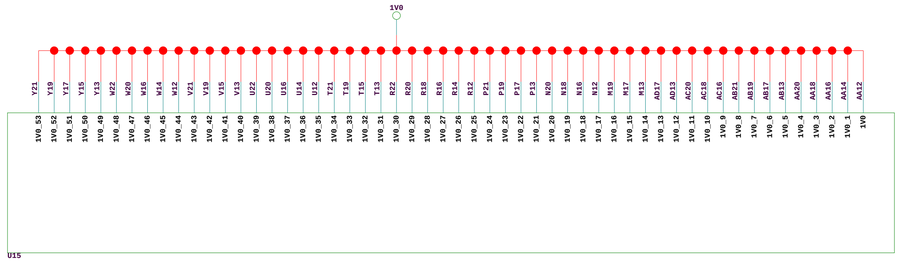
FOR 8 BIT ADC USING 2.56V REFERENCE:

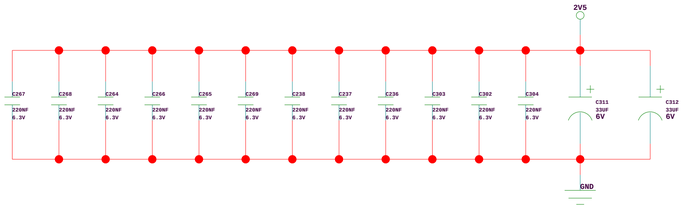
ADC COUNT AT MAX POWER	CURRENT/BIT (A)
33	0.1
31	0.21
34	0.1
35	0.1
28	0.45
31	0.21
26	1.0

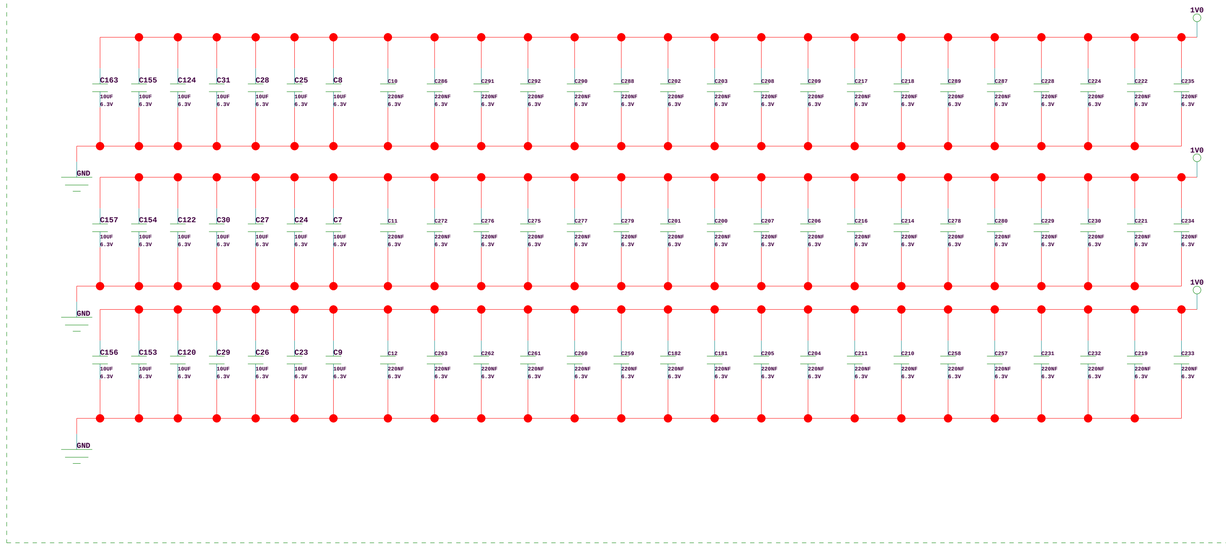
ROACH/iBOB2	ROACH_MONITOR
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
2-22-2008_13:23	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 2 OF 25

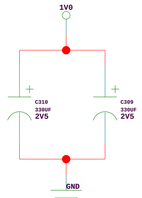


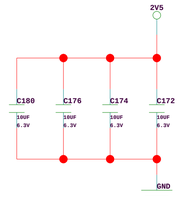
ROACH/iBOB2	ROACH_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-22-2008_13:23; PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 3 OF 25

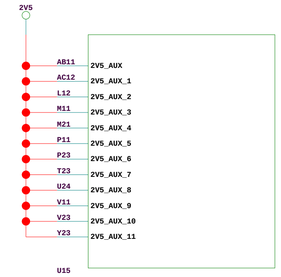


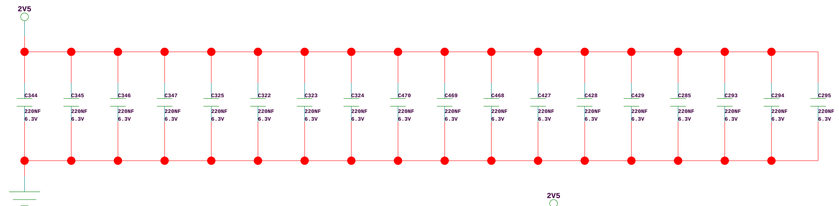


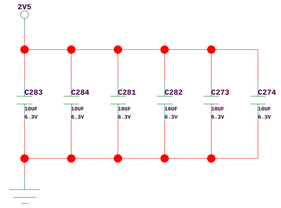


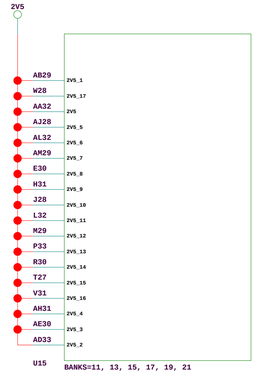


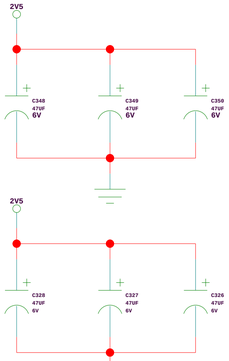


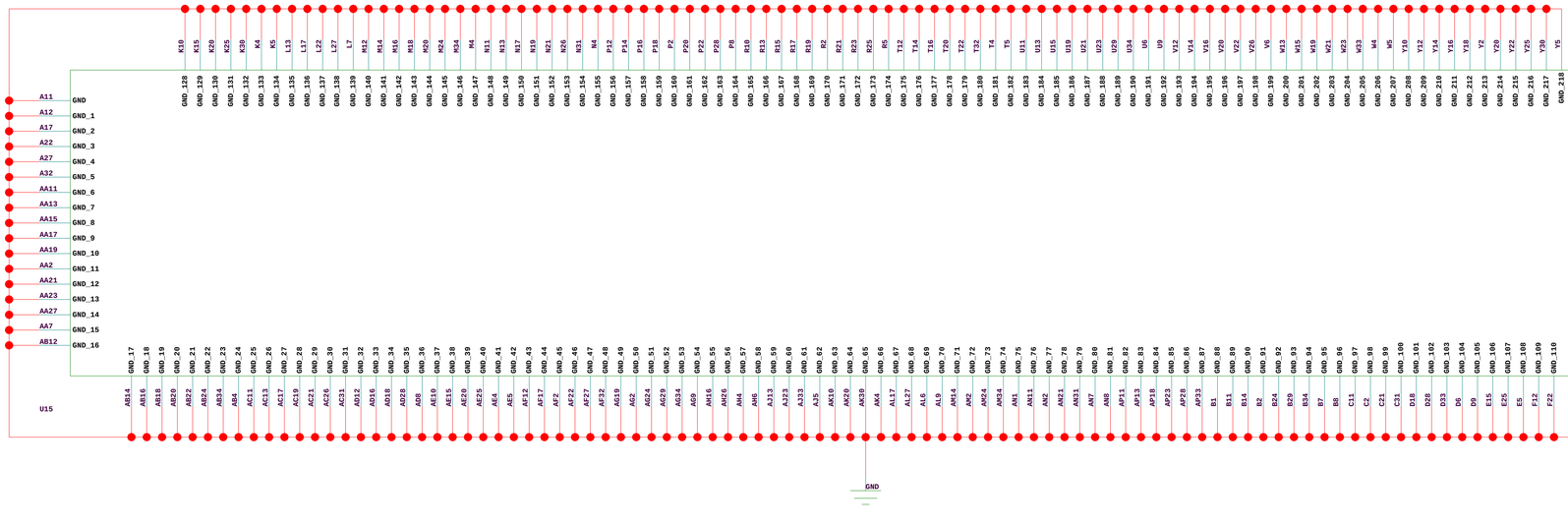












ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

2-22-2008_13:23

PATH PATH

ROACH_5V_POWER

DOC NO NRF-ADM-XXX-SD-0001

REVISION A

DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 4 OF 25

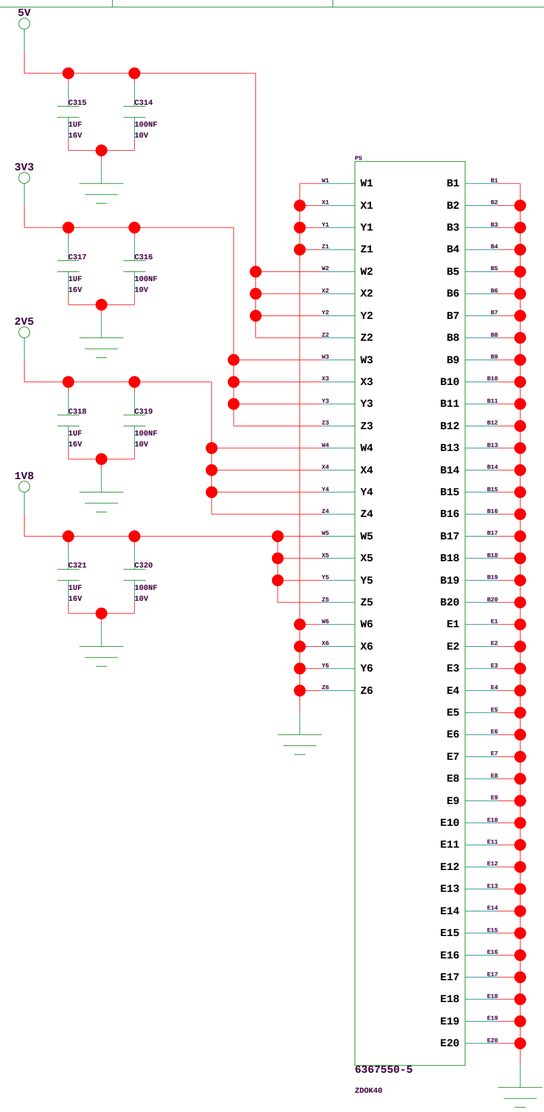
A		B		C		D		E		F		G		H		J		K		L		M		

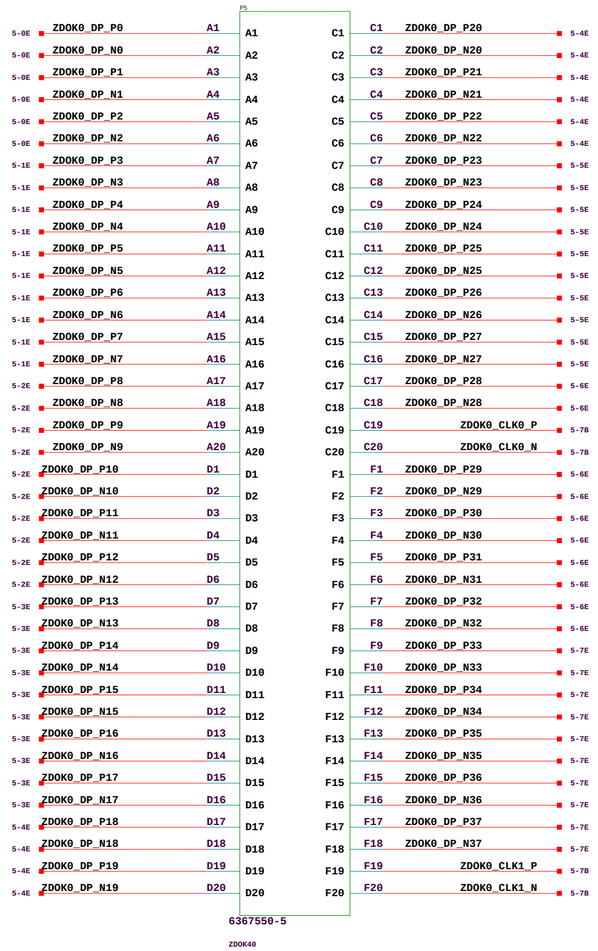
5-5L	ZDOK0_CLK0_P	J20	ZDOK0_CLK0_P
5-5L	ZDOK0_CLK0_N	J21	ZDOK0_CLK0_N
5-3L	ZDOK0_CLK1_P	H19	ZDOK0_CLK1_P
5-3L	ZDOK0_CLK1_N	H20	ZDOK0_CLK1_N

ZDOK0_DP_P[37]	B33	ZDOK0_DP_P37	5-3L
ZDOK0_DP_N[37]	C33	ZDOK0_DP_N37	5-3L
ZDOK0_DP_P[36]	F25	ZDOK0_DP_P36	5-3L
ZDOK0_DP_N[36]	F26	ZDOK0_DP_N36	5-3L
ZDOK0_DP_P[35]	E32	ZDOK0_DP_P35	5-4L
ZDOK0_DP_N[35]	E33	ZDOK0_DP_N35	5-4L
ZDOK0_DP_P[34]	F33	ZDOK0_DP_P34	5-4L
ZDOK0_DP_N[34]	E34	ZDOK0_DP_N34	5-4L
ZDOK0_DP_P[33]	G32	ZDOK0_DP_P33	5-4L
ZDOK0_DP_N[33]	H32	ZDOK0_DP_N33	5-4L
ZDOK0_DP_P[32]	J27	ZDOK0_DP_P32	5-4L
ZDOK0_DP_N[32]	J26	ZDOK0_DP_N32	5-4L
ZDOK0_DP_P[31]	H34	ZDOK0_DP_P31	5-4L
ZDOK0_DP_N[31]	J34	ZDOK0_DP_N31	5-4L
ZDOK0_DP_P[30]	K31	ZDOK0_DP_P30	5-5L
ZDOK0_DP_N[30]	L31	ZDOK0_DP_N30	5-5L
ZDOK0_DP_P[29]	L30	ZDOK0_DP_P29	5-5L
ZDOK0_DP_N[29]	M30	ZDOK0_DP_N29	5-5L
ZDOK0_DP_P[28]	C34	ZDOK0_DP_P28	5-5L
ZDOK0_DP_N[28]	D34	ZDOK0_DP_N28	5-5L
ZDOK0_DP_P[27]	E29	ZDOK0_DP_P27	5-5L
ZDOK0_DP_N[27]	F29	ZDOK0_DP_N27	5-5L
ZDOK0_DP_P[26]	H25	ZDOK0_DP_P26	5-6L
ZDOK0_DP_N[26]	H24	ZDOK0_DP_N26	5-6L
ZDOK0_DP_P[25]	G30	ZDOK0_DP_P25	5-6L
ZDOK0_DP_N[25]	F30	ZDOK0_DP_N25	5-6L
ZDOK0_DP_P[24]	G33	ZDOK0_DP_P24	5-6L
ZDOK0_DP_N[24]	F34	ZDOK0_DP_N24	5-6L
ZDOK0_DP_P[23]	J30	ZDOK0_DP_P23	5-6L
ZDOK0_DP_N[23]	J31	ZDOK0_DP_N23	5-6L
ZDOK0_DP_P[22]	L25	ZDOK0_DP_P22	5-6L
ZDOK0_DP_N[22]	L26	ZDOK0_DP_N22	5-6L
ZDOK0_DP_P[21]	L29	ZDOK0_DP_P21	5-7L
ZDOK0_DP_N[21]	K29	ZDOK0_DP_N21	5-7L
ZDOK0_DP_P[20]	N27	ZDOK0_DP_P20	5-7L
ZDOK0_DP_N[20]	M27	ZDOK0_DP_N20	5-7L
ZDOK0_DP_P[19]	B32	ZDOK0_DP_P19	5-3J
ZDOK0_DP_N[19]	A33	ZDOK0_DP_N19	5-3J
ZDOK0_DP_P[18]	E26	ZDOK0_DP_P18	5-3J
ZDOK0_DP_N[18]	E27	ZDOK0_DP_N18	5-3J
ZDOK0_DP_P[17]	G25	ZDOK0_DP_P17	5-3J
ZDOK0_DP_N[17]	G26	ZDOK0_DP_N17	5-3J
ZDOK0_DP_P[16]	G27	ZDOK0_DP_P16	5-4J
ZDOK0_DP_N[16]	H27	ZDOK0_DP_N16	5-4J
ZDOK0_DP_P[15]	J24	ZDOK0_DP_P15	5-4J
ZDOK0_DP_N[15]	J25	ZDOK0_DP_N15	5-4J
ZDOK0_DP_P[14]	H30	ZDOK0_DP_P14	5-4J
ZDOK0_DP_N[14]	G31	ZDOK0_DP_N14	5-4J
ZDOK0_DP_P[13]	K27	ZDOK0_DP_P13	5-4J
ZDOK0_DP_N[13]	K26	ZDOK0_DP_N13	5-4J
ZDOK0_DP_P[12]	J32	ZDOK0_DP_P12	5-4J
ZDOK0_DP_N[12]	H33	ZDOK0_DP_N12	5-4J
ZDOK0_DP_P[11]	K33	ZDOK0_DP_P11	5-5J
ZDOK0_DP_N[11]	K32	ZDOK0_DP_N11	5-5J
ZDOK0_DP_P[10]	L34	ZDOK0_DP_P10	5-5J
ZDOK0_DP_N[10]	K34	ZDOK0_DP_N10	5-5J
ZDOK0_DP_P[9]	C32	ZDOK0_DP_P9	5-5J
ZDOK0_DP_N[9]	D32	ZDOK0_DP_N9	5-5J
ZDOK0_DP_P[8]	E28	ZDOK0_DP_P8	5-5J
ZDOK0_DP_N[8]	F28	ZDOK0_DP_N8	5-5J
ZDOK0_DP_P[7]	F31	ZDOK0_DP_P7	5-5J
ZDOK0_DP_N[7]	E31	ZDOK0_DP_N7	5-5J
ZDOK0_DP_P[6]	H28	ZDOK0_DP_P6	5-6J
ZDOK0_DP_N[6]	G28	ZDOK0_DP_N6	5-6J
ZDOK0_DP_P[5]	H29	ZDOK0_DP_P5	5-6J
ZDOK0_DP_N[5]	J29	ZDOK0_DP_N5	5-6J
ZDOK0_DP_P[4]	K24	ZDOK0_DP_P4	5-6J
ZDOK0_DP_N[4]	L24	ZDOK0_DP_N4	5-6J
ZDOK0_DP_P[3]	K28	ZDOK0_DP_P3	5-6J
ZDOK0_DP_N[3]	L28	ZDOK0_DP_N3	5-6J
ZDOK0_DP_P[2]	M25	ZDOK0_DP_P2	5-6J
ZDOK0_DP_N[2]	M26	ZDOK0_DP_N2	5-6J
ZDOK0_DP_P[1]	M28	ZDOK0_DP_P1	5-7J
ZDOK0_DP_N[1]	N28	ZDOK0_DP_N1	5-7J
ZDOK0_DP_P[0]	M31	ZDOK0_DP_P0	5-7J
ZDOK0_DP_N[0]	N30	ZDOK0_DP_N0	5-7J

U15

BANKS=11, 13, 15, 17, 19, 21





ROACH/iBOB2	**ROACH_ADC_0**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-22-2008_13:23 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 5 OF 25

A		B		C		D		E		F		G		H		J		K		L		M		


ZDOK1_CLK0_P H17
ZDOK1_CLK0_N H18
ZDOK1_CLK1_P K17
ZDOK1_CLK1_N L18
ZDOK1_CLK0_P
ZDOK1_CLK0_N
ZDOK1_CLK1_P
ZDOK1_CLK1_N
AD31 ZDOK1_DP_P37
AE31 ZDOK1_DP_N37
AF33 ZDOK1_DP_P36
AE33 ZDOK1_DP_N36
AF31 ZDOK1_DP_P35
AG31 ZDOK1_DP_N35
AG32 ZDOK1_DP_P34
AH32 ZDOK1_DP_N34
AG28 ZDOK1_DP_P33
AH28 ZDOK1_DP_N33
AF24 ZDOK1_DP_P32
AG25 ZDOK1_DP_N32
AJ30 ZDOK1_DP_P31
AH30 ZDOK1_DP_N31
AK28 ZDOK1_DP_P30
AK27 ZDOK1_DP_N30
AK26 ZDOK1_DP_P29
AJ27 ZDOK1_DP_N29
AB27 ZDOK1_DP_P28
AC27 ZDOK1_DP_N28
AD30 ZDOK1_DP_P27
AC29 ZDOK1_DP_N27
AE29 ZDOK1_DP_P26
AD29 ZDOK1_DP_N26
AG33 ZDOK1_DP_P25
AH33 ZDOK1_DP_N25
AF29 ZDOK1_DP_P24
AF30 ZDOK1_DP_N24
AG27 ZDOK1_DP_P23
AG26 ZDOK1_DP_N23
AK34 ZDOK1_DP_P22
AK33 ZDOK1_DP_N22
AL34 ZDOK1_DP_P21
AL33 ZDOK1_DP_N21
AJ25 ZDOK1_DP_P20
AH25 ZDOK1_DP_N20
AB30 ZDOK1_DP_P19
AC30 ZDOK1_DP_N19
AC28 ZDOK1_DP_P18
AD27 ZDOK1_DP_N18
AC25 ZDOK1_DP_P17
AC24 ZDOK1_DP_N17
AE28 ZDOK1_DP_P16
AF28 ZDOK1_DP_N16
AD24 ZDOK1_DP_P15
AE24 ZDOK1_DP_N15
AF25 ZDOK1_DP_P14
AF26 ZDOK1_DP_N14
AH29 ZDOK1_DP_P13
AG30 ZDOK1_DP_N13
AH27 ZDOK1_DP_P12
AJ26 ZDOK1_DP_N12
AM33 ZDOK1_DP_P11
AM32 ZDOK1_DP_N11
AN32 ZDOK1_DP_P10
AP32 ZDOK1_DP_N10
AC34 ZDOK1_DP_P9
AD34 ZDOK1_DP_N9
AD32 ZDOK1_DP_P8
AE32 ZDOK1_DP_N8
AF34 ZDOK1_DP_P7
AE34 ZDOK1_DP_N7
AD26 ZDOK1_DP_P6
AD25 ZDOK1_DP_N6
AE27 ZDOK1_DP_P5
AE26 ZDOK1_DP_N5
AH34 ZDOK1_DP_P4
AJ34 ZDOK1_DP_N4
AJ32 ZDOK1_DP_P3
AK32 ZDOK1_DP_N3
AJ31 ZDOK1_DP_P2
AK31 ZDOK1_DP_N2
AK29 ZDOK1_DP_P1
AJ29 ZDOK1_DP_N1
AN34 ZDOK1_DP_P0
AN33 ZDOK1_DP_N0
U15
BANKS=11, 13, 15, 17, 19, 21
5V
3V3
2V5
1V8
C337 1UF 16V
C336 100NF 10V
C339 1UF 16V
C338 100NF 10V
C340 1UF 16V
C341 100NF 10V
C343 1UF 16V
C342 100NF 10V
P7
6367550-5
ZDOK40
ZDOK1_DP_P0 A1
ZDOK1_DP_N0 A2
ZDOK1_DP_P1 A3
ZDOK1_DP_N1 A4
ZDOK1_DP_P2 A5
ZDOK1_DP_N2 A6
ZDOK1_DP_P3 A7
ZDOK1_DP_N3 A8
ZDOK1_DP_P4 A9
ZDOK1_DP_N4 A10
ZDOK1_DP_P5 A11
ZDOK1_DP_N5 A12
ZDOK1_DP_P6 A13
ZDOK1_DP_N6 A14
ZDOK1_DP_P7 A15
ZDOK1_DP_N7 A16
ZDOK1_DP_P8 A17
ZDOK1_DP_N8 A18
ZDOK1_DP_P9 A19
ZDOK1_DP_N9 A20
ZDOK1_DP_P10 D1
ZDOK1_DP_N10 D2
ZDOK1_DP_P11 D3
ZDOK1_DP_N11 D4
ZDOK1_DP_P12 D5
ZDOK1_DP_N12 D6
ZDOK1_DP_P13 D7
ZDOK1_DP_N13 D8
ZDOK1_DP_P14 D9
ZDOK1_DP_N14 D10
ZDOK1_DP_P15 D11
ZDOK1_DP_N15 D12
ZDOK1_DP_P16 D13
ZDOK1_DP_N16 D14
ZDOK1_DP_P17 D15
ZDOK1_DP_N17 D16
ZDOK1_DP_P18 D17
ZDOK1_DP_N18 D18
ZDOK1_DP_P19 D19
ZDOK1_DP_N19 D20
C1 ZDOK1_DP_P20
C2 ZDOK1_DP_N20
C3 ZDOK1_DP_P21
C4 ZDOK1_DP_N21
C5 ZDOK1_DP_P22
C6 ZDOK1_DP_N22
C7 ZDOK1_DP_P23
C8 ZDOK1_DP_N23
C9 ZDOK1_DP_P24
C10 ZDOK1_DP_N24
C11 ZDOK1_DP_P25
C12 ZDOK1_DP_N25
C13 ZDOK1_DP_P26
C14 ZDOK1_DP_N26
C15 ZDOK1_DP_P27
C16 ZDOK1_DP_N27
C17 ZDOK1_DP_P28
C18 ZDOK1_DP_N28
C19 ZDOK1_CLK0_P
C20 ZDOK1_CLK0_N
F1 ZDOK1_DP_P29
F2 ZDOK1_DP_N29
F3 ZDOK1_DP_P30
F4 ZDOK1_DP_N30
F5 ZDOK1_DP_P31
F6 ZDOK1_DP_N31
F7 ZDOK1_DP_P32
F8 ZDOK1_DP_N32
F9 ZDOK1_DP_P33
F10 ZDOK1_DP_N33
F11 ZDOK1_DP_P34
F12 ZDOK1_DP_N34
F13 ZDOK1_DP_P35
F14 ZDOK1_DP_N35
F15 ZDOK1_DP_P36
F16 ZDOK1_DP_N36
F17 ZDOK1_DP_P37
F18 ZDOK1_DP_N37
F19 ZDOK1_CLK1_P
F20 ZDOK1_CLK1_N
6367550-5
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
2-22-2008_13:23
PATH PATH
ROACH_ADC_1
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 6 OF 25

MAIN CLOCK - 100MHZ

CRYSTEK
CCLD-023-25-100.000
100.00MHZ
EPSON TOYOCOM
EG2121CA100.000LHPN

IODELAY CLOCK - 200MHZ

CRYSTEK
CCLD-024-25-200.000
200.00MHZ
EPSON TOYOCOM
EG2121CA200.000LHPN

PLACE CLOSE TO CONNECTORS

POPULATE JUMPER FOR DC COUPLING

POPULATE JUMPER FOR DC COUPLING

BANKS=3

ADCMP605BCPZ

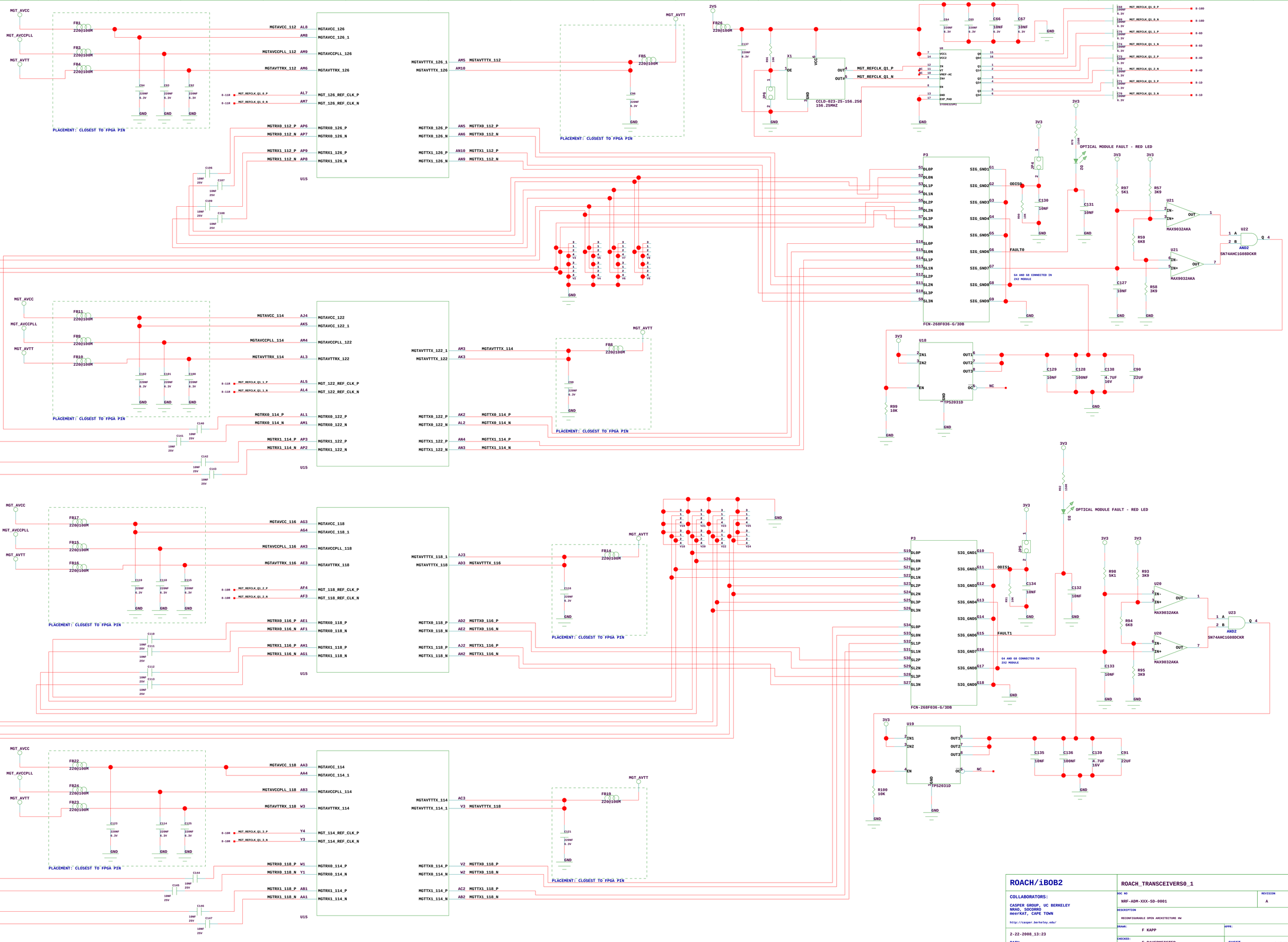
ADCMP605BCPZ

ADR03AUJ-R2

LVDS

LVDS

ROACH/iBOB2	ROACH_V5_CLK
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-22-2008_13:23	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 7 OF 25


MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB3 220@100M
FB4 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_112 AL8 MGTAVCC_126
AM8 MGTAVCC_126_1
MGTAVCCPLL_112 AM9 MGTAVCCPLL_126
MGTAVTTRX_112 AM6 MGTAVTTRX_126
MGT_REFCLK_Q1_0_P AL7 MGT_126_REF_CLK_P
MGT_REFCLK_Q1_0_N AM7 MGT_126_REF_CLK_N
MGTRX0_112_P AP6 MGTRX0_126_P
MGTRX0_112_N AP7 MGTRX0_126_N
MGTRX1_112_P AP9 MGTRX1_126_P
MGTRX1_112_N AP8 MGTRX1_126_N
U15
MGTAVTTTX_126_1 AM5 MGTAVTTTX_112
MGTAVTTTX_126 AM10
MGTTX0_126_P AN5 MGTTX0_112_P
MGTTX0_126_N AN6 MGTTX0_112_N
MGTTX1_126_P AN10 MGTTX1_112_P
MGTTX1_126_N AN9 MGTTX1_112_N
FB5 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
2V5
FB26 220@100M
X1
CCLD-023-25-156.250 156.25MHZ
OUT MGT_REFCLK_Q1_P
OUT MGT_REFCLK_Q1_N
VCC
OE
GND
JP6
R88 10K
C68 MGT_REFCLK_Q1_0_P
C69 MGT_REFCLK_Q1_0_N
C75 MGT_REFCLK_Q1_1_P
C74 MGT_REFCLK_Q1_1_N
C73 MGT_REFCLK_Q1_2_P
C72 MGT_REFCLK_Q1_2_N
C71 MGT_REFCLK_Q1_3_P
C70 MGT_REFCLK_Q1_3_N
220NF 6.3V
B-10D
B-6D
B-4D
B-1D
P3
FCN-268F036-G/3DB
SIG_GND1 SIG_GND2 SIG_GND3 SIG_GND4 SIG_GND5 SIG_GND6 SIG_GND7 SIG_GND8 SIG_GND9
ODIS0
FAULT0
G4 AND G8 CONNECTED IN 2X2 MODULE
JP4
R89 10K
C130 10NF
C131 10NF
R95 3K9
R97 5K1
R59 100R
OPTICAL MODULE FAULT - RED LED
U21 MAX9032AKA
U22 SN74AHC1G08DCKR AND2
RS7 3K9
RS9 6K8
RS8 3K9
C127 10NF
3V3
GND
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB11 220@100M
FB9 220@100M
FB10 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_114 AJ4 MGTAVCC_122
AK5 MGTAVCC_122_1
MGTAVCCPLL_114 AM4 MGTAVCCPLL_122
MGTAVTTRX_114 AL3 MGTAVTTRX_122
MGT_REFCLK_Q3_1_P AL5 MGT_122_REF_CLK_P
MGT_REFCLK_Q3_1_N AL4 MGT_122_REF_CLK_N
MGTRX0_114_P AL1 MGTRX0_122_P
MGTRX0_114_N AM1 MGTRX0_122_N
MGTRX1_114_P AP3 MGTRX1_122_P
MGTRX1_114_N AP2 MGTRX1_122_N
U15
MGTAVTTTX_122_1 AM3 MGTAVTTTX_114
MGTAVTTTX_122 AK3
MGTTX0_122_P AK2 MGTTX0_114_P
MGTTX0_122_N AL2 MGTTX0_114_N
MGTTX1_122_P AN4 MGTTX1_114_P
MGTTX1_122_N AN3 MGTTX1_114_N
FB8 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
U18 TPS2031D
R99 10K
C129 10NF
C128 100NF
C138 4.7UF 16V
C90 22UF
C135 10NF
C136 100NF
C139 4.7UF 16V
C91 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB17 220@100M
FB15 220@100M
FB16 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_116 AG3 MGTAVCC_118
AG4 MGTAVCC_118_1
MGTAVCCPLL_116 AH3 MGTAVCCPLL_118
MGTAVTTRX_116 AE3 MGTAVTTRX_118
MGT_REFCLK_Q3_2_P AF4 MGT_118_REF_CLK_P
MGT_REFCLK_Q3_2_N AF3 MGT_118_REF_CLK_N
MGTRX0_116_P AE1 MGTRX0_118_P
MGTRX0_116_N AF1 MGTRX0_118_N
MGTRX1_116_P AH1 MGTRX1_118_P
MGTRX1_116_N AG1 MGTRX1_118_N
U15
MGTAVTTTX_118_1 AJ3 MGTAVTTTX_116
MGTAVTTTX_118 AD3 MGTAVTTTX_116
MGTTX0_118_P AD2 MGTTX0_116_P
MGTTX0_118_N AE2 MGTTX0_116_N
MGTTX1_118_P AJ2 MGTTX1_116_P
MGTTX1_118_N AH2 MGTTX1_116_N
FB14 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
JP5
R98 5K1
R94 6K8
R93 3K9
R92 100R
OPTICAL MODULE FAULT - RED LED
U20 MAX9032AKA
U23 SN74AHC1G08DCKR AND2
C132 10NF
C133 10NF
R95 3K9
FAULT1
ODIS1
G4 AND G8 CONNECTED IN 2X2 MODULE
FCN-268F036-G/3DB
U19 TPS2031D
R100 10K
C135 10NF
C136 100NF
C139 4.7UF 16V
C91 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB22 220@100M
FB24 220@100M
FB23 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_118 AA3 MGTAVCC_114
AA4 MGTAVCC_114_1
MGTAVCCPLL_118 AB3 MGTAVCCPLL_114
MGTAVTTRX_118 W3 MGTAVTTRX_114
MGT_REFCLK_Q3_3_P Y4 MGT_114_REF_CLK_P
MGT_REFCLK_Q3_3_N Y3 MGT_114_REF_CLK_N
MGTRX0_118_P W1 MGTRX0_114_P
MGTRX0_118_N Y1 MGTRX0_114_N
MGTRX1_118_P AB1 MGTRX1_114_P
MGTRX1_118_N AA1 MGTRX1_114_N
U15
MGTAVTTTX_114 AC3 MGTAVTTTX_118
MGTAVTTTX_114_1 V3 MGTAVTTTX_118
MGTTX0_114_P V2 MGTTX0_118_P
MGTTX0_114_N W2 MGTTX0_118_N
MGTTX1_114_P AC2 MGTTX1_118_P
MGTTX1_114_N AB2 MGTTX1_118_N
FB19 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
2-22-2008_13:23
PATH
ROACH_TRANSCEIVERS0_1
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE MW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 8 OF 25

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

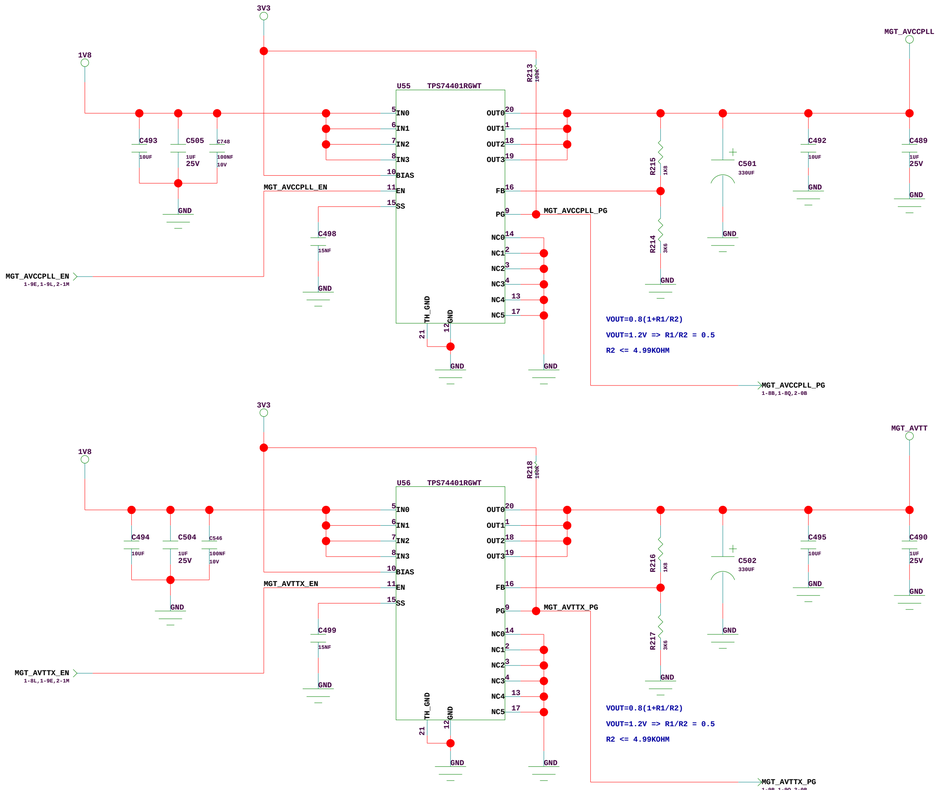
G4 AND G8 CONNECTED IN 2X2 MODULE

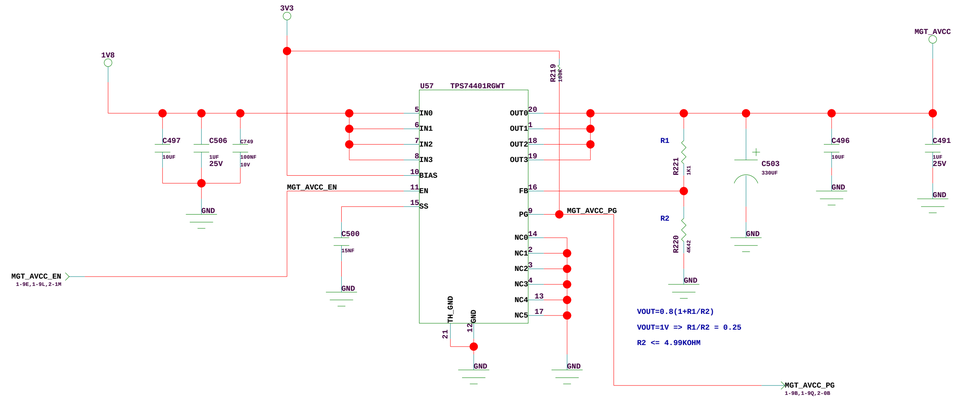
OPTICAL MODULE FAULT - RED LED

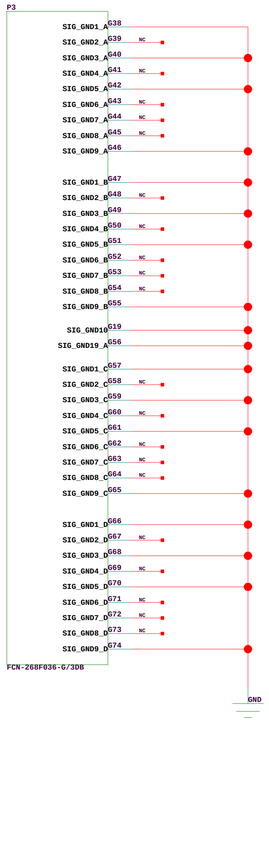
CCLD-023-25-156.250
156.25MHZ

FCN-268F036-G/3DB

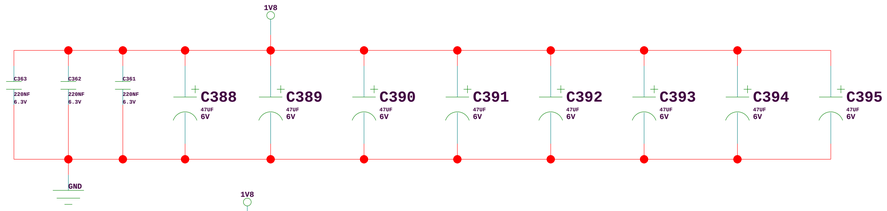
ROACH/iBOB2	ROACH_TRANSCEIVERS2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-22-2008_13:23	DRAWN: F KAPP APPR:
PATH PATH	CHECKED: E BAUERMEISTER SHEET 9 OF 25

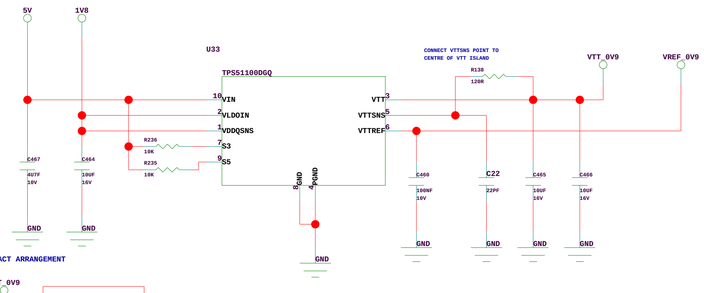




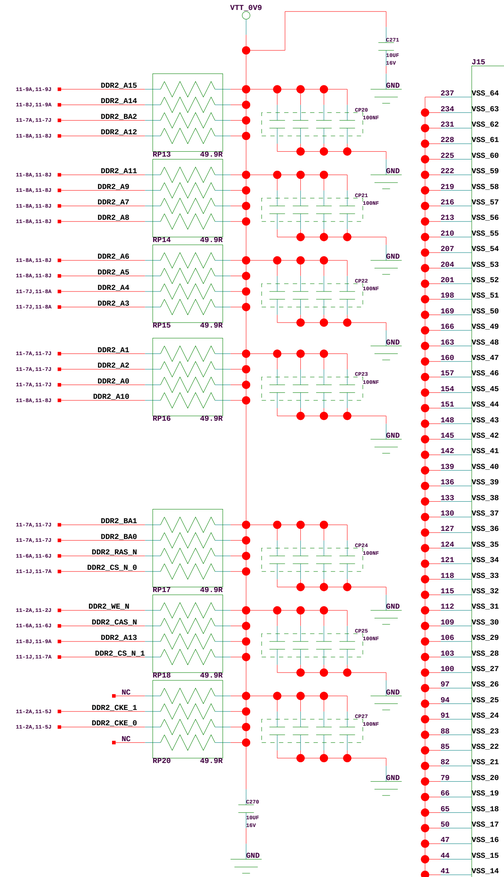


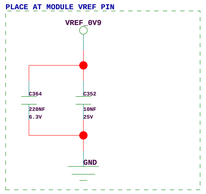
ROACH/iBOB2	ROACH_TRANSCEIVERS_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-22-2008_13:23	DRAWN: F KAPP · APPR:
PATH PATH	CHECKED: E BAUERMEISTER · SHEET 10 OF 25

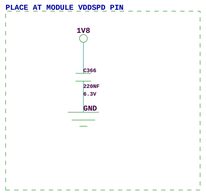


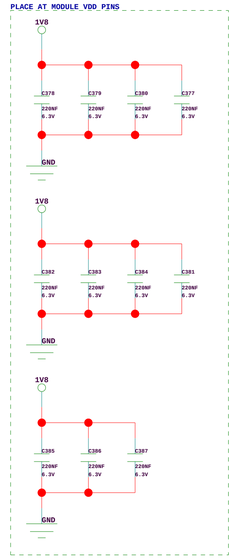


VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
PLACE ONE 10uF CAPACITOR ON EITHER END OF ISLAND

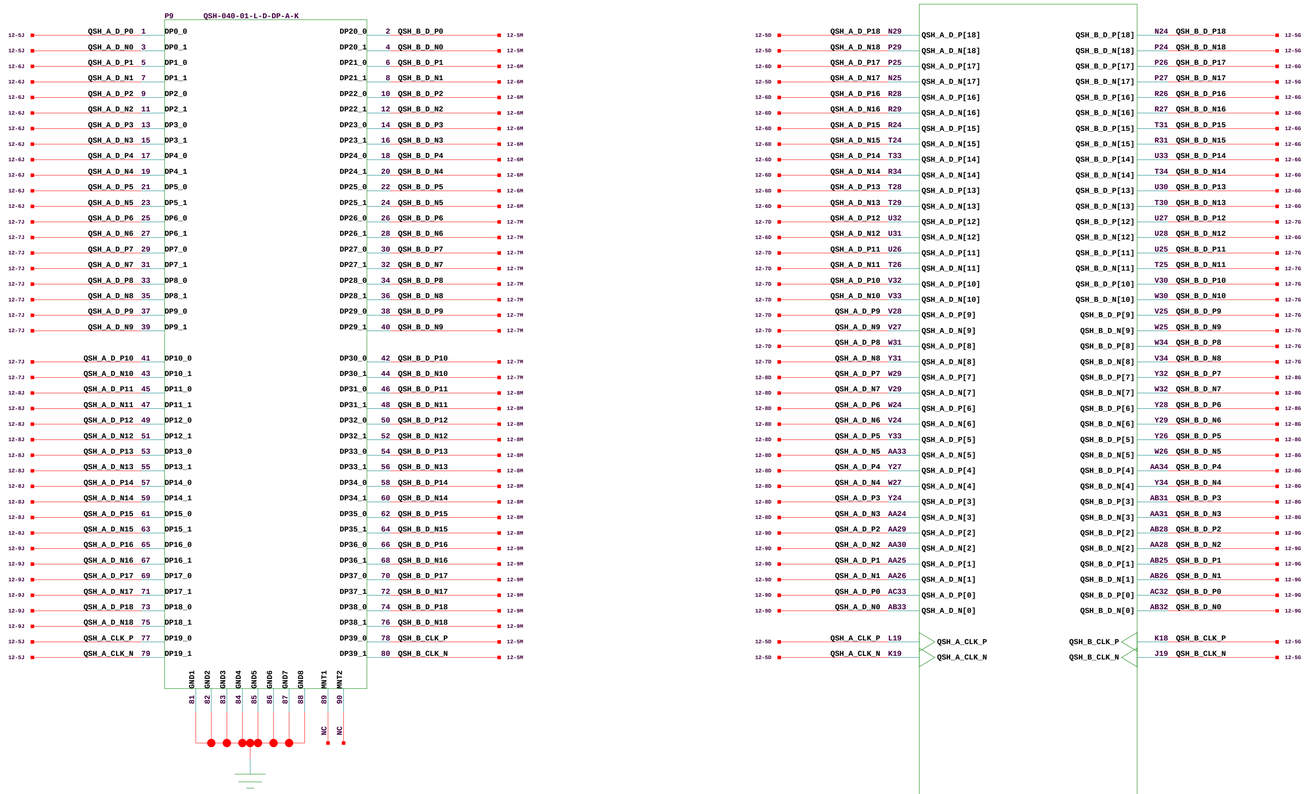








ROACH/iBOB2	ROACH_DDR2_DIMM
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE NW
2-22-2008_13:23	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 11 OF 25



ROACH/iBOB2

ROACH_DIFF_GPIO

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

2-22-2008_13:23

PATH PATH

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 12 OF 25

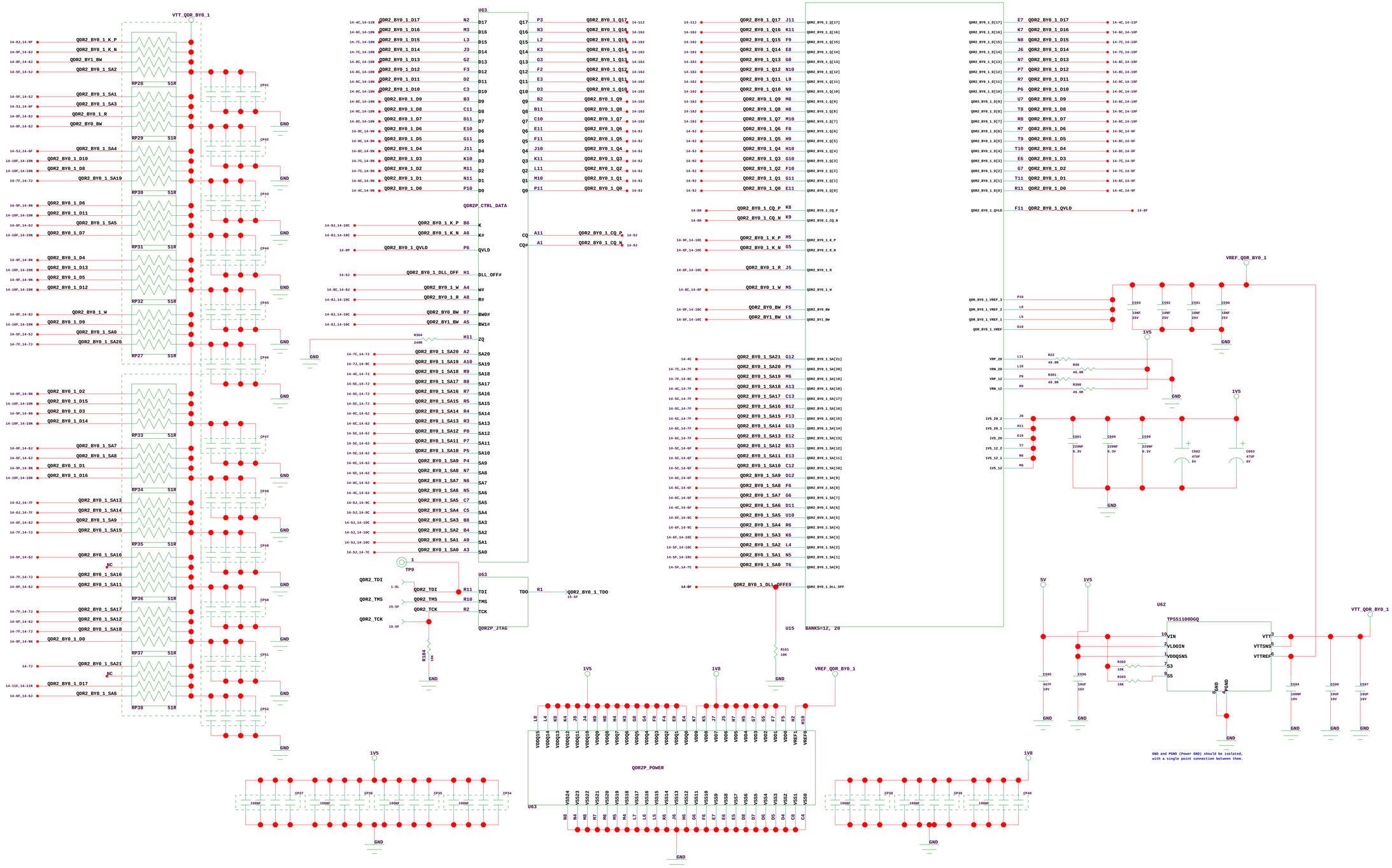
GPIOLVC18[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

GPIOLVC25[0] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

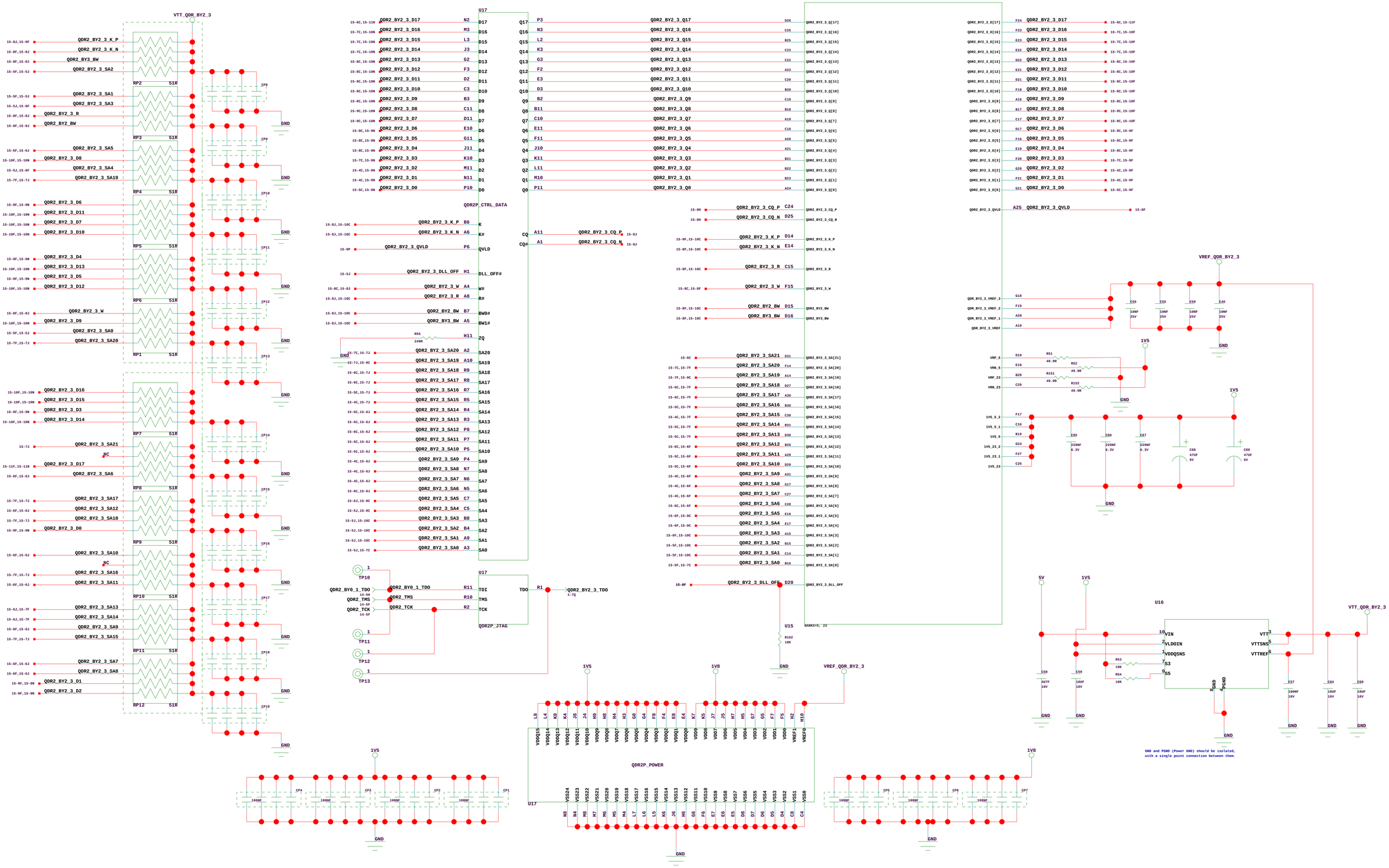
IO VOLTAGE LEVEL SELECT	
1-2: 3.3V	DEFAULT
2-3: 2.5V	

IF CR58 IS ON, CLOCK CAPABLE GPIO'S ARE OUTPUTS

ROACH/iBOB2	ROACH_GPIO_MISC
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
2-22-2008_13:23 PATH PATH	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MM
	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 13 OF 25



ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-22-2008_13:23 PATH PATH	DRAWN: F KAPP · APPR: · CHECKED: E BAUERMEISTER · SHEET 14 OF 25

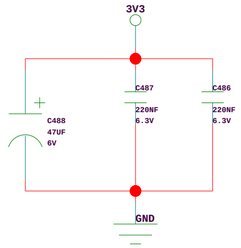


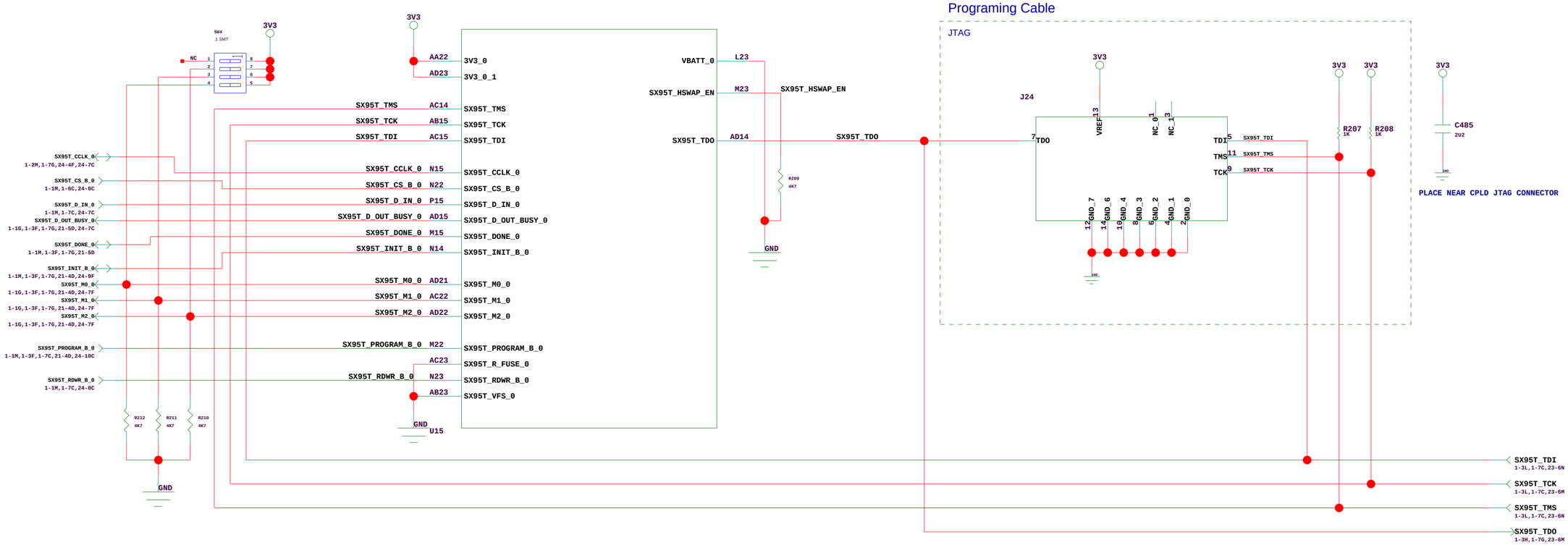
ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-22-2008_13:23 PATH PATH	DRAWN: F KAPP · APPR:
	CHECKED: E BAUERMEISTER · SHEET 15 OF 25

TBD

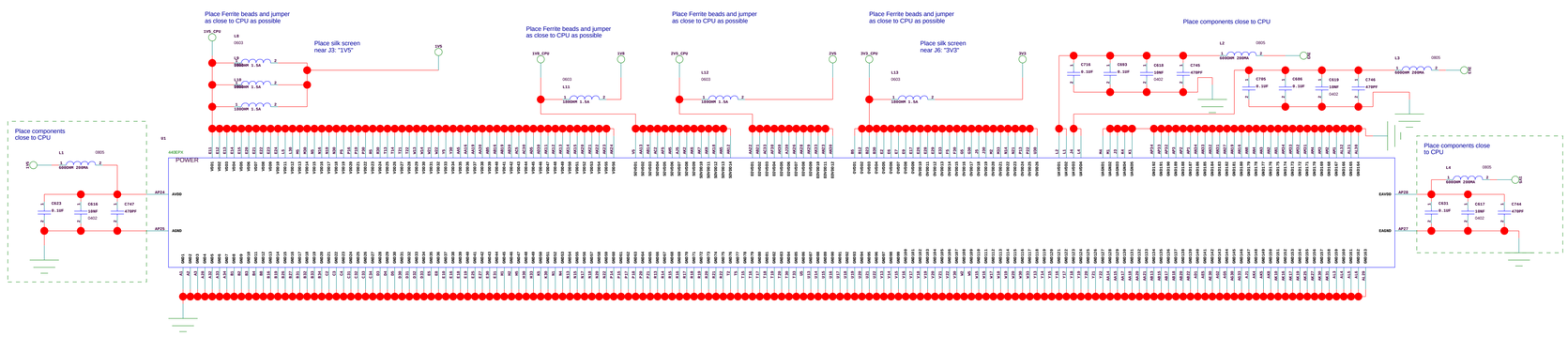
VALID CONFIGURATION MODES

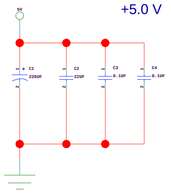
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

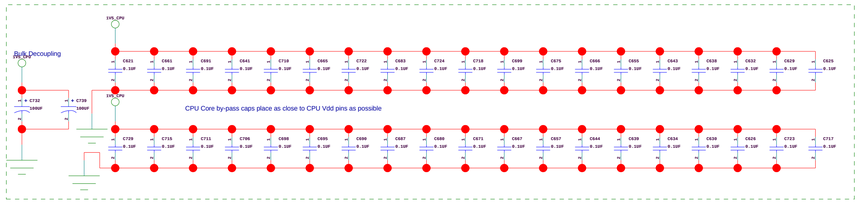


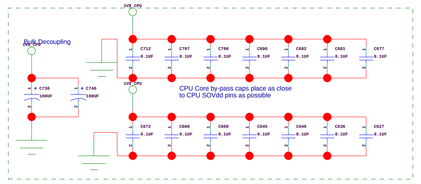


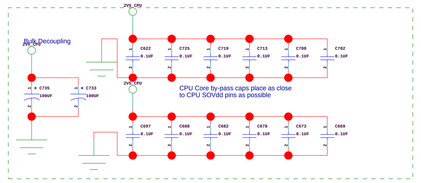
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
2-22-2008_13:23 PATH PATH	

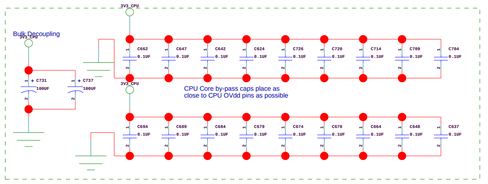


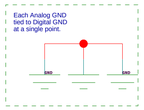










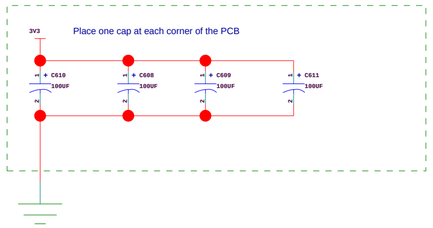


REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: **CASPER GROUP, UC BERKELEY** **NRAO, SOCORRO** **meerKAT, CAPE TOWN** http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 17 OF 25
2-22-2008_13:23 PATH PATH	

REMOVED 3V3 GENERATION



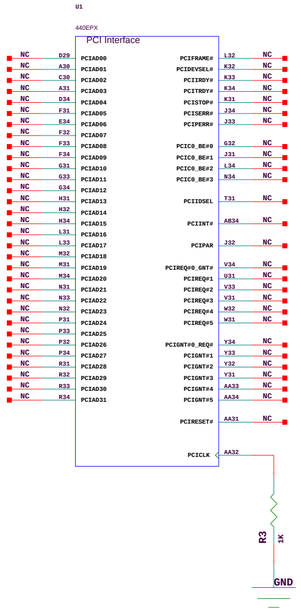
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET: 18 OF 25
2-22-2008_13:23 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-22-2008_13:23 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups. Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

Place nearest PHY pin 96

Place nearest PHY pin 101

Place nearest PHY pin 98

Place nearest PHY pin 100

Place as close to PHY CORE VDD power pins as possible

Place as close to PHY IO VDD power pins as possible

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible.

Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5

Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY

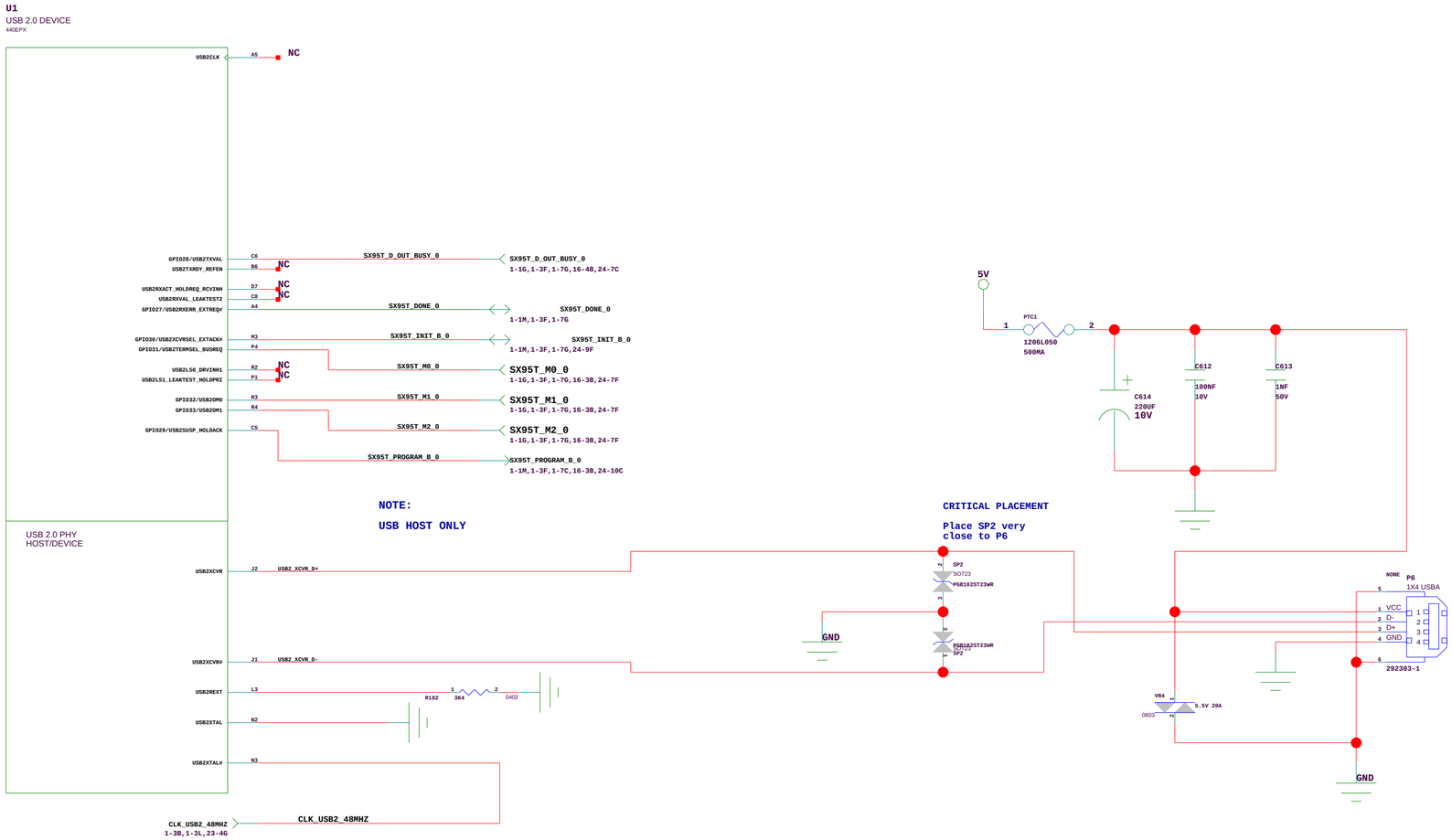
CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

Place jumpers in line with signals

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

UNUSED SECOND ETHERNET MAC

ROACH/iBOB2	ROACH_PPC_ETH1
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-22-2008_13:23	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 20 OF 25



ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25
2-22-2008_13:23 PATH PATH	

DDR_PA[15:0]

DDR_PD[63:0]

U1

DDR SDRAM

64DEPX

DDR_PD0	MEMDATA00	MEMADDR00	DDR_PA0
DDR_PD1	MEMDATA01	MEMADDR01	DDR_PA1
DDR_PD2	MEMDATA02	MEMADDR02	DDR_PA2
DDR_PD3	MEMDATA03	MEMADDR03	DDR_PA3
DDR_PD4	MEMDATA04	MEMADDR04	DDR_PA4
DDR_PD5	MEMDATA05	MEMADDR05	DDR_PA5
DDR_PD6	MEMDATA06	MEMADDR06	DDR_PA6
DDR_PD7	MEMDATA07	MEMADDR07	DDR_PA7
DDR_PD8	MEMDATA08	MEMADDR08	DDR_PA8
DDR_PD9	MEMDATA09	MEMADDR09	DDR_PA9
DDR_PD10	MEMDATA10	MEMADDR10	DDR_PA10
DDR_PD11	MEMDATA11	MEMADDR11	DDR_PA11
DDR_PD12	MEMDATA12	MEMADDR12	DDR_PA12
DDR_PD13	MEMDATA13	MEMADDR13	DDR_PA13
DDR_PD14	MEMDATA14		
DDR_PD15	MEMDATA15	BA0	DDR_PBA0
DDR_PD16	MEMDATA16	BA1	DDR_PBA1
DDR_PD17	MEMDATA17	BA2	DDR_PBA2
DDR_PD18	MEMDATA18		
DDR_PD19	MEMDATA19	RAS#	DDR_PRAS#
DDR_PD20	MEMDATA20	CAS#	DDR_PCAS#
DDR_PD21	MEMDATA21	WE#	DDR_PWE#
DDR_PD22	MEMDATA22		
DDR_PD23	MEMDATA23	DM0	DDR_PDM0
DDR_PD24	MEMDATA24	DM1	DDR_PDM1
DDR_PD25	MEMDATA25	DM2	DDR_PDM2
DDR_PD26	MEMDATA26	DM3	DDR_PDM3
DDR_PD27	MEMDATA27	DM4	DDR_PDM4
DDR_PD28	MEMDATA28	DM5	DDR_PDM5
DDR_PD29	MEMDATA29	DM6	DDR_PDM6
DDR_PD30	MEMDATA30	DM7	DDR_PDM7
DDR_PD31	MEMDATA31	DM8	DDR_PDM8
DDR_PD32	MEMDATA32		
DDR_PD33	MEMDATA33	DQS0	DDR_PDQS0
DDR_PD34	MEMDATA34	DQS1	DDR_PDQS1
DDR_PD35	MEMDATA35	DQS2	DDR_PDQS2
DDR_PD36	MEMDATA36	DQS3	DDR_PDQS3
DDR_PD37	MEMDATA37	DQS4	DDR_PDQS4
DDR_PD38	MEMDATA38	DQS5	DDR_PDQS5
DDR_PD39	MEMDATA39	DQS6	DDR_PDQS6
DDR_PD40	MEMDATA40	DQS7	DDR_PDQS7
DDR_PD41	MEMDATA41	DQS8	DDR_PDQS8
DDR_PD42	MEMDATA42		
DDR_PD43	MEMDATA43	MEMODT0	DDR_PODT0
DDR_PD44	MEMDATA44	MEMODT1	DDR_PODT1
DDR_PD45	MEMDATA45		
DDR_PD46	MEMDATA46	BANKSEL#0	DDR_PCS0#
DDR_PD47	MEMDATA47	BANKSEL#1	DDR_PCS1#
DDR_PD48	MEMDATA48		
DDR_PD49	MEMDATA49	MEMCLKEN	DDR_PCKE
DDR_PD50	MEMDATA50		
DDR_PD51	MEMDATA51	MEMCLKOUT	DDR_CLKOUT
DDR_PD52	MEMDATA52		
DDR_PD53	MEMDATA53	MEMCLKOUT#	DDR_CLKOUT#
DDR_PD54	MEMDATA54		
DDR_PD55	MEMDATA55		
DDR_PD56	MEMDATA56		
DDR_PD57	MEMDATA57		
DDR_PD58	MEMDATA58		
DDR_PD59	MEMDATA59		
DDR_PD60	MEMDATA60		
DDR_PD61	MEMDATA61		
DDR_PD62	MEMDATA62		
DDR_PD63	MEMDATA63		

ECC0	PPC_ECC0	22-9F
ECC1	PPC_ECC1	22-9F
ECC2	PPC_ECC2	22-9F
ECC3	PPC_ECC3	22-10F
ECC4	PPC_ECC4	22-10F
ECC5	PPC_ECC5	22-10F
ECC6	PPC_ECC6	22-10F
ECC7	PPC_ECC7	22-10F

SVREF1A, SVREF1B, SVREF2A, SVREF2B

DDR_VREF_0V9

5V

1V8

C158 0.10F

C148 0.10F

C151 0.10F 0402

C152 0.10F 0402

C149 100F 0402

Place parts as close to CPU as possible

DDR2 Clock line must be 500ps longer than Address/Command lines
To compensate for additional loading when using unbuffered DIMM's
See P84 of PPC440EPx for more information

J8

PPC_ECC7	22-6D	168	DDR2_DIMM_CB7
PPC_ECC6	22-6D	167	DDR2_DIMM_CB6
PPC_ECC5	22-7D	162	DDR2_DIMM_CB5
PPC_ECC4	22-7D	161	DDR2_DIMM_CB4
PPC_ECC3	22-7D	49	DDR2_DIMM_CB3
PPC_ECC2	22-7D	48	DDR2_DIMM_CB2
PPC_ECC1	22-7D	43	DDR2_DIMM_CB1
PPC_ECC0	22-7D	42	DDR2_DIMM_CB0
DDR_PDQ63		236	DDR2_DIMM_DQ[63]
DDR_PDQ62		235	DDR2_DIMM_DQ[62]
DDR_PDQ61		230	DDR2_DIMM_DQ[61]
DDR_PDQ60		229	DDR2_DIMM_DQ[60]
DDR_PDQ59		117	DDR2_DIMM_DQ[59]
DDR_PDQ58		116	DDR2_DIMM_DQ[58]
DDR_PDQ57		111	DDR2_DIMM_DQ[57]
DDR_PDQ56		110	DDR2_DIMM_DQ[56]
DDR_PDQ55		227	DDR2_DIMM_DQ[55]
DDR_PDQ54		226	DDR2_DIMM_DQ[54]
DDR_PDQ53		218	DDR2_DIMM_DQ[53]
DDR_PDQ52		217	DDR2_DIMM_DQ[52]
DDR_PDQ51		108	DDR2_DIMM_DQ[51]
DDR_PDQ50		107	DDR2_DIMM_DQ[50]
DDR_PDQ49		99	DDR2_DIMM_DQ[49]
DDR_PDQ48		98	DDR2_DIMM_DQ[48]
DDR_PDQ47		215	DDR2_DIMM_DQ[47]
DDR_PDQ46		214	DDR2_DIMM_DQ[46]
DDR_PDQ45		209	DDR2_DIMM_DQ[45]
DDR_PDQ44		208	DDR2_DIMM_DQ[44]
DDR_PDQ43		96	DDR2_DIMM_DQ[43]
DDR_PDQ42		95	DDR2_DIMM_DQ[42]
DDR_PDQ41		90	DDR2_DIMM_DQ[41]
DDR_PDQ40		89	DDR2_DIMM_DQ[40]
DDR_PDQ39		206	DDR2_DIMM_DQ[39]
DDR_PDQ38		205	DDR2_DIMM_DQ[38]
DDR_PDQ37		200	DDR2_DIMM_DQ[37]
DDR_PDQ36		199	DDR2_DIMM_DQ[36]
DDR_PDQ35		87	DDR2_DIMM_DQ[35]
DDR_PDQ34		86	DDR2_DIMM_DQ[34]
DDR_PDQ33		81	DDR2_DIMM_DQ[33]
DDR_PDQ32		80	DDR2_DIMM_DQ[32]
DDR_PDQ31		159	DDR2_DIMM_DQ[31]
DDR_PDQ30		158	DDR2_DIMM_DQ[30]
DDR_PDQ29		153	DDR2_DIMM_DQ[29]
DDR_PDQ28		152	DDR2_DIMM_DQ[28]
DDR_PDQ27		40	DDR2_DIMM_DQ[27]
DDR_PDQ26		39	DDR2_DIMM_DQ[26]
DDR_PDQ25		34	DDR2_DIMM_DQ[25]
DDR_PDQ24		33	DDR2_DIMM_DQ[24]
DDR_PDQ23		150	DDR2_DIMM_DQ[23]
DDR_PDQ22		149	DDR2_DIMM_DQ[22]
DDR_PDQ21		144	DDR2_DIMM_DQ[21]
DDR_PDQ20		143	DDR2_DIMM_DQ[20]
DDR_PDQ19		31	DDR2_DIMM_DQ[19]
DDR_PDQ18		30	DDR2_DIMM_DQ[18]
DDR_PDQ17		25	DDR2_DIMM_DQ[17]
DDR_PDQ16		24	DDR2_DIMM_DQ[16]
DDR_PDQ15		141	DDR2_DIMM_DQ[15]
DDR_PDQ14		140	DDR2_DIMM_DQ[14]
DDR_PDQ13		132	DDR2_DIMM_DQ[13]
DDR_PDQ12		131	DDR2_DIMM_DQ[12]
DDR_PDQ11		22	DDR2_DIMM_DQ[11]
DDR_PDQ10		21	DDR2_DIMM_DQ[10]
DDR_PDQ9		13	DDR2_DIMM_DQ[9]
DDR_PDQ8		12	DDR2_DIMM_DQ[8]
DDR_PDQ7		129	DDR2_DIMM_DQ[7]
DDR_PDQ6		128	DDR2_DIMM_DQ[6]
DDR_PDQ5		123	DDR2_DIMM_DQ[5]
DDR_PDQ4		122	DDR2_DIMM_DQ[4]
DDR_PDQ3		10	DDR2_DIMM_DQ[3]
DDR_PDQ2		9	DDR2_DIMM_DQ[2]
DDR_PDQ1		4	DDR2_DIMM_DQ[1]
DDR_PDQ0		3	DDR2_DIMM_DQ[0]
		101	DDR2_DIMM_SA2
		240	DDR2_DIMM_SA1
		239	DDR2_DIMM_SA0
		120	DDR2_DIMM_SCL
		119	DDR2_DIMM_SDA

879160001

1V8

R228 4K7

R227 4K7

PPC_DDR2_DIMM_SCL

PPC_DDR2_DIMM_SDA

GND

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA1	22-9D,22-10L
DDR2_DIMM_BA[1]	190	DDR_PBA2	22-9L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-7L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	NC	
DDR2_DIMM_CK_N[2]	221	NC	
DDR2_DIMM_CK_P[1]	137	NC	
DDR2_DIMM_CK_N[1]	138	NC	
DDR2_DIMM_CK_P[0]	185	DDR_CLKOUT	
DDR2_DIMM_CK_N[0]	186	DDR_CLKOUT#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-8D,22-11L
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-8D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D
PAR_OUT	55	PPC_DDR2_ERROR	1
PAR_IN	68	PAR_IN	TP4
			1
			TP5

R226 4K7

PPC_DDR2_RESET_N

1-2B,1-2M,24-10F

C455 5PF 50V

GND

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

DDR_VTT

22-6K,22-8D	DDR_PCKE	RP24
	DDR_PA15	
	DDR_PA14	
22-8K,22-9D	DDR_PBA1	
	DDR_PA12	RP23
	DDR_PA11	
	DDR_PA9	
	NC	
	DDR_PA7	RP22
	DDR_PA8	
	DDR_PA6	
	DDR_PA5	
	DDR_PA4	RP21
	DDR_PA3	
	DDR_PA1	
	DDR_PA2	
22-8K,22-9D	DDR_PA0	RP25
	DDR_PBA2	
22-8K,22-9D	DDR_PA10	
	DDR_PBA0	
22-7K,22-9D	DDR_PRAS#	RP26
22-3K,22-9D	DDR_PWE#	
22-3K,22-9D	DDR_PCS0#	
22-8K,22-9D	DDR_PCAS#	
22-3K,22-9D	DDR_PCS1#	RP19
22-9D	DDR_PODT0	
	DDR_PA13	
22-8D	DDR_PODT1	

CP26, CP28, CP29, CP30, CP32, CP31, CP33

GND

J8

VSS_64	237	69	VDD_1
VSS_63	234	67	VDD_2
VSS_62	231	64	VDD_3
VSS_61	228	62	VDD_4
VSS_60	225	59	VDD_5
VSS_59	222	56	VDD_6
VSS_58	219	53	VDD_7
VSS_57	216	51	VDD_8
VSS_56	213		VDD_9
VSS_55	210		VDD_10
VSS_54	207		VDD_11
VSS_53	204		
VSS_52	201		
VSS_51	198		
VSS_50	169		
VSS_49	166		
VSS_48	163		
VSS_47	160		
VSS_46	157		
VSS_45	154		
VSS_44	151		
VSS_43	148		
VSS_42	145		
VSS_41	142		
VSS_40	139		
VSS_39	136		
VSS_38	133		
VSS_37	130		
VSS_36	127		
VSS_35	124		
VSS_34	121		
VSS_33	118		
VSS_32	115		
VSS_31	112		
VSS_30	109		
VSS_29	106		
VSS_28	103		
VSS_27	100		
VSS_26	97		
VSS_25	94		
VSS_24	91		
VSS_23	88		
VSS_22	85		
VSS_21	82		
VSS_20	79		
VSS_19	66		
VSS_18	65		
VSS_17	50		
VSS_16	47		
VSS_15	44		
VSS_14	41		
VSS_13	38		
VSS_12	35		
VSS_11	32		
VSS_10	29		
VSS_9	26		
VSS_8	23		
VSS_7	20		
VSS_6	17		
VSS_5	14		
VSS_4	11		
VSS_3	8		
VSS_2	5		
VSS_1	2		

879160001

DDR_VREF_0V9

VREF 1

1V8

VDDSPD 238

1V8

VDD_11 197
VDD_10 189
VDD_9 187
VDD_8 184
VDD_7 178
VDD_6 172
VDD_5 69
VDD_4 67
VDD_3 64
VDD_2 59
VDD_1 53

1V8

VDDQ_11 194
VDDQ_10 191
VDDQ_9 181
VDDQ_8 175
VDDQ_7 170
VDDQ_6 78
VDDQ_5 75
VDDQ_4 72
VDDQ_3 62
VDDQ_2 56
VDDQ_1 51

GND

5V

1V8

U32

TPS51100DGQ

10	VIN	VTT	3
2	VLDOIN	VTTSNS	5
1	VDDQSNS	VTTREF	6
7	S3		
9	S5		
8	GND	PGND	4

R230 10K

R229 10K

R6 120R

C459 4U7F 10V

C456 10UF 16V

C453 100NF 10V

C21 22PF

C457 10UF 16V

C458 10UF 16V

DDR_VREF_0V9

DDR_VTT

GND

DDR_VREF_0V9

1V8

1V8

1V8

C432 100NF 10V
C433 10NF 25V
C454 100NF 10V
C434 10NF 25V
C430 100NF 10V
C443 10NF 25V
C431 100NF 10V
C444 10NF 25V
C436 100NF 10V
C445 10NF 25V
C435 100NF 10V
C446 10NF 25V

GND

1V8

1V8

1V8

C438 100NF 10V
C451 10NF 25V
C437 100NF 10V
C452 10NF 25V
C439 100NF 10V
C449 10NF 25V
C440 100NF 10V
C450 10NF 25V
C441 100NF 10V
C448 10NF 25V
C442 100NF 10V
C447 10NF 25V

GND

PLACE NEAREST DDR2 MODULE PINS

ROACH/iBOB2

ROACH_PPC_DDR2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

2-22-2008_13:23

PATH PATH

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 22 OF 25

PWR_GOOD
1-2G,1-3H,24-8R

3V3

PWR_GOOD monitors the +1.0v, 1V5, 1V8, 2V5, and 3V3 supplies

U31
SOT-23-5
MIC2779A-29

RESET_POR#
1-2M,1-3H,24-7F

RESET_POR#
6,11
1-2G,1-3L,1-5G,24-7F,25-5G

GND

SPST
SW1

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_3V3_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz

U9
SOIC-8
CY2291SFX_0211

SEL_SYSCLK
1-1M,1-3H,24-10F

CLK_UART_11_0592MHZ
1-1L,1-5G,25-2D

CLK_SYS_33MHZ

CLK_CPLD_33MHZ
1-1G,1-2L,24-10F

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible

U24
CY2292FZX_0211

CLK_SEL_M66EN
1-1M,1-3H,24-10F

CLK_GETH0_25MHZ
1-3L,1-4B,28-4E

CLK_USB2_48MHZ
1-3B,1-3L,21-2D

CLK_CPLD_50MHZ
1-1G,1-3L,24-10F

IRQ0-9 have programmable polarity per section 10.5.7 (UIC0_PPC 440ep user manual

U1
440EPX
SYSTEM
INTERRUPTS
PPC440EPX-NTA533T

CLK_TMRCLK
1-1M,1-3H,24-10C

SYSERR
1-1G,1-3L,24-10C

PPC_THERMONA
1-3L,1-9E,2-4L

PPC_THERMONB
1-3L,1-9E,2-4L

TEST POINT

NO POP
RO1 - RO5

MONITOR_INT
1-3H,1-9E,2-1P

VS_INT#
1-3H,1-5L,25-8Q

STTM_ALERT
1-3H,1-5L,25-2B

GPIO44
1-3L

SX95T_TDI
1-3L,1-7C,16-2L

SX95T_TCK
1-3L,1-7C,16-2L

SX95T_TMS
1-3L,1-7C,16-2L

SX95T_TDO
1-3H,1-7G,16-2L

GETH0_INT#
1-3H,1-4E,28-4E

TRACE & JTAG CONNECTORS

P1
2x8
.12K H SMT

CPU_TDO
CPU_TDI
CPU_TCK
CPU_TMS
CPU_HALT#

23-2G,23-2H

DEBUG_TRST#

VCC_JTAG

R26 is for current limiting and should be <100 Ohms.

Critical placement and routing of the Trace connector and nets. Up to CPU frequency/4

TRACE PORT

J1
25PA F SMT

RiscWatch
JTAG

CPU_TRST#
1-2M,1-3H,24-9C

DEBUG_TRST#
1-1G,1-3L,24-9C

TMC_CLK
23-2E

VCC_JTAG

ROACH/iBOB2	ROACH_PPC_TST_CLK_IO
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
2-22-2008_13:23; PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 23 OF 25

roach_cpld_XC2C256_7VQ100C_pcb

NC	4	PAD4	
NC	7	PAD8	
CLK_TMSCLK	9	PAD10	1-1M,1-3H,23-6H
SYSRMR	10	PAD12	1-1G,1-3L,23-6H
EXT_RESET#	11	PAD15	1-2G,1-4L,25-6F
SX95T_PROGRAM_B_0	12	PAD16	1-1M,1-3F,1-7C,16-3B,21-4D
SX95T_DONE_0	13	PAD17	1-1M,1-3F,1-7G,21-5D
PCS_2	14	PAD18	1-1G,1-4L,25-7B
PB_WE	15	PAD19	1-1G,1-4L,25-5G,25-6M,25-7B,25-9B
DEBUG_TRST#	16	PAD20	1-1G,1-3L,23-1F
CPU_TRST#	17	PAD21	1-2M,1-3H,23-2F
PWRE_0#	18	PAD23	1-2G,1-4L,25-6M,25-7B,25-9B
PADO[27:31]	19	PADO27	1-2G,1-4L,25-10B
	20	PADO28	
	21	PADO29	
	22	PADO30	
	23	PADO31	
PDATA[0:7]	24	PDATA0	1-2M,1-4L
	25	PDATA1	
	26	PDATA2	
	28	PDATA3	
	30	PDATA4	
	31	PDATA7	
	32	PDATA6	
	33	PDATA5	
POE#	34	PAD54	1-1G,1-5L,25-5G,25-7M,25-10B
SX95T_RDWR_B_0	35	PAD55	1-1M,1-7C,16-3B
SX95T_D_IN_0	38	PAD59	1-1M,1-7C,16-4B
SX95T_D_OUT_BUSY_0	40	PAD64	1-1G,1-3F,1-7G,16-4B,21-5D
PER_CCLK_ENF	41	PAD65	
CLK_PERCLK	42	PAD66	1-1G,1-4L,24-6C,25-6F
SX95T_CCLK_0	43	PAD67	1-2M,1-7G,24-4F
FRY_BY#	44	PAD68	
FWP#	45	PAD69	1-1G,1-4L,25-7J
EE1_WP#	46	PAD70	1-1M,1-4G,25-8J
EE2_BOOT_WP#	48	PAD73	1-2M,1-5G,25-3A
STTM_AS#	49	PAD74	1-2M,1-4G,25-5A
SELECTMAP_CS	50	PAD75	1-2M,1-5G,25-1B
	51	PAD76	1-2G,1-5L,25-7B
SX95T_CS_B_0	52	PAD77	1-1M,1-6C,16-4B
	53	PAD81	
PPC_RESET	54	PAD82	1-2G,1-9E,2-2R
SYS_CONFIG[0:7]	56	PAD86	SYS_CONFIG0
	57	PAD87	SYS_CONFIG1
	58	PAD88	SYS_CONFIG2
	59	PAD89	SYS_CONFIG3
	60	PAD90	SYS_CONFIG4
	61	PAD95	SYS_CONFIG5
	64	PAD100	SYS_CONFIG6
	66	PAD102	SYS_CONFIG7
	68	PAD105	
	69	PAD107	
	70	PAD108	
RESET_CPLD#	71	PAD109	1-1M,1-4G,25-3J
	74	PAD112	
	75	PAD113	
	76	PAD114	
	77	PAD115	
	78	PAD117	
	79	PAD118	
	80	PAD119	
	83	PAD125	
	85	PAD131	
	86	PAD132	
	87	PAD133	
	88	PAD134	
	91	PAD137	
	92	PAD138	
	94	PAD142	
	95	PAD143	
	96	PAD144	
	97	PAD145	
	98	PAD146	
	100	PAD152	
	101	PAD154	
	102	PAD156	
	103	PAD158	
	104	PAD160	
	105	PAD161	
	106	PAD162	
	107	PAD163	
	110	PAD167	
	111	PAD168	
	112	PAD169	
	113	PAD171	
	114	PAD173	
	115	PAD175	
	116	PAD176	
	117	PAD177	
	118	PAD178	
	119	PAD186	
	120	PAD187	
	121	PAD190	
	124	PAD191	
	125	PAD192	
	126	PAD194	
	128	PAD195	
	129	PAD196	
	130	PAD197	
SX95T_INIT_B_0	131	PAD199	1-1M,1-3F,1-7G,21-4D
	132	PAD204	
	133	PAD206	
	134	PAD207	
	135	PAD208	
	136	PAD211	
	137	PAD212	
	138	PAD213	
	139	PAD214	
	140	PAD217	
	142		

U54 XC2C256_7VQ144C

CLK_CPLD_50MHZ — 1-1G,1-3L,23-4G
CLK_CPLD_33MHZ — 1-1G,1-2L,23-4G
GETH0_RST# — 1-2M,1-4B,25-4E
PPC_DDR2_RESET_N — 1-1B,1-2M,22-5K
CLK_SEL_MGGEN — 1-1M,1-3H,23-5D
SEL_SYSCLK — 1-1M,1-3H,23-7G

BOOT_CFG0 — 1-1M,1-4G,25-1J
BOOT_CFG1 — 1-1M,1-4G,25-1J
BOOT_CFG2 — 1-1M,1-4G,25-1J

3V3 — R016 10K — Q402
3V3 — R011 10K — Q402
3V3 — R014 10K — Q402

SD/MMC/MMCPLUS CONNECTOR

J17 — SDSR13-A0-0005

10	CMD/DI	DAT0/DO	2
6	CLK/SCLK	DAT1	1
		DAT2	13
7	VDD	DAT3	12
8	VSS1	DAT4	11
4	VSS2	DAT5	9
		DAT6	5
14	SD_CD_COM	DAT7	3
15	SD_WP_COM		
		MNT1	16
		MNT2	17

3V3 — C615 0.1UF — Q402

PWR_GOOD — 1-2G,1-3H,23-10G

RESETS

CPU_TRST# = '1' when JTAG_TRST# = '1' and RESET_PORR = '1' else '0'; see errata sheet

Boot Configuration

SysErr will be used to drive Status LED (active H)

USER_LED1 — R201 1500 — Q402 — CR3 — CR5
SYSERR# — R202 1500 — Q402 — CR4 GRN — CR6 — GRN
RESET_RUFPOR# — R203 1500 — Q402 — RED

R198 10K — Q402
R194 10K — Q402
R195 10K — Q402
R196 10K — Q402
SW2 — APOLE — User DIP-Switch

USER_DIP0
USER_DIP1
USER_DIP2
USER_DIP3

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

R204 10K — Q402
R205 10K — Q402
R206 10K — Q402
SW3 — APOLE — Configuration DIP-Swith

1-1G,1-5G,25-3N

CFG_DIP0
CFG_DIP1
CFG_DIP2
MGGEN

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

roach_cpld_XC2C256_7VQ100C_configpins

U54 XC2C256_7VQ144C

NC	2	PAD1
NC	3	PAD3
NC	5	PAD5
NC	6	PAD7
NC	39	PAD62
	63	TDI
	65	TMS
	67	TCK
	122	TDO
NC	143	PAD218

Xilinx Programing Cable

JTAG — J22

3V3 — VREF 13 — NC_0 8 — NC_1 14
TDO 7 — TDI 9 — TMS 11 — TCK 10
GND_7 12 — GND_6 10 — GND_4 8 — GND_3 6 — GND_2 4 — GND_1 2 — GND_0
R193 1K — R192 1K

3V3 — C484 20Z — PLACE NEAR CPLD JTAG CONNECTOR

ENABLE PER_CLK CONNECTION TO CONFIGURATION I/F MUST CO-ORDINATE WITH SX95T_CCLK_0 AND MODE TO AVOID CLASH

R135 10K — 3V3
R305 330R — R306 240R — PLACE AT END OF DAISY CHAIN

CLK_PERCLK — 1-1G,1-4L,24-7C,25-6F

SN74AHC1G125DCKT — U2
PER_CCLK_ENF — 1 OE# — VCC 5 — 3V3
CLK_PERCLK — 2 A — Y 4 — SX95T_CCLK_0
GND 3
C13 100NF 10V

SX95T_CCLK_0 — 1-2M,1-7G,24-7C

roach_cpld_XC2C256_7VQ100C_powerpins

U54 XC2C256_7VQ144C

VCC 1 — VAUX 8 — VCCIO_3 27 — VCC_1 37 — VCCIO_4 55 — VCCIO_5 73 — VCC_2 84 — VCCIO_6 93 — VCCIO 109 — VCCIO_1 127 — VCCIO_2 141

GND_3 29 — GND_4 36 — GND_5 47 — GND_6 62 — GND_7 72 — GND_8 89 — GND_9 90 — GND_10 99 — GND 108 — GND_1 123 — GND_2 144

PLACE NEAR CPLD POWER PINS

C473 C474 C475 C476 C477 C478 C479 C480 C481 C482 C483 — 100NF 10V — 3V3

ROACH/iBOB2	ROACH_PPC_CPLD
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-22-2008_13:23; PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 24 OF 25

PDATA[0:31]
1-2M,1-4L

PADD[20:31]
1-2G,1-4L,24-9B,25-10B

PADD[2:31]

PADD30 IS THE LSB FOR 16 BIT WIDE BUS TRANSFERS

**NOTE:
DMA SIGNALS
IN GREEN TEXT**

PADD2 IS THE MSB

3V3

PCS_3_GPIO910 — 25-7C
PDE# — 1-1G,1-5L,24-8C,25-5G,25-7B,25-7M
PR_W# — 1-1G,1-4L,24-9C,25-5G,25-6M,25-7B
PWBE_0# — 1-2G,1-4L,24-9C,25-6M,25-7B
PWBE_1# — 25-6M,25-7C
PWBE_2# — 25-7C
PWBE_3# — 25-7C
PREADY — 25-7C,25-8Q
PBLAST# — 25-6M,25-7C
PCS_0 — 1-1G,1-4L,24-9C
PCS_1 — 1-1G,1-5L,24-6C
SELECTMAP_CS — 1-2G,1-5L,24-6C
PCS_2 — 1-1G,1-4L,24-9C
SELECTMAP_CS — 25-10B
PCS_3_GPIO910 — 25-10B
PDE# — 1-1G,1-5L,24-8C,25-5G,25-7M,25-10B
PR_W# — 1-1G,1-4L,24-9C,25-5G,25-6M,25-9B
PWBE_0# — 1-2G,1-4L,24-9C,25-6M,25-9B
PWBE_1# — 25-6M,25-9B
PWBE_2# — 25-9B
PWBE_3# — 25-9B
PREADY — 25-9B
PBLAST# — 25-6M,25-9B

M66EN — 1-1G,1-5G,24-5H

EE1_WP — 1-2M,1-5G,24-7C
EE2_BOOT_WP — 1-2M,1-4G,24-7C

STTM_ALERT — 1-3M,1-5L,23-6M
STTM_AS — 1-2M,1-5G,24-7C

SCPCLK — 1-5L
SCPDI — 1-5L
SCPDO — 1-5L

I2C0_SCLK — 1-5L,1-9B,2-2P
I2C0_33_DATA — 1-5L,1-8E

I2C0_SCLK
I2C0_33_DATA
I2C0_66_DATA
I2C0_SDATA

ATMEL AT24C04N-10SU-1.8 (U42, U43, U44)

NO POP

BUF_TA-6 PI5A3157 — SHD BD TO A

U1 — AXEXPX

External Slave Peripheral

PERDATA[31:0]
PERADDR[31:2]
PERADDR[0]
PERCS0#
PERCS1#_GPIO06
PERCS2#
PERCS3#_GPIO09
PERCS4#_GPIO10
PERDE#
PERR_W#
PERBE0#
PERBE1#
PERBE2#
PERBE3#
PERREADY
PERBLAST#

PERADDR67_GPIO66_DMAREQ2
PERADDR66_GPIO61_DMAACK2
PERADDR65_GPIO62_EOT2_TC2
GPIO63_PERADDR64_DMAREQ3
GPIO64_PERADDR63_DMAACK3
GPIO65_PERADDR62_EOT3_TC3

DMAREQ2
DMAACK2
EOT2/TC2
DMAREQ3
DMAACK3
EOT3/TC3

EXTRESET2
PERCLK
PERERR_GPIO11

R6 0R — CLK_PERCLK

R134 3K3 — R133 3K3 — R132 3K3 — R84 3K3 — R83 3K3 — R5 3K3 — 3V3

R85 1K

EXT_RESET#
EPB RESET OUTPUT
1-2G,1-4L,24-10C

CLK_PERCLK
1-1G,1-4L,24-4C,24-7C

External Master Peripheral Interface

U42 FBGA64 32Mx16 MIRROR BIT — FLASH 32Mx16 rMAM

PADD30 … PADD2 — A0 … A25
PADD30 … PADD16 — DQ0 … DQ15
WP#/ACC
BY/RY#
PCS_0
RESET#

RY_BY# — 1-1G,1-4L,24-7C
PWP# — 1-1M,1-4G,24-7C

R84 3K3 — R81 3K3 — R80 3K3 — 3V3

JP3
C654 0.1UF — C656 0.1UF — C659 0.1UF

PADD30 … PADD16 — PERDATA31 … PERDATA15

PERDATA[15:0] — PDATA15 … PDATA0

PERR_W# — 1-1G,1-5L,24-8C,25-7B,25-10B
PDE# — 1-1G,1-5L,24-8C,25-5G,25-7B,25-10B
PWBE_1# — 25-7C,25-9B
PWBE_0# — 1-2G,1-4L,24-9C,25-7B,25-9B
PBLAST# — 25-7C,25-9B

U15 — BANKS=1, 2, 4
CHIP SELECT 1

PADD30 … PADD2 — PER_A[30] … PER_A[2]
PCS_1 — PER_CS0
POE# — PER_OE_N
PR_W# — PER_R_W_N
PWBE_1# — PER_WBE[1]
PWBE_0# — PER_WBE[0]
PBLAST# — PER_B_LAST

PERDATA[31:16] — PER_D[15] … PER_D[0]
PER_D_PAR[1] — NC
PER_D_PAR[0] — NC
PER_INT — G23 — VS_INT#
PER_READY — K12 — PREADY
PER_CLK — H12 — CLK_PERCLK

VS_INT# — 1-3M,1-5L,23-7N

3V3_4_1 — AL12
3V3_4 — AG14
3V3_3 — AM19
3V3_2 — AM21
3V3_1_1 — G14
3V3_1 — D13

C334 470F 6V — C335 470F 6V — C330 220NF 6.3V — C331 220NF 6.3V — C332 220NF 6.3V — C333 220NF 6.3V

GND

UART1_TX — 1-3M,1-5G,23-7G
UART1_RX — 1-3M,1-5G,23-7G
PERPARB_UART1_RTS#
PERPARB_UART1_CTS#
CLK_UART_11_0592MHZ — 1-3L,1-5G,23-7G

U1 — UART
UARTSERCLK
UART1_TX_UART0_TX
UART1_RX_UART0_RX
UART1_RTS#_UART0_RTS#
UART1_CTS#_UART0_CTS#
UART2_TX_UART0_DTR#
UART2_RX_UART0_RI#
UART2_RTS#_UART0_DSR#
UART2_CTS#_UART0_DCD#

U48 TDFN_ZA-6 PI5A3157 — SHD BD TO A — UART1_CTS#
U45 TDFN_ZA-6 PI5A3157 — SHD BD TO A — UART2_RTS#
U46 TDFN_ZA-6 PI5A3157 — SHD BD TO A — UART2_CTS#

R82 3K3 — R81 3K3 — R80 3K3

C652 0.1UF — C649 0.1UF

RESET_CPLD# — 1-1M,1-4G,24-5C

BOOT_CFG2 — 1-1M,1-4G,24-10M
BOOT_CFG1 — 1-1M,1-4G,24-11M
BOOT_CFG0 — 1-1M,1-4G,24-11M

U44 SSOP20 ICL3225ECA — C192 0.1UF — C194 0.1UF — C193 0.1UF — C195 0.1UF
U43 SSOP20 ICL3225ECA — C196 0.1UF — C198 0.1UF — C197 0.1UF — C199 0.1UF

X_UART1_TX — 1-3M,1-5L,23-7N
X_UART1_RX — 1-3M,1-5L,23-7N
X_UART1_RTS# — 1-3M,1-5L,23-7N
X_UART1_CTS# — 1-3M,1-5L,23-7N
X_UART2_TX — 1-3M,1-5L,23-7N
X_UART2_RX — 1-3M,1-5L,23-7N
X_UART2_RTS# — 1-3M,1-5L,23-7N
X_UART2_CTS# — 1-3M,1-5L,23-7N

R86 10K — R87 10K

P2 — DSUB9FEMALE 180 HOLE — SF RSUB MALE — UART Port 0

J14 — UART Port 1 — HLE-105-02-G-DV

NC — X_UART2_RX — X_UART2_TX — NC — X_UART2_RTS# — NC — NC

IIC0_SCLK — 1-5L,1-9B,2-2P
IIC0_33_DATA — 1-5L,1-8E

IIC0 — IIC0SCLK, IIC0SDATA
IIC1_SPI — SCPCLKOUT_IIC1SCLK, SCPDI_IIC1SDATA, SCPDO
NAND Flash Interface — NOT USED

NFALE, NFCLE, NFREN#, NFWEN# — NC NC NC NC
NFRDYBUSY#
NFCE3#_PERCS3#

R77 3K3 — R78 3K3 — R76 3K3 — R75 3K3 — R74 3K3 — R73 3K3

SCPCLK — SCPDI — SCPDO

RN5 4.7K 8 SMT — RN6 4.7K 8 SMT

U41 SOT23-6 AD7414-R — STTM_ALERT — I2C0_SCLK — I2C0_SDATA

C651 0.1UF

**ROUTE AS DAISY CHAIN - U1 - U15 - U54 - TERMINATION
KEEP STUBS AS SHORT AS POSSIBLE**

1-1G,1-5L,24-8C,25-7B,25-7M,25-10B — PDE#
1-1G,1-4L,24-9C,25-6M,25-7B,25-9B — PR_W#
RESET_PORB# — 1-2G,1-3L,1-5G,23-8J,24-7F

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

2-22-2008_13:23

PATH PATH

ROACH_PPC_NVM_SERIAL

DOC NO: NRF-ADM-XXX-SD-0001
REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET: 25 OF 25