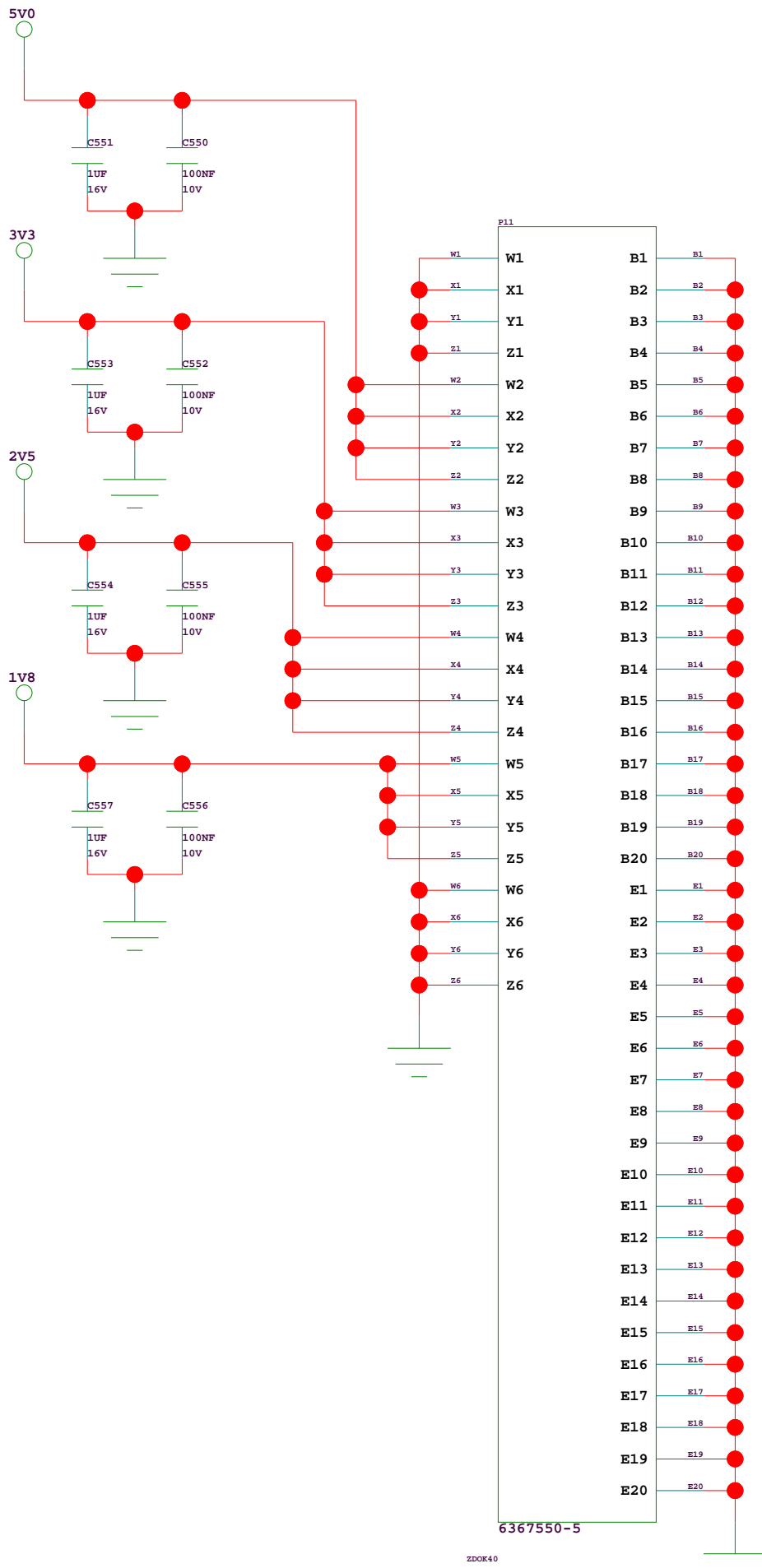
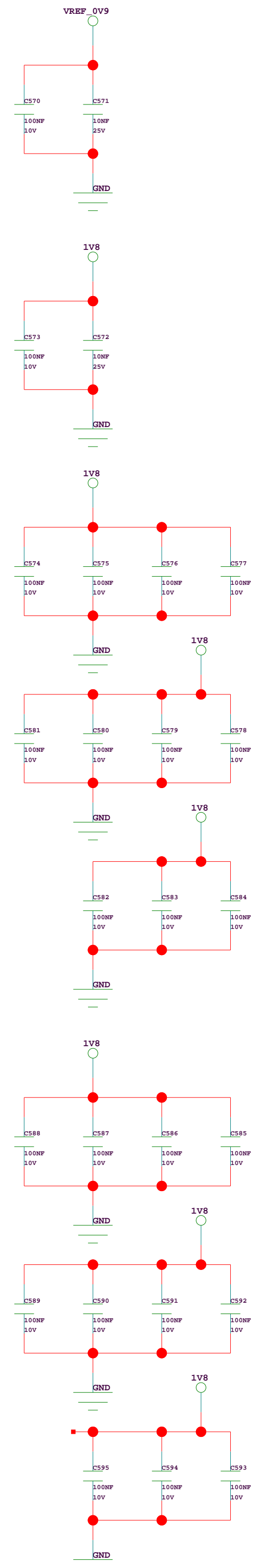
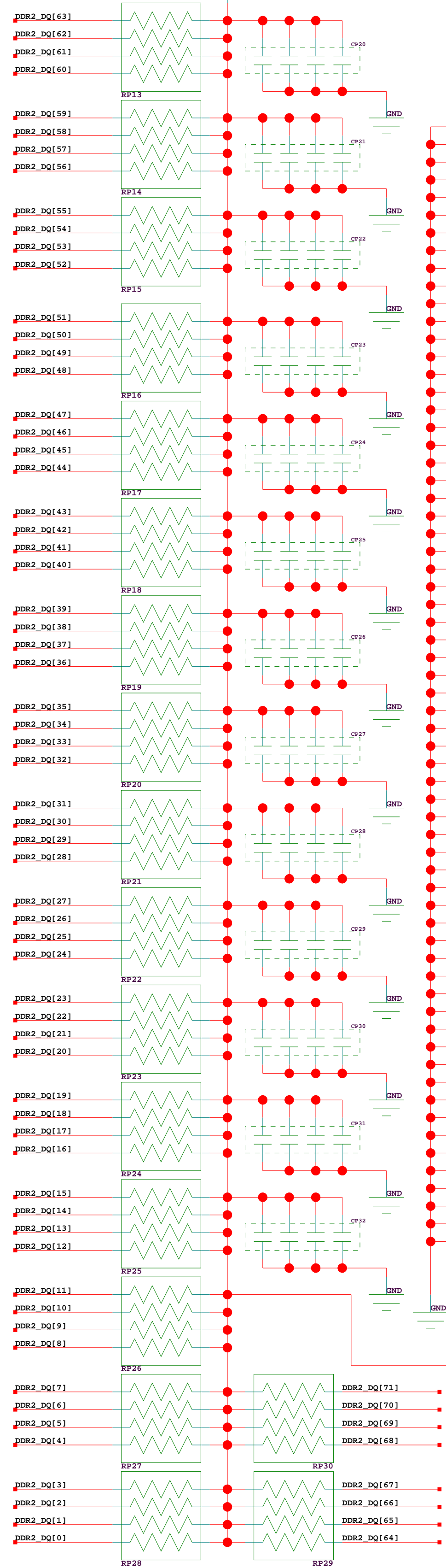
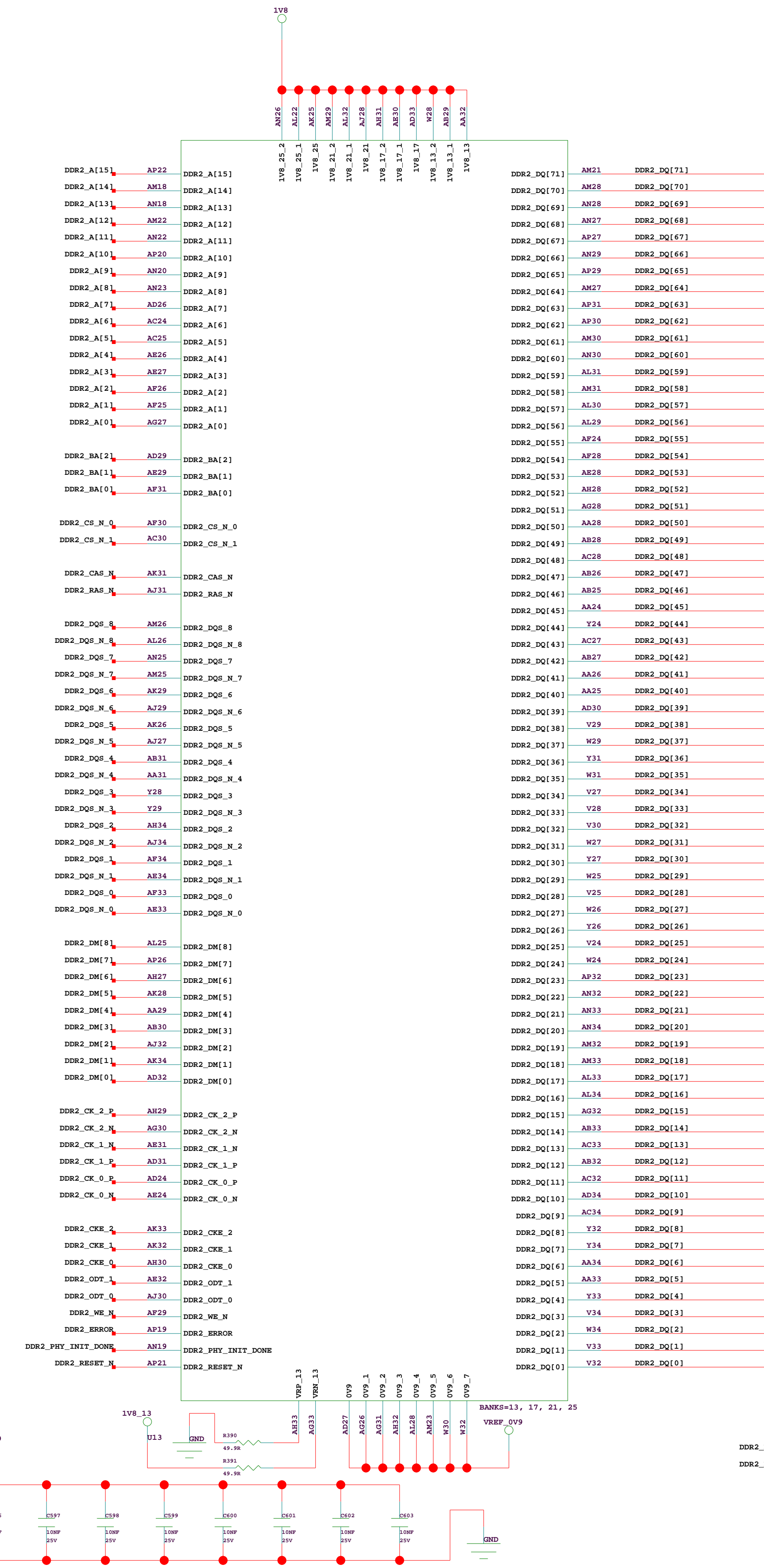


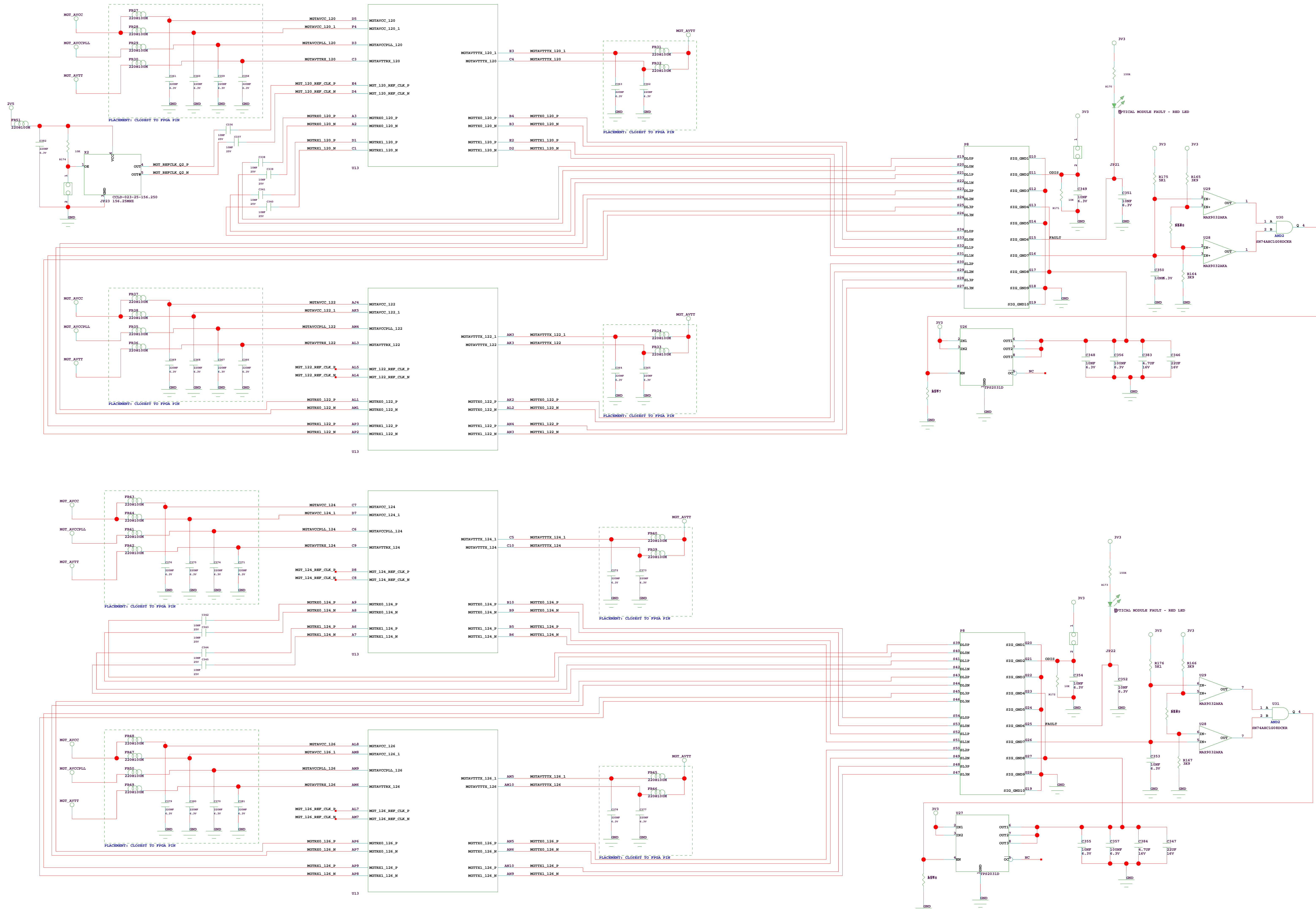
ZDOK1_DP_P[37]	AG10	ZDOK1_DP_P[37]
ZDOK1_DP_N[37]	AG11	ZDOK1_DP_N[37]
ZDOK1_DP_P[36]	AG8	ZDOK1_DP_P[36]
ZDOK1_DP_N[36]	AH8	ZDOK1_DP_N[36]
ZDOK1_DP_P[35]	AH9	ZDOK1_DP_P[35]
ZDOK1_DP_N[35]	AH10	ZDOK1_DP_N[35]
ZDOK1_DP_P[34]	AF11	ZDOK1_DP_P[34]
ZDOK1_DP_N[34]	AE11	ZDOK1_DP_N[34]
ZDOK1_DP_P[33]	AJ9	ZDOK1_DP_P[33]
ZDOK1_DP_N[33]	AJ10	ZDOK1_DP_N[33]
ZDOK1_DP_P[32]	AF9	ZDOK1_DP_P[32]
ZDOK1_DP_N[32]	AF10	ZDOK1_DP_N[32]
ZDOK1_DP_P[31]	AK8	ZDOK1_DP_P[31]
ZDOK1_DP_N[31]	AK9	ZDOK1_DP_N[31]
ZDOK1_DP_P[30]	AK11	ZDOK1_DP_P[30]
ZDOK1_DP_N[30]	AJ11	ZDOK1_DP_N[30]
ZDOK1_DP_P[29]	AD10	ZDOK1_DP_P[29]
ZDOK1_DP_N[29]	AD11	ZDOK1_DP_N[29]
ZDOK1_DP_P[28]	AE8	ZDOK1_DP_P[28]
ZDOK1_DP_N[28]	AD9	ZDOK1_DP_N[28]
ZDOK1_DP_P[27]	AL11	ZDOK1_DP_P[27]
ZDOK1_DP_N[27]	AL10	ZDOK1_DP_N[27]
ZDOK1_DP_P[26]	AC10	ZDOK1_DP_P[26]
ZDOK1_DP_N[26]	AC9	ZDOK1_DP_N[26]
ZDOK1_DP_P[25]	AM12	ZDOK1_DP_P[25]
ZDOK1_DP_N[25]	AM11	ZDOK1_DP_N[25]
ZDOK1_DP_P[24]	AC8	ZDOK1_DP_P[24]
ZDOK1_DP_N[24]	AB8	ZDOK1_DP_N[24]
ZDOK1_DP_P[23]	AP12	ZDOK1_DP_P[23]
ZDOK1_DP_N[23]	AN12	ZDOK1_DP_N[23]
ZDOK1_DP_P[22]	AA8	ZDOK1_DP_P[22]
ZDOK1_DP_N[22]	AA9	ZDOK1_DP_N[22]
ZDOK1_DP_P[21]	AN13	ZDOK1_DP_P[21]
ZDOK1_DP_N[21]	AM13	ZDOK1_DP_N[21]
ZDOK1_DP_P[20]	AB10	ZDOK1_DP_P[20]
ZDOK1_DP_N[20]	AA10	ZDOK1_DP_N[20]
ZDOK1_DP_P[19]	AN14	ZDOK1_DP_P[19]
ZDOK1_DP_N[19]	AP14	ZDOK1_DP_N[19]
ZDOK1_DP_P[18]	V10	ZDOK1_DP_P[18]
ZDOK1_DP_N[18]	V9	ZDOK1_DP_N[18]
ZDOK1_DP_P[17]	AK7	ZDOK1_DP_P[17]
ZDOK1_DP_N[17]	AK6	ZDOK1_DP_N[17]
ZDOK1_DP_P[16]	V8	ZDOK1_DP_P[16]
ZDOK1_DP_N[16]	U8	ZDOK1_DP_N[16]
ZDOK1_DP_P[15]	AJ7	ZDOK1_DP_P[15]
ZDOK1_DP_N[15]	AJ6	ZDOK1_DP_N[15]
ZDOK1_DP_P[14]	W10	ZDOK1_DP_P[14]
ZDOK1_DP_N[14]	W9	ZDOK1_DP_N[14]
ZDOK1_DP_P[13]	AH7	ZDOK1_DP_P[13]
ZDOK1_DP_N[13]	AG7	ZDOK1_DP_N[13]
ZDOK1_DP_P[12]	Y11	ZDOK1_DP_P[12]
ZDOK1_DP_N[12]	W11	ZDOK1_DP_N[12]
ZDOK1_DP_P[11]	W7	ZDOK1_DP_P[11]
ZDOK1_DP_N[11]	V7	ZDOK1_DP_N[11]
ZDOK1_DP_P[10]	AG5	ZDOK1_DP_P[10]
ZDOK1_DP_N[10]	AF5	ZDOK1_DP_N[10]
ZDOK1_DP_P[9]	AE7	ZDOK1_DP_P[9]
ZDOK1_DP_N[9]	AF6	ZDOK1_DP_N[9]
ZDOK1_DP_P[8]	W6	ZDOK1_DP_P[8]
ZDOK1_DP_N[8]	Y6	ZDOK1_DP_N[8]
ZDOK1_DP_P[7]	AD6	ZDOK1_DP_P[7]
ZDOK1_DP_N[7]	AE6	ZDOK1_DP_N[7]
ZDOK1_DP_P[6]	AA6	ZDOK1_DP_P[6]
ZDOK1_DP_N[6]	Y7	ZDOK1_DP_N[6]
ZDOK1_DP_P[5]	AD4	ZDOK1_DP_P[5]
ZDOK1_DP_N[5]	AD5	ZDOK1_DP_N[5]
ZDOK1_DP_P[4]	Y8	ZDOK1_DP_P[4]
ZDOK1_DP_N[4]	Y9	ZDOK1_DP_N[4]
ZDOK1_DP_P[3]	AC7	ZDOK1_DP_P[3]
ZDOK1_DP_N[3]	AD7	ZDOK1_DP_N[3]
ZDOK1_DP_P[2]	AA5	ZDOK1_DP_P[2]
ZDOK1_DP_N[2]	AB5	ZDOK1_DP_N[2]
ZDOK1_DP_P[1]	AB6	ZDOK1_DP_P[1]
ZDOK1_DP_N[1]	AB7	ZDOK1_DP_N[1]
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ZDOK1_DP_N[0]	AC5	ZDOK1_DP_N[0]

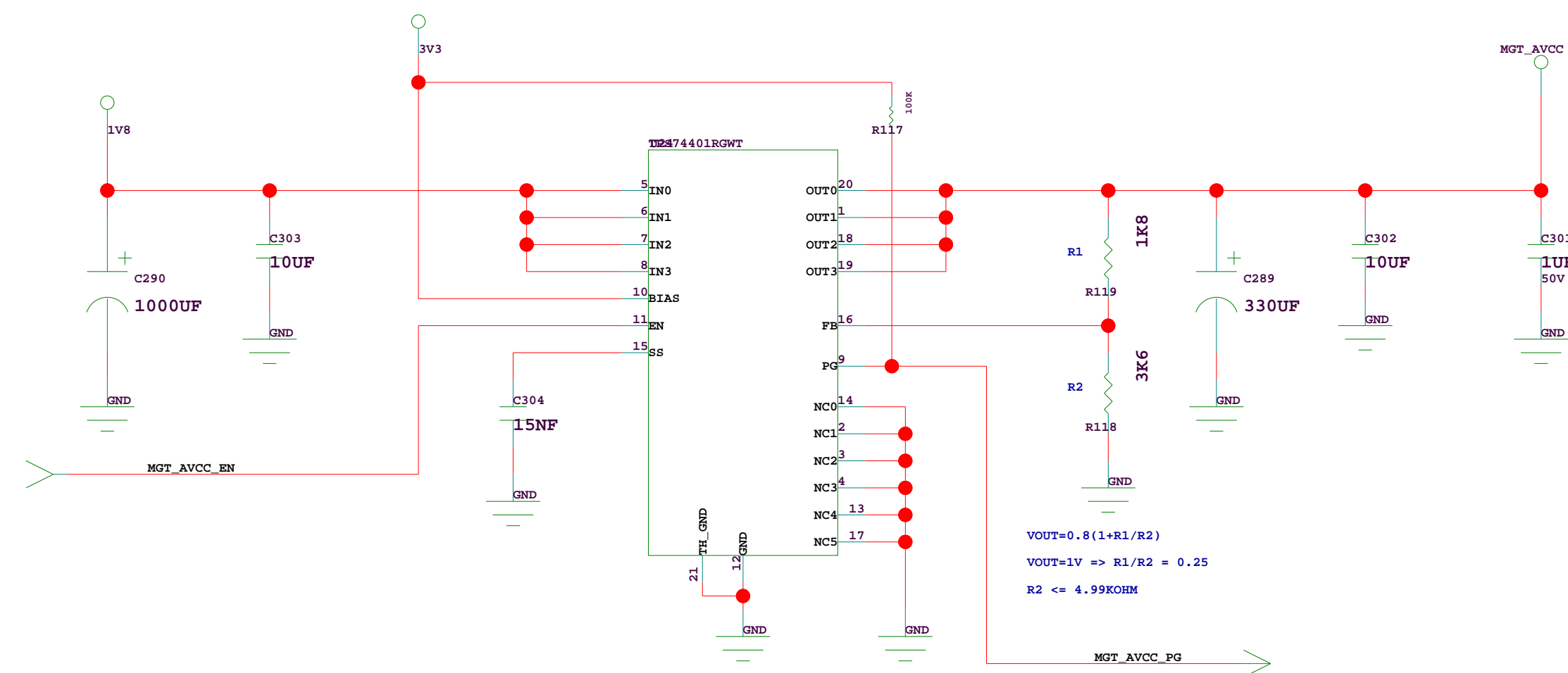
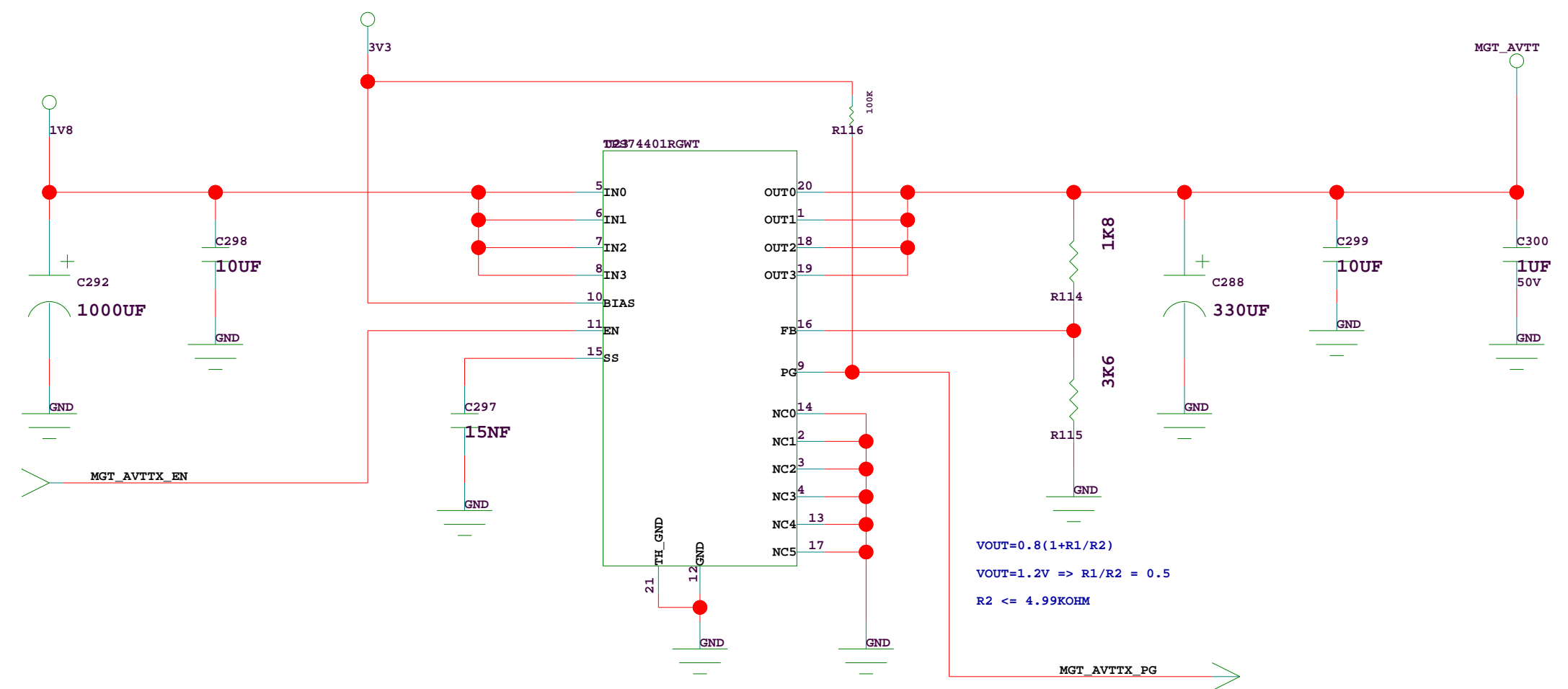
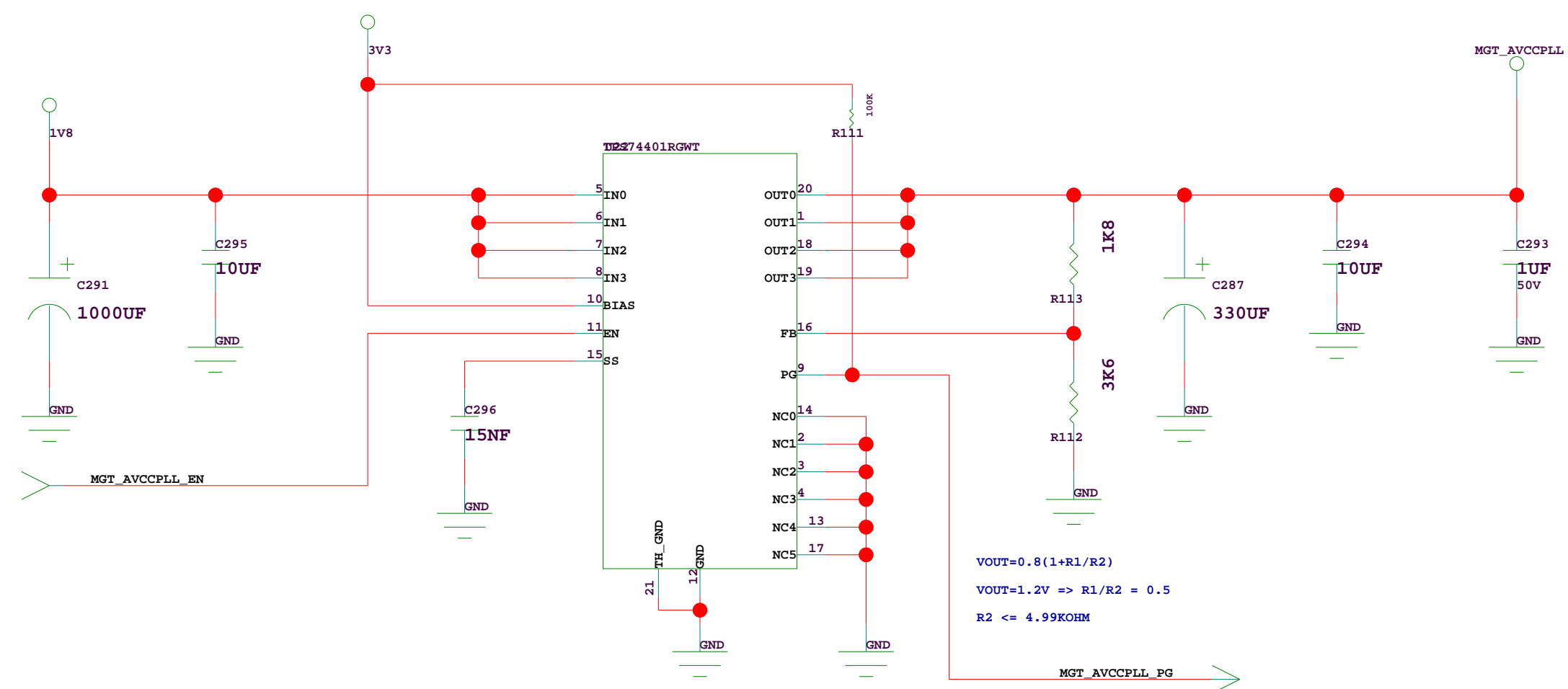


ZDOK1_DP_P[0]	A1	C1	C1	ZDOK1_DP_P[20]
ZDOK1_DP_N[0]	A2	C2	C2	ZDOK1_DP_N[20]
ZDOK1_DP_P[1]	A3	C3	C3	ZDOK1_DP_P[21]
ZDOK1_DP_N[1]	A4	C4	C4	ZDOK1_DP_N[21]
ZDOK1_DP_P[2]	A5	C5	C5	ZDOK1_DP_P[22]
ZDOK1_DP_N[2]	A6	C6	C6	ZDOK1_DP_N[22]
ZDOK1_DP_P[3]	A7	C7	C7	ZDOK1_DP_P[23]
ZDOK1_DP_N[3]	A8	C8	C8	ZDOK1_DP_N[23]
ZDOK1_DP_P[4]	A9	C9	C9	ZDOK1_DP_P[24]
ZDOK1_DP_N[4]	A10	C10	C10	ZDOK1_DP_N[24]
ZDOK1_DP_P[5]	A11	C11	C11	ZDOK1_DP_P[25]
ZDOK1_DP_N[5]	A12	C12	C12	ZDOK1_DP_N[25]
ZDOK1_DP_P[6]	A13	C13	C13	ZDOK1_DP_P[26]
ZDOK1_DP_N[6]	A14	C14	C14	ZDOK1_DP_N[26]
ZDOK1_DP_P[7]	A15	C15	C15	ZDOK1_DP_P[27]
ZDOK1_DP_N[7]	A16	C16	C16	ZDOK1_DP_N[27]
ZDOK1_DP_P[8]	A17	C17	C17	ZDOK1_DP_P[28]
ZDOK1_DP_N[8]	A18	C18	C18	ZDOK1_DP_N[28]
ZDOK1_DP_P[9]	A19	C19	C19	ZDOK1_DP_P[29]
ZDOK1_DP_N[9]	A20	C20	C20	ZDOK1_DP_N[29]
ZDOK1_DP_P[10]	D1	F1	F1	ZDOK1_DP_P[30]
ZDOK1_DP_N[10]	D2	F2	F2	ZDOK1_DP_N[30]
ZDOK1_DP_P[11]	D3	F3	F3	ZDOK1_DP_P[31]
ZDOK1_DP_N[11]	D4	F4	F4	ZDOK1_DP_N[31]
ZDOK1_DP_P[12]	D5	F5	F5	ZDOK1_DP_P[32]
ZDOK1_DP_N[12]	D6	F6	F6	ZDOK1_DP_N[32]
ZDOK1_DP_P[13]	D7	F7	F7	ZDOK1_DP_P[33]
ZDOK1_DP_N[13]	D8	F8	F8	ZDOK1_DP_N[33]
ZDOK1_DP_P[14]	D9	F9	F9	ZDOK1_DP_P[34]
ZDOK1_DP_N[14]	D10	F10	F10	ZDOK1_DP_N[34]
ZDOK1_DP_P[15]	D11	F11	F11	ZDOK1_DP_P[35]
ZDOK1_DP_N[15]	D12	F12	F12	ZDOK1_DP_N[35]
ZDOK1_DP_P[16]	D13	F13	F13	ZDOK1_DP_P[36]
ZDOK1_DP_N[16]	D14	F14	F14	ZDOK1_DP_N[36]
ZDOK1_DP_P[17]	D15	F15	F15	ZDOK1_DP_P[37]
ZDOK1_DP_N[17]	D16	F16	F16	ZDOK1_DP_N[37]
ZDOK1_DP_P[18]	D17	F17	F17	ZDOK1_CLK0_P
ZDOK1_DP_N[18]	D18	F18	F18	ZDOK1_CLK0_N
ZDOK1_DP_P[19]	D19	F19	F19	ZDOK1_CLK1_P
ZDOK1_DP_N[19]	D20	F20	F20	ZDOK1_CLK1_N



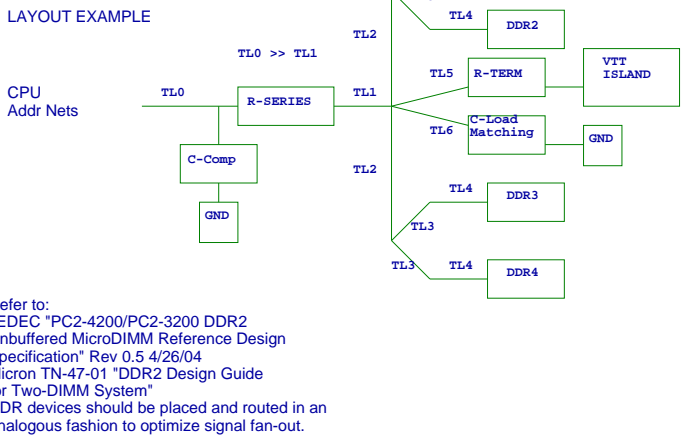














The RGMII signaling is 125 MHz using both rising and falling edges of the clock.  
The Tx and the Rx side trace length should be matched within the signal group to minimize timing skew.  
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.  
Minimize the number of vias on the RGMII lines to minimize timing skew.  
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

10

ETHERNET Mgt

ETHERNET Mgt

ETHERNET Mgt

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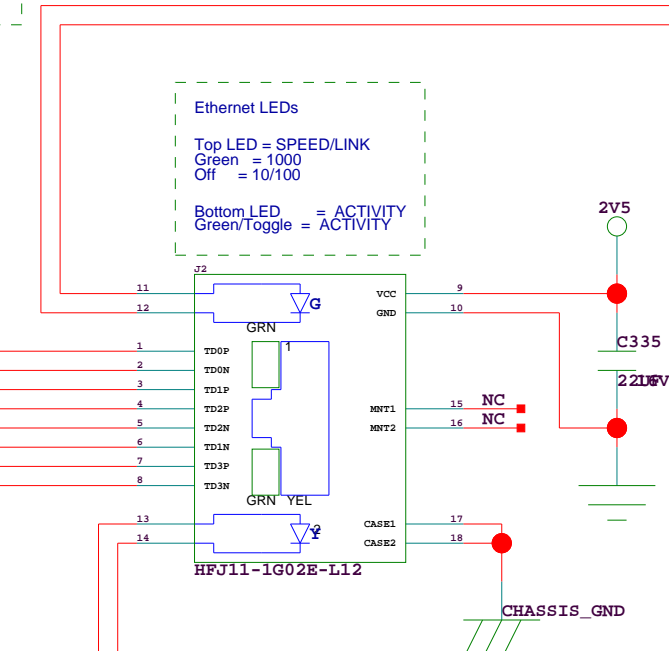
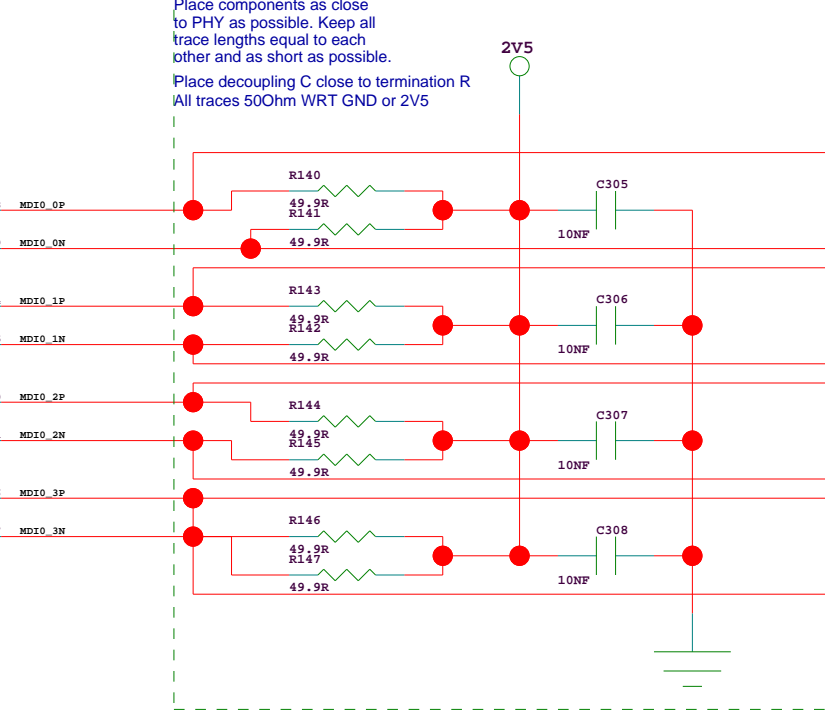
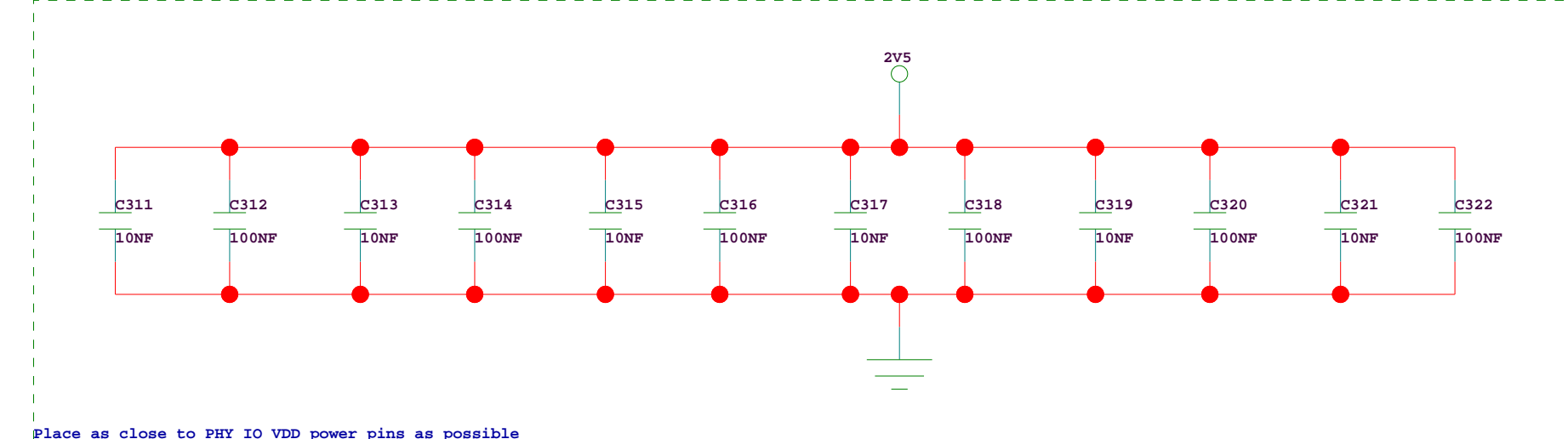
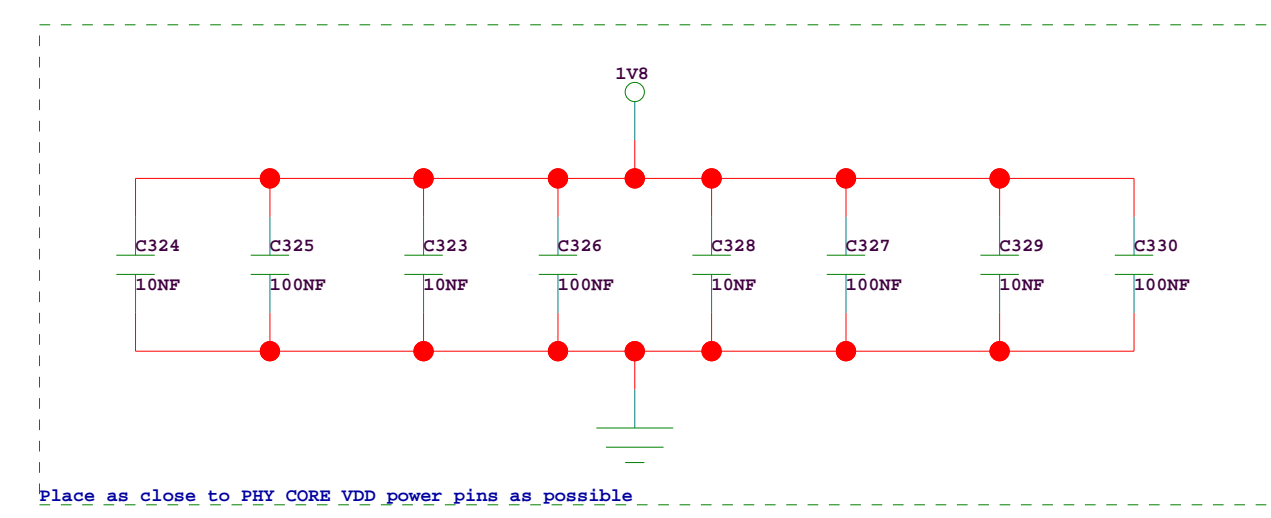
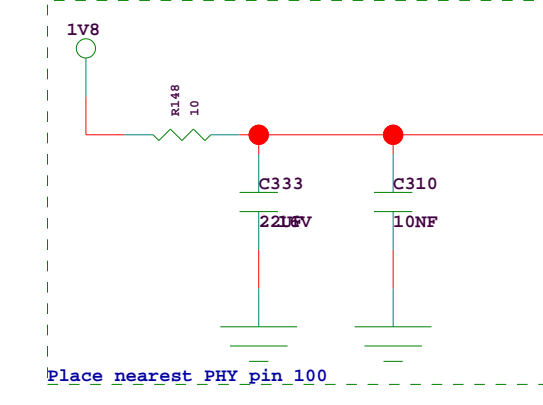
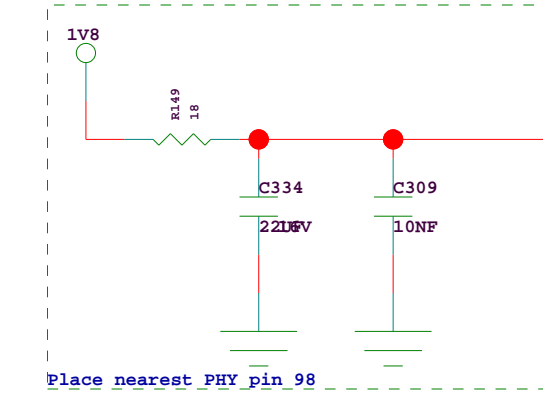
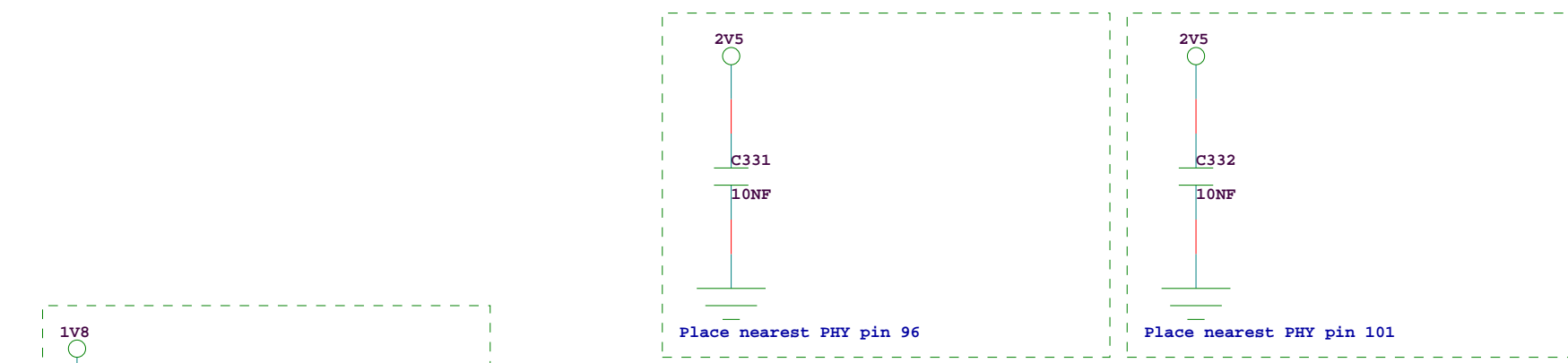
ETHERNET Mgt

ETHERNET Mgt

ETHERNET Mgt

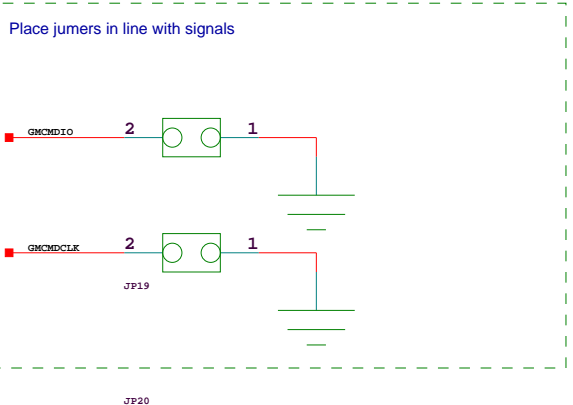
ETHERNET Mgt

ETHERNET Mgt



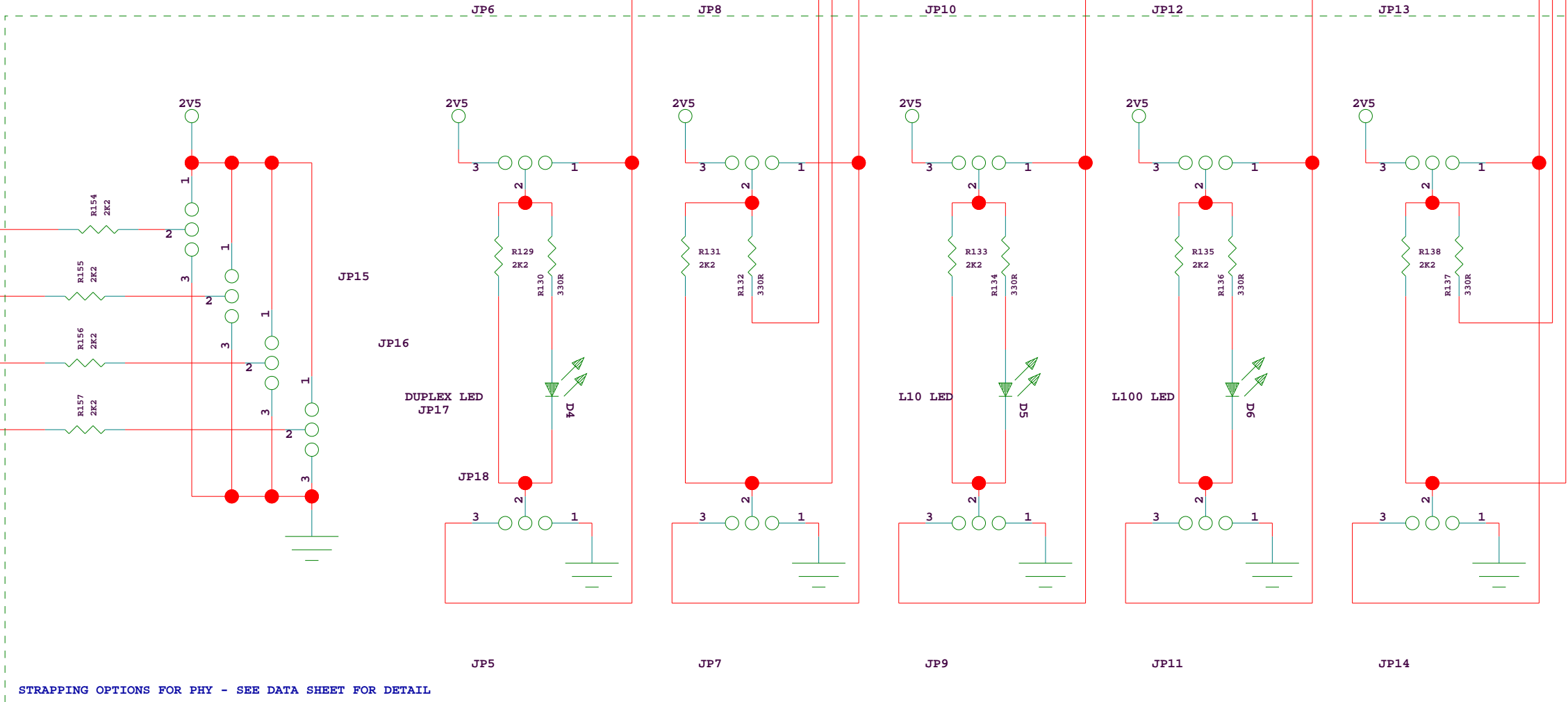
Place resistors as close to CPU as possible and keep all traces lengths equal

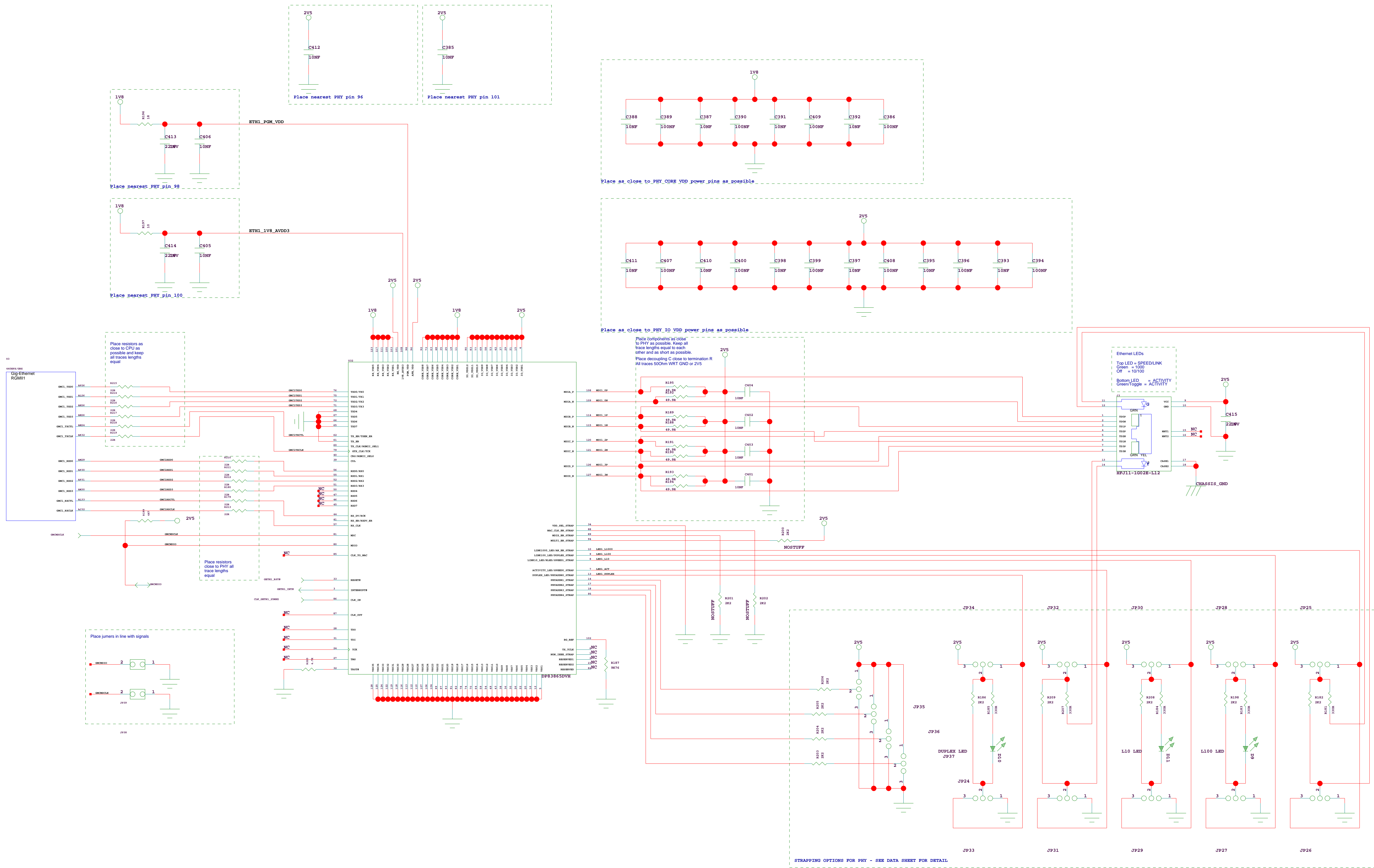
Place resistors close to PHY all trace lengths equal

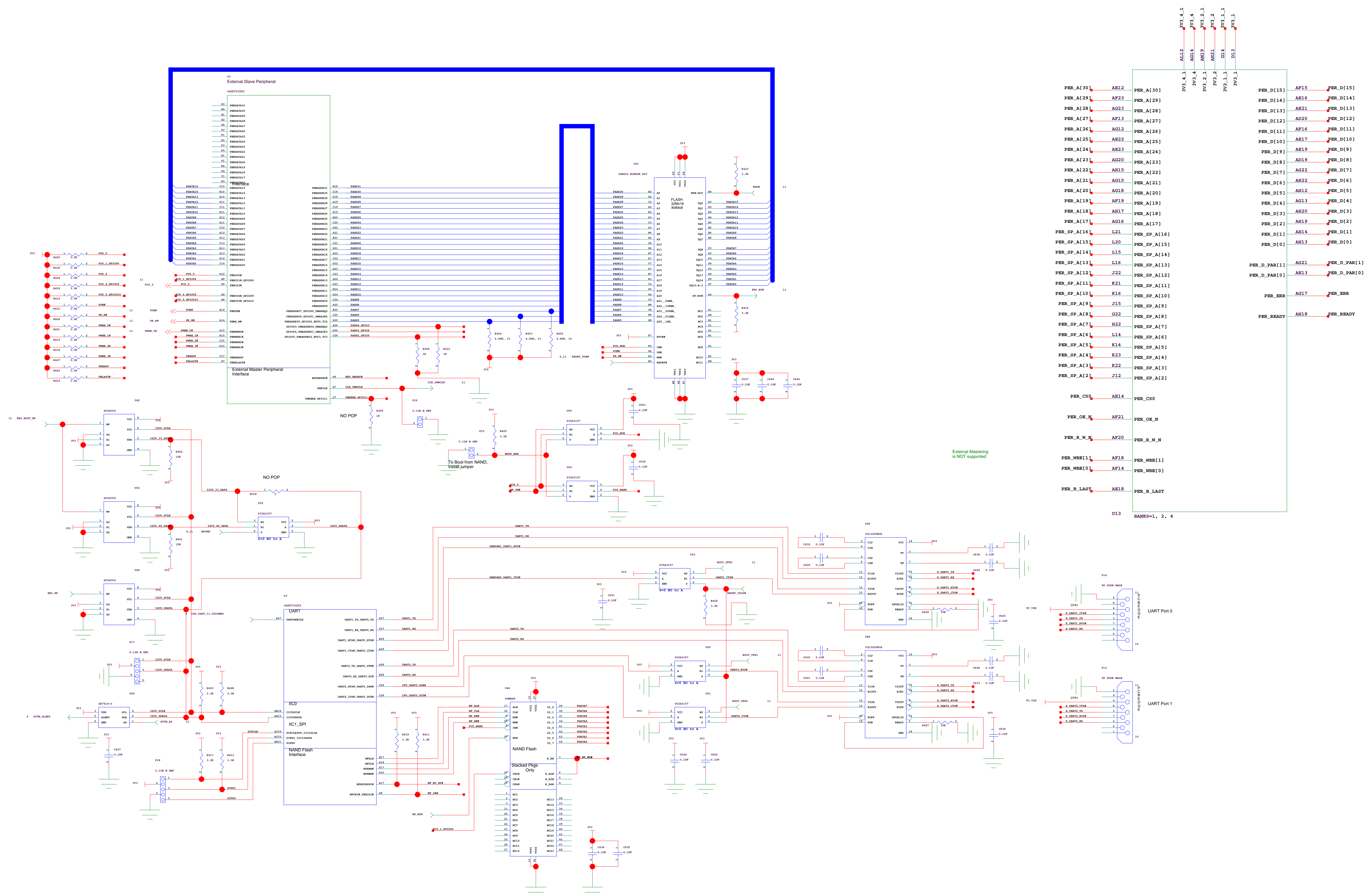


NO STUFF

NO STUFF



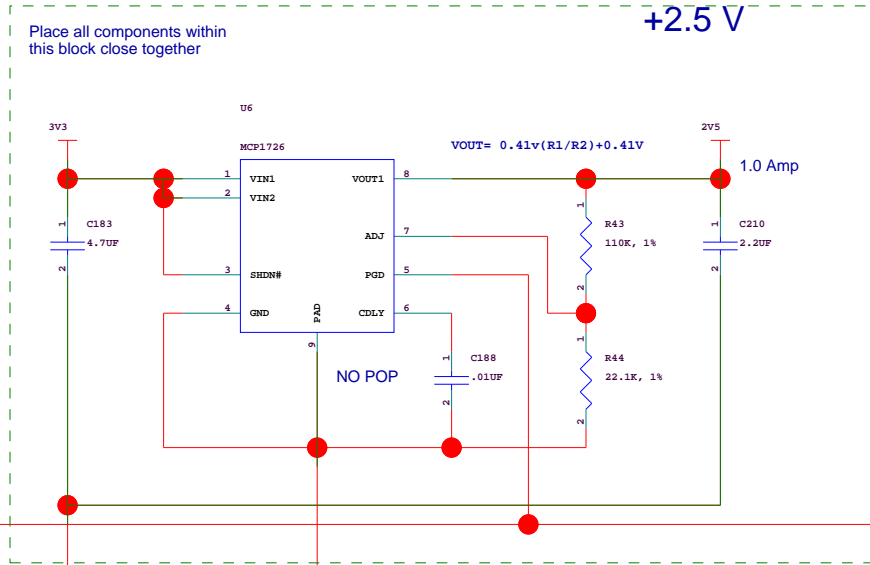
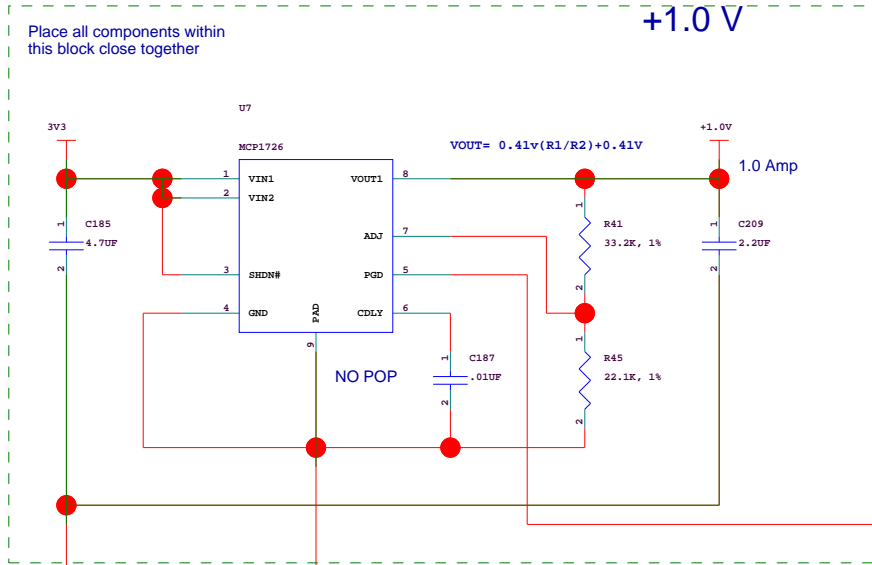
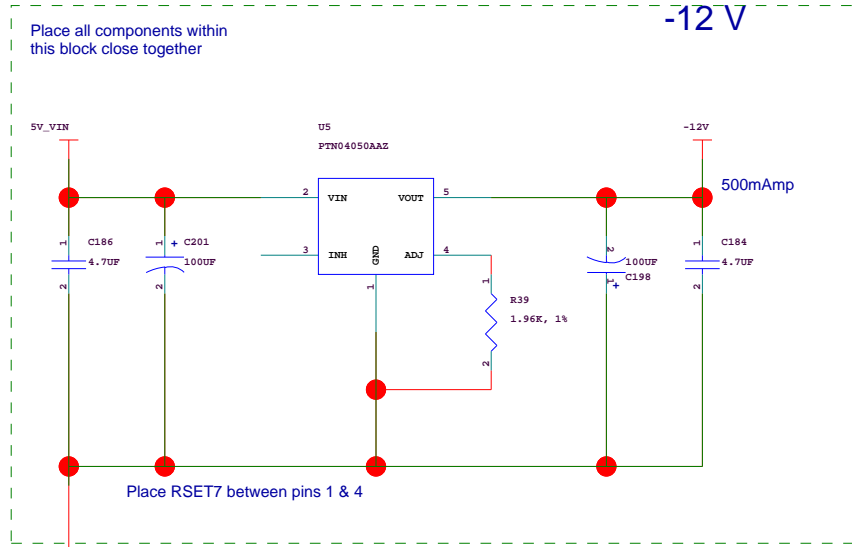
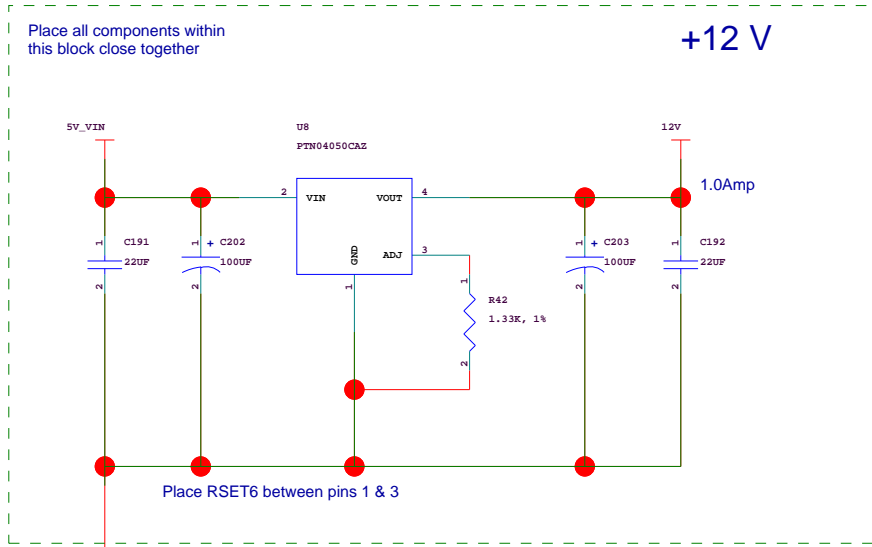
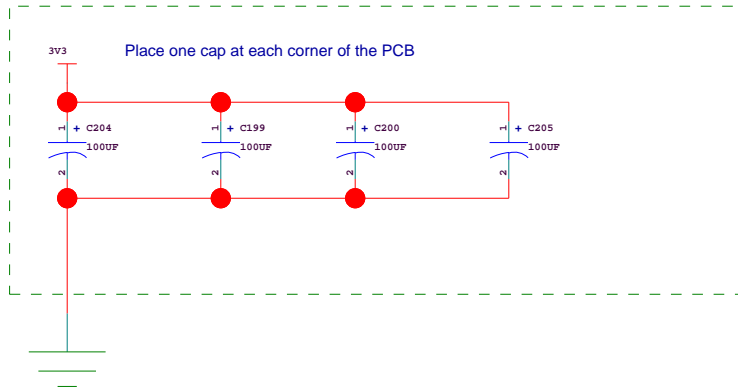
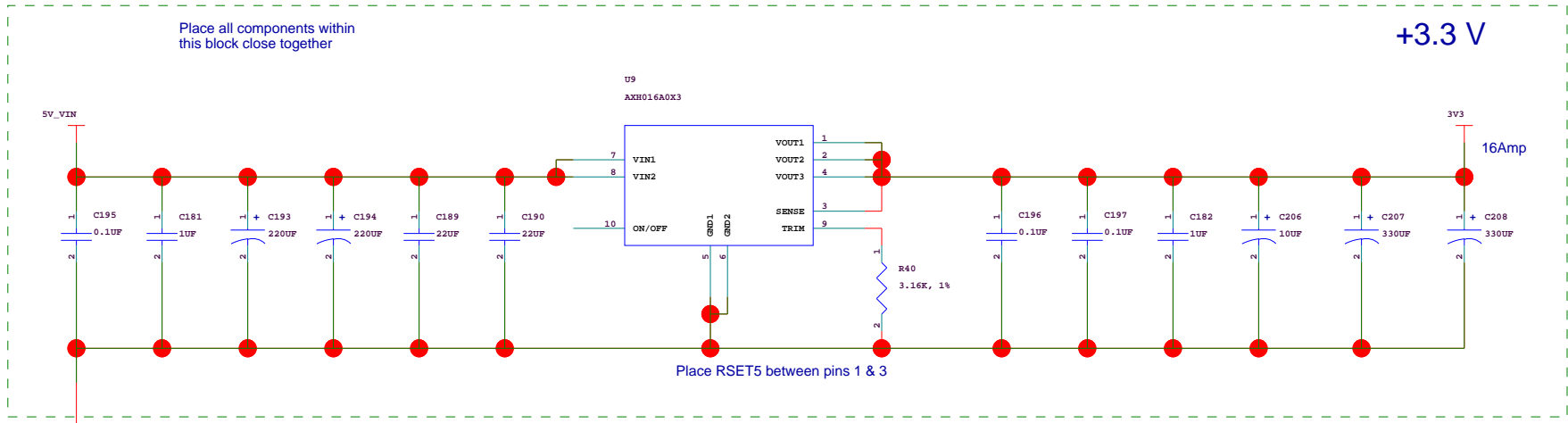














F

E

D

C

B

A

F

E

D

C

B

A

PWR\_GOOD monitors the  
+1.0v, 1V5, 1V8,  
2V5, and 3V3 supplies

IRQ0-9 have programmable polarity per  
section 10.5.7 (UIC0\_PR) 440ep user  
manual

Critical Placement and Route  
Clock Rules:

Clock Rules:  
CLK\_UART1\_11.0592mhz = as short as possible  
CLK\_SYS\_33mhz = as short as possible  
CLK\_CPLD\_33mhz = CLK\_SYS\_33mhz

Critical Placement and Route  
Clock Rules:


Clock Rules:  
CLK\_PC13\_66/33mhz = as short as possible  
CLK\_PC12\_66/33mhz = CLK\_PC13\_66/33mhz  
CLK\_PC11\_66/33mhz = CLK\_PC12\_66/33mhz + 2.5"  
CLK\_GETH0\_25mhz = as short as possible  
CLK\_GETH1\_25mhz = CLK\_GETH0\_25mhz  
CLK\_CPLD\_50mhz = as short as possible  
CLK\_USB2\_0\_48mhz = as short as possible  
CLK\_USB2\_0\_12mhz = as short as possible

TRACE & JTAG CONNECTORS

Critical placement and routing  
of the Trace connector and nets.  
Up to CPU frequency/4

TRACE PORT

R26 is for current  
limiting and should  
be <100 Ohms.



**KAROO ARRAY TELESCOPE, NRF**  
UNIT 12, LONSDALE BUILDING  
LONSDALE WAY, PINELANDS, 7405  
SOUTH AFRICA

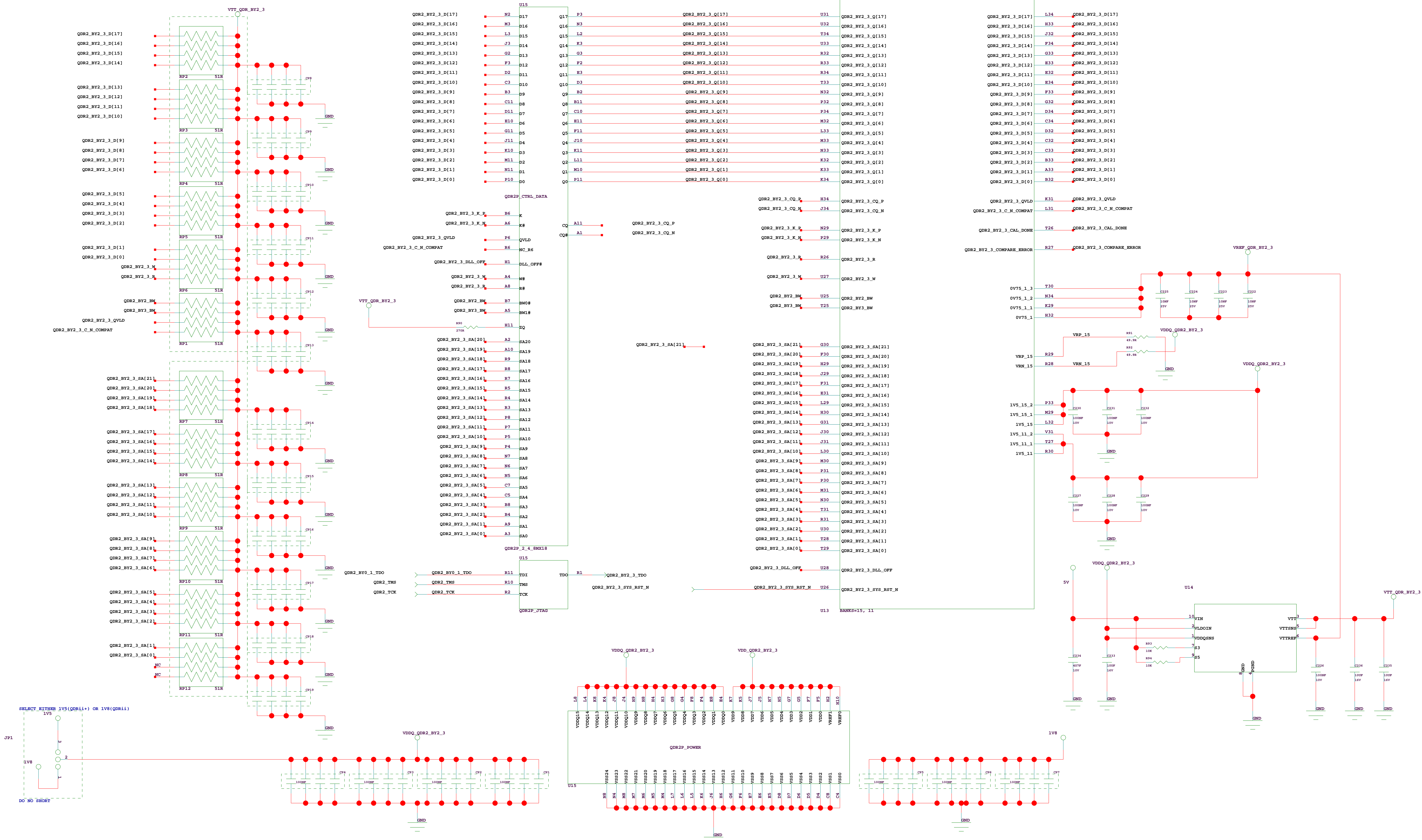
TITLE

**ROACH\_PPC\_TST\_CLK\_IO**

CHECKED BY	DWG NO	REV
<PUT NAME HERE>	A2	0
DRAWN BY	SCALE	SHEET
<PUT NAME HERE>	NTS	1 of 1

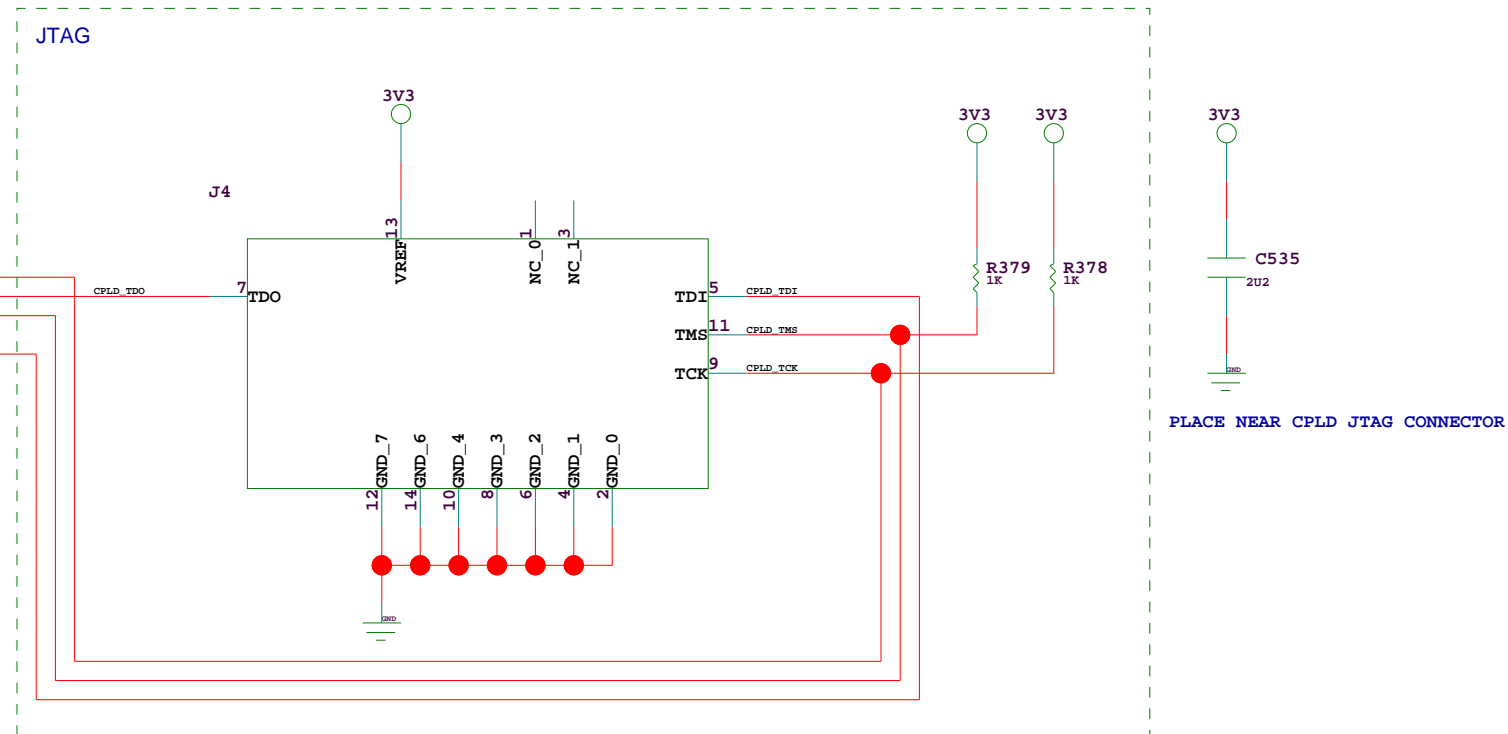
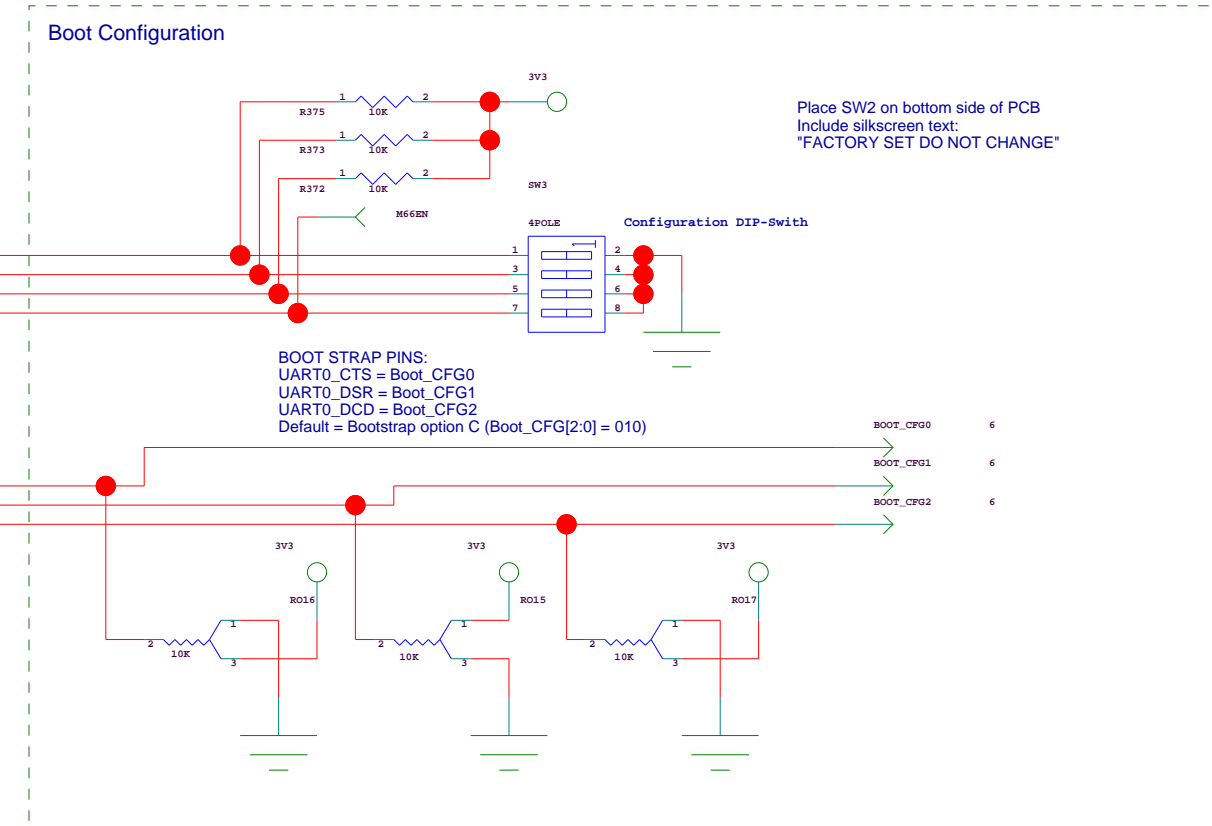
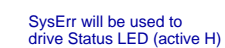
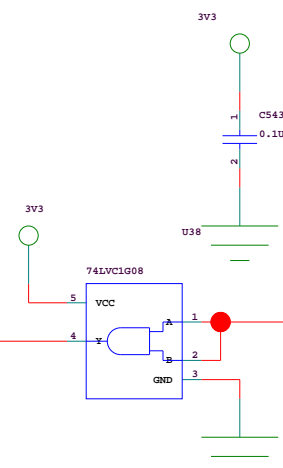
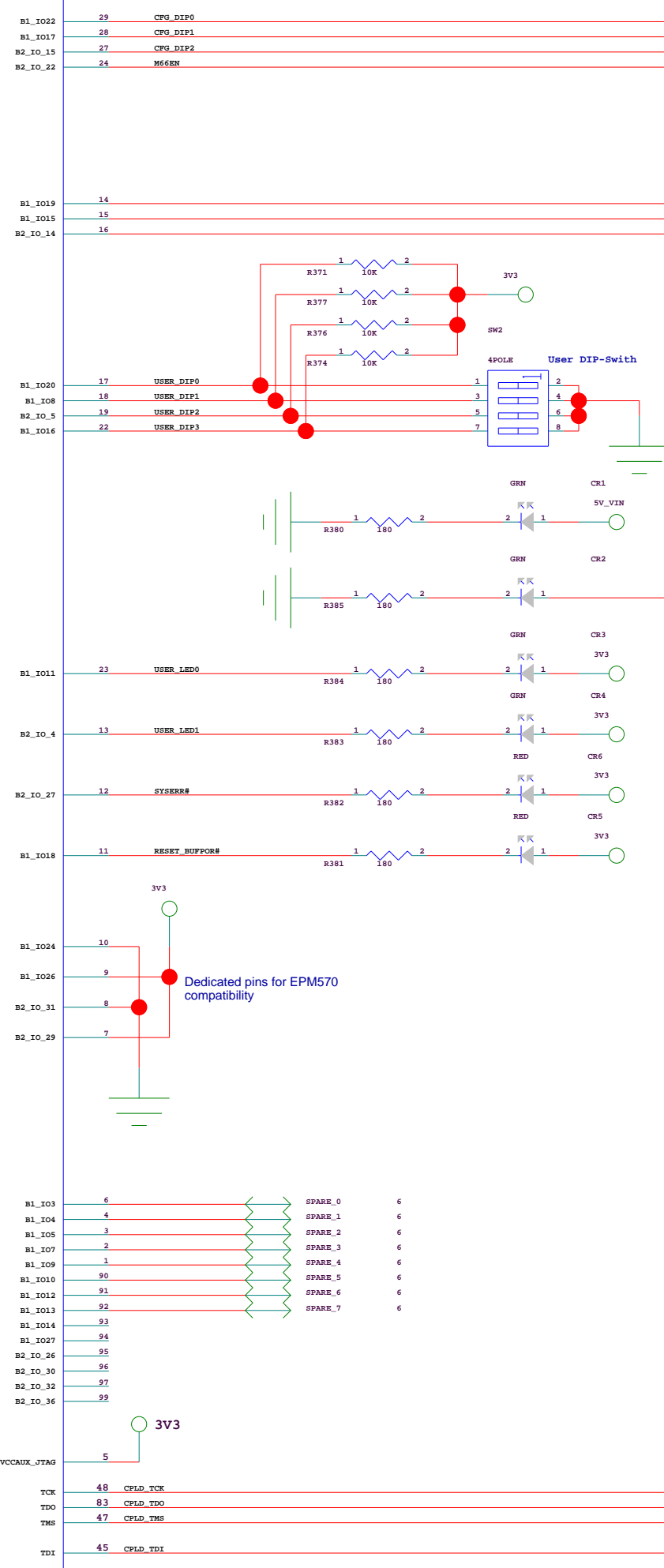
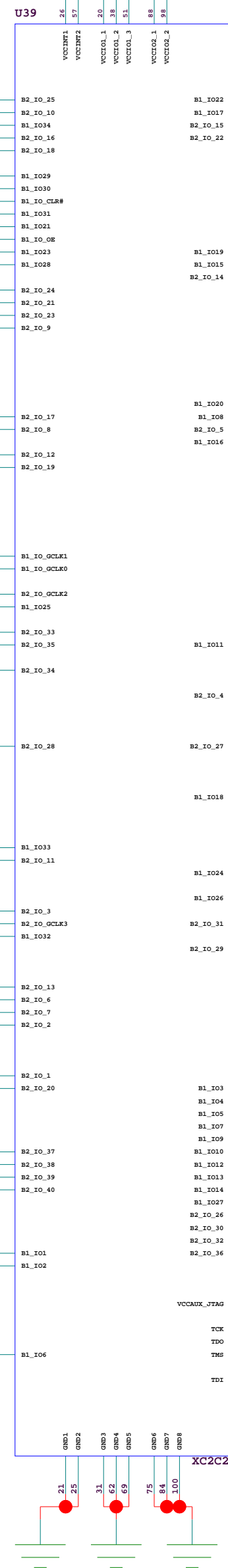
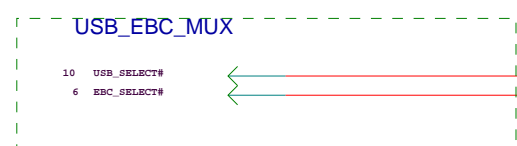
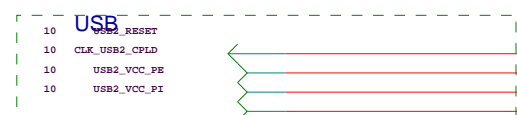
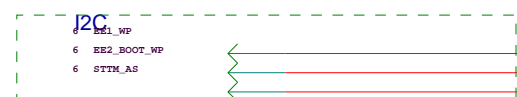
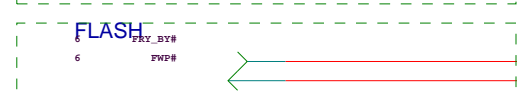
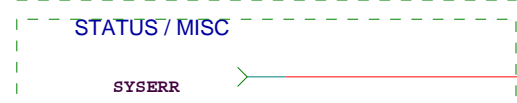
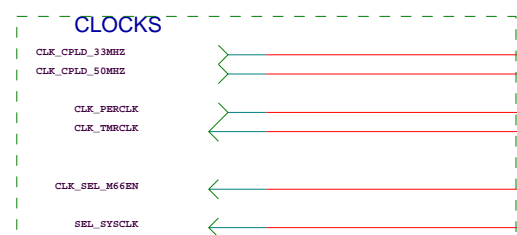
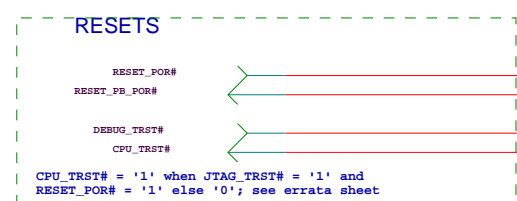
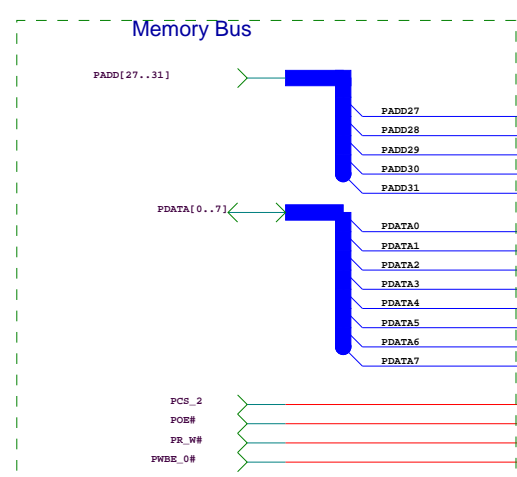
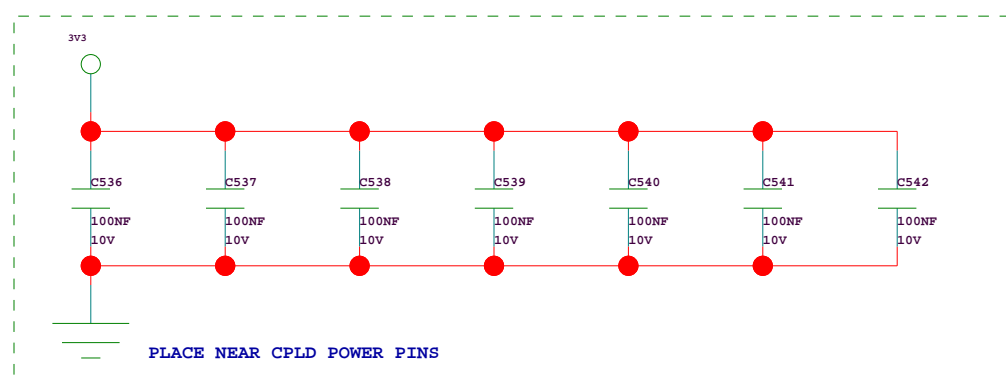
9-3-2007\_12:23











Assertion of USB2\_RESET may be asynchronous to CLK\_USB2\_CPLD  
De-assertion of USB2\_RESET must be synchronous to CLK\_USB2\_CPLD

PLACE NEAR CPLD JTAG CONNECTOR

