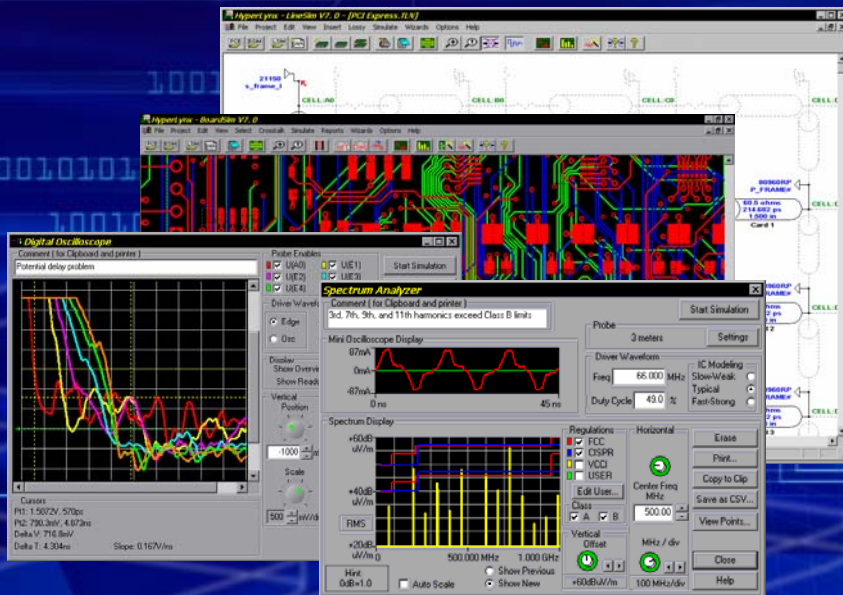


HyperLynx

Signal Integrity and EMC Software for High-Speed PCB Design

DDR2 Technology Webinar



Steve McKinney

Technical Marketing Engineer

Steven_McKinney@Mentor.com

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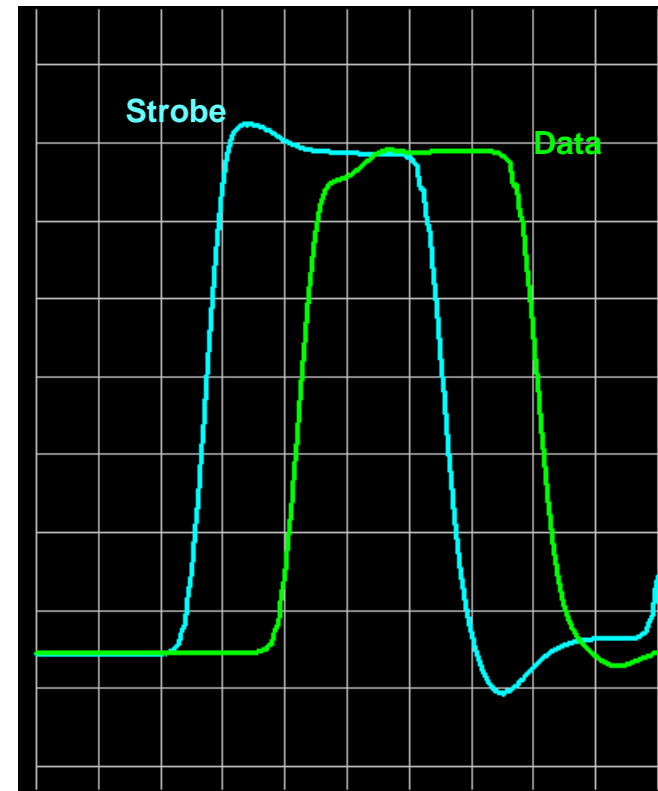
HyperLynx High Speed Webinars

www.mentor.com/pcb/events

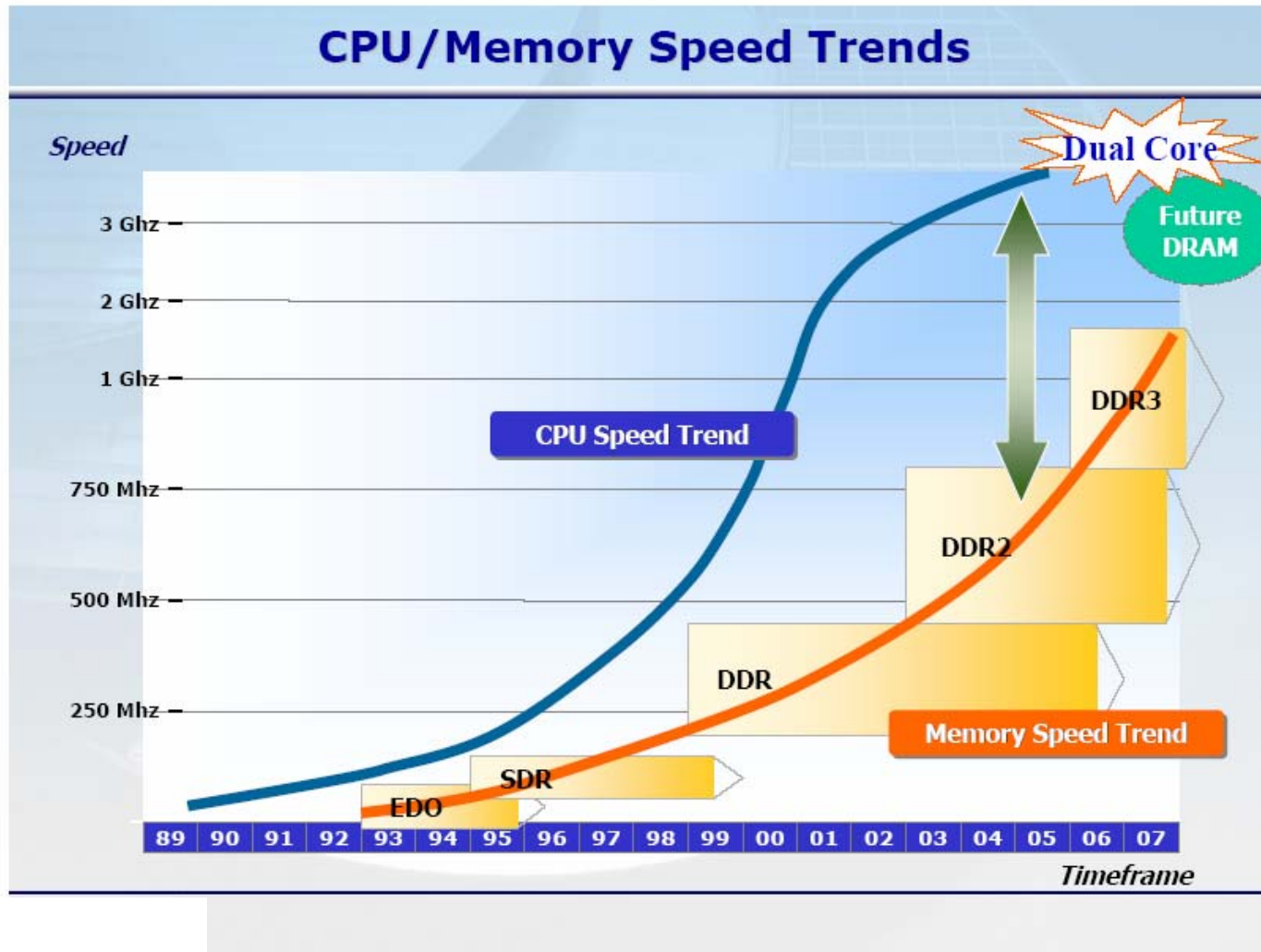
Presentation Date	Topics
	+
23-Aug	IBIS Model Validation & Verification
6-Sep	Differential Signaling: Simulating Skew Sensitivity & Noise Rejection
13-Sep	Controlling Crosstalk in High-Speed PCB Design
20-Sep	SATA - Successful Serial ATA Design
4-Oct	Controlling Emissions, EMI, EMC
18-Oct	PCI Express Interconnect Design
1-Nov	DDR2 Design Dos and Don'ts
15-Nov	Timing is Everything in Common Clock Designs
29-Nov	Technology, Topology, & Termination: Fundamentals of High-Speed Design
13-Dec	SERDES Design Made Easy

HyperLynx DDR2 Technology Kit

1. **Introduction**
2. **DDR/DDR2 Overview**
3. **Design Challenges**
4. **Simulation**
5. **Design Guidelines**



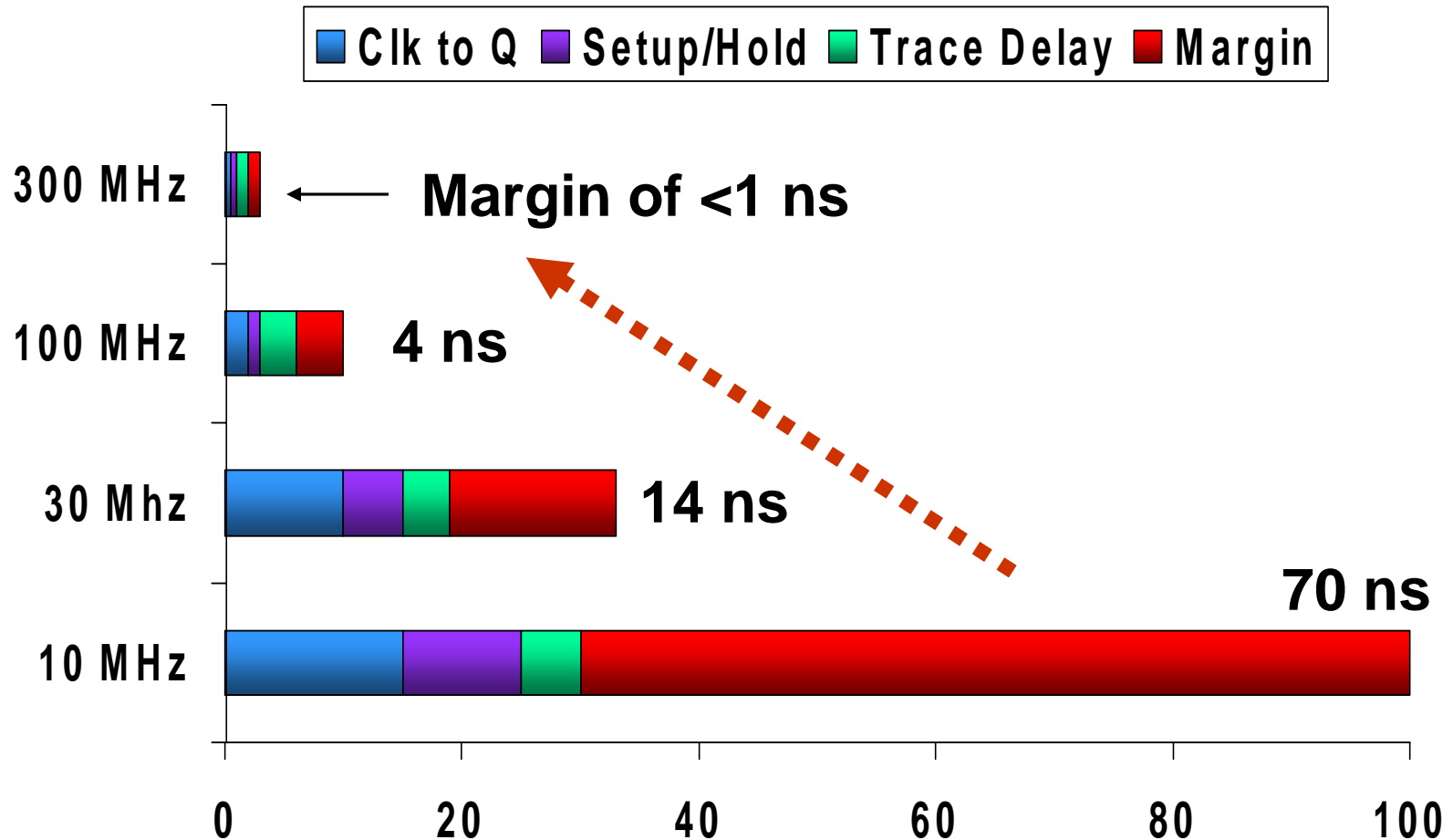
Memory Trends



*Courtesy of Hynix Semiconductor

Faster Clocks

Tighter Timing Budgets

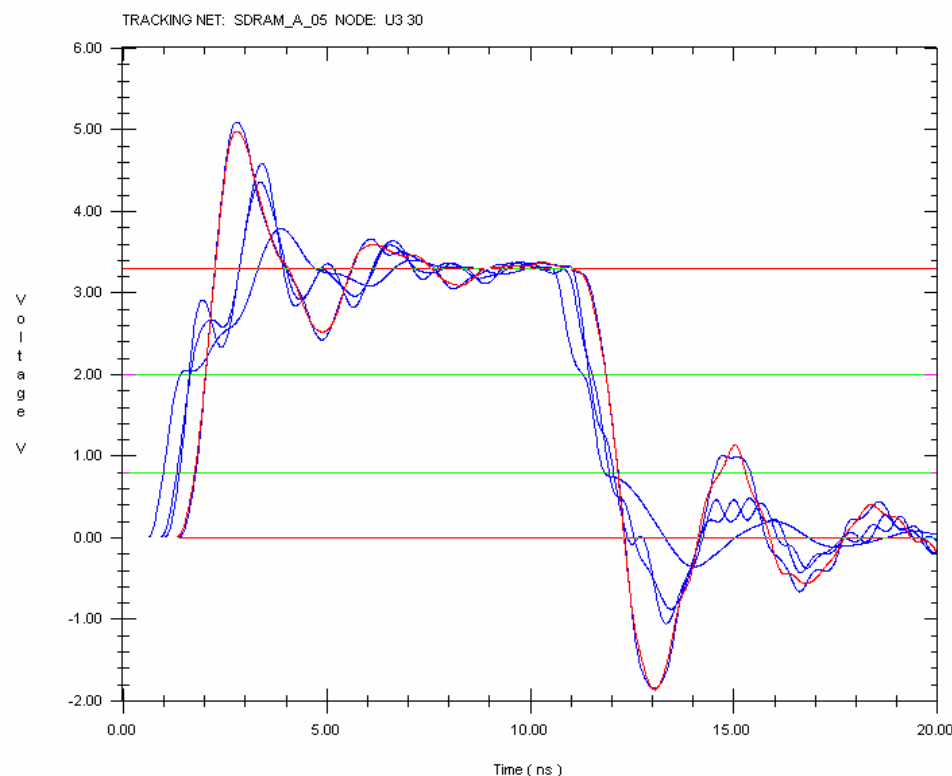


Faster Edge Rates

Poor Signal Integrity

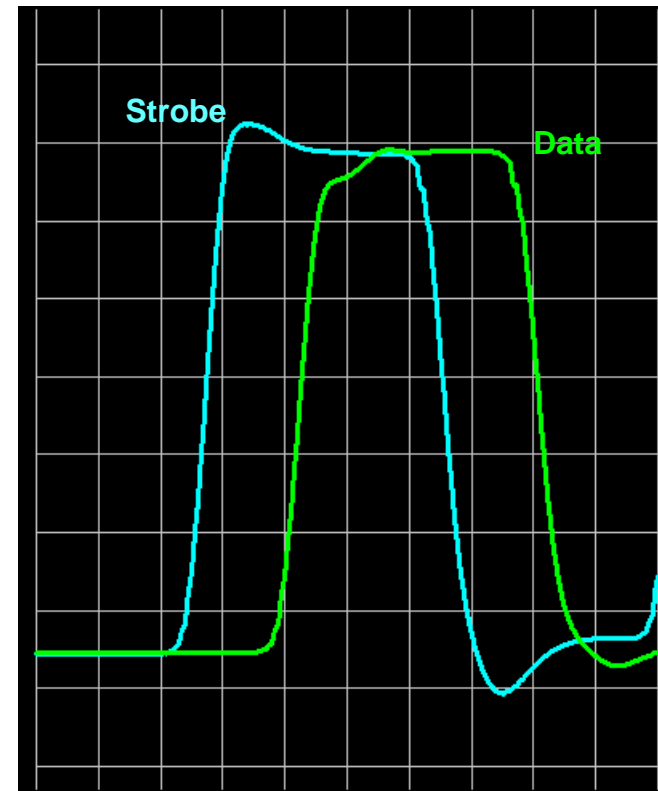
■ Faster Clocks mean faster edge rates

- What kind of problems can you expect on your PCB board?
- Threshold errors
- Ringing
- Delay errors
- Overshoot
- Oscillation
- Crosstalk
- EMI problems



HyperLynx DDR2 Technology Kit

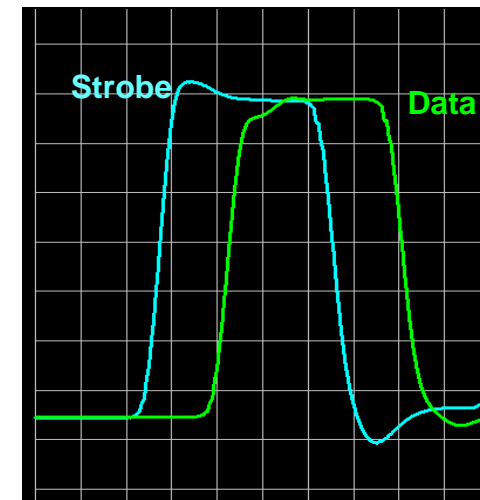
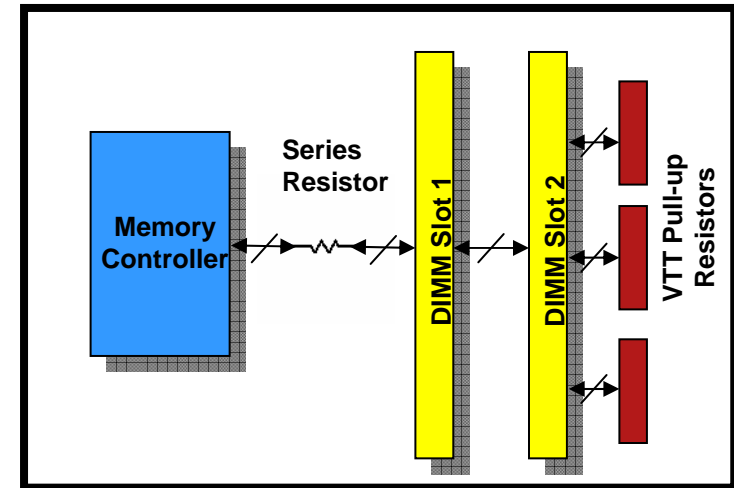
1. Introduction
2. **DDR/DDR2 Overview**
3. Design Challenges
4. Simulation
5. Design Guidelines



DDR Technology

■ DDR Operating Speeds

- DDR200 (100 MHz clock)
- DDR266 (133 MHz clock)
- DDR333 (166.67 MHz clock)
- DDR400 (200 MHz clock)



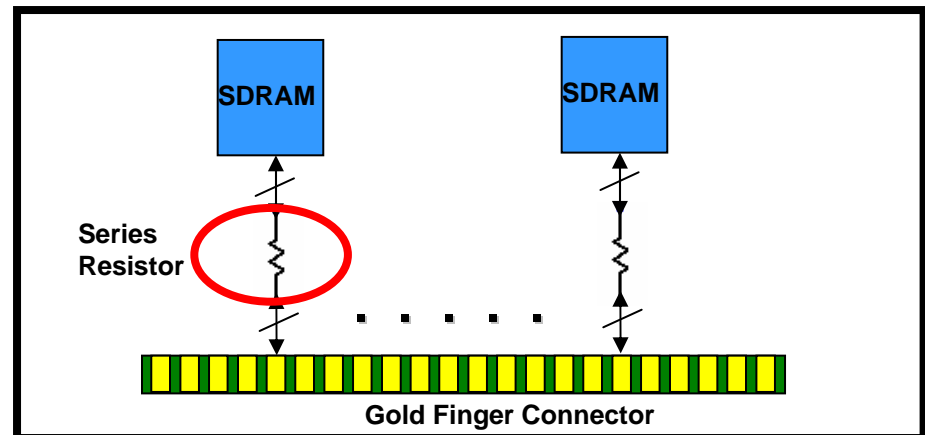
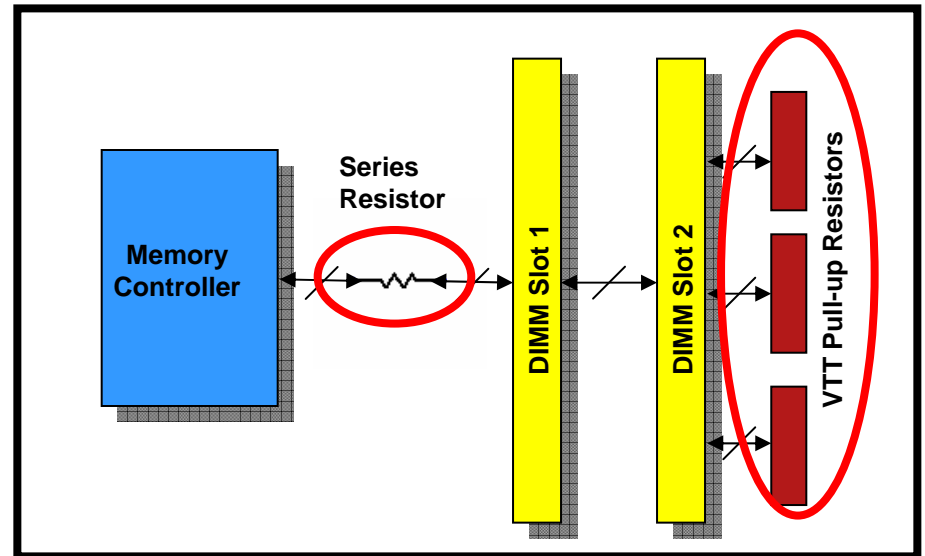
DDR Termination

■ Termination

— Requires series termination

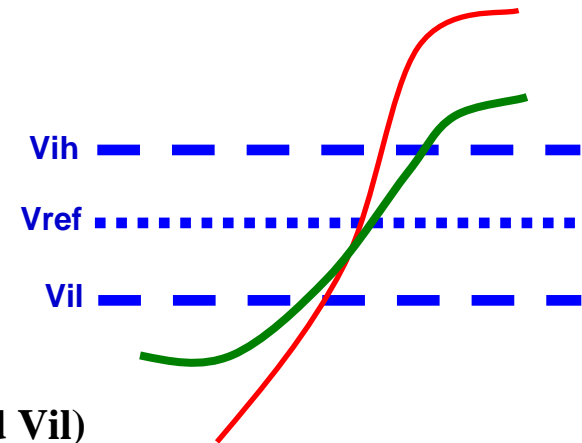
- Series terminator on DIMMs
- Series terminator on your PCB

— Pull-up termination to V_{tt}



DDR Electrical Characteristics

- DDR uses SSTL_2 buffer technology
 - 2.5V technology
 - Class I drivers for point to point connection – Half drive strength
 - Class II drivers for multi-drop connection – Full drive strength
- Some important voltages to remember
 - $V_{ref} = 1.25V$
 - Used for setting up timing thresholds (V_{ih} and V_{il})
 - Must be kept stable
 - $V_{ih} = 1.56V$ Nominal
 - $V_{ref} + 0.31$ - Logic high threshold
 - $V_{il} = 0.97V$ Nominal
 - $V_{ref} - 0.31$ - Logic low threshold

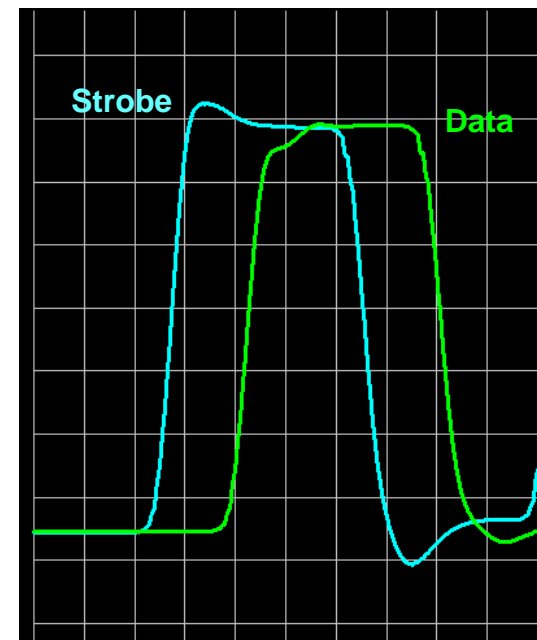
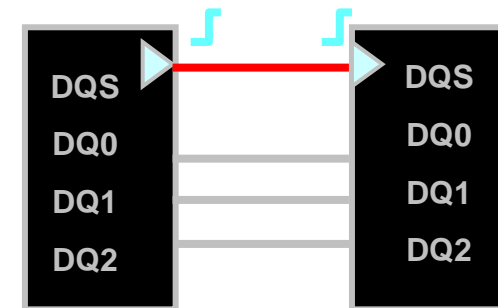


DDR2 Technology

■ DDR2 Operating Speeds

- DDR2-400 (200 MHz clock)
- DDR2-533 (266 MHz clock)
- DDR2-667 (333 MHz clock)
- DDR2-800 (400 MHz clock)

■ Source-Synchronous interface like original DDR



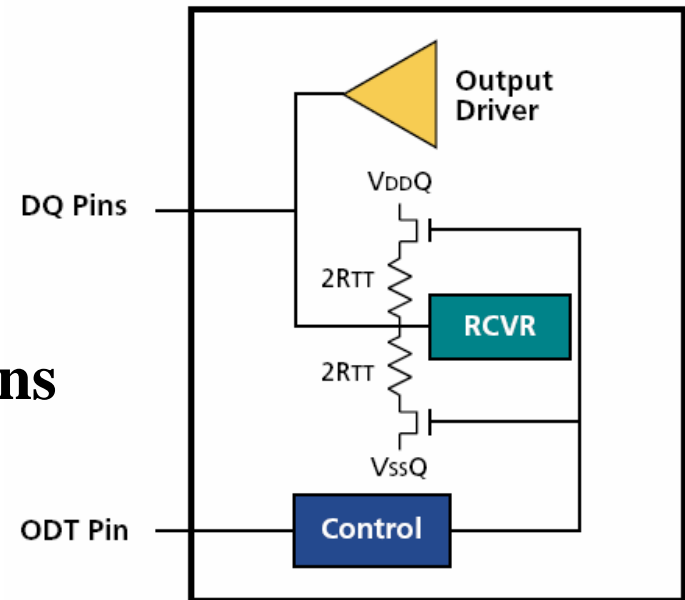
DDR2 Bandwidth

- **Not necessarily improved bandwidth over DDR**
 - Original DDR2 has higher latency than DDR reducing effective bandwidth.
 - New lower latency DDR2 memory modules are improving this gap

Memory Bandwidth (Single Channel)					
DDR		DDR2			
DDR333	DDR400	DDR2-400	DDR2-533	DDR2-667	DDR2-800
2.7 GB/s	3.2 GB/s	3.2 GB/s	4.266 GB/s	5.33 GB/s	6.4 GB/s

DDR2 On Die Termination

- **ODT – On Die Termination**
 - Built into the controller and SDRAM
 - Offers multiple termination values for different configurations
 - 50 Ohm, 75 Ohm, 150 Ohm
 - Turns on or off depending on Read/Write cycle



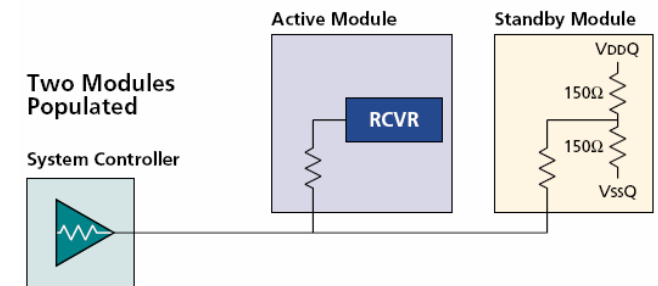
* Courtesy of Micron

DDR2 On Die Termination

■ How ODT works – Example of a 2 module system

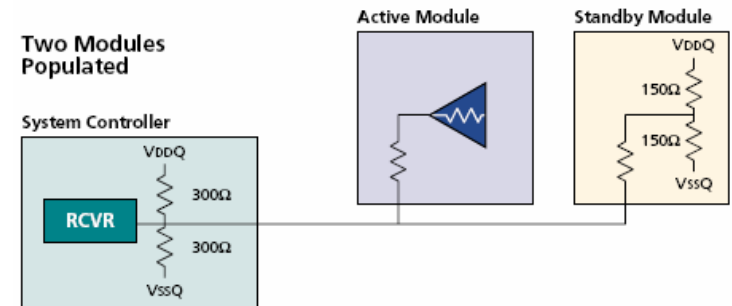
— Write operation

- ODT off at Controller
- DIMM receiving data has ODT of 150 Ohms
- DIMM not receiving data has ODT of 75 Ohms



— Read operation

- ODT off at driving DIMM
- ODT 150 Ohms at Controller
- DIMM not driving has ODT of 75 Ohms

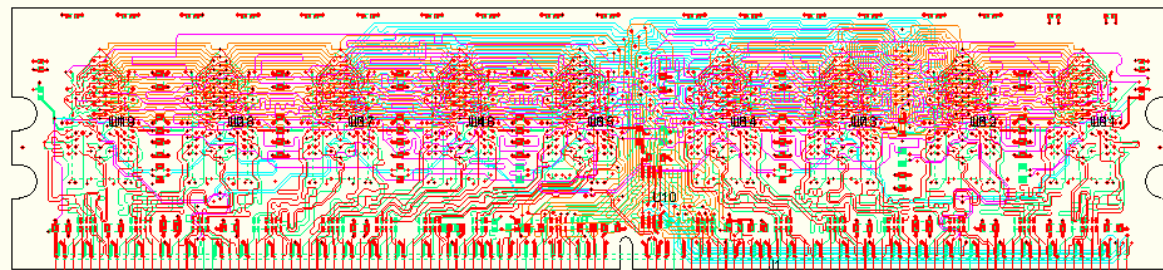


* Courtesy of Micron

DDR2 DIMM Technology



- Same as DDR, DIMMs come in many configurations
 - x4, x8, x16 SDRAM devices
 - 1, 2 or 4 Rank (or Bank) DIMMs
 - Registered or Unbuffered Address/CMD signals
 - Non-ECC (x64 bits) or ECC (x72 bits)
 - Parity or no Parity for Address signals
 - Stacked or un-Stacked components
- DIMM layout is controlled by JEDEC
 - Many manufacturers shared responsibility of creating the DIMM layout data



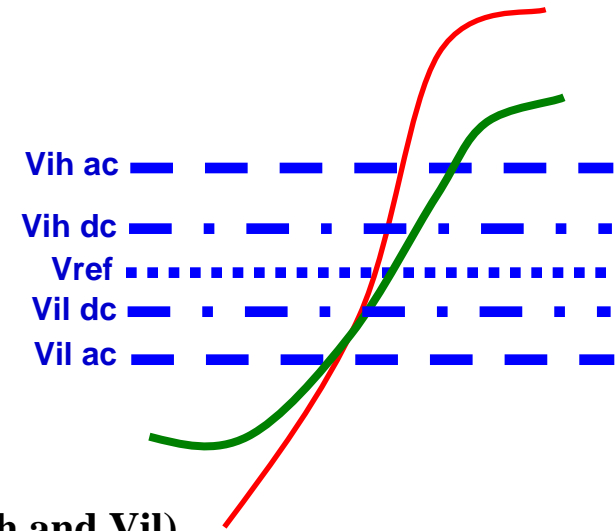
DDR2 Electrical Characteristics

- **DDR2 uses SSTL18 buffer technology**

- **1.8V technology**
- **Class I drivers for point to point connection – Half drive strength**
- **Class II drivers for multi-drop connection – Full drive strength**

- **Some important voltages to remember**

- **Vref = 900 mV**
 - Used for setting up switching thresholds (Vih and Vil)
- **Vih/Vil AC Thresholds**
 - = Vref +/- 250 mV for DDR2-400 & 533
 - = Vref +/- 200 mV for DDR2-667 & 800
- **Vih/Vil DC Thresholds**
 - = Vref +/- 125 mV for all DDR2

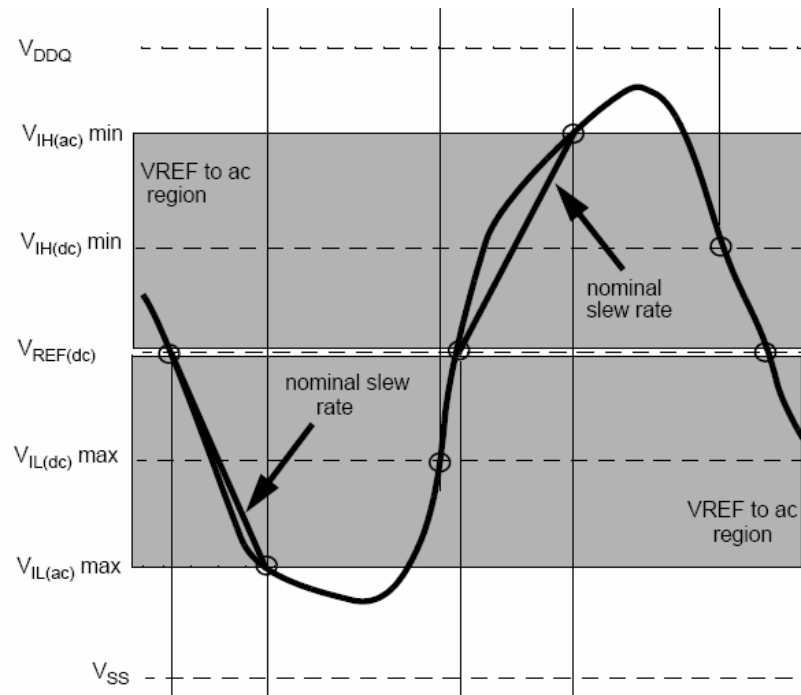


DDR2 Timing Characteristics

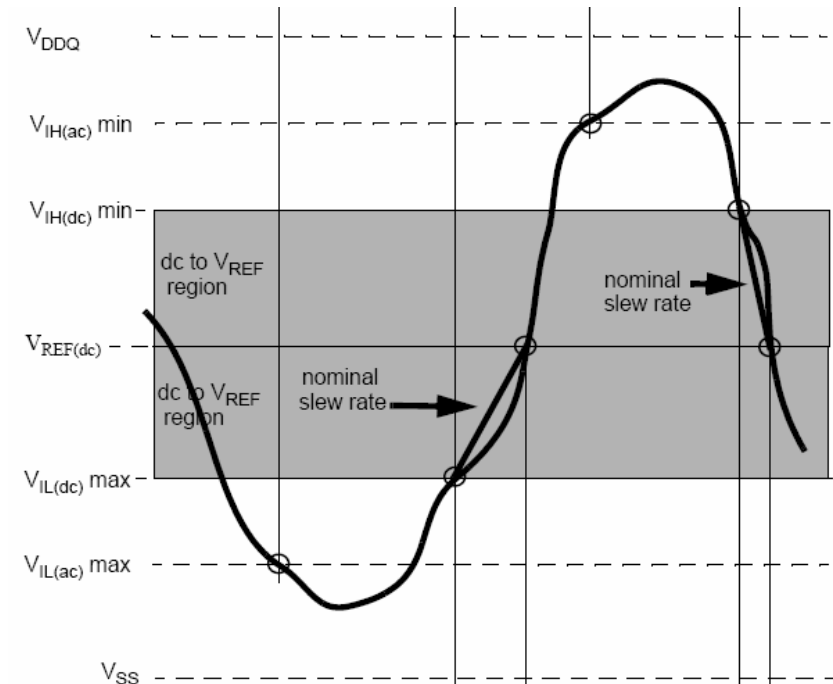
- Signal derating required to meet setup and hold times

- Find nominal slew rate

- Setup



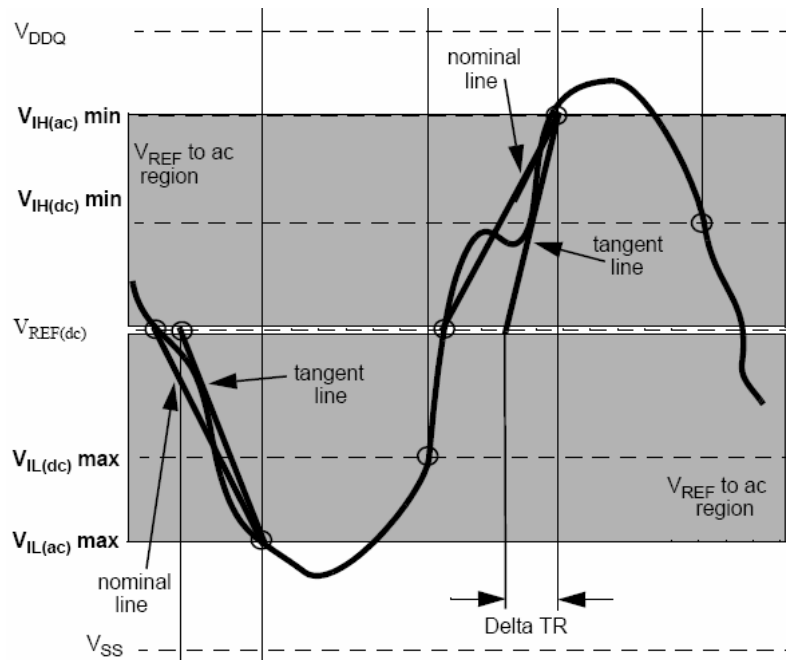
- Hold



DDR2 Timing Characteristics

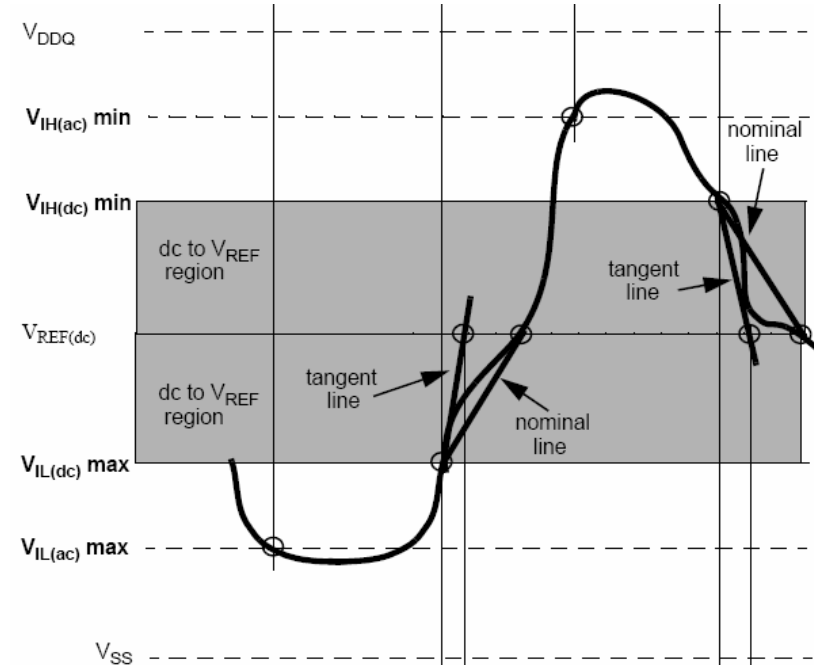
■ Setup

- If any of the signal falls to the right of the nominal slew rate in the switching region, signal must be derated



■ Hold

- If any of the signal falls to the left of the nominal slew rate in the switching region, signal must be derated



DDR2 Timing Characteristics

■ Setup slew rate measurement

— Rising Edge

- Last crossing of $V_{ref} + \text{DC Guard-band}$ to first crossing of V_{ih-ac}

— Falling Edge

- Last crossing of $V_{ref} - \text{DC Guard-band}$ to first crossing of V_{il-ac}

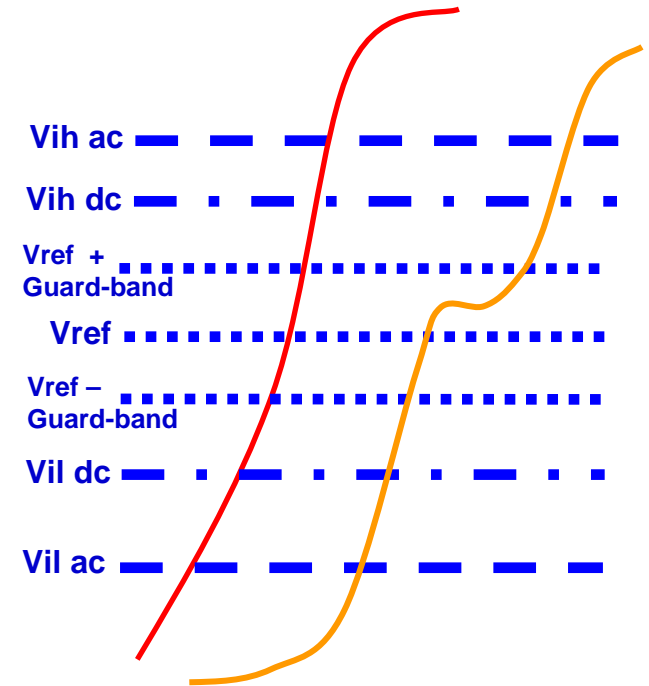
■ Hold slew rate measurement

— Rising Edge

- First crossing of V_{il-dc} to the first crossing of $V_{ref} - \text{AC Guard-band}$

— Falling Edge

- First crossing of V_{ih-dc} to the first crossing of $V_{ref} + \text{AC Guard-band}$



DDR2 Timing Characteristics

- Derate or Prorate setup and hold times based on slew rate information

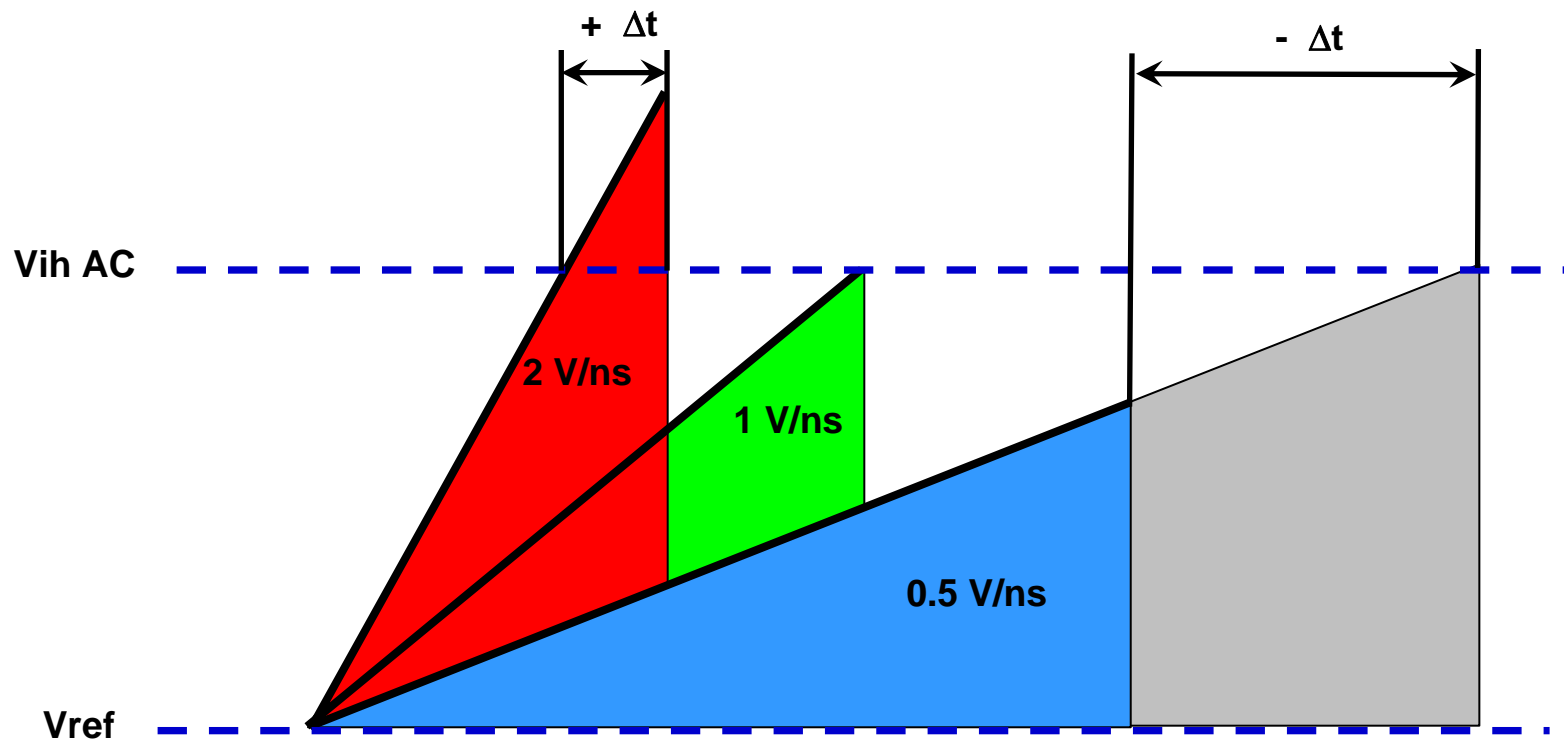
Table 45 — Derating values for DDR2-400, DDR2-533.

		tIS, tIH Derating Values for DDR2-400, DDR2-533							
		CK,CK Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	Units	Notes
Com- mand/Ad- dress Slew rate (V/ns)	4.0	+187	+94	+217	+124	+247	+154	ps	1
	3.5	+179	+89	+209	+119	+239	+149	ps	1
	3.0	+167	+83	+197	+113	+227	+143	ps	1
	2.5	+150	+75	+180	+105	+210	+135	ps	1
	2.0	+125	+45	+155	+75	+185	+105	ps	1
	1.5	+83	+21	+113	+51	+143	+81	ps	1
	1.0	0	0	+30	+30	+60	60	ps	1
	0.9	-11	-14	+19	+16	+49	+46	ps	1
	0.8	-25	-31	+5	-1	+35	+29	ps	1
	0.7	-43	-54	-13	-24	+17	+6	ps	1
	0.6	-67	-83	-37	-53	-7	-23	ps	1
	0.5	-110	-125	-80	-95	-50	-65	ps	1
	0.4	-175	-188	-145	-158	-115	-128	ps	1
	0.3	-285	-292	-255	-262	-225	-232	ps	1
	0.25	-350	-375	-320	-345	-290	-315	ps	1
	0.2	-525	-500	-495	-470	-465	-440	ps	1
	0.15	-800	-708	-770	-678	-740	-648	ps	1
	0.1	-1450	-1125	-1420	-1095	-1390	-1065	ps	1

DDR2 Timing Characteristics

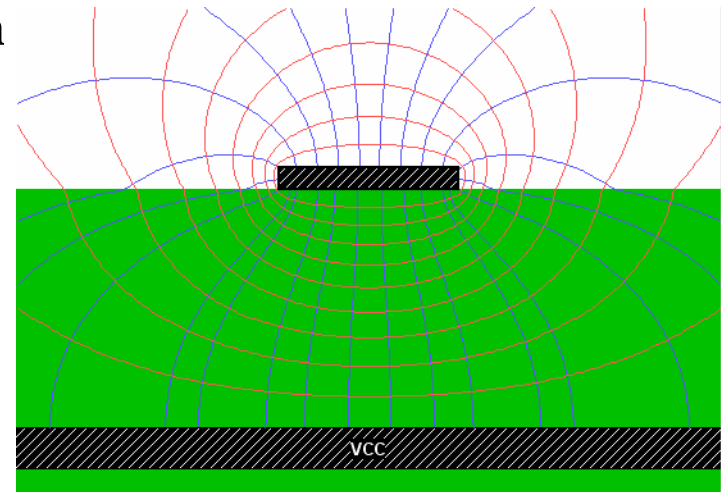
■ Why Derating?

- Consider the area under the curve – Charge Model concept



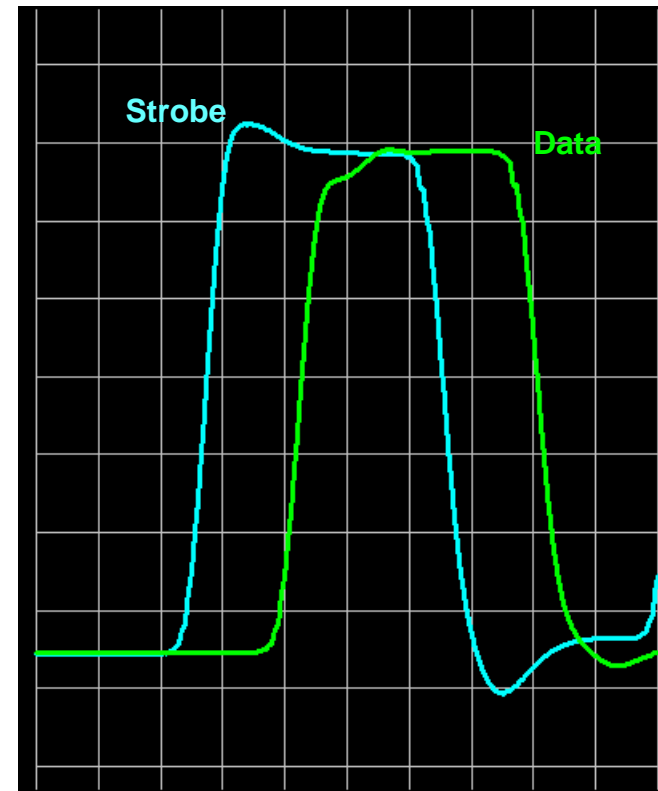
DDR2 Impedance Characteristics

- Recommended impedance of 50 ohms
 - Different than DDR
 - 60 Ohm recommended impedance in DDR
 - Slew rate issues don't exist since spec limit was increased from 4 V/ns in DDR to 5 V/ns in DDR2
 - Simulate with different impedance values to determine the best solution



HyperLynx DDR2 Technology Kit

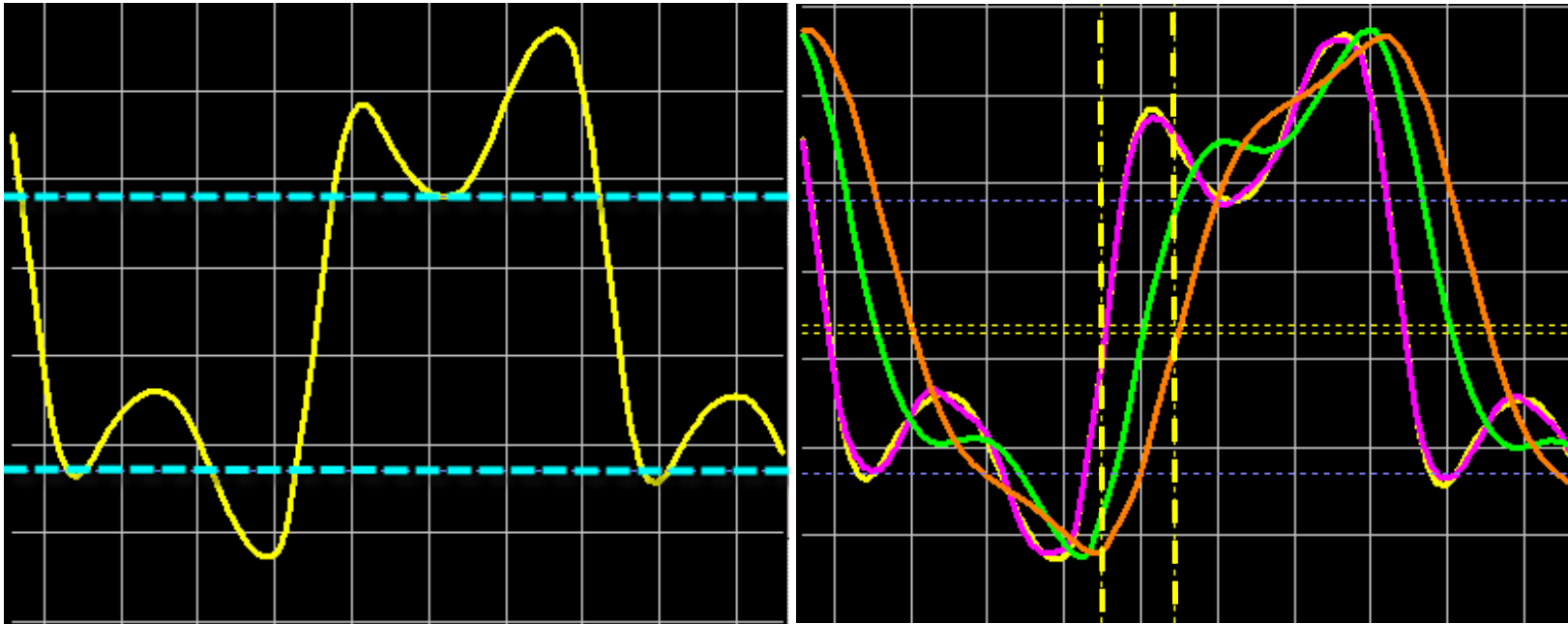
1. Introduction
2. DDR/DDR2 Overview
3. **Design Challenges**
4. Simulation
5. Design Guidelines



DDR/DDR2 Design Challenges

Reflections and Skew

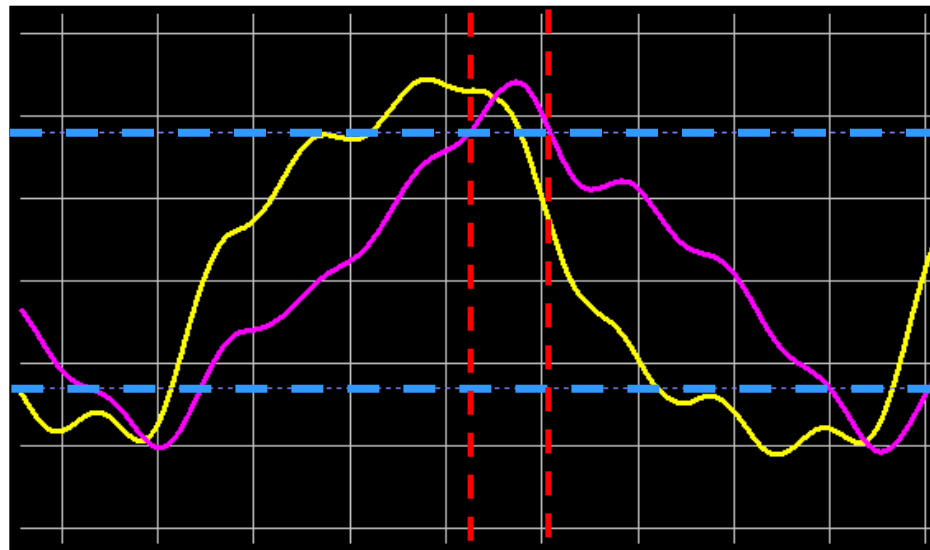
- Reflections seen on signal edges
- Skew between DQ bits consuming timing budget



DDR/DDR2 Design Challenges

Address timing

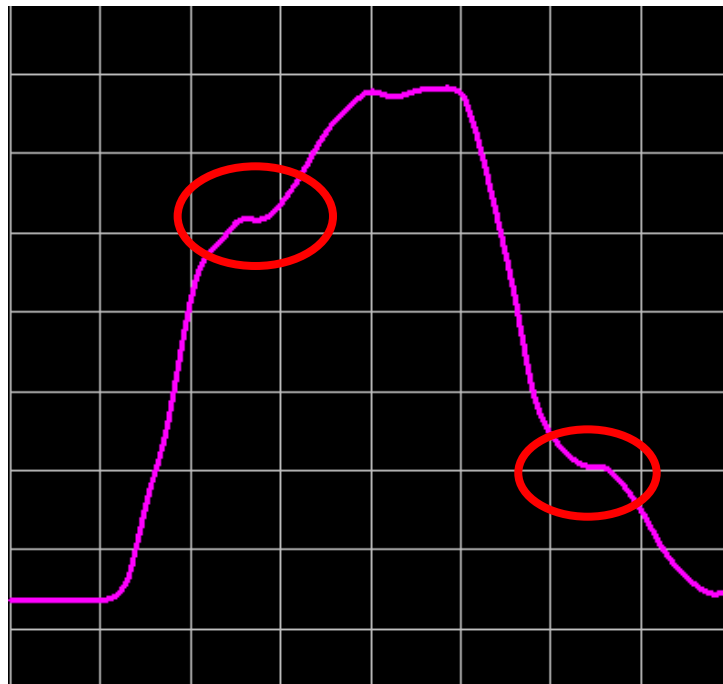
- Very little timing budget for Address/Control signals under heavily loaded conditions



DDR/DDR2 Design Challenges

Crosstalk

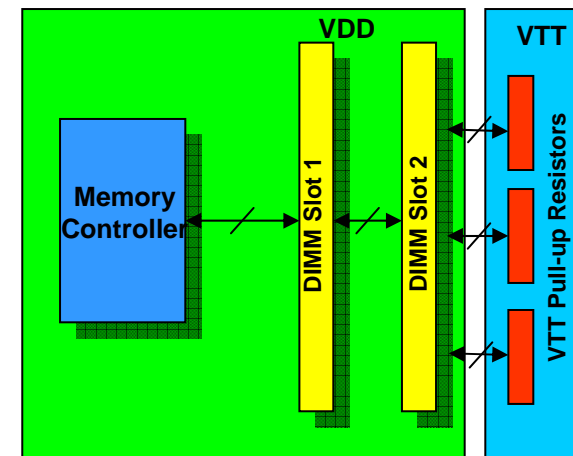
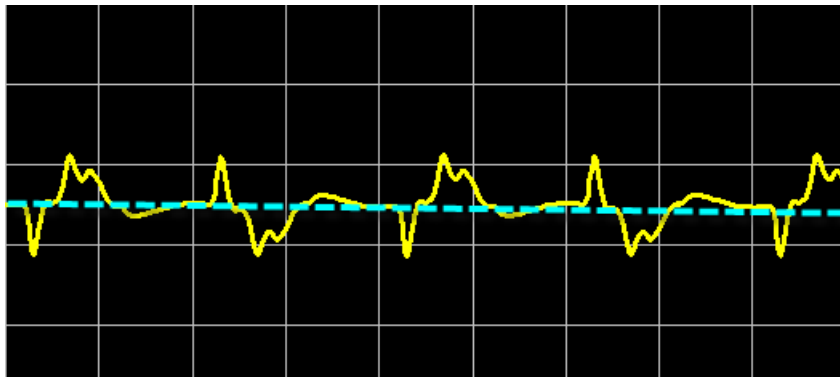
- **Crosstalk on Strobe Signals**
 - Often seen as “glitches” on the strobe edges
 - Can cause double clocking



DDR2 Design Challenges

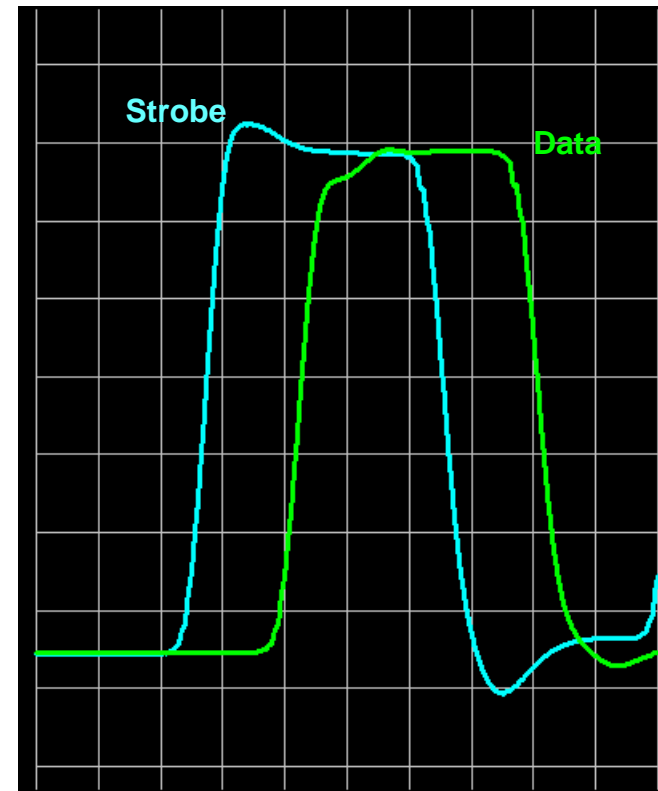
Power Plane Stability

- **Vref and VDD Stability**
 - SSO can cause fluctuations in Vref due to inadequate decoupling
 - Causes the Vref level to shift which changes the Vih and Vil switching thresholds



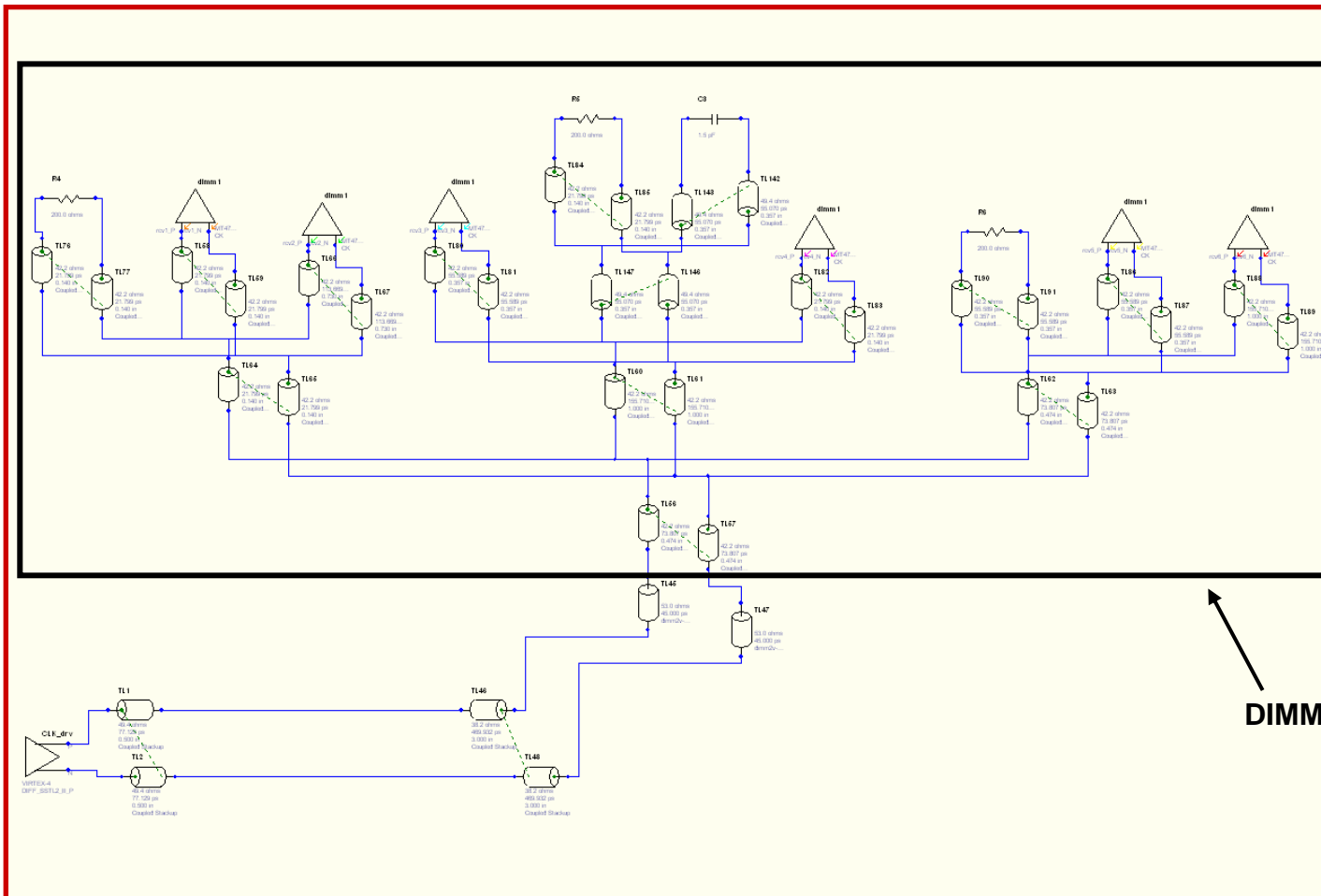
HyperLynx DDR2 Technology Kit

1. Introduction
2. DDR/DDR2 Overview
3. Design Challenges
4. **Simulation**
5. Design Guidelines



DDR2 Simulation

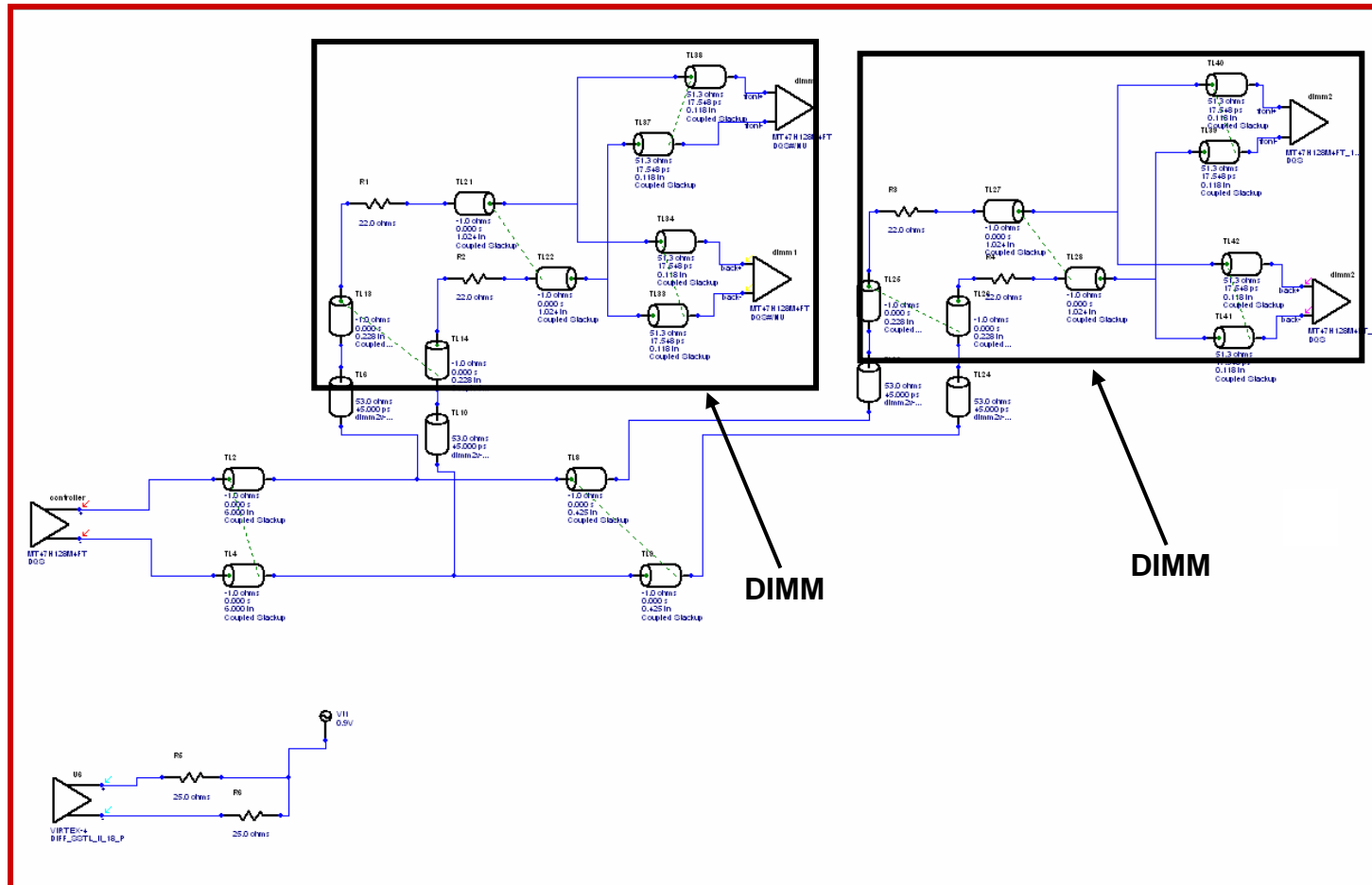
Clock Topology – LineSim



DIMM

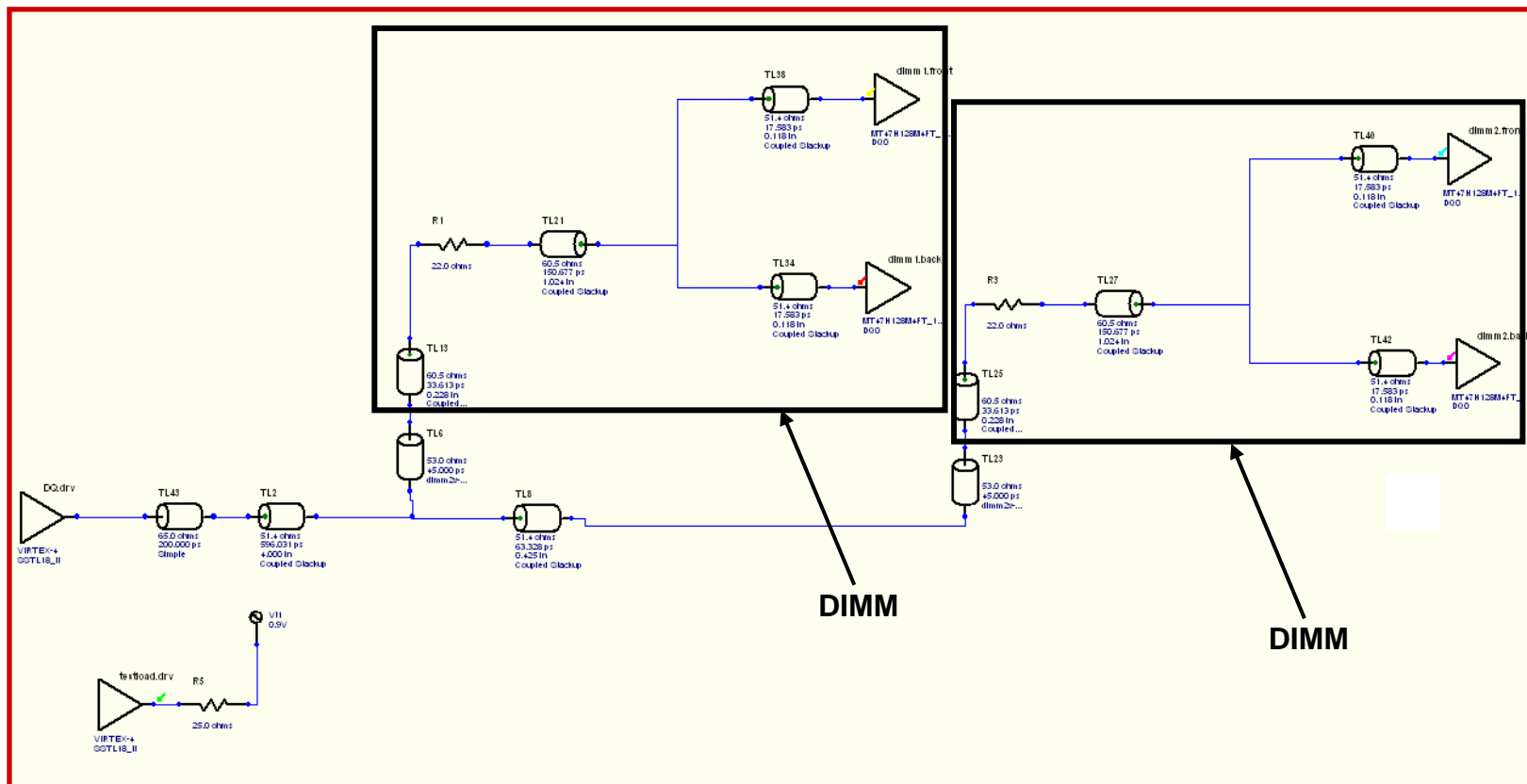
DDR2 Simulation

Differential DQS Topology – LineSim



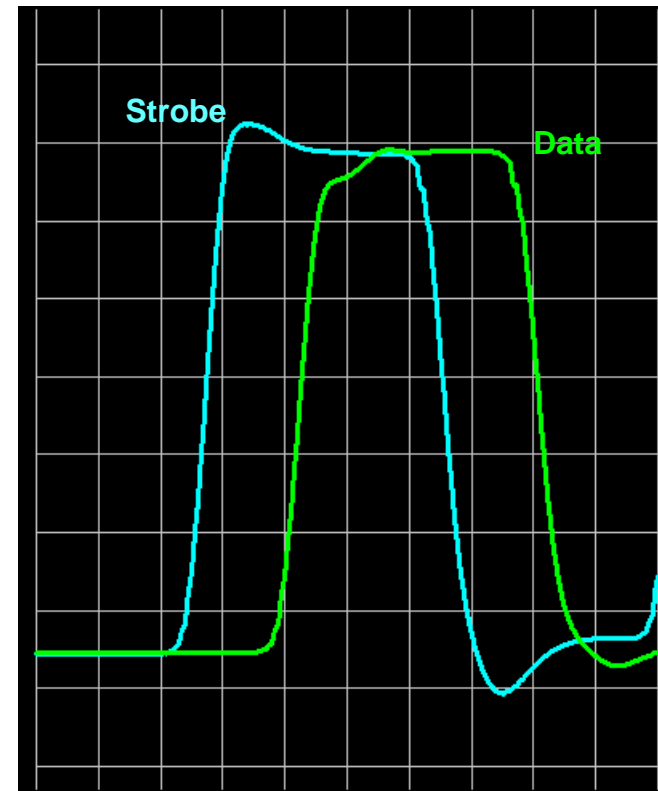
DDR2 Simulation

DQ Topology – LineSim



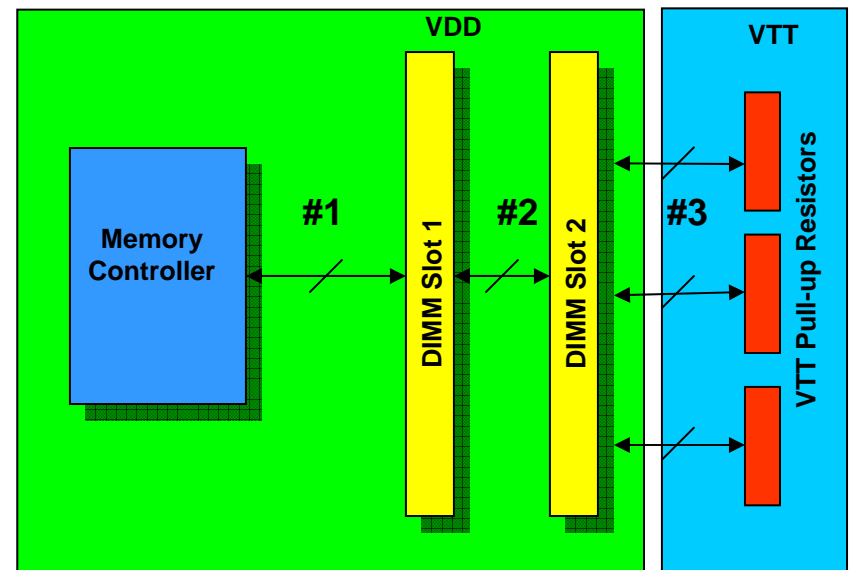
HyperLynx DDR2 Technology Kit

1. Introduction
2. DDR Overview
3. DDR2 Overview
4. Design Challenges
5. Simulation
6. **Design Guidelines**



DDR2 Design Guidelines

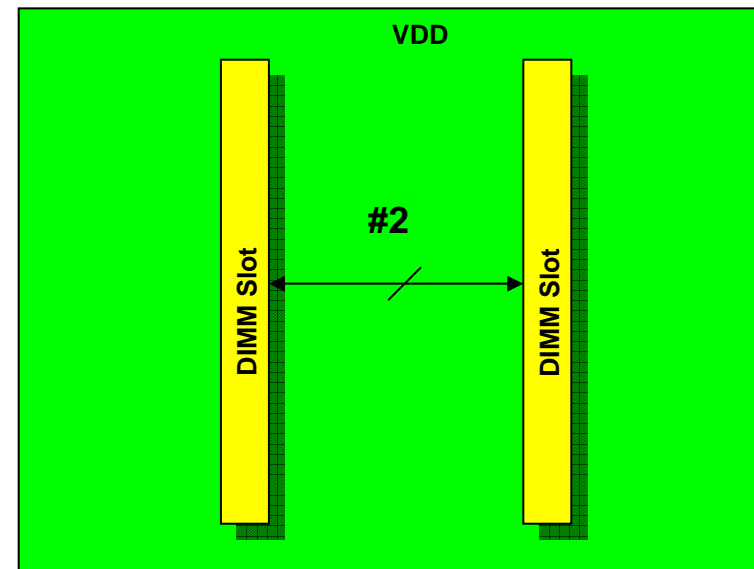
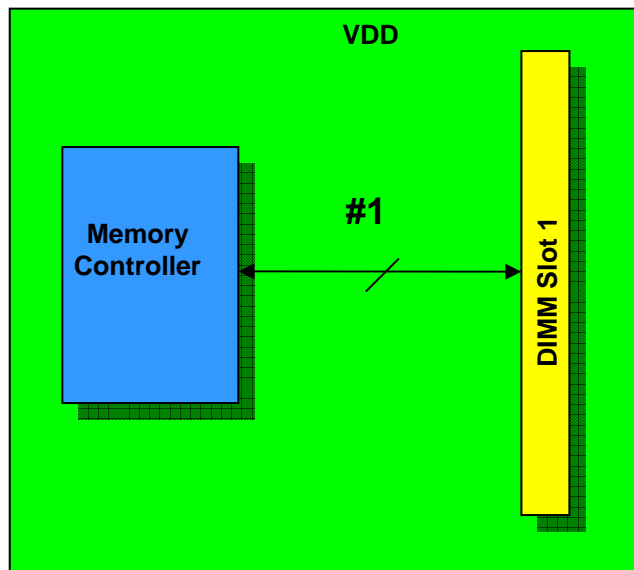
- **What results are important**
 - **We need to constrain 4 critical lengths**
 1. Net length from the controller to the 1st DIMM slot
 2. Net length between DIMM slots
 3. Net length from last slot to the pull-up termination (only Address/Command)
 4. All DQS/DQ groups should be length matched to minimize skew within the group and across the channel



DDR2 Design Guidelines

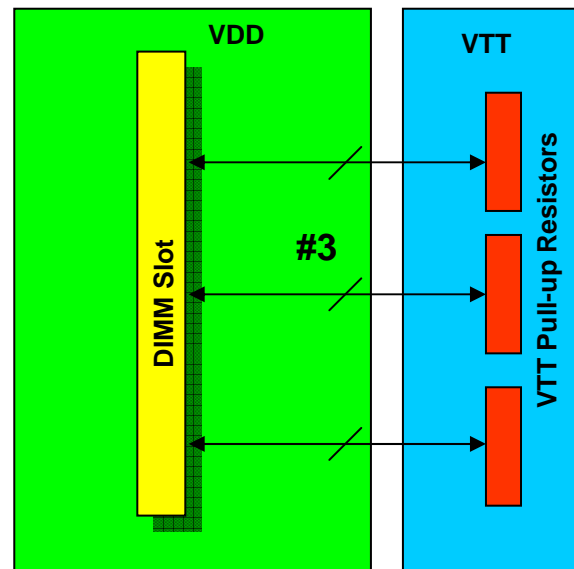
■ What results are important

- #1 This length from the controller to the first DIMM is typically between 1.9” and 4.5”
- #2 The length between the DIMMs is typically around 425 mils



DDR2 Design Guidelines

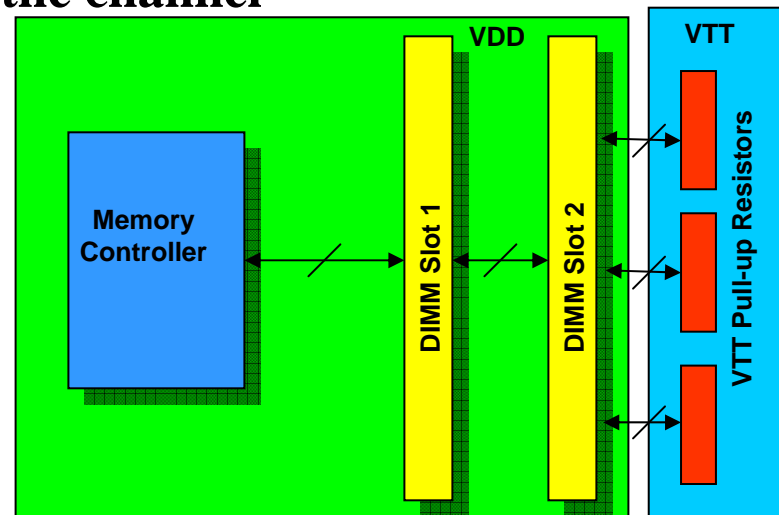
- **What results are important**
 - **#3 The length from the last DIMM to the pull-up resistors is typically 200 mils to 550 mils**
 - Only applies to the Address and Command nets – Data nets use ODT
 - No timing importance here



DDR2 Design Guidelines

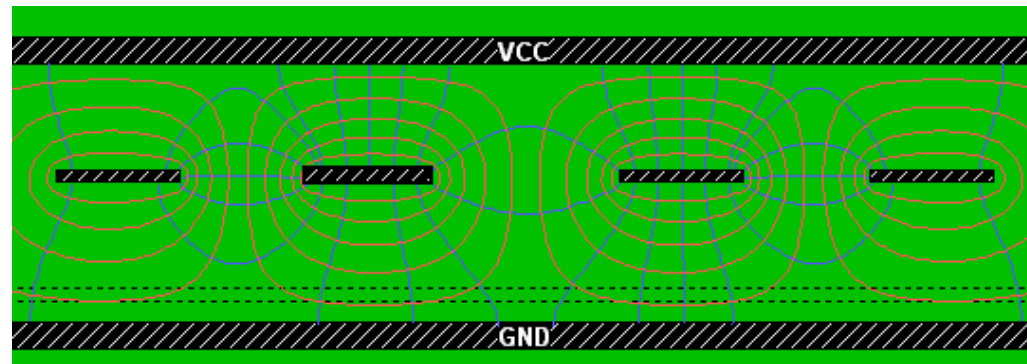
■ What results are important

- #4 This constraint is very **critical**.
- A data group (DQ) has an associated strobe (DQS);
- This group should be length matched to each other with minimum skew
- Typical constraints are about 50 mils within the group
 - Try to spread this out across the channel
 - +/- 30 mils for length #1
 - +/- 20 mils for length #2
 - Overall skew between byte lanes should be +/- 500 mils
 - Skew between address nets should be +/- 200 mils



DDR2 Design Guidelines

- **Spacing Recommendations**
 - Varies depending on stackup
 - Typically rules of thumb say $3H$ spacing
 - For a 5 mil dielectric this would be 15 mils
 - For signals coupled closely to reference planes, often $1.5H$ can be used or ~8 mils



HyperLynx Design Kits

<http://www.mentor.com/hyperlynx/customer/examples/>

HyperLynx Design Kits - Microsoft Internet Explorer

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HyperLynx Design Kits: v7.5 or Newer

Design Kit	Description	Download/ReadMe
DDR	The HyperLynx DDR technology kit enables hardware engineers to quickly develop a DDR memory subsystem solution space, making tradeoffs between termination, minimum and maximum routing constraints, and DIMM loading in order to meet the signal integrity and timing requirements in the JEDEC DDR specification (www.jedec.org).	DDR.zip (2,678 KB)
PCI/PCI-X	The Personal Computer Interface (PCI and PCI-X) represents the most prolific I/O standard for the transfer of data between a CPU and its peripherals (www.pcisig.com), with common applications that include Video, SCSI, Fibre Channel, and Ethernet adaptors, as well as Modems, and other bridge applications. With speeds ranging from 66 to 533 MHz, PCI-X technology is used not	PCI-X.zip (1,984 KB)

PCB SYSTEMS

- AccuSim/Continuum
- Analog Designer
- AutoTherm
- Board Station
- Data Management
- Design Capture
- Design/Board Architect
- Design Flow Management
- DesignView
- Destiny RE
- DxDesigner
- eProduct Designer
- Expedition PCB
- Falcon Framework
- Geom Genie
- HyperLynx
- I/O Designer
- ICX
- Library Management System (LMS)

SUPPORTNET RESOURCES

- Open Service Request
- Contact Support
- Community
- About 5 STAR Support
- Environment Support
- All Downloads
- All System Configurations
- All Documentation
- Self-Paced Learning

HYPERLYNX SUPPORT RESOURCES

- Downloads
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- Product Documentation
- TechNotes
- AppNotes
- Design Kits
- Self-Paced Learning
- Forums

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Presentation Date	Topics
	+
23-Aug	IBIS Model Validation & Verification
6-Sep	Differential Signaling: Simulating Skew Sensitivity & Noise Rejection
13-Sep	Controlling Crosstalk in High-Speed PCB Design
20-Sep	SATA - Successful Serial ATA Design
4-Oct	Controlling Emissions, EMI, EMC
18-Oct	PCI Express Interconnect Design
1-Nov	DDR2 Design Dos and Don'ts
15-Nov	Timing is Everything in Common Clock Designs
29-Nov	Technology, Topology, & Termination: Fundamentals of High-Speed Design
13-Dec	SERDES Design Made Easy

The background is a vibrant blue with a complex pattern of white lines and shapes. These include a grid of dots connected by lines, resembling a circuit board or a network diagram. There are also several overlapping, semi-transparent rectangular frames and circular patterns, some of which contain binary code (0s and 1s). The overall aesthetic is high-tech and digital.

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