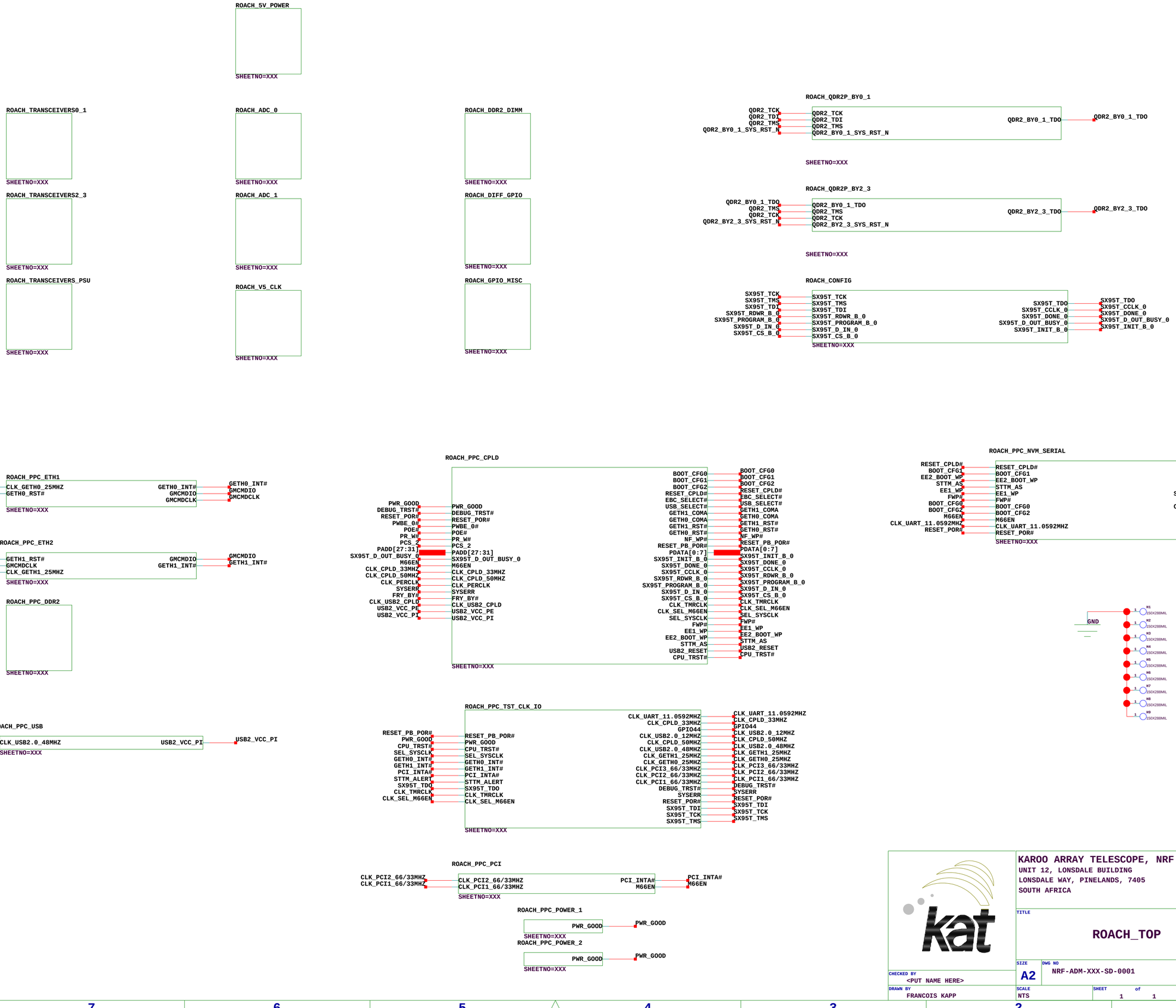


KAROO ARRAY TELESCOPE, NRF
UNIT 12, LONSDALE BUILDING
LONSDALE WAY, PINELANDS, 7405
SOUTH AFRICA

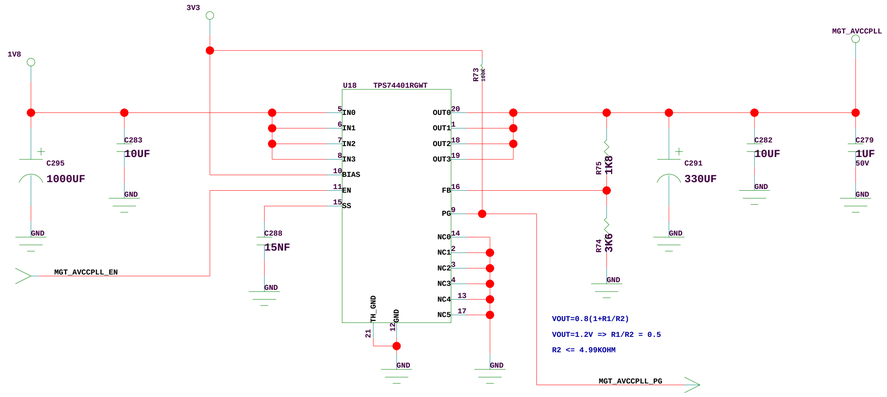
TITLE: ROACH_TOP

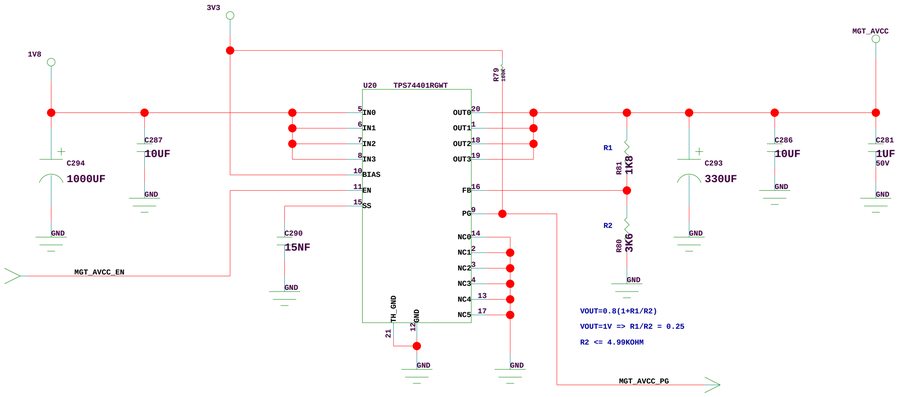
CHECKED BY: <PUT NAME HERE>	SIZE: A2	DWG NO: NRF-ADM-XXX-SD-0001
DRAWN BY: FRANCOIS KAPP	SCALE: NTS	SHEET 1 of 1

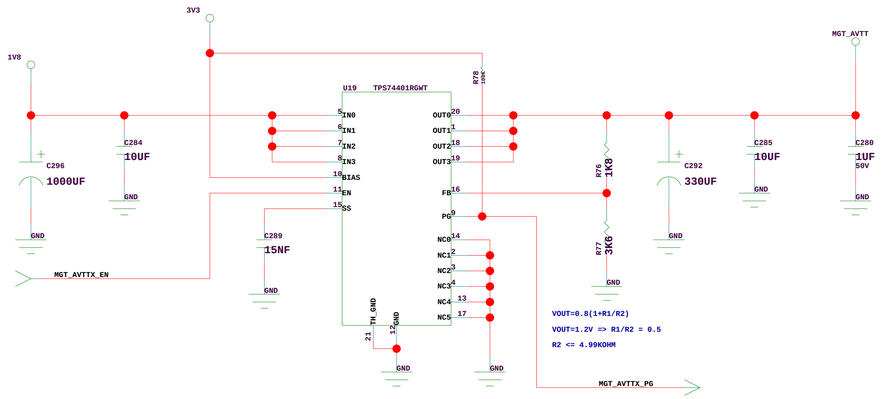
REV: A

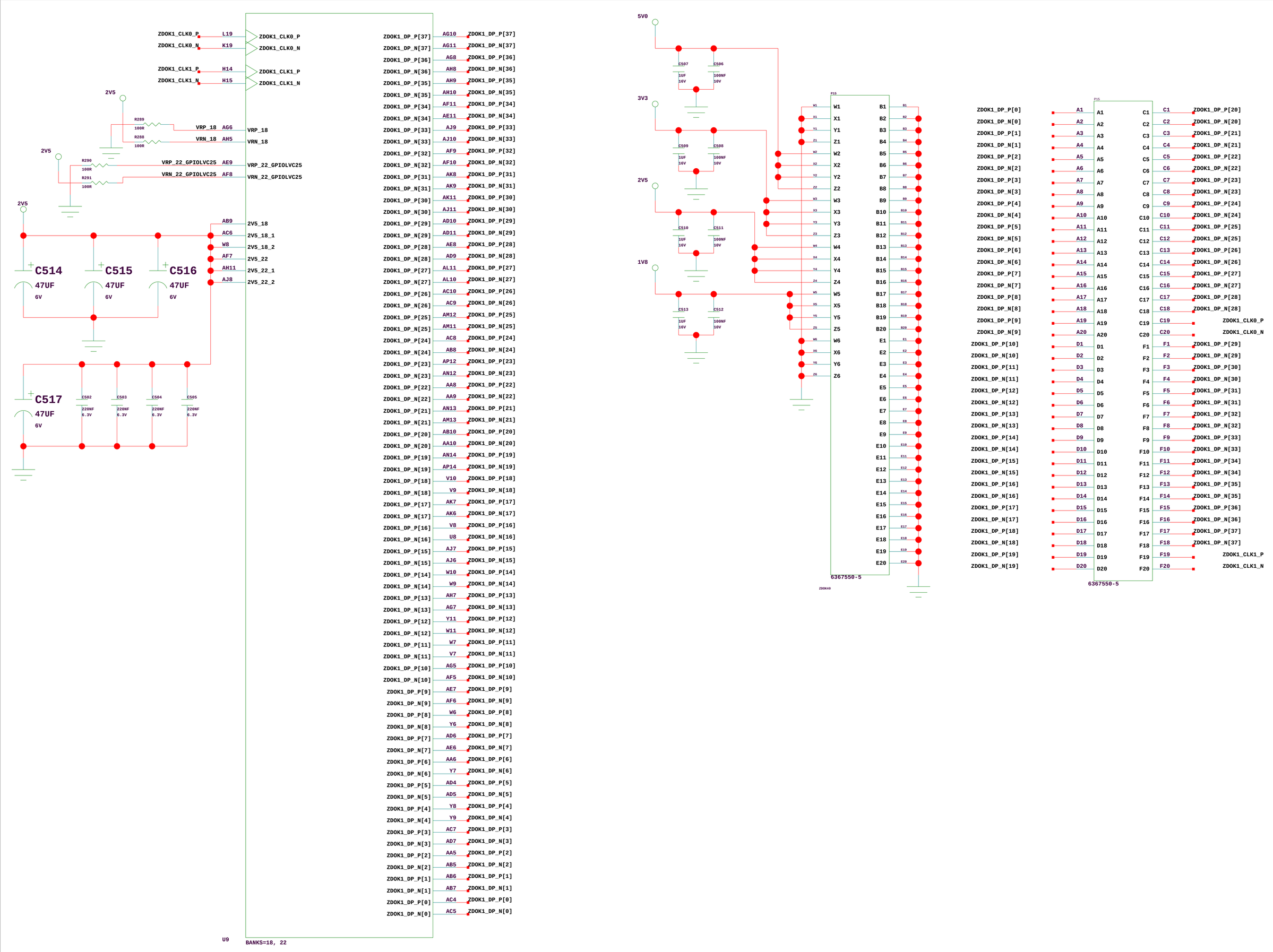
9-20-2007_11:16

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
2V5
FB1 220@100M
FB2 220@100M
FB3 220@100M
FB4 220@100M
FB26 220@100M
C234 220NF 6.3V
C233 220NF 6.3V
C232 220NF 6.3V
C231 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
C276 220NF 6.3V
R68 10K
X1
DE
VCC
OUT
GND
JP4
CCLD-023-25-156.250
156.25MHZ
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
C243 10NF 25V
C244 10NF 25V
C245 10NF 25V
C246 10NF 25V
C248 10NF 25V
C247 10NF 25V
C250 10NF 25V
C251 10NF 25V
C252 10NF 25V
MGTAVCC_112 R3
MGTAVCC_112_1 R4
MGTAVCCPLL_112 T3
MGTAVTTRX_112 N3
MGT_112_REF_CLK_P P4
MGT_112_REF_CLK_N P3
MGTRX0_112_P N1
MGTRX0_112_N P1
MGTRX1_112_P T1
MGTRX1_112_N R1
MGTAVCC_112
MGTAVCC_112_1
MGTAVCCPLL_112
MGTAVTTRX_112
MGT_112_REF_CLK_P
MGT_112_REF_CLK_N
MGTRX0_112_P
MGTRX0_112_N
MGTRX1_112_P
MGTRX1_112_N
U9
MGTRREF V4
MGT_VTRXC V5
MGTAVTTTX_112 M3
MGTAVTTTX_112_1 U3
MGTTX0_112_P M2
MGTTX0_112_N N2
MGTTX1_112_P U2
MGTTX1_112_N T2
MGTRREF
MGTAVTTRXC
MGTAVTTTX_112
MGTAVTTTX_112_1
MGTTX0_112_P
MGTTX0_112_N
MGTTX1_112_P
MGTTX1_112_N
R67 49.9R
MGT_AVTT
FB25 220@100M
FB5 220@100M
FB6 220@100M
C265 220NF 6.3V
C236 220NF 6.3V
C235 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
P6
S1 DL0P
S2 DL0N
S3 DL1P
S4 DL1N
S5 DL2P
S6 DL2N
S7 DL3P
S8 DL3N
S10 SL0P
S15 SL0N
S14 SL1P
S13 SL1N
S12 SL2P
S11 SL2N
S16 SL3P
S9 SL3N
MGTRX0_114_P
MGTRX0_114_N
MGTRX1_114_P
MGTRX1_114_N
SIG_GND1 G1
SIG_GND2 G2
SIG_GND3 G3
SIG_GND4 G4
SIG_GND5 G5
SIG_GND6 G6
SIG_GND7 G7
SIG_GND8 G8
SIG_GND9 G9
SIG_GND10 G19
ODIS
FAULT
FCN-268F036-G/3DB
3V3
R61 10K
OPTICAL MODULE FAULT - RED LED
JP2
C269 10NF 6.3V
C270 10NF 6.3V
R69 5K1
R58 3K9
R60 6K8
R59 3K9
C266 10NF 6.3V
U15
U14
MAX9032AKA
U16
AND2
SN74AHC1G08DCKR
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB11 220@100M
FB12 220@100M
FB9 220@100M
FB10 220@100M
C242 220NF 6.3V
C241 220NF 6.3V
C240 220NF 6.3V
C239 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_114 AA3
MGTAVCC_114_1 AA4
MGTAVCCPLL_114 AB3
MGTAVTTRX_114 W3
MGT_114_REF_CLK_P NC Y4
MGT_114_REF_CLK_N NC Y3
MGTRX0_114_P W1
MGTRX0_114_N Y1
MGTRX1_114_P AB1
MGTRX1_114_N AA1
MGTAVCC_114
MGTAVCC_114_1
MGTAVCCPLL_114
MGTAVTTRX_114
MGT_114_REF_CLK_P
MGT_114_REF_CLK_N
MGTRX0_114_P
MGTRX0_114_N
MGTRX1_114_P
MGTRX1_114_N
U9
MGTAVTTTX_114 AC3
MGTAVTTTX_114_1 V3
MGTTX0_114_P V2
MGTTX0_114_N W2
MGTTX1_114_P AC2
MGTTX1_114_N AB2
MGTAVTTTX_114
MGTAVTTTX_114_1
MGTTX0_114_P
MGTTX0_114_N
MGTTX1_114_P
MGTTX1_114_N
MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT
FB8 220@100M
FB7 220@100M
C237 220NF 6.3V
C238 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
U12
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
TPS2031D
R71 10K
C268 10NF 6.3V
C267 100NF 6.3V
C277 4.7UF 16V
C229 22UF 16V
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB17 220@100M
FB18 220@100M
FB15 220@100M
FB16 220@100M
C259 220NF 6.3V
C258 220NF 6.3V
C257 220NF 6.3V
C254 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
C249 10NF 25V
C250 10NF 25V
C251 10NF 25V
C252 10NF 25V
MGTAVCC_116 J3
MGTAVCC_116_1 J4
MGTAVCCPLL_116 K3
MGTAVTTRX_116 G3
MGT_116_REF_CLK_P NC H4
MGT_116_REF_CLK_N NC H3
MGTRX0_116_P G1
MGTRX0_116_N H1
MGTRX1_116_P K1
MGTRX1_116_N J1
MGTAVCC_116
MGTAVCC_116_1
MGTAVCCPLL_116
MGTAVTTRX_116
MGT_116_REF_CLK_P
MGT_116_REF_CLK_N
MGTRX0_116_P
MGTRX0_116_N
MGTRX1_116_P
MGTRX1_116_N
U9
MGTAVTTTX_116_1 L3
MGTAVTTTX_116 F3
MGTTX0_116_P F2
MGTTX0_116_N G2
MGTTX1_116_P L2
MGTTX1_116_N K2
MGTAVTTTX_116_1
MGTAVTTTX_116
MGTTX0_116_P
MGTTX0_116_N
MGTTX1_116_P
MGTTX1_116_N
FB14 220@100M
FB13 220@100M
C255 220NF 6.3V
C256 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
P6
S19 DL0P
S20 DL0N
S21 DL1P
S22 DL1N
S23 DL2P
S24 DL2N
S25 DL3P
S26 DL3N
S34 SL0P
S33 SL0N
S32 SL1P
S31 SL1N
S30 SL2P
S29 SL2N
S28 SL3P
S27 SL3N
MGTRX0_116_P
MGTRX0_116_N
MGTRX1_116_P
MGTRX1_116_N
SIG_GND1 G10
SIG_GND2 G11
SIG_GND3 G12
SIG_GND4 G13
SIG_GND5 G14
SIG_GND6 G15
SIG_GND7 G16
SIG_GND8 G17
SIG_GND9 G18
SIG_GND10 G19
ODIS
FAULT
FCN-268F036-G/3DB
3V3
R64 10K
OPTICAL MODULE FAULT - RED LED
JP3
C273 10NF 6.3V
C271 10NF 6.3V
R70 5K1
R65 3K9
R66 6K8
R67 3K9
C272 10NF 6.3V
U15
U14
MAX9032AKA
U17
AND2
SN74AHC1G08DCKR
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB22 220@100M
FB21 220@100M
FB24 220@100M
FB23 220@100M
C262 220NF 6.3V
C263 220NF 6.3V
C253 220NF 6.3V
C264 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_118 AG3
MGTAVCC_118_1 AG4
MGTAVCCPLL_118 AH3
MGTAVTTRX_118 AE3
MGT_118_REF_CLK_P NC AF4
MGT_118_REF_CLK_N NC AF3
MGTRX0_118_P AE1
MGTRX0_118_N AF1
MGTRX1_118_P AH1
MGTRX1_118_N AG1
MGTAVCC_118
MGTAVCC_118_1
MGTAVCCPLL_118
MGTAVTTRX_118
MGT_118_REF_CLK_P
MGT_118_REF_CLK_N
MGTRX0_118_P
MGTRX0_118_N
MGTRX1_118_P
MGTRX1_118_N
U9
MGTAVTTTX_118_1 AJ3
MGTAVTTTX_118 AD3
MGTTX0_118_P AD2
MGTTX0_118_N AE2
MGTTX1_118_P AJ2
MGTTX1_118_N AH2
MGTAVTTTX_118_1
MGTAVTTTX_118
MGTTX0_118_P
MGTTX0_118_N
MGTTX1_118_P
MGTTX1_118_N
FB19 220@100M
FB20 220@100M
C261 220NF 6.3V
C260 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
U13
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
TPS2031D
R72 10K
C274 10NF 6.3V
C275 100NF 6.3V
C278 4.7UF 16V
C230 22UF 16V


3V3
1V8
U18
TPS74401RGWT
R73
10MK
MGT_AVCCPLL
C295
1000UF
C283
10UF
C288
15NF
MGT_AVCCPLL_EN
IN0
IN1
IN2
IN3
BIAS
EN
SS
OUT0
OUT1
OUT2
OUT3
FB
PG
NC0
NC1
NC2
NC3
NC4
NC5
TH_GND
GND
R75
1K8
R74
3K6
C291
330UF
C282
10UF
C279
1UF
50V
VOUT=0.8(1+R1/R2)
VOUT=1.2V => R1/R2 = 0.5
R2 <= 4.99KOHM
MGT_AVCCPLL_PG


3V3
1V8
U20
TPS74401RGWT
R79
10MK
MGT_AVCC
C294
1000UF
C287
10UF
C290
15NF
MGT_AVCC_EN
IN0
IN1
IN2
IN3
BIAS
EN
SS
OUT0
OUT1
OUT2
OUT3
FB
PG
NC0
NC1
NC2
NC3
NC4
NC5
TH_GND
GND
R1
R81
1K8
R2
R80
3K6
C293
330UF
C286
10UF
C281
1UF
50V
VOUT=0.8(1+R1/R2)
VOUT=1V => R1/R2 = 0.25
R2 <= 4.99KOHM
MGT_AVCC_PG


3V3
1V8
U19
TPS74401RGWT
R78
10MK
MGT_AVTT
C296
1000UF
C284
10UF
C289
15NF
MGT_AVTTX_EN
IN0
IN1
IN2
IN3
BIAS
EN
SS
OUT0
OUT1
OUT2
OUT3
FB
PG
NC0
NC1
NC2
NC3
NC4
NC5
TH_GND
GND
R76
1K8
R77
3K6
C292
330UF
C285
10UF
C280
1UF
50V
VOUT=0.8(1+R1/R2)
VOUT=1.2V => R1/R2 = 0.5
R2 <= 4.99KOHM
MGT_AVTTX_PG


ZDOK1_CLK0_P L19 ZDOK1_CLK0_P
ZDOK1_CLK0_N K19 ZDOK1_CLK0_N
ZDOK1_CLK1_P H14 ZDOK1_CLK1_P
ZDOK1_CLK1_N H15 ZDOK1_CLK1_N
2V5
R289 100R VRP_18 AG6 VRP_18
R288 100R VRN_18 AH5 VRN_18
R290 100R VRP_22_GPIOLVC25 AE9 VRP_22_GPIOLVC25
R291 100R VRN_22_GPIOLVC25 AF8 VRN_22_GPIOLVC25
AB9 2V5_18
AC6 2V5_18_1
W8 2V5_18_2
AF7 2V5_22
AH11 2V5_22_1
AJ8 2V5_22_2
C514 47UF 6V
C515 47UF 6V
C516 47UF 6V
C517 47UF 6V
C502 220NF 6.3V
C503 220NF 6.3V
C504 220NF 6.3V
C505 220NF 6.3V
ZDOK1_DP_P[37] AG10 ZDOK1_DP_P[37]
ZDOK1_DP_N[37] AG11 ZDOK1_DP_N[37]
ZDOK1_DP_P[36] AG8 ZDOK1_DP_P[36]
ZDOK1_DP_N[36] AH8 ZDOK1_DP_N[36]
ZDOK1_DP_P[35] AH9 ZDOK1_DP_P[35]
ZDOK1_DP_N[35] AH10 ZDOK1_DP_N[35]
ZDOK1_DP_P[34] AF11 ZDOK1_DP_P[34]
ZDOK1_DP_N[34] AE11 ZDOK1_DP_N[34]
ZDOK1_DP_P[33] AJ9 ZDOK1_DP_P[33]
ZDOK1_DP_N[33] AJ10 ZDOK1_DP_N[33]
ZDOK1_DP_P[32] AF9 ZDOK1_DP_P[32]
ZDOK1_DP_N[32] AF10 ZDOK1_DP_N[32]
ZDOK1_DP_P[31] AK8 ZDOK1_DP_P[31]
ZDOK1_DP_N[31] AK9 ZDOK1_DP_N[31]
ZDOK1_DP_P[30] AK11 ZDOK1_DP_P[30]
ZDOK1_DP_N[30] AJ11 ZDOK1_DP_N[30]
ZDOK1_DP_P[29] AD10 ZDOK1_DP_P[29]
ZDOK1_DP_N[29] AD11 ZDOK1_DP_N[29]
ZDOK1_DP_P[28] AE8 ZDOK1_DP_P[28]
ZDOK1_DP_N[28] AD9 ZDOK1_DP_N[28]
ZDOK1_DP_P[27] AL11 ZDOK1_DP_P[27]
ZDOK1_DP_N[27] AL10 ZDOK1_DP_N[27]
ZDOK1_DP_P[26] AC10 ZDOK1_DP_P[26]
ZDOK1_DP_N[26] AC9 ZDOK1_DP_N[26]
ZDOK1_DP_P[25] AM12 ZDOK1_DP_P[25]
ZDOK1_DP_N[25] AM11 ZDOK1_DP_N[25]
ZDOK1_DP_P[24] AC8 ZDOK1_DP_P[24]
ZDOK1_DP_N[24] AB8 ZDOK1_DP_N[24]
ZDOK1_DP_P[23] AP12 ZDOK1_DP_P[23]
ZDOK1_DP_N[23] AN12 ZDOK1_DP_N[23]
ZDOK1_DP_P[22] AA8 ZDOK1_DP_P[22]
ZDOK1_DP_N[22] AA9 ZDOK1_DP_N[22]
ZDOK1_DP_P[21] AN13 ZDOK1_DP_P[21]
ZDOK1_DP_N[21] AM13 ZDOK1_DP_N[21]
ZDOK1_DP_P[20] AB10 ZDOK1_DP_P[20]
ZDOK1_DP_N[20] AA10 ZDOK1_DP_N[20]
ZDOK1_DP_P[19] AN14 ZDOK1_DP_P[19]
ZDOK1_DP_N[19] AP14 ZDOK1_DP_N[19]
ZDOK1_DP_P[18] V10 ZDOK1_DP_P[18]
ZDOK1_DP_N[18] V9 ZDOK1_DP_N[18]
ZDOK1_DP_P[17] AK7 ZDOK1_DP_P[17]
ZDOK1_DP_N[17] AK6 ZDOK1_DP_N[17]
ZDOK1_DP_P[16] V8 ZDOK1_DP_P[16]
ZDOK1_DP_N[16] U8 ZDOK1_DP_N[16]
ZDOK1_DP_P[15] AJ7 ZDOK1_DP_P[15]
ZDOK1_DP_N[15] AJ6 ZDOK1_DP_N[15]
ZDOK1_DP_P[14] W10 ZDOK1_DP_P[14]
ZDOK1_DP_N[14] W9 ZDOK1_DP_N[14]
ZDOK1_DP_P[13] AH7 ZDOK1_DP_P[13]
ZDOK1_DP_N[13] AG7 ZDOK1_DP_N[13]
ZDOK1_DP_P[12] Y11 ZDOK1_DP_P[12]
ZDOK1_DP_N[12] W11 ZDOK1_DP_N[12]
ZDOK1_DP_P[11] W7 ZDOK1_DP_P[11]
ZDOK1_DP_N[11] V7 ZDOK1_DP_N[11]
ZDOK1_DP_P[10] AG5 ZDOK1_DP_P[10]
ZDOK1_DP_N[10] AF5 ZDOK1_DP_N[10]
ZDOK1_DP_P[9] AE7 ZDOK1_DP_P[9]
ZDOK1_DP_N[9] AF6 ZDOK1_DP_N[9]
ZDOK1_DP_P[8] W6 ZDOK1_DP_P[8]
ZDOK1_DP_N[8] Y6 ZDOK1_DP_N[8]
ZDOK1_DP_P[7] AD6 ZDOK1_DP_P[7]
ZDOK1_DP_N[7] AE6 ZDOK1_DP_N[7]
ZDOK1_DP_P[6] AA6 ZDOK1_DP_P[6]
ZDOK1_DP_N[6] Y7 ZDOK1_DP_N[6]
ZDOK1_DP_P[5] AD4 ZDOK1_DP_P[5]
ZDOK1_DP_N[5] AD5 ZDOK1_DP_N[5]
ZDOK1_DP_P[4] Y8 ZDOK1_DP_P[4]
ZDOK1_DP_N[4] Y9 ZDOK1_DP_N[4]
ZDOK1_DP_P[3] AC7 ZDOK1_DP_P[3]
ZDOK1_DP_N[3] AD7 ZDOK1_DP_N[3]
ZDOK1_DP_P[2] AA5 ZDOK1_DP_P[2]
ZDOK1_DP_N[2] AB5 ZDOK1_DP_N[2]
ZDOK1_DP_P[1] AB6 ZDOK1_DP_P[1]
ZDOK1_DP_N[1] AB7 ZDOK1_DP_N[1]
ZDOK1_DP_P[0] AC4 ZDOK1_DP_P[0]
ZDOK1_DP_N[0] AC5 ZDOK1_DP_N[0]
U9
BANKS=18, 22
5V0
3V3
2V5
1V8
C507 1UF 16V
C506 100NF 10V
C509 1UF 16V
C508 100NF 10V
C510 1UF 16V
C511 100NF 10V
C513 1UF 16V
C512 100NF 10V
P15
W1 X1 Y1 Z1 W2 X2 Y2 Z2 W3 X3 Y3 Z3 W4 X4 Y4 Z4 W5 X5 Y5 Z5 W6 X6 Y6 Z6
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20
E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20
6367550-5
ZDOK40
ZDOK1_DP_P[0] A1 A1 C1 C1 ZDOK1_DP_P[20]
ZDOK1_DP_N[0] A2 A2 C2 C2 ZDOK1_DP_N[20]
ZDOK1_DP_P[1] A3 A3 C3 C3 ZDOK1_DP_P[21]
ZDOK1_DP_N[1] A4 A4 C4 C4 ZDOK1_DP_N[21]
ZDOK1_DP_P[2] A5 A5 C5 C5 ZDOK1_DP_P[22]
ZDOK1_DP_N[2] A6 A6 C6 C6 ZDOK1_DP_N[22]
ZDOK1_DP_P[3] A7 A7 C7 C7 ZDOK1_DP_P[23]
ZDOK1_DP_N[3] A8 A8 C8 C8 ZDOK1_DP_N[23]
ZDOK1_DP_P[4] A9 A9 C9 C9 ZDOK1_DP_P[24]
ZDOK1_DP_N[4] A10 A10 C10 C10 ZDOK1_DP_N[24]
ZDOK1_DP_P[5] A11 A11 C11 C11 ZDOK1_DP_P[25]
ZDOK1_DP_N[5] A12 A12 C12 C12 ZDOK1_DP_N[25]
ZDOK1_DP_P[6] A13 A13 C13 C13 ZDOK1_DP_P[26]
ZDOK1_DP_N[6] A14 A14 C14 C14 ZDOK1_DP_N[26]
ZDOK1_DP_P[7] A15 A15 C15 C15 ZDOK1_DP_P[27]
ZDOK1_DP_N[7] A16 A16 C16 C16 ZDOK1_DP_N[27]
ZDOK1_DP_P[8] A17 A17 C17 C17 ZDOK1_DP_P[28]
ZDOK1_DP_N[8] A18 A18 C18 C18 ZDOK1_DP_N[28]
ZDOK1_DP_P[9] A19 A19 C19 C19 ZDOK1_CLK0_P
ZDOK1_DP_N[9] A20 A20 C20 C20 ZDOK1_CLK0_N
ZDOK1_DP_P[10] D1 D1 F1 F1 ZDOK1_DP_P[29]
ZDOK1_DP_N[10] D2 D2 F2 F2 ZDOK1_DP_N[29]
ZDOK1_DP_P[11] D3 D3 F3 F3 ZDOK1_DP_P[30]
ZDOK1_DP_N[11] D4 D4 F4 F4 ZDOK1_DP_N[30]
ZDOK1_DP_P[12] D5 D5 F5 F5 ZDOK1_DP_P[31]
ZDOK1_DP_N[12] D6 D6 F6 F6 ZDOK1_DP_N[31]
ZDOK1_DP_P[13] D7 D7 F7 F7 ZDOK1_DP_P[32]
ZDOK1_DP_N[13] D8 D8 F8 F8 ZDOK1_DP_N[32]
ZDOK1_DP_P[14] D9 D9 F9 F9 ZDOK1_DP_P[33]
ZDOK1_DP_N[14] D10 D10 F10 F10 ZDOK1_DP_N[33]
ZDOK1_DP_P[15] D11 D11 F11 F11 ZDOK1_DP_P[34]
ZDOK1_DP_N[15] D12 D12 F12 F12 ZDOK1_DP_N[34]
ZDOK1_DP_P[16] D13 D13 F13 F13 ZDOK1_DP_P[35]
ZDOK1_DP_N[16] D14 D14 F14 F14 ZDOK1_DP_N[35]
ZDOK1_DP_P[17] D15 D15 F15 F15 ZDOK1_DP_P[36]
ZDOK1_DP_N[17] D16 D16 F16 F16 ZDOK1_DP_N[36]
ZDOK1_DP_P[18] D17 D17 F17 F17 ZDOK1_DP_P[37]
ZDOK1_DP_N[18] D18 D18 F18 F18 ZDOK1_DP_N[37]
ZDOK1_DP_P[19] D19 D19 F19 F19 ZDOK1_CLK1_P
ZDOK1_DP_N[19] D20 D20 F20 F20 ZDOK1_CLK1_N
6367550-5

1V8

C520 220NF 6.3V
C519 220NF 6.3V
C518 220NF 6.3V
C546 47UF 6V
C547 47UF 6V
C548 47UF 6V
C549 47UF 6V
C550 47UF 6V
C551 47UF 6V
C579 47UF 6V
C580 47UF 6V

GND

5V
1V8

U48
VIN
VLDOIN
VDDQSNS
S3
S5
GND
GND

R299 10K
R298 10K

C564 4U7F 10V
C565 100F 16V
GND
GND

VTT_0V9
VREF_0V9

VTT
VTTSNS
VTTREF

C560 100NF 10V
C566 100F 16V
C567 100F 16V
GND
GND
GND

1V8

AN26 AL22 AK26 AM29 AL32 AJ28 AM31 AE30 AU33 W28 AD29 AA32
1V8_25_2 1V8_25_1 1V8_25 1V8_21_2 1V8_21_1 1V8_21 1V8_17_2 1V8_17_1 1V8_17 1V8_13_2 1V8_13_1 1V8_13

DDR2_A[15] AP22 DDR2_A[15]
DDR2_A[14] AM18 DDR2_A[14]
DDR2_A[13] AN18 DDR2_A[13]
DDR2_A[12] AM22 DDR2_A[12]
DDR2_A[11] AN22 DDR2_A[11]
DDR2_A[10] AP20 DDR2_A[10]
DDR2_A[9] AN20 DDR2_A[9]
DDR2_A[8] AN23 DDR2_A[8]
DDR2_A[7] AD26 DDR2_A[7]
DDR2_A[6] AC24 DDR2_A[6]
DDR2_A[5] AC25 DDR2_A[5]
DDR2_A[4] AE26 DDR2_A[4]
DDR2_A[3] AE27 DDR2_A[3]
DDR2_A[2] AF26 DDR2_A[2]
DDR2_A[1] AF25 DDR2_A[1]
DDR2_A[0] AG27 DDR2_A[0]

DDR2_BA[2] AD29 DDR2_BA[2]
DDR2_BA[1] AE29 DDR2_BA[1]
DDR2_BA[0] AF31 DDR2_BA[0]

DDR2_CS_N_0 AF30 DDR2_CS_N_0
DDR2_CS_N_1 AC30 DDR2_CS_N_1

DDR2_CAS_N AK31 DDR2_CAS_N
DDR2_RAS_N AJ31 DDR2_RAS_N

DDR2_DQS_8 AM26 DDR2_DQS_8
DDR2_DQS_N_8 AL26 DDR2_DQS_N_8
DDR2_DQS_7 AN25 DDR2_DQS_7
DDR2_DQS_N_7 AM25 DDR2_DQS_N_7
DDR2_DQS_6 AK29 DDR2_DQS_6
DDR2_DQS_N_6 AJ29 DDR2_DQS_N_6
DDR2_DQS_5 AK26 DDR2_DQS_5
DDR2_DQS_N_5 AJ27 DDR2_DQS_N_5
DDR2_DQS_4 AB31 DDR2_DQS_4
DDR2_DQS_N_4 AA31 DDR2_DQS_N_4
DDR2_DQS_3 Y28 DDR2_DQS_3
DDR2_DQS_N_3 Y29 DDR2_DQS_N_3
DDR2_DQS_2 AH34 DDR2_DQS_2
DDR2_DQS_N_2 AJ34 DDR2_DQS_N_2
DDR2_DQS_1 AF34 DDR2_DQS_1
DDR2_DQS_N_1 AE34 DDR2_DQS_N_1
DDR2_DQS_0 AF33 DDR2_DQS_0
DDR2_DQS_N_0 AE33 DDR2_DQS_N_0

DDR2_DM[8] AL25 DDR2_DM[8]
DDR2_DM[7] AP26 DDR2_DM[7]
DDR2_DM[6] AH27 DDR2_DM[6]
DDR2_DM[5] AK28 DDR2_DM[5]
DDR2_DM[4] AA29 DDR2_DM[4]
DDR2_DM[3] AB30 DDR2_DM[3]
DDR2_DM[2] AJ32 DDR2_DM[2]
DDR2_DM[1] AK34 DDR2_DM[1]
DDR2_DM[0] AD32 DDR2_DM[0]

DDR2_CK_2_P AH29 DDR2_CK_2_P
DDR2_CK_2_N AG30 DDR2_CK_2_N
DDR2_CK_1_N AE31 DDR2_CK_1_N
DDR2_CK_1_P AD31 DDR2_CK_1_P
DDR2_CK_0_P AD24 DDR2_CK_0_P
DDR2_CK_0_N AE24 DDR2_CK_0_N

DDR2_CKE_2 AK33 DDR2_CKE_2
DDR2_CKE_1 AK32 DDR2_CKE_1
DDR2_CKE_0 AH30 DDR2_CKE_0
DDR2_ODT_1 AE32 DDR2_ODT_1
DDR2_ODT_0 AJ30 DDR2_ODT_0
DDR2_WE_N AF29 DDR2_WE_N
DDR2_ERROR AP19 DDR2_ERROR

1 DDR2_PHY_INIT_DONE AN19 DDR2_PHY_INIT_DONE
TP2
DDR2_RESET_N AP21 DDR2_RESET_N

VRP_13 VRN_13 0V9 0V9_1 0V9_2 0V9_3 0V9_4 0V9_5 0V9_6 0V9_7
BANKS=13, 17, 21, 25

1V8
U9
GND
R292 49.9R
R293 49.9R
AH33 AG33 AD27 AG26 AG31 AA32 AL28 AM23 W30 W32
VREF_0V9

VREF_0V9
C552 10NF 25V
C553 10NF 25V
C554 10NF 25V
C555 10NF 25V
C556 10NF 25V
C557 10NF 25V
C558 10NF 25V
C559 10NF 25V
GND

DDR2_DQ[71] AM21 DDR2_DQ[71] 168 DDR2_DIMM_CB7
DDR2_DQ[70] AM28 DDR2_DQ[70] 167 DDR2_DIMM_CB6
DDR2_DQ[69] AN28 DDR2_DQ[69] 162 DDR2_DIMM_CB5
DDR2_DQ[68] AN27 DDR2_DQ[68] 161 DDR2_DIMM_CB4
DDR2_DQ[67] AP27 DDR2_DQ[67] 49 DDR2_DIMM_CB3
DDR2_DQ[66] AN29 DDR2_DQ[66] 48 DDR2_DIMM_CB2
DDR2_DQ[65] AP29 DDR2_DQ[65] 43 DDR2_DIMM_CB1
DDR2_DQ[64] AM27 DDR2_DQ[64] 42 DDR2_DIMM_CB0
DDR2_DQ[63] AP31 DDR2_DQ[63] 236 DDR2_DIMM_DQ[63]
DDR2_DQ[62] AP30 DDR2_DQ[62] 235 DDR2_DIMM_DQ[62]
DDR2_DQ[61] AM30 DDR2_DQ[61] 230 DDR2_DIMM_DQ[61]
DDR2_DQ[60] AN30 DDR2_DQ[60] 229 DDR2_DIMM_DQ[60]
DDR2_DQ[59] AL31 DDR2_DQ[59] 117 DDR2_DIMM_DQ[59]
DDR2_DQ[58] AM31 DDR2_DQ[58] 116 DDR2_DIMM_DQ[58]
DDR2_DQ[57] AL30 DDR2_DQ[57] 111 DDR2_DIMM_DQ[57]
DDR2_DQ[56] AL29 DDR2_DQ[56] 110 DDR2_DIMM_DQ[56]
DDR2_DQ[55] AF24 DDR2_DQ[55] 227 DDR2_DIMM_DQ[55]
DDR2_DQ[54] AF28 DDR2_DQ[54] 226 DDR2_DIMM_DQ[54]
DDR2_DQ[53] AE28 DDR2_DQ[53] 218 DDR2_DIMM_DQ[53]
DDR2_DQ[52] AH28 DDR2_DQ[52] 217 DDR2_DIMM_DQ[52]
DDR2_DQ[51] AG28 DDR2_DQ[51] 108 DDR2_DIMM_DQ[51]
DDR2_DQ[50] AA28 DDR2_DQ[50] 107 DDR2_DIMM_DQ[50]
DDR2_DQ[49] AB28 DDR2_DQ[49] 99 DDR2_DIMM_DQ[49]
DDR2_DQ[48] AC28 DDR2_DQ[48] 98 DDR2_DIMM_DQ[48]
DDR2_DQ[47] AB26 DDR2_DQ[47] 215 DDR2_DIMM_DQ[47]
DDR2_DQ[46] AB25 DDR2_DQ[46] 214 DDR2_DIMM_DQ[46]
DDR2_DQ[45] AA24 DDR2_DQ[45] 209 DDR2_DIMM_DQ[45]
DDR2_DQ[44] Y24 DDR2_DQ[44] 208 DDR2_DIMM_DQ[44]
DDR2_DQ[43] AC27 DDR2_DQ[43] 96 DDR2_DIMM_DQ[43]
DDR2_DQ[42] AB27 DDR2_DQ[42] 95 DDR2_DIMM_DQ[42]
DDR2_DQ[41] AA26 DDR2_DQ[41] 90 DDR2_DIMM_DQ[41]
DDR2_DQ[40] AA25 DDR2_DQ[40] 89 DDR2_DIMM_DQ[40]
DDR2_DQ[39] AD30 DDR2_DQ[39] 206 DDR2_DIMM_DQ[39]
DDR2_DQ[38] V29 DDR2_DQ[38] 205 DDR2_DIMM_DQ[38]
DDR2_DQ[37] W29 DDR2_DQ[37] 200 DDR2_DIMM_DQ[37]
DDR2_DQ[36] Y31 DDR2_DQ[36] 199 DDR2_DIMM_DQ[36]
DDR2_DQ[35] W31 DDR2_DQ[35] 87 DDR2_DIMM_DQ[35]
DDR2_DQ[34] V27 DDR2_DQ[34] 86 DDR2_DIMM_DQ[34]
DDR2_DQ[33] V28 DDR2_DQ[33] 81 DDR2_DIMM_DQ[33]
DDR2_DQ[32] V30 DDR2_DQ[32] 80 DDR2_DIMM_DQ[32]
DDR2_DQ[31] W27 DDR2_DQ[31] 159 DDR2_DIMM_DQ[31]
DDR2_DQ[30] Y27 DDR2_DQ[30] 158 DDR2_DIMM_DQ[30]
DDR2_DQ[29] W25 DDR2_DQ[29] 153 DDR2_DIMM_DQ[29]
DDR2_DQ[28] V25 DDR2_DQ[28] 152 DDR2_DIMM_DQ[28]
DDR2_DQ[27] W26 DDR2_DQ[27] 40 DDR2_DIMM_DQ[27]
DDR2_DQ[26] Y26 DDR2_DQ[26] 39 DDR2_DIMM_DQ[26]
DDR2_DQ[25] V24 DDR2_DQ[25] 34 DDR2_DIMM_DQ[25]
DDR2_DQ[24] W24 DDR2_DQ[24] 33 DDR2_DIMM_DQ[24]
DDR2_DQ[23] AP32 DDR2_DQ[23] 150 DDR2_DIMM_DQ[23]
DDR2_DQ[22] AN32 DDR2_DQ[22] 149 DDR2_DIMM_DQ[22]
DDR2_DQ[21] AN33 DDR2_DQ[21] 144 DDR2_DIMM_DQ[21]
DDR2_DQ[20] AN34 DDR2_DQ[20] 143 DDR2_DIMM_DQ[20]
DDR2_DQ[19] AM32 DDR2_DQ[19] 31 DDR2_DIMM_DQ[19]
DDR2_DQ[18] AM33 DDR2_DQ[18] 30 DDR2_DIMM_DQ[18]
DDR2_DQ[17] AL33 DDR2_DQ[17] 25 DDR2_DIMM_DQ[17]
DDR2_DQ[16] AL34 DDR2_DQ[16] 24 DDR2_DIMM_DQ[16]
DDR2_DQ[15] AG32 DDR2_DQ[15] 141 DDR2_DIMM_DQ[15]
DDR2_DQ[14] AB33 DDR2_DQ[14] 140 DDR2_DIMM_DQ[14]
DDR2_DQ[13] AC33 DDR2_DQ[13] 132 DDR2_DIMM_DQ[13]
DDR2_DQ[12] AB32 DDR2_DQ[12] 131 DDR2_DIMM_DQ[12]
DDR2_DQ[11] AC32 DDR2_DQ[11] 22 DDR2_DIMM_DQ[11]
DDR2_DQ[10] AD34 DDR2_DQ[10] 21 DDR2_DIMM_DQ[10]
DDR2_DQ[9] AC34 DDR2_DQ[9] 13 DDR2_DIMM_DQ[9]
DDR2_DQ[8] Y32 DDR2_DQ[8] 12 DDR2_DIMM_DQ[8]
DDR2_DQ[7] Y34 DDR2_DQ[7] 129 DDR2_DIMM_DQ[7]
DDR2_DQ[6] AA34 DDR2_DQ[6] 128 DDR2_DIMM_DQ[6]
DDR2_DQ[5] AA33 DDR2_DQ[5] 123 DDR2_DIMM_DQ[5]
DDR2_DQ[4] Y33 DDR2_DQ[4] 122 DDR2_DIMM_DQ[4]
DDR2_DQ[3] V34 DDR2_DQ[3] 10 DDR2_DIMM_DQ[3]
DDR2_DQ[2] W34 DDR2_DQ[2] 9 DDR2_DIMM_DQ[2]
DDR2_DQ[1] V33 DDR2_DQ[1] 4 DDR2_DIMM_DQ[1]
DDR2_DQ[0] V32 DDR2_DQ[0] 3 DDR2_DIMM_DQ[0]

1V8
R296 4K7
R297 4K7
DDR2_DIMM_SCL 120 DDR2_SCL
DDR2_DIMM_SDA 119 DDR2_SDA
GND

J9
DDR2_DIMM_A[15] 173 DDR2_A[15]
DDR2_DIMM_A[14] 174 DDR2_A[14]
DDR2_DIMM_A[13] 196 DDR2_A[13]
DDR2_DIMM_A[12] 176 DDR2_A[12]
DDR2_DIMM_A[11] 57 DDR2_A[11]
DDR2_DIMM_A[10] 70 DDR2_A[10]
DDR2_DIMM_A[9] 177 DDR2_A[9]
DDR2_DIMM_A[8] 179 DDR2_A[8]
DDR2_DIMM_A[7] 58 DDR2_A[7]
DDR2_DIMM_A[6] 180 DDR2_A[6]
DDR2_DIMM_A[5] 60 DDR2_A[5]
DDR2_DIMM_A[4] 61 DDR2_A[4]
DDR2_DIMM_A[3] 182 DDR2_A[3]
DDR2_DIMM_A[2] 63 DDR2_A[2]
DDR2_DIMM_A[1] 183 DDR2_A[1]
DDR2_DIMM_A[0] 188 DDR2_A[0]

DDR2_DIMM_BA[2] 54 DDR2_BA[2]
DDR2_DIMM_BA[1] 190 DDR2_BA[1]
DDR2_DIMM_BA[0] 71 DDR2_BA[0]

DDR2_DIMM_CAS# 74 DDR2_CAS_N

DDR2_DIMM_RAS# 192 DDR2_RAS_N

DDR2_DIMM_CK_P[2] 220 DDR2_CK_2_P
DDR2_DIMM_CK_N[2] 221 DDR2_CK_2_N
DDR2_DIMM_CK_P[1] 137 DDR2_CK_1_P
DDR2_DIMM_CK_N[1] 138 DDR2_CK_1_N
DDR2_DIMM_CK_P[0] 185 DDR2_CK_0_P
DDR2_DIMM_CK_N[0] 186 DDR2_CK_0_N

C561 5PF 50V
C562 5PF 50V
C563 5PF 50V

DDR2_DIMM_CKE[1] 171 DDR2_CKE_1
DDR2_DIMM_CKE[0] 52 DDR2_CKE_0

DDR2_DIMM_DM_CB 164 DDR2_DM[8]
DDR2_DIMM_DM[7] 232 DDR2_DM[7]
DDR2_DIMM_DM[6] 223 DDR2_DM[6]
DDR2_DIMM_DM[5] 211 DDR2_DM[5]
DDR2_DIMM_DM[4] 202 DDR2_DM[4]
DDR2_DIMM_DM[3] 155 DDR2_DM[3]
DDR2_DIMM_DM[2] 146 DDR2_DM[2]
DDR2_DIMM_DM[1] 134 DDR2_DM[1]
DDR2_DIMM_DM[0] 125 DDR2_DM[0]

DDR2_DIMM_DQS_CB_P 46 DDR2_DQS_8
DDR2_DIMM_DQS_CB_N 45 DDR2_DQS_N_8
DDR2_DIMM_DQS_P[7] 114 DDR2_DQS_7
DDR2_DIMM_DQS_N[7] 113 DDR2_DQS_N_7
DDR2_DIMM_DQS_P[6] 105 DDR2_DQS_6
DDR2_DIMM_DQS_N[6] 104 DDR2_DQS_N_6
DDR2_DIMM_DQS_P[5] 93 DDR2_DQS_5
DDR2_DIMM_DQS_N[5] 92 DDR2_DQS_N_5
DDR2_DIMM_DQS_P[4] 84 DDR2_DQS_4
DDR2_DIMM_DQS_N[4] 83 DDR2_DQS_N_4
DDR2_DIMM_DQS_P[3] 37 DDR2_DQS_3
DDR2_DIMM_DQS_N[3] 36 DDR2_DQS_N_3
DDR2_DIMM_DQS_P[2] 28 DDR2_DQS_2
DDR2_DIMM_DQS_N[2] 27 DDR2_DQS_N_2
DDR2_DIMM_DQS_P[1] 16 DDR2_DQS_1
DDR2_DIMM_DQS_N[1] 15 DDR2_DQS_N_1
DDR2_DIMM_DQS_P[0] 7 DDR2_DQS_0
DDR2_DIMM_DQS_N[0] 6 DDR2_DQS_N_0

DDR2_DIMM_WE# 73 DDR2_WE_N

DDR2_DIMM_ODT[1] 77 DDR2_ODT_1
DDR2_DIMM_ODT[0] 195 DDR2_ODT_0

R294 49R
R295 49R
GND

DDR2_DIMM_RESET# 18 DDR2_RESET_N

DDR2_DIMM_S#[1] 76 DDR2_CS_N_1
DDR2_DIMM_S#[0] 193 DDR2_CS_N_0

ERR_OUT 55 DDR2_ERROR
PAR_IN 68 PAR_IN
NC

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VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

VTT_0V9

DDR2_A[15]
DDR2_A[14]
DDR2_A[13]
DDR2_A[12]
RP20
CP27
GND

DDR2_A[11]
DDR2_A[10]
DDR2_A[9]
DDR2_A[8]
RP21
CP28
GND

DDR2_A[7]
DDR2_A[6]
DDR2_A[5]
DDR2_A[4]
RP22
CP29
GND

DDR2_A[3]
DDR2_A[2]
DDR2_A[1]
DDR2_A[0]
RP23
CP30
GND

DDR2_BA[2]
DDR2_BA[1]
DDR2_BA[0]
DDR2_CAS_N
RP24
CP31
GND

DDR2_RAS_N
DDR2_WE_N
DDR2_CS_N_1
DDR2_CS_N_0
RP25
CP32
GND

DDR2_CKE_2
DDR2_CKE_1
DDR2_CKE_0
NC
RP26
CP33
GND

J9

237 VSS_64
234 VSS_63
231 VSS_62
228 VSS_61
225 VSS_60
222 VSS_59
219 VSS_58
216 VSS_57
213 VSS_56
210 VSS_55
207 VSS_54
204 VSS_53
201 VSS_52
198 VSS_51
169 VSS_50
166 VSS_49
163 VSS_48
160 VSS_47
157 VSS_46
154 VSS_45
151 VSS_44
148 VSS_43
145 VSS_42
142 VSS_41
139 VSS_40
136 VSS_39
133 VSS_38
130 VSS_37
127 VSS_36
124 VSS_35
121 VSS_34
118 VSS_33
115 VSS_32
112 VSS_31
109 VSS_30
106 VSS_29
103 VSS_28
100 VSS_27
97 VSS_26
94 VSS_25
91 VSS_24
88 VSS_23
85 VSS_22
82 VSS_21
79 VSS_20
66 VSS_19
65 VSS_18
50 VSS_17
47 VSS_16
44 VSS_15
41 VSS_14
38 VSS_13
35 VSS_12
32 VSS_11
29 VSS_10
26 VSS_9
23 VSS_8
20 VSS_7
17 VSS_6
14 VSS_5
11 VSS_4
8 VSS_3
5 VSS_2
2 VSS_1

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VREF_0V9
VREF 1
1V8
VDDSPD 238
1V8
VDD_11 197
VDD_10 189
VDD_9 187
VDD_8 184
VDD_7 178
VDD_6 172
VDD_5 69
VDD_4 67
VDD_3 64
VDD_2 59
VDD_1 53
1V8
VDDQ_11 194
VDDQ_10 191
VDDQ_9 181
VDDQ_8 175
VDDQ_7 170
VDDQ_6 78
VDDQ_5 75
VDDQ_4 72
VDDQ_3 62
VDDQ_2 56
VDDQ_1 51

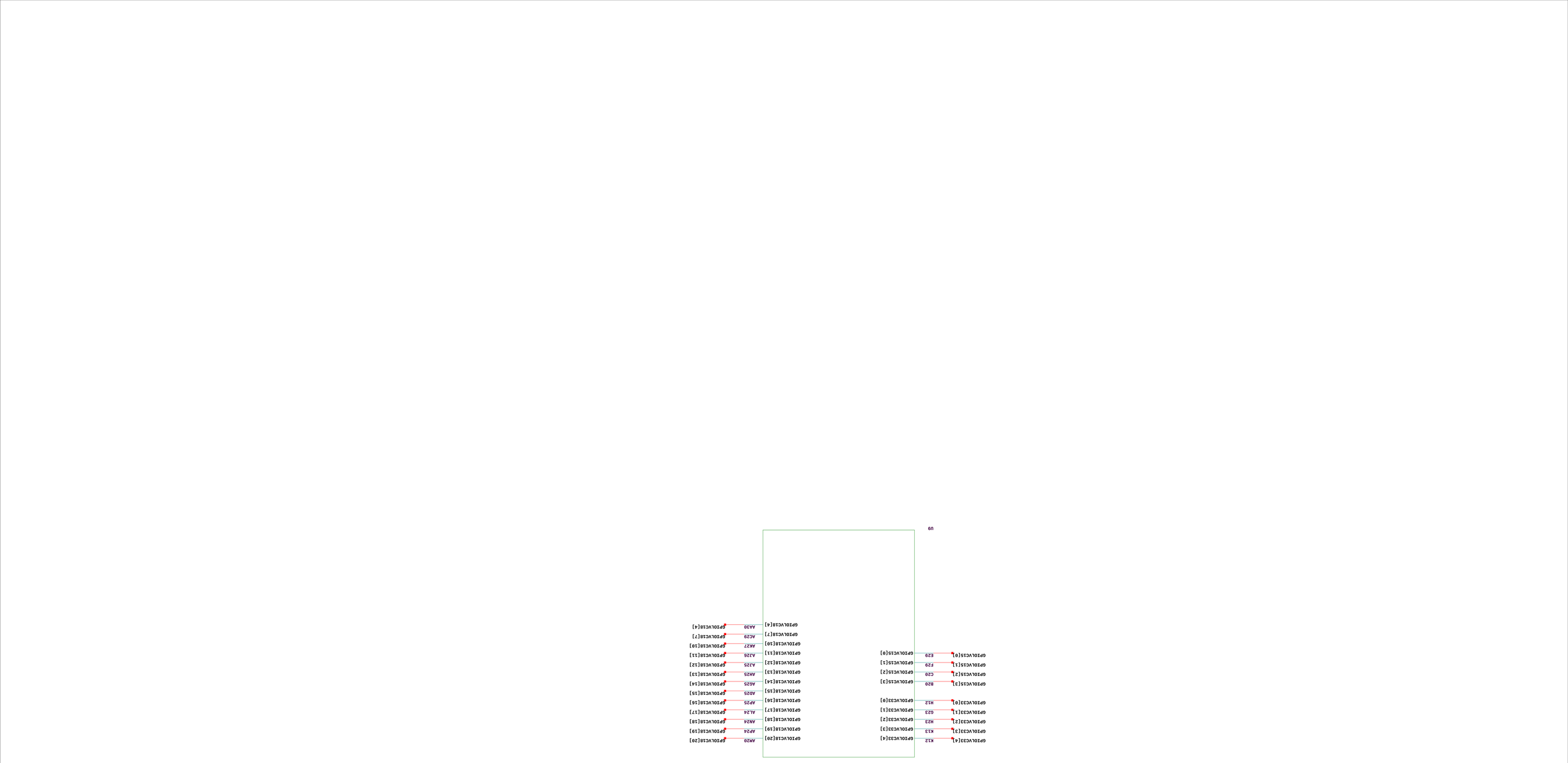
PLACE AT MODULE VREF PIN
VREF_0V9
C521 220NF 6.3V
C527 10NF 25V
GND

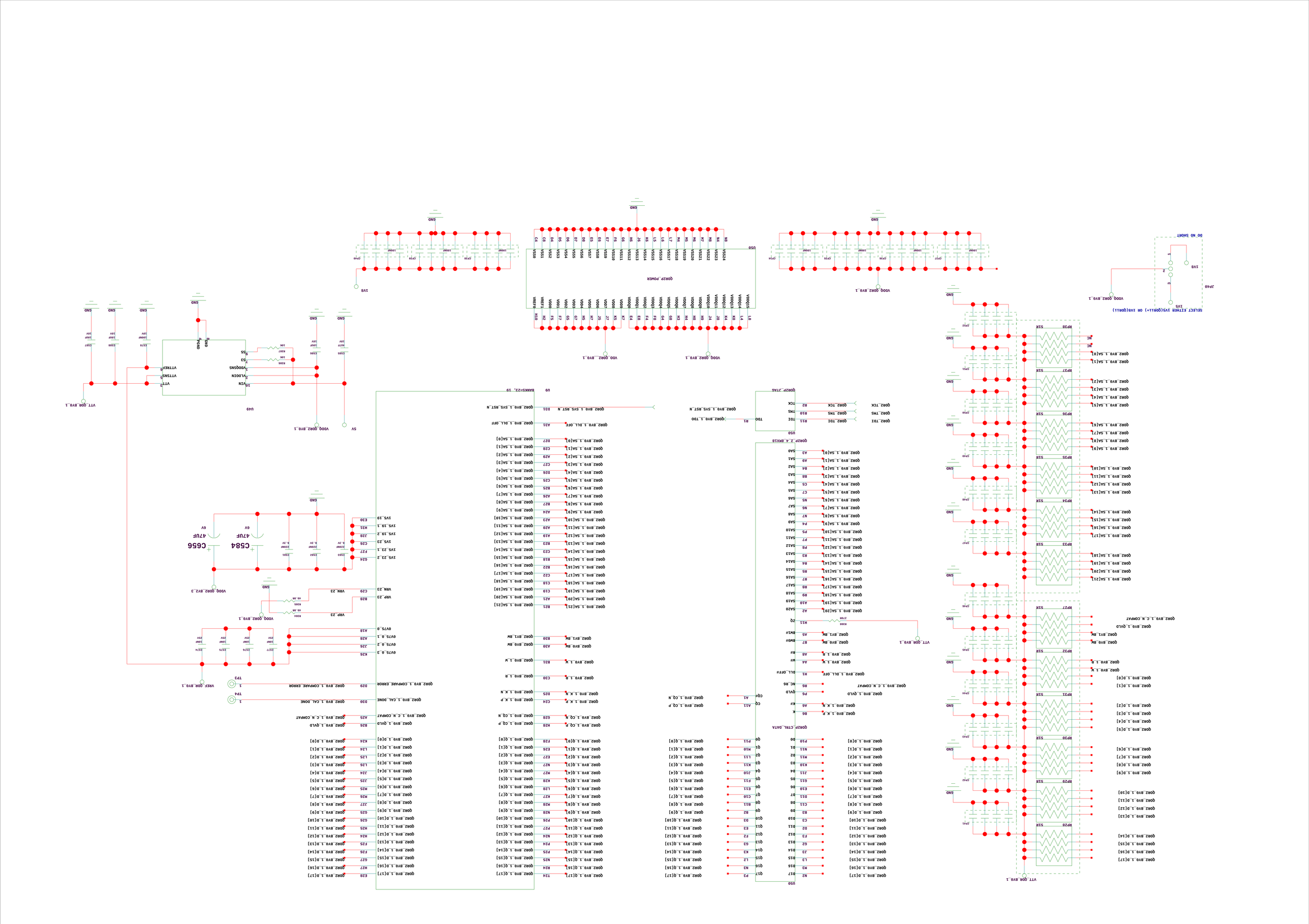
PLACE AT MODULE VDDSPD PIN
1V8
C523 220NF 6.3V
GND

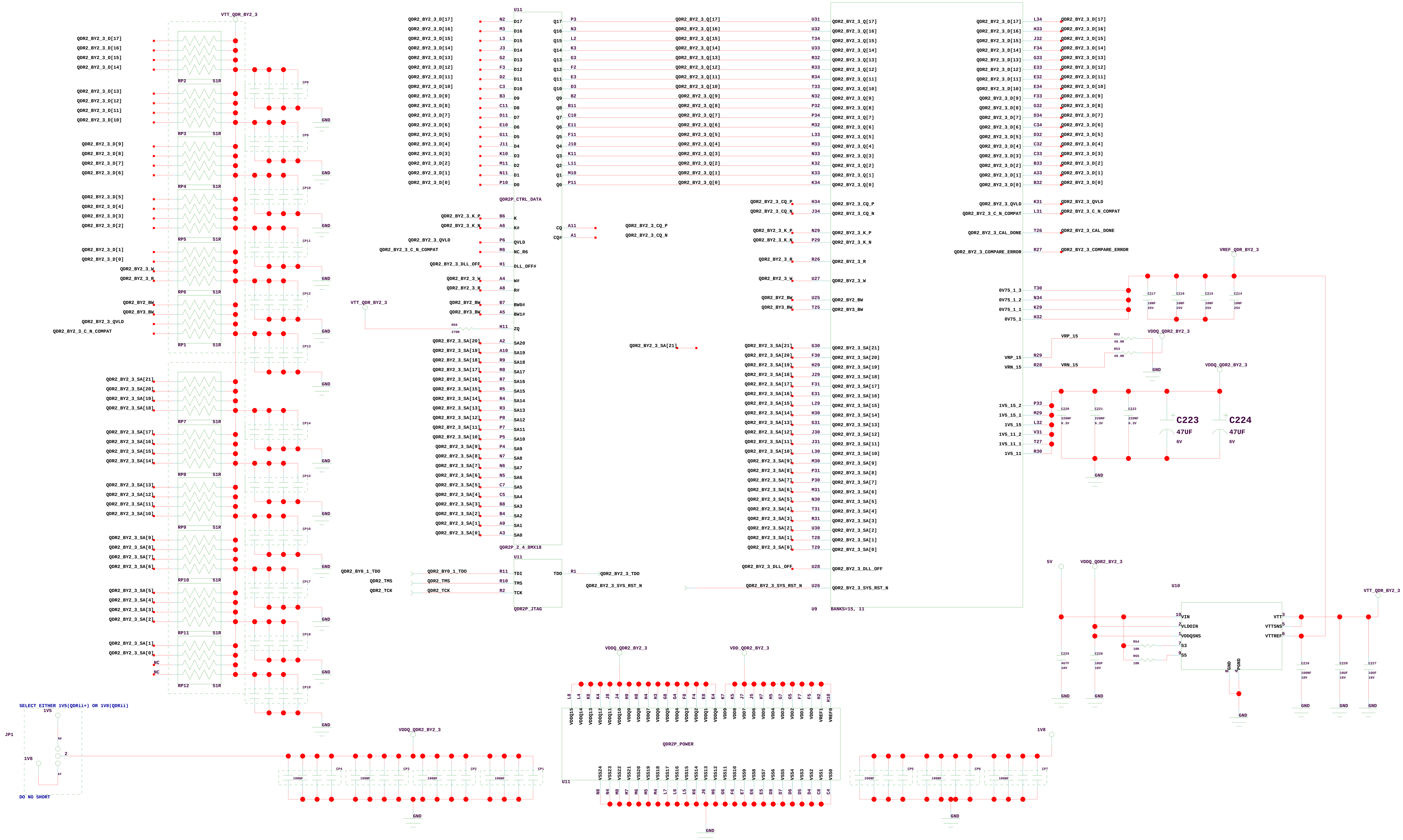
PLACE AT MODULE VDD PINS
1V8
C536 220NF 6.3V
C537 220NF 6.3V
C538 220NF 6.3V
C535 220NF 6.3V
GND
1V8
C540 220NF 6.3V
C541 220NF 6.3V
C542 220NF 6.3V
C539 220NF 6.3V
GND
1V8
C543 220NF 6.3V
C544 220NF 6.3V
C545 220NF 6.3V
GND

1V8
C522 220NF 6.3V
C524 220NF 6.3V
C525 220NF 6.3V
C526 220NF 6.3V
C528 220NF 6.3V
C529 220NF 6.3V
C530 220NF 6.3V
C531 220NF 6.3V
C532 220NF 6.3V
C533 220NF 6.3V
C534 220NF 6.3V
GND

PLACE AT MODULE VDDQ PINS


U9
GPIOLVC33[4]
GPIOLVC33[3]
GPIOLVC33[2]
GPIOLVC33[1]
GPIOLVC33[0]
GPIOLVC18[3]
GPIOLVC18[2]
GPIOLVC18[1]
GPIOLVC18[0]
K12
K13
H23
G23
M12
B20
C20
F20
E20
GPIOLVC33[4]
GPIOLVC33[3]
GPIOLVC33[2]
GPIOLVC33[1]
GPIOLVC33[0]
GPIOLVC15[3]
GPIOLVC15[2]
GPIOLVC15[1]
GPIOLVC15[0]
GPIOLVC18[20]
GPIOLVC18[19]
GPIOLVC18[18]
GPIOLVC18[17]
GPIOLVC18[16]
GPIOLVC18[15]
GPIOLVC18[14]
GPIOLVC18[13]
GPIOLVC18[12]
GPIOLVC18[11]
GPIOLVC18[10]
GPIOLVC18[7]
GPIOLVC18[4]
AM20
AP24
AN24
AL24
AP25
AD25
AM25
AA25
AJ25
AJ26
AK27
AC29
AA30
GPIOLVC18[20]
GPIOLVC18[19]
GPIOLVC18[18]
GPIOLVC18[17]
GPIOLVC18[16]
GPIOLVC18[15]
GPIOLVC18[14]
GPIOLVC18[13]
GPIOLVC18[12]
GPIOLVC18[11]
GPIOLVC18[10]
GPIOLVC18[7]
GPIOLVC18[4]

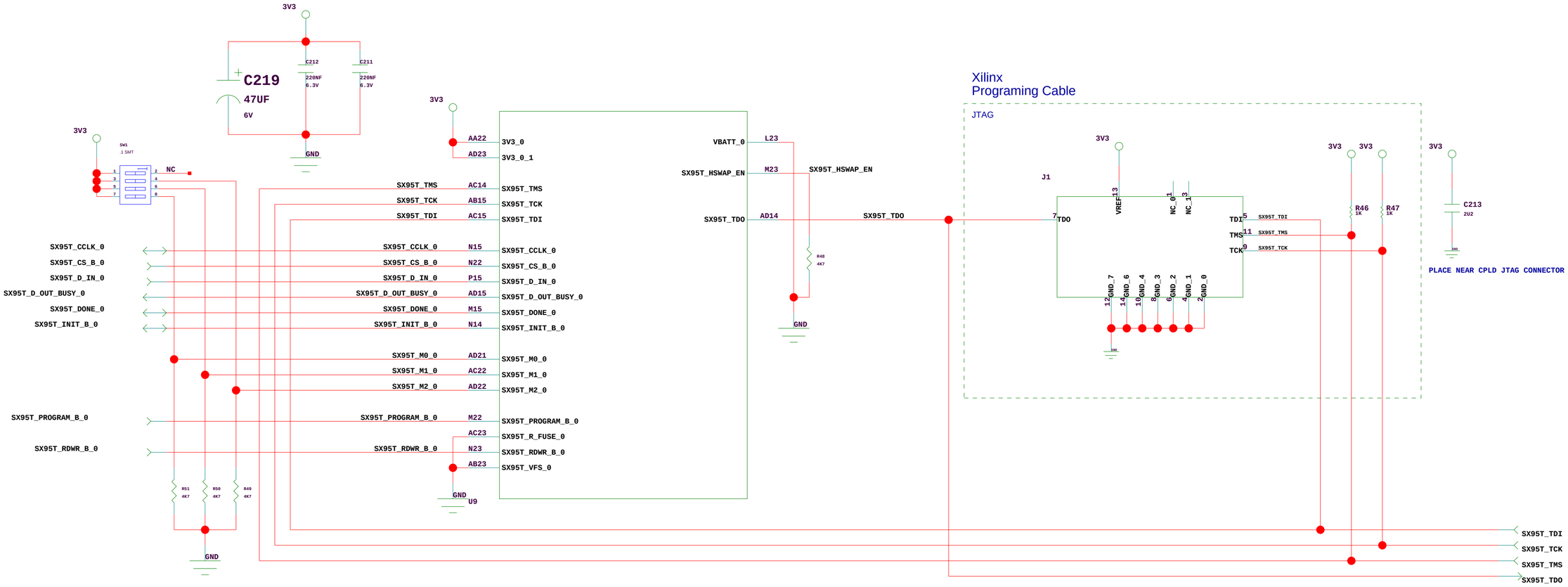

DO NOT SHORT
JP40
1V8
VDDQ_QDR2_BV9_1
SELECT EITHER 1V9(QDR11+) OR 1V8(QDR11)
1V9
GND
VDDQ_QDR2_BV9_1
QDR2P_POWER
VDD_QDR2_BV9_1
VTT_QDR_BV9_1
QDR2_BV9_1_SA[0]
QDR2_BV9_1_SA[1]
QDR2_BV9_1_SA[2]
QDR2_BV9_1_SA[3]
QDR2_BV9_1_SA[4]
QDR2_BV9_1_SA[5]
QDR2_BV9_1_SA[6]
QDR2_BV9_1_SA[7]
QDR2_BV9_1_SA[8]
QDR2_BV9_1_SA[9]
QDR2_BV9_1_SA[10]
QDR2_BV9_1_SA[11]
QDR2_BV9_1_SA[12]
QDR2_BV9_1_SA[13]
QDR2_BV9_1_SA[14]
QDR2_BV9_1_SA[15]
QDR2_BV9_1_SA[16]
QDR2_BV9_1_SA[17]
QDR2_BV9_1_SA[18]
QDR2_BV9_1_SA[19]
QDR2_BV9_1_SA[20]
QDR2_BV9_1_SA[21]
QDR2_BV9_1_C_N_COMPAT
QDR2_BV9_1_QVLD
QDR2_BV9_1_BW
QDR2_BV9_1_R
QDR2_BV9_1_W
QDR2_BV9_1_K_P
QDR2_BV9_1_K_N
QDR2_BV9_1_D[0]
QDR2_BV9_1_D[1]
QDR2_BV9_1_D[2]
QDR2_BV9_1_D[3]
QDR2_BV9_1_D[4]
QDR2_BV9_1_D[5]
QDR2_BV9_1_D[6]
QDR2_BV9_1_D[7]
QDR2_BV9_1_D[8]
QDR2_BV9_1_D[9]
QDR2_BV9_1_D[10]
QDR2_BV9_1_D[11]
QDR2_BV9_1_D[12]
QDR2_BV9_1_D[13]
QDR2_BV9_1_D[14]
QDR2_BV9_1_D[15]
QDR2_BV9_1_D[16]
QDR2_BV9_1_D[17]
RP38 51R
RP37 51R
RP36 51R
RP35 51R
RP34 51R
RP33 51R
RP32 51R
RP31 51R
RP30 51R
RP29 51R
RP28 51R
NC
NC
QDR2_BV9_1_SA[0]
QDR2_BV9_1_SA[1]
QDR2_BV9_1_SA[2]
QDR2_BV9_1_SA[3]
QDR2_BV9_1_SA[4]
QDR2_BV9_1_SA[5]
QDR2_BV9_1_SA[6]
QDR2_BV9_1_SA[7]
QDR2_BV9_1_SA[8]
QDR2_BV9_1_SA[9]
QDR2_BV9_1_SA[10]
QDR2_BV9_1_SA[11]
QDR2_BV9_1_SA[12]
QDR2_BV9_1_SA[13]
QDR2_BV9_1_SA[14]
QDR2_BV9_1_SA[15]
QDR2_BV9_1_SA[16]
QDR2_BV9_1_SA[17]
QDR2_BV9_1_SA[18]
QDR2_BV9_1_SA[19]
QDR2_BV9_1_SA[20]
QDR2_BV9_1_SA[21]
QDR2_BV9_1_C_N_COMPAT
QDR2_BV9_1_QVLD
QDR2_BV9_1_BW
QDR2_BV9_1_R
QDR2_BV9_1_W
QDR2_BV9_1_K_P
QDR2_BV9_1_K_N
QDR2_BV9_1_D[0]
QDR2_BV9_1_D[1]
QDR2_BV9_1_D[2]
QDR2_BV9_1_D[3]
QDR2_BV9_1_D[4]
QDR2_BV9_1_D[5]
QDR2_BV9_1_D[6]
QDR2_BV9_1_D[7]
QDR2_BV9_1_D[8]
QDR2_BV9_1_D[9]
QDR2_BV9_1_D[10]
QDR2_BV9_1_D[11]
QDR2_BV9_1_D[12]
QDR2_BV9_1_D[13]
QDR2_BV9_1_D[14]
QDR2_BV9_1_D[15]
QDR2_BV9_1_D[16]
QDR2_BV9_1_D[17]
VTT_QDR_BV9_1
U50
QDR2P_2_4_BMX18
QDR2P_CTRL_DATA
QDR2P_JTAG
QDR2_TDI
QDR2_TMS
QDR2_TCK
QDR2_BV9_1_SYS_RST_N
QDR2_BV9_1_TDO
TDO
TDI
TMS
TCK
R1
R2
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
R44
R45
R46
R47
R48
R49



VTT_QDR_BY2_3
RP1 51R
RP2 51R
RP3 51R
RP4 51R
RP5 51R
RP6 51R
RP7 51R
RP8 51R
RP9 51R
RP10 51R
RP11 51R
RP12 51R
GND
QDR2_BY2_3_QVLD
QDR2_BY2_3_C_N_COMPAT
U11
QDR2P_CTRL_DATA
QDR2P_2_4_8MX18
QDR2P_JTAG
QDR2P_POWER
QDR2_BY0_1_TDO
QDR2_TMS
QDR2_TCK
QDR2_BY2_3_TDO
QDR2_BY2_3_SYS_RST_N
QDR2_BY2_3_CQ_P
QDR2_BY2_3_CQ_N
QDR2_BY2_3_SA[21]
U9
BANKS=15, 11
VREF_QDR_BY2_3
VDDQ_QDR2_BY2_3
VDD_QDR2_BY2_3
VRP_15
VRN_15
C223 47UF 6V
C224 47UF 6V
U10
VIN
VLDOIN
VDDQSNS
S3
S5
VTT
VTTSNS
VTTREF
5V
1V5
1V8
JP1
SELECT EITHER 1V5(QDRii+) OR 1V8(QDRii)
DO NO SHORT

TBD

VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input



The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups. Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

Place nearest PHY pin 96

Place nearest PHY pin 101

Place nearest PHY pin 98

Place nearest PHY pin 100

Place as close to PHY CORE VDD power pins as possible

Place as close to PHY IO VDD power pins as possible

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place jumers in line with signals

Place components as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible.

Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5

Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

Bottom LED
Green/Toggle = ACTIVITY

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

ETHERNET Mgt.

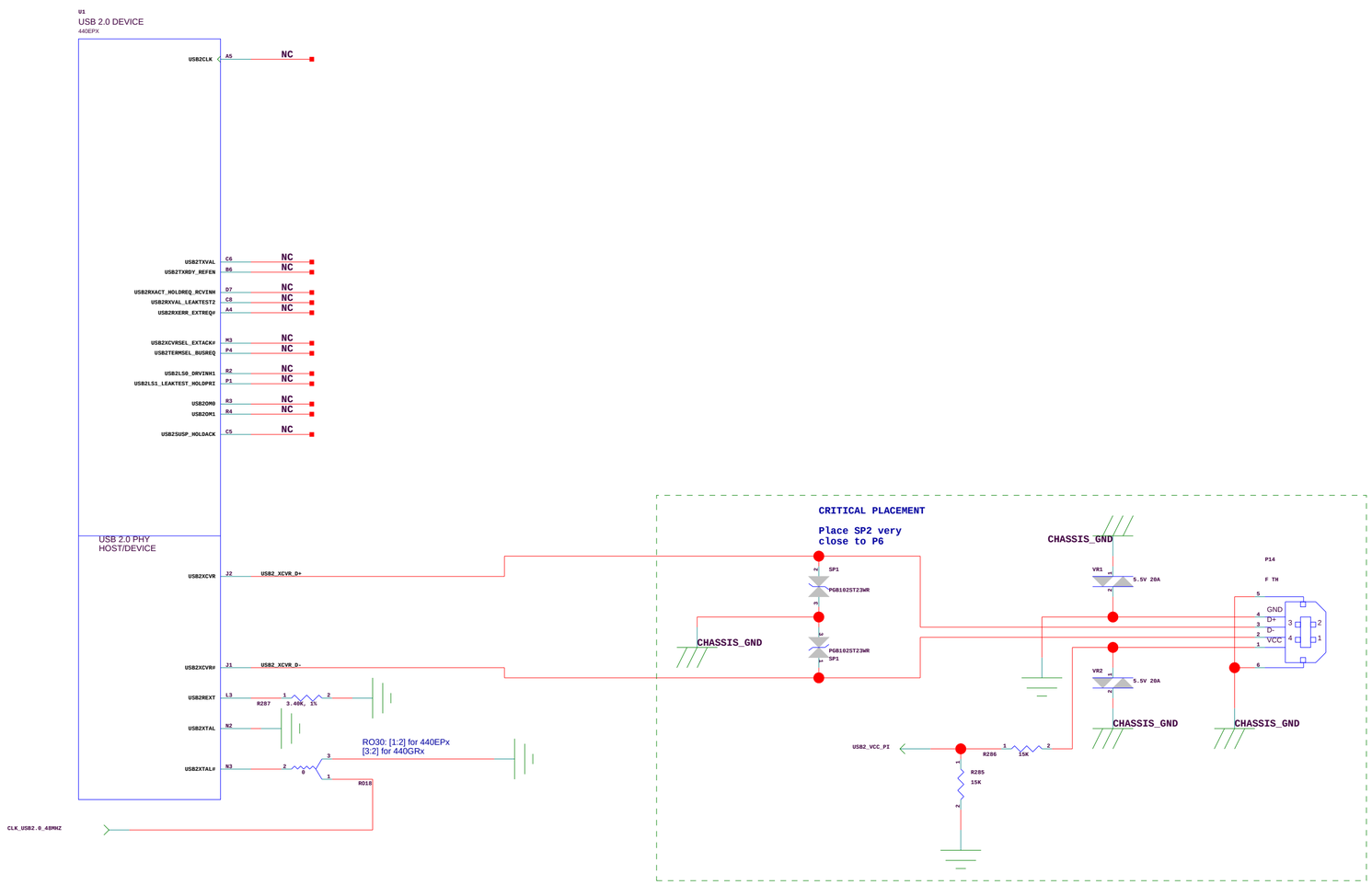
Gig-Ethernet RGMII0

DP83865DVH

HFJ11-1G02E-L12

2V5
C482
10NF
Place nearest PHY pin 96
2V5
C455
10NF
Place nearest PHY pin 101
1V8
C458 10NF
C459 100NF
C457 10NF
C460 100NF
C461 10NF
C479 100NF
C462 10NF
C456 100NF
Place as close to PHY CORE VDD power pins as possible
1V8
R256 1R
C483 22UF/6V
C476 10NF
Place nearest PHY pin 98
ETH1_PGM_VDD
1V8
R257 1R
C484 22UF/6V
C475 10NF
Place nearest PHY pin 100
ETH1_1V8_AVDD3
2V5
C481 10NF
C477 100NF
C480 10NF
C470 100NF
C468 10NF
C469 100NF
C467 10NF
C478 100NF
C465 10NF
C466 100NF
C463 10NF
C464 100NF
Place as close to PHY IO VDD power pins as possible
2V5
2V5
1V8
1V8
2V5
U1
4408PX
GigE/Ethernet ROM#1
GMC1_TXD0
GMC1_TXD1
GMC1_TXD2
GMC1_TXD3
GMC1_TXCTL
GMC1_TXCLK
GMC1_RXD0
GMC1_RXD1
GMC1_RXD2
GMC1_RXD3
GMC1_RXCTL
GMC1_RXCLK
GMCMDCLK
GMCMDIO
Place resistors as close to CPU as possible and keep all traces lengths equal
Place resistors close to PHY all trace lengths equal
Place jumers in line with signals
JP39
JP38
U47
DP83865DVH
Place components as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible.
Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5
MDIA_P
MDIA_N
MDIB_P
MDIB_N
MDIC_P
MDIC_N
MDID_P
MDID_N
R255 49.9R
R249 49.9R
R251 49.9R
R253 49.9R
C474 10NF
C472 10NF
C473 10NF
C471 10NF
49.9R
49.9R
49.9R
49.9R
VDD_SEL_STRAP
MAC_CLK_EN_STRAP
MDIX_EN_STRAP
MULTI_EN_STRAP
LINK1000_LED/AN_EN_STRAP
LINK100_LED/DUPLEX_STRAP
LINK10_LED/RLED/SPEED1_STRAP
ACTIVITY_LED/SPEED0_STRAP
DUPLEX_LED/PHYAD0B0_STRAP
PHYAD0B1_STRAP
PHYAD0B2_STRAP
PHYAD0B3_STRAP
PHYAD0B4_STRAP
R260 2K2
NOSTUFF
R261 2K2
R262 2K2
NOSTUFF
R247 5K76
Ethernet LEDs
Top LED = SPEED/LINK
Green = 1000
Off = 10/100
Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY
HFJ11-1G02E-L12
C485 22UF/6V
CHASSIS_GND
JP35
JP36
JP34
JP32
JP30
JP28
JP25
JP24
DUPLEX LED JP37
L10 LED
L100 LED
D10
D11
D9
R246 2K2
R269 2K2
R268 2K2
R258 2K2
R242 2K2
R244 330R
R267 330R
R241 330R
R243 330R
JP33
JP31
JP29
JP27
JP26
STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL


VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
DDR_VTT
DDR_PA[15:0]
DDR_PDQ[63:0]
DDR SDRAM
J6
879160001
U27
VIN
VLDOIN
VDDQSNS
S3
S5
VTT
VTTSNS
VTTREF
GND
PGND
5V
1V8
DDR_VREF_0V9
DDR_CLKOUT
DDR_CLKOUT#
500ps Loop
Place parts as close to CPU as possible
PPC_DDR2_DIMM_SCL
PPC_DDR2_DIMM_SDA
PPC_DDR2_RESET_N
PPC_DDR2_ERROR
PAR_IN
ERR_OUT
RP13
RP14
RP15
RP16
RP17
RP18
RP19
PLACE NEAREST DDR2 MODULE PINS



KAROO ARRAY TELESCOPE, NRF UNIT 12, LONSDALE BUILDING LONSDALE WAY, PINELANDS, 7405 SOUTH AFRICA			
TITLE: ROACH_PPC_USB			
CHECKED BY: <PUT NAME HERE>	SIZE: A2	DWG NO: <PUT DRAWING NUMBER HERE>	REV: 0
DRAWN BY: <PUT NAME HERE>	SCALE: NTS	SHEET: 1 of 1	9-20-2007_11:16

Memory Bus

PAD0[27..31]

PAD0C7
PAD0C6
PAD0C5
PAD0C4
PAD0C3
P4 PAD4
P7 PAD8
P9 PAD10
P10 PAD12
P11 PAD15

PDAT4[0..7]

PDAT40
PDAT41
PDAT42
PDAT43
PDAT44
PDAT45
PDAT46
PDAT47
P12 PAD16
P13 PAD17
P14 PAD18
P15 PAD19
P16 PAD20
P17 PAD21
P18 PAD23
P19 PAD28

NC P20 PAD29
NC P21 PAD30
NC P22 PAD31
NC P23 PAD32
NC P24 PAD33
NC P25 PAD34
NC P26 PAD35
NC P28 PAD44

PCS_2 P30 PAD48
PDE# P31 PAD49
PE_WR P32 PAD50
PWRE_DF P33 PAD52

RESETS

CPU_TRST# = '1' when JTAG_TRST# = '1' and RESET_PORN = '1' else '0'; see errata sheet

RESET_PORN P34 PAD54
RESET_PB_PORN P35 PAD55
NC P38 PAD59
DEBUG_TRST# P40 PAD64
CPU_TRST# P41 PAD65

CLOCKS

CLK_CPLD_33MHZ P42 PAD66
CLK_CPLD_50MHZ P43 PAD67
CLK_PERCLK P44 PAD68
CLK_TMRCLK P45 PAD69
CLK_SEL_M66EN P46 PAD70
SEL_SYSCLK P48 PAD73

STATUS / MISC

SYSERR P49 PAD74

FLASH

FDY_BSY P50 PAD75
FWP# P51 PAD76

I2C

EE1_WP P52 PAD77
EE2_BOOT_WP P53 PAD81
ST7M_AS P54 PAD82

USB

USB2_RESET P56 PAD86
CLK_USB2_CPLD P57 PAD87
USB2_VCC_PE P58 PAD88
USB2_VCC_FI P59 PAD89

Assertion of USB2_RESET may be asynchronous to CLK_USB2_CPLD
De-assertion of USB2_RESET must be synchronous to CLK_USB2_CPLD

NAND FLASH

WP_NPV P60 PAD90

ETHERNET

GETH1_COMA P61 PAD95
GETH0_COMA P64 PAD100
GETH0_RST# P66 PAD102
GETH1_RST# P68 PAD105

USB_EBC_MUX

USB_SELECT# P69 PAD107
EBC_SELECT# P70 PAD108
RESET_CPLD# P71 PAD109

NC P74 PAD112
NC P75 PAD113

roach_cpld_XC2C256_7VQ100C_pcb

U22

P142 PAD217
P140 PAD214
P139 PAD213
P138 PAD212
P137 PAD211
P136 PAD208
P135 PAD207
P134 PAD206
P133 PAD204
P132 PAD199
P131 PAD197
P130 PAD196
P129 PAD195
P128 PAD194
P126 PAD192
P125 PAD191
P124 PAD190
P121 PAD187
P120 PAD186
P119 PAD178
P118 PAD177
P117 PAD176
P116 PAD175
P115 PAD173
P114 PAD171
P113 PAD169
P112 PAD168
P111 PAD167
P110 PAD166
P107 PAD163
P106 PAD162
P105 PAD161
P104 PAD160
P103 PAD158
P102 NC PAD156
P101 NC PAD154
P100 NC PAD152
P98 NC PAD146
P97 NC PAD145
P96 NC PAD144
P95 NC PAD143
P94 NC PAD142
P92 NC PAD138
P91 NC PAD137
P88 NC PAD134
P87 NC PAD133
P86 NC PAD132
P85 NC PAD131
P83 NC PAD125
P82 NC PAD121
P81 NC PAD120
P80 NC PAD119
P79 NC PAD118
P78 NC PAD117
P77 NC PAD115
P76 NC PAD114

USER_DIP0
USER_DIP1
USER_DIP2
USER_DIP3
SW2 4POLE User DIP-Swith

CFG_DIP0
CFG_DIP1
CFG_DIP2
M66EN

USER_LED0
USER_LED1
SYSERR#
RESET_BUFPORN

SysErr will be used to drive Status LED (active H)

SX95T_CCLK_0
SX95T_CS_B_0
SX95T_D_IN_0
SX95T_D_OUT_BUSY_0
SX95T_DONE_0
SX95T_INIT_B_0
SX95T_PROGRAM_B_0
SX95T_RDWR_B_0

CMD/DI
CLK/SCLK

J3 GMMC001LEU

2 CMD/DI
5 CLK/SCLK
4 VDD
3 VSS1
6 VSS2
14 SW
15 GND1
16 GND2
17 GND3
18 GND4

DAT0/DO 7
DAT1 8
DAT2 9
DAT3 1
DAT4 10
DAT5 11
DAT6 12
DAT7 13
MNT1 19NC
MNT2 20NC

SV_VIN
74LVC1G66
VCC
GND
PWR_GOOD
C308 0.1UF 0402

Boot Configuration

SW3 4POLE Configuration DIP-Swith

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

BOOT_CFG0
BOOT_CFG1
BOOT_CFG2

roach_cpld_XC2C256_7VQ100C_configpins

NC P2 PAD1
NC P3 PAD3
NC P5 PAD5
NC P6 PAD7
NC P39 PAD62
P63 TDI
P65 TMS
P67 TCK
P122 TDO
NC P143 PAD218

U22

Xilinx
Programing Cable

JTAG

J2

TDO 7
VREF 13
NC_0 8
NC_1 3
TDI 5 CPLD_TDI
TMS 11 CPLD_TMS
TCK 9 CPLD_TCK

GND_7 12
GND_6 10
GND_4 8
GND_3 6
GND_2 4
GND_1 2
GND_0

R83 1K
R82 1K

C309 2U2

PLACE NEAR CPLD JTAG CONNECTOR

roach_cpld_XC2C256_7VQ100C_powerpins

P1 VCC
P8 VAUX
P27 VCCIO_3
P37 VCC_1
P55 VCCIO_4
P73 VCCIO_5
P84 VCC_2
P93 VCCIO_6
P109 VCCIO
P127 VCCIO_1
P141 VCCIO_2

P29 GND_3
P36 GND_4
P47 GND_5
P62 GND_6
P72 GND_7
P89 GND_8
P90 GND_9
P99 GND_10
P108 GND
P123 GND_1
P144 GND_2

U22

C297 C298 C299 C300 C301 C302 C303 C304 C305 C306 C307
100NF 10V

PLACE NEAR CPLD POWER PINS

PWR_GOOD monitors the
+1.0v, 1V5, 1V8,
2V5, and 3V3 supplies

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_3V3_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz

IRQ0-9 have programmable polarity per
section 10.5.7 (UIC0_PR) 440ep user
manual

Critical Placement and Route
Clock Rules:

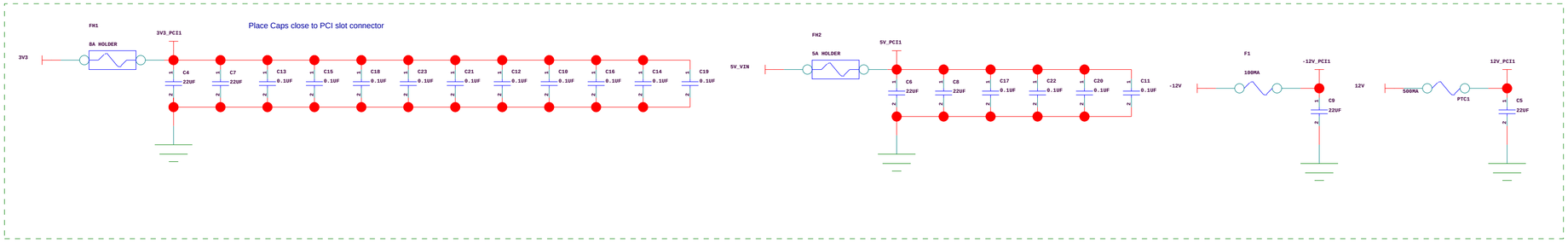
Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible

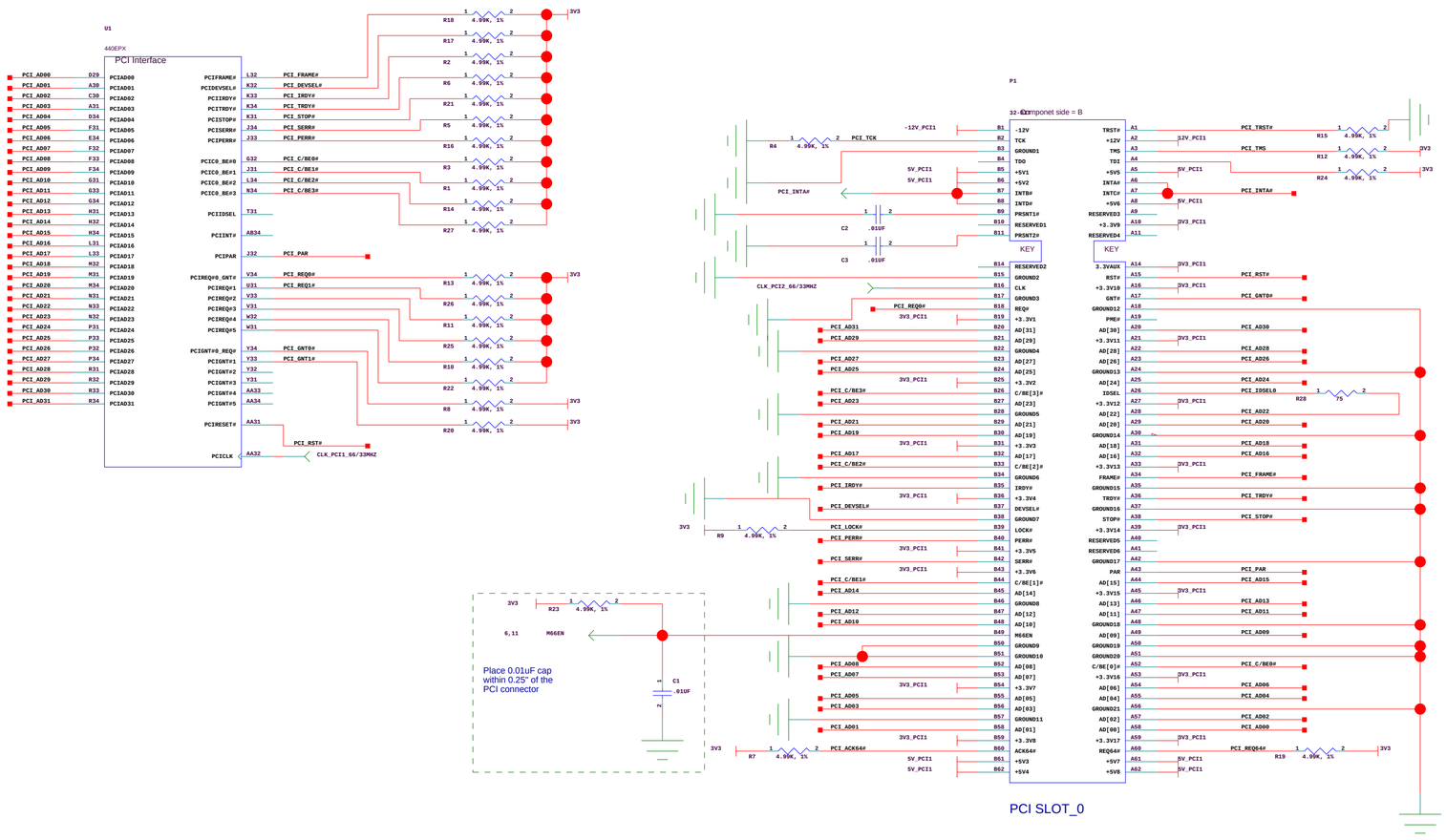
TRACE & JTAG CONNECTORS

Critical placement and routing
of the Trace connector and nets.
Up to CPU frequency/4

R26 is for current
limiting and should
be <100 Ohms.

NO POP
RO1 - RO5





PCI SLOT_0

Include silkscreen text:
"SUPPORTS 3V3 IO ONLY"

Optional PRSNT signals are not used, max 25W is available		
PRSNT1#	PRSNT2#	Expansion Configuration
Open	Open	No expansion board present
Ground	Open	Expansion board present, 25 W maximum
Open	Ground	Expansion board present, 15 W maximum
Ground	Ground	Expansion board present, 7.5 W maximum

KAROO ARRAY TELESCOPE, NRF
UNIT 12, LONSDALE BUILDING
LONSDALE WAY, PINELANDS, 7405
SOUTH AFRICA

TITLE: ROACH_PPC_PCI

CHECKED BY: <PUT NAME HERE>
DRAWN BY: <PUT NAME HERE>
SIZE: A2
DWG NO: <PUT DRAWING NUMBER HERE>
REV: 0
SCALE: NTS
SHEET: 1 of 1
9-20-2007_11:16

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J3: "1V5"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J4: "1V8"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J5: "2V5"

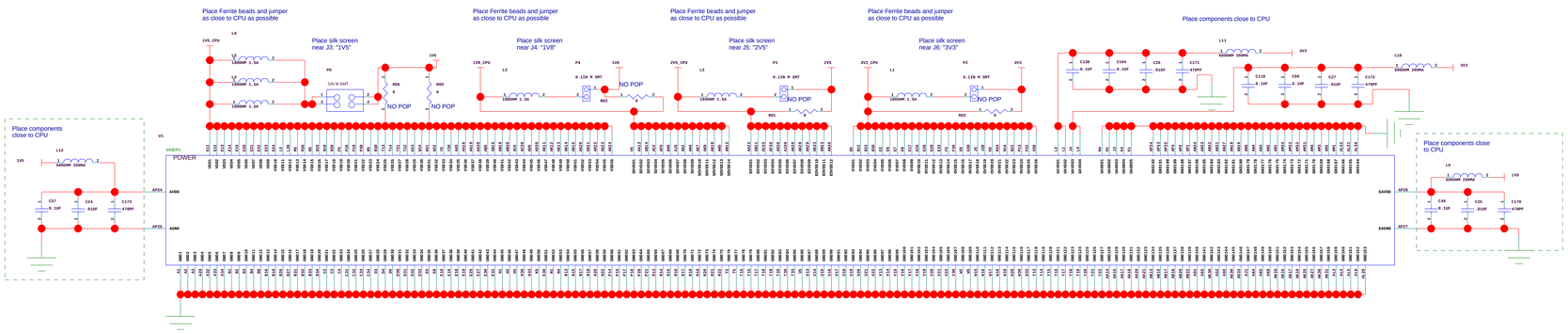
Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J6: "3V3"

Place components close to CPU

Place components close to CPU

Place components close to CPU



5V

FH5

5A HOLDER

5V_VIN

+5.0 V

C23 220UF
C31 220UF
C29 0.10F
C100 0.10F

Alternate power input terminal
Two 10A fuses result in 16A rating

Bulk Decoupling

CPU Core by-pass caps place as close to CPU Vdd pins as possible

Bulk Decoupling

CPU Core by-pass caps place as close to CPU SOVdd pins as possible

Bulk Decoupling

CPU Core by-pass caps place as close to CPU DVdd pins as possible

Each Analog GND tied to Digital GND at a single point.

+1.8 V

Place all components within this block close together

~2.9Amp

VOUT= 0.6v(1+R1/R2)

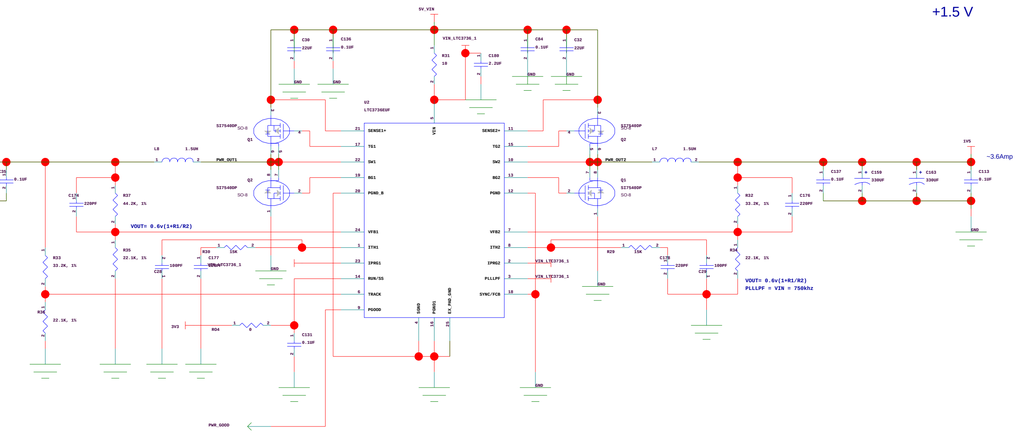
Place these 4 caps close to DDR parts

PWR_GOOD

+1.5 V

~3.6Amp

VOUT= 0.6v(1+R1/R2)
PLLLPF = VIN = 750khz

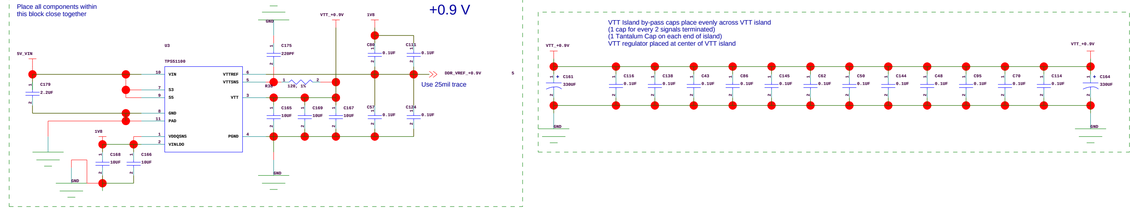


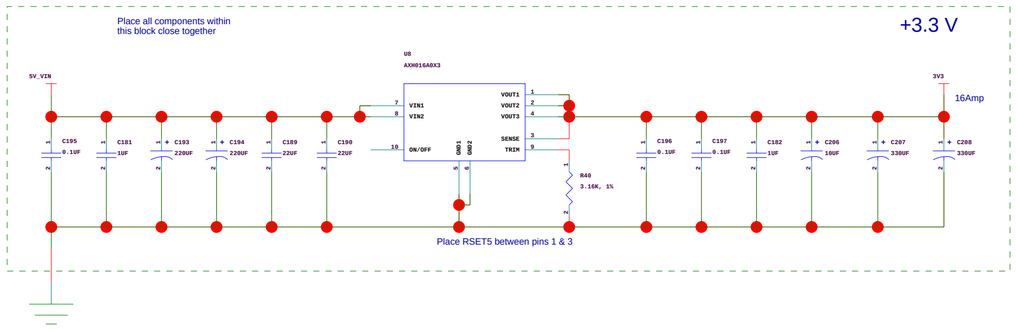
Place all components within this block close together

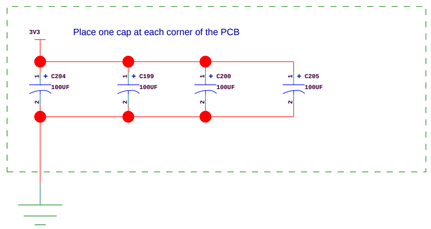
+0.9 V

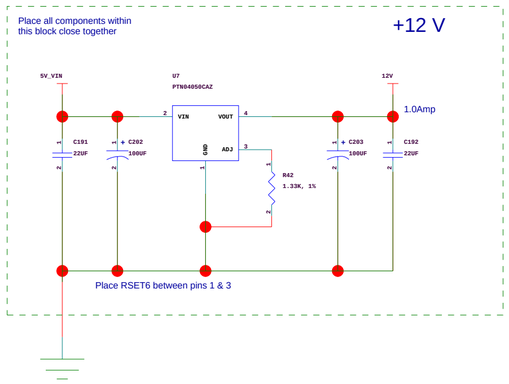
Use 25mil trace

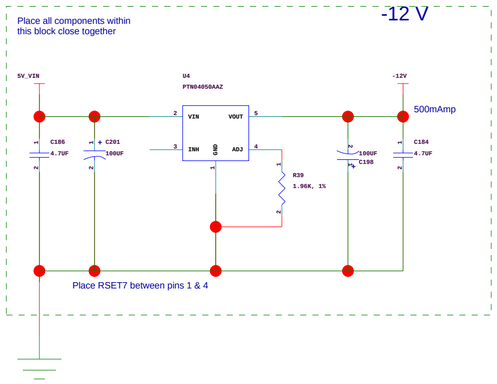
VTT island by-pass caps place evenly across VTT island
(1 cap for every 2 signals terminated)
(1 Tantalum Cap on each end of island)
VTT regulator placed at center of VTT island

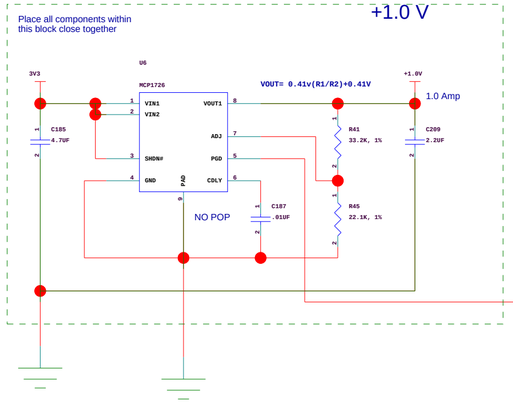


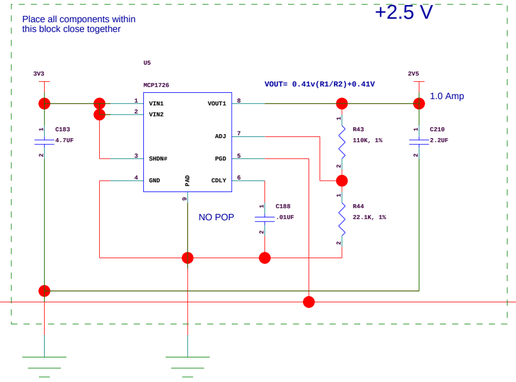








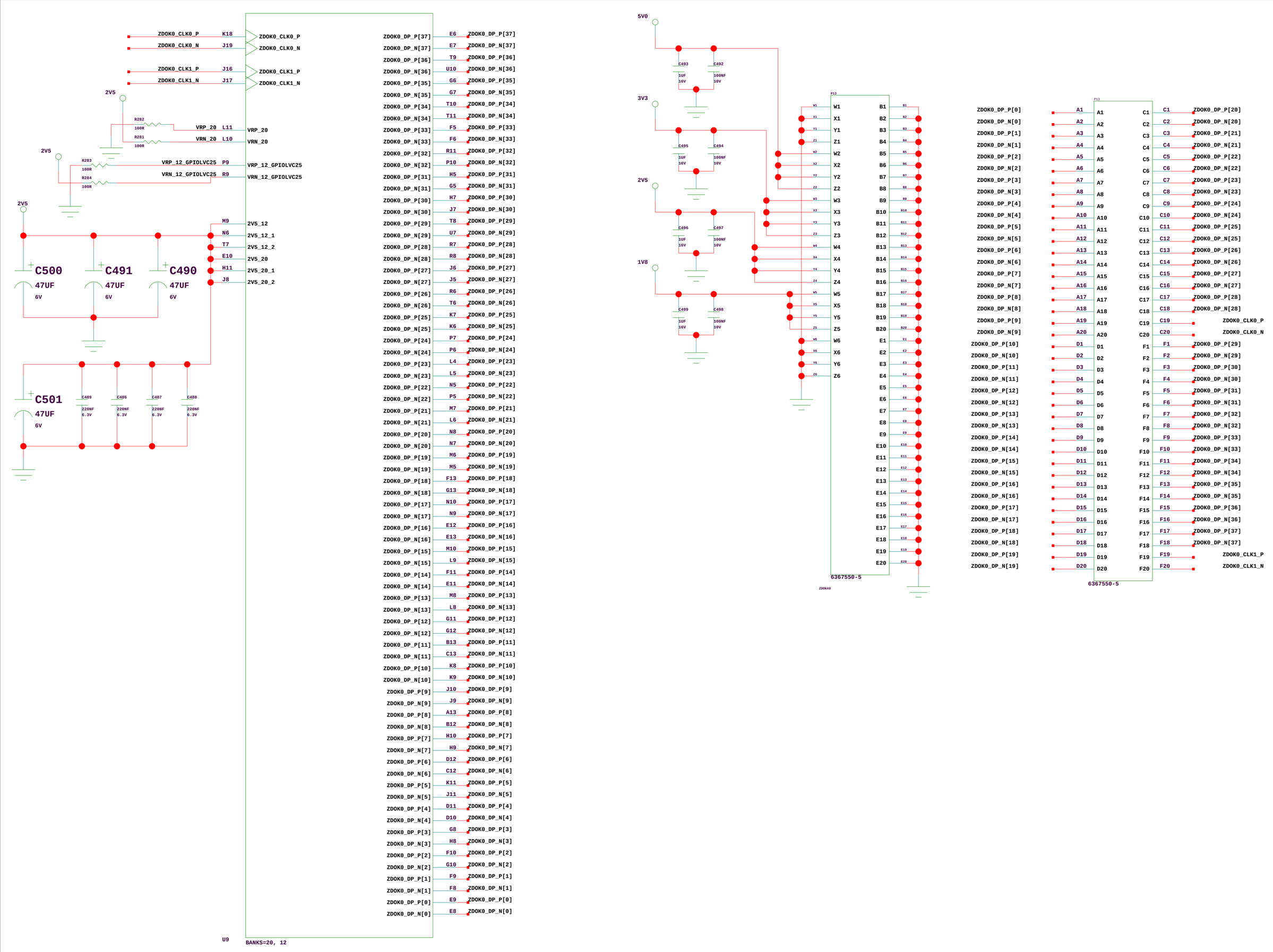


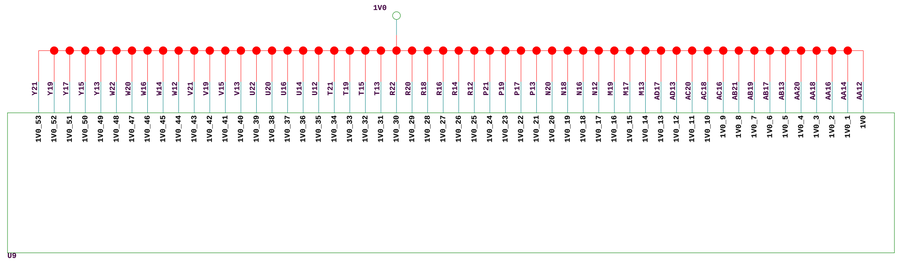


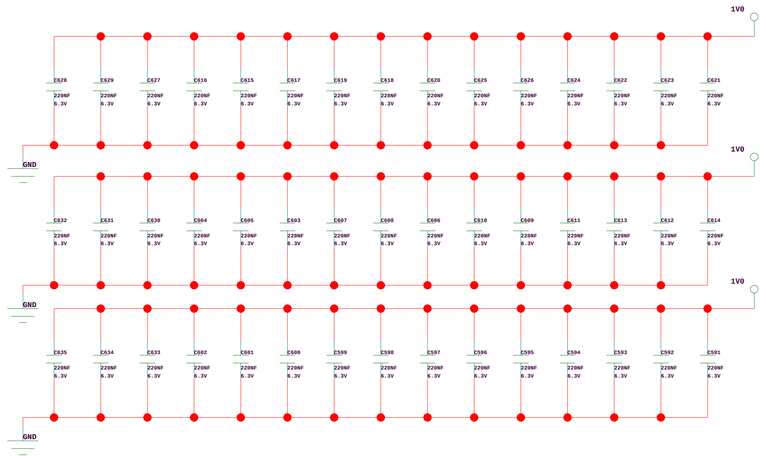
KAROO ARRAY TELESCOPE, NRF
UNIT 12, LONSDALE BUILDING
LONSDALE WAY, PINELANDS, 7405
SOUTH AFRICA

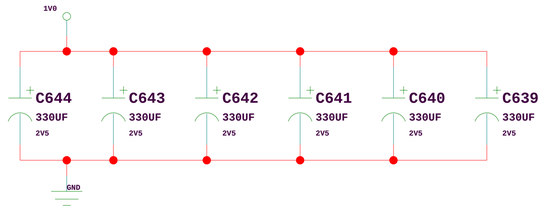
TITLE: ROACH_PPC_POWER_2

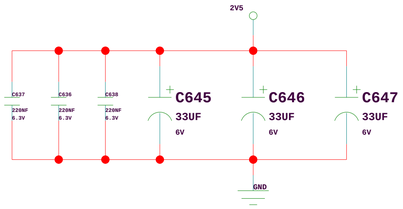
CHECKED BY: <PUT NAME HERE>	SIZE: A2	DWG NO: <PUT DRAWING NUMBER HERE>	REV: 0
DRAWN BY: <PUT NAME HERE>	SCALE: NTS	SHEET: 1 of 1	9-20-2007_11:16

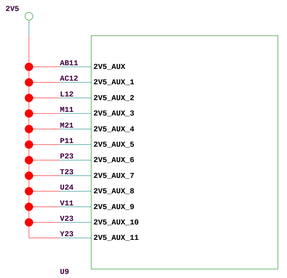

ZDOK0_CLK0_P K18
ZDOK0_CLK0_N J19
ZDOK0_CLK1_P J16
ZDOK0_CLK1_N J17
2V5
R282 100R
R281 100R
VRP_20 L11
VRN_20 L10
R283 100R
R284 100R
VRP_12_GPIOLVC25 P9
VRN_12_GPIOLVC25 R9
M9 N6 T7 E10 H11 J8
2V5_12 2V5_12_1 2V5_12_2 2V5_20 2V5_20_1 2V5_20_2
C500 47UF 6V
C491 47UF 6V
C490 47UF 6V
C501 47UF 6V
C489 220NF 6.3V
C486 220NF 6.3V
C487 220NF 6.3V
C488 220NF 6.3V
U9
BANKS=20, 12
ZDOK0_DP_P[37] E6
ZDOK0_DP_N[37] E7
ZDOK0_DP_P[36] T9
ZDOK0_DP_N[36] U10
ZDOK0_DP_P[35] G6
ZDOK0_DP_N[35] G7
ZDOK0_DP_P[34] T10
ZDOK0_DP_N[34] T11
ZDOK0_DP_P[33] F5
ZDOK0_DP_N[33] F6
ZDOK0_DP_P[32] R11
ZDOK0_DP_N[32] P10
ZDOK0_DP_P[31] H5
ZDOK0_DP_N[31] G5
ZDOK0_DP_P[30] H7
ZDOK0_DP_N[30] J7
ZDOK0_DP_P[29] T8
ZDOK0_DP_N[29] U7
ZDOK0_DP_P[28] R7
ZDOK0_DP_N[28] R8
ZDOK0_DP_P[27] J6
ZDOK0_DP_N[27] J5
ZDOK0_DP_P[26] R6
ZDOK0_DP_N[26] T6
ZDOK0_DP_P[25] K7
ZDOK0_DP_N[25] K6
ZDOK0_DP_P[24] P7
ZDOK0_DP_N[24] P6
ZDOK0_DP_P[23] L4
ZDOK0_DP_N[23] L5
ZDOK0_DP_P[22] N5
ZDOK0_DP_N[22] P5
ZDOK0_DP_P[21] M7
ZDOK0_DP_N[21] L6
ZDOK0_DP_P[20] N8
ZDOK0_DP_N[20] N7
ZDOK0_DP_P[19] M6
ZDOK0_DP_N[19] M5
ZDOK0_DP_P[18] F13
ZDOK0_DP_N[18] G13
ZDOK0_DP_P[17] N10
ZDOK0_DP_N[17] N9
ZDOK0_DP_P[16] E12
ZDOK0_DP_N[16] E13
ZDOK0_DP_P[15] M10
ZDOK0_DP_N[15] L9
ZDOK0_DP_P[14] F11
ZDOK0_DP_N[14] E11
ZDOK0_DP_P[13] M8
ZDOK0_DP_N[13] L8
ZDOK0_DP_P[12] G11
ZDOK0_DP_N[12] G12
ZDOK0_DP_P[11] B13
ZDOK0_DP_N[11] C13
ZDOK0_DP_P[10] K8
ZDOK0_DP_N[10] K9
ZDOK0_DP_P[9] J10
ZDOK0_DP_N[9] J9
ZDOK0_DP_P[8] A13
ZDOK0_DP_N[8] B12
ZDOK0_DP_P[7] H10
ZDOK0_DP_N[7] H9
ZDOK0_DP_P[6] D12
ZDOK0_DP_N[6] C12
ZDOK0_DP_P[5] K11
ZDOK0_DP_N[5] J11
ZDOK0_DP_P[4] D11
ZDOK0_DP_N[4] D10
ZDOK0_DP_P[3] G8
ZDOK0_DP_N[3] H8
ZDOK0_DP_P[2] F10
ZDOK0_DP_N[2] G10
ZDOK0_DP_P[1] F9
ZDOK0_DP_N[1] F8
ZDOK0_DP_P[0] E9
ZDOK0_DP_N[0] E8
5V0
3V3
2V5
1V8
C493 1UF 16V
C492 100NF 10V
C495 1UF 16V
C494 100NF 10V
C496 1UF 16V
C497 100NF 10V
C499 1UF 16V
C498 100NF 10V
P13
W1 X1 Y1 Z1 W2 X2 Y2 Z2 W3 X3 Y3 Z3 W4 X4 Y4 Z4 W5 X5 Y5 Z5 W6 X6 Y6 Z6
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20
6367550-5
ZDOK40
ZDOK0_DP_P[0] ZDOK0_DP_N[0] ZDOK0_DP_P[1] ZDOK0_DP_N[1] ZDOK0_DP_P[2] ZDOK0_DP_N[2] ZDOK0_DP_P[3] ZDOK0_DP_N[3] ZDOK0_DP_P[4] ZDOK0_DP_N[4] ZDOK0_DP_P[5] ZDOK0_DP_N[5] ZDOK0_DP_P[6] ZDOK0_DP_N[6] ZDOK0_DP_P[7] ZDOK0_DP_N[7] ZDOK0_DP_P[8] ZDOK0_DP_N[8] ZDOK0_DP_P[9] ZDOK0_DP_N[9] ZDOK0_DP_P[10] ZDOK0_DP_N[10] ZDOK0_DP_P[11] ZDOK0_DP_N[11] ZDOK0_DP_P[12] ZDOK0_DP_N[12] ZDOK0_DP_P[13] ZDOK0_DP_N[13] ZDOK0_DP_P[14] ZDOK0_DP_N[14] ZDOK0_DP_P[15] ZDOK0_DP_N[15] ZDOK0_DP_P[16] ZDOK0_DP_N[16] ZDOK0_DP_P[17] ZDOK0_DP_N[17] ZDOK0_DP_P[18] ZDOK0_DP_N[18] ZDOK0_DP_P[19] ZDOK0_DP_N[19]
P13
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15 F16 F17 F18 F19 F20
ZDOK0_DP_P[20] ZDOK0_DP_N[20] ZDOK0_DP_P[21] ZDOK0_DP_N[21] ZDOK0_DP_P[22] ZDOK0_DP_N[22] ZDOK0_DP_P[23] ZDOK0_DP_N[23] ZDOK0_DP_P[24] ZDOK0_DP_N[24] ZDOK0_DP_P[25] ZDOK0_DP_N[25] ZDOK0_DP_P[26] ZDOK0_DP_N[26] ZDOK0_DP_P[27] ZDOK0_DP_N[27] ZDOK0_DP_P[28] ZDOK0_DP_N[28] ZDOK0_CLK0_P ZDOK0_CLK0_N ZDOK0_DP_P[29] ZDOK0_DP_N[29] ZDOK0_DP_P[30] ZDOK0_DP_N[30] ZDOK0_DP_P[31] ZDOK0_DP_N[31] ZDOK0_DP_P[32] ZDOK0_DP_N[32] ZDOK0_DP_P[33] ZDOK0_DP_N[33] ZDOK0_DP_P[34] ZDOK0_DP_N[34] ZDOK0_DP_P[35] ZDOK0_DP_N[35] ZDOK0_DP_P[36] ZDOK0_DP_N[36] ZDOK0_DP_P[37] ZDOK0_DP_N[37] ZDOK0_CLK1_P ZDOK0_CLK1_N
6367550-5

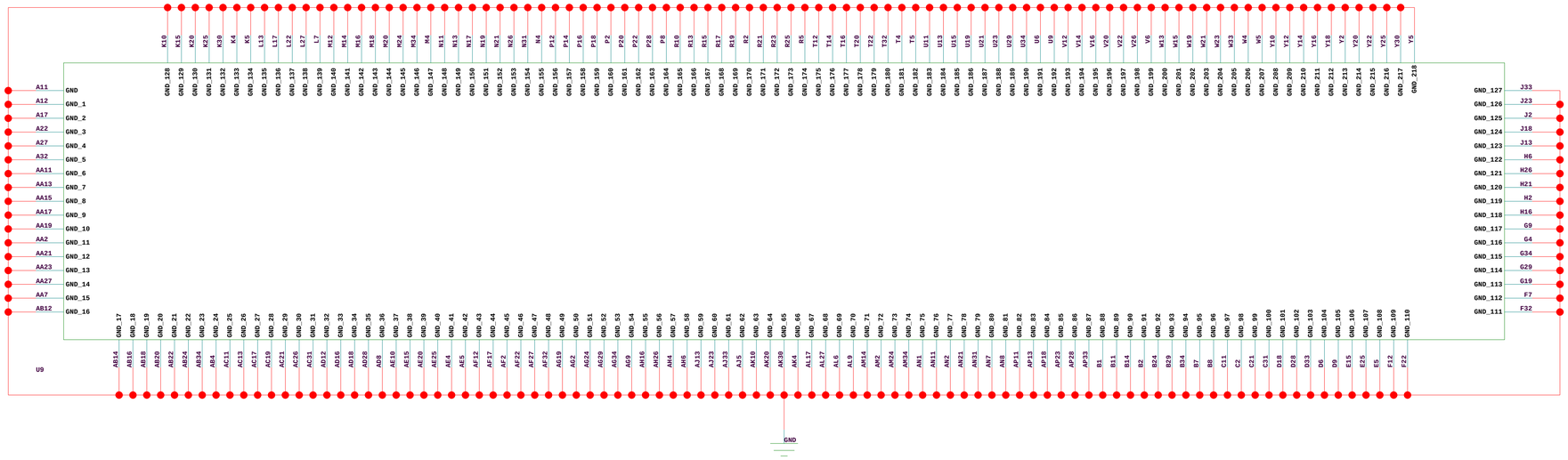

1V0
1V0_53 1V0_52 1V0_51 1V0_50 1V0_49 1V0_48 1V0_47 1V0_46 1V0_45 1V0_44 1V0_43 1V0_42 1V0_41 1V0_40 1V0_39 1V0_38 1V0_37 1V0_36 1V0_35 1V0_34 1V0_33 1V0_32 1V0_31 1V0_30 1V0_29 1V0_28 1V0_27 1V0_26 1V0_25 1V0_24 1V0_23 1V0_22 1V0_21 1V0_20 1V0_19 1V0_18 1V0_17 1V0_16 1V0_15 1V0_14 1V0_13 1V0_12 1V0_11 1V0_10 1V0_9 1V0_8 1V0_7 1V0_6 1V0_5 1V0_4 1V0_3 1V0_2 1V0_1 1V0
U9

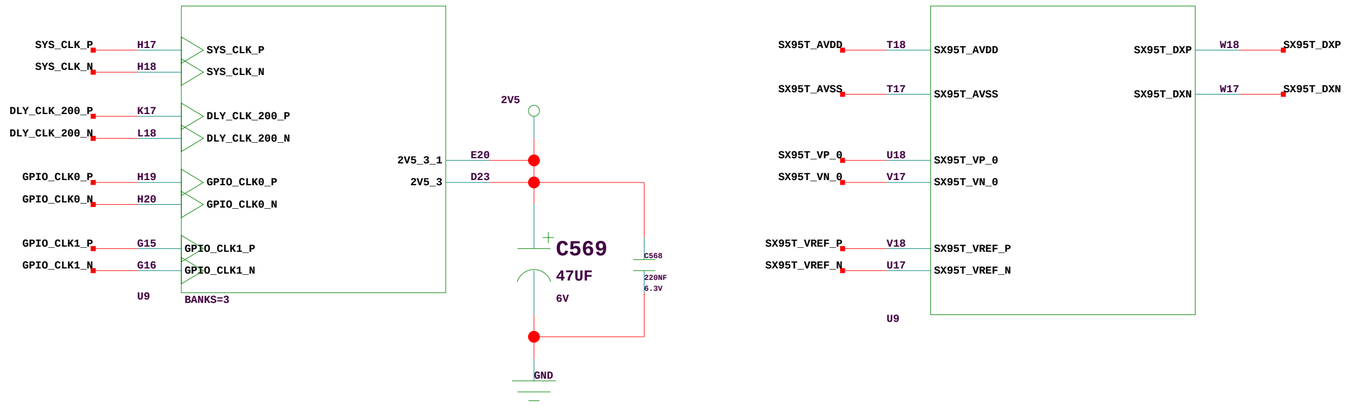

1V0
C628 C629 C627 C616 C615 C617 C619 C618 C620 C625 C626 C624 C622 C623 C621
220NF 6.3V
GND
1V0
C632 C631 C630 C604 C605 C603 C607 C608 C606 C610 C609 C611 C613 C612 C614
GND
1V0
C635 C634 C633 C602 C601 C600 C599 C598 C597 C596 C595 C594 C593 C592 C591
GND


1V0
C644 C643 C642 C641 C640 C639
330UF
2V5
GND


2V5
C637 C636 C638
220NF 6.3V
C645 C646 C647
33UF
6V
GND


2V5
AB11 AC12 L12 M11 M21 P11 P23 T23 U24 V11 Y23 Y23
2V5_AUX 2V5_AUX_1 2V5_AUX_2 2V5_AUX_3 2V5_AUX_4 2V5_AUX_5 2V5_AUX_6 2V5_AUX_7 2V5_AUX_8 2V5_AUX_9 2V5_AUX_10 2V5_AUX_11
U9


K10 K15 K20 K25 K30 K4 K5 L13 L17 L22 L27 L7 M12 M14 M16 M18 M20 M24 M24 M4 N11 N13 N17 N19 N21 N26 N31 N4 P12 P14 P16 P18 P2 P20 P22 P28 P8 R10 R13 R15 R17 R19 R2 R21 R23 R25 R5 T12 T14 T16 T20 T22 T32 T4 T5 U11 U13 U15 U19 U21 U23 U29 U34 U6 U9 V12 V14 V16 V20 V22 V26 V6 W13 W15 W19 W21 W23 W4 W5 Y10 Y12 Y14 Y16 Y18 Y2 Y20 Y22 Y25 Y30 Y5
GND_128 GND_129 GND_130 GND_131 GND_132 GND_133 GND_134 GND_135 GND_136 GND_137 GND_138 GND_139 GND_140 GND_141 GND_142 GND_143 GND_144 GND_145 GND_146 GND_147 GND_148 GND_149 GND_150 GND_151 GND_152 GND_153 GND_154 GND_155 GND_156 GND_157 GND_158 GND_159 GND_160 GND_161 GND_162 GND_163 GND_164 GND_165 GND_166 GND_167 GND_168 GND_169 GND_170 GND_171 GND_172 GND_173 GND_174 GND_175 GND_176 GND_177 GND_178 GND_179 GND_180 GND_181 GND_182 GND_183 GND_184 GND_185 GND_186 GND_187 GND_188 GND_189 GND_190 GND_191 GND_192 GND_193 GND_194 GND_195 GND_196 GND_197 GND_198 GND_199 GND_200 GND_201 GND_202 GND_203 GND_204 GND_205 GND_206 GND_207 GND_208 GND_209 GND_210 GND_211 GND_212 GND_213 GND_214 GND_215 GND_216 GND_217 GND_218
A11 A12 A17 A22 A27 A32 AA11 AA13 AA15 AA17 AA19 AA2 AA21 AA23 AA27 AA7 AB12
GND GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16
GND_127 GND_126 GND_125 GND_124 GND_123 GND_122 GND_121 GND_120 GND_119 GND_118 GND_117 GND_116 GND_115 GND_114 GND_113 GND_112 GND_111
J33 J23 J2 J18 J13 H6 H26 H21 H2 H16 G9 G4 G34 G29 G19 F7 F32
GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_25 GND_26 GND_27 GND_28 GND_29 GND_30 GND_31 GND_32 GND_33 GND_34 GND_35 GND_36 GND_37 GND_38 GND_39 GND_40 GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67 GND_68 GND_69 GND_70 GND_71 GND_72 GND_73 GND_74 GND_75 GND_76 GND_77 GND_78 GND_79 GND_80 GND_81 GND_82 GND_83 GND_84 GND_85 GND_86 GND_87 GND_88 GND_89 GND_90 GND_91 GND_92 GND_93 GND_94 GND_95 GND_96 GND_97 GND_98 GND_99 GND_100 GND_101 GND_102 GND_103 GND_104 GND_105 GND_106 GND_107 GND_108 GND_109 GND_110
AB14 AB16 AB18 AB20 AB22 AB24 AB34 AB4 AC11 AC13 AC17 AC19 AC21 AC26 AC31 AD12 AD16 AD18 AD28 AD8 AE10 AE15 AE20 AE25 AE4 AE5 AF12 AF17 AF2 AF22 AF27 AF32 AG19 AG2 AG24 AG29 AG34 AG9 AH16 AH26 AH4 AH6 AJ13 AJ23 AJ33 AJ5 AK10 AK20 AK30 AK4 AL17 AL27 AL6 AL9 AM14 AM2 AM24 AM34 AN1 AN11 AN2 AN21 AN7 AN8 AP11 AP13 AP18 AP23 AP28 AP33 B1 B11 B14 B2 B24 B29 B34 B7 B8 C11 C2 C21 C31 D18 D28 D3 D6 D9 E15 E25 E5 F12 F22
U9
GND


SYS_CLK_P
H17
SYS_CLK_N
H18
DLY_CLK_200_P
K17
DLY_CLK_200_N
L18
GPIO_CLK0_P
H19
GPIO_CLK0_N
H20
GPIO_CLK1_P
G15
GPIO_CLK1_N
G16
U9
BANKS=3
2V5_3_1
E20
2V5_3
D23
2V5
C569
47UF
6V
C568
220NF
6.3V
GND
SX95T_AVDD
T18
SX95T_AVSS
T17
SX95T_VP_0
U18
SX95T_VN_0
V17
SX95T_VREF_P
V18
SX95T_VREF_N
U17
U9
SX95T_DXP
W18
SX95T_DXN
W17

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
2V5
FB27 220@100M
FB28 220@100M
FB29 220@100M
FB30 220@100M
FB51 220@100M
C454 220NF 6.3V
R238 10K
X2
OE
VCC
OUT+
OUT-
JP23 156.25MHZ
CCLD-023-25-156.250
C413 220NF 6.3V
C412 220NF 6.3V
C411 220NF 6.3V
C410 220NF 6.3V
C422 10NF 25V
C423 10NF 25V
C424 10NF 25V
C425 10NF 25V
C427 10NF 25V
C426 10NF 25V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_120 D5 MGTAVCC_120
MGTAVCC_120_1 F4 MGTAVCC_120_1
MGTAVCCPLL_120 D3 MGTAVCCPLL_120
MGTAVTTRX_120 C3 MGTAVTTRX_120
MGT_120_REF_CLK_P E4 MGT_120_REF_CLK_P
MGT_120_REF_CLK_N D4 MGT_120_REF_CLK_N
MGTRX0_120_P A3 MGTRX0_120_P
MGTRX0_120_N A2 MGTRX0_120_N
MGTRX1_120_P D1 MGTRX1_120_P
MGTRX1_120_N C1 MGTRX1_120_N
MGT_REFCLK_Q2_P
MGT_REFCLK_Q2_N
U9
MGTAVTTTX_120_1 E3 MGTAVTTTX_120_1
MGTAVTTTX_120 C4 MGTAVTTTX_120
MGTTX0_120_P B4 MGTTX0_120_P
MGTTX0_120_N B3 MGTTX0_120_N
MGTTX1_120_P E2 MGTTX1_120_P
MGTTX1_120_N D2 MGTTX1_120_N
MGT_AVTT
FB31 220@100M
FB32 220@100M
C415 220NF 6.3V
C414 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
P6
S39 DL0P
S40 DL0N
S41 DL1P
S42 DL1N
S43 DL2P
S44 DL2N
S45 DL3P
S46 DL3N
S54 SL0P
S53 SL0N
S52 SL1P
S51 SL1N
S50 SL2P
S49 SL2N
S48 SL3P
S47 SL3N
FCN-268F036-G/3DB
SIG_GND1 G20
SIG_GND2 G21
SIG_GND3 G22
SIG_GND4 G23
SIG_GND5 G24
SIG_GND6 G25
SIG_GND7 G26
SIG_GND8 G27
SIG_GND9 G28
SIG_GND10 G19
ODIS
FAULT
R239 10K
C446 10NF 6.3V
C448 10NF 6.3V
JP21
3V3
R229 150R
OPTICAL MODULE FAULT - RED LED
R228 5K1
R227 3K9
R226 6K8
R225 3K9
U44
U43
MAX9032AKA
U45
AND2
SN74AHC1G08DCKR
C447 10NF 6.3V
U41
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
TPS2031D
R224 10K
C445 10NF 6.3V
C444 100NF 6.3V
C408 4.7UF 16V
C406 22UF 16V
GND

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB37 220@100M
FB38 220@100M
FB35 220@100M
FB36 220@100M
C421 220NF 6.3V
C420 220NF 6.3V
C419 220NF 6.3V
C418 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_122 AJ4 MGTAVCC_122
MGTAVCC_122_1 AK5 MGTAVCC_122_1
MGTAVCCPLL_122 AM4 MGTAVCCPLL_122
MGTAVTTRX_122 AL3 MGTAVTTRX_122
MGT_122_REF_CLK_P NC AL5 MGT_122_REF_CLK_P
MGT_122_REF_CLK_N NC AL4 MGT_122_REF_CLK_N
MGTRX0_122_P AL1 MGTRX0_122_P
MGTRX0_122_N AM1 MGTRX0_122_N
MGTRX1_122_P AP3 MGTRX1_122_P
MGTRX1_122_N AP2 MGTRX1_122_N
U9
MGTAVTTTX_122_1 AM3 MGTAVTTTX_122_1
MGTAVTTTX_122 AK3 MGTAVTTTX_122
MGTTX0_122_P AK2 MGTTX0_122_P
MGTTX0_122_N AL2 MGTTX0_122_N
MGTTX1_122_P AN4 MGTTX1_122_P
MGTTX1_122_N AN3 MGTTX1_122_N
FB34 220@100M
FB33 220@100M
C416 220NF 6.3V
C417 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
P6
S55 DL0P
S56 DL0N
S59 DL1P
S60 DL1N
S61 DL2P
S62 DL2N
S63 DL3P
S64 DL3N
S72 SL0P
S71 SL0N
S70 SL1P
S69 SL1N
S68 SL2P
S67 SL2N
S66 SL3P
S65 SL3N
FCN-268F036-G/3DB
SIG_GND1 G29
SIG_GND2 G30
SIG_GND3 G31
SIG_GND4 G32
SIG_GND5 G33
SIG_GND6 G34
SIG_GND7 G35
SIG_GND8 G36
SIG_GND9 G37
SIG_GND10 G19
ODIS
FAULT
R233 10K
C451 10NF 6.3V
C449 10NF 6.3V
JP22
3V3
R232 150R
OPTICAL MODULE FAULT - RED LED
R233 5K1
R234 3K9
R235 6K8
R236 3K9
U44
U43
MAX9032AKA
U46
AND2
SN74AHC1G08DCKR
C450 10NF 6.3V
U42
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
TPS2031D
R237 10K
C452 10NF 6.3V
C453 100NF 6.3V
C409 4.7UF 16V
C407 22UF 16V
GND

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB43 220@100M
FB44 220@100M
FB41 220@100M
FB42 220@100M
C438 220NF 6.3V
C437 220NF 6.3V
C436 220NF 6.3V
C433 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_124 C7 MGTAVCC_124
MGTAVCC_124_1 D7 MGTAVCC_124_1
MGTAVCCPLL_124 C6 MGTAVCCPLL_124
MGTAVTTRX_124 C9 MGTAVTTRX_124
MGT_124_REF_CLK_P NC D8 MGT_124_REF_CLK_P
MGT_124_REF_CLK_N NC C8 MGT_124_REF_CLK_N
MGTRX0_124_P A9 MGTRX0_124_P
MGTRX0_124_N A8 MGTRX0_124_N
MGTRX1_124_P A6 MGTRX1_124_P
MGTRX1_124_N A7 MGTRX1_124_N
U9
MGTAVTTTX_124_1 C5 MGTAVTTTX_124_1
MGTAVTTTX_124 C10 MGTAVTTTX_124
MGTTX0_124_P B10 MGTTX0_124_P
MGTTX0_124_N B9 MGTTX0_124_N
MGTTX1_124_P B5 MGTTX1_124_P
MGTTX1_124_N B6 MGTTX1_124_N
MGT_AVTT
FB40 220@100M
FB39 220@100M
C434 220NF 6.3V
C435 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C428 10NF 25V
C429 10NF 25V
C430 10NF 25V
C431 10NF 25V
P6
S57 DL0P
S58 DL0N
S59 DL1P
S60 DL1N
S61 DL2P
S62 DL2N
S63 DL3P
S64 DL3N
S72 SL0P
S71 SL0N
S70 SL1P
S69 SL1N
S68 SL2P
S67 SL2N
S66 SL3P
S65 SL3N
FCN-268F036-G/3DB
SIG_GND1 G29
SIG_GND2 G30
SIG_GND3 G31
SIG_GND4 G32
SIG_GND5 G33
SIG_GND6 G34
SIG_GND7 G35
SIG_GND8 G36
SIG_GND9 G37
SIG_GND10 G19
ODIS
FAULT
R231 10K
C451 10NF 6.3V
C449 10NF 6.3V
JP22
3V3
R232 150R
OPTICAL MODULE FAULT - RED LED
R233 5K1
R234 3K9
R235 6K8
R236 3K9
U44
U43
MAX9032AKA
U46
AND2
SN74AHC1G08DCKR
C450 10NF 6.3V
U42
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
TPS2031D
R237 10K
C452 10NF 6.3V
C453 100NF 6.3V
C409 4.7UF 16V
C407 22UF 16V
GND

PADD[2:31]

U1
External Slave Peripheral

External Master Peripheral Interface

U9
BANKS=1, 2, 4
CHIP SELECT 1

U1
UART
IIC0
IIC1_SPI
NAND Flash Interface

U32
32MX16 MOBILE DDR
FLASH 32MX16 4M4B

U28 U29 U30 U31 AT24C64

U33 U34 ICL3225ECA

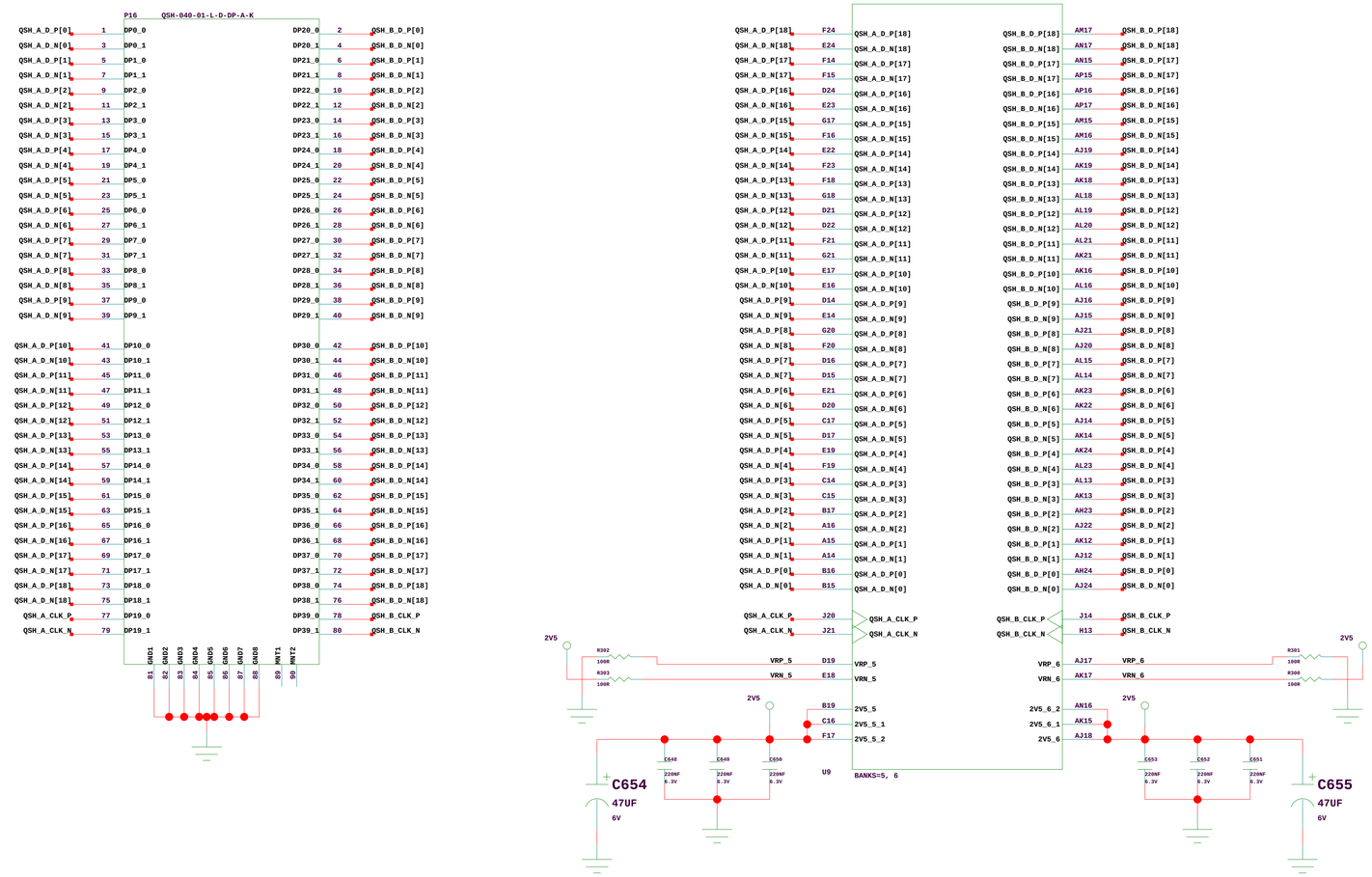
U35 U36 U37 U38 P15SA3157

P8
9P DSUB MALE

J7
HLE-105-02-G-DV

To Boot from NAND, install jumper

NO POP


P16 QSH-040-01-L-D-DP-A-K
QSH_A_D_P[0] 1 DP0_0
QSH_A_D_N[0] 3 DP0_1
QSH_A_D_P[1] 5 DP1_0
QSH_A_D_N[1] 7 DP1_1
QSH_A_D_P[2] 9 DP2_0
QSH_A_D_N[2] 11 DP2_1
QSH_A_D_P[3] 13 DP3_0
QSH_A_D_N[3] 15 DP3_1
QSH_A_D_P[4] 17 DP4_0
QSH_A_D_N[4] 19 DP4_1
QSH_A_D_P[5] 21 DP5_0
QSH_A_D_N[5] 23 DP5_1
QSH_A_D_P[6] 25 DP6_0
QSH_A_D_N[6] 27 DP6_1
QSH_A_D_P[7] 29 DP7_0
QSH_A_D_N[7] 31 DP7_1
QSH_A_D_P[8] 33 DP8_0
QSH_A_D_N[8] 35 DP8_1
QSH_A_D_P[9] 37 DP9_0
QSH_A_D_N[9] 39 DP9_1
QSH_A_D_P[10] 41 DP10_0
QSH_A_D_N[10] 43 DP10_1
QSH_A_D_P[11] 45 DP11_0
QSH_A_D_N[11] 47 DP11_1
QSH_A_D_P[12] 49 DP12_0
QSH_A_D_N[12] 51 DP12_1
QSH_A_D_P[13] 53 DP13_0
QSH_A_D_N[13] 55 DP13_1
QSH_A_D_P[14] 57 DP14_0
QSH_A_D_N[14] 59 DP14_1
QSH_A_D_P[15] 61 DP15_0
QSH_A_D_N[15] 63 DP15_1
QSH_A_D_P[16] 65 DP16_0
QSH_A_D_N[16] 67 DP16_1
QSH_A_D_P[17] 69 DP17_0
QSH_A_D_N[17] 71 DP17_1
QSH_A_D_P[18] 73 DP18_0
QSH_A_D_N[18] 75 DP18_1
QSH_A_CLK_P 77 DP19_0
QSH_A_CLK_N 79 DP19_1
DP20_0 2 QSH_B_D_P[0]
DP20_1 4 QSH_B_D_N[0]
DP21_0 6 QSH_B_D_P[1]
DP21_1 8 QSH_B_D_N[1]
DP22_0 10 QSH_B_D_P[2]
DP22_1 12 QSH_B_D_N[2]
DP23_0 14 QSH_B_D_P[3]
DP23_1 16 QSH_B_D_N[3]
DP24_0 18 QSH_B_D_P[4]
DP24_1 20 QSH_B_D_N[4]
DP25_0 22 QSH_B_D_P[5]
DP25_1 24 QSH_B_D_N[5]
DP26_0 26 QSH_B_D_P[6]
DP26_1 28 QSH_B_D_N[6]
DP27_0 30 QSH_B_D_P[7]
DP27_1 32 QSH_B_D_N[7]
DP28_0 34 QSH_B_D_P[8]
DP28_1 36 QSH_B_D_N[8]
DP29_0 38 QSH_B_D_P[9]
DP29_1 40 QSH_B_D_N[9]
DP30_0 42 QSH_B_D_P[10]
DP30_1 44 QSH_B_D_N[10]
DP31_0 46 QSH_B_D_P[11]
DP31_1 48 QSH_B_D_N[11]
DP32_0 50 QSH_B_D_P[12]
DP32_1 52 QSH_B_D_N[12]
DP33_0 54 QSH_B_D_P[13]
DP33_1 56 QSH_B_D_N[13]
DP34_0 58 QSH_B_D_P[14]
DP34_1 60 QSH_B_D_N[14]
DP35_0 62 QSH_B_D_P[15]
DP35_1 64 QSH_B_D_N[15]
DP36_0 66 QSH_B_D_P[16]
DP36_1 68 QSH_B_D_N[16]
DP37_0 70 QSH_B_D_P[17]
DP37_1 72 QSH_B_D_N[17]
DP38_0 74 QSH_B_D_P[18]
DP38_1 76 QSH_B_D_N[18]
DP39_0 78 QSH_B_CLK_P
DP39_1 80 QSH_B_CLK_N
GND1 81
GND2 82
GND3 83
GND4 84
GND5 85
GND6 86
GND7 87
GND8 88
MH1 89
MH2 90
QSH_A_D_P[18] F24 QSH_A_D_P[18]
QSH_A_D_N[18] E24 QSH_A_D_N[18]
QSH_A_D_P[17] F14 QSH_A_D_P[17]
QSH_A_D_N[17] F15 QSH_A_D_N[17]
QSH_A_D_P[16] D24 QSH_A_D_P[16]
QSH_A_D_N[16] E23 QSH_A_D_N[16]
QSH_A_D_P[15] G17 QSH_A_D_P[15]
QSH_A_D_N[15] F16 QSH_A_D_N[15]
QSH_A_D_P[14] E22 QSH_A_D_P[14]
QSH_A_D_N[14] F23 QSH_A_D_N[14]
QSH_A_D_P[13] F18 QSH_A_D_P[13]
QSH_A_D_N[13] G18 QSH_A_D_N[13]
QSH_A_D_P[12] D21 QSH_A_D_P[12]
QSH_A_D_N[12] D22 QSH_A_D_N[12]
QSH_A_D_P[11] F21 QSH_A_D_P[11]
QSH_A_D_N[11] G21 QSH_A_D_N[11]
QSH_A_D_P[10] E17 QSH_A_D_P[10]
QSH_A_D_N[10] E16 QSH_A_D_N[10]
QSH_A_D_P[9] D14 QSH_A_D_P[9]
QSH_A_D_N[9] E14 QSH_A_D_N[9]
QSH_A_D_P[8] G20 QSH_A_D_P[8]
QSH_A_D_N[8] F20 QSH_A_D_N[8]
QSH_A_D_P[7] D16 QSH_A_D_P[7]
QSH_A_D_N[7] D15 QSH_A_D_N[7]
QSH_A_D_P[6] E21 QSH_A_D_P[6]
QSH_A_D_N[6] D20 QSH_A_D_N[6]
QSH_A_D_P[5] C17 QSH_A_D_P[5]
QSH_A_D_N[5] D17 QSH_A_D_N[5]
QSH_A_D_P[4] E19 QSH_A_D_P[4]
QSH_A_D_N[4] F19 QSH_A_D_N[4]
QSH_A_D_P[3] C14 QSH_A_D_P[3]
QSH_A_D_N[3] C15 QSH_A_D_N[3]
QSH_A_D_P[2] B17 QSH_A_D_P[2]
QSH_A_D_N[2] A16 QSH_A_D_N[2]
QSH_A_D_P[1] A15 QSH_A_D_P[1]
QSH_A_D_N[1] A14 QSH_A_D_N[1]
QSH_A_D_P[0] B16 QSH_A_D_P[0]
QSH_A_D_N[0] B15 QSH_A_D_N[0]
QSH_A_CLK_P J20 QSH_A_CLK_P
QSH_A_CLK_N J21 QSH_A_CLK_N
VRP_5 D19 VRP_5
VRN_5 E18 VRN_5
B19 2V5_5
C16 2V5_5_1
F17 2V5_5_2
U9
BANKS=5, 6
QSH_B_D_P[18] AM17 QSH_B_D_P[18]
QSH_B_D_N[18] AN17 QSH_B_D_N[18]
QSH_B_D_P[17] AN15 QSH_B_D_P[17]
QSH_B_D_N[17] AP15 QSH_B_D_N[17]
QSH_B_D_P[16] AP16 QSH_B_D_P[16]
QSH_B_D_N[16] AP17 QSH_B_D_N[16]
QSH_B_D_P[15] AM15 QSH_B_D_P[15]
QSH_B_D_N[15] AM16 QSH_B_D_N[15]
QSH_B_D_P[14] AJ19 QSH_B_D_P[14]
QSH_B_D_N[14] AK19 QSH_B_D_N[14]
QSH_B_D_P[13] AK18 QSH_B_D_P[13]
QSH_B_D_N[13] AL18 QSH_B_D_N[13]
QSH_B_D_P[12] AL19 QSH_B_D_P[12]
QSH_B_D_N[12] AL20 QSH_B_D_N[12]
QSH_B_D_P[11] AL21 QSH_B_D_P[11]
QSH_B_D_N[11] AK21 QSH_B_D_N[11]
QSH_B_D_P[10] AK16 QSH_B_D_P[10]
QSH_B_D_N[10] AL16 QSH_B_D_N[10]
QSH_B_D_P[9] AJ16 QSH_B_D_P[9]
QSH_B_D_N[9] AJ15 QSH_B_D_N[9]
QSH_B_D_P[8] AJ21 QSH_B_D_P[8]
QSH_B_D_N[8] AJ20 QSH_B_D_N[8]
QSH_B_D_P[7] AL15 QSH_B_D_P[7]
QSH_B_D_N[7] AL14 QSH_B_D_N[7]
QSH_B_D_P[6] AK23 QSH_B_D_P[6]
QSH_B_D_N[6] AK22 QSH_B_D_N[6]
QSH_B_D_P[5] AJ14 QSH_B_D_P[5]
QSH_B_D_N[5] AK14 QSH_B_D_N[5]
QSH_B_D_P[4] AK24 QSH_B_D_P[4]
QSH_B_D_N[4] AL23 QSH_B_D_N[4]
QSH_B_D_P[3] AL13 QSH_B_D_P[3]
QSH_B_D_N[3] AK13 QSH_B_D_N[3]
QSH_B_D_P[2] AH23 QSH_B_D_P[2]
QSH_B_D_N[2] AJ22 QSH_B_D_N[2]
QSH_B_D_P[1] AK12 QSH_B_D_P[1]
QSH_B_D_N[1] AJ12 QSH_B_D_N[1]
QSH_B_D_P[0] AH24 QSH_B_D_P[0]
QSH_B_D_N[0] AJ24 QSH_B_D_N[0]
QSH_B_CLK_P J14 QSH_B_CLK_P
QSH_B_CLK_N H13 QSH_B_CLK_N
VRP_6 AJ17 VRP_6
VRN_6 AK17 VRN_6
AN16 2V5_6_2
AK15 2V5_6_1
AJ18 2V5_6
2V5
R302 100R
R303 100R
R301 100R
R300 100R
C648 220NF 6.3V
C649 220NF 6.3V
C650 220NF 6.3V
C653 220NF 6.3V
C652 220NF 6.3V
C651 220NF 6.3V
C654 47UF 6V
C655 47UF 6V