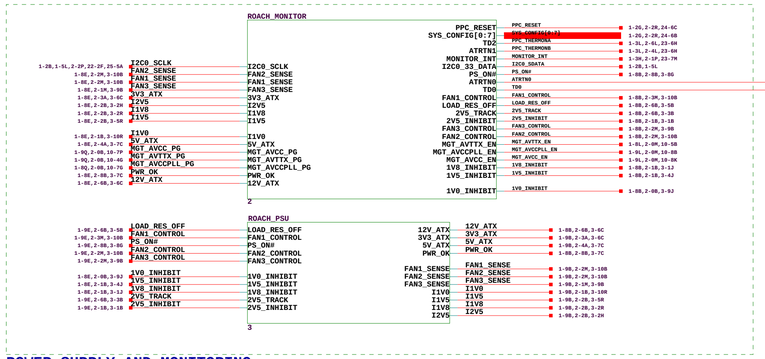
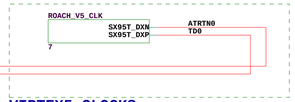
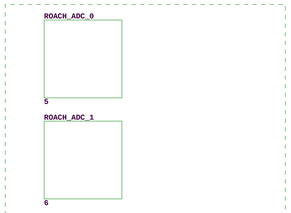
VIRTEX5



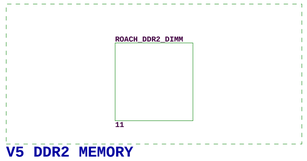
POWER SUPPLY AND MONITORING



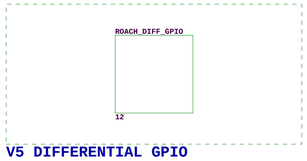
VIRTEX5 CLOCKS



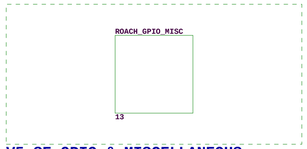
ZDOK/ADC INTERFACE



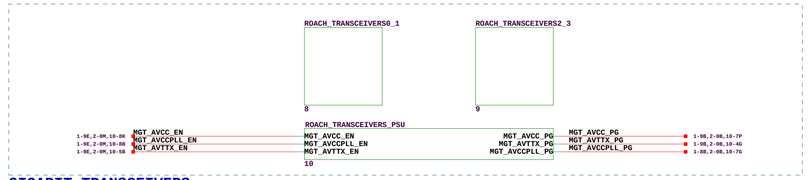
V5 DDR2 MEMORY



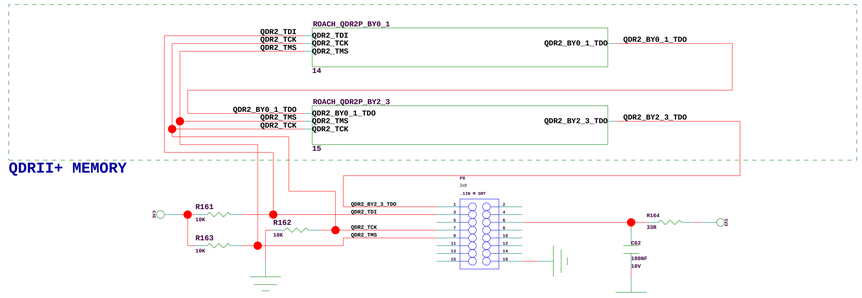
V5 DIFFERENTIAL GPIO



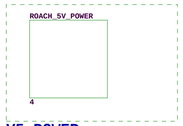
V5 SE GPIO & MISCELLANEOUS



GIGABIT TRANSCEIVERS



QDRII+ MEMORY

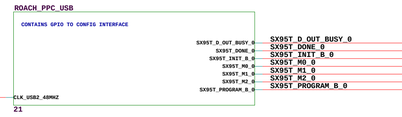


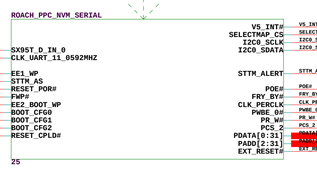
V5 POWER

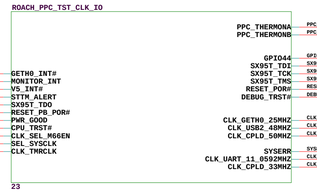
VIRTEX5 CONFIGURATION

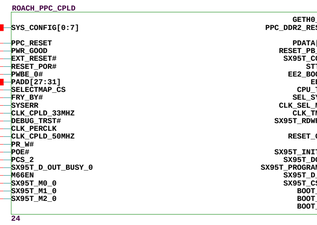
V5 SE GPIO & MISCELLANEOUS

PPC









MECHANICAL

BOARD FIDUCIALS

LOGO'S

PLACEHOLDER FOR PCB
MEERKAT LOGO

PLACEHOLDER FOR PCB
CASPER LOGO

PLACEHOLDER FOR PCB
ROACH LOGO

PLACEHOLDER FOR PCB
NRAO LOGO

BOARD SERIAL NUMBER

CONTRIBUTORS

ETIENNE BAUERMEISTER
HENRY CHEN
STEVE DURAND
FRANCOIS KAPP
ALAN LANGMAN
GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2	ROACH_TOP
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-18-2008_23:38	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 1 OF 25

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

TIE TO GROUND IF PLL'S ARE NOT USED

PLACE AT ACTEL 3V3 POWER PINS

PLACE AT ACTEL 1V5 POWER PINS

roach_AFS600_powerpins

roach_AFS600_configpins

roach_AFS600_pcb

PB POWER SWITCH

KEY - REMOVE PIN

MONITOR RESET

XPORT - PLACE IN REAR I/O REGION

TEMPERATURE DIODE HEADER

ACTEL JTAG CONNECTOR

SPARE ANALOG VOLTAGE INPUT #0

SPARE ANALOG VOLTAGE INPUT #1

SPARE GATE DRIVE OUTPUT #0

SPARE GATE DRIVE OUTPUT #1

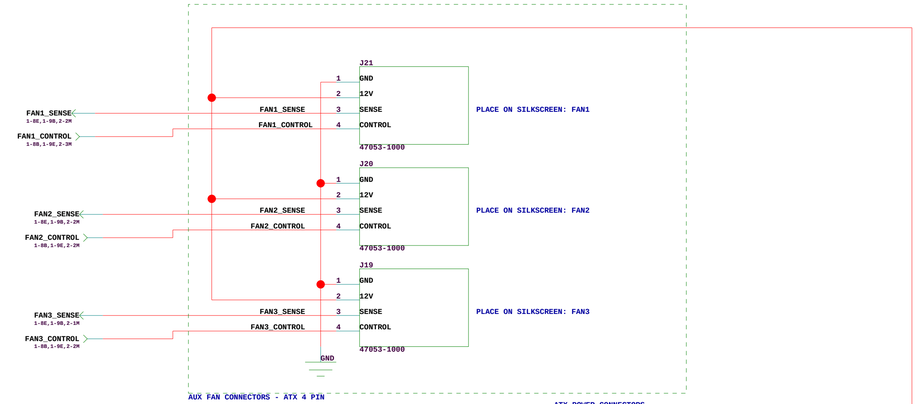
REFERENCE RESISTOR/ADC VALUES

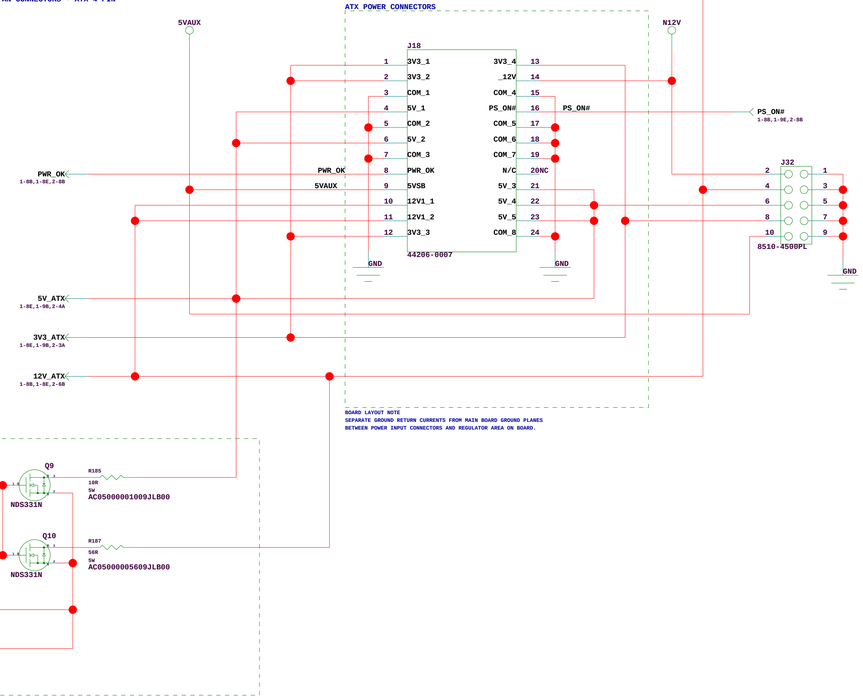
VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)
12V	0R01	3.36	0.11
5V	0R0047	6.78	0.22
3V3	0R01	3.47	0.12
2V5	0R01	3.56	0.13
1V8	0R0022	12.91	0.37
1V5	0R0047	6.77	0.22
1V0	0R01	26.79	0.72

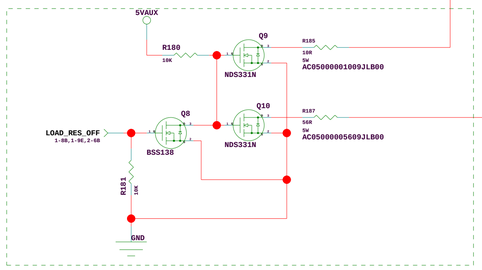
FOR 8 BIT ADC USING 2.56V REFERENCE:

ADC COUNT AT MAX POWER	CURRENT/BIT (A)
33	0.1
31	0.21
34	0.1
35	0.1
28	0.45
31	0.21
26	1.0

ROACH/iBOB2	ROACH_MONITOR
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
6-18-2008_23:38	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 2 OF 25

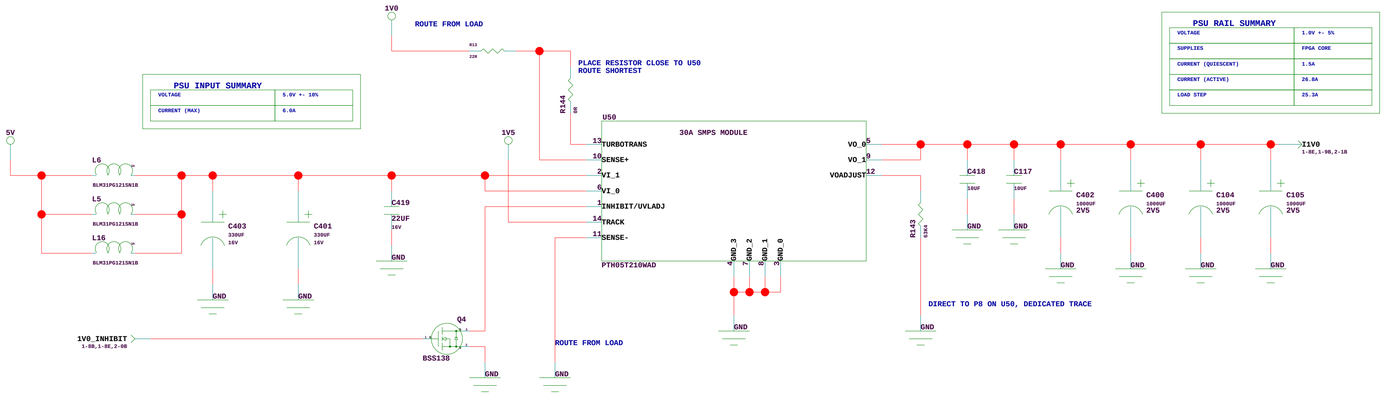






LOAD RESISTORS FOR ATX PSU MIN LOAD
SWITCH OFF ONCE LOAD EXCEEDS MINIMUM SPEC
ADJUST RESISTOR VALUES FOR ACTUAL SUPPLY

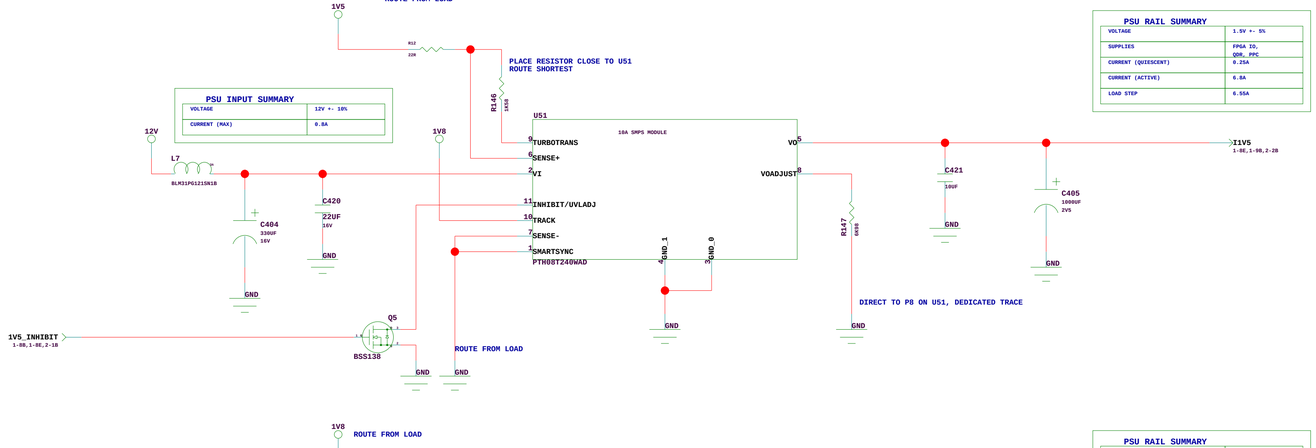
BOARD LAYOUT NOTE
SEPARATE GROUND RETURN CURRENTS FROM MAIN BOARD GROUND PLANES
BETWEEN POWER INPUT CONNECTORS AND REGULATOR AREA ON BOARD.



PSU INPUT SUMMARY	
VOLTAGE	5.0V +- 10%
CURRENT (MAX)	6.0A

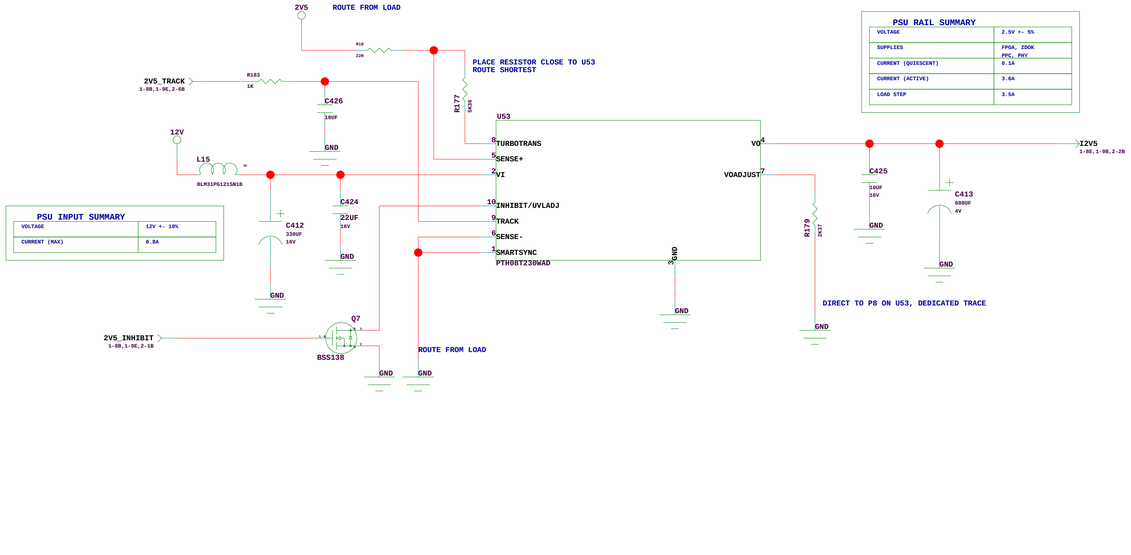
PSU RAIL SUMMARY	
VOLTAGE	1.0V +- 5%
SUPPLIES	FPGA CORE
CURRENT (QUIESCENT)	1.5A
CURRENT (ACTIVE)	26.8A
LOAD STEP	25.3A

1.2V SUPPLY DELETED - NOT REQUIRED



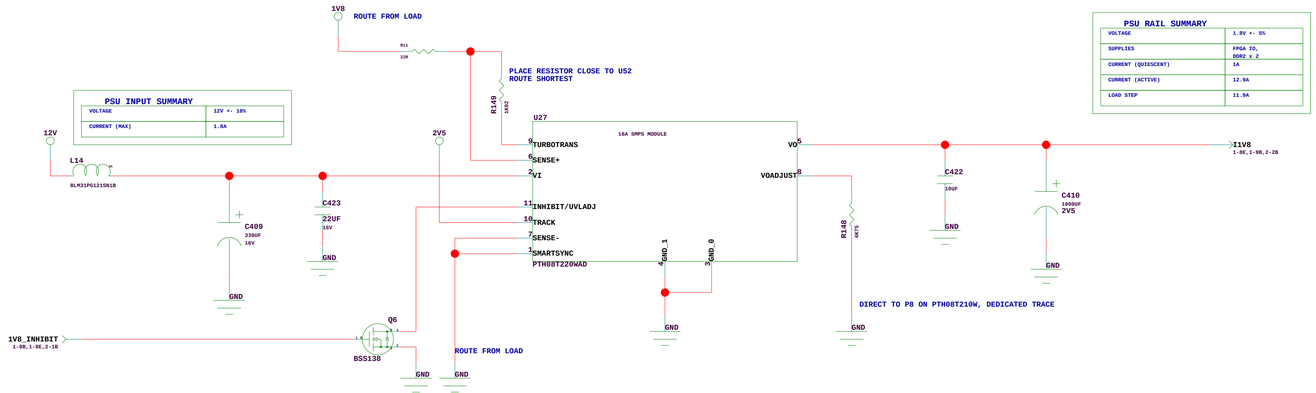
PSU INPUT SUMMARY	
VOLTAGE	12V +- 10%
CURRENT (MAX)	0.8A

PSU RAIL SUMMARY	
VOLTAGE	1.5V +- 5%
SUPPLIES	FPGA IO, QDR, PPC
CURRENT (QUIESCENT)	0.25A
CURRENT (ACTIVE)	6.8A
LOAD STEP	6.55A



PSU INPUT SUMMARY	
VOLTAGE	12V +- 10%
CURRENT (MAX)	0.8A

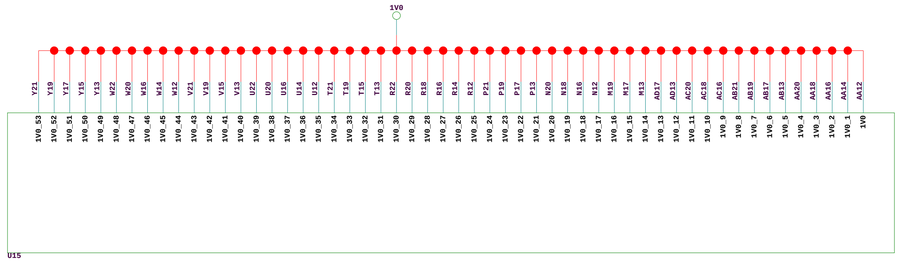
PSU RAIL SUMMARY	
VOLTAGE	2.5V +- 5%
SUPPLIES	FPGA, ZDOK PPC, PHY
CURRENT (QUIESCENT)	0.1A
CURRENT (ACTIVE)	3.6A
LOAD STEP	3.5A

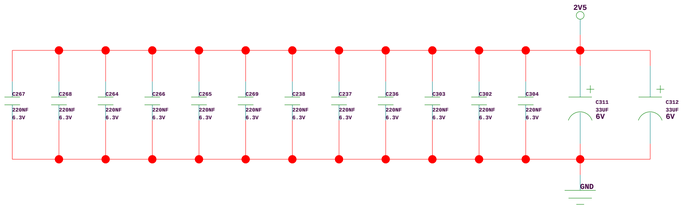


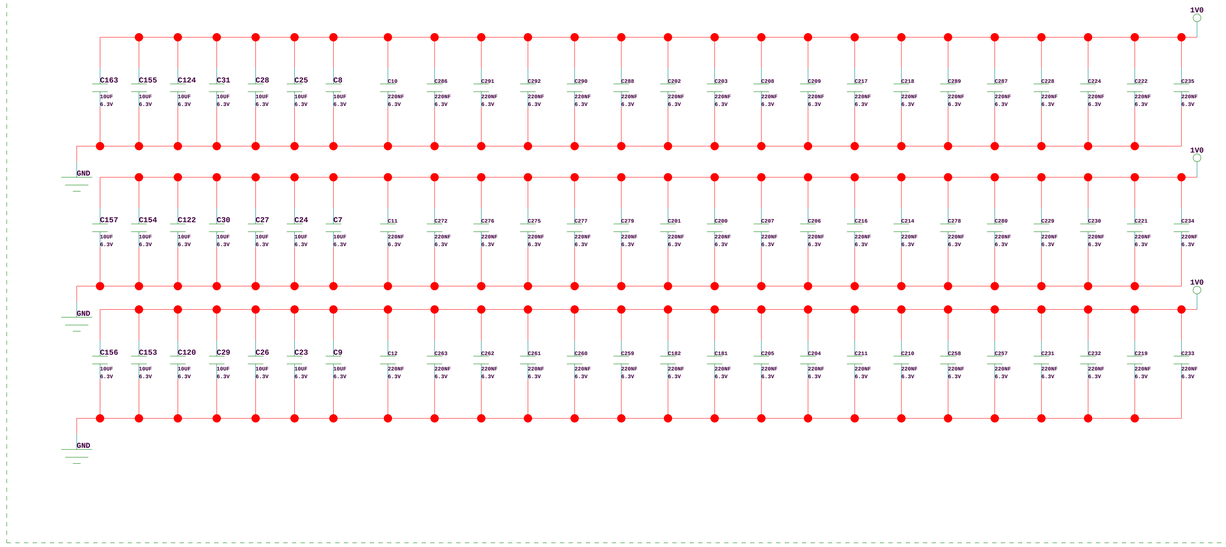
PSU INPUT SUMMARY	
VOLTAGE	12V +- 10%
CURRENT (MAX)	1.8A

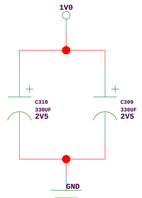
PSU RAIL SUMMARY	
VOLTAGE	1.8V +- 5%
SUPPLIES	FPGA IO, DDR2 x 2
CURRENT (QUIESCENT)	1A
CURRENT (ACTIVE)	12.9A
LOAD STEP	11.9A

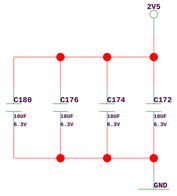
ROACH/iBOB2	ROACH_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-18-2008_23:38	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 3 OF 25

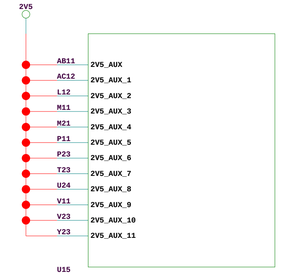


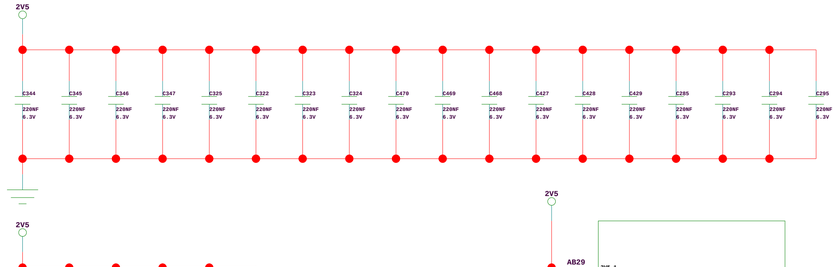


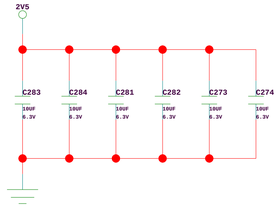


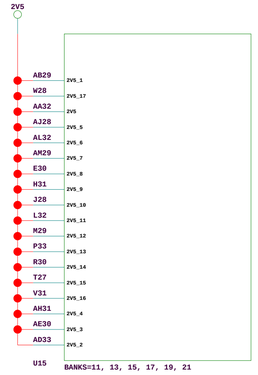


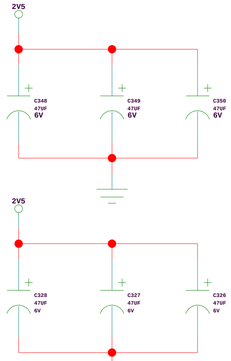


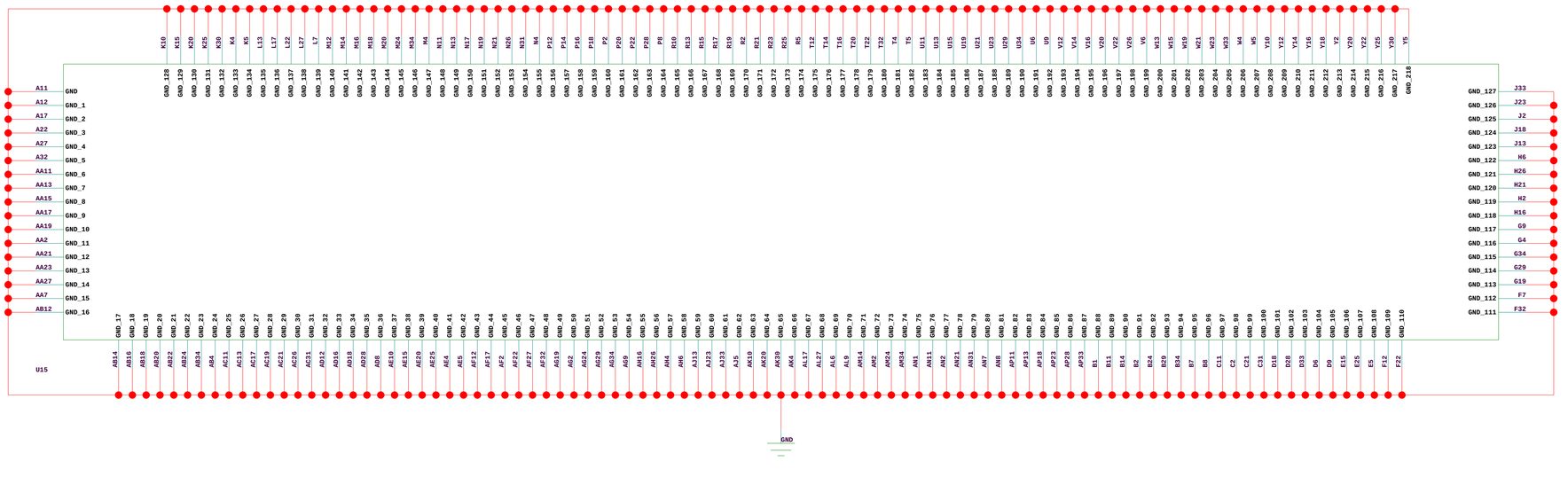








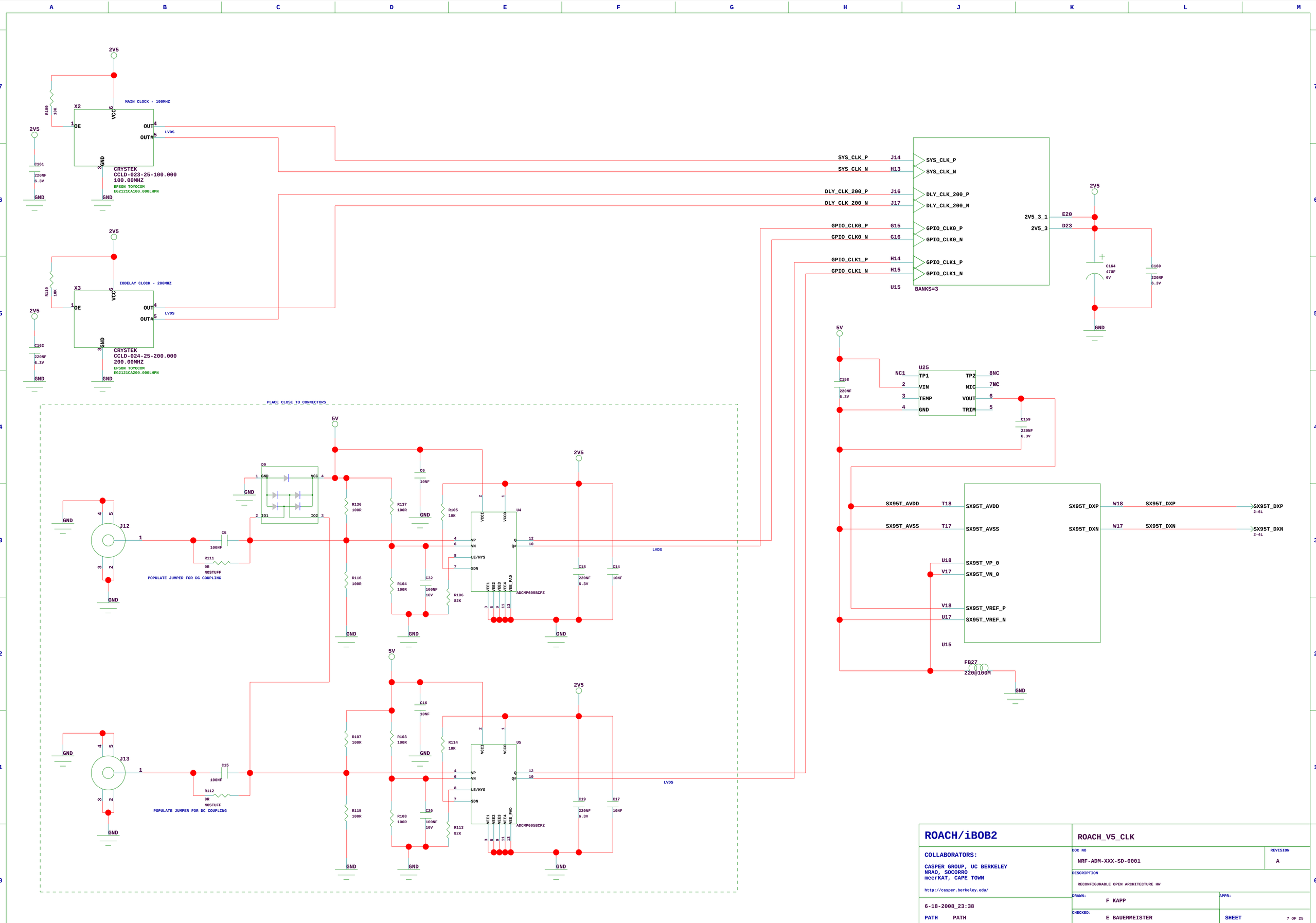




ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
6-18-2008_23:38 PATH PATH	

| | | |

ROACH/iBOB2	**ROACH_ADC_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 6 OF 25
6-18-2008_23:38 PATH PATH	



ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

6-18-2008_23:38

PATH PATH

ROACH_V5_CLK

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

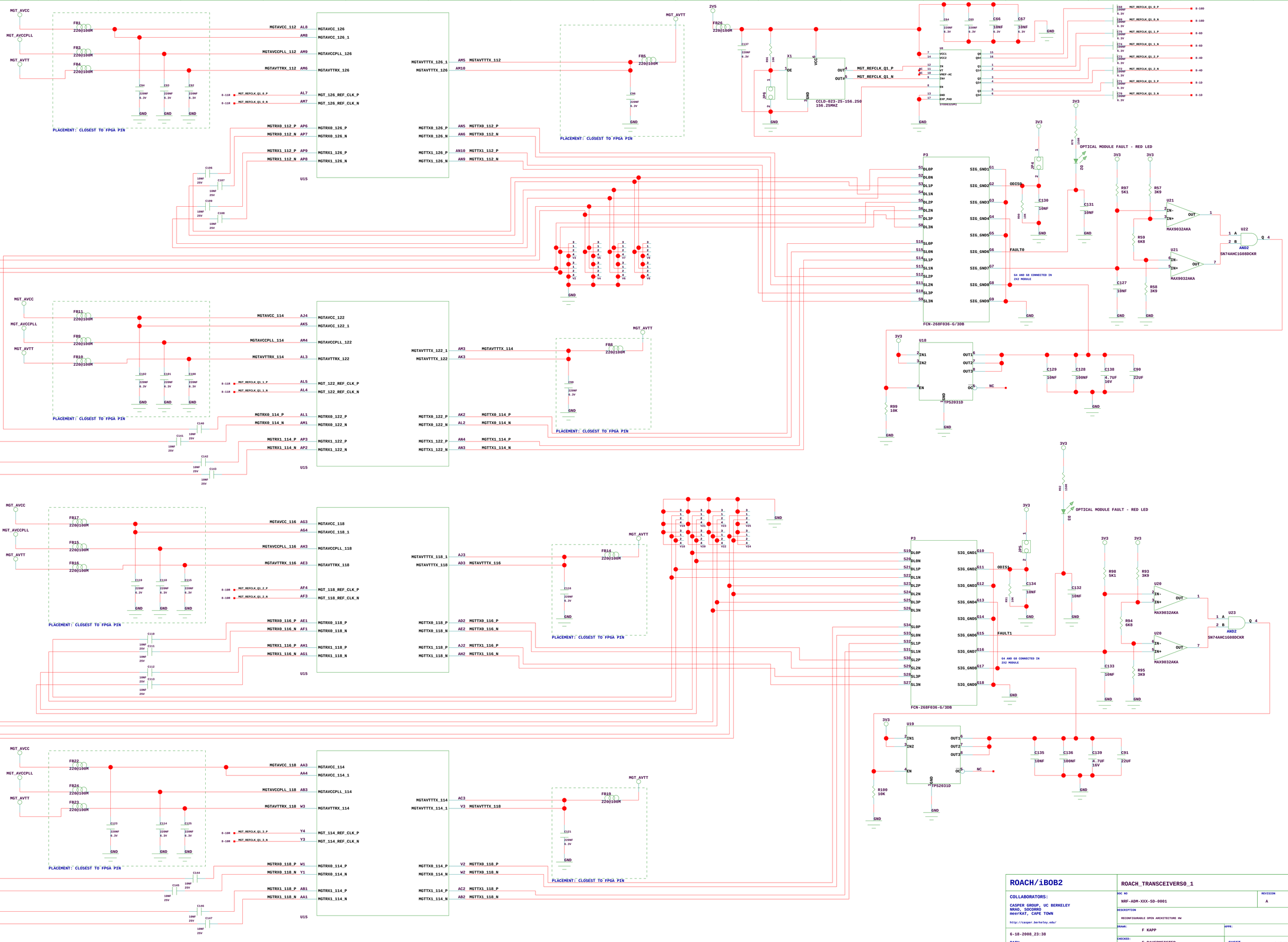
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 7 OF 25


MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB3 220@100M
FB4 220@100M
C84 220NF 6.3V
C93 220NF 6.3V
C92 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_112 AL8 MGTAVCC_126
AM8 MGTAVCC_126_1
MGTAVCCPLL_112 AM9 MGTAVCCPLL_126
MGTAVTTRX_112 AM6 MGTAVTTRX_126
B-11R MGT_REFCLK_Q1_0_P AL7 MGT_126_REF_CLK_P
B-11R MGT_REFCLK_Q1_0_N AM7 MGT_126_REF_CLK_N
MGTRX0_112_P AP6 MGTRX0_126_P
MGTRX0_112_N AP7 MGTRX0_126_N
MGTRX1_112_P AP9 MGTRX1_126_P
MGTRX1_112_N AP8 MGTRX1_126_N
U15
MGTAVTTTX_126_1 AM5 MGTAVTTTX_112
MGTAVTTTX_126 AM10
MGTTX0_126_P AN5 MGTTX0_112_P
MGTTX0_126_N AN6 MGTTX0_112_N
MGTTX1_126_P AN10 MGTTX1_112_P
MGTTX1_126_N AN9 MGTTX1_112_N
MGT_AVTT
FB5 220@100M
C96 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C106 10NF 25V
C107 10NF 25V
C109 10NF 25V
C108 10NF 25V
2V5
FB26 220@100M
C137 220NF 6.3V
R84 10K
X1 CCLD-023-25-156.250 156.25MHZ
JP6
OE
VCC
OUT
GND
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
U8 SY89832UMI
VCC1 VCC2 IN VT VREF-AC /IN EN GND EXP_PAD
Q0 /Q0 Q1 /Q1 Q2 /Q2 Q3 /Q3
C64 220NF 6.3V
C65 220NF 6.3V
C66 10NF 6.3V
C67 10NF 6.3V
C68 100NF 6.3V MGT_REFCLK_Q1_0_P B-10D
C69 100NF 6.3V MGT_REFCLK_Q1_0_N B-10D
C75 100NF 6.3V MGT_REFCLK_Q1_1_P B-6D
C74 100NF 6.3V MGT_REFCLK_Q1_1_N B-6D
C73 100NF 6.3V MGT_REFCLK_Q1_2_P B-4D
C72 100NF 6.3V MGT_REFCLK_Q1_2_N B-4D
C71 100NF 6.3V MGT_REFCLK_Q1_3_P B-1D
C70 100NF 6.3V MGT_REFCLK_Q1_3_N B-1D
P3
FCN-268F036-G/3DB
S1 DL0P
S2 DL0N
S3 DL1P
S4 DL1N
S5 DL2P
S6 DL2N
S7 DL3P
S8 DL3N
S16 SL0P
S15 SL0N
S14 SL1P
S13 SL1N
S12 SL2P
S11 SL2N
S10 SL3P
S9 SL3N
SIG_GND1 G1
SIG_GND2 G2
SIG_GND3 G3
SIG_GND4 G4
SIG_GND5 G5
SIG_GND6 G6
SIG_GND7 G7
SIG_GND8 G8
SIG_GND9 G9
ODIS0
FAULT0
G4 AND G8 CONNECTED IN 2X2 MODULE
3V3
JP4
R85 10K
C130 10NF
C131 10NF
R79 100R
D2
OPTICAL MODULE FAULT - RED LED
R97 5K1
RS7 3K9
U21 MAX9032AKA
R59 6K8
U21 MAX9032AKA
U22 SN74AHC1G08DCKR AND2
RS8 3K9
C127 10NF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB11 220@100M
FB9 220@100M
FB10 220@100M
C102 220NF 6.3V
C101 220NF 6.3V
C100 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_114 AJ4 MGTAVCC_122
AK5 MGTAVCC_122_1
MGTAVCCPLL_114 AM4 MGTAVCCPLL_122
MGTAVTTRX_114 AL3 MGTAVTTRX_122
B-11R MGT_REFCLK_Q3_1_P AL5 MGT_122_REF_CLK_P
B-11R MGT_REFCLK_Q3_1_N AL4 MGT_122_REF_CLK_N
MGTRX0_114_P AL1 MGTRX0_122_P
MGTRX0_114_N AM1 MGTRX0_122_N
MGTRX1_114_P AP3 MGTRX1_122_P
MGTRX1_114_N AP2 MGTRX1_122_N
U15
MGTAVTTTX_122_1 AM3 MGTAVTTTX_114
MGTAVTTTX_122 AK3
MGTTX0_122_P AK2 MGTTX0_114_P
MGTTX0_122_N AL2 MGTTX0_114_N
MGTTX1_122_P AN4 MGTTX1_114_P
MGTTX1_122_N AN3 MGTTX1_114_N
FB8 220@100M
C99 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C140 10NF 25V
C141 10NF 25V
C142 10NF 25V
C143 10NF 25V
3V3
U18 TPS2031D
IN1 IN2 EN GND OUT1 OUT2 OUT3 OC NC
R99 10K
C129 10NF
C128 100NF
C138 4.7UF 16V
C90 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB17 220@100M
FB15 220@100M
FB16 220@100M
C119 220NF 6.3V
C118 220NF 6.3V
C115 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_116 AG3 MGTAVCC_118
AG4 MGTAVCC_118_1
MGTAVCCPLL_116 AH3 MGTAVCCPLL_118
MGTAVTTRX_116 AE3 MGTAVTTRX_118
B-10R MGT_REFCLK_Q3_2_P AF4 MGT_118_REF_CLK_P
B-10R MGT_REFCLK_Q3_2_N AF3 MGT_118_REF_CLK_N
MGTRX0_116_P AE1 MGTRX0_118_P
MGTRX0_116_N AF1 MGTRX0_118_N
MGTRX1_116_P AH1 MGTRX1_118_P
MGTRX1_116_N AG1 MGTRX1_118_N
U15
MGTAVTTTX_118_1 AJ3
MGTAVTTTX_118 AD3 MGTAVTTTX_116
MGTTX0_118_P AD2 MGTTX0_116_P
MGTTX0_118_N AE2 MGTTX0_116_N
MGTTX1_118_P AJ2 MGTTX1_116_P
MGTTX1_118_N AH2 MGTTX1_116_N
FB14 220@100M
C110 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C110 10NF 25V
C111 10NF 25V
C112 10NF 25V
C113 10NF 25V
P3
FCN-268F036-G/3DB
S19 DL6P
S20 DL6N
S21 DL7P
S22 DL7N
S23 DL2P
S24 DL2N
S25 DL3P
S26 DL3N
S34 SL6P
S33 SL6N
S32 SL1P
S31 SL1N
S30 SL2P
S29 SL2N
S28 SL3P
S27 SL3N
SIG_GND1 G10
SIG_GND2 G11
SIG_GND3 G12
SIG_GND4 G13
SIG_GND5 G14
SIG_GND6 G15
SIG_GND7 G16
SIG_GND8 G17
SIG_GND9 G18
ODIS1
FAULT1
G4 AND G8 CONNECTED IN 2X2 MODULE
3V3
JP5
R91 10K
C134 10NF
R82 100R
D3
OPTICAL MODULE FAULT - RED LED
R98 5K1
R93 3K9
U20 MAX9032AKA
R94 6K8
U20 MAX9032AKA
U23 SN74AHC1G08DCKR AND2
R95 3K9
C132 10NF
C133 10NF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB22 220@100M
FB24 220@100M
FB23 220@100M
C123 220NF 6.3V
C114 220NF 6.3V
C125 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_118 AA3 MGTAVCC_114
AA4 MGTAVCC_114_1
MGTAVCCPLL_118 AB3 MGTAVCCPLL_114
MGTAVTTRX_118 W3 MGTAVTTRX_114
B-10R MGT_REFCLK_Q3_3_P Y4 MGT_114_REF_CLK_P
B-10R MGT_REFCLK_Q3_3_N Y3 MGT_114_REF_CLK_N
MGTRX0_118_P W1 MGTRX0_114_P
MGTRX0_118_N Y1 MGTRX0_114_N
MGTRX1_118_P AB1 MGTRX1_114_P
MGTRX1_118_N AA1 MGTRX1_114_N
U15
MGTAVTTTX_114 AC3
MGTAVTTTX_114_1 V3 MGTAVTTTX_118
MGTTX0_114_P V2 MGTTX0_118_P
MGTTX0_114_N W2 MGTTX0_118_N
MGTTX1_114_P AC2 MGTTX1_118_P
MGTTX1_114_N AB2 MGTTX1_118_N
FB19 220@100M
C121 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C144 10NF 25V
C145 10NF 25V
C146 10NF 25V
C147 10NF 25V
3V3
U19 TPS2031D
IN1 IN2 EN GND OUT1 OUT2 OUT3 OC NC
R100 10K
C135 10NF
C136 100NF
C139 4.7UF 16V
C91 22UF
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
6-18-2008_23:38
PATH
ROACH_TRANSCEIVERS0_1
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
CHECKED: E BAUERMEISTER
APPR:
SHEET 8 OF 25

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

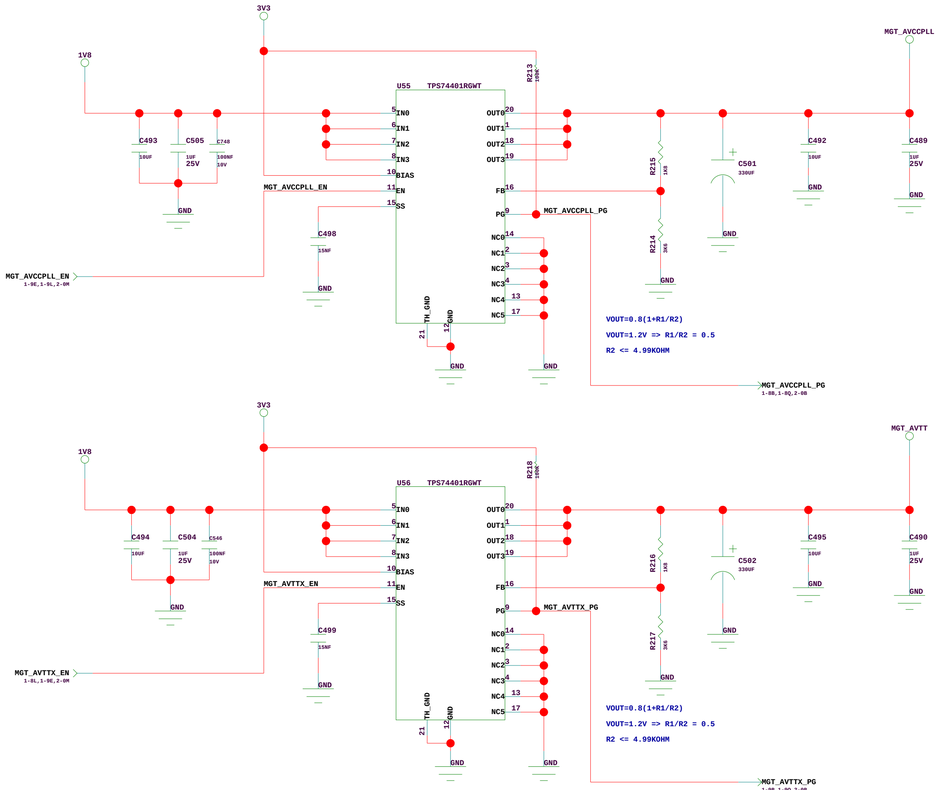
G4 AND G8 CONNECTED IN 2X2 MODULE

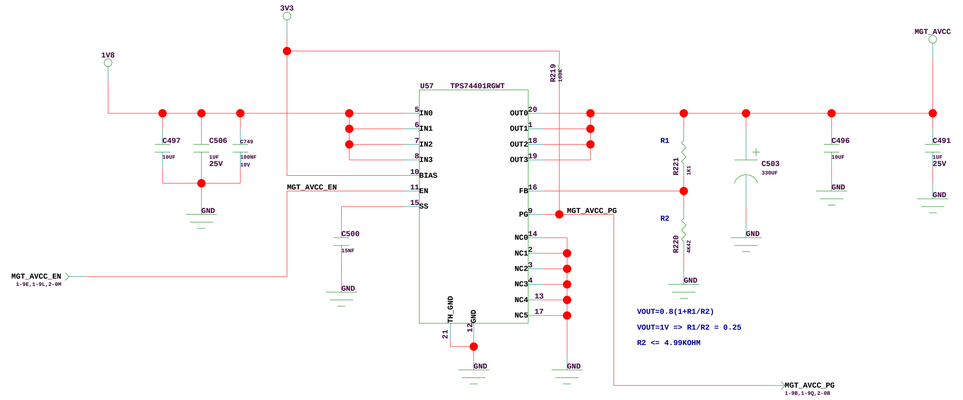
OPTICAL MODULE FAULT - RED LED

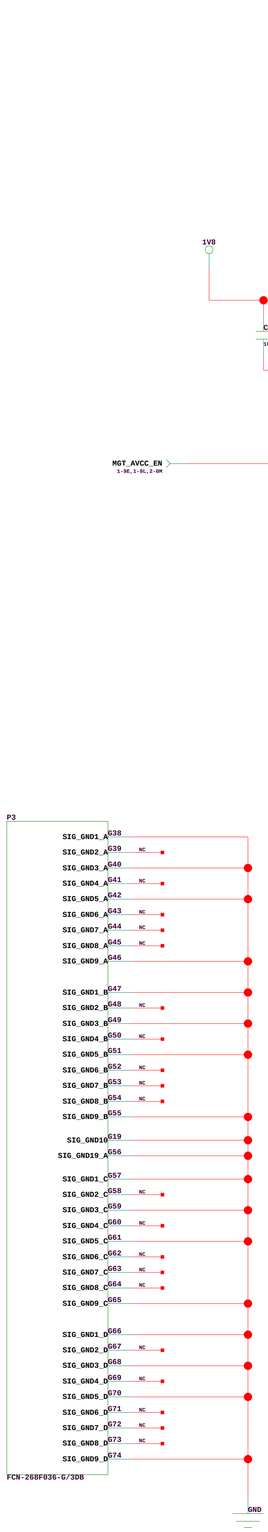
FCN-268F036-G/3DB

CCLD-023-25-156.250 156.25MHZ

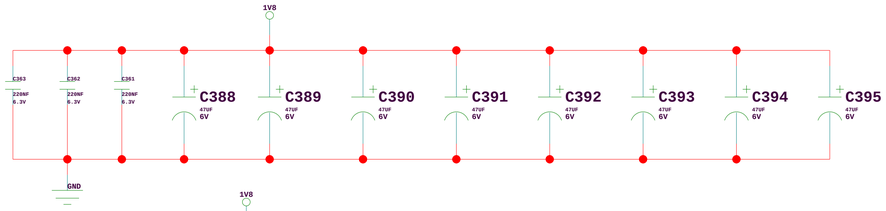
ROACH/iBOB2	ROACH_TRANSCEIVERS2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-18-2008_23:38	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 9 OF 25

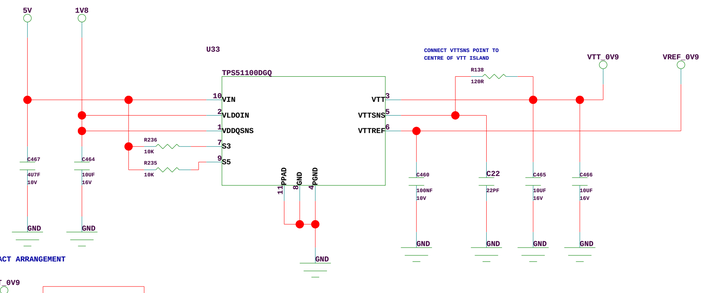




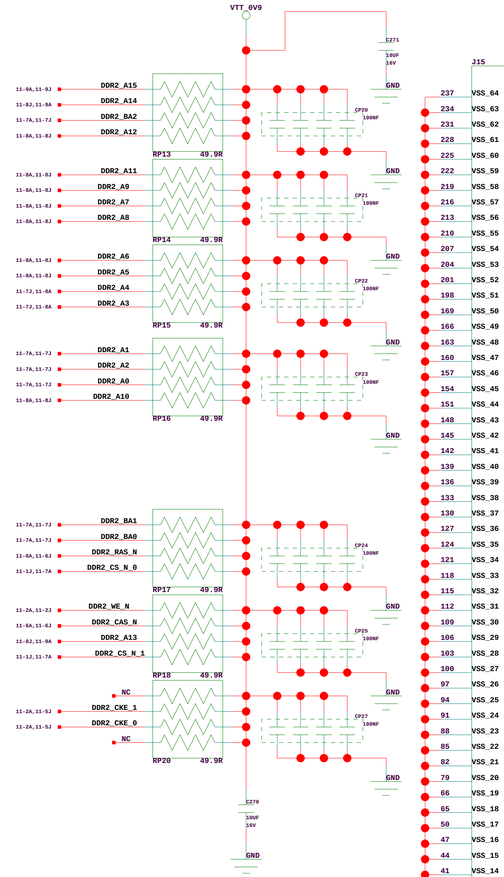


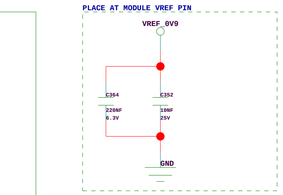
ROACH/iBOB2	**ROACH_TRANSCEIVERS_PSU**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-18-2008_23:38	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 10 OF 25

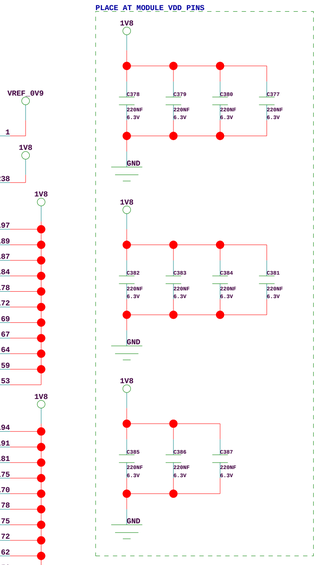


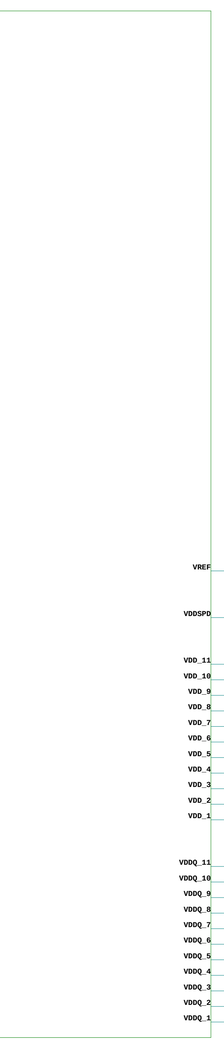


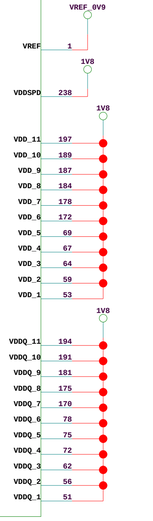
VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
PLACE ONE 10uF CAPACITOR ON EITHER END OF ISLAND

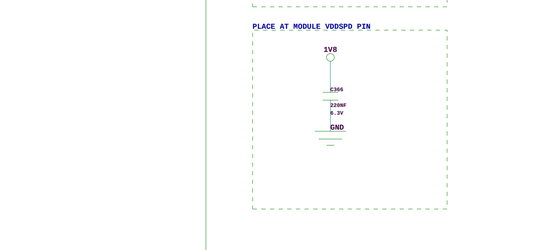


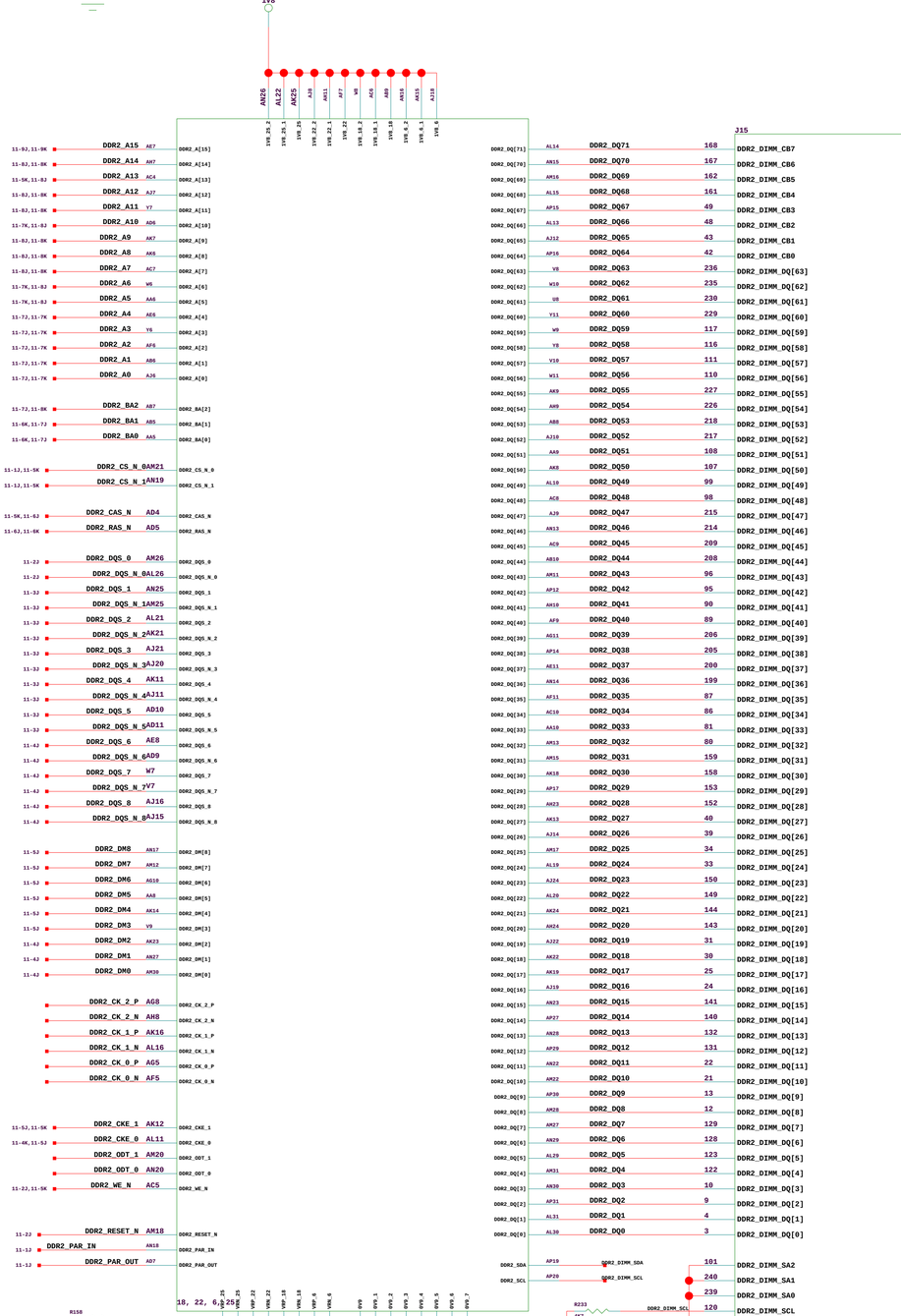


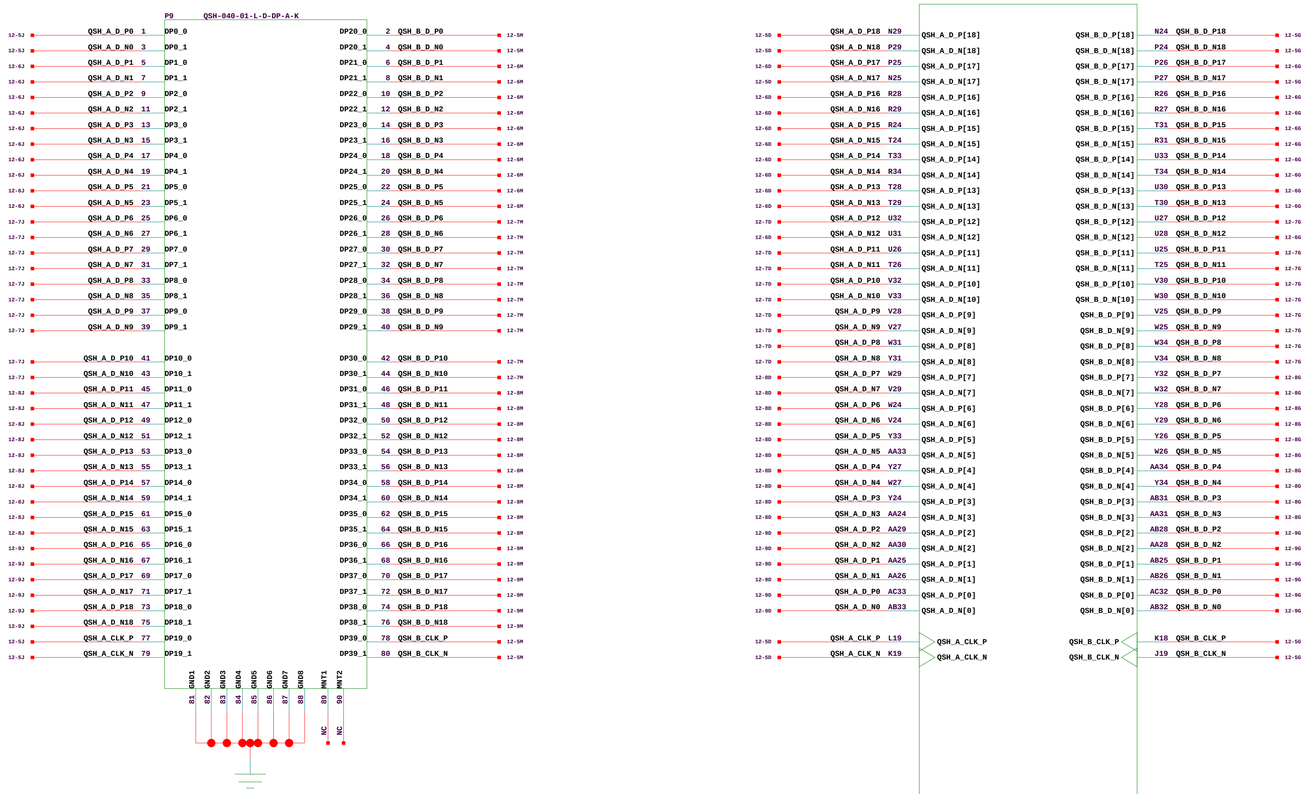




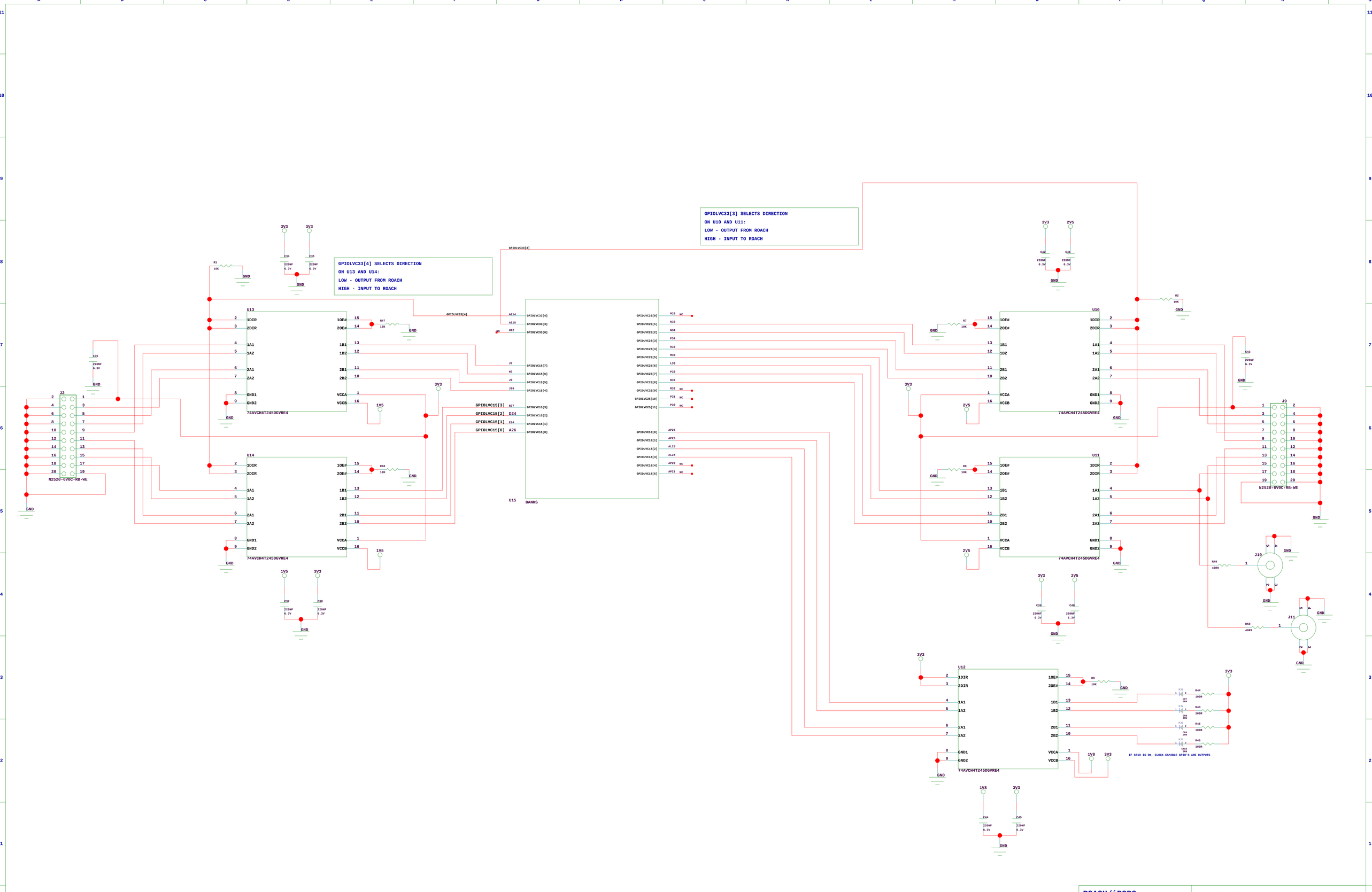




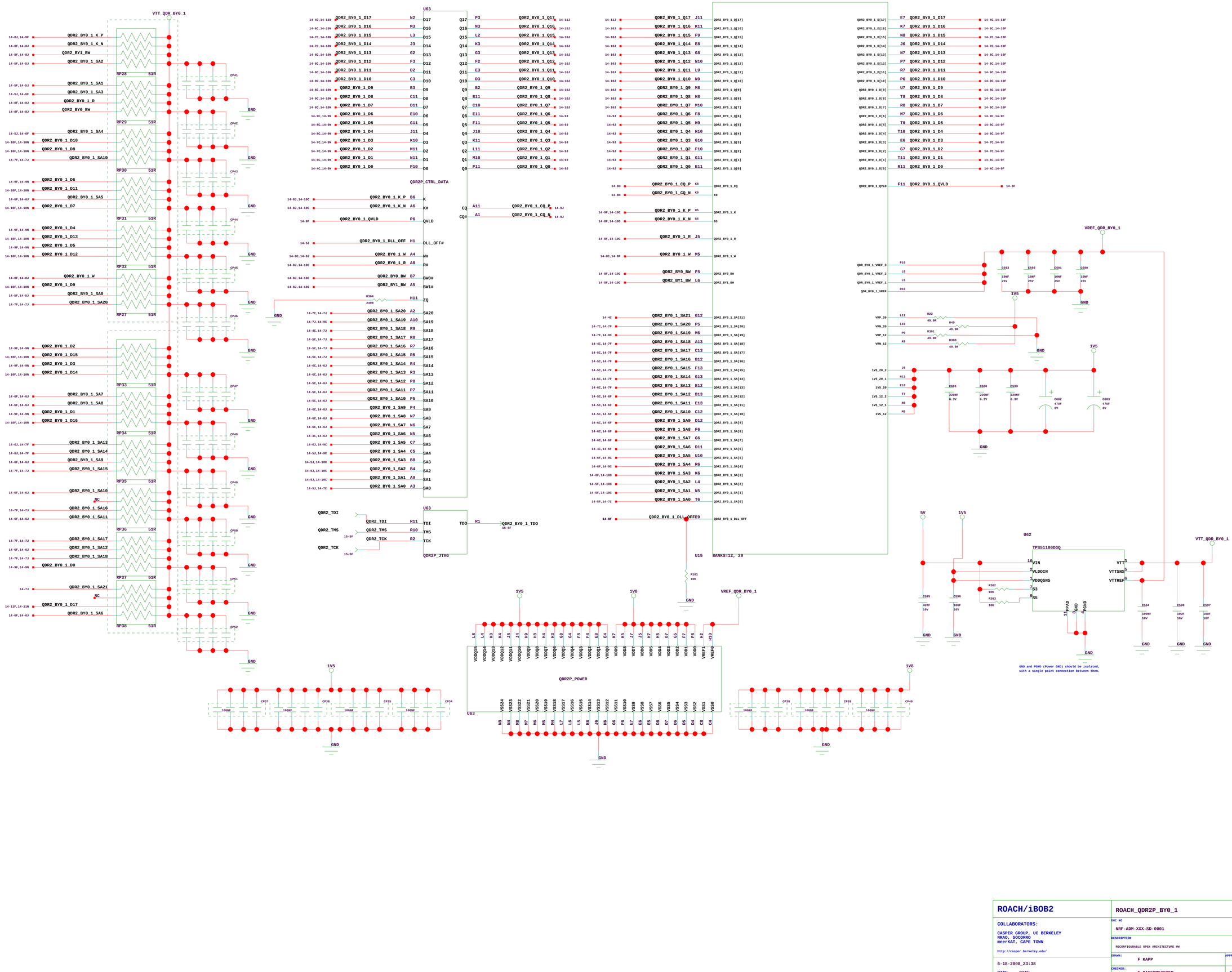




ROACH/iBOB2	ROACH_DIFF_GPIO
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
6-18-2008_23:38 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 12 OF 25



ROACH/iBOB2	**ROACH_GPIO_MISC**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-18-2008_23:38 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 13 OF 25



ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS:	DOC NO: NRF-ADM-XXX-SD-0001
CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN	REVISION: A
http://casper.berkeley.edu/	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-18-2008_23:38	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 14 OF 25

VTT_QDR_BY2_3

RP1 51R
RP2 51R
RP3 51R
RP4 51R
RP5 51R
RP6 51R
RP7 51R
RP8 51R
RP9 51R
RP10 51R
RP11 51R
RP12 51R

15-8J,15-9F QDR2_BY2_3_K_P
15-8F,15-8J QDR2_BY2_3_K_N
15-8F,15-8J QDR3_BY3_BW
15-5F,15-5J QDR2_BY2_3_SA2
15-5F,15-5J QDR2_BY2_3_SA1
15-5J,15-6F QDR2_BY2_3_SA3
15-8F,15-8J QDR2_BY2_3_R
15-8F,15-8J QDR2_BY2_BW
15-6F,15-6J QDR2_BY2_3_SA5
15-10F,15-10N QDR2_BY2_3_D8
15-5J,15-6F QDR2_BY2_3_SA4
15-7F,15-7J QDR2_BY2_3_SA19
15-9F,15-9N QDR2_BY2_3_D6
15-10F,15-10N QDR2_BY2_3_D11
15-10F,15-10N QDR2_BY2_3_D7
15-10F,15-10N QDR2_BY2_3_D10
15-9F,15-9N QDR2_BY2_3_D4
15-10F,15-10N QDR2_BY2_3_D13
15-9F,15-9N QDR2_BY2_3_D5
15-10F,15-10N QDR2_BY2_3_D12
15-8F,15-8J QDR2_BY2_3_W
15-10F,15-10N QDR2_BY2_3_D9
15-5F,15-5J QDR2_BY2_3_SA0
15-7F,15-7J QDR2_BY2_3_SA20
15-10F,15-10N QDR2_BY2_3_D16
15-10F,15-10N QDR2_BY2_3_D15
15-9F,15-9N QDR2_BY2_3_D3
15-10F,15-10N QDR2_BY2_3_D14
15-7J QDR2_BY2_3_SA21
NC
15-11F,15-11N QDR2_BY2_3_D17
15-6F,15-6J QDR2_BY2_3_SA6
15-7F,15-7J QDR2_BY2_3_SA17
15-6F,15-6J QDR2_BY2_3_SA12
15-7F,15-7J QDR2_BY2_3_SA18
15-9F,15-9N QDR2_BY2_3_D0
15-6F,15-6J QDR2_BY2_3_SA10
NC
15-7F,15-7J QDR2_BY2_3_SA16
15-6F,15-6J QDR2_BY2_3_SA11
15-6J,15-7F QDR2_BY2_3_SA13
15-6J,15-7F QDR2_BY2_3_SA14
15-6F,15-6J QDR2_BY2_3_SA9
15-7F,15-7J QDR2_BY2_3_SA15
15-6F,15-6J QDR2_BY2_3_SA7
15-6F,15-6J QDR2_BY2_3_SA8
15-9F,15-9N QDR2_BY2_3_D1
15-9F,15-9N QDR2_BY2_3_D2

CP1 100NF
CP2 100NF
CP3 100NF
CP4 100NF
CP8
CP9
CP10
CP11
CP12
CP13
CP14
CP15
CP16
CP17
CP18
CP19

GND

U17

15-6C,15-11N QDR2_BY2_3_D17 N2 D17
15-7C,15-10N QDR2_BY2_3_D16 M3 D16
15-7C,15-10N QDR2_BY2_3_D15 L3 D15
15-7C,15-10N QDR2_BY2_3_D14 J3 D14
15-8C,15-10N QDR2_BY2_3_D13 G2 D13
15-8C,15-10N QDR2_BY2_3_D12 F3 D12
15-9C,15-10N QDR2_BY2_3_D11 D2 D11
15-8C,15-10N QDR2_BY2_3_D10 C3 D10
15-8C,15-10N QDR2_BY2_3_D9 B3 D9
15-9C,15-10N QDR2_BY2_3_D8 C11 D8
15-9C,15-10N QDR2_BY2_3_D7 D11 D7
15-9C,15-9N QDR2_BY2_3_D6 E10 D6
15-8C,15-9N QDR2_BY2_3_D5 G11 D5
15-8C,15-9N QDR2_BY2_3_D4 J11 D4
15-7C,15-9N QDR2_BY2_3_D3 K10 D3
15-4C,15-9N QDR2_BY2_3_D2 M11 D2
15-4C,15-9N QDR2_BY2_3_D1 N11 D1
15-5C,15-9N QDR2_BY2_3_D0 P10 D0

QDR2P_CTRL_DATA

15-8J,15-10C QDR2_BY2_3_K_P B6 K
15-8J,15-10C QDR2_BY2_3_K_N A6 K#
15-9P QDR2_BY2_3_QVLD P6 QVLD
15-5J QDR2_BY2_3_DLL_OFF H1 DLL_OFF#
15-8C,15-8J QDR2_BY2_3_W A4 W#
15-8J,15-10C QDR2_BY2_3_R A8 R#
15-8J,15-10C QDR2_BY2_BW B7 BW0#
15-8J,15-10C QDR2_BY3_BW A5 BW1#
R55 240R
H11 ZQ
15-7C,15-7J GND
15-7J,15-9C QDR2_BY2_3_SA20 A2 SA20
15-6C,15-7J QDR2_BY2_3_SA19 A10 SA19
15-6C,15-7J QDR2_BY2_3_SA18 R9 SA18
15-6C,15-7J QDR2_BY2_3_SA17 R8 SA17
15-5C,15-7J QDR2_BY2_3_SA16 R7 SA16
15-4C,15-7J QDR2_BY2_3_SA15 R5 SA15
15-5C,15-6J QDR2_BY2_3_SA14 R4 SA14
15-5C,15-6J QDR2_BY2_3_SA13 R3 SA13
15-6C,15-6J QDR2_BY2_3_SA12 P8 SA12
15-5C,15-6J QDR2_BY2_3_SA11 P7 SA11
15-5C,15-6J QDR2_BY2_3_SA10 P5 SA10
15-4C,15-6J QDR2_BY2_3_SA9 P4 SA9
15-4C,15-6J QDR2_BY2_3_SA8 N7 SA8
15-4C,15-6J QDR2_BY2_3_SA7 N6 SA7
15-6C,15-6J QDR2_BY2_3_SA6 N5 SA6
15-6J,15-9C QDR2_BY2_3_SA5 C7 SA5
15-5J,15-9C QDR2_BY2_3_SA4 C5 SA4
15-5J,15-10C QDR2_BY2_3_SA3 B8 SA3
15-5J,15-10C QDR2_BY2_3_SA2 B4 SA2
15-5J,15-10C QDR2_BY2_3_SA1 A9 SA1
15-5J,15-7C QDR2_BY2_3_SA0 A3 SA0

Q17 P3 QDR2_BY2_3_Q17 D26 QDR2_BY2_3_Q[17]
Q16 N3 QDR2_BY2_3_Q16 C25 QDR2_BY2_3_Q[16]
Q15 L2 QDR2_BY2_3_Q15 B25 QDR2_BY2_3_Q[15]
Q14 K3 QDR2_BY2_3_Q14 C23 QDR2_BY2_3_Q[14]
Q13 G3 QDR2_BY2_3_Q13 C22 QDR2_BY2_3_Q[13]
Q12 F2 QDR2_BY2_3_Q12 A23 QDR2_BY2_3_Q[12]
Q11 E3 QDR2_BY2_3_Q11 C20 QDR2_BY2_3_Q[11]
Q10 D3 QDR2_BY2_3_Q10 B20 QDR2_BY2_3_Q[10]
Q9 B2 QDR2_BY2_3_Q9 C19 QDR2_BY2_3_Q[9]
Q8 B11 QDR2_BY2_3_Q8 B18 QDR2_BY2_3_Q[8]
Q7 C10 QDR2_BY2_3_Q7 A19 QDR2_BY2_3_Q[7]
Q6 E11 QDR2_BY2_3_Q6 C18 QDR2_BY2_3_Q[6]
Q5 F11 QDR2_BY2_3_Q5 A20 QDR2_BY2_3_Q[5]
Q4 J10 QDR2_BY2_3_Q4 A21 QDR2_BY2_3_Q[4]
Q3 K11 QDR2_BY2_3_Q3 B21 QDR2_BY2_3_Q[3]
Q2 L11 QDR2_BY2_3_Q2 B22 QDR2_BY2_3_Q[2]
Q1 M10 QDR2_BY2_3_Q1 B23 QDR2_BY2_3_Q[1]
Q0 P11 QDR2_BY2_3_Q0 A24 QDR2_BY2_3_Q[0]

CQ A11 QDR2_BY2_3_CQ_P 15-9J
CQ# A1 QDR2_BY2_3_CQ_N 15-9J

15-8N QDR2_BY2_3_CQ_P C24 QDR2_BY2_3_CQ
15-8N QDR2_BY2_3_CQ_N D25 D25
15-9F,15-10C QDR2_BY2_3_K_P D14 QDR2_BY2_3_K
15-8F,15-10C QDR2_BY2_3_K_N E14 E14
15-8F,15-10C QDR2_BY2_3_R C15 QDR2_BY2_3_R
15-8C,15-8F QDR2_BY2_3_W F15 QDR2_BY2_3_W
15-8F,15-10C QDR2_BY2_BW D15 QDR2_BY2_BW
15-8F,15-10C QDR3_BY3_BW D16 QDR3_BY3_BW

15-6C QDR2_BY2_3_SA21 D31 QDR2_BY2_3_SA[21]
15-7C,15-7F QDR2_BY2_3_SA20 F14 QDR2_BY2_3_SA[20]
15-7F,15-9C QDR2_BY2_3_SA19 A14 QDR2_BY2_3_SA[19]
15-6C,15-7F QDR2_BY2_3_SA18 D27 QDR2_BY2_3_SA[18]
15-6C,15-7F QDR2_BY2_3_SA17 A30 QDR2_BY2_3_SA[17]
15-5C,15-7F QDR2_BY2_3_SA16 B30 QDR2_BY2_3_SA[16]
15-4C,15-7F QDR2_BY2_3_SA15 C30 QDR2_BY2_3_SA[15]
15-5C,15-7F QDR2_BY2_3_SA14 B31 QDR2_BY2_3_SA[14]
15-5C,15-7F QDR2_BY2_3_SA13 D30 QDR2_BY2_3_SA[13]
15-6C,15-6F QDR2_BY2_3_SA12 B26 QDR2_BY2_3_SA[12]
15-5C,15-6F QDR2_BY2_3_SA11 A29 QDR2_BY2_3_SA[11]
15-5C,15-6F QDR2_BY2_3_SA10 D29 QDR2_BY2_3_SA[10]
15-4C,15-6F QDR2_BY2_3_SA9 A31 QDR2_BY2_3_SA[9]
15-4C,15-6F QDR2_BY2_3_SA8 G17 QDR2_BY2_3_SA[8]
15-4C,15-6F QDR2_BY2_3_SA7 C27 QDR2_BY2_3_SA[7]
15-6C,15-6F QDR2_BY2_3_SA6 C28 QDR2_BY2_3_SA[6]
15-6F,15-9C QDR2_BY2_3_SA5 E16 QDR2_BY2_3_SA[5]
15-6F,15-9C QDR2_BY2_3_SA4 E17 QDR2_BY2_3_SA[4]
15-6F,15-10C QDR2_BY2_3_SA3 A15 QDR2_BY2_3_SA[3]
15-5F,15-10C QDR2_BY2_3_SA2 B15 QDR2_BY2_3_SA[2]
15-5F,15-10C QDR2_BY2_3_SA1 C14 QDR2_BY2_3_SA[1]
15-5F,15-7C QDR2_BY2_3_SA0 B16 QDR2_BY2_3_SA[0]
15-8F QDR2_BY2_3_DLL_OFF D20 QDR2_BY2_3_DLL_OFF

BANK3=5, 23

U15
R102 10K
GND

QDR2_BY2_3_Q[17] F24 QDR2_BY2_3_D17 15-6C,15-11F
QDR2_BY2_3_Q[16] F23 QDR2_BY2_3_D16 15-7C,15-10F
QDR2_BY2_3_Q[15] E23 QDR2_BY2_3_D15 15-7C,15-10F
QDR2_BY2_3_Q[14] E22 QDR2_BY2_3_D14 15-7C,15-10F
QDR2_BY2_3_Q[13] D22 QDR2_BY2_3_D13 15-8C,15-10F
QDR2_BY2_3_Q[12] E21 QDR2_BY2_3_D12 15-8C,15-10F
QDR2_BY2_3_Q[11] D21 QDR2_BY2_3_D11 15-9C,15-10F
QDR2_BY2_3_Q[10] F18 QDR2_BY2_3_D10 15-8C,15-10F
QDR2_BY2_3_Q[9] A16 QDR2_BY2_3_D9 15-8C,15-10F
QDR2_BY2_3_Q[8] B17 QDR2_BY2_3_D8 15-9C,15-10F
QDR2_BY2_3_Q[7] C17 QDR2_BY2_3_D7 15-9C,15-10F
QDR2_BY2_3_Q[6] D17 QDR2_BY2_3_D6 15-9C,15-9F
QDR2_BY2_3_Q[5] F16 QDR2_BY2_3_D5 15-8C,15-9F
QDR2_BY2_3_Q[4] E19 QDR2_BY2_3_D4 15-8C,15-9F
QDR2_BY2_3_Q[3] F20 QDR2_BY2_3_D3 15-7C,15-9F
QDR2_BY2_3_Q[2] G20 QDR2_BY2_3_D2 15-4C,15-9F
QDR2_BY2_3_Q[1] F21 QDR2_BY2_3_D1 15-4C,15-9F
QDR2_BY2_3_Q[0] G21 QDR2_BY2_3_D0 15-5C,15-9F

QDR2_BY2_3_QVLD A25 QDR2_BY2_3_QVLD 15-8F

VREF_QDR_BY2_3
QDR_BY2_3_VREF_3 G18
QDR_BY2_3_VREF_2 F19
QDR_BY2_3_VREF_1 A28
QDR_BY2_3_VREF A18
C56 10NF 25V
C55 10NF 25V
C50 10NF 25V
C46 10NF 25V
GND

1V5
VRP_5 D19 RS1 49.9R
VRN_5 E18 RS2 49.9R
VRP_23 B28 R151 49.9R
VRN_23 C29 R152 49.9R
GND

1V5
1V5_5_2 F17
1V5_5_1 C16
1V5_5 B19
1V5_23_2 G24
1V5_23_1 F27
1V5_23 C26
C85 220NF 6.3V
C86 220NF 6.3V
C87 220NF 6.3V
C88 470UF 6V
C89 470UF 6V
GND

5V
1V5
C58 4U7F 10V
C59 10UF 16V
GND

U16
R53 10K
R54 10K
18 VIN
2 VLDOIN
1 VDDQSNS
7 S3
9 S5
17 PPAD
5 GND
4 PGND
GND

VTT 3
VTTSNS 5
VTTREF 6
C57 100NF 10V
C84 10UF 16V
C69 10UF 16V
GND
VTT_QDR_BY2_3

GND and PGND (Power GND) should be isolated, with a single point connection between them.

QDR2_BY0_1_TDO 14-5H QDR2_BY0_1_TDO R11
QDR2_TMS 14-5K QDR2_TMS R10
QDR2_TCK 14-5F QDR2_TCK R2

U17
TDI
TMS
TCK
TDO R1 QDR2_BY2_3_TDO
QDR2P_JTAG

1V5
1V8
VREF_QDR_BY2_3

L8 VDDQ15
L4 VDDQ14
K8 VDDQ13
K4 VDDQ12
J8 VDDQ11
J4 VDDQ10
H9 VDDQ9
H8 VDDQ8
H4 VDDQ7
H3 VDDQ6
G8 VDDQ5
G4 VDDQ4
F9 VDDQ3
F4 VDDQ2
E8 VDDQ1
E4 VDDQ0
K7 VDD9
K5 VDD8
J7 VDD7
J5 VDD6
H7 VDD5
H5 VDD4
G7 VDD3
G5 VDD2
F7 VDD1
F5 VDD0
H2 VREF1
H10 VREF0

QDR2P_POWER

U17

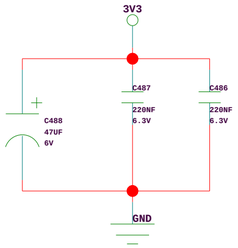
N8 VSS24
M4 VSS23
M8 VSS22
M7 VSS21
M6 VSS20
M5 VSS19
M4 VSS18
L7 VSS17
L6 VSS16
L5 VSS15
K6 VSS14
J6 VSS13
H6 VSS12
G6 VSS11
F6 VSS10
E7 VSS9
E6 VSS8
E5 VSS7
D8 VSS6
D7 VSS5
D6 VSS4
D5 VSS3
D4 VSS2
C8 VSS1
C4 VSS0

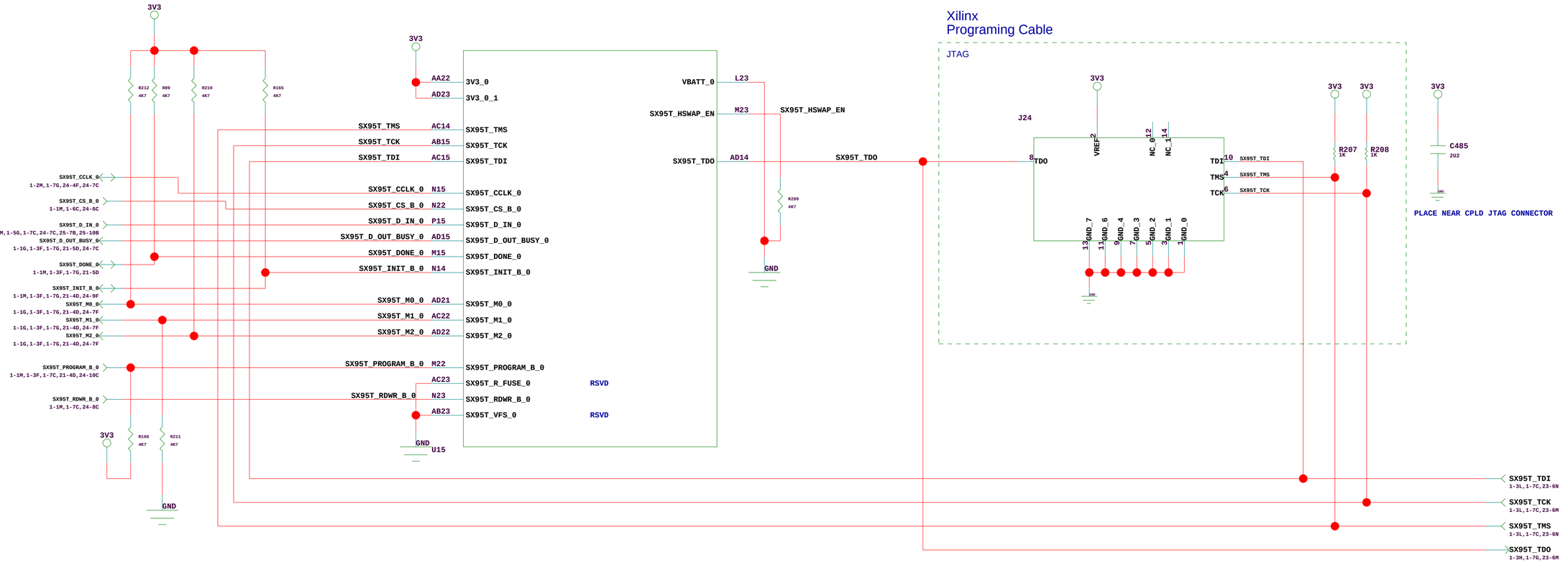
1V8
CP5 100NF
CP6 100NF
CP7 100NF
GND

ROACH/iBOB2	ROACH_QDR2P_BY2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO NRF-ADM-XXX-SD-0001 REVISION A
	DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
6-18-2008_23:38 PATH PATH	DRAWN: F KAPP APPR:
	CHECKED: E BAUERMEISTER SHEET 15 OF 25

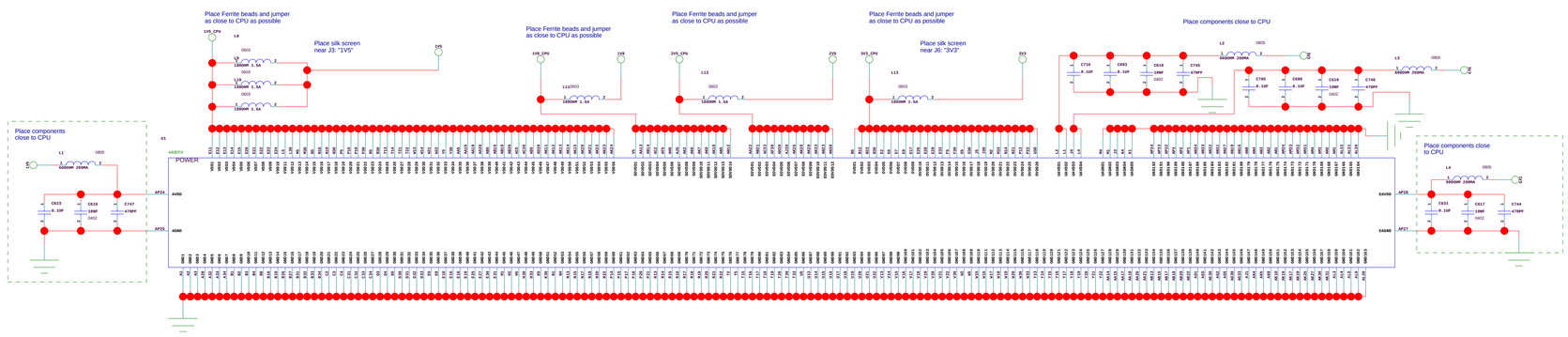
TBD

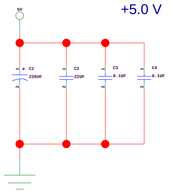
VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

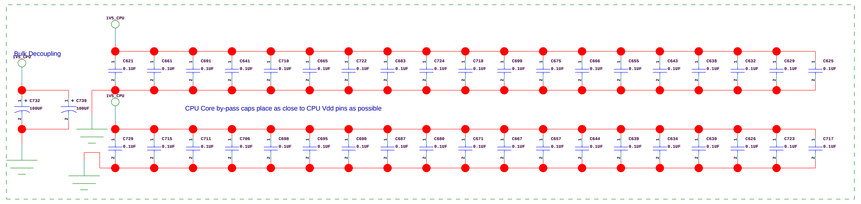


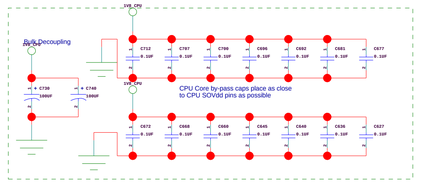


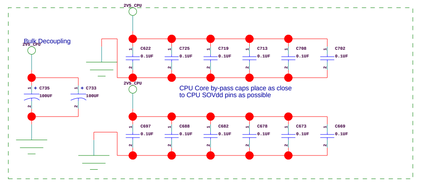
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
6-18-2008_23:38 PATH PATH	

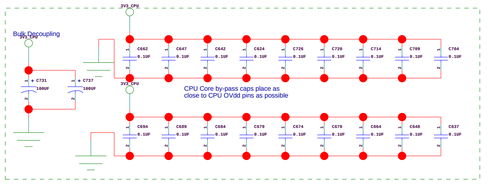


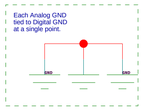










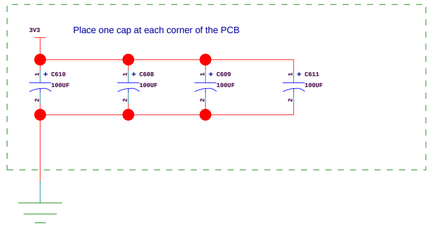


REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: **CASPER GROUP, UC BERKELEY** **NRAO, SOCORRO** **meerKAT, CAPE TOWN** http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MK
6-18-2008_23:38 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 17 OF 25

REMOVED 3V3 GENERATION



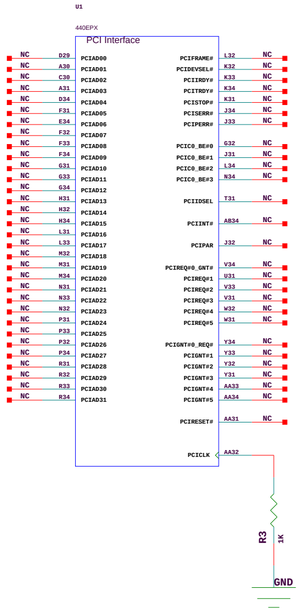
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET 18 OF 25
6-18-2008_23:38 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-18-2008_23:38 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

Place nearest PHY pin 96

2V5 C533 10NF

Place nearest PHY pin 101

2V5 C534 10NF

Place nearest PHY pin 98

1V8 R233 1R C536 22UF C511 10NF

Place nearest PHY pin 100

1V8 R232 1R C535 22UF C512 10NF

Place as close to PHY CORE VDD power pins as possible

1V8 C526 10NF C527 100NF C525 10NF C528 100NF C530 10NF C529 100NF C531 10NF C532 100NF

Place as close to PHY IO VDD power pins as possible

2V5 C513 10NF C514 100NF C515 10NF C516 100NF C517 10NF C518 100NF C519 10NF C520 100NF C521 10NF C522 100NF C523 10NF C524 100NF

U3 440EP4 Gig-Ethernet RGMII1

GMC1_TXD0 AF26 NC
GMC1_TXD1 AL26 NC
GMC1_TXD2 AN26 NC
GMC1_TXD3 AK26 NC
GMC1_TXCTL AK24 NC
GMC1_TXCLK AK32 NC
GMC1_RXD0 AK29 NC
GMC1_RXD1 AF30 NC
GMC1_RXD2 AF31 NC
GMC1_RXD3 AK30 NC
GMC1_RXCTL AL33 NC
GMC1_RXCLK AJ32 NC

UNUSED SECOND ETHERNET MAC

1V8 2V5 2V5 1V8 2V5

U1 440EP4 Gig-Ethernet RGMII0

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups. Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

Place resistors as close to CPU as possible and keep all traces lengths equal

GMC0_TXD0 AL24 R241 22R
GMC0_TXD1 AN23 R240 22R
GMC0_TXD2 AN25 R239 22R
GMC0_TXD3 AL25 R238 22R
GMC0_TXCTL AK34 R242 22R
GMC0_TXCLK AM27 R243 22R
GMC0_RXD0 AL28 GMCRXD0 R244 22R
GMC0_RXD1 AF29 GMCRXD1 R245 22R
GMC0_RXD2 AM28 GMCRXD2 R246 22R
GMC0_RXD3 AN29 GMCRXD3 R247 22R
GMC0_RXCTL AJ31 GMCRXCTL R248 22R
GMC0_RXCLK AN28 GMCRXCLK R249 22R
GMCTXCLK AL27 R250 22R
GMCREFCLK AJ33 GMCREFCLK_125MHZ R277 22R
GMCMDCLK AL34 GMCMDCLK R267 1K
GMCMDIO AK34 GMCMDIO

ETHERNET Mgt.

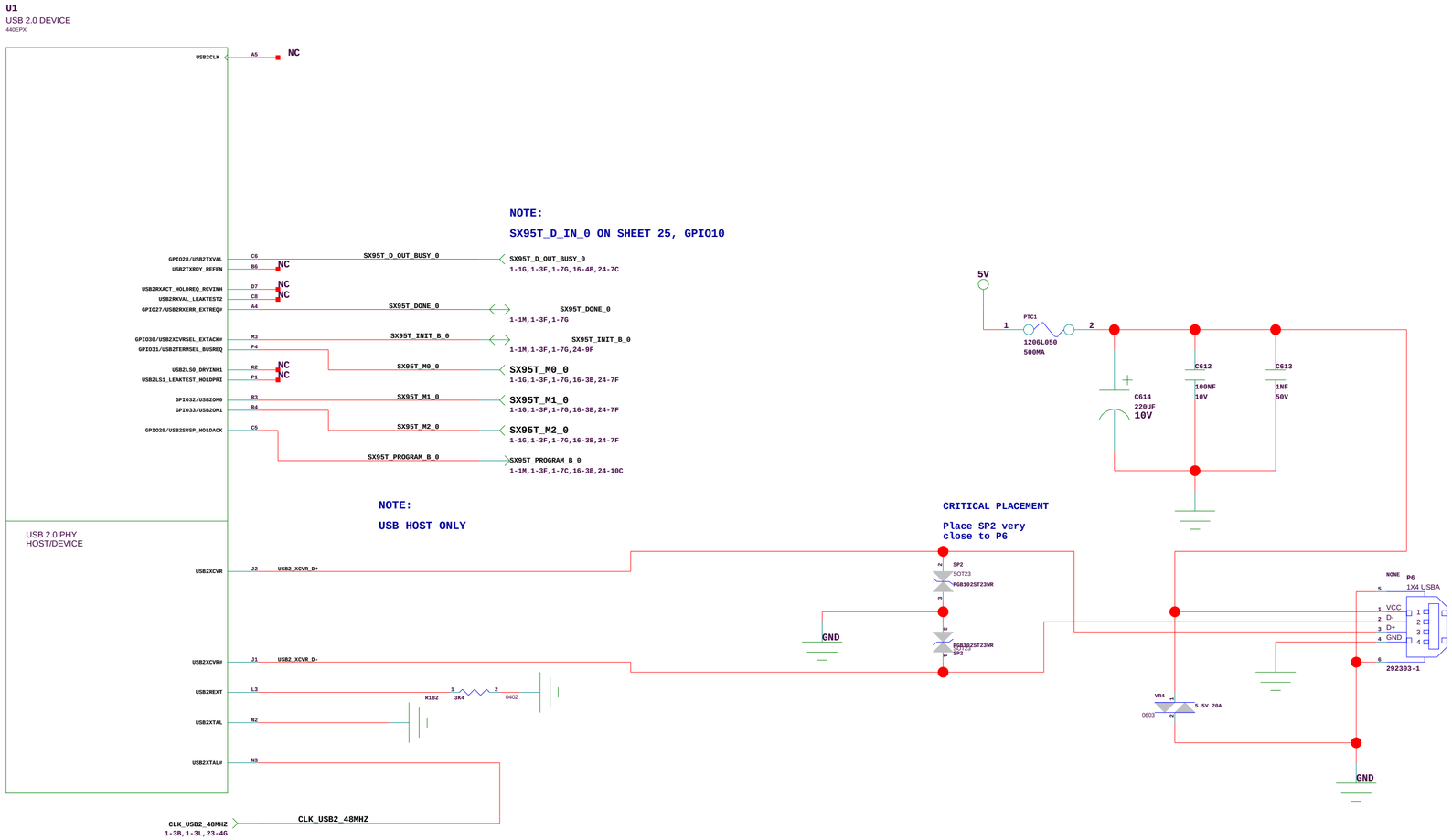
R219 1K 2V5

1-4E,20-3C GMCMDCLK
1-4E,20-3C GMCMDIO

Place resistors close to PHY all trace lengths equal

GMCRXD0 GMCRXD1 GMCRXD2 GMCRXD3 GMCRXCTL GMCRXCLK GMCTXD0 GMCTXD1 GMCTXD2 GMCTXD3 GMCRXCTL GMCTXCLK

NC NC NC



ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-18-2008_23:38 PATH PATH	DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET 21 OF 25

DDR_PA[15:0]

DDR_PD0[63:0]

U1

DDR SDRAM

44OEPX

DDR_PD0	AB2	MEMDATA00	MEMADDR00
DDR_PD1	AP22	MEMDATA01	MEMADDR01
DDR_PD2	AM26	MEMDATA02	MEMADDR02
DDR_PD3	AL28	MEMDATA03	MEMADDR03
DDR_PD4	AL22	MEMDATA04	MEMADDR04
DDR_PD5	AM22	MEMDATA05	MEMADDR05
DDR_PD6	AR21	MEMDATA06	MEMADDR06
DDR_PD7	AP21	MEMDATA07	MEMADDR07
DDR_PD8	AP28	MEMDATA08	MEMADDR08
DDR_PD9	AL18	MEMDATA09	MEMADDR09
DDR_PD10	AR17	MEMDATA10	MEMADDR10
DDR_PD11	AP17	MEMDATA11	MEMADDR11
DDR_PD12	AN26	MEMDATA12	MEMADDR12
DDR_PD13	AP18	MEMDATA13	MEMADDR13
DDR_PD14	AN18	MEMDATA14	
DDR_PD15	AP16	MEMDATA15	BA0
DDR_PD16	AM16	MEMDATA16	BA1
DDR_PD17	AP15	MEMDATA17	BA2
DDR_PD18	AP14	MEMDATA18	
DDR_PD19	AL14	MEMDATA19	RAS#
DDR_PD20	AL17	MEMDATA20	CAS#
DDR_PD21	AM17	MEMDATA21	WE#
DDR_PD22	AN15	MEMDATA22	
DDR_PD23	AM15	MEMDATA23	DM0
DDR_PD24	AP13	MEMDATA24	DM1
DDR_PD25	AN13	MEMDATA25	DM2
DDR_PD26	AP12	MEMDATA26	DM3
DDR_PD27	AL12	MEMDATA27	DM4
DDR_PD28	AM14	MEMDATA28	DM5
DDR_PD29	AN14	MEMDATA29	DM6
DDR_PD30	AL13	MEMDATA30	DM7
DDR_PD31	AM13	MEMDATA31	DM8
DDR_PD32	AF3	MEMDATA32	
DDR_PD33	AF1	MEMDATA33	DQS0
DDR_PD34	AD4	MEMDATA34	DQS1
DDR_PD35	AD3	MEMDATA35	DQS2
DDR_PD36	AB3	MEMDATA36	DQS3
DDR_PD37	AF2	MEMDATA37	DQS4
DDR_PD38	AE2	MEMDATA38	DQS5
DDR_PD39	AE1	MEMDATA39	DQS6
DDR_PD40	AC3	MEMDATA40	DQS7
DDR_PD41	AC1	MEMDATA41	DQS8
DDR_PD42	AA4	MEMDATA42	
DDR_PD43	AA3	MEMDATA43	MEMODT0
DDR_PD44	AD2	MEMDATA44	MEMODT1
DDR_PD45	AC4	MEMDATA45	
DDR_PD46	AB1	MEMDATA46	BANKSEL#0
DDR_PD47	AB2	MEMDATA47	BANKSEL#1
DDR_PD48	Y3	MEMDATA48	
DDR_PD49	Y2	MEMDATA49	MEMCLKEN
DDR_PD50	Y4	MEMDATA50	
DDR_PD51	V3	MEMDATA51	MEMCLKOUT
DDR_PD52	AA2	MEMDATA52	
DDR_PD53	AA1	MEMDATA53	MEMCLKOUT#
DDR_PD54	W3	MEMDATA54	
DDR_PD55	W1	MEMDATA55	
DDR_PD56	V1	MEMDATA56	
DDR_PD57	U2	MEMDATA57	
DDR_PD58	T4	MEMDATA58	
DDR_PD59	R1	MEMDATA59	
DDR_PD60	V2	MEMDATA60	
DDR_PD61	U1	MEMDATA61	
DDR_PD62	T2	MEMDATA62	
DDR_PD63	T3	MEMDATA63	

DDR_PA0	AM5	MEMADDR00	
DDR_PA1	AP4	MEMADDR01	
DDR_PA2	AM3	MEMADDR02	
DDR_PA3	AM6	MEMADDR03	
DDR_PA4	AP6	MEMADDR04	
DDR_PA5	AN6	MEMADDR05	
DDR_PA6	AL7	MEMADDR06	
DDR_PA7	AN7	MEMADDR07	
DDR_PA8	AM7	MEMADDR08	
DDR_PA9	AP7	MEMADDR09	
DDR_PA10	AL2	MEMADDR10	
DDR_PA11	AL6	MEMADDR11	
DDR_PA12	AN8	MEMADDR12	
DDR_PA13	AN4	MEMADDR13	
DDR_PBA0	AJ3		22-7L,22-8K
DDR_PBA1	AN3		22-8K,22-8L
DDR_PBA2	AP8		22-8K,22-10L
DDR_PRAS#	AJ4		22-7K,22-7L
DDR_PCAS#	AN4		22-7L,22-8K
DDR_PWE#	AJ2		22-3K,22-7L
DDR_PDM0	AL21	DM0	22-5K
DDR_PDM1	AP18	DM1	22-6K
DDR_PDM2	AP15	DM2	22-6K
DDR_PDM3	AL14	DM3	22-6K
DDR_PDM4	AD4	DM4	22-6K
DDR_PDM5	AB3	DM5	22-6K
DDR_PDM6	Y3	DM6	22-6K
DDR_PDM7	V3	DM7	22-6K
DDR_PDM8	AN10	DM8	22-6K
DDR_PDQS0	AM21	DQS0	22-6K
DDR_PDQS1	AM19	DQS1	22-4K
DDR_PDQS2	AL15	DQS2	22-4K
DDR_PDQS3	AM13	DQS3	22-4K
DDR_PDQS4	AB3	DQS4	22-4K
DDR_PDQS5	AB4	DQS5	22-5K
DDR_PDQS6	W3	DQS6	22-5K
DDR_PDQS7	Y3	DQS7	22-5K
DDR_PDQS8	AP10	DQS8	22-5K
DDR_PODT0	AN3	MEMODT0	22-7L
DDR_PODT1	AN1	MEMODT1	22-6L
DDR_PCS0#	AN2	BANKSEL#0	22-3K,22-7L
DDR_PCS1#	AM1	BANKSEL#1	22-3K,22-7L
DDR_PCKE	AN9	MEMCLKEN	22-6K,22-11L
DDR_PCLKOUT	AL1	MEMCLKOUT	22-2A
DDR_PCLKOUT#	AM1	MEMCLKOUT#	22-2A

PPC_ECC0	AM11	ECC0	22-9F
PPC_ECC1	AL11	ECC1	22-9F
PPC_ECC2	AM9	ECC2	22-9F
PPC_ECC3	AL9	ECC3	22-10F
PPC_ECC4	AM11	ECC4	22-10F
PPC_ECC5	AN11	ECC5	22-10F
PPC_ECC6	AM10	ECC6	22-10F
PPC_ECC7	AP9	ECC7	22-10F

DDR2 Clock line must be 500ps longer than Address/Command lines
To compensate for additional loading when using unbuffered DIMM's
See P84 of PPC440EPx for more information

DDR_VREF_0V9

5V

1V8

DDR_VTT

U32
TPS51100DGQ

VIN	10		
VLDOIN	2		
VDDQSNS	1		
S3	7		
S5	8		
VTT	3		
VTTSNS	5		
VTTREF	6		
PPAD	11		
GND	9		
PGND	4		

R230 10K
R229 10K
R6 120R
C459 .01UF 16V
C456 10UF 16V
C453 100NF 10V
C21 22PF
C457 10UF 16V
C458 10UF 16V

GND

J8

PPC_ECC7	22-6D	168	DDR2_DIMM_CB7
PPC_ECC6	22-6D	167	DDR2_DIMM_CB6
PPC_ECC5	22-7D	162	DDR2_DIMM_CB5
PPC_ECC4	22-7D	161	DDR2_DIMM_CB4
PPC_ECC3	22-7D	49	DDR2_DIMM_CB3
PPC_ECC2	22-7D	48	DDR2_DIMM_CB2
PPC_ECC1	22-7D	43	DDR2_DIMM_CB1
PPC_ECC0	22-7D	42	DDR2_DIMM_CB0
DDR_PDQ63		236	DDR2_DIMM_DQ[63]
DDR_PDQ62		235	DDR2_DIMM_DQ[62]
DDR_PDQ61		230	DDR2_DIMM_DQ[61]
DDR_PDQ60		229	DDR2_DIMM_DQ[60]
DDR_PDQ59		117	DDR2_DIMM_DQ[59]
DDR_PDQ58		116	DDR2_DIMM_DQ[58]
DDR_PDQ57		111	DDR2_DIMM_DQ[57]
DDR_PDQ56		110	DDR2_DIMM_DQ[56]
DDR_PDQ55		227	DDR2_DIMM_DQ[55]
DDR_PDQ54		226	DDR2_DIMM_DQ[54]
DDR_PDQ53		218	DDR2_DIMM_DQ[53]
DDR_PDQ52		217	DDR2_DIMM_DQ[52]
DDR_PDQ51		108	DDR2_DIMM_DQ[51]
DDR_PDQ50		107	DDR2_DIMM_DQ[50]
DDR_PDQ49		99	DDR2_DIMM_DQ[49]
DDR_PDQ48		98	DDR2_DIMM_DQ[48]
DDR_PDQ47		215	DDR2_DIMM_DQ[47]
DDR_PDQ46		214	DDR2_DIMM_DQ[46]
DDR_PDQ45		209	DDR2_DIMM_DQ[45]
DDR_PDQ44		208	DDR2_DIMM_DQ[44]
DDR_PDQ43		96	DDR2_DIMM_DQ[43]
DDR_PDQ42		95	DDR2_DIMM_DQ[42]
DDR_PDQ41		90	DDR2_DIMM_DQ[41]
DDR_PDQ40		89	DDR2_DIMM_DQ[40]
DDR_PDQ39		206	DDR2_DIMM_DQ[39]
DDR_PDQ38		205	DDR2_DIMM_DQ[38]
DDR_PDQ37		200	DDR2_DIMM_DQ[37]
DDR_PDQ36		199	DDR2_DIMM_DQ[36]
DDR_PDQ35		87	DDR2_DIMM_DQ[35]
DDR_PDQ34		86	DDR2_DIMM_DQ[34]
DDR_PDQ33		81	DDR2_DIMM_DQ[33]
DDR_PDQ32		80	DDR2_DIMM_DQ[32]
DDR_PDQ31		159	DDR2_DIMM_DQ[31]
DDR_PDQ30		158	DDR2_DIMM_DQ[30]
DDR_PDQ29		153	DDR2_DIMM_DQ[29]
DDR_PDQ28		152	DDR2_DIMM_DQ[28]
DDR_PDQ27		40	DDR2_DIMM_DQ[27]
DDR_PDQ26		39	DDR2_DIMM_DQ[26]
DDR_PDQ25		34	DDR2_DIMM_DQ[25]
DDR_PDQ24		33	DDR2_DIMM_DQ[24]
DDR_PDQ23		150	DDR2_DIMM_DQ[23]
DDR_PDQ22		149	DDR2_DIMM_DQ[22]
DDR_PDQ21		144	DDR2_DIMM_DQ[21]
DDR_PDQ20		143	DDR2_DIMM_DQ[20]
DDR_PDQ19		31	DDR2_DIMM_DQ[19]
DDR_PDQ18		30	DDR2_DIMM_DQ[18]
DDR_PDQ17		25	DDR2_DIMM_DQ[17]
DDR_PDQ16		24	DDR2_DIMM_DQ[16]
DDR_PDQ15		141	DDR2_DIMM_DQ[15]
DDR_PDQ14		140	DDR2_DIMM_DQ[14]
DDR_PDQ13		132	DDR2_DIMM_DQ[13]
DDR_PDQ12		131	DDR2_DIMM_DQ[12]
DDR_PDQ11		22	DDR2_DIMM_DQ[11]
DDR_PDQ10		21	DDR2_DIMM_DQ[10]
DDR_PDQ9		13	DDR2_DIMM_DQ[9]
DDR_PDQ8		12	DDR2_DIMM_DQ[8]
DDR_PDQ7		129	DDR2_DIMM_DQ[7]
DDR_PDQ6		128	DDR2_DIMM_DQ[6]
DDR_PDQ5		123	DDR2_DIMM_DQ[5]
DDR_PDQ4		122	DDR2_DIMM_DQ[4]
DDR_PDQ3		10	DDR2_DIMM_DQ[3]
DDR_PDQ2		9	DDR2_DIMM_DQ[2]
DDR_PDQ1		4	DDR2_DIMM_DQ[1]
DDR_PDQ0		3	DDR2_DIMM_DQ[0]
		101	DDR2_DIMM_SA2
		240	DDR2_DIMM_SA1
		239	DDR2_DIMM_SA0
I2C0_SCLK	1-2B,1-5L,1-9B,2-2P,2S-5A	120	DDR2_DIMM_SCL
I2C0_SDATA	1-2B,1-5L,1-9E	119	DDR2_DIMM_SDA
		879160001	

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA2	22-9D,22-10L
DDR2_DIMM_BA[1]	190	DDR_PBA1	22-8L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-7L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	DDR_PCLKOUT2	
DDR2_DIMM_CK_N[2]	221	DDR_PCLKOUT2#	
DDR2_DIMM_CK_P[1]	137	DDR_PCLKOUT1	
DDR2_DIMM_CK_N[1]	138	DDR_PCLKOUT1#	
DDR2_DIMM_CK_P[0]	185	DDR_PCLKOUT0	
DDR2_DIMM_CK_N[0]	186	DDR_PCLKOUT0#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-8D,22-11L
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-8D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	1-2B,1-2M,24-10F
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D
PAR_OUT	55	PPC_DDR2_ERROR	1 TP4
PAR_IN	68	PAR_IN	1 TP5

C313 5PF 50V
C308 5PF 50V
C455 5PF 50V

R226 33 4K7

PPC_DDR2_RESET_N

GND

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

DDR_VTT

22-6K,22-8D	DDR_PCKE	RP24	CP26
	DDR_PA15		
	DDR_PA14		
22-8K,22-8D	DDR_PBA2		
	DDR_PA12	RP23	CP28
	DDR_PA11		
	DDR_PA9		
	NC		
	DDR_PA7	RP22	CP29
	DDR_PA8		
	DDR_PA6		
	DDR_PA5		
	DDR_PA4	RP21	CP30
	DDR_PA3		
	DDR_PA1		
	DDR_PA2		
	DDR_PA0	RP25	CP32
22-8K,22-8D	DDR_PBA1		
	DDR_PA10		
22-8K,22-8D	DDR_PBA0		
22-7K,22-8D	DDR_PRAS#	RP26	CP31
22-3K,22-8D	DDR_PWE#		
22-3K,22-8D	DDR_PCS0#		
22-8K,22-8D	DDR_PCAS#		
22-3K,22-8D	DDR_PCS1#	RP19	CP33
22-8D	DDR_PODT0		
	DDR_PA13		
22-8D	DDR_PODT1		

GND

J8

VSS_64	237	194	VDDQ_11
VSS_63	234	191	VDDQ_10
VSS_62	231	181	VDDQ_9
VSS_61	228	175	VDDQ_8
VSS_60	225	170	VDDQ_7
VSS_59	222	78	VDDQ_6
VSS_58	219	75	VDDQ_5
VSS_57	216	72	VDDQ_4
VSS_56	213	62	VDDQ_3
VSS_55	210	56	VDDQ_2
VSS_54	207	51	VDDQ_1
VSS_53	204		
VSS_52	201		
VSS_51	198		
VSS_50	169		
VSS_49	166		
VSS_48	163		
VSS_47	160		
VSS_46	157		
VSS_45	154		
VSS_44	151		
VSS_43	148		
VSS_42	145		
VSS_41	142		
VSS_40	139		
VSS_39	136		
VSS_38	133		
VSS_37	130		
VSS_36	127		
VSS_35	124		
VSS_34	121		
VSS_33	118		
VSS_32	115		
VSS_31	112		
VSS_30	109		
VSS_29	106		
VSS_28	103		
VSS_27	100		
VSS_26	97		
VSS_25	94		
VSS_24	91		
VSS_23	88		
VSS_22	85		
VSS_21	82		
VSS_20	79		
VSS_19	66		
VSS_18	65		
VSS_17	50		
VSS_16	47		
VSS_15	44		
VSS_14	41		
VSS_13	38		
VSS_12	35		
VSS_11	32		
VSS_10	29		
VSS_9	26		
VSS_8	23		
VSS_7	20		
VSS_6	17		
VSS_5	14		
VSS_4	11		
VSS_3	8		
VSS_2	5		
VSS_1	2		

879160001

GND

DDR_VREF_0V9

VREF 1

3V3

VDDSPD 238

1V8

GND

L17
0603
1000OHM 1.5A

C329 .01UF 10V
C300 100NF 10V
C63 10NF 25V

1V8

R167 10K

AVDD 8
AGND 7
OE 22
OS 21

DDR_PCLKOUT#
DDR_PCLKOUT

R168 120R

CLK 4
CLK# 5

Y0	38	DDR_PCLKOUT0	
Y0#	37	DDR_PCLKOUT0#	
Y1	39	DDR_PCLKOUT1	
Y1#	40	DDR_PCLKOUT1#	
Y2	3	DDR_PCLKOUT2	
Y2#	2	DDR_PCLKOUT2#	
Y3	11	NC	
Y3#	12	NC	
Y4	14	NC	
Y4#	13	NC	
Y5	34	NC	
Y5#	35	NC	
Y6	33	NC	
Y6#	32	NC	
Y7	29	NC	
Y7#	30	NC	
Y8	19	NC	
Y8#	18	NC	
Y9	16	NC	
Y9#	17	NC	

FBIN 27
FBIN# 26
FBOUT 24
FBOUT# 25
VS 23
GND1 15
GND2 31
10 10
.01 .01
CDCU877...

GND

FBOUT#

FBOUT

ROUTE ALL DDR CLOCKS AS LENGTH MATCHED ONLY
ROUTE DDR_PCLKOUT NETS 500PS LONGER THAN ADDR, CMD CTRL SIGNAL NETS
DDR_PCLKOUT NETS CAN BE SWAPPED ON CLOCK BUFFER FOR ROUTING
FBOUT NETS LENGTH MATCHED TO DDR_PCLKn NETS

DDR_VREF_0V9

1V8

C432	100NF 10V	C433	10NF 25V
C454	100NF 10V	C434	10NF 25V
C439	100NF 10V	C443	10NF 25V
C431	100NF 10V	C444	10NF 25V
C436	100NF 10V	C445	10NF 25V
C435	100NF 10V	C446	10NF 25V
C438	100NF 10V	C451	10NF 25V
C437	100NF 10V	C452	10NF 25V
C439	100NF 10V	C449	10NF 25V
C440	100NF 10V	C450	10NF 25V
C441	100NF 10V	C448	10NF 25V
C442	100NF 10V	C447	10NF 25V

GND

PLACE NEAREST DDR2 MODULE PINS

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

6-18-2008_23:38

PATH PATH

ROACH_PPC_DDR2

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

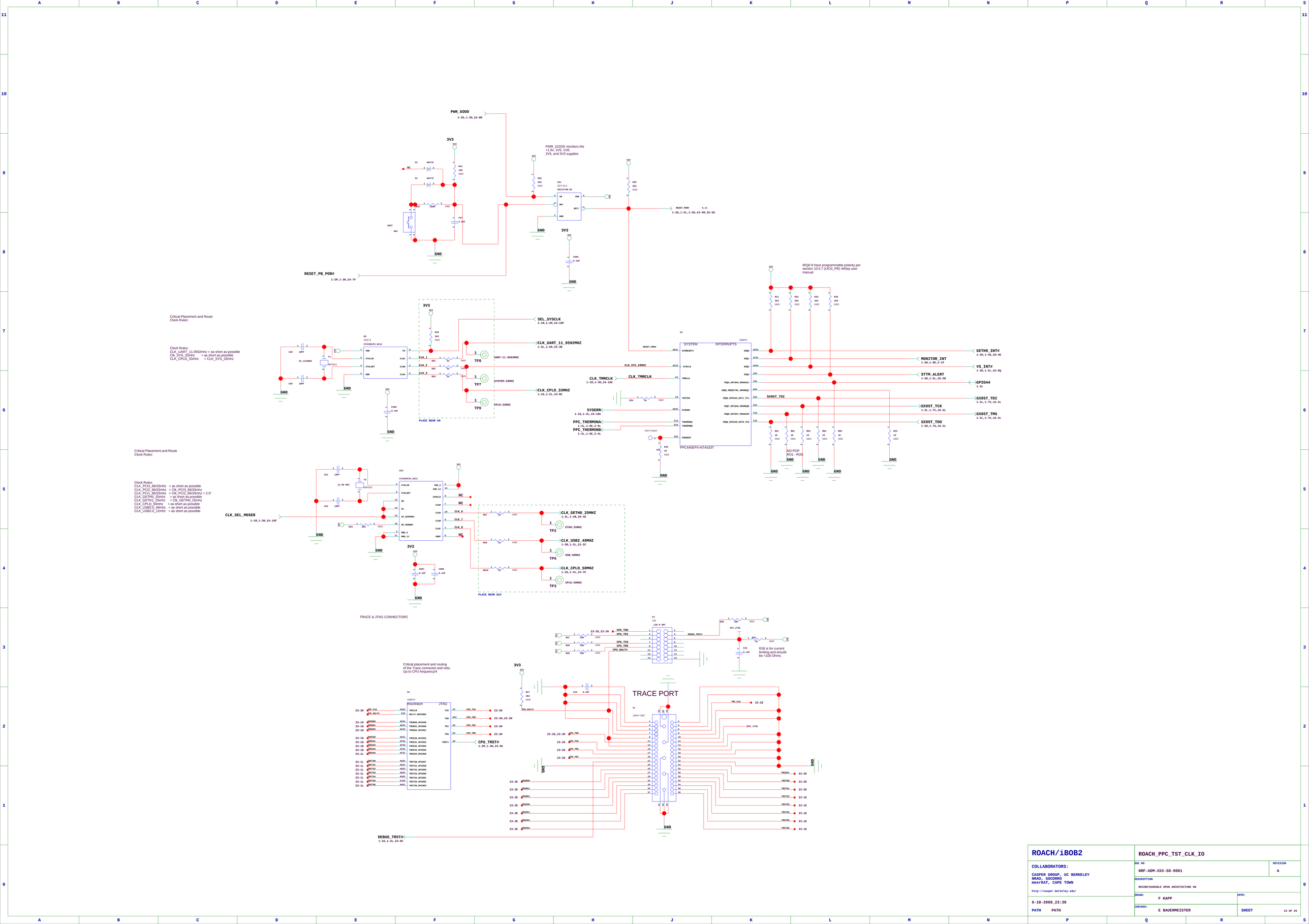
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 22 OF 25



ROACH/iBOB2	**ROACH_PPC_TST_CLK_IO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-18-2008_23:38	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 23 OF 25

roach_cpld_XC2C256_7VQ100C_pcb

CLK_TMCLK	4	PAD4	PAD217 142 NC
SYSRR	7	PAD8	PAD214 140 NC
EXT_RESETf	9	PAD10	PAD213 139 GETH0_RST#
SX95T_PROGRAM_B_0	10	PAD12	PAD212 138 PPC_DDR2_RESET_N
SX95T_DONE_0	11	PAD15	PAD211 137 CLK_SEL_MGGEN
PCS_2	12	PAD16	PAD208 136 SEL_SYSCLK
PB_WI	13	PAD17	PAD207 135 NC
DEBUG_TRSTf	14	PAD18	PAD206 134 NC
CPU_TRSTn	15	PAD19	PAD204 133 NC
FWBE_B#	16	PAD20	PAD199 132 NC
PADO[27:31]	17	PAD21	PAD197 131 SX95T_INIT_B_0
	18	PAD23	PAD196 130 NC
	19	PAD28	PAD195 129
	20	PAD29	PAD194 128
	21	PAD30	PAD192 126
PDATA[0:7]	22	PAD31	PAD191 125 NC
	23	PAD32	PAD190 124 NC
	24	PAD33	PAD187 121
	25	PAD34	PAD186 120 DAT1
	26	PAD35	PAD178 119 DAT0_DO
	28	PAD44	PAD177 118 DAT7
CLK_CPLD_33MHZ	30	PAD48	PAD176 117 DAT6
	31	PAD49	PAD175 116 CLK_SCLK
CLK_PERCLK	32	PAD50	PAD173 115 DAT5
	33	PAD52	PAD171 114 DAT4
PDE#	34	PAD54	PAD169 113 CMD_DI
SX95T_RDWR_B_0	35	PAD55	PAD168 112 DAT3
CLK_CPLD_50MHZ	38	PAD59	PAD167 111 DAT2
SX95T_D_IN_0	40	PAD64	PAD166 110
SX95T_D_OUT_BUSY_0	41	PAD65	PAD163 107
PER_CCLK_ENf	42	PAD66	PAD162 106 SX95T_M0_0
SX95T_CCLK_0	43	PAD67	PAD161 105 SX95T_M1_0
FRY_BYf	44	PAD68	PAD160 104 SX95T_M2_0
FWPC	45	PAD69	PAD158 103 NC
EE1_WPC	46	PAD70	PAD156 102 RESET_PB_POR#
EE2_BOOT_WPC	48	PAD73	PAD154 101 USER_LED1
STTM_ASC	49	PAD74	PAD152 100 SYSERR#
SELECTMAP_CS	50	PAD75	PAD146 98 RESET_BUFPOR#
	51 NC	PAD76	PAD145 97
SX95T_CS_B_0	52	PAD77	PAD144 96 USER_DIP0
	53 NC	PAD81	PAD143 95 USER_DIP1
PPC_RESET	54	PAD82	PAD142 94 USER_DIP2
SYS_CONFIG0	56	PAD86	PAD138 92 USER_DIP3
SYS_CONFIG1	57	PAD87	PAD137 91
SYS_CONFIG2	58	PAD88	PAD134 88
SYS_CONFIG3	59	PAD89	PAD133 87
SYS_CONFIG4	60	PAD90	PAD132 86 NC
SYS_CONFIG5	61	PAD95	PAD131 85 NC
SYS_CONFIG6	64	PAD100	PAD125 83 NC
SYS_CONFIG7	66	PAD102	PAD121 82 NC
	68 NC	PAD105	PAD120 81 NC
	69 NC	PAD107	PAD119 80 NC
	70 NC	PAD108	PAD118 79 NC
RESET_CPLD#	71	PAD109	PAD117 77 NC
	74 NC	PAD112	PAD115 76 NC
	75 NC	PAD113	PAD114

SYS_CONFIG[0:7] 1-2G,1-9E,2-2R — SYS_CONFIG[0:7]

U54 XC2C256_7VQ144C

RESETS

CPU_TRSTn = '1' when JTAG_TRSTn = '1' and RESET_PORn = '1' else '0'; see errata sheet

SD/MMC/MMCPLUS CONNECTOR

J17 SDSR13-A0-0005

10	CMD/DI	DAT0/DO	2
6	CLK/SCLK	DAT1	1
		DAT2	13
7	VDD	DAT3	12
8	VSS1	DAT4	11
4	VSS2	DAT5	9
		DAT6	5
14	SD_CD_COM	DAT7	3
15	SD_WP_COM		
		MNT1	16
		MNT2	17

3V3 — R135 10K — PER_CCLK_ENf

CLK_PERCLK 1-1G,1-4L,24-8B,25-6F — R305 330R — R306 240R

SN74AHC1G125DCKT: 1 OE# — 2 A — 3 GND — 4 Y — 5 VCC — U2

SX95T_CCLK_0 — C13 100NF 10V — SX95T_CCLK_0 1-2M,1-7G,24-7C

ENABLE PER_CLK CONNECTION TO CONFIGURATION I/F MUST CO-ORDINATE WITH SX95T_CCLK_0 AND MODE TO AVOID CLASH

PLACE AT END OF DAISY CHAIN

U54 XC2C256_7VQ144C — roach_cpld_XC2C256_7VQ100C_powerpins

VCC	VAUX	VCCIO_3	VCC_1	VCCIO_4	VCCIO_5	VCC_2	VCCIO_6	VCCIO	VCCIO_1	VCCIO_2
1	8	27	37	55	73	84	93	109	127	141

GND_3	GND_4	GND_5	GND_6	GND_7	GND_8	GND_9	GND_10	GND	GND_1	GND_2
29	36	47	62	72	89	99	99	108	123	144

PLACE NEAR CPLD POWER PINS

C473–C483 100NF 10V

SysErr will be used to drive Status LED (active H)

Boot Configuration

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

Configuration DIP-Switch

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

BOOT_CFG0 1-1M,1-4G,25-1J
BOOT_CFG1 1-1M,1-4G,25-1J
BOOT_CFG2 1-1M,1-4G,25-1J

R197 330R — R199 330R — U35 SC70-5 74LVC1G08 — C81 100N — C82 100N — C615 0.1UF — PWR_GOOD 1-2G,1-3M,23-10G

roach_cpld_XC2C256_7VQ100C_configpins

U54 XC2C256_7VQ144C

NC	2	PAD1	
NC	3	PAD3	
NC	5	PAD5	
NC	6	PAD7	
NC	39	PAD62	
	63	TDI	
	65	TMS	
	67	TCK	
	122	TDO	
	143	PAD218	

RESET_PORn 1-2G,1-3L,1-5G,23-9J,25-5G

Xilinx Programing Cable

JTAG

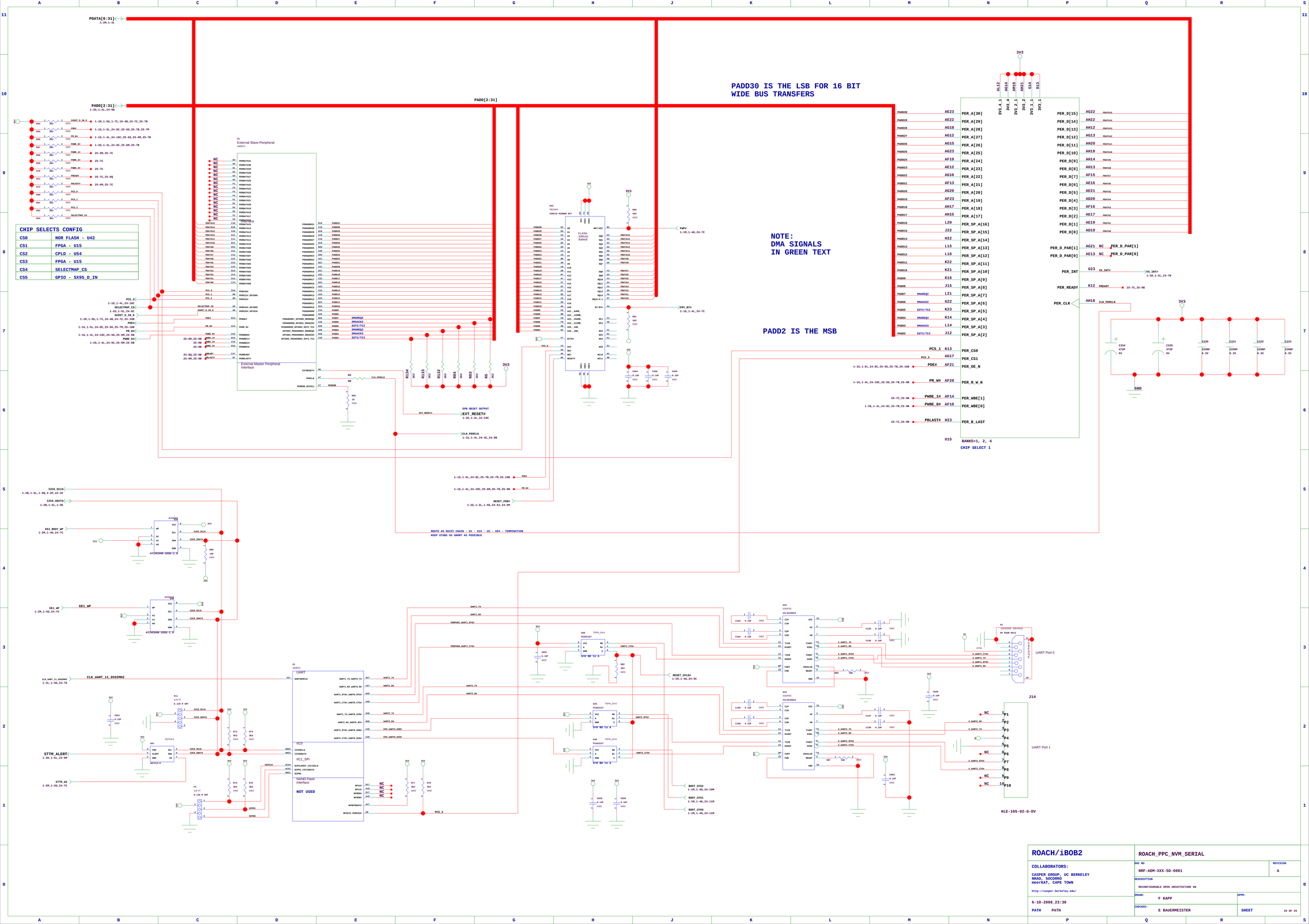
J22: TDO — VREF 2 — NC_0 12 — NC_1 14 — TDI 10 CPLD_TDI — TMS 8 CPLD_TMS — TCK 6 CPLD_TCK — GND_7 17 — GND_6 15 — GND_4 9 — GND_3 7 — GND_2 5 — GND_1 3 — GND_0 1

R193 1K — R192 1K

C484 20Z

PLACE NEAR CPLD JTAG CONNECTOR

ROACH/iBOB2	ROACH_PPC_CPLD
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO NRF-ADM-XXX-SD-0001 — REVISION A
	DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
6-18-2008_23:38 PATH PATH	DRAWN: F KAPP — APPR: — CHECKED: E BAUERMEISTER — SHEET 24 OF 25



ROACH/iBOB2	ROACH_PPC_NVM_SERIAL
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-18-2008_23:38 PATH PATH	DRAWN: F KAPP — APPR:
	CHECKED: E BAUERMEISTER — SHEET 25 OF 25