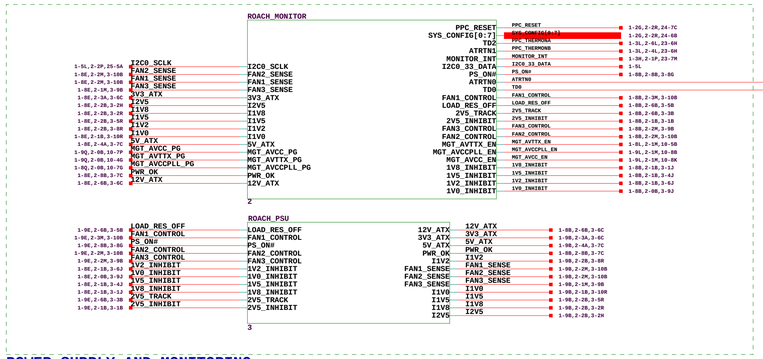
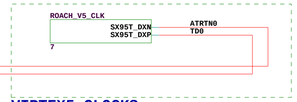
VIRTEX5

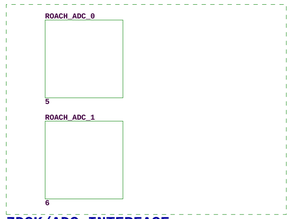
POWER SUPPLY AND MONITORING



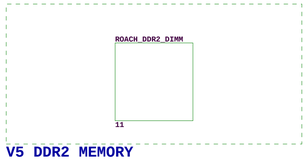
VIRTEX5 CLOCKS



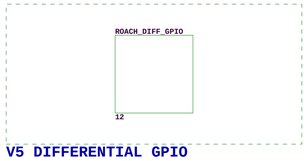
ZDOK/ADC INTERFACE



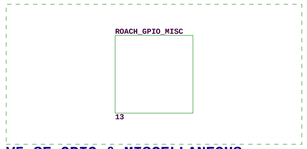
V5 DDR2 MEMORY



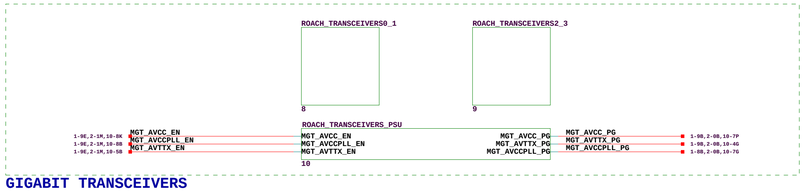
V5 DIFFERENTIAL GPIO



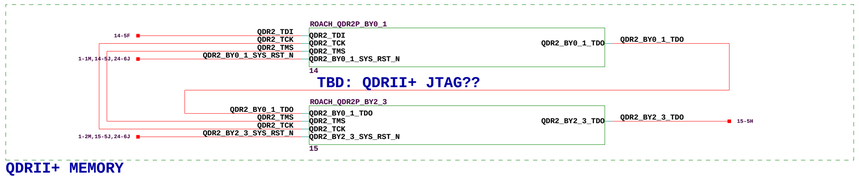
V5 SE GPIO & MISCELLANEOUS



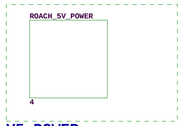
GIGABIT TRANSCEIVERS



QDRII+ MEMORY



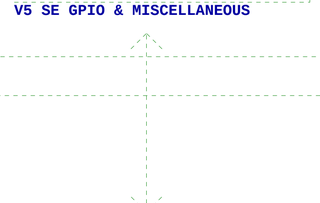
V5 POWER

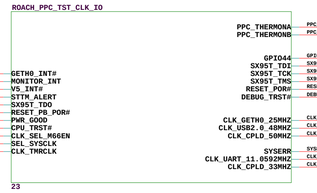


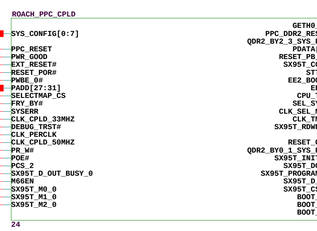
VIRTEX5 CONFIGURATION

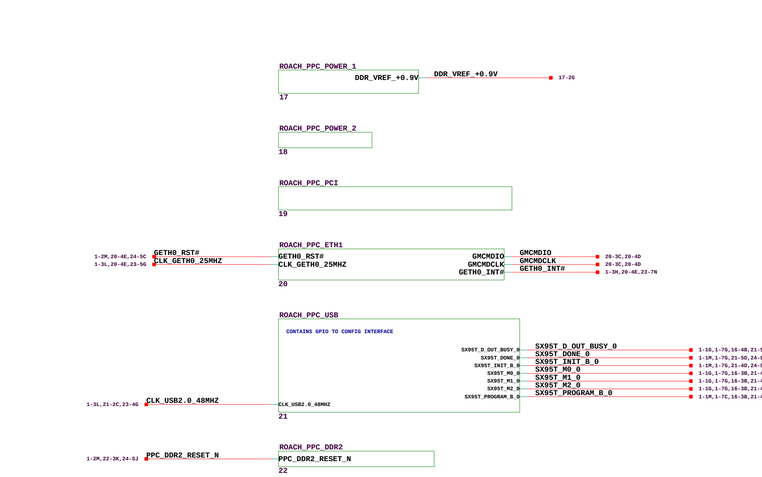
PPC

V5 SE GPIO & MISCELLANEOUS

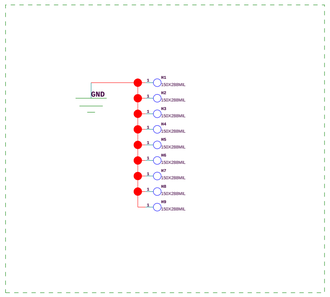








MECHANICAL



CONTRIBUTORS

ETIENNE BAUERMEISTER
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HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2	**ROACH_TOP**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-22-2007_16:25	DRAWN: F KAPP · APPR:
PATH PATH	CHECKED: E BAUERMEISTER · SHEET 1 OF 25

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

TIE TO GROUND IF PLL'S ARE NOT USED

PLACE AT ACTEL 3V3 POWER PINS

PLACE AT ACTEL 1V5 POWER PINS

roach_AFS600_powerpins

roach_AFS600_pcb

roach_AFS600_configpins

PB POWER SWITCH

KEY - REMOVE PIN

MONITOR RESET

XPORT - PLACE IN REAR I/O REGION

TEMPERATURE DIODE HEADER

ACTEL JTAG CONNECTOR

ROACH/iBOB2	ROACH_MONITOR
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-22-2007_16:25	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 2 OF 25

AUX FAN CONNECTORS - ATX 4 PIN

J21 — 47053-1000
- 1 GND
- 2 12V
- 3 SENSE — FAN1_SENSE — FAN1_SENSE 1-8E,1-9B,2-2M
- 4 CONTROL — FAN1_CONTROL — FAN1_CONTROL 1-8B,1-9E,2-3M

PLACE ON SILKSCREEN: FAN1

J20 — 47053-1000
- 1 GND
- 2 12V
- 3 SENSE — FAN2_SENSE — FAN2_SENSE 1-8E,1-9B,2-2M
- 4 CONTROL — FAN2_CONTROL — FAN2_CONTROL 1-8B,1-9E,2-3M

PLACE ON SILKSCREEN: FAN2

J19 — 47053-1000
- 1 GND
- 2 12V
- 3 SENSE — FAN3_SENSE — FAN3_SENSE 1-8E,1-9B,2-1M
- 4 CONTROL — FAN3_CONTROL — FAN3_CONTROL 1-8B,1-9E,2-2M

PLACE ON SILKSCREEN: FAN3

GND

ATX POWER CONNECTORS

5VAUX N12V

J18 — 44206-0007

1	3V3_1	3V3_4	13
2	3V3_2	_12V	14
3	COM_1	COM_4	15
4	5V_1	PS_ON#	16
5	COM_2	COM_5	17
6	5V_2	COM_6	18
7	COM_3	COM_7	19
8	PWR_OK	N/C	20NC
9	5VSB	5V_3	21
10	12V1_1	5V_4	22
11	12V1_2	5V_5	23
12	3V3_3	COM_8	24

PS_ON# — PS_ON# 1-8B,1-9E,2-8B

PWR_OK — PWR_OK 1-8B,1-8E,2-8B

5VAUX — 5VSB

J32 — 0015453110
- 1 3
- 2 4
- 5 6
- 7 8
- 9 10

5V_ATX 1-8E,1-9B,2-4A

3V3_ATX 1-8E,1-9B,2-3A

12V_ATX 1-8B,1-8E,2-6B

GND

LOAD RESISTORS FOR ATX PSU MIN LOAD
SWITCH OFF ONCE LOAD EXCEEDS MINIMUM SPEC
ADJUST RESISTOR VALUES FOR ACTUAL SUPPLY

5VAUX

R180 10K — Q9 NDS331N — R185 10R 5W AC05000001009JLB00

LOAD_RES_OFF 1-8B,1-9B,2-6B — Q8 BSS138 — Q10 NDS331N — R187 56R 5W AC05000005609JLB00

R181 1K — GND

J16 — 39-29-9042
- 1 COM1 — 12V1 3
- 2 COM2 — 12V2 4

GND

1V0

ROUTE FROM LOAD

PLACE RESISTOR CLOSE TO PTH08T210WAD
ROUTE SHORTEST

R144 TBD

U50 — PTH08T210WAD

13	TURBOTRANS	VO_0	5
10	SENSE+	VO_1	9
2	VI_1	VOADJUST	12
6	VI_0	GND_3	4
1	INHIBIT/UVLADJ	GND_2	7
14	TRACK	GND_1	8
11	SENSE-	GND_0	3

12V — L6 BLM31PG121SN1B — C403 330UF 16V — C401 330UF 16V — C419 10UF — GND

1V2

1V0_INHIBIT 1-8B,1-8E,2-6B — Q4 BSS138

ROUTE FROM LOAD

R143 TBD — C418 10UF — C402 1000UF 2V5 — C400 1000UF 2V5 — I1V0 1-8E,1-9B,2-1B

DIRECT TO P8 ON PTH08T210W, DEDICATED TRACE

1V2

ROUTE FROM LOAD

PLACE RESISTOR CLOSE TO PTH08T210WAD
ROUTE SHORTEST

R142 3K3

U49 — PTH08T210WAD

13	TURBOTRANS	VO_0	5
10	SENSE+	VO_1	9
2	VI_1	VOADJUST	12
6	VI_0	GND_3	4
1	INHIBIT/UVLADJ	GND_2	7
14	TRACK	GND_1	8
11	SENSE-	GND_0	3

12V — L5 BLM31PG121SN1B — C399 330UF 16V — C397 330UF 16V — C417 10UF — GND

1V5

1V2_INHIBIT 1-8B,1-8E,2-1B — Q3 BSS138

ROUTE FROM LOAD

R145 3K4 — C416 10UF — C398 1000UF 2V5 — C396 1000UF 2V5 — I1V2 1-8E,1-9B,2-2B

DIRECT TO P8 ON PTH08T210W, DEDICATED TRACE

1V5

ROUTE FROM LOAD

PLACE RESISTOR CLOSE TO PTH08T210WAD
ROUTE SHORTEST

R146 TBD

U51 — PTH08T210WAD

13	TURBOTRANS	VO_0	5
10	SENSE+	VO_1	9
2	VI_1	VOADJUST	12
6	VI_0	GND_3	4
1	INHIBIT/UVLADJ	GND_2	7
14	TRACK	GND_1	8
11	SENSE-	GND_0	3

12V — L7 BLM31PG121SN1B — C404 330UF 16V — C406 330UF 16V — C420 10UF — GND

1V8

1V5_INHIBIT 1-8B,1-8E,2-1B — Q5 BSS138

ROUTE FROM LOAD

R147 TBD — C421 10UF — C405 1000UF 2V5 — C407 1000UF 2V5 — I1V5 1-8E,1-9B,2-2B

DIRECT TO P8 ON PTH08T210W, DEDICATED TRACE

1V8

ROUTE FROM LOAD

PLACE RESISTOR CLOSE TO PTH08T210WAD
ROUTE SHORTEST

R149 TBD

U52 — PTH08T210WAD

13	TURBOTRANS	VO_0	5
10	SENSE+	VO_1	9
2	VI_1	VOADJUST	12
6	VI_0	GND_3	4
1	INHIBIT/UVLADJ	GND_2	7
14	TRACK	GND_1	8
11	SENSE-	GND_0	3

12V — L14 BLM31PG121SN1B — C411 330UF 16V — C409 330UF 16V — C423 10UF — GND

2V5

1V8_INHIBIT 1-8B,1-8E,2-1B — Q6 BSS138

ROUTE FROM LOAD

R148 TBD — C422 10UF — C410 1000UF 2V5 — C408 1000UF 2V5 — I1V8 1-8E,1-9B,2-2B

DIRECT TO P8 ON PTH08T210W, DEDICATED TRACE

2V5

ROUTE FROM LOAD

PLACE RESISTOR CLOSE TO PTH08T210WAD
ROUTE SHORTEST

2V5_TRACK 1-8B,1-9E,2-6B — R183 1K

R177 TBD

U53 — PTH08T210WAD

13	TURBOTRANS	VO_0	5
10	SENSE+	VO_1	9
2	VI_1	VOADJUST	12
6	VI_0	GND_3	4
1	INHIBIT/UVLADJ	GND_2	7
14	TRACK	GND_1	8
11	SENSE-	GND_0	3

12V — L15 BLM31PG121SN1B — C412 330UF 16V — C414 330UF 16V — C424 10UF — C426 10UF — GND

2V5_INHIBIT 1-8B,1-9E,2-1B — Q7 BSS138

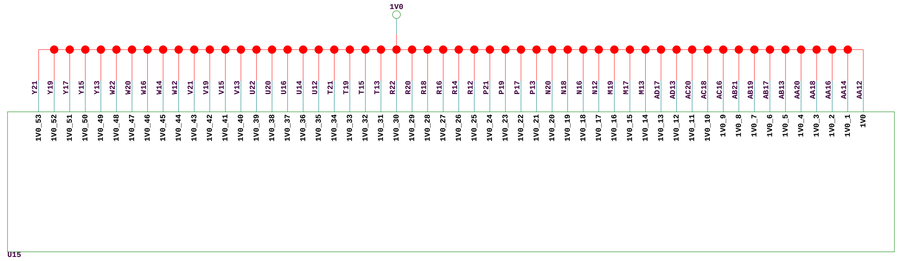
ROUTE FROM LOAD

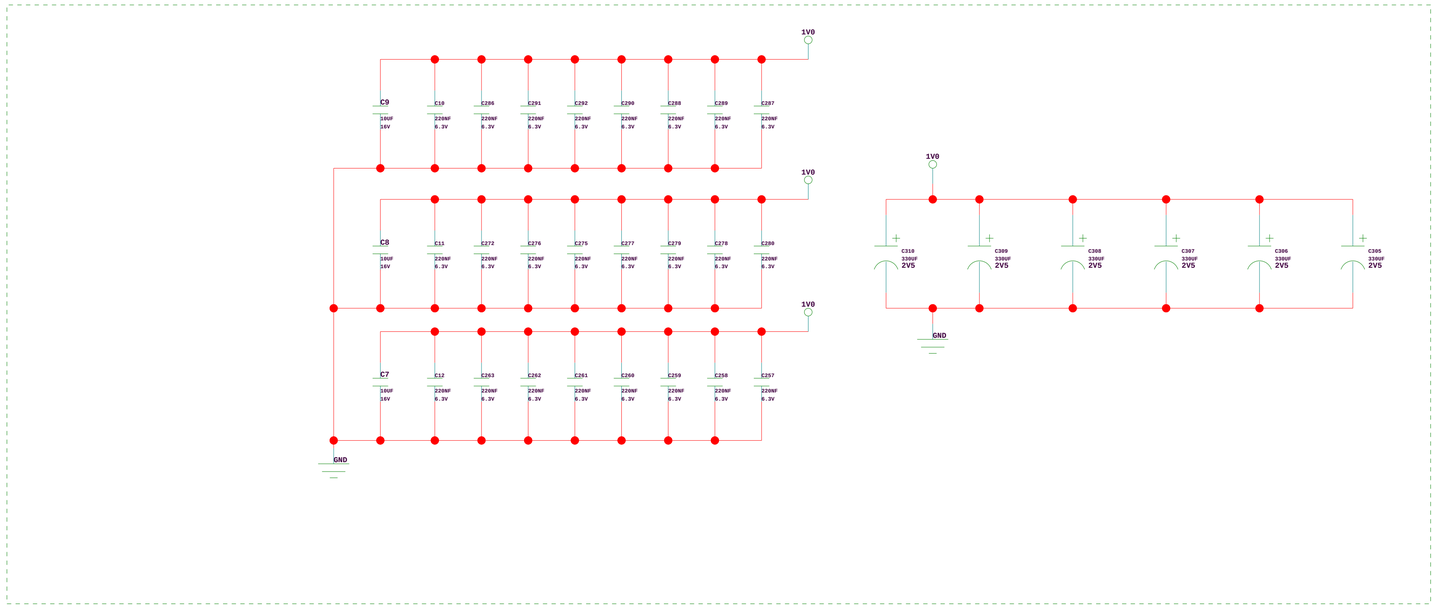
R179 TBD — C425 10UF 16V — C413 470UF 6.3V — C415 470UF 6.3V — I2V5 1-8E,1-9B,2-2B

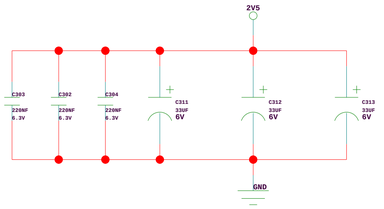
DIRECT TO P8 ON PTH08T210W, DEDICATED TRACE

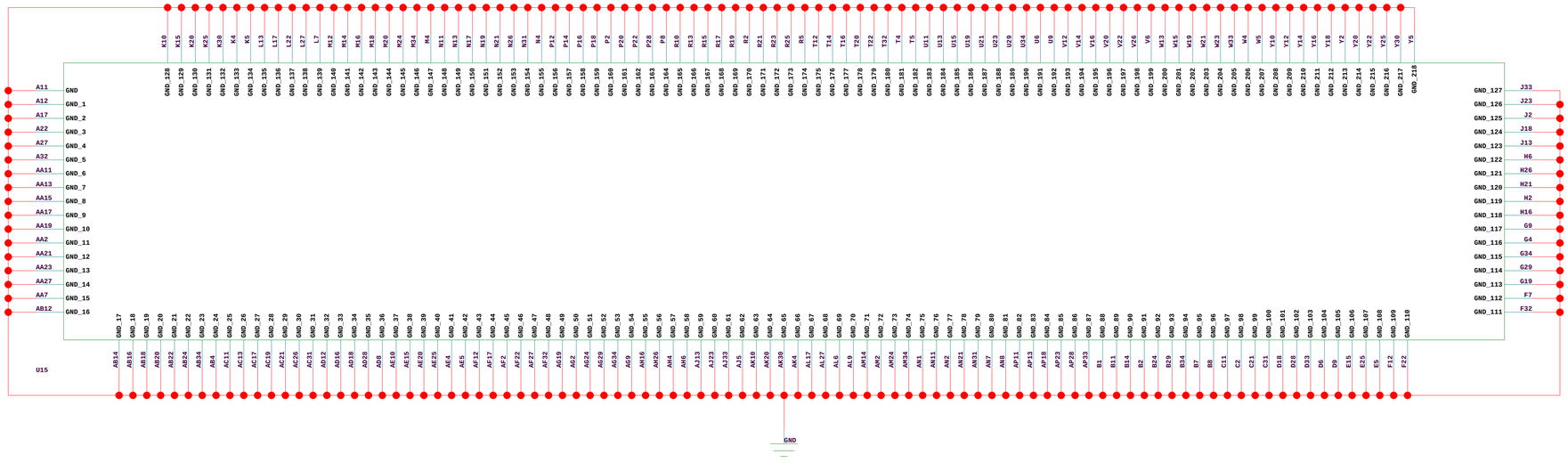
ADJUSTMENT AND T2 RESISTOR VALUES TBD
SOURCE VOLTAGES TO BE SELECTED

ROACH/iBOB2	ROACH_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE RW
10-22-2007_16:25 PATH PATH	DRAWN: F KAPP — APPR:
	CHECKED: E BAUERMEISTER — SHEET 3 OF 25









ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
10-22-2007_16:25 PATH PATH	

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

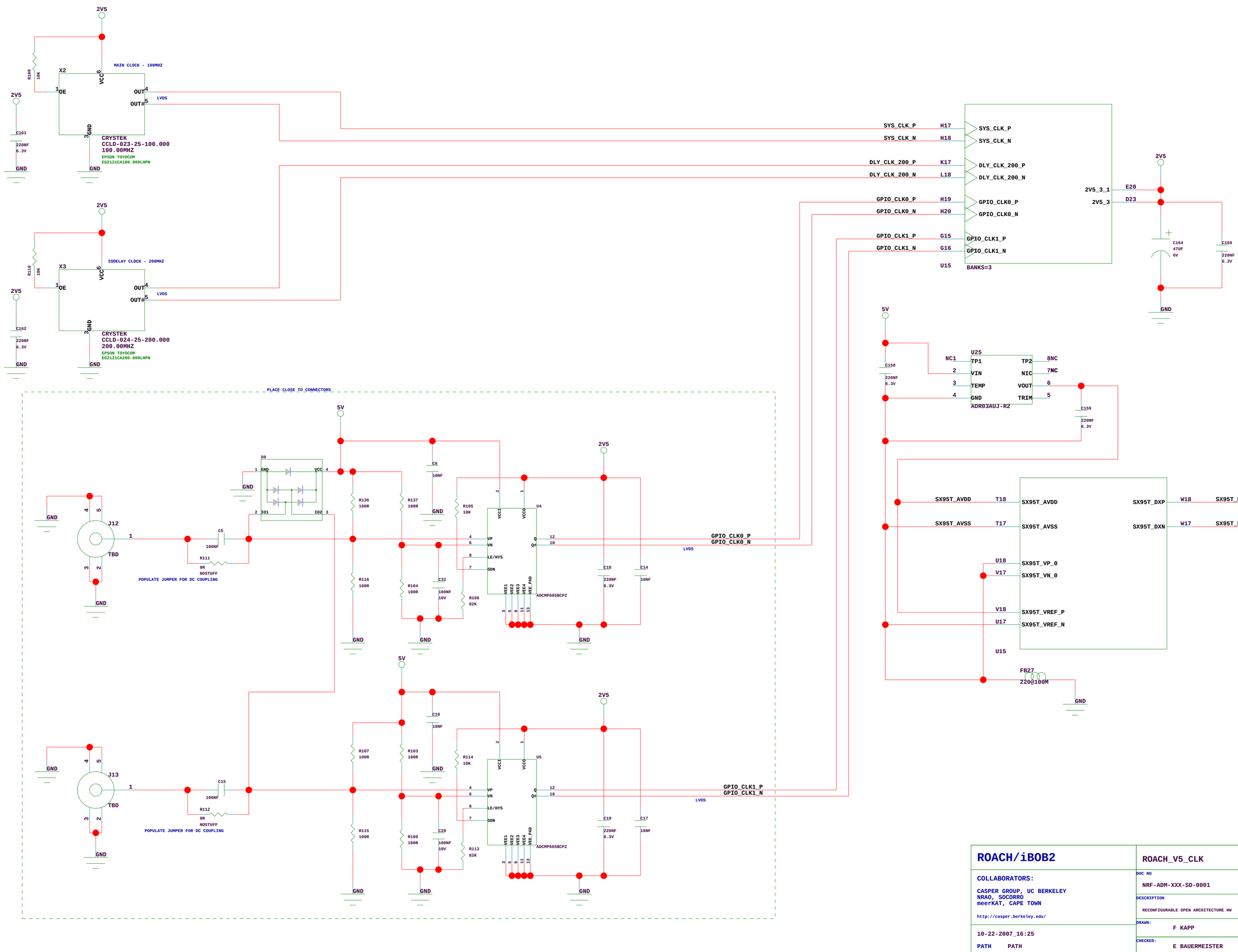
10-22-2007_16:25

PATH PATH

ROACH_ADC_0

DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 5 OF 25

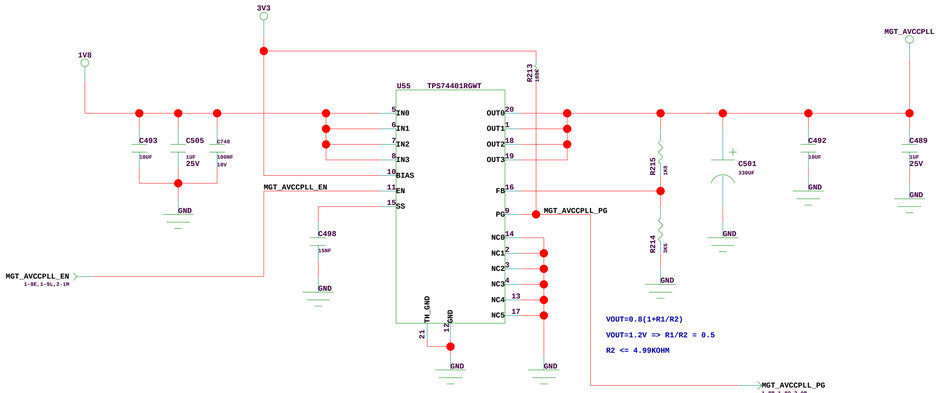
ROACH/iBOB2	**ROACH_ADC_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-22-2007_16:25 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 6 OF 25

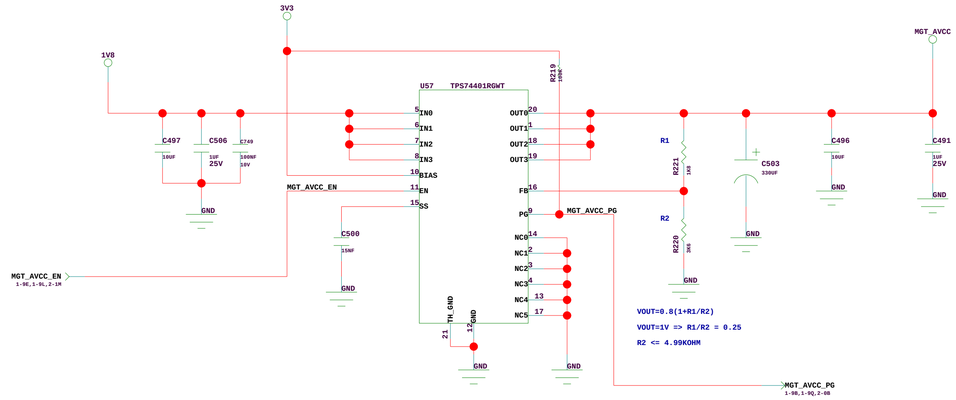


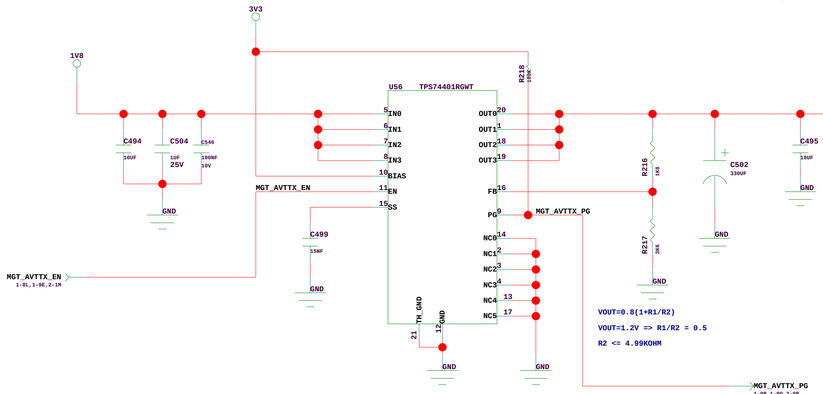
ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
10-22-2007_16:25 PATH PATH	

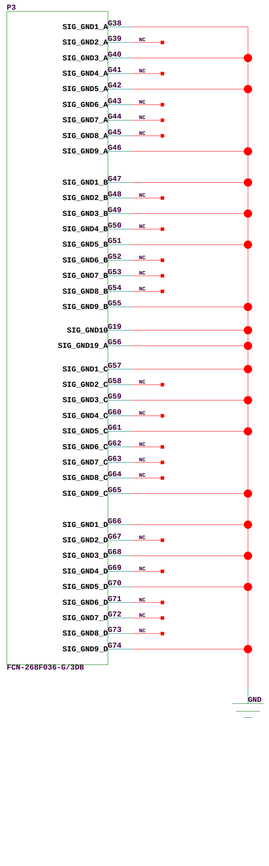
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB3 220@100M
FB4 220@100M
MGTAVCC_112 R3
MGTAVCC_112_1 R4
MGTAVCCPLL_112 T3
MGTAVTTRX_112 N3
MGTAVCC_112
MGTAVCC_112_1
MGTAVCCPLL_112
MGTAVTTRX_112
C84 220NF 6.3V
C93 220NF 6.3V
C92 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGT_112_REF_CLK_P P4
MGT_112_REF_CLK_N P3
MGT_112_REF_CLK_P
MGT_112_REF_CLK_N
MGTRX0_112_P N1
MGTRX0_112_N P1
MGTRX1_112_P T1
MGTRX1_112_N R1
MGTRX0_112_P
MGTRX0_112_N
MGTRX1_112_P
MGTRX1_112_N
U15
MGTRREF V4
MGT_VTRXC V5
MGTAVTTTX_112 M3
MGTAVTTTX_112_1 U3
MGTRREF
MGTAVTTRXC
MGTAVTTTX_112
MGTAVTTTX_112_1
R56 49.9R
MGT_AVTT
FB25 220@100M
FB5 220@100M
C125 220NF 6.3V
C95 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTTX0_112_P M2
MGTTX0_112_N N2
MGTTX1_112_P U2
MGTTX1_112_N T2
MGTTX0_112_P
MGTTX0_112_N
MGTTX1_112_P
MGTTX1_112_N
MGTTX0_112_P
MGTTX0_112_N
MGTTX1_112_P
MGTTX1_112_N
2V5
FB26 220@100M
C137 220NF 6.3V
R84 10K
X1
OE
VCC
OUT
OUT*
GND
JP6
CCLD-023-25-156.250
156.25MHZ
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
C104 10NF 25V
C105 10NF 25V
C106 10NF 25V
C107 10NF 25V
C109 10NF 25V
C108 10NF 25V
P3
SL0P S1
SL0N S2
SL1P S3
SL1N S4
SL2P S5
SL2N S6
SL3P S7
SL3N S8
SL6P S34
SL6N S33
SL5P S32
SL5N S31
SL4P S30
SL4N S29
SL3P S28
SL3N S27
SIG_GND1 G1
SIG_GND2 G2
SIG_GND3 G3
SIG_GND4 G4
SIG_GND5 G5
SIG_GND6 G6
SIG_GND7 G7
SIG_GND8 G8
SIG_GND9 G9
FCN-268F036-G/3DB
ODIS0
FAULT0
G4 AND G8 CONNECTED IN 2X2 MODULE
3V3
JP4
R50 10K
C130 10NF
C131 10NF
R79 150R
D2
OPTICAL MODULE FAULT - RED LED
R97 5K1
RS7 3K9
RS9 6K8
RS8 3K9
C127 10NF
U21 MAX9032AKA
U22 AND2 SN74AHC1G08DCKR
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB11 220@100M
FB9 220@100M
FB10 220@100M
MGTAVCC_114 AA3
MGTAVCC_114_1 AA4
MGTAVCCPLL_114 AB3
MGTAVTTRX_114 W3
MGTAVCC_114
MGTAVCC_114_1
MGTAVCCPLL_114
MGTAVTTRX_114
C102 220NF 6.3V
C101 220NF 6.3V
C100 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGT_114_REF_CLK_P NC Y4
MGT_114_REF_CLK_N NC Y3
MGT_114_REF_CLK_P
MGT_114_REF_CLK_N
MGTRX0_114_P W1
MGTRX0_114_N Y1
MGTRX1_114_P AB1
MGTRX1_114_N AA1
MGTRX0_114_P
MGTRX0_114_N
MGTRX1_114_P
MGTRX1_114_N
U15
C140 10NF 25V
C141 10NF 25V
C142 10NF 25V
C143 10NF 25V
MGTAVTTTX_114 AC3
MGTAVTTTX_114_1 V3
MGTAVTTTX_114
MGTAVTTTX_114_1
MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT
FB8 220@100M
C99 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTTX0_114_P V2
MGTTX0_114_N W2
MGTTX1_114_P AC2
MGTTX1_114_N AB2
MGTTX0_114_P
MGTTX0_114_N
MGTTX1_114_P
MGTTX1_114_N
U18 TPS2031D
R99 10K
C129 10NF
C128 100NF
C138 4.7UF 16V
C90 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB17 220@100M
FB15 220@100M
FB16 220@100M
MGTAVCC_116 J3
MGTAVCC_116_1 J4
MGTAVCCPLL_116 K3
MGTAVTTRX_116 G3
MGTAVCC_116
MGTAVCC_116_1
MGTAVCCPLL_116
MGTAVTTRX_116
C119 220NF 6.3V
C118 220NF 6.3V
C115 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGT_116_REF_CLK_P NC H4
MGT_116_REF_CLK_N NC H3
MGT_116_REF_CLK_P
MGT_116_REF_CLK_N
MGTRX0_116_P G1
MGTRX0_116_N H1
MGTRX1_116_P K1
MGTRX1_116_N J1
MGTRX0_116_P
MGTRX0_116_N
MGTRX1_116_P
MGTRX1_116_N
U15
C110 10NF 25V
C111 10NF 25V
C112 10NF 25V
C113 10NF 25V
MGTAVTTTX_116_1 L3
MGTAVTTTX_116 F3
MGTAVTTTX_116_1
MGTAVTTTX_116
MGT_AVTT
FB14 220@100M
C116 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTTX0_116_P F2
MGTTX0_116_N G2
MGTTX1_116_P L2
MGTTX1_116_N K2
MGTTX0_116_P
MGTTX0_116_N
MGTTX1_116_P
MGTTX1_116_N
P3
SL9P S19
SL9N S20
SL8P S21
SL8N S22
SL7P S23
SL7N S24
SL6P S25
SL6N S26
SL5P S34
SL5N S33
SL4P S32
SL4N S31
SL3P S30
SL3N S29
SL2P S28
SL2N S27
SIG_GND1 G10
SIG_GND2 G11
SIG_GND3 G12
SIG_GND4 G13
SIG_GND5 G14
SIG_GND6 G15
SIG_GND7 G16
SIG_GND8 G17
SIG_GND9 G18
FCN-268F036-G/3DB
ODIS1
FAULT1
G4 AND G8 CONNECTED IN 2X2 MODULE
3V3
JP5
R51 10K
C134 10NF
C132 10NF
R98 5K1
R93 3K9
R94 6K8
R95 3K9
C133 10NF
U20 MAX9032AKA
U23 AND2 SN74AHC1G08DCKR
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB22 220@100M
FB24 220@100M
FB23 220@100M
MGTAVCC_118 AG3
MGTAVCC_118_1 AG4
MGTAVCCPLL_118 AH3
MGTAVTTRX_118 AE3
MGTAVCC_118
MGTAVCC_118_1
MGTAVCCPLL_118
MGTAVTTRX_118
C123 220NF 6.3V
C114 220NF 6.3V
C125 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGT_118_REF_CLK_P NC AF4
MGT_118_REF_CLK_N NC AF3
MGT_118_REF_CLK_P
MGT_118_REF_CLK_N
MGTRX0_118_P AE1
MGTRX0_118_N AF1
MGTRX1_118_P AH1
MGTRX1_118_N AG1
MGTRX0_118_P
MGTRX0_118_N
MGTRX1_118_P
MGTRX1_118_N
U15
C144 10NF 25V
C145 10NF 25V
C146 10NF 25V
C147 10NF 25V
MGTAVTTTX_118_1 AJ3
MGTAVTTTX_118 AD3
MGTAVTTTX_118_1
MGTAVTTTX_118
MGT_AVTT
FB19 220@100M
C121 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTTX0_118_P AD2
MGTTX0_118_N AE2
MGTTX1_118_P AJ2
MGTTX1_118_N AH2
MGTTX0_118_P
MGTTX0_118_N
MGTTX1_118_P
MGTTX1_118_N
P3
SL12P S12
SL12N S11
SL13P S10
SL13N S9
SL14P S16
SL14N S15
SL15P S14
SL15N S13
SL16P S36
SL16N S35
SL17P S38
SL17N S37
SL18P S40
SL18N S39
SL19P S42
SL19N S41
SIG_GND1 G10
SIG_GND2 G11
SIG_GND3 G12
SIG_GND4 G13
SIG_GND5 G14
SIG_GND6 G15
SIG_GND7 G16
SIG_GND8 G17
SIG_GND9 G18
FCN-268F036-G/3DB
3V3
U19 TPS2031D
R100 10K
C135 10NF
C136 100NF
C139 4.7UF 16V
C91 22UF
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
10-22-2007_16:25
PATH PATH
ROACH_TRANSCEIVERS0_1
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
CHECKED: E BAUERMEISTER
APPR:
SHEET 8 OF 25

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB28
FB30
FB31
220@100M
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_120
MGTAVCCPLL_120
MGTAVTTRX_120
MGTAVTTTX_120
MGT_120_REF_CLK_P
MGT_120_REF_CLK_N
MGTRX0_120_P
MGTRX0_120_N
MGTRX1_120_P
MGTRX1_120_N
MGTTX0_120_P
MGTTX0_120_N
MGTTX1_120_P
MGTTX1_120_N
U15
2V5
FB52
C248
220NF
R.3V
R131
10K
X4
OE
VCC
OUT
GND
JP9
CCLD-023-25-156.250
156.25MHZ
MGT_REFCLK_Q2_P
MGT_REFCLK_Q2_N
C181
C182
C183
C184
C186
C185
10NF
25V
FB32
C173
FB38
FB36
FB37
C179
C178
C177
C251
C252
C250
C249
FB44
FB42
FB43
C220
C215
C212
FB41
C213
C187
C188
C189
C190
FB49
FB51
FB50
C225
C191
C226
C256
C255
C254
C253
P3
S39
S40
S41
S42
S43
S44
S45
S46
S54
S53
S52
S51
S50
S49
S48
S47
DL0P
DL0N
DL1P
DL1N
DL2P
DL2N
DL3P
DL3N
SL0P
SL0N
SL1P
SL1N
SL2P
SL2N
SL3P
SL3N
FCN-268F036-G/3DB
SIG_GND1
SIG_GND2
SIG_GND3
SIG_GND4
SIG_GND5
SIG_GND6
SIG_GND7
SIG_GND8
SIG_GND9
G20
G21
G22
G23
G24
G25
G26
G27
G28
ODIS2
FAULT2
FAULT3
G4 AND G8 CONNECTED IN 2X2 MODULE
JP7
JP8
R123
10K
R124
10K
C240
C242
C245
C243
3V3
R132
150R
OPTICAL MODULE FAULT - RED LED
R121
5K1
R120
3K9
R126
5K1
R127
3K9
U34
U30
MAX9032AKA
R119
6K8
R118
3K9
R128
6K8
R129
3K9
C241
C244
U36
U37
AND2
SN74AHC1G08DCKR
U28
U29
TPS2031D
R130
10K
R117
10K
C246
C247
C168
C166
C239
C227
C167
C165
10NF
100NF
4.7UF
16V
22UF
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
10-22-2007_16:25
PATH
ROACH_TRANSCEIVERS2_3
DOC NO
NRF-ADM-XXX-SD-0001
REVISION
A
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:
F KAPP
APPR:
CHECKED:
E BAUERMEISTER
SHEET
9 OF 25

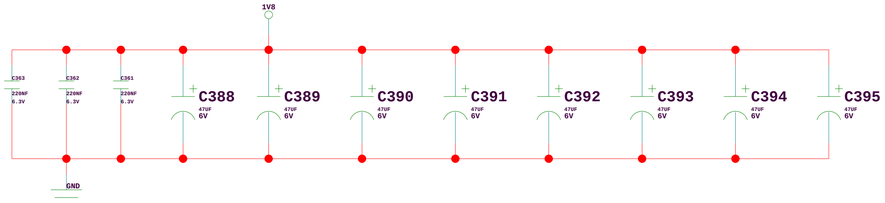


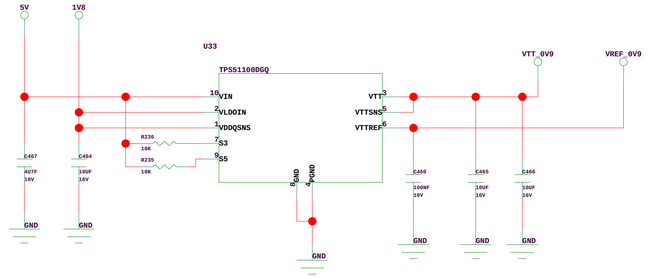


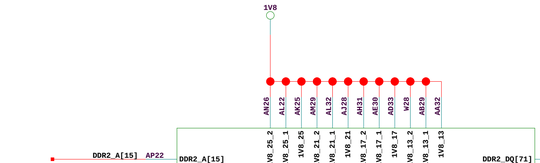


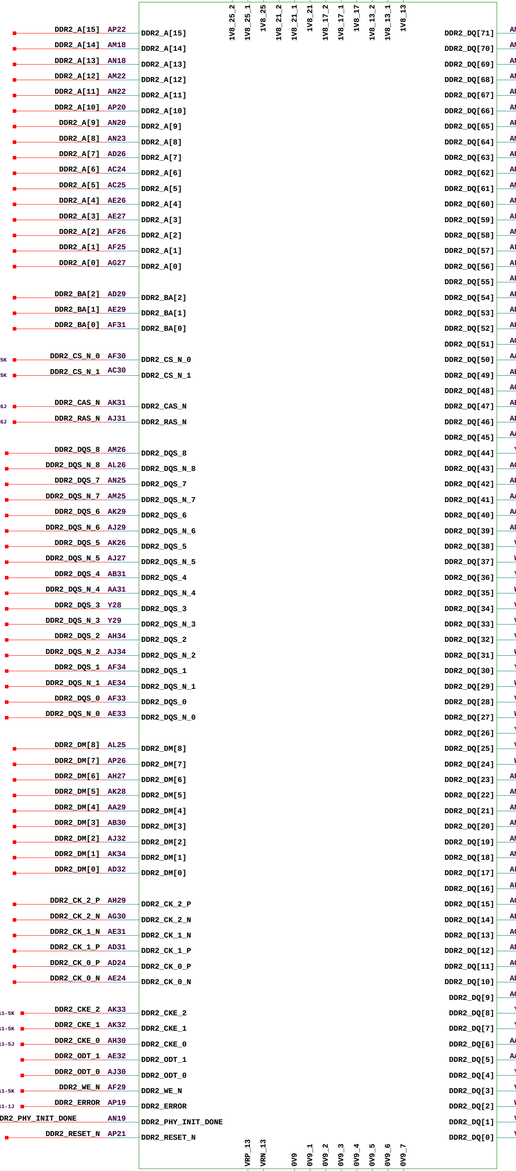


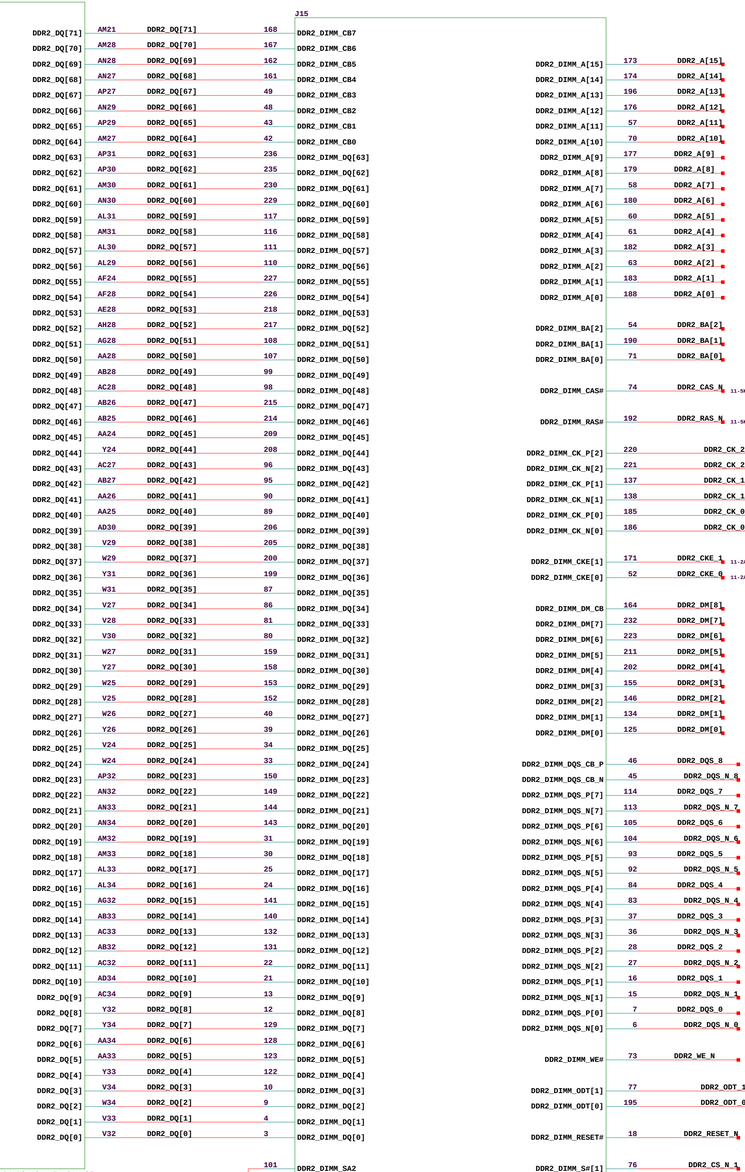
ROACH/iBOB2	ROACH_TRANSCEIVERS_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-22-2007_16:25	DRAWN: F KAPP · APPR:
PATH PATH	CHECKED: E BAUERMEISTER · SHEET 10 OF 25

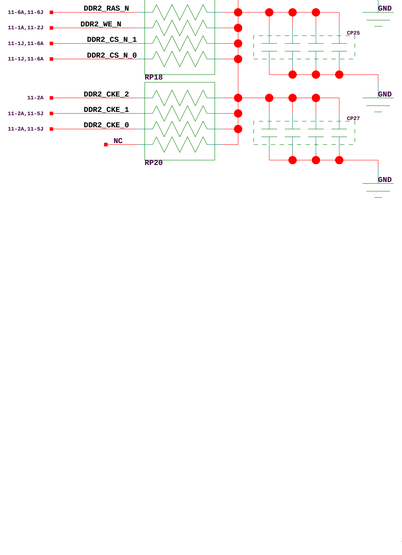


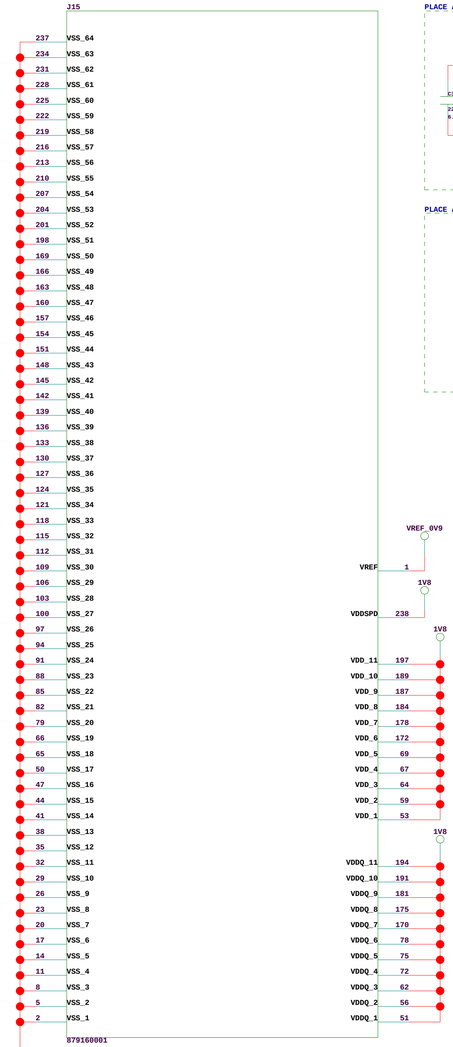


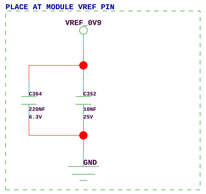


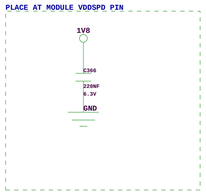


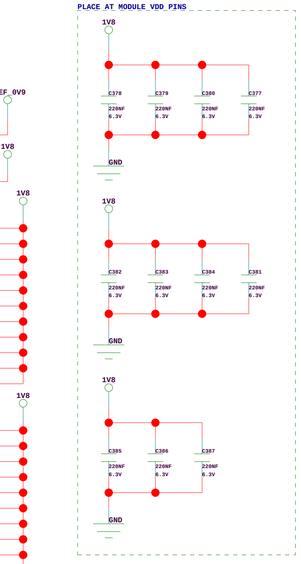


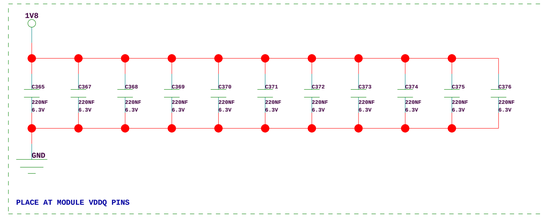




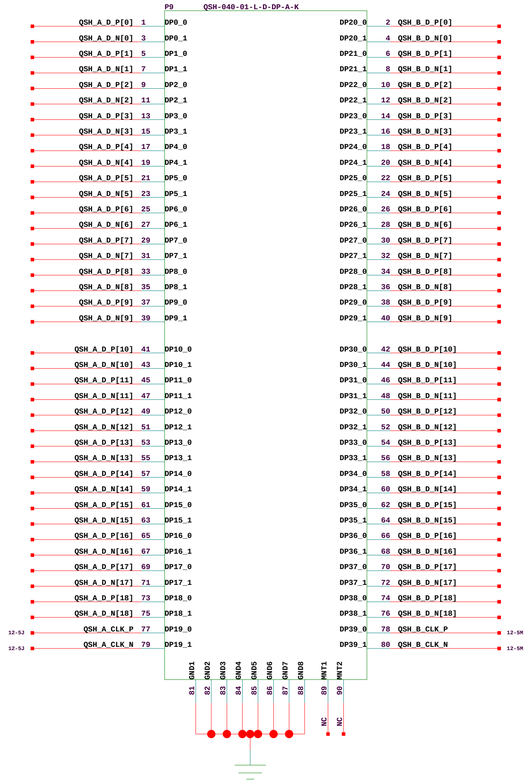


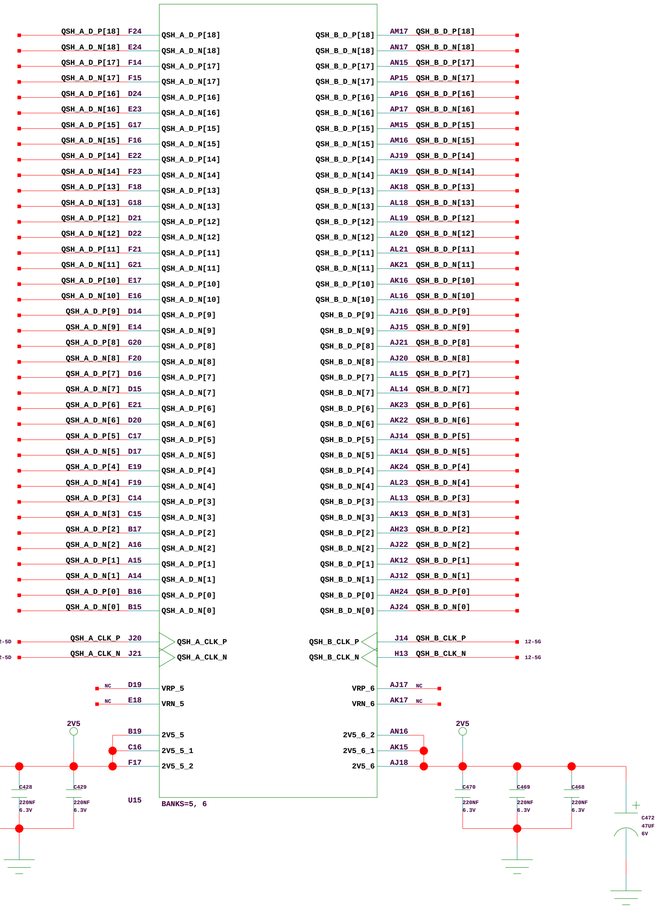






ROACH/iBOB2	**ROACH_DDR2_DIMM**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-22-2007_16:25 PATH PATH	DRAWN: F KAPP APPR:
	CHECKED: E BAUERMEISTER SHEET 11 OF 25





ROACH/iBOB2	**ROACH_DIFF_GPIO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-22-2007_16:25 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 12 OF 25

GPIOLVC18[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

GPIOLVC18[20] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

IO VOLTAGE LEVEL SELECT	
1-2: 3.3V	DEFAULT
2-3: 2.5V	

GPIOLVC18[4] IS DUAL FUNCTION:
1. DRIVES LED
2. CONTROLS DIRECTION ON GPIOLVC33[1-4]

IF CR18 IS ON, CLOCK CAPABLE GPIO'S ARE OUTPUTS

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

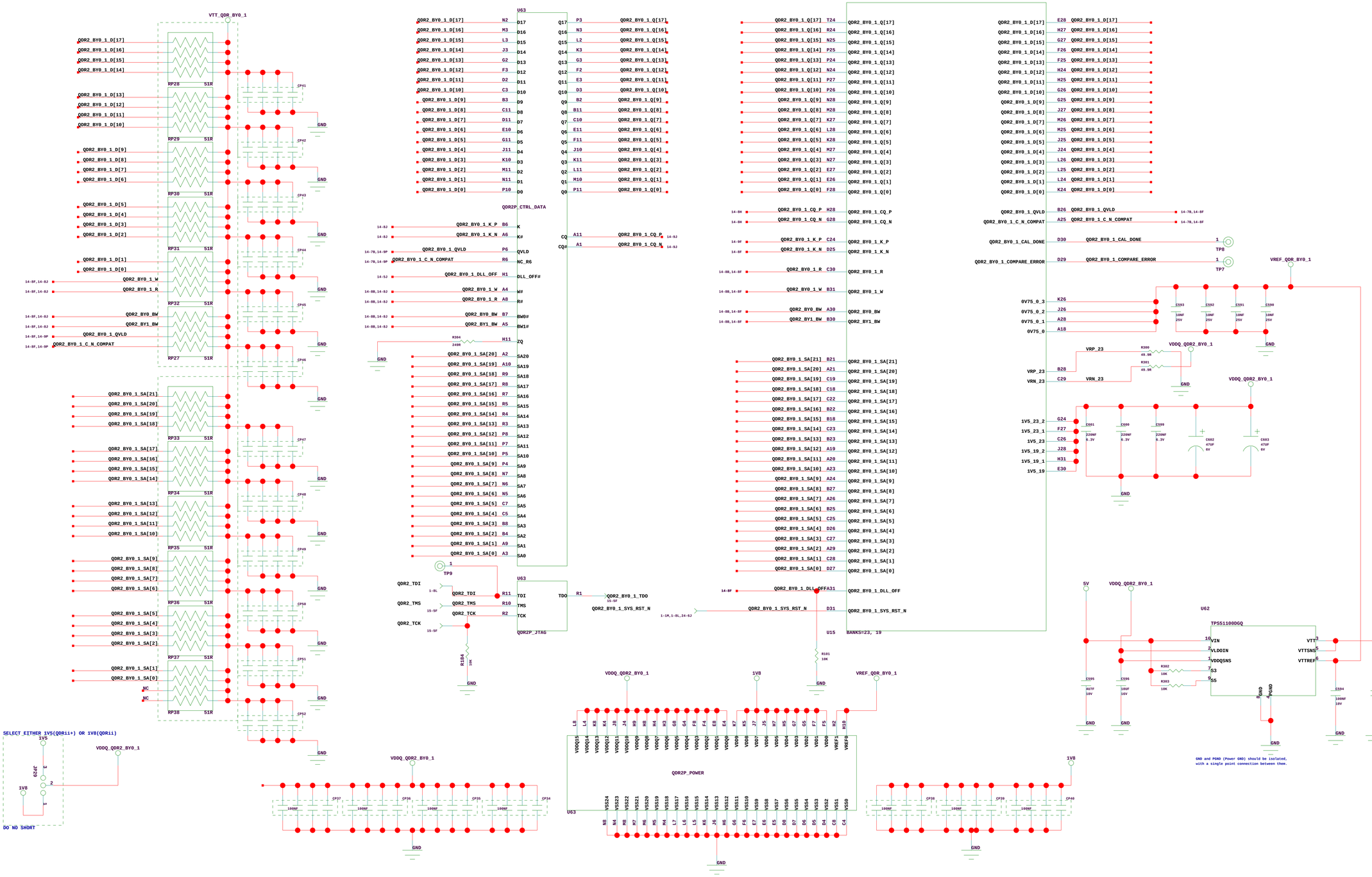
http://casper.berkeley.edu/

10-22-2007_16:25

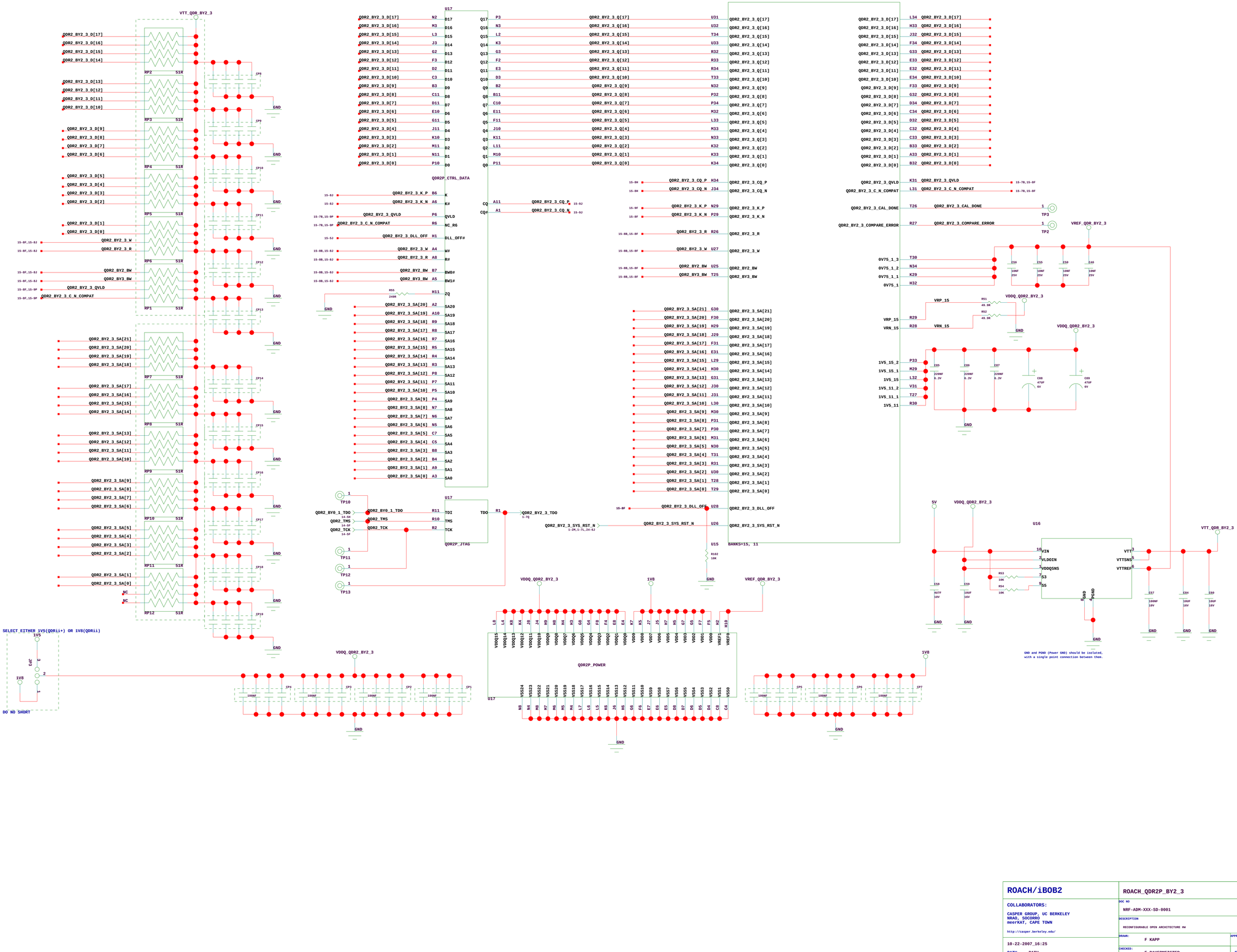
PATH PATH

ROACH_GPIO_MISC

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	13 OF 25

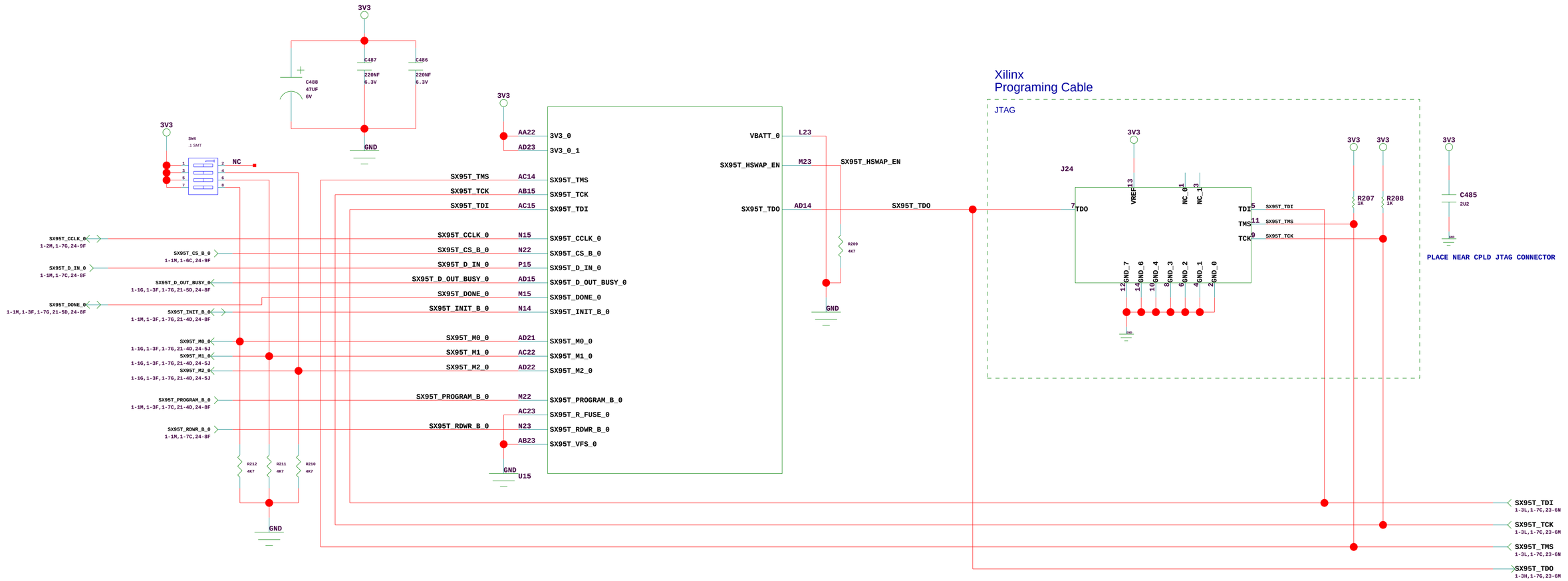


ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS:	DOC NO: NRF-ADM-XXX-SD-0001
CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN	REVISION: A
http://casper.berkeley.edu/	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-22-2007_16:25	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET: 14 OF 25

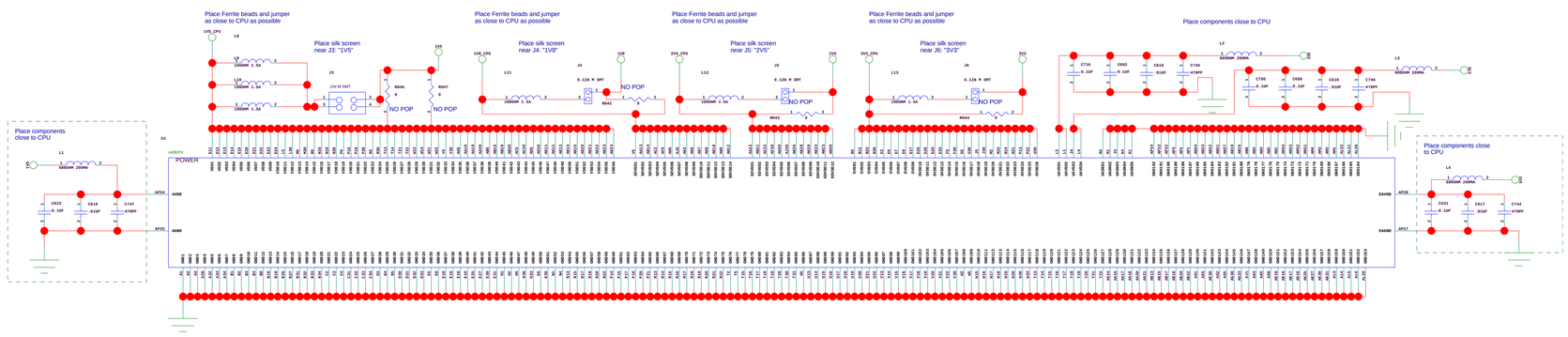

VTT_QDR_BY2_3
RP1 51R
RP2 51R
RP3 51R
RP4 51R
RP5 51R
RP6 51R
RP7 51R
RP8 51R
RP9 51R
RP10 51R
RP11 51R
RP12 51R
CP1 CP2 CP3 CP4 CP5 CP6 CP7 CP8 CP9 CP10 CP11 CP12 CP13 CP14 CP15 CP16 CP17 CP18 CP19
GND
QDR2_BY2_3_D[17] QDR2_BY2_3_D[16] QDR2_BY2_3_D[15] QDR2_BY2_3_D[14]
QDR2_BY2_3_D[13] QDR2_BY2_3_D[12] QDR2_BY2_3_D[11] QDR2_BY2_3_D[10]
QDR2_BY2_3_D[9] QDR2_BY2_3_D[8] QDR2_BY2_3_D[7] QDR2_BY2_3_D[6]
QDR2_BY2_3_D[5] QDR2_BY2_3_D[4] QDR2_BY2_3_D[3] QDR2_BY2_3_D[2]
QDR2_BY2_3_D[1] QDR2_BY2_3_D[0]
QDR2_BY2_3_W
QDR2_BY2_3_R
QDR2_BY2_BW
QDR3_BY3_BW
QDR2_BY2_3_QVLD
QDR2_BY2_3_C_N_COMPAT
QDR2_BY2_3_SA[21] QDR2_BY2_3_SA[20] QDR2_BY2_3_SA[19] QDR2_BY2_3_SA[18]
QDR2_BY2_3_SA[17] QDR2_BY2_3_SA[16] QDR2_BY2_3_SA[15] QDR2_BY2_3_SA[14]
QDR2_BY2_3_SA[13] QDR2_BY2_3_SA[12] QDR2_BY2_3_SA[11] QDR2_BY2_3_SA[10]
QDR2_BY2_3_SA[9] QDR2_BY2_3_SA[8] QDR2_BY2_3_SA[7] QDR2_BY2_3_SA[6]
QDR2_BY2_3_SA[5] QDR2_BY2_3_SA[4] QDR2_BY2_3_SA[3] QDR2_BY2_3_SA[2]
QDR2_BY2_3_SA[1] QDR2_BY2_3_SA[0]
NC
NC
SELECT_EITHER_1V5(QDRii+) OR 1V8(QDRii)
1V5
1V8
JP3
DO NOT SHORT
VDDQ_QDR2_BY2_3
100NF
U17
QDR2P_CTRL_DATA
QDR2_BY2_3_K_P
QDR2_BY2_3_K_N
QDR2_BY2_3_QVLD
QDR2_BY2_3_C_N_COMPAT
QDR2_BY2_3_DLL_OFF
QDR2_BY2_3_W
QDR2_BY2_3_R
QDR2_BY2_BW
QDR3_BY3_BW
RS5 249R
QDR2_BY2_3_SA[20] QDR2_BY2_3_SA[19] QDR2_BY2_3_SA[18] QDR2_BY2_3_SA[17]
QDR2_BY2_3_SA[16] QDR2_BY2_3_SA[15] QDR2_BY2_3_SA[14] QDR2_BY2_3_SA[13]
QDR2_BY2_3_SA[12] QDR2_BY2_3_SA[11] QDR2_BY2_3_SA[10] QDR2_BY2_3_SA[9]
QDR2_BY2_3_SA[8] QDR2_BY2_3_SA[7] QDR2_BY2_3_SA[6] QDR2_BY2_3_SA[5]
QDR2_BY2_3_SA[4] QDR2_BY2_3_SA[3] QDR2_BY2_3_SA[2] QDR2_BY2_3_SA[1]
QDR2_BY2_3_SA[0]
TP10 TP11 TP12 TP13
QDR2_BY0_1_TDO
QDR2_TMS
QDR2_TCK
QDR2P_JTAG
QDR2_BY2_3_TDO
QDR2_BY2_3_SYS_RST_N
QDR2_BY2_3_Q[17] QDR2_BY2_3_Q[16] QDR2_BY2_3_Q[15] QDR2_BY2_3_Q[14]
QDR2_BY2_3_Q[13] QDR2_BY2_3_Q[12] QDR2_BY2_3_Q[11] QDR2_BY2_3_Q[10]
QDR2_BY2_3_Q[9] QDR2_BY2_3_Q[8] QDR2_BY2_3_Q[7] QDR2_BY2_3_Q[6]
QDR2_BY2_3_Q[5] QDR2_BY2_3_Q[4] QDR2_BY2_3_Q[3] QDR2_BY2_3_Q[2]
QDR2_BY2_3_Q[1] QDR2_BY2_3_Q[0]
QDR2_BY2_3_CQ_P
QDR2_BY2_3_CQ_N
QDR2_BY2_3_DLL_OFF
R102 10K
BANKS=15, 11
QDR2P_POWER
1V8
VREF_QDR_BY2_3
5V
U16
VIN VLDOIN VDDQSNS S3 S5 PGND GND VTT VTTSNS VTTREF
RS3 10K
RS4 10K
VTT_QDR_BY2_3
GND and PGND (Power GND) should be isolated, with a single point connection between them.
TP3
TP2
0V75_1_3 0V75_1_2 0V75_1_1 0V75_1
VRP_15 VRN_15
RS1 49.9R
RS2 49.9R
1V5_15_2 1V5_15_1 1V5_15 1V5_11_2 1V5_11_1 1V5_11
220NF 6.3V
10NF 25V
10UF 16V
4U7F 10V
100NF 10V
47UF 6V
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
10-22-2007_16:25
PATH PATH
ROACH_QDR2P_BY2_3
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
CHECKED: E BAUERMEISTER
APPR:
SHEET 15 OF 25

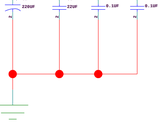
TBD

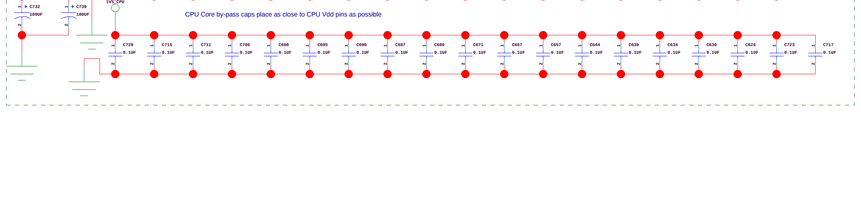
VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

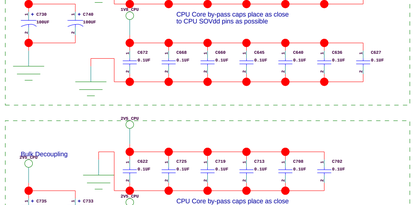


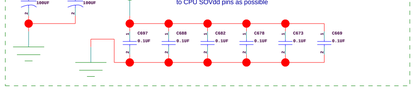
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
10-22-2007_16:25 PATH PATH	

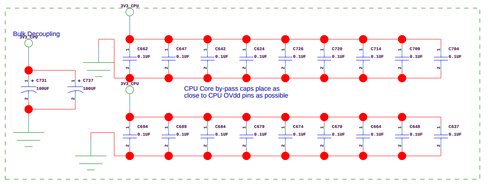


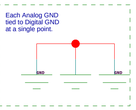




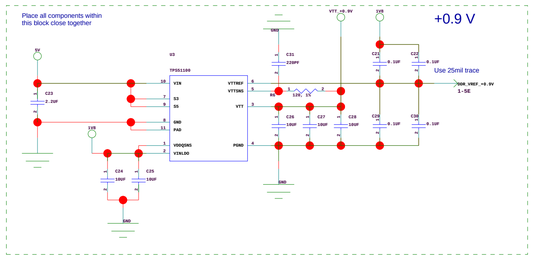


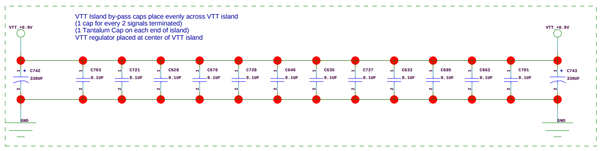






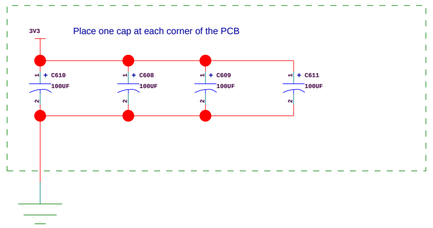
REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS





ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 17 OF 25
10-22-2007_16:25	
PATH PATH	

REMOVED 3V3 GENERATION



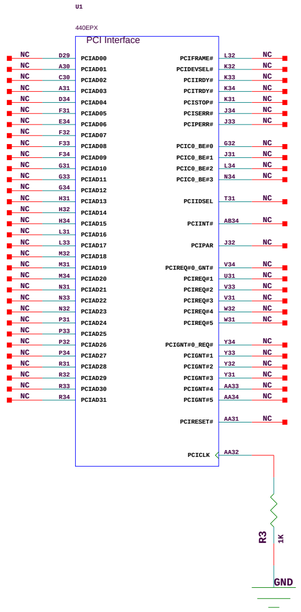
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	**ROACH_PPC_POWER_2**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET: 18 OF 25
10-22-2007_16:25 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-22-2007_16:25 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups. Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

Place nearest PHY pin 96

Place nearest PHY pin 101

Place nearest PHY pin 98

Place nearest PHY pin 100

Place as close to PHY CORE VDD power pins as possible

Place as close to PHY IO VDD power pins as possible

UNUSED SECOND ETHERNET MAC

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place jumpers in line with signals

Place decoupling C close to termination R All traces 50Ohm WRT GND or 2V5

Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY

NOSTUFF

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

ROACH/iBOB2	ROACH_PPC_ETH1
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
10-22-2007_16:25	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 20 OF 25

U1

USB 2.0 DEVICE

440EPX

USB2CLK — A5 — NC

GPIO28/USB2TXVAL — C6 — NC
USB2TXRDY_REFEN — B6 — NC
USB2RXACT_HOLDREQ_RCVINH — D7 — NC
USB2RXVAL_LEAKTEST2 — C8 — NC
GPIO27/USB2RXERR_EXTREQ# — A4

GPIO30/USB2XCVRSEL_EXTACK# — M3
GPIO31/USB2TERMSEL_BUSREQ — P4
USB2LS0_DRVINH1 — R2 — NC
USB2LS1_LEAKTEST_HOLDPRI — P1 — NC
GPIO32/USB2OM0 — R3
GPIO33/USB2OM1 — R4
GPIO29/USB2SUSP_HOLDACK — C5

USB 2.0 PHY
HOST/DEVICE

USB2XCVR — J2 — USB2_XCVR_D+
USB2XCVR# — J1 — USB2_XCVR_D-
USB2REXT — L3 — R182 3.40K, 1%
USB2XTAL — N2
USB2XTAL# — N3

CLK_USB2.0_48MHZ
1-3B,1-3L,23-4G

SX95T_D_OUT_BUSY_0 → SX95T_D_OUT_BUSY_0 1-1G,1-3F,1-7G,16-4B,24-8F
SX95T_DONE_0 → SX95T_DONE_0 1-1M,1-3F,1-7G,24-8F
SX95T_INIT_B_0 → SX95T_INIT_B_0 1-1M,1-3F,1-7G,24-8F
SX95T_M0_0 → SX95T_M0_0 1-1G,1-3F,1-7G,16-3B,24-5J
SX95T_M1_0 → SX95T_M1_0 1-1G,1-3F,1-7G,16-3B,24-5J
SX95T_M2_0 → SX95T_M2_0 1-1G,1-3F,1-7G,16-3B,24-5J
SX95T_PROGRAM_B_0 → SX95T_PROGRAM_B_0 1-1M,1-3F,1-7C,16-3B,24-8F

NOTE:

USB HOST ONLY

5V — PTC1 1206L050 500MA — C614 220UF 10V — C612 100NF 10V — C613 1NF 50V

CRITICAL PLACEMENT

Place SP2 very close to P6

SP2 — PGB102ST23WR — CHASSIS_GND

P6 1X4 USBA
1 VCC
2 D-
3 D+
4 GND
5, 6
292303-1

VR4 5.5V 20A
VR3 5.5V 20A

CHASSIS_GND

ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-22-2007_16:25 PATH PATH	DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET 21 OF 25

DDR_PA[15:0]

DDR_PD0[63:0]

U1

DDR SDRAM

64DEPX

DDR_PD0	AB2	MEMDATA00	
DDR_PD1	AF2	MEMDATA01	
DDR_PD2	AK5	MEMDATA02	
DDR_PD3	AL28	MEMDATA03	
DDR_PD4	AL22	MEMDATA04	
DDR_PD5	AK22	MEMDATA05	
DDR_PD6	AK21	MEMDATA06	
DDR_PD7	AP21	MEMDATA07	
DDR_PD8	AP28	MEMDATA08	
DDR_PD9	AL18	MEMDATA09	
DDR_PD10	AK17	MEMDATA10	
DDR_PD11	AP17	MEMDATA11	
DDR_PD12	AN28	MEMDATA12	
DDR_PD13	AP18	MEMDATA13	
DDR_PD14	AK18	MEMDATA14	
DDR_PD15	AP16	MEMDATA15	
DDR_PD16	AM16	MEMDATA16	
DDR_PD17	AP15	MEMDATA17	
DDR_PD18	AL15	MEMDATA18	
DDR_PD19	AP14	MEMDATA19	
DDR_PD20	AL17	MEMDATA20	
DDR_PD21	AM17	MEMDATA21	
DDR_PD22	AK15	MEMDATA22	
DDR_PD23	AM15	MEMDATA23	
DDR_PD24	AP13	MEMDATA24	
DDR_PD25	AK13	MEMDATA25	
DDR_PD26	AP12	MEMDATA26	
DDR_PD27	AL12	MEMDATA27	
DDR_PD28	AK14	MEMDATA28	
DDR_PD29	AK11	MEMDATA29	
DDR_PD30	AL13	MEMDATA30	
DDR_PD31	AM12	MEMDATA31	
DDR_PD32	AF3	MEMDATA32	
DDR_PD33	AF1	MEMDATA33	
DDR_PD34	AD4	MEMDATA34	
DDR_PD35	AD3	MEMDATA35	
DDR_PD36	AB3	MEMDATA36	
DDR_PD37	AF2	MEMDATA37	
DDR_PD38	AE2	MEMDATA38	
DDR_PD39	AE1	MEMDATA39	
DDR_PD40	AC3	MEMDATA40	
DDR_PD41	AC1	MEMDATA41	
DDR_PD42	AA4	MEMDATA42	
DDR_PD43	AA3	MEMDATA43	
DDR_PD44	AD2	MEMDATA44	
DDR_PD45	AC4	MEMDATA45	
DDR_PD46	AB1	MEMDATA46	
DDR_PD47	AB2	MEMDATA47	
DDR_PD48	Y3	MEMDATA48	
DDR_PD49	Y2	MEMDATA49	
DDR_PD50	Y4	MEMDATA50	
DDR_PD51	V3	MEMDATA51	
DDR_PD52	AA2	MEMDATA52	
DDR_PD53	AA1	MEMDATA53	
DDR_PD54	W3	MEMDATA54	
DDR_PD55	W1	MEMDATA55	
DDR_PD56	V1	MEMDATA56	
DDR_PD57	U2	MEMDATA57	
DDR_PD58	T4	MEMDATA58	
DDR_PD59	R1	MEMDATA59	
DDR_PD60	V3	MEMDATA60	
DDR_PD61	V1	MEMDATA61	
DDR_PD62	T3	MEMDATA62	
DDR_PD63	T1	MEMDATA63	

		MEMADDR00	DDR_PA0
		MEMADDR01	DDR_PA1
		MEMADDR02	DDR_PA2
		MEMADDR03	DDR_PA3
		MEMADDR04	DDR_PA4
		MEMADDR05	DDR_PA5
		MEMADDR06	DDR_PA6
		MEMADDR07	DDR_PA7
		MEMADDR08	DDR_PA8
		MEMADDR09	DDR_PA9
		MEMADDR10	DDR_PA10
		MEMADDR11	DDR_PA11
		MEMADDR12	DDR_PA12
		MEMADDR13	DDR_PA13
AJ23		BA0	DDR_PBA0
AK3		BA1	DDR_PBA1
AP8		BA2	DDR_PBA2
AJ24		RAS#	DDR_PRAS#
AN4		CAS#	DDR_PCAS#
AJ2		WE#	DDR_PWE#
AL21		DM0	DDR_PDM0
AP18		DM1	DDR_PDM1
AP15		DM2	DDR_PDM2
AL14		DM3	DDR_PDM3
AD4		DM4	DDR_PDM4
AB3		DM5	DDR_PDM5
T5		DM6	DDR_PDM6
E3		DM7	DDR_PDM7
AN18		DM8	DDR_PDM8
AR21		DQS0	DDR_PDQS0
AM19		DQS1	DDR_PDQS1
AL16		DQS2	DDR_PDQS2
AM13		DQS3	DDR_PDQS3
AE3		DQS4	DDR_PDQS4
AN4		DQS5	DDR_PDQS5
W3		DQS6	DDR_PDQS6
T4		DQS7	DDR_PDQS7
AP10		DQS8	DDR_PDQS8
AN3		MEMODT0	DDR_PODT0
AR1		MEMODT1	DDR_PODT1
AN2		BANKSELA0	DDR_PCS0#
AM1		BANKSELA1	DDR_PCS1#
AN9		MEMCLKEN	DDR_PCKE
AL1		MEMCLKOUT	DDR_CLKOUT
AR1		MEMCLKOUT#	DDR_CLKOUT#

R213 500ps Loop

		ECC0	PPC_ECC0
		ECC1	PPC_ECC1
		ECC2	PPC_ECC2
		ECC3	PPC_ECC3
		ECC4	PPC_ECC4
		ECC5	PPC_ECC5
		ECC6	PPC_ECC6
		ECC7	PPC_ECC7

22-9F, 22-9F, 22-9F, 22-10F, 22-10F, 22-10F, 22-10F, 22-10F

		SVREF1A	
		SVREF1B	
		SVREF2A	
		SVREF2B	

DDR_VREF_0V9

5V

1V8

C158 0.10F

C148 0.10F

C151 0.10F 0402

C152 0.10F 0402

C148 0.01F

Place parts as close to CPU as possible

U32

10	VIN	VTT	3
2	VLDOIN	VTTSNS	5
1	VDDQSNS	VTTREF	6
7	S3		
9	S5		
8	GND	PGND	4

R230 10K

R229 10K

C459 .047F 10V

C456 10UF 16V

C453 100NF 10V

C457 10UF 16V

C458 10UF 16V

DDR_VTT

DDR_VREF_0V9

GND

J8

22-6D	PPC_ECC7	168
22-6D	PPC_ECC6	167
22-7D	PPC_ECC5	162
22-7D	PPC_ECC4	161
22-7D	PPC_ECC3	49
22-7D	PPC_ECC2	48
22-7D	PPC_ECC1	43
22-7D	PPC_ECC0	42
DDR_PDQ63		236
DDR_PDQ62		235
DDR_PDQ61		230
DDR_PDQ60		229
DDR_PDQ59		117
DDR_PDQ58		116
DDR_PDQ57		111
DDR_PDQ56		110
DDR_PDQ55		227
DDR_PDQ54		226
DDR_PDQ53		218
DDR_PDQ52		217
DDR_PDQ51		108
DDR_PDQ50		107
DDR_PDQ49		99
DDR_PDQ48		98
DDR_PDQ47		215
DDR_PDQ46		214
DDR_PDQ45		209
DDR_PDQ44		208
DDR_PDQ43		96
DDR_PDQ42		95
DDR_PDQ41		90
DDR_PDQ40		89
DDR_PDQ39		206
DDR_PDQ38		205
DDR_PDQ37		200
DDR_PDQ36		199
DDR_PDQ35		87
DDR_PDQ34		86
DDR_PDQ33		81
DDR_PDQ32		80
DDR_PDQ31		159
DDR_PDQ30		158
DDR_PDQ29		153
DDR_PDQ28		152
DDR_PDQ27		40
DDR_PDQ26		39
DDR_PDQ25		34
DDR_PDQ24		33
DDR_PDQ23		150
DDR_PDQ22		149
DDR_PDQ21		144
DDR_PDQ20		143
DDR_PDQ19		31
DDR_PDQ18		30
DDR_PDQ17		25
DDR_PDQ16		24
DDR_PDQ15		141
DDR_PDQ14		140
DDR_PDQ13		132
DDR_PDQ12		131
DDR_PDQ11		22
DDR_PDQ10		21
DDR_PDQ9		13
DDR_PDQ8		12
DDR_PDQ7		129
DDR_PDQ6		128
DDR_PDQ5		123
DDR_PDQ4		122
DDR_PDQ3		10
DDR_PDQ2		9
DDR_PDQ1		4
DDR_PDQ0		3
	DDR2_DIMM_CB7	
	DDR2_DIMM_CB6	
	DDR2_DIMM_CB5	
	DDR2_DIMM_CB4	
	DDR2_DIMM_CB3	
	DDR2_DIMM_CB2	
	DDR2_DIMM_CB1	
	DDR2_DIMM_CB0	
	DDR2_DIMM_DQ[63]	
	DDR2_DIMM_DQ[62]	
	DDR2_DIMM_DQ[61]	
	DDR2_DIMM_DQ[60]	
	DDR2_DIMM_DQ[59]	
	DDR2_DIMM_DQ[58]	
	DDR2_DIMM_DQ[57]	
	DDR2_DIMM_DQ[56]	
	DDR2_DIMM_DQ[55]	
	DDR2_DIMM_DQ[54]	
	DDR2_DIMM_DQ[53]	
	DDR2_DIMM_DQ[52]	
	DDR2_DIMM_DQ[51]	
	DDR2_DIMM_DQ[50]	
	DDR2_DIMM_DQ[49]	
	DDR2_DIMM_DQ[48]	
	DDR2_DIMM_DQ[47]	
	DDR2_DIMM_DQ[46]	
	DDR2_DIMM_DQ[45]	
	DDR2_DIMM_DQ[44]	
	DDR2_DIMM_DQ[43]	
	DDR2_DIMM_DQ[42]	
	DDR2_DIMM_DQ[41]	
	DDR2_DIMM_DQ[40]	
	DDR2_DIMM_DQ[39]	
	DDR2_DIMM_DQ[38]	
	DDR2_DIMM_DQ[37]	
	DDR2_DIMM_DQ[36]	
	DDR2_DIMM_DQ[35]	
	DDR2_DIMM_DQ[34]	
	DDR2_DIMM_DQ[33]	
	DDR2_DIMM_DQ[32]	
	DDR2_DIMM_DQ[31]	
	DDR2_DIMM_DQ[30]	
	DDR2_DIMM_DQ[29]	
	DDR2_DIMM_DQ[28]	
	DDR2_DIMM_DQ[27]	
	DDR2_DIMM_DQ[26]	
	DDR2_DIMM_DQ[25]	
	DDR2_DIMM_DQ[24]	
	DDR2_DIMM_DQ[23]	
	DDR2_DIMM_DQ[22]	
	DDR2_DIMM_DQ[21]	
	DDR2_DIMM_DQ[20]	
	DDR2_DIMM_DQ[19]	
	DDR2_DIMM_DQ[18]	
	DDR2_DIMM_DQ[17]	
	DDR2_DIMM_DQ[16]	
	DDR2_DIMM_DQ[15]	
	DDR2_DIMM_DQ[14]	
	DDR2_DIMM_DQ[13]	
	DDR2_DIMM_DQ[12]	
	DDR2_DIMM_DQ[11]	
	DDR2_DIMM_DQ[10]	
	DDR2_DIMM_DQ[9]	
	DDR2_DIMM_DQ[8]	
	DDR2_DIMM_DQ[7]	
	DDR2_DIMM_DQ[6]	
	DDR2_DIMM_DQ[5]	
	DDR2_DIMM_DQ[4]	
	DDR2_DIMM_DQ[3]	
	DDR2_DIMM_DQ[2]	
	DDR2_DIMM_DQ[1]	
	DDR2_DIMM_DQ[0]	
	DDR2_DIMM_SA2	
	DDR2_DIMM_SA1	
	DDR2_DIMM_SA0	
	DDR2_DIMM_SCL	
	DDR2_DIMM_SDA	

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1V8

R228 4K7

R227 4K7

PPC_DDR2_DIMM_SCL

PPC_DDR2_DIMM_SDA

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA1	22-8L,22-9D
DDR2_DIMM_BA[1]	190	DDR_PBA2	22-8L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-8L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	NC	
DDR2_DIMM_CK_N[2]	221	NC	
DDR2_DIMM_CK_P[1]	137	NC	
DDR2_DIMM_CK_N[1]	138	NC	
DDR2_DIMM_CK_P[0]	185	DDR_CLKOUT	
DDR2_DIMM_CK_N[0]	186	DDR_CLKOUT#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-7L,22-8D
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-9D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D
ERR_OUT	55	PPC_DDR2_ERROR	
PAR_IN	68	PAR_IN	

C455 .5PF 50V

R226 4K7

PPC_DDR2_RESET_N

1-2B,1-2M,24-5J

TP4

TP5

VTT VOLTAGE TERMINATION IN COMPACT ARRANGEMENT

DDR_VTT

RP24

RP23

RP22

RP21

RP25

RP26

RP19

CP26

CP28

CP29

CP30

CP32

CP31

CP33

DDR_PA15		
DDR_PA14		
DDR_PA13		
DDR_PA12		
DDR_PA11		
DDR_PA10		
DDR_PA9		
DDR_PA8		
DDR_PA7		
DDR_PA6		
DDR_PA5		
DDR_PA4		
DDR_PA3		
DDR_PA2		
DDR_PA1		
DDR_PA0		
DDR_PBA1	22-8K,22-9D	
DDR_PBA2	22-8K,22-9D	
DDR_PBA0	22-8K,22-9D	
DDR_PCAS#	22-8K,22-9D	
DDR_PRAS#	22-7K,22-9D	
DDR_PCKE	22-6K,22-8D	
DDR_PWE#	22-3K,22-9D	
DDR_PCS0#	22-3K,22-8D	
DDR_PCS1#	22-3K,22-8D	
DDR_PODT0	22-8D	
DDR_PODT1	22-8D	
NC		

J8

	237	VSS_64	
	234	VSS_63	
	231	VSS_62	
	228	VSS_61	
	225	VSS_60	
	222	VSS_59	
	219	VSS_58	
	216	VSS_57	
	213	VSS_56	
	210	VSS_55	
	207	VSS_54	
	204	VSS_53	
	201	VSS_52	
	198	VSS_51	
	169	VSS_50	
	166	VSS_49	
	163	VSS_48	
	160	VSS_47	
	157	VSS_46	
	154	VSS_45	
	151	VSS_44	
	148	VSS_43	
	145	VSS_42	
	142	VSS_41	
	139	VSS_40	
	136	VSS_39	
	133	VSS_38	
	130	VSS_37	
	127	VSS_36	
	124	VSS_35	
	121	VSS_34	
	118	VSS_33	
	115	VSS_32	
	112	VSS_31	
	109	VSS_30	
	106	VSS_29	
	103	VSS_28	
	100	VSS_27	
	97	VSS_26	
	94	VSS_25	
	91	VSS_24	
	88	VSS_23	
	85	VSS_22	
	82	VSS_21	
	79	VSS_20	
	66	VSS_19	
	65	VSS_18	
	50	VSS_17	
	47	VSS_16	
	44	VSS_15	
	41	VSS_14	
	38	VSS_13	
	35	VSS_12	
	32	VSS_11	
	29	VSS_10	
	26	VSS_9	
	23	VSS_8	
	20	VSS_7	
	17	VSS_6	
	14	VSS_5	
	11	VSS_4	
	8	VSS_3	
	5	VSS_2	
	2	VSS_1	
	194	VDDQ_11	
	191	VDDQ_10	
	181	VDDQ_9	
	175	VDDQ_8	
	170	VDDQ_7	
	78	VDDQ_6	
	75	VDDQ_5	
	72	VDDQ_4	
	62	VDDQ_3	
	56	VDDQ_2	
	51	VDDQ_1	

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DDR_VREF_0V9

VREF 1

1V8

VDDSPD 238

1V8

VDD_11 197

VDD_10 189

VDD_9 187

VDD_8 184

VDD_7 178

VDD_6 172

VDD_5 69

VDD_4 67

VDD_3 64

VDD_2 59

VDD_1 53

1V8

VDDQ_11 194

VDDQ_10 191

VDDQ_9 181

VDDQ_8 175

VDDQ_7 170

VDDQ_6 78

VDDQ_5 75

VDDQ_4 72

VDDQ_3 62

VDDQ_2 56

VDDQ_1 51

GND

DDR_VREF_0V9

1V8

C432 100NF 10V

C433 10NF 25V

C454 100NF 10V

C434 10NF 25V

C430 100NF 10V

C443 10NF 25V

C431 100NF 10V

C444 10NF 25V

C436 100NF 10V

C445 10NF 25V

C435 100NF 10V

C446 10NF 25V

C438 100NF 10V

C451 10NF 25V

C437 100NF 10V

C452 10NF 25V

C439 100NF 10V

C449 10NF 25V

C440 100NF 10V

C450 10NF 25V

C441 100NF 10V

C448 10NF 25V

C442 100NF 10V

C447 10NF 25V

PLACE NEAREST DDR2 MODULE PINS

ROACH/iBOB2

ROACH_PPC_DDR2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

10-22-2007_16:25

PATH PATH

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 22 OF 25


PWR_GOOD monitors the +1.0v, 1V5, 1V8, 2V5, and 3V3 supplies
RESET_PB_POR#
Critical Placement and Route Clock Rules:
Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_SYS_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz
SEL_SYSCLK
CLK_UART_11.0592MHZ
CLK_CPLD_33MHZ
CLK_TMRCLK
SYSERR
PPC_THERMONA
PPC_THERMONB
IRQ0-9 have programmable polarity per section 10.5.7 (UIC0_PR) 440ep user manual
GETH0_INT#
MONITOR_INT
V5_INT#
STTM_ALERT
GPIO44
SX95T_TDI
SX95T_TCK
SX95T_TMS
SX95T_TDO
NO POP R01 - R05
PPC440EPX-NTA533T
Critical Placement and Route Clock Rules:
Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible
CLK_SEL_M66EN
CLK_GETH0_25MHZ
CLK_USB2.0_48MHZ
CLK_CPLD_50MHZ
TRACE & JTAG CONNECTORS
R26 is for current limiting and should be <100 Ohms.
Critical placement and routing of the Trace connector and nets. Up to CPU frequency/4
TRACE PORT
CPU_TRST#
DEBUG_TRST#

ROACH/iBOB2	ROACH_PPC_TST_CLK_IO
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-22-2007_16:25	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 23 OF 25

Memory Bus

PA09[27:21]
1-2G,1-4L,25-10B

PADATA[0:7]
1-2M,1-4L

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roach_cpld_XC2C256_7VQ100C_pcb

PAD027	4	PAD4
PAD028	7	PAD8
PAD029	9	PAD10
PAD030	10	PAD12
PAD031	11	PAD15
PDATA0	12	PAD16
PDATA1	13	PAD17
PDATA2	14	PAD18
PDATA3	15	PAD19
PDATA4	16	PAD20
PDATA5	17	PAD21
PDATA6	18	PAD23
PDATA7	19	PAD28
NC	20	PAD29
NC	21	PAD30
NC	22	PAD31
NC	23	PAD32
NC	24	PAD33
NC	25	PAD34
NC	26	PAD35
	28	PAD44
SELECTMAP_CS 1-2G,1-5L,25-7B	30	PAD48
PCS_2 1-1G,1-4L,25-7B	31	PAD49
PDS0 1-1G,1-5L,25-5G,25-7B,25-7M,25-10B	32	PAD50
PR_WE 1-1G,1-4L,25-5G,26-6M,d5-7B,25-9B	33	PAD52
PWRE_B# 1-2G,1-4L,25-6M,25-7B,25-9B	34	PAD54
RESET_PDN# 1-2G,1-3L,1-5G,23-9J,25-5G	35	PAD55
RESET_PB_PDN# 1-2M,1-3H,23-8E	38	PAD59
PPC_RESET 1-2G,1-9E,2-2R	40	PAD64
DEBUG_TRST# 1-1G,1-3L,23-1F	41	PAD65
CPU_TRST# 1-2M,1-3M,23-2F	42	PAD66
CLK_CPLD_33MHZ 1-1G,1-2L,23-6G	43	PAD67
CLK_CPLD_33MHZ 1-1G,1-3L,23-4G	44	PAD68
CLK_PXICLK 1-1G,1-4L,25-6F	45	PAD69
CLK_TMSCLK 1-1M,1-3H,23-6H	46	PAD70
CLK_SEL_PXIEN# 1-1M,1-3H,23-5D	48	PAD73
SEL_SYSCLK 1-1M,1-3N,23-7G	49	PAD74
SYSERR 1-1G,1-3L,23-8H	50	PAD75
FRY_BSY 1-1G,1-4L,25-7J	51	PAD76
PAPSC 1-1M,1-4G,25-8J	52	PAD77
EE1_WP 1-2M,1-5L,25-1A	53	PAD81
EE2_BOOT_WP 1-2M,1-4G,25-5A	54	PAD82
ETTM_ASC 1-2M,1-5G,25-1B	56	PAD86
SYS_CONFIG0	57	PAD87
SYS_CONFIG1	58	PAD88
SYS_CONFIG2	59	PAD89
SYS_CONFIG3	60	PAD90
SYS_CONFIG4	61	PAD95
SYS_CONFIG5	64	PAD100
SYS_CONFIG6	66	PAD102
GETH0_RST# 1-2M,1-4B,20-4E	68	PAD105
NC	69	PAD107
NC	70	PAD108
RESET_CPLD# 1-1M,1-4G,25-3J	71	PAD109
NC	74	PAD112
PER_CCLK_EN#	75	PAD113

SYS_CONFIG[0:7]
1-2G,1-9E,2-2R

RESETS

CPU_TRST# = '1' when JTAG_TRST# = '1' and RESET_PDN# = '1' else '0';
see errata sheet

CLOCKS

STATUS / MISC

FLASH

I2C

ETHERNET

PAD217	142	USER_DIP0
PAD214	140	USER_DIP1
PAD213	139	USER_DIP2
PAD212	138	USER_DIP3
PAD211	137	CFG_DIP0
PAD208	136	CFG_DIP1
PAD207	135	CFG_DIP2
PAD206	134	M66EN
PAD204	133	
PAD199	132	
PAD197	131	
PAD196	130	USER_LED0
PAD195	129	USER_LED1
PAD194	128	SYSERR#
PAD192	126	RESET_BUFPOR#
PAD191	125	SX95T_CCLK_0
PAD190	124	
PAD187	121	SX95T_D_IN_0
PAD186	120	SX95T_D_OUT_BUSY_0
PAD178	119	SX95T_DONE_0
PAD177	118	SX95T_INIT_B_0
PAD176	117	SX95T_PROGRAM_B_0
PAD175	116	SX95T_ROWB_B_0
PAD173	115	CMD/DI
PAD171	114	CLK/SCLK
PAD169	113	
PAD168	112	
PAD167	111	
PAD166	110	
PAD163	107	
PAD162	106	
PAD161	105	
PAD160	104	
PAD158	103	
PAD156	102	
PAD154	101	NC
PAD152	100	NC
PAD146	98	NC
PAD145	97	NC
PAD144	96	NC
PAD143	95	NC
PAD142	94	NC
PAD138	92	NC
PAD137	91	NC
PAD134	88	NC
PAD133	87	
PAD132	86	
PAD131	85	
PAD125	83	
PAD121	82	NC
PAD120	81	NC
PAD119	80	NC
PAD118	79	NC
PAD117	78	
PAD115	77	
PAD114	76	

XC2C256_7VQ100C

SW2
4POLE
User DIP-Swith

SX95T_M0_0
1-1G,1-3F,1-7G,16-3B,21-4D
SX95T_M1_0
1-1G,1-3F,1-7G,16-3B,21-4D
SX95T_M2_0
1-1G,1-3F,1-7G,16-3B,21-4D

QDR2_BY0_1_SYS_RST_N
1-1M,1-8L,14-5J
QDR2_BY2_3_SYS_RST_N
1-2M,1-7L,15-5J
PPC_DDR2_RESET_N
1-2G,1-2M,22-2B
EXT_RESET#
1-2G,1-4L,25-6F

SysErr will be used to drive Status LED (active H)

PWR_GOOD
1-2G,1-3H,23-10G

Boot Configuration

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

SW3
4POLE
Configuration DIP-Swith

1-1G,1-5G,25-3B

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

BOOT_CFG0
1-1M,1-4G,25-1J
BOOT_CFG1
1-1M,1-4G,25-1J
BOOT_CFG2
1-1M,1-4G,25-1J

SD/MMC/MMCPLUS CONNECTOR

J17
GMC05004SEU

CMD/DI	10	DAT0/DO
CLK/SCLK	6	DAT1
VDD	7	DAT2
VSS1	8	DAT3
VSS2	4	DAT4
SD_CD_COM	14	DAT5
SD_WP_COM	15	DAT6
		DAT7
MNT1	16	NC
MNT2	17	NC

DAT0/DO	2	DAT0/DO
DAT1	1	DAT1
DAT2	13	DAT2
DAT3	12	DAT3
DAT4	11	DAT4
DAT5	9	DAT5
DAT6	5	DAT6
DAT7	3	DAT7

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roach_cpld_XC2C256_7VQ100C_configpins

NC	2	PAD1
NC	3	PAD3
NC	5	PAD5
NC	6	PAD7
NC	39	PAD62
	63	TDI
	65	TMS
	67	TCK
	122	TDO
NC	143	PAD218

XC2C256_7VQ100C

Xilinx
Programing Cable

JTAG

J22

PLACE NEAR CPLD JTAG CONNECTOR

ENABLE PER_CLK CONNECTION
TO CONFIGURATION I/F
MUST CO-ORDINATE WITH
SX95T_CCLK_0 AND MODE
TO AVOID CLASH

SN74AHC1G125DCKT

PLACE NEAR CPLD POWER PINS

U54

roach_cpld_XC2C256_7VQ100C_powerpins

XC2C256_7VQ100C

VCC	1	GND_3
VAUX	8	GND_4
VCCIO_3	27	GND_5
VCC_1	37	GND_6
VCCIO_4	55	GND_7
VCCIO_5	73	GND_8
VCC_2	84	GND_9
VCCIO_6	93	GND_10
VCCIO	109	GND
VCCIO_1	127	GND_1
VCCIO_2	141	GND_2

C473	100NF 10V	
C474	100NF 10V	
C475	100NF 10V	
C476	100NF 10V	
C477	100NF 10V	
C478	100NF 10V	
C479	100NF 10V	
C480	100NF 10V	
C481	100NF 10V	
C482	100NF 10V	
C483	100NF 10V	

ROACH/iBOB2	ROACH_PPC_CPLD
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A; DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
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ROACH/iBOB2	**ROACH_PPC_NVM_SERIAL**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-22-2007_16:25 PATH PATH	DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET 25 OF 25