VIRTEX5

POWER SUPPLY AND MONITORING

ROACH_MONITOR

PPC_RESET
SYS_CONFIG[0:7]
TDZ
ATRTN1
MONITOR_INT
I2C0_33_DATA
PS_ON#
ATRTN0
TDO
FAN1_CONTROL
LOAD_RES_OFF
2V5_TRACK
2V5_INHIBIT
FAN2_CONTROL
MGT_AVTTX_EN
MGT_AVCCPLL_EN
MGT_AVCC_EN
1V0_INHIBIT
1V5_INHIBIT
1V0_INHIBIT

1-4B,1-6L,2-2P,22-2F,25-5A I2C0_SCLK
1-9E,2-3N,3-10A FAN2_SENSE
1-9E,2-3M,3-11A FAN1_SENSE
1-9E,2-3H,3-9A FAN3_SENSE
1-9E,2-3A,3-6C 3V3_ATX
1-9E,2-2B,3-2M 2V5
1-9E,2-2B,3-2M 1V8
1-9E,2-2B,3-5R 1V5
1V0
1-9E,2-1B,3-10E 5V_ATX
1-9E,2-4A,3-6C MGT_AVCC_PG
1-10Q,2-9B,10-7P MGT_AVTTX_PG
1-9Q,2-8B,10-4G MGT_AVCCPLL_PG
1-9E,2-8B,3-7C PWR_OK
1-9E,2-8B,3-7C 12V_ATX
1-9E,2-6B,3-6C
2

ROACH_PSU

1-10E,2-6B,3-4B LOAD_RES_OFF
1-10E,2-3N,3-10A FAN1_CONTROL
1-10E,2-8B,3-7G PS_ON#
1-10E,2-3J,3-10A FAN2_CONTROL
1-10E,2-3J,3-9A FAN3_CONTROL
1V0_INHIBIT
1-9E,2-8B,3-9J 1V5_INHIBIT
1-9E,2-1B,3-4J 1V8_INHIBIT
2V5_TRACK
1-10E,2-8B,3-3B 2V5_INHIBIT
1-10E,2-1B,3-1B
3

12V_ATX
3V3_ATX
5V_ATX
PWR_OK
FAN1_SENSE
FAN2_SENSE
FAN3_SENSE
I1V0
I1V5
I1V8
I2V5

1-9B,2-6B,3-6C
1-10B,2-3A,3-6C
1-10B,2-4A,3-6C
1-9B,2-8B,3-7C
1-10B,2-3H,3-11A
1-10B,2-3H,3-10A
1-10B,2-3H,3-9A
1-10B,2-1B,3-10R
1-10B,2-2B,3-5R
1-10B,2-2B,3-2R
1-10B,2-2B,3-2H

VIRTEX5 CLOCKS

ROACH_V5_CLK
SX95T_DXN
SX95T_DXP
ATRTN0
TDO
7

ZDOK/ADC INTERFACE

ROACH_ADC_0
5
ROACH_ADC_1
6

V5 DDR2 MEMORY

ROACH_DDR2_DIMM
11

V5 DIFFERENTIAL GPIO

ROACH_DIFF_GPIO
12

V5 SE GPIO & MISCELLANEOUS

ROACH_GPIO_MISC
13

GIGABIT TRANSCEIVERS

ROACH_TRANSCEIVERS0_1
MGT_REFCLK_Q1_1_P
MGT_REFCLK_Q1_1_N
MGT_REFCLK_Q2_0_P
MGT_REFCLK_Q2_0_N
ROACH_TRANSCEIVERS2_3
MGT_REFCLK_Q2_0_P
MGT_REFCLK_Q2_0_N
MGT_REFCLK_Q1_1_P
MGT_REFCLK_Q1_1_N
8
9

ROACH_TRANSCEIVERS_PSU

1-10E,2-8M,10-8K MGT_AVCC_EN
1-10E,2-8M,10-8B MGT_AVCCPLL_EN
1-10E,2-8M,10-8B MGT_AVTTX_EN
MGT_AVCC_PG
MGT_AVTTX_PG
MGT_AVCCPLL_PG
MGT_AVCC_PG 1-10B,2-8B,10-7P
MGT_AVTTX_PG 1-10B,2-8B,10-4G
MGT_AVCCPLL_PG 1-10B,2-8B,10-7G
10

QDRII+ MEMORY

ROACH_QDR2P_BY0_1
QDR2_TDI
QDR2_TCK
QDR2_TMS
QDR2_BY0_1_TDO
QDR2_BY0_1_TDO
14

ROACH_QDR2P_BY2_3
QDR2_BY0_1_TDO
QDR2_TMS
QDR2_TCK
QDR2_BY2_3_TDO
QDR2_BY2_3_TDO
15

R161 10K
R162 10K
R163 10K
QDR2_BY2_3_TDO
QDR2_TDI
QDR2_TCK
QDR2_TMS
P6 2x5 .1IN M SMT
R164 33R
C62 100NF 10V

V5 POWER

ROACH_5V_POWER
4

VIRTEX5 CONFIGURATION

ROACH_CONFIG

1-2M,1-6G,16-4B,24-7C,25-7B,25-10B SX95T_D_IN_0
1-3G,16-2L,24-5M SX95T_TCK
1-3G,16-2L,24-5M SX95T_TMS
1-3M,16-2L,24-5M CPLD_TDO
1-2M,16-3B,24-9C SX95T_RDWR_B_0
1-2M,1-4F,16-3B,21-4D,24-10C SX95T_PROGRAM_B_0
1-2M,16-4B,24-6C SX95T_CS_B_0
16

SX95T_M2_0 SX95T_M2_0 1-2G,1-4F,16-3B,21-4D,24-7F
SX95T_M1_0 SX95T_M1_0 1-2G,1-4F,16-3B,21-4D,24-7F
SX95T_M0_0 SX95T_M0_0 1-2G,1-4F,16-3B,23-4D,24-7F
SX95T_DONE_0 SX95T_DONE_0 1-2M,1-6F,21-5D
SX95T_CCLK_0 SX95T_CCLK_0 1-3M,24-4F,24-7C
SX95T_D_OUT_BUSY_0 SX95T_D_OUT_BUSY_0 1-2G,1-4F,16-4B,21-5D,24-7C
SX95T_INIT_B_0 SX95T_INIT_B_0 1-2M,1-6F,21-4D,24-9F
SX95T_TDO SX95T_TDO 1-3G,16-2L,24-6M

PPC

ROACH_PPC_POWER_1
17
ROACH_PPC_POWER_2
18
ROACH_PPC_PCI
19

ROACH_PPC_ETH1

1-3M,20-4E,24-10F GETH0_RST#
1-4L,20-4E,23-5G CLK_GETH0_25MHZ
GETH0_RST#
CLK_GETH0_25MHZ
20

GMCMDIO
GMCMDCLK
GETH0_INT#
GMCMDIO 20-3C,20-4D
GMCMDCLK 20-3C,20-4D
GETH0_INT# 1-4M,20-4E,23-7N

ROACH_PPC_USB

CONTAINS GPIO TO CONFIG INTERFACE

SX95T_D_OUT_BUSY_0 SX95T_D_OUT_BUSY_0 1-2G,1-8G,16-4B,21-5D,24-7C
SX95T_DONE_0 SX95T_DONE_0 1-2M,1-8G,21-5D
SX95T_INIT_B_0 SX95T_INIT_B_0 1-2M,1-8G,21-4D,24-9F
SX95T_M0_0 SX95T_M0_0 1-2G,1-8G,16-3B,21-4D,24-7F
SX95T_M1_0 SX95T_M1_0 1-2G,1-8G,16-3B,21-4D,24-7F
SX95T_M2_0 SX95T_M2_0 1-2G,1-8G,16-3B,21-4D,24-7F
SX95T_PROGRAM_B_0 SX95T_PROGRAM_B_0 1-2M,1-8G,16-3B,21-4D,24-10C

1-4L,21-2C,23-4G CLK_USB2_48MHZ
CLK_USB2_48MHZ
21

ROACH_PPC_DDR2

1-4L,1-10B,2-2P,22-2F,25-5A I2C0_SCLK
1-6L,1-10E I2C0_SDATA
1-3M,22-3K,24-10F PPC_DDR2_RESET_N
I2C0_SCLK
I2C0_SDATA
PPC_DDR2_RESET_N
22

PLACE OVER PLANE SPLIT AT BOTTOM OF PCB NEAR ADC CONNECTORS

2V5 C296 C297 C298 C299 100NF 10V
5VAUX
5V C351 C396 C397 C398 100NF 10V
1V0
3V3_ATX C417 C471 C472 C620 100NF 10V
3V3
1V8 C391 C397 C395 C394 100NF 10V
12V
1V5 C497 C498 C411 C414 100NF 10V
GND

ROACH_PPC_NVM_SERIAL

1-2M,1-8D,16-4B,24-7C,25-7B,25-10B SX95T_D_IN_0
1-4L,23-7G,25-3B CLK_UART_11_0592MHZ
1-3M,24-7C,25-4A EE1_WP
1-3M,24-7C,25-1B STTM_AS
1-3G,1-4L,23-9J,24-5M,25-5G RESET_POR#
1-2M,24-7C,25-8J FWP#
1-3M,24-7C,25-5A EE2_BOOT_WP
1-2M,24-11M,25-1J BOOT_CFG0
1-2M,24-11M,25-1J BOOT_CFG1
1-2M,24-10M,25-1J BOOT_CFG2
1-2M,24-5C,25-1J RESET_CPLD#
1-2M,24-6C,25-7B,25-9Q,25-9B PREADY
SX95T_D_IN_0
CLK_UART_11_0592MHZ
EE1_WP
STTM_AS
RESET_POR#
FWP#
EE2_BOOT_WP
BOOT_CFG0
BOOT_CFG1
BOOT_CFG2
RESET_CPLD#
PREADY
25

V5_INT# V5_INT# 1-4M,23-7N,25-8Q
SELECTMAP_CS SELECTMAP_CS 1-3G,24-6C,25-7B
I2C0_SCLK I2C0_SCLK 1-4B,1-10B,2-2P,22-2F,25-5A
I2C0_SDATA I2C0_SDATA 1-3B,1-10E
STTM_ALERT STTM_ALERT 1-4M,23-6M,25-2B
POE# POE# 1-2G,24-8C,25-5G,25-7B,25-7M,25-10B
FRY_BY# FRY_BY# 1-3G,24-7C,25-7J
CLK_PERCLK CLK_PERCLK 1-2G,24-4C,24-8B,25-6F
PWBE_0# PWBE_0# 1-3G,24-9C,25-6M,25-7B,25-9B
PR_W# PR_W# 1-2G,24-10C,25-5G,25-6M,25-7B,25-9B
PCS_2 PCS_2 1-2G,24-10C,25-7B
PDATA[0:31] PDATA[0:31] 1-3M
PADD[2:31] PADD[2:31] 1-3G,24-9B
EXT_RESET# EXT_RESET# 1-3G,24-10C,25-6F

ROACH_PPC_TST_CLK_IO

1-3M,23-6N,24-6C CPLD_INT
1-5E,20-4E,23-7N GETH0_INT#
1-10E,2-2P,23-7M MONITOR_INT
1-6L,23-7N,25-9Q V5_INT#
1-6L,23-6M,25-2B STTM_ALERT
1-3M,23-8E,24-7F RESET_PB_POR#
1-3G,23-5G,24-8R PWR_GOOD
1-3M,23-2P,24-9C CPU_TRST#
1-2M,23-5Q,24-10F CLK_SEL_M66EN
1-2M,23-7G,24-10F SEL_SYSCLK
1-2M,23-6M,24-10C CLK_TMRCLK
CPLD_INT
GETH0_INT#
MONITOR_INT
V5_INT#
STTM_ALERT
RESET_PB_POR#
PWR_GOOD
CPU_TRST#
CLK_SEL_M66EN
SEL_SYSCLK
CLK_TMRCLK
23

PPC_THERMONA PPC_THERMONA 1-10E,2-6L,23-6H
PPC_THERMONB PPC_THERMONB 1-10E,2-4L,23-6H
GPIO44 GPIO44 23-6N
RESET_POR# RESET_POR# 1-3G,1-6G,23-9J,24-5M,25-5G
DEBUG_TRST# DEBUG_TRST# 1-2G,23-1F,24-9C
CLK_GETH0_25MHZ CLK_GETH0_25MHZ 1-5B,20-4E,23-5G
CLK_USB2_48MHZ CLK_USB2_48MHZ 1-4B,21-2C,23-4G
CLK_CPLD_50MHZ CLK_CPLD_50MHZ 1-2G,23-4G,24-7C
SYSERR SYSERR 1-2G,23-6M,24-10C
CLK_UART_11_0592MHZ CLK_UART_11_0592MHZ 1-6G,23-7G,25-3B
CLK_CPLD_33MHZ CLK_CPLD_33MHZ 1-2G,23-8G,24-8C

ROACH_PPC_CPLD

SX95T_TMS SX95T_TMS 1-8D,16-2L,24-5M
SX95T_TCK SX95T_TCK 1-8D,16-2L,24-5M
SX95T_TDO SX95T_TDO 1-8G,16-2L,24-6M
1-10E,2-2P,24-6B SYS_CONFIG[0:7]
SYS_CONFIG[0:7]
1-10E,2-3P,24-6C PPC_RESET
1-4M,23-10G,24-8R PWR_GOOD
1-5L,24-10C,25-6F EXT_RESET#
1-4L,1-6G,23-9J,24-5M,25-5G RESET_POR#
1-5L,24-9C,25-6M,25-7B,25-9B PWBE_0#
1-5L,24-9B PADD[27:31]
1-6L,24-6C,25-7B SELECTMAP_CS
1-4L,24-7C,25-7J FRY_BY#
1-4L,23-6N,24-10C SYSERR
1-4L,23-6G,24-8C CLK_CPLD_33MHZ
1-4L,23-1F,24-9C DEBUG_TRST#
1-5L,24-4C,24-8B,25-6F CLK_PERCLK
1-4L,23-4G,24-7C CLK_CPLD_50MHZ
PR_W#
POE#
PCS_2
1-4F,1-8G,16-4B,21-5D,24-7C SX95T_D_OUT_BUSY_0
24-5M M66EN
1-4F,1-8G,16-3B,21-4D,24-7F SX95T_M0_0
1-4F,1-8G,16-3B,21-4D,24-7F SX95T_M1_0
1-4F,1-8G,16-3B,21-4D,24-7F SX95T_M2_0
SX95T_M0_0
SX95T_M1_0
SX95T_M2_0
24

CPLD_TDO CPLD_TDO 1-8D,16-2L,24-5M
GETH0_RST# GETH0_RST# 1-5B,20-4E,24-10F
PPC_DDR2_RESET_N PPC_DDR2_RESET_N 1-3B,22-3K,24-10F
CPLD_INT CPLD_INT 1-4M,23-6N,24-6C
PDATA[0:7] PDATA[0:7] 1-5L
RESET_PB_POR# RESET_PB_POR# 1-4M,23-8E,24-7F
SX95T_CCLK_0 SX95T_CCLK_0 1-8G,24-4F,24-7C
STTM_AS STTM_AS 1-6G,24-7C,25-1B
EE2_BOOT_WP EE2_BOOT_WP 1-5G,24-7C,25-5A
EE1_WP EE1_WP 1-6G,24-7C,25-4A
CPU_TRST# CPU_TRST# 1-4M,23-2F,24-9C
SEL_SYSCLK SEL_SYSCLK 1-4M,23-7G,24-10F
CLK_SEL_M66EN CLK_SEL_M66EN 1-4M,23-5Q,24-10F
CLK_TMRCLK CLK_TMRCLK 1-4M,23-6G,24-10C
SX95T_RDWR_B_0 SX95T_RDWR_B_0 1-8D,16-3B,24-8C
FWP# FWP# 1-6G,24-7C,25-8J
RESET_CPLD# RESET_CPLD# 1-5G,24-5C,25-1J
PREADY PREADY 1-5G,24-6C,25-7B,25-8Q,25-9B
SX95T_INIT_B_0 SX95T_INIT_B_0 1-4F,1-8G,21-4D,24-9F
SX95T_DONE_0 SX95T_DONE_0 1-4F,1-8G,21-5D
SX95T_PROGRAM_B_0 SX95T_PROGRAM_B_0 1-4F,1-8G,16-3B,21-4D,24-10C
SX95T_D_IN_0 SX95T_D_IN_0 1-8G,1-8D,16-4B,24-7C,25-7B,25-10B
SX95T_CS_B_0 SX95T_CS_B_0 1-8D,16-4B,24-6C
BOOT_CFG0 BOOT_CFG0 1-5G,24-11M,25-1J
BOOT_CFG1 BOOT_CFG1 1-5G,24-11M,25-1J
BOOT_CFG2 BOOT_CFG2 1-5G,24-10M,25-1J
24

MECHANICAL

GND
M1 M2 M3 M4 M5 M6 M7 M8 M9 SJO4200ML
M10
M11

BOARD FIDUCIALS

NC FU1 FU2 FU3 PLACE TOP
NC FU4 FU5 FU6 PLACE BOTTOM
NC FU9 FU8 FU7 PLACE TOP ON BORDER TAB
NC FU12 FU11 FU10 PLACE BOTTOM ON BORDER TAB

LOGO'S

PLACEHOLDER FOR PCB MEERKAT LOGO

PLACEHOLDER FOR PCB CASPER LOGO

PLACEHOLDER FOR PCB ROACH LOGO

PLACEHOLDER FOR PCB NRAO LOGO

BOARD SERIAL NUMBER

CONTRIBUTORS

ETIENNE BAUERMEISTER
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FRANCOIS KAPP
ALAN LANGMAN
GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

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PATH PATH

ROACH_TOP

DOC NO ROACH
REVISION 1.0.2
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 1 OF 25

roach_AFS600_pcb

roach_AFS600_powerpins

roach_AFS600_configpins

PLACE AT ACTEL 3V3 POWER PINS

PLACE AT ACTEL 1V5 POWER PINS

TIE TO GROUND IF PLL'S ARE NOT USED

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

PB POWER SWITCH

KEY - REMOVE PIN

MONITOR RESET

15-91-2140

XPORT - PLACE IN REAR I/O REGION
XP1001001-03R

TEMPERATURE DIODE HEADER
J31

15-91-2200

SPARE ANALOG VOLTAGE INPUT #0
SPARE ANALOG VOLTAGE INPUT #1
SPARE GATE DRIVE OUTPUT #0
SPARE GATE DRIVE OUTPUT #1

15-91-2080

N2520-6VDC-RB-WE

ACTEL JTAG CONNECTOR

REFERENCE RESISTOR/ADC VALUES

VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)	FOR 8 BIT ADC USING 2.56V REFERENCE: ADC COUNT AT MAX POWER	CURRENT/BIT (A)
12V	0R01	3.36	0.11	33	0.1
5V	0R0047	6.78	0.22	31	0.21
3V3	0R01	3.47	0.12	34	0.1
2V5	0R01	3.56	0.13	35	0.1
1V8	0R0022	12.91	0.37	28	0.45
1V5	0R0047	6.77	0.22	31	0.21
1V0	0R001	26.79	0.72	26	1.0

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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PATH PATH

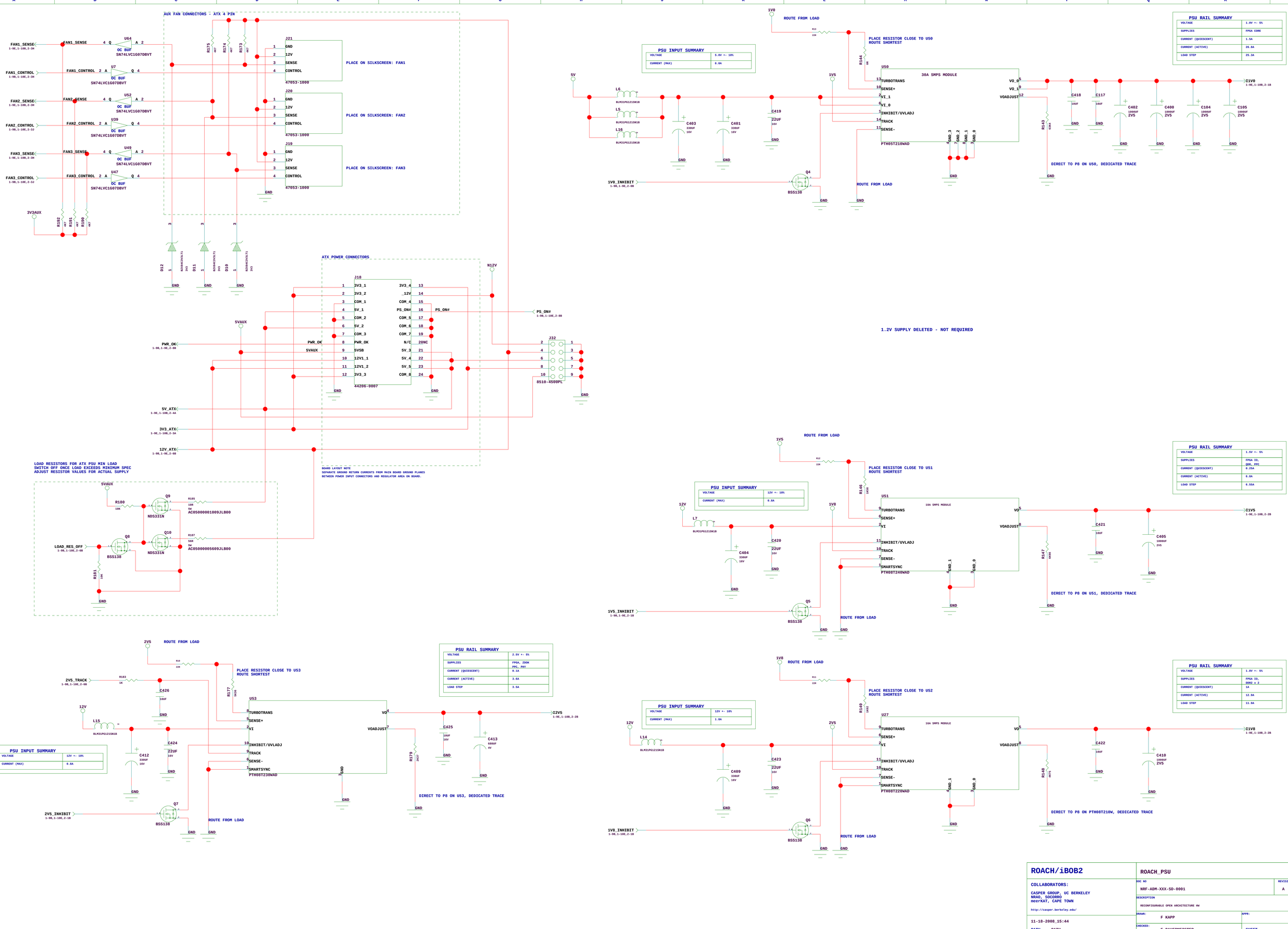
ROACH_MONITOR

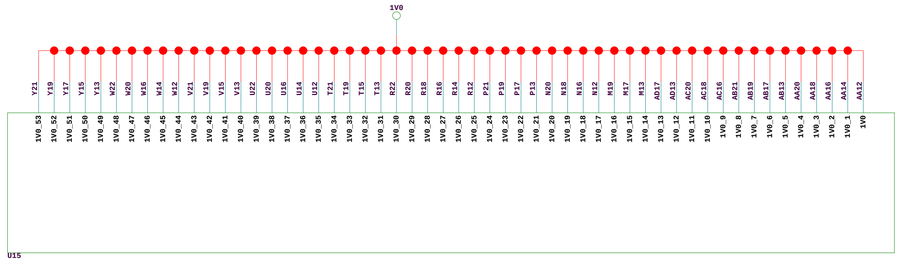
DOC NO: NRF-ADM-XXX-SD-0001
REVISION: A

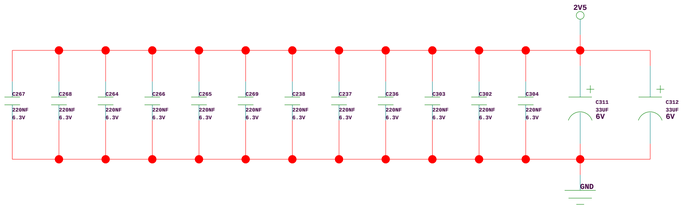
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

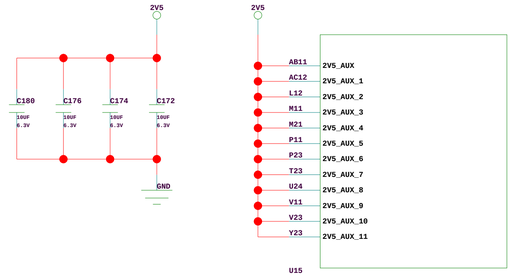
DRAWN: F KAPP
APPR:

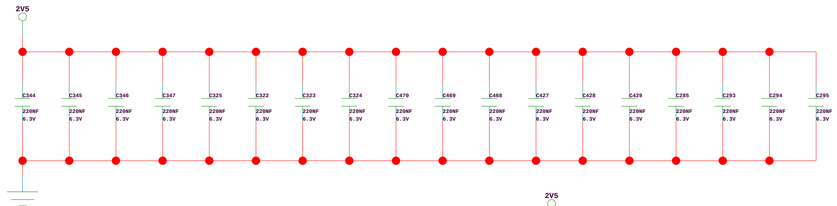
CHECKED: E BAUERMEISTER
SHEET 2 OF 25

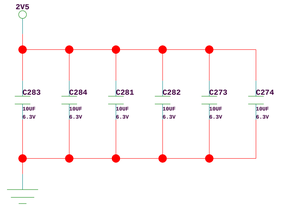

AUX FAN CONNECTORS - ATX 4 PIN
FAN1_SENSE
FAN1_CONTROL
FAN2_SENSE
FAN2_CONTROL
FAN3_SENSE
FAN3_CONTROL
U64
U7
U52
U39
U49
U47
OC BUF
SN74LVC1G07DBVT
R175
R174
R173
R192
R191
R190
3V3AUX
J21
J20
J19
47053-1000
GND
PLACE ON SILKSCREEN: FAN1
PLACE ON SILKSCREEN: FAN2
PLACE ON SILKSCREEN: FAN3
D12
D11
D10
BZX84C3V3LT1
ATX POWER CONNECTORS
J18
44206-0007
N12V
PS_ON#
5VAUX
PWR_OK
5V_ATX
3V3_ATX
12V_ATX
J32
8510-4500PL
LOAD RESISTORS FOR ATX PSU MIN LOAD
SWITCH OFF ONCE LOAD EXCEEDS MINIMUM SPEC
ADJUST RESISTOR VALUES FOR ACTUAL SUPPLY
Q9
Q10
Q8
NDS331N
BSS138
AC05000001009JLB00
AC05000005609JLB00
LOAD_RES_OFF
R180
R185
R187
R181
BOARD LAYOUT NOTE
SEPARATE GROUND RETURN CURRENTS FROM MAIN BOARD GROUND PLANES
BETWEEN POWER INPUT CONNECTORS AND REGULATOR AREA ON BOARD.
1V0
ROUTE FROM LOAD
PLACE RESISTOR CLOSE TO U50
ROUTE SHORTEST
R144
U50
30A SMPS MODULE
PTH05T210WAD
PSU INPUT SUMMARY
VOLTAGE 5.0V +- 10%
CURRENT (MAX) 6.0A
5V
L6
L5
L16
BLM31PG121SN1B
C403
330UF
16V
C401
C419
22UF
C418
10UF
C117
C402
1000UF
2V5
C400
C104
C105
I1V0
1-9E,1-10B,2-1B
VO_0
VO_1
VOADJUST
R143
604K
DIRECT TO P8 ON U50, DEDICATED TRACE
1V0_INHIBIT
Q4
1V5
1V5_INHIBIT
Q5
R146
R147
U51
16A SMPS MODULE
PTH08T240WAD
C404
C420
C421
C405
I1V5
2V5_TRACK
2V5_INHIBIT
Q7
R183
1K
C426
C424
C412
L15
U53
PTH08T230WAD
R177
R176
R179
2K87
C425
C413
I2V5
DIRECT TO P8 ON U53, DEDICATED TRACE
1V8
R149
R148
U27
PTH08T220WAD
C409
C423
C422
C410
I1V8
DIRECT TO P8 ON PTH08T210W, DEDICATED TRACE
1V8_INHIBIT
Q6
1.2V SUPPLY DELETED - NOT REQUIRED
PSU RAIL SUMMARY
VOLTAGE 1.0V +- 5%
SUPPLIES FPGA CORE
CURRENT (QUIESCENT) 1.5A
CURRENT (ACTIVE) 26.8A
LOAD STEP 25.3A
PSU RAIL SUMMARY
VOLTAGE 1.5V +- 5%
SUPPLIES FPGA IO, QDR, PPC
CURRENT (QUIESCENT) 0.25A
CURRENT (ACTIVE) 6.8A
LOAD STEP 6.55A
PSU RAIL SUMMARY
VOLTAGE 2.5V +- 5%
SUPPLIES FPGA, ZDOK PPC, PHY
CURRENT (QUIESCENT) 0.1A
CURRENT (ACTIVE) 3.6A
LOAD STEP 3.5A
PSU RAIL SUMMARY
VOLTAGE 1.8V +- 5%
SUPPLIES FPGA IO, DDR2 x 2
CURRENT (QUIESCENT) 1A
CURRENT (ACTIVE) 12.9A
LOAD STEP 11.9A
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
11-18-2008_15:44
PATH PATH
ROACH_PSU
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 3 OF 25

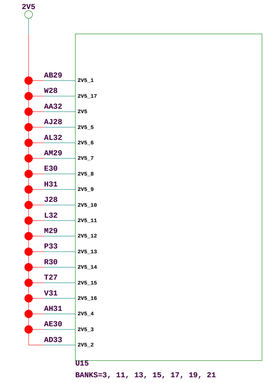


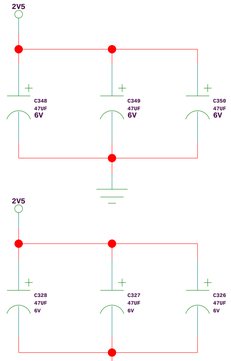


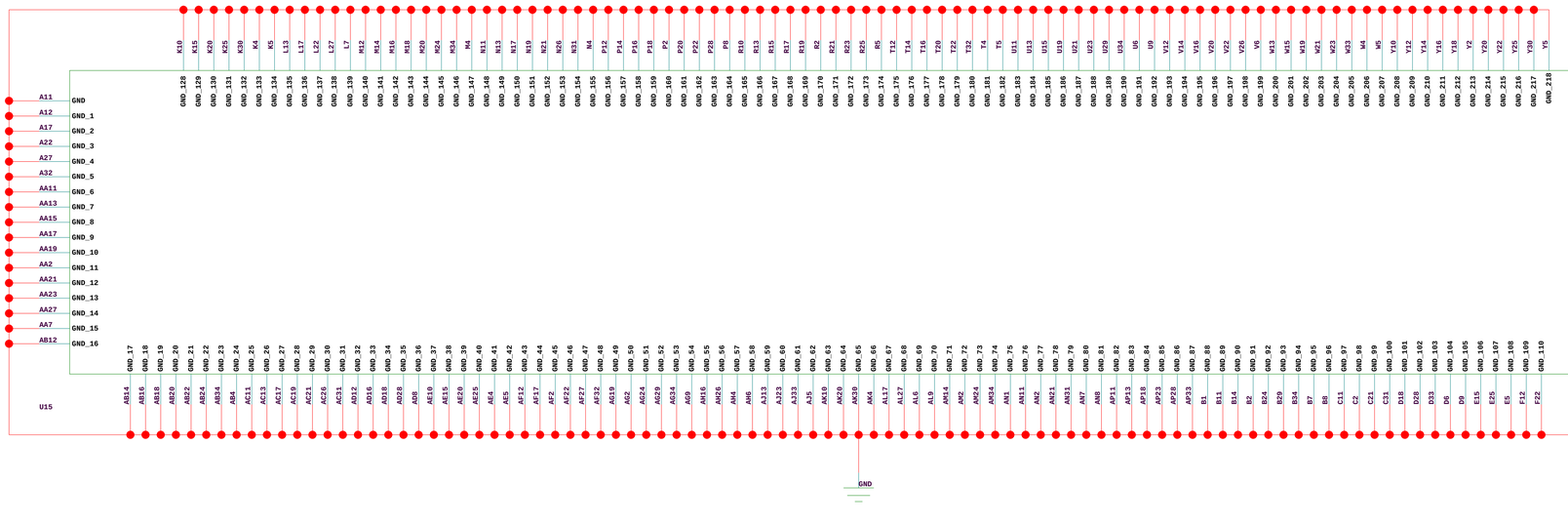




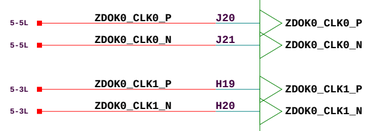


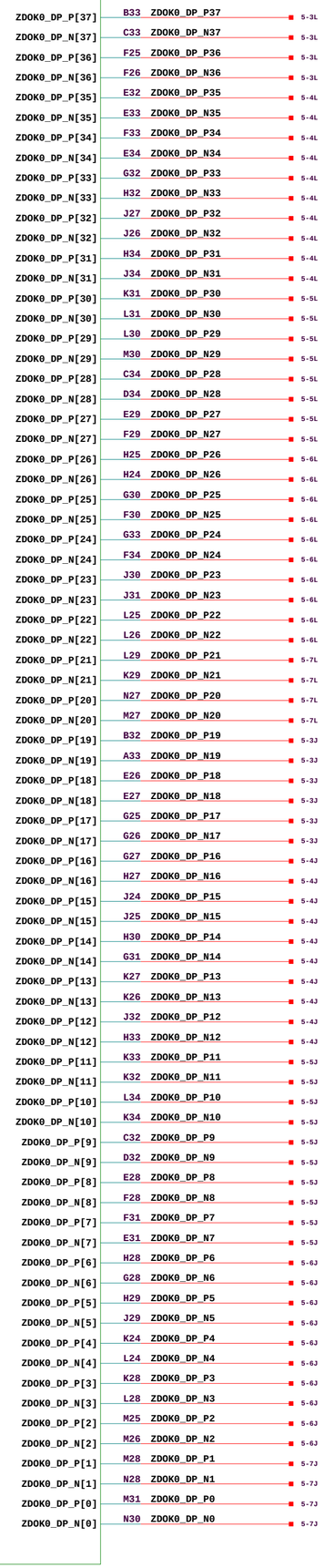






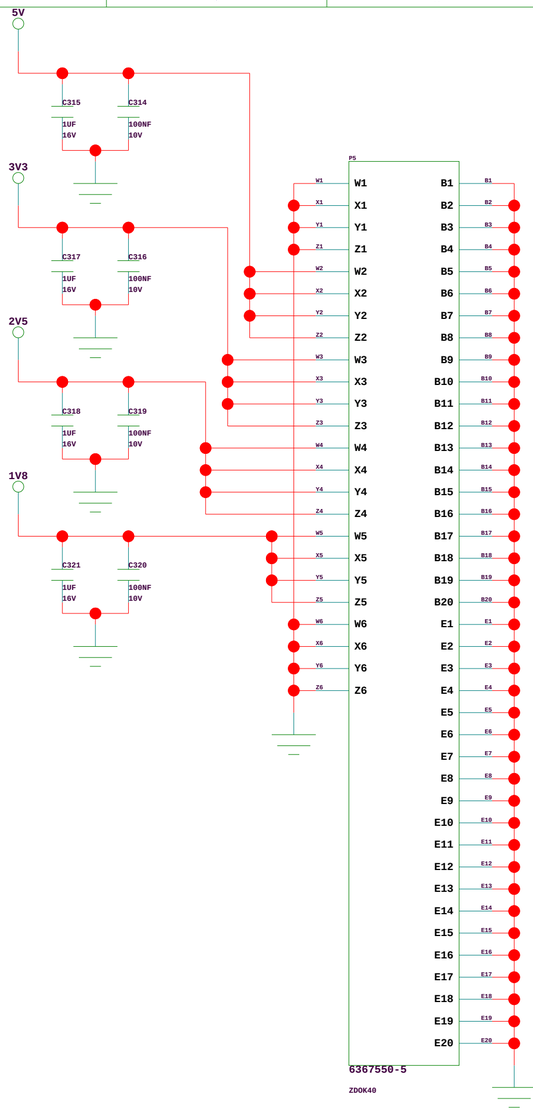
ROACH/iBOB2	ROACH_5V_POWER
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 4 OF 25
11-18-2008_15:44 PATH PATH	

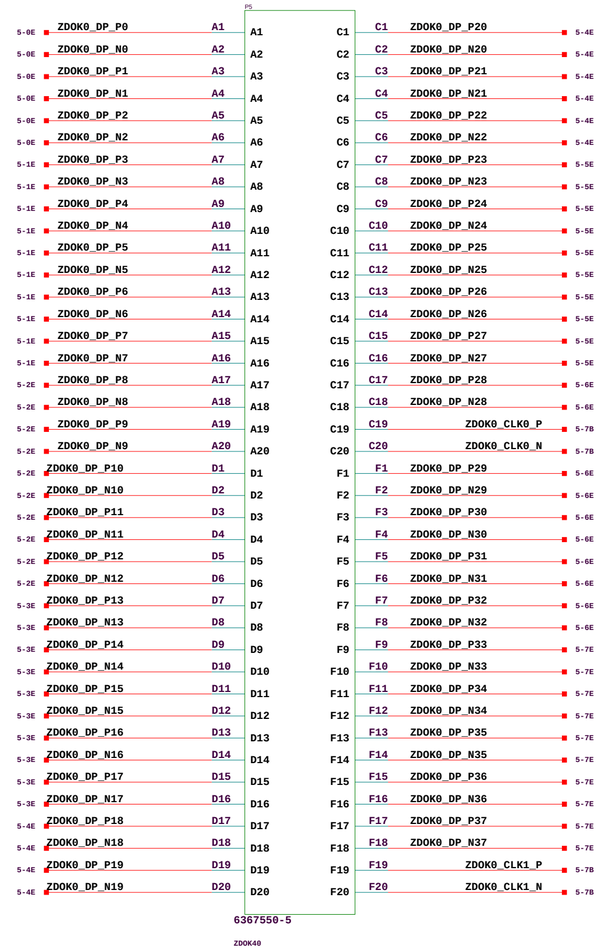




U15

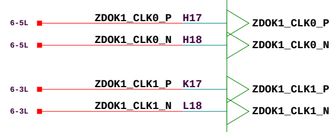
BANKS=3, 11, 15, 19

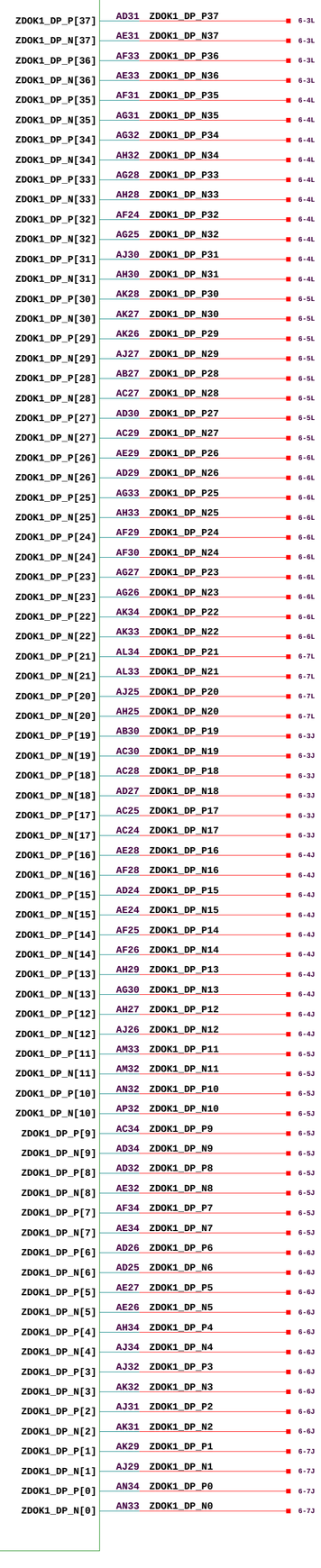




PLACE TEXT ON PCB: ZDOK0

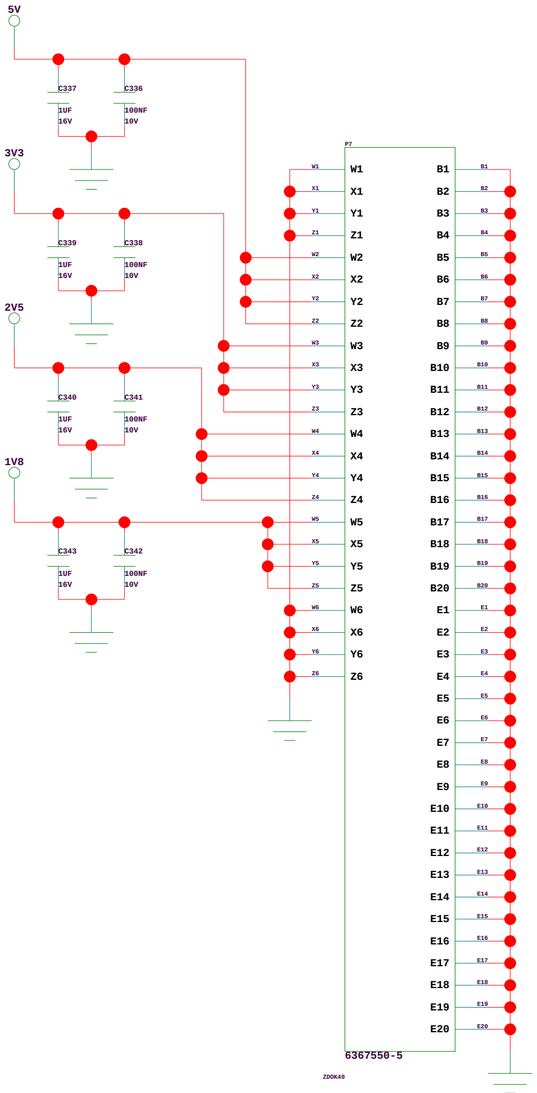
ROACH/iBOB2	**ROACH_ADC_0**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-18-2008_15:44 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 5 OF 25

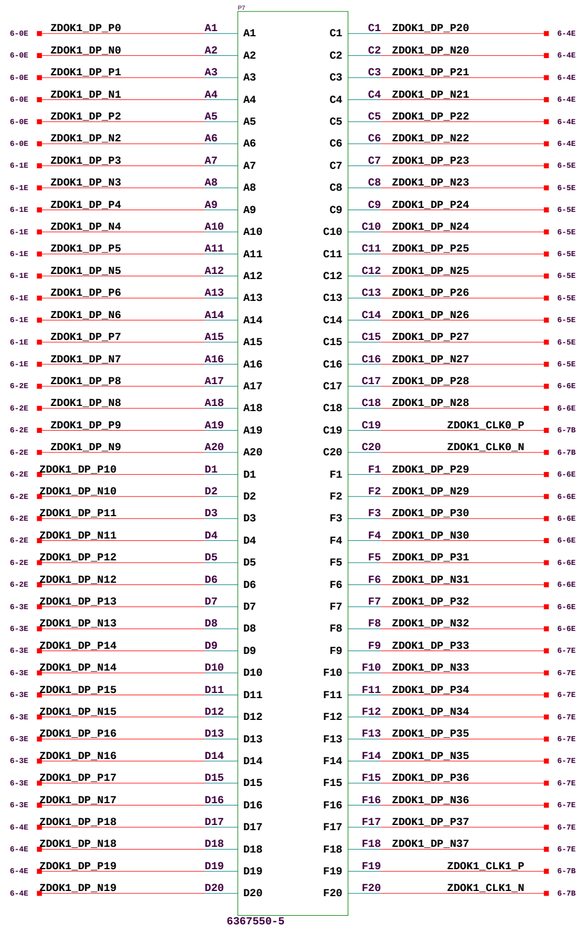




U15

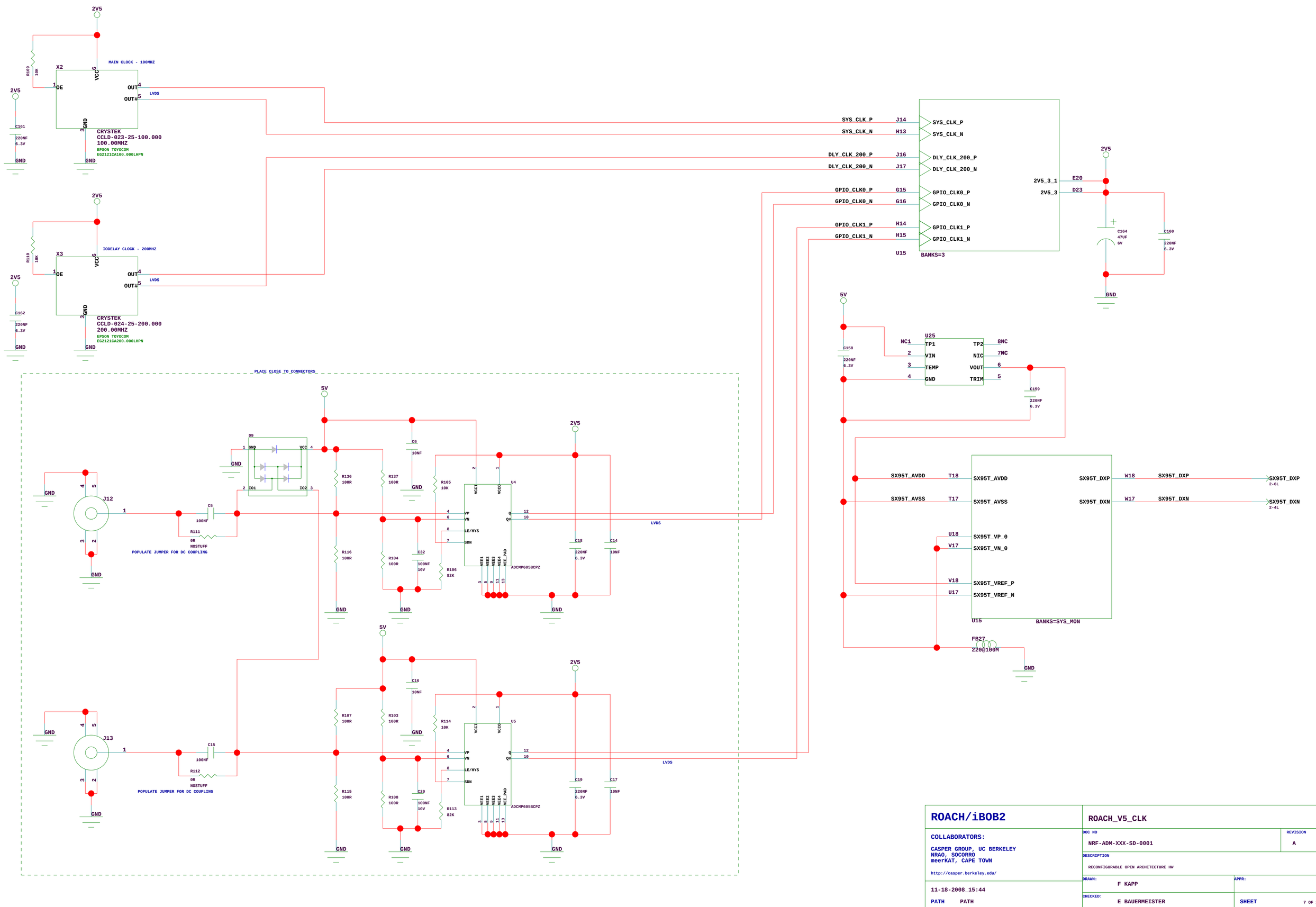
BANKS=3, 13, 17, 21





PLACE TEXT ON PCB: ZDOK1

ROACH/iBOB2	**ROACH_ADC_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-18-2008_15:44 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 6 OF 25



ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
11-18-2008_15:44 PATH PATH	

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB3 220@100M
FB4 220@100M
C84 220NF 6.3V
C93 220NF 6.3V
C92 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_112 AL8 MGTAVCC_126
AM8 MGTAVCC_126_1
MGTAVCCPLL_112 AM9 MGTAVCCPLL_126
MGTAVTTRX_112 AM6 MGTAVTTRX_126
NC AL7 MGT_126_REF_CLK_P
NC AM7 MGT_126_REF_CLK_N
MGTRX0_112_P AP6 MGTRX0_126_P
MGTRX0_112_N AP7 MGTRX0_126_N
MGTRX1_112_P AP9 MGTRX1_126_P
MGTRX1_112_N AP8 MGTRX1_126_N
U15
MGTAVTTTX_126_1 AM5 MGTAVTTTX_112
MGTAVTTTX_126 AM10
MGTTX0_126_P AN5 MGTTX0_112_P
MGTTX0_126_N AN6 MGTTX0_112_N
MGTTX1_126_P AN10 MGTTX1_112_P
MGTTX1_126_N AN9 MGTTX1_112_N
MGT_AVTT
FB5 220@100M
C96 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C106 10NF 25V
C107 10NF 25V
C109 10NF 25V
C108 10NF 25V
V1 V2 V3 V4 V5 V6 V7 V8
2V5
FB26 220@100M
C137 220NF 6.3V
R84 10K
JP6
X1 CCLD-023-25-156.250 156.25MHZ
OE VCC OUT OUT GND
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
C64 220NF 6.3V
C65 220NF 6.3V
C66 10NF 6.3V
C67 10NF 6.3V
U8 SY89832UMI
VCC1 VCC2 IN IN VT VREF-AC EN EN GND EXP_PAD
Q0 Q0 Q1 Q1 Q2 Q2 Q3 Q3
R178 100R
R176 100R
C75 100NF 6.3V
C74 100NF 6.3V
C71 100NF 6.3V
C70 100NF 6.3V
MGT_REFCLK_Q1_1_P
MGT_REFCLK_Q1_1_N
MGT_REFCLK_Q1_3_P
MGT_REFCLK_Q1_3_N
MGT_REFCLK_Q1_1_P 9-1B
MGT_REFCLK_Q1_1_N 9-1B
MGT_REFCLK_Q1_3_P 8-1D
MGT_REFCLK_Q1_3_N 8-1D
3V3
R75 100R
D2
OPTICAL MODULE FAULT - RED LED
P3 FCN-268F036-G/3DB
DL0P DL0N DL1P DL1N DL2P DL2N DL3P DL3N
SL0P SL0N SL1P SL1N SL2P SL2N SL3P SL3N
SIG_GND1 SIG_GND2 SIG_GND3 SIG_GND4 SIG_GND5 SIG_GND6 SIG_GND7 SIG_GND8 SIG_GND9
G1 G2 G3 G4 G5 G6 G7 G8 G9
FAULT0
G4 AND G8 CONNECTED IN 2X2 MODULE
C131 10NF
R97 5K1
RS7 3K9
U21 MAX9032AKA
RS9 6K8
C127 10NF
RS8 3K9
U22 SN74AHC1G08DCKR AND2
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB11 220@100M
FB9 220@100M
FB10 220@100M
C102 220NF 6.3V
C101 220NF 6.3V
C100 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_114 AJ4 MGTAVCC_122
AK5 MGTAVCC_122_1
MGTAVCCPLL_114 AM4 MGTAVCCPLL_122
MGTAVTTRX_114 AL3 MGTAVTTRX_122
NC AL5 MGT_122_REF_CLK_P
NC AL4 MGT_122_REF_CLK_N
MGTRX0_114_P AL1 MGTRX0_122_P
MGTRX0_114_N AM1 MGTRX0_122_N
MGTRX1_114_P AP3 MGTRX1_122_P
MGTRX1_114_N AP2 MGTRX1_122_N
U15
MGTAVTTTX_122_1 AM3 MGTAVTTTX_114
MGTAVTTTX_122 AK3
MGTTX0_122_P AK2 MGTTX0_114_P
MGTTX0_122_N AL2 MGTTX0_114_N
MGTTX1_122_P AN4 MGTTX1_114_P
MGTTX1_122_N AN3 MGTTX1_114_N
FB8 220@100M
C99 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C140 10NF 25V
C141 10NF 25V
C142 10NF 25V
C143 10NF 25V
V9 V10 V11 V12 V13 V14 V15 V16
3V3
U18 TPS2031D
IN1 IN2 EN GND OUT1 OUT2 OUT3 OC NC
R99 10K
C129 10NF
C128 100NF
C138 4.7UF 16V
C90 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB17 220@100M
FB15 220@100M
FB16 220@100M
C119 220NF 6.3V
C118 220NF 6.3V
C115 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C110 10NF 25V
C111 10NF 25V
C112 10NF 25V
C113 10NF 25V
MGTAVCC_116 AG3 MGTAVCC_118
AG4 MGTAVCC_118_1
MGTAVCCPLL_116 AH3 MGTAVCCPLL_118
MGTAVTTRX_116 AE3 MGTAVTTRX_118
MGT_REFCLK_Q2_0_P 9-11B
MGT_REFCLK_Q2_0_P AF4 MGT_118_REF_CLK_P
MGT_REFCLK_Q2_0_N AF3 MGT_118_REF_CLK_N
MGT_REFCLK_Q2_0_N 9-11B
MGTRX0_116_P AE1 MGTRX0_118_P
MGTRX0_116_N AF1 MGTRX0_118_N
MGTRX1_116_P AH1 MGTRX1_118_P
MGTRX1_116_N AG1 MGTRX1_118_N
U15
MGTAVTTTX_118_1 AJ3
MGTAVTTTX_118 AD3 MGTAVTTTX_116
MGTTX0_118_P AD2 MGTTX0_116_P
MGTTX0_118_N AE2 MGTTX0_116_N
MGTTX1_118_P AJ2 MGTTX1_116_P
MGTTX1_118_N AH2 MGTTX1_116_N
MGT_AVTT
FB14 220@100M
C116 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
V17 V18 V19 V20 V21 V22 V23 V24 V25
P3 FCN-268F036-G/3DB
DL0P DL0N DL1P DL1N DL2P DL2N DL3P DL3N
SL0P SL0N SL1P SL1N SL2P SL2N SL3P SL3N
SIG_GND1 SIG_GND2 SIG_GND3 SIG_GND4 SIG_GND5 SIG_GND6 SIG_GND7 SIG_GND8 SIG_GND9
G10 G11 G12 G13 G14 G15 G16 G17 G18
FAULT1
G4 AND G8 CONNECTED IN 2X2 MODULE
R98 5K1
R93 3K9
R94 6K8
R95 3K9
C132 10NF
C133 10NF
U20 MAX9032AKA
U23 SN74AHC1G08DCKR AND2
3V3
U19 TPS2031D
IN1 IN2 EN GND OUT1 OUT2 OUT3 OC NC
R100 10K
C135 10NF
C136 100NF
C139 4.7UF 16V
C91 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB22 220@100M
FB24 220@100M
FB23 220@100M
C123 220NF 6.3V
C114 220NF 6.3V
C125 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
C144 10NF 25V
C145 10NF 25V
C146 10NF 25V
C147 10NF 25V
MGTAVCC_118 AA3 MGTAVCC_114
AA4 MGTAVCC_114_1
MGTAVCCPLL_118 AB3 MGTAVCCPLL_114
MGTAVTTRX_118 W3 MGTAVTTRX_114
8-10B MGT_REFCLK_Q1_3_P Y4 MGT_114_REF_CLK_P
8-10B MGT_REFCLK_Q1_3_N Y3 MGT_114_REF_CLK_N
MGTRX0_118_P W1 MGTRX0_114_P
MGTRX0_118_N Y1 MGTRX0_114_N
MGTRX1_118_P AB1 MGTRX1_114_P
MGTRX1_118_N AA1 MGTRX1_114_N
U15
MGTAVTTTX_114 AC3
MGTAVTTTX_114_1 V3 MGTAVTTTX_118
MGTTX0_114_P V2 MGTTX0_118_P
MGTTX0_114_N W2 MGTTX0_118_N
MGTTX1_114_P AC2 MGTTX1_118_P
MGTTX1_114_N AB2 MGTTX1_118_N
MGT_AVTT
FB19 220@100M
C121 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
V26 V27 V28 V29 V30 V31 V32
P3 FCN-268F036-G/3DB
DL0P DL0N DL1P DL1N DL2P DL2N DL3P DL3N
SL0P SL0N SL1P SL1N SL2P SL2N SL3P SL3N
SIG_GND1 SIG_GND2 SIG_GND3 SIG_GND4 SIG_GND5 SIG_GND6 SIG_GND7 SIG_GND8 SIG_GND9
G10 G11 G12 G13 G14 G15 G16 G17 G18
FAULT2
G4 AND G8 CONNECTED IN 2X2 MODULE
R82 100R
OPTICAL MODULE FAULT - RED LED
D3
R91 5K1
R92 3K9
R96 6K8
R97 3K9
C134 10NF
C137 10NF
U24 MAX9032AKA
U25 SN74AHC1G08DCKR AND2
3V3
U22 TPS2031D
IN1 IN2 EN GND OUT1 OUT2 OUT3 OC NC
R101 10K
C140 10NF
C141 100NF
C142 4.7UF 16V
C143 22UF

ROACH/iBOB2	**ROACH_TRANSCEIVERS0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-18-2008_15:44	DRAWN: F KAPP APPR:
PATH	CHECKED: E BAUERMEISTER SHEET: 8 OF 25

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

G4 AND G8 CONNECTED IN
2X2 MODULE

OPTICAL MODULE FAULT - RED LED

CCLD-023-25-156.250
156.25MHZ

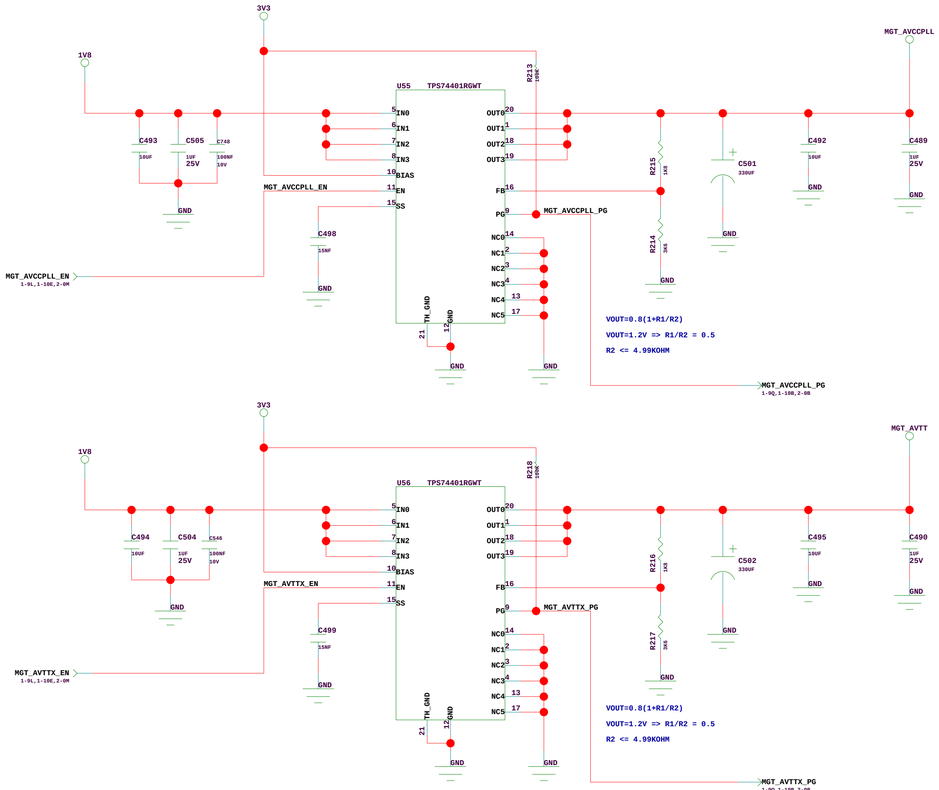
FCN-268F036-G/3DB

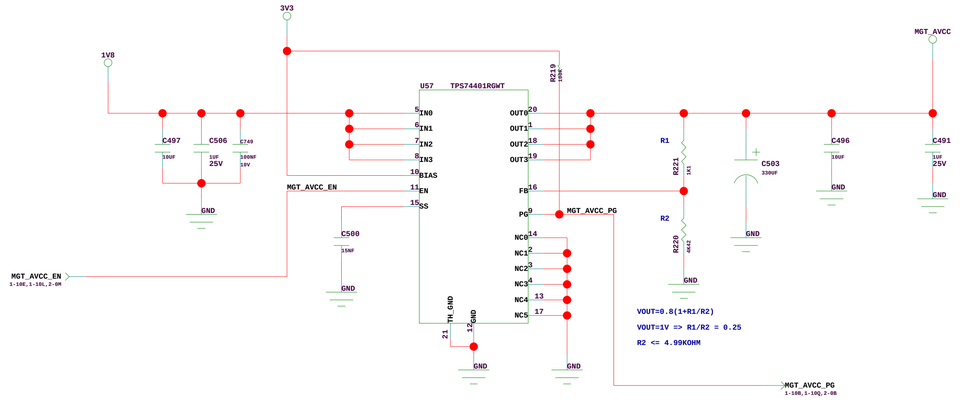
TPS2031D

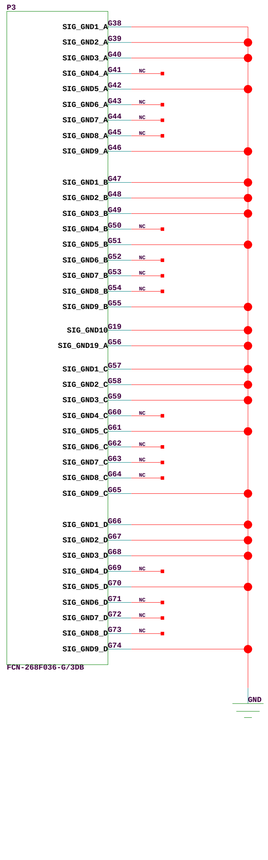
SN74AHC1G08DCKR

MAX9032AKA

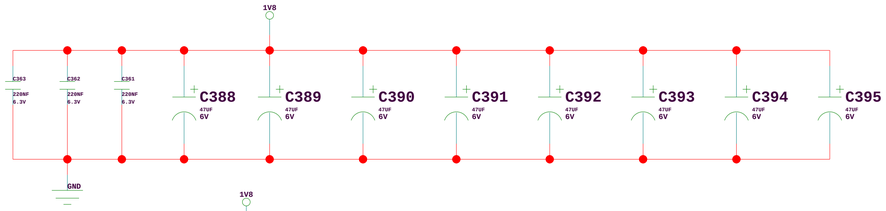
ROACH/iBOB2	ROACH_TRANSCEIVERS2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-18-2008_15:44	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 9 OF 25

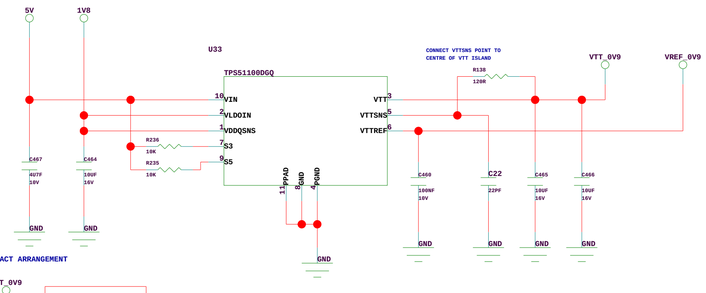




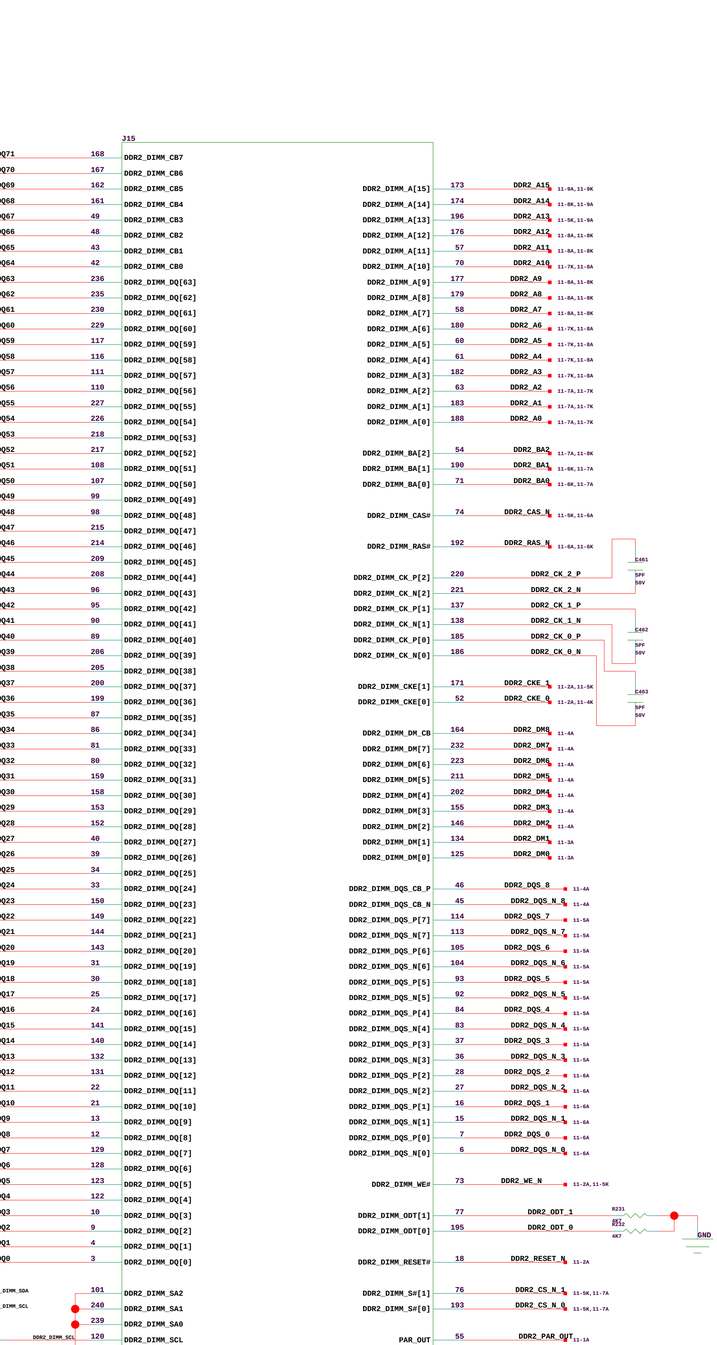


ROACH/iBOB2	**ROACH_TRANSCEIVERS_PSU**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-18-2008_15:44	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 10 OF 25





VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
PLACE ONE 10uF CAPACITOR ON EITHER END OF ISLAND



ROACH/iBOB2	**ROACH_DDR2_DIMM**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE NW
11-18-2008_15:44 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 11 OF 25

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

11-18-2008_15:44

PATH PATH

ROACH_DIFF_GPIO

DOC NO: NRF-ADM-XXX-SD-0001
REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 12 OF 25

GPIOLVC33[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

GPIOLVC33[3] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

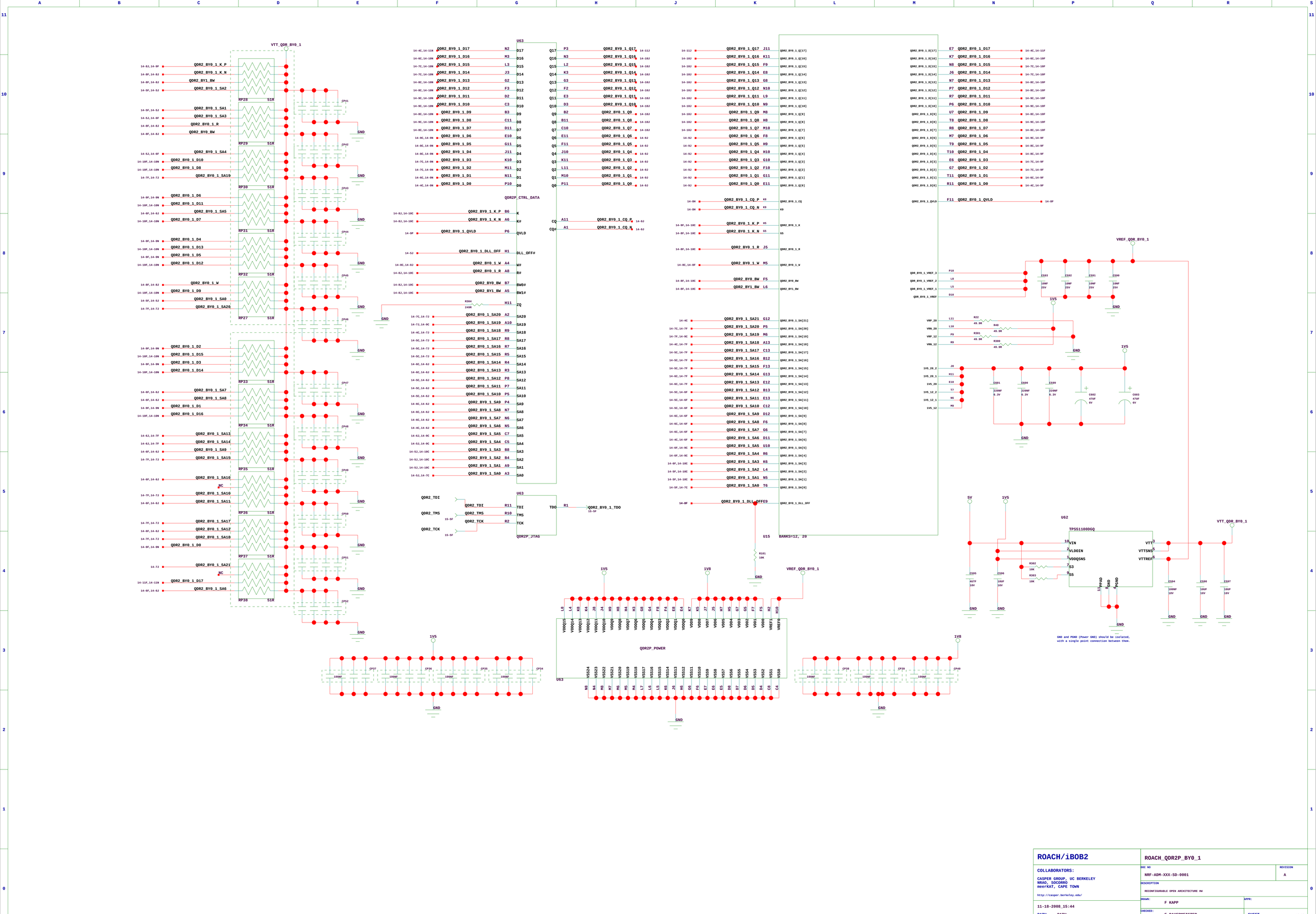
IF CR10 IS ON, CLOCK CAPABLE GPIO'S ARE OUTPUTS

U15
BANKS=5, 11, 25

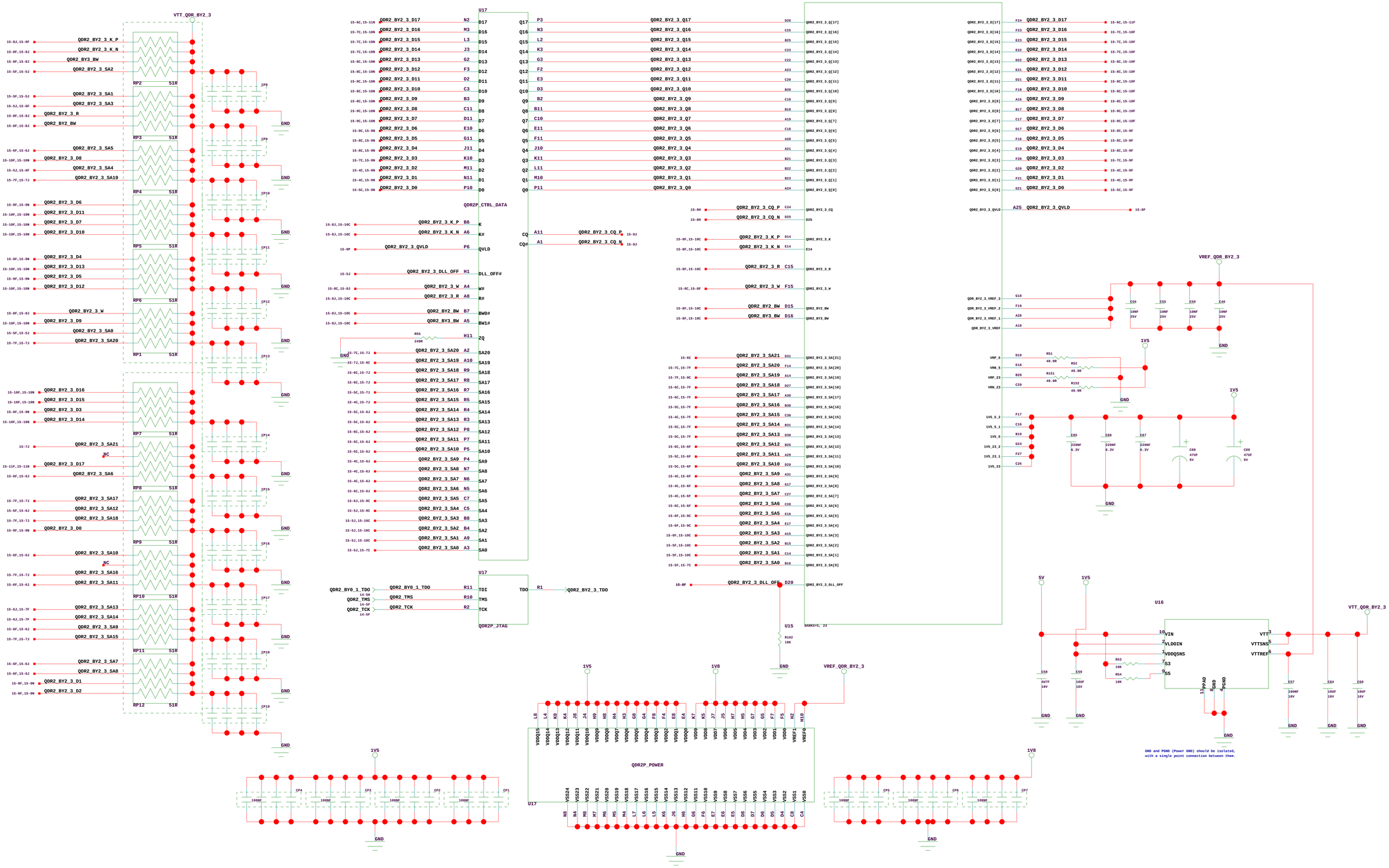
74AVCH4T245DGVRE4

N2520-6VDC-RB-WE

ROACH/iBOB2	ROACH_GPIO_MISC
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MM
11-18-2008_15:44; PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 13 OF 25



ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-18-2008_15:44 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 14 OF 25



ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

11-18-2008_15:44

PATH PATH

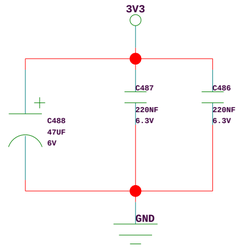
ROACH_QDR2P_BY2_3

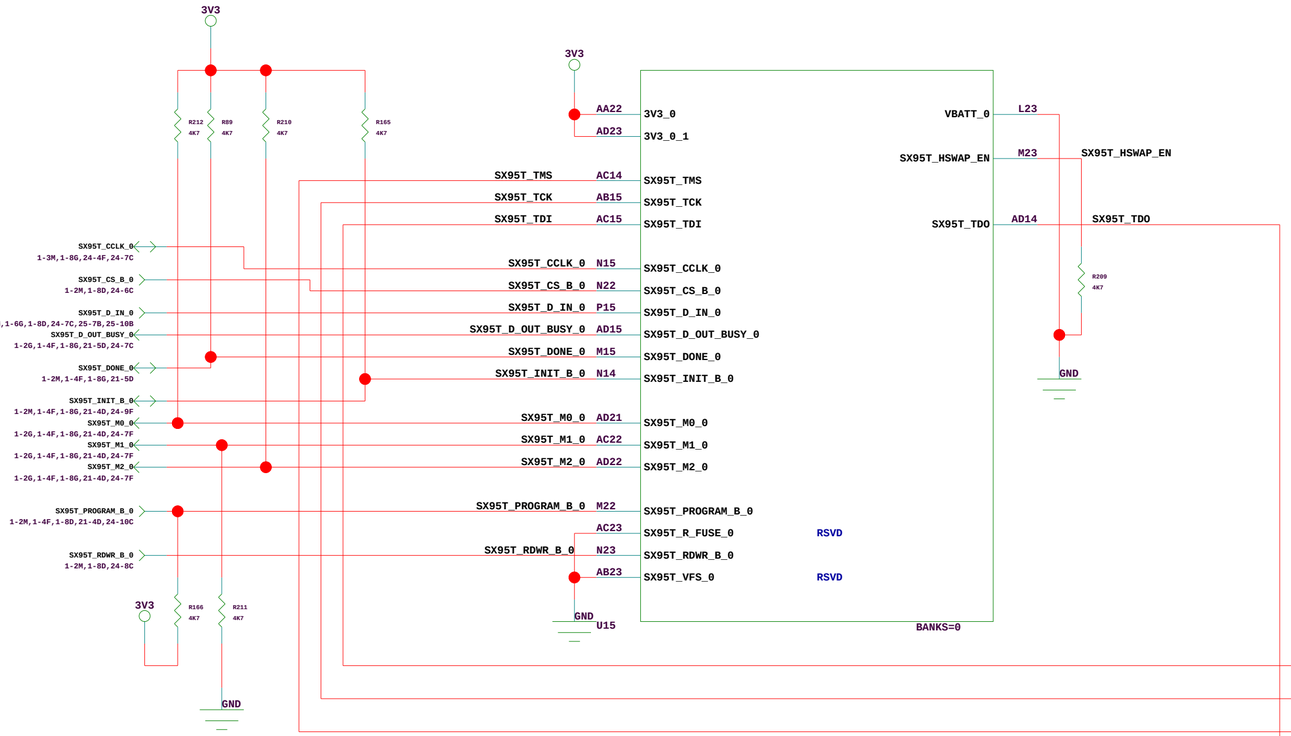
DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET: 15 OF 25

TBD

VALID CONFIGURATION MODES

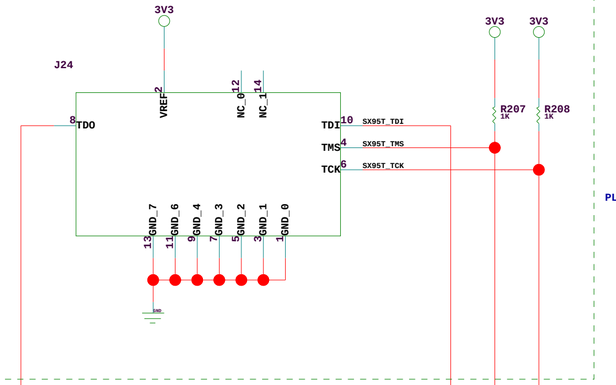
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

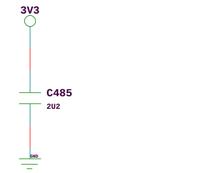




Xilinx
Programing Cable

JTAG





PLACE NEAR CPLD JTAG CONNECTOR

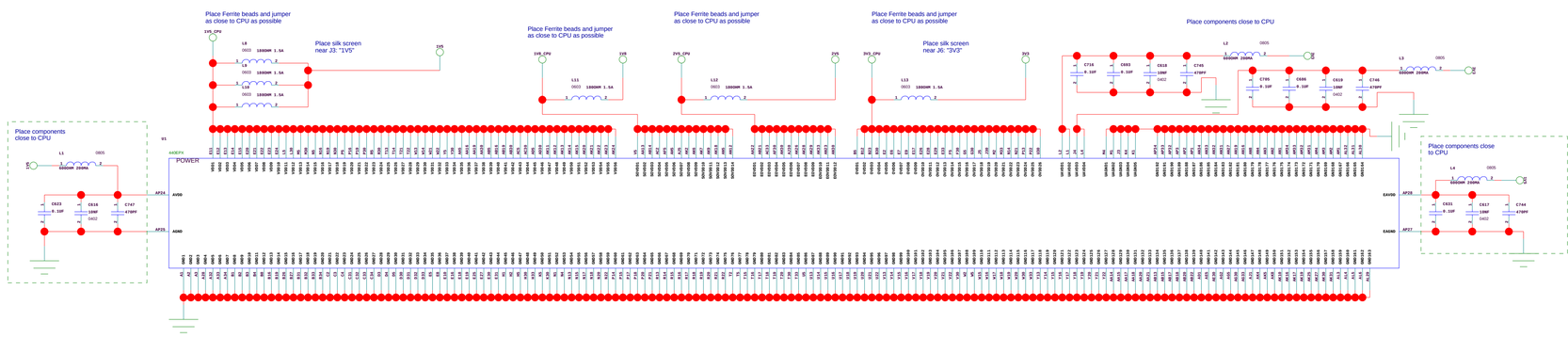
CPLD_TDO 1-3M,1-8D,24-5M

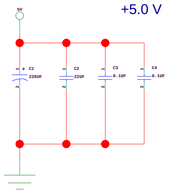
SX95T_TCK 1-3G,1-8D,24-5M

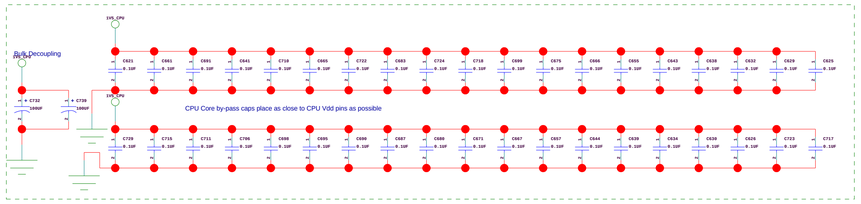
SX95T_TMS 1-3G,1-8D,24-5M

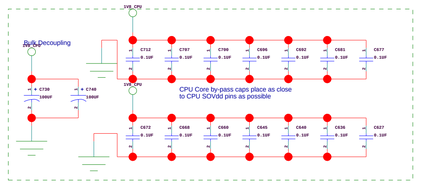
SX95T_TDO 1-3G,1-8G,24-6M

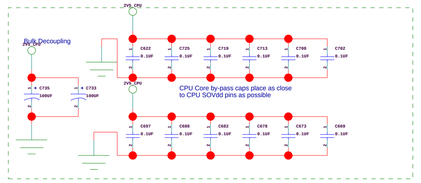
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-18-2008_15:44 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25

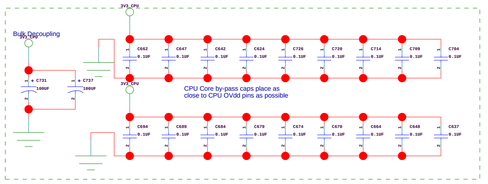


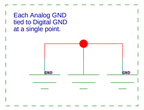










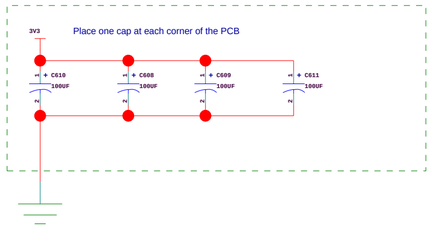


REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: **CASPER GROUP, UC BERKELEY** **NRAO, SOCORRO** **meerKAT, CAPE TOWN** http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET: 17 OF 25
11-18-2008_15:44 PATH PATH	

REMOVED 3V3 GENERATION



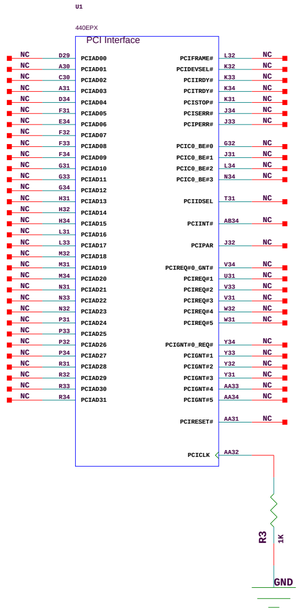
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

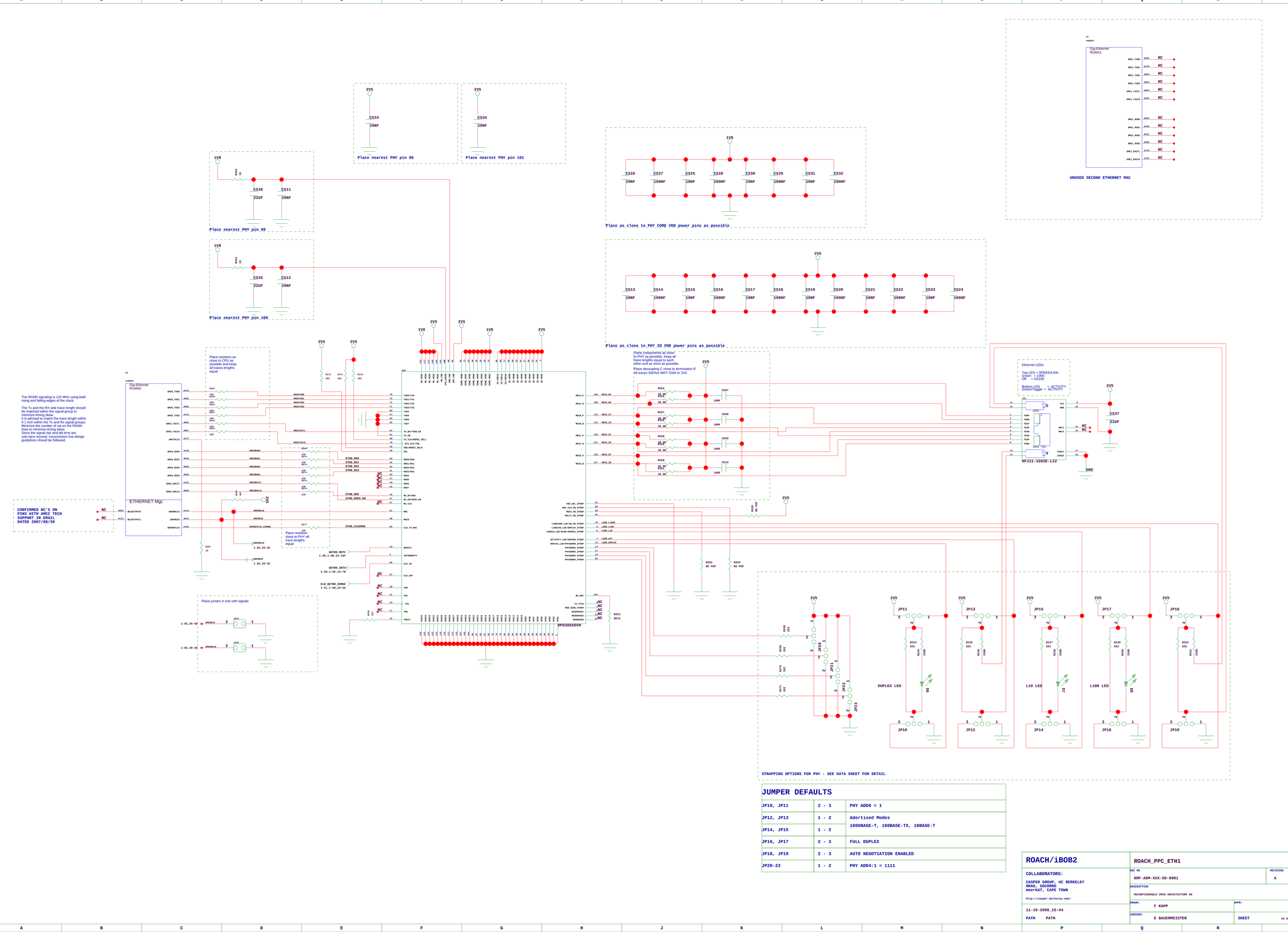
REMOVED +2V5 GENERATION

ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET: 18 OF 25
11-18-2008_15:44 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25
11-18-2008_15:44 PATH PATH	



JUMPER DEFAULTS

JP10, JP11	2 - 3	PHY ADD0 = 1
JP12, JP13	1 - 2	Adertised Modes 1000BASE-T, 100BASE-TX, 10BASE-T
JP14, JP15	1 - 2	
JP16, JP17	2 - 3	FULL DUPLEX
JP18, JP19	2 - 3	AUTO NEGOTIATION ENABLED
JP20-23	1 - 2	PHY ADD4:1 = 1111

ROACH/iBOB2	ROACH_PPC_ETH1
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 20 OF 25
11-18-2008_15:44	
PATH PATH	

U1

USB 2.0 DEVICE

440EPX

USB2CLK — A5 — NC

SECOND USB INTERFACE NOT IMPLEMENTED

NOTE:

SX95T_D_IN_0 ON SHEET 25, GPIO10

GPIO28/USB2TXVAL	C6	SX95T_D_OUT_BUSY_0	SX95T_D_OUT_BUSY_0 1-2G,1-4F,1-8G,16-4B,24-7C
USB2TXRDY_REFEN	B6	NC	
USB2RXACT_HOLDREQ_RCVINH	D7	NC	
USB2RXVAL_LEAKTEST2	C8	NC	
GPIO27/USB2RXERR_EXTREQ#	A4	SX95T_DONE_0	SX95T_DONE_0 1-2M,1-4F,1-8G
GPIO30/USB2XCVRSEL_EXTACK#	M3	SX95T_INIT_B_0	SX95T_INIT_B_0 1-2M,1-4F,1-8G,24-9F
GPIO31/USB2TERMSEL_BUSREQ	P4		
USB2LS0_DRVINH1	R2	SX95T_M0_0	SX95T_M0_0 1-2G,1-4F,1-8G,16-3B,24-7F
USB2LS1_LEAKTEST_HOLDPRI	P1	NC	
GPIO32/USB2OM0	R3	SX95T_M1_0	SX95T_M1_0 1-2G,1-4F,1-8G,16-3B,24-7F
GPIO33/USB2OM1	R4		
GPIO29/USB2SUSP_HOLDACK	C5	SX95T_M2_0	SX95T_M2_0 1-2G,1-4F,1-8G,16-3B,24-7F
		SX95T_PROGRAM_B_0	SX95T_PROGRAM_B_0 1-2M,1-4F,1-8D,16-3B,24-10C

NOTE:

USB HOST ONLY

USB 2.0 PHY
HOST/DEVICE

USB2XCVR — J2 — USB2_XCVR_D+

USB2XCVR# — J1 — USB2_XCVR_D-

USB2REXT — L3 — R182 3K4 0402 — GND

USB2XTAL — N2

USB2XTAL# — N3

CLK_USB2_48MHZ — CLK_USB2_48MHZ
1-4B,1-4L,23-4G

CRITICAL PLACEMENT

Place SP2 very close to P6

SP2 — SOT23 — PGB102ST23WR

SP2 — SOT23 — PGB102ST23WR

GND

5V — PTC1 1206L050 500MA — C614 220UF 10V — C612 100NF 10V — C613 1NF 50V

VR4 0603 5.5V 20A

P6 1X4 USBA
1 VCC
2 D-
3 D+
4 GND
5
6
89485-8001

GND

ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-18-2008_15:44 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25

Z_ADDR

DDR_PA[15:0]

DDR_PDQ[63:0]

PPC_ECC[7:0]

DDR SDRAM

U1 — 64DEPX

DDR_PDQ0	MEMDATA00	MEMADDR00	DDR_PA0
DDR_PDQ1	MEMDATA01	MEMADDR01	DDR_PA1
DDR_PDQ2	MEMDATA02	MEMADDR02	DDR_PA2
DDR_PDQ3	MEMDATA03	MEMADDR03	DDR_PA3
DDR_PDQ4	MEMDATA04	MEMADDR04	DDR_PA4
DDR_PDQ5	MEMDATA05	MEMADDR05	DDR_PA5
DDR_PDQ6	MEMDATA06	MEMADDR06	DDR_PA6
DDR_PDQ7	MEMDATA07	MEMADDR07	DDR_PA7
DDR_PDQ8	MEMDATA08	MEMADDR08	DDR_PA8
DDR_PDQ9	MEMDATA09	MEMADDR09	DDR_PA9
DDR_PDQ10	MEMDATA10	MEMADDR10	DDR_PA10
DDR_PDQ11	MEMDATA11	MEMADDR11	DDR_PA11
DDR_PDQ12	MEMDATA12	MEMADDR12	DDR_PA12
DDR_PDQ13	MEMDATA13	MEMADDR13	DDR_PA13
DDR_PDQ14	MEMDATA14		
DDR_PDQ15	MEMDATA15	BA0	DDR_PBA0
DDR_PDQ16	MEMDATA16	BA1	DDR_PBA1
DDR_PDQ17	MEMDATA17	BA2	DDR_PBA2
DDR_PDQ18	MEMDATA18		
DDR_PDQ19	MEMDATA19	RAS#	DDR_PRAS#
DDR_PDQ20	MEMDATA20	CAS#	DDR_PCAS#
DDR_PDQ21	MEMDATA21	WE#	DDR_PWE#
DDR_PDQ22	MEMDATA22		
DDR_PDQ23	MEMDATA23	DM0	DDR_PDM0
DDR_PDQ24	MEMDATA24	DM1	DDR_PDM1
DDR_PDQ25	MEMDATA25	DM2	DDR_PDM2
DDR_PDQ26	MEMDATA26	DM3	DDR_PDM3
DDR_PDQ27	MEMDATA27	DM4	DDR_PDM4
DDR_PDQ28	MEMDATA28	DM5	DDR_PDM5
DDR_PDQ29	MEMDATA29	DM6	DDR_PDM6
DDR_PDQ30	MEMDATA30	DM7	DDR_PDM7
DDR_PDQ31	MEMDATA31	DM8	DDR_PDM8
DDR_PDQ32	MEMDATA32		
DDR_PDQ33	MEMDATA33	DQS0	DDR_PDQS0
DDR_PDQ34	MEMDATA34	DQS1	DDR_PDQS1
DDR_PDQ35	MEMDATA35	DQS2	DDR_PDQS2
DDR_PDQ36	MEMDATA36	DQS3	DDR_PDQS3
DDR_PDQ37	MEMDATA37	DQS4	DDR_PDQS4
DDR_PDQ38	MEMDATA38	DQS5	DDR_PDQS5
DDR_PDQ39	MEMDATA39	DQS6	DDR_PDQS6
DDR_PDQ40	MEMDATA40	DQS7	DDR_PDQS7
DDR_PDQ41	MEMDATA41	DQS8	DDR_PDQS8
DDR_PDQ42	MEMDATA42		
DDR_PDQ43	MEMDATA43	MEMODT0	DDR_PODT0
DDR_PDQ44	MEMDATA44	MEMODT1	DDR_PODT1
DDR_PDQ45	MEMDATA45		
DDR_PDQ46	MEMDATA46	BANKSELA0	DDR_PCS0#
DDR_PDQ47	MEMDATA47	BANKSELA1	DDR_PCS1#
DDR_PDQ48	MEMDATA48		
DDR_PDQ49	MEMDATA49	MEMCLKEN	DDR_PCKE
DDR_PDQ50	MEMDATA50		
DDR_PDQ51	MEMDATA51	MEMCLKOUT	DDR_PCLKOUT
DDR_PDQ52	MEMDATA52		
DDR_PDQ53	MEMDATA53	MEMCLKOUT#	DDR_PCLKOUT#
DDR_PDQ54	MEMDATA54		
DDR_PDQ55	MEMDATA55		
DDR_PDQ56	MEMDATA56		
DDR_PDQ57	MEMDATA57		
DDR_PDQ58	MEMDATA58		
DDR_PDQ59	MEMDATA59		
DDR_PDQ60	MEMDATA60		
DDR_PDQ61	MEMDATA61		
DDR_PDQ62	MEMDATA62		
DDR_PDQ63	MEMDATA63		

	ECC0	PPC_ECC0
	ECC1	PPC_ECC1
	ECC2	PPC_ECC2
	ECC3	PPC_ECC3
	ECC4	PPC_ECC4
	ECC5	PPC_ECC5
	ECC6	PPC_ECC6
	ECC7	PPC_ECC7

DDR_VREF_0V9 — 1V8 — C158 0.1UF — C149 0.1UF — C151 0.1UF 0402 — C152 0.1UF — C148 10NF 0402

Place parts as close to CPU as possible

5V — 1V8 — C459 4U7F 16V — C456 10UF 16V — GND

U32 TPS51100DGQ

10	VIN	
2	VLDOIN	
1	VDDQSNS	R230 10K
7	S3	R229 10K
8	S5	
11	PPAD	
9	GND	
4	PGND	
3	VTT	
5	VTTSNS	
6	VTTREF	

R6 120R — DDR_VTT — C453 100NF 16V — C21 22PF — C457 10UF 16V — C458 10UF 16V — GND

DDR_VREF_0V9

1V8 — L17 0603 1000HM 1.5A — C329 4U7F 16V — C300 100NF 16V — C63 10NF 25V — GND

R167 10K

DDR_PCLKOUT0 — DDR_PCLKOUT — R168 120R

Z_IN

AVDD	8	
AGND	7	
OE	22	
OS	21	
CLK	4	DDR_PCLKOUT
CLK#	5	DDR_PCLKOUT#
Y0	38	NC
Y0#	37	NC
Y1	39	DDR_PCLKOUT1
Y1#	40	DDR_PCLKOUT1#
Y2	3	NC
Y2#	2	NC
Y3	11	NC
Y3#	12	NC
Y4	14	NC
Y4#	13	NC
Y5	34	NC
Y5#	35	NC
Y6	33	NC
Y6#	32	NC
Y7	29	NC
Y7#	30	NC
Y8	19	DDR_PCLKOUT0
Y8#	18	DDR_PCLKOUT0#
Y9	16	DDR_PCLKOUT2
Y9#	17	DDR_PCLKOUT2#

Z_OUT

R169 120R — FBIN 27 — FBIN# 26 — U6 CDCU877ARHAT — GND0 — GND2 — 10 — 41 — FBOUT 24 — FBOUT# 25 — GND

FBOUT# — FBOUT — Z_FB

J8

DDR_PDQ63	153	236	DDR2_DIMM_DQ[29]
DDR_PDQ62	152	235	DDR2_DIMM_DQ[28]
DDR_PDQ61	40	230	DDR2_DIMM_DQ[27]
DDR_PDQ60	39	229	DDR2_DIMM_DQ[26]
DDR_PDQ59	34	117	DDR2_DIMM_DQ[25]
DDR_PDQ58	33	116	DDR2_DIMM_DQ[24]
DDR_PDQ57	150	111	DDR2_DIMM_DQ[23]
DDR_PDQ56	149	110	DDR2_DIMM_DQ[22]
DDR_PDQ55	144	227	DDR2_DIMM_DQ[21]
DDR_PDQ54	143	226	DDR2_DIMM_DQ[20]
DDR_PDQ53	31	218	DDR2_DIMM_DQ[19]
DDR_PDQ52	30	217	DDR2_DIMM_DQ[18]
DDR_PDQ51	25	108	DDR2_DIMM_DQ[17]
DDR_PDQ50	24	107	DDR2_DIMM_DQ[16]
DDR_PDQ49	141	99	DDR2_DIMM_DQ[15]
DDR_PDQ48	140	98	DDR2_DIMM_DQ[14]
DDR_PDQ47	132	215	DDR2_DIMM_DQ[13]
DDR_PDQ46	131	214	DDR2_DIMM_DQ[12]
DDR_PDQ45	22	209	DDR2_DIMM_DQ[11]
DDR_PDQ44	21	208	DDR2_DIMM_DQ[10]
DDR_PDQ43	13	96	DDR2_DIMM_DQ[9]
DDR_PDQ42	12	95	DDR2_DIMM_DQ[8]
DDR_PDQ41	129	90	DDR2_DIMM_DQ[7]
DDR_PDQ40	128	89	DDR2_DIMM_DQ[6]
DDR_PDQ39	123	206	DDR2_DIMM_DQ[5]
DDR_PDQ38	122	205	DDR2_DIMM_DQ[4]
DDR_PDQ37	10	200	DDR2_DIMM_DQ[3]
DDR_PDQ36	9	199	DDR2_DIMM_DQ[2]
DDR_PDQ35	4	87	DDR2_DIMM_DQ[1]
DDR_PDQ34	3	86	DDR2_DIMM_DQ[0]
PPC_ECC7	168	81	DDR2_DIMM_CB7
PPC_ECC6	167	80	DDR2_DIMM_CB6
PPC_ECC5	162	159	DDR2_DIMM_CB5
PPC_ECC4	161	158	DDR2_DIMM_CB4
PPC_ECC3	49	153	DDR2_DIMM_CB3
PPC_ECC2	48	152	DDR2_DIMM_CB2
PPC_ECC1	43	40	DDR2_DIMM_CB1
PPC_ECC0	42	39	DDR2_DIMM_CB0
	101	34	DDR2_DIMM_SA2
	240	33	DDR2_DIMM_SA1
	239	150	DDR2_DIMM_SA0
	120	149	DDR2_DIMM_SCL
	119	144	DDR2_DIMM_SDA
		143	
		31	
		30	
		25	
		24	
		141	
		140	
		132	
		131	
		22	
		21	
		13	
		12	
		129	
		128	
		123	
		122	
		10	
		9	
		4	
		3	
		879160001	

I2C0_SCLK — 1-48,1-6L,1-10B,2-2P,2S-5A
I2C0_SDATA — 1-3B,1-6L,1-10E

GND

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA2	22-9D,22-10L
DDR2_DIMM_BA[1]	190	DDR_PBA1	22-8L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-7L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	DDR_PCLKOUT2	C313 5PF 50V
DDR2_DIMM_CK_N[2]	221	DDR_PCLKOUT2#	
DDR2_DIMM_CK_P[1]	137	DDR_PCLKOUT1	C308 5PF 50V
DDR2_DIMM_CK_N[1]	138	DDR_PCLKOUT1#	
DDR2_DIMM_CK_P[0]	185	DDR_PCLKOUT0	C455 5PF 50V
DDR2_DIMM_CK_N[0]	186	DDR_PCLKOUT0#	
DDR2_DIMM_CKE[1]	171		
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-8D,22-11L
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-9D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	R226 82 4K7
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	PPC_DDR2_RESET_N 1-3B,1-3M,24-10F
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D
PAR_OUT	55	PPC_DDR2_ERROR	1 TP4
PAR_IN	68	PAR_IN	1 TP5

GND

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

DDR_VTT

22-8K,22-8D	DDR_PCKE	RP24	CP26
	DDR_PA15		
	DDR_PA14		
22-8K,22-8D	DDR_PBA2		
	DDR_PA12	RP23	CP28
	DDR_PA11		
	DDR_PA9		
	NC		
	DDR_PA7	RP22	CP29
	DDR_PA8		
	DDR_PA6		
	DDR_PA5		
	DDR_PA4	RP21	CP30
	DDR_PA3		
	DDR_PA1		
	DDR_PA2		
22-8K,22-8D	DDR_PA0	RP25	CP32
	DDR_PBA1		
	DDR_PA10		
22-8K,22-8D	DDR_PBA0		
22-7K,22-8D	DDR_PRAS#	RP26	CP31
22-3K,22-8D	DDR_PWE#		
22-3K,22-8D	DDR_PCS0#		
22-8K,22-8D	DDR_PCAS#		
22-3K,22-8D	DDR_PCS1#	RP19	CP33
22-8D	DDR_PODT0		
	DDR_PA13		
22-8D	DDR_PODT1		

GND

J8

VSS_64	237	187	VDD_9
VSS_63	234	184	VDD_8
VSS_62	231	178	VDD_7
VSS_61	228	172	VDD_6
VSS_60	225	69	VDD_5
VSS_59	222	67	VDD_4
VSS_58	219	64	VDD_3
VSS_57	216	59	VDD_2
VSS_56	213	53	VDD_1
VSS_55	210		
VSS_54	207	194	VDDQ_11
VSS_53	204	191	VDDQ_10
VSS_52	201	181	VDDQ_9
VSS_51	198	175	VDDQ_8
VSS_50	169	170	VDDQ_7
VSS_49	166	78	VDDQ_6
VSS_48	163	75	VDDQ_5
VSS_47	160	72	VDDQ_4
VSS_46	157	62	VDDQ_3
VSS_45	154	56	VDDQ_2
VSS_44	151	51	VDDQ_1
VSS_43	148		
VSS_42	145		
VSS_41	142		
VSS_40	139		
VSS_39	136		
VSS_38	133		
VSS_37	130		
VSS_36	127		
VSS_35	124		
VSS_34	121		
VSS_33	118		
VSS_32	115		
VSS_31	112		
VSS_30	109		
VSS_29	106		
VSS_28	103		
VSS_27	100		
VSS_26	97		
VSS_25	94		
VSS_24	91		
VSS_23	88		
VSS_22	85		
VSS_21	82		
VSS_20	79		
VSS_19	66		
VSS_18	65		
VSS_17	50		
VSS_16	47		
VSS_15	44		
VSS_14	41		
VSS_13	38		
VSS_12	35		
VSS_11	32		
VSS_10	29		
VSS_9	26		
VSS_8	23		
VSS_7	20		
VSS_6	17		
VSS_5	14		
VSS_4	11		
VSS_3	8		
VSS_2	5		
VSS_1	2		

879160001

GND

DDR_VREF_0V9 — VREF 1

3V3 — VDDSPD 238

1V8

GND

DDR_VREF_0V9: C432 100NF 16V, C433 10NF 25V, GND

1V8: C454 100NF 16V, C434 10NF 25V, GND

1V8: C439 100NF 16V, C443 10NF 25V, C431 100NF 16V, C444 10NF 25V, GND

1V8: C436 100NF 16V, C445 10NF 25V, C435 100NF 16V, C446 10NF 25V, GND

1V8: C438 100NF 16V, C451 10NF 25V, C437 100NF 16V, C452 10NF 25V, GND

1V8: C439 100NF 16V, C449 10NF 25V, C440 100NF 16V, C450 10NF 25V, GND

1V8: C441 100NF 16V, C448 10NF 25V, C442 100NF 16V, C447 10NF 25V, GND

PLACE NEAREST DDR2 MODULE PINS

PowerPC DRAM Interface:

- DDR2 240 pin DIMM
- 72 bit ECC
- Unbuffered and Registered DIMMs supported
- Up to 2GB supported
- CAS Latencies: 2, 2.5 or 3
- Clock Frequencies: 133MHz to 166MHz
- Single Ended Strobes

PPC DDR2 LAYOUT NOTES

ROUTE ALL DDR CLOCKS AS LENGTH MATCHED ONLY - DIFFERENTIAL ROUTING NOT REQUIRED

CLOCK DELAYS MUST ADHERE TO THE FOLLOWING:
Z_IN + Z_OUT - Z_FB = Z_ADDR + 500 ps (+-25 ps)
WHERE:
Z_IN = PROPAGATION DELAY ON DDR_PCLKOUT/DDR_PCLKOUT#
Z_OUT = PROPAGATION DELAY ON DDR_PCLKOUTn/DDR_PCLKOUTn#
Z_FB = PROPAGATION DELAY ON FBOUT/FBOUT#
Z_ADDR = PROPAGATION DELAY ON DDR_PADD[13:0]

DDR_PCLKOUTn/DDR_PCLKOUTn# NETS CAN BE SWAPPED ON CLOCK BUFFER TO EASE ROUTING

ALL DQ, DQS, DM, ADDR, CMD AND CTRL LINES LENGTH MATCHED TO 400 ps
MATCHING WITHIN BYTE LANE: 50 ps
209 ps < TRACE LENGTH < 800 ps

U6 THERMAL TAB TO BE CONNECTED TO GND PLANE WITH THERMAL VIAS

ROACH/iBOB2	ROACH_PPC_DDR2
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
11-18-2008_15:44 PATH PATH	DRAWN: F KAPP — APPR: — CHECKED: E BAUERMEISTER — SHEET 22 OF 25

PWR_GOOD
1-3G,1-4H,24-8R

3V3

PWR_GOOD monitors the +1.0v, 1V5, 1V8, 2V5, and 3V3 supplies

RESET_PB_POR#
1-3M,1-4H,24-7F

RESET_PORH
1-3G,1-4L,1-6G,24-5M,25-5G

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_3V3_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz

PLACE NEAR U9

SEL_SYSCLK
1-3M,1-4H,24-10F

CLK_UART_11_0592MHZ
1-4L,1-6G,25-3B

UART:11.0592MHZ

SYSTEM:33MHZ

CLK_CPLD_33MHZ
1-2G,1-4L,24-8C

CPLD:33MHZ

CLK_SYS_33MHZ

CLK_TMRCLK
1-2M,1-4H,24-10C

SYSERR
1-2G,1-4L,24-10C

PPC_THERMONA
1-4L,1-10E,2-4L

PPC_THERMONB
1-4L,1-10E,2-4L

PPC440EPX-NTA533T

IRQ0-9 have programmable polarity per section 10.5.7 (UIC0_PR) 440ep user manual

MONITOR_INT
1-4H,1-10E,2-2F

VS_INT#
1-4H,1-6L,25-8Q

STTM_ALERT
1-4H,1-6L,25-2B

GPIO44
1-4L

CPLD_INT
1-3M,1-4H,24-6C

NO POP
RO1 - RO5

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz ÷ 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible

CLK_SEL_M66EN
1-2M,1-4H,24-10F

PLACE NEAR U24

CLK_GETH0_25MHZ
1-4L,1-5B,29-4E

CLK_USB2_48MHZ
1-4B,1-4L,21-2C

CLK_CPLD_50MHZ
1-2G,1-4L,24-7C

TRACE & JTAG CONNECTORS

Critical placement and routing of the Trace connector and nets. Up to CPU frequency/4

TRACE PORT

R26 is for current limiting and should be <100 Ohms.

DEBUG_TRST#
1-2G,1-4L,24-9C

ROACH/iBOB2	ROACH_PPC_TST_CLK_IO
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
11-18-2008_15:44	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 23 OF 25

roach_cpld_XC2C256_7VQ100C_pcb

CLK_TMCLK	4	PAD4	
SYSRR	7	PAD8	
EXT_RESET#	9	PAD10	
SX95T_PROGRAM_B_0	10	PAD12	
SX95T_DONE_0	11	PAD15	
PCS_2	12	PAD16	
PB_WE	13	PAD17	
DEBUG_TRST#	14	PAD18	
CPU_TRST#	15	PAD19	
FWBE_0#	16	PAD20	
PADATA[0:7]	17	PAD21	
	18	PAD23	
	19	PAD28	
	20	PAD29	
	21	PAD30	
	22	PAD31	
	23	PAD32	
	24	PAD33	
	25	PAD34	
	26	PAD35	
	28	PAD44	
CLK_CPLD_33MHZ	30	PAD48	
	31	PAD49	
CLK_PERCLK	32	PAD50	
	33	PAD52	
PGE3	34	PAD54	
	35	PAD55	
SX95T_RDWR_B_0	38	PAD59	
CLK_CPLD_50MHZ	40	PAD64	
SX95T_D_IN_0	41	PAD65	
SX95T_D_OUT_BUSY_0	42	PAD66	
PER_CCLK_ENF	43	PAD67	
SX95T_CCLK_0	44	PAD68	
FRY_BY3	45	PAD69	
FWP#	46	PAD70	
EE1_WP#	48	PAD73	
EE2_BOOT_WP#	49	PAD74	
STTM_AS#	50	PAD75	
SELECTMAP_CS	51	PAD76	
PMEAD#	52	PAD77	
SX95T_CS_B_0	53	PAD81	
CPLD_INT#	54	PAD82	
PPC_RESET	56	PAD86	
SYS_CONFIG0	57	PAD87	
SYS_CONFIG1	58	PAD88	
SYS_CONFIG2	59	PAD89	
SYS_CONFIG3	60	PAD90	
SYS_CONFIG4	61	PAD95	
SYS_CONFIG5	64	PAD100	
SYS_CONFIG6	66	PAD102	
NC	68	PAD105	
NC	69	PAD107	
NC	70	PAD108	
RESET_CPLD#	71	PAD109	
NC	74	PAD112	
NC	75	PAD113	

SYS_CONFIG[6:0] — 1-3G,1-10E,2-2R

RESET_CPLD# — 1-2M,1-5G,25-3J

PAD217	142	NC	
PAD214	140	NC	
PAD213	139	GETH0_RST#	1-3M,1-5B,28-4E
PAD212	138	PPC_DDR2_RESET_N	1-3B,1-3M,22-3K
PAD211	137	CLK_SEL_MGGEN	1-2M,1-4A,23-5D
PAD208	136	SEL_SYSCLK	1-3M,1-4H,23-7G
PAD207	135	NC	
PAD206	134	NC	
PAD204	133	NC	
PAD199	132	NC	
PAD197	131	SX95T_INIT_B_0	1-2M,1-4F,1-8G,21-4D
PAD196	130	NC	
PAD195	129		
PAD194	128		
PAD192	126		
PAD191	125	NC	
PAD190	124	NC	
PAD187	121	MMC_WP	
PAD186	120	DAT1	
PAD178	119	DAT0_DO	
PAD177	118	DAT7	
PAD176	117	DAT6	
PAD175	116	CLK_SCLK	
PAD173	115	DAT5	
PAD171	114	DAT4	
PAD169	113	CMD_DI	
PAD168	112	DAT3	
PAD167	111	DAT2	
PAD166	110	MMC_CD	
PAD163	107	SX95T_M0_0	1-2G,1-4F,1-8G,16-3B,21-4D
PAD162	106	SX95T_M1_0	1-2G,1-4F,1-8G,16-3B,21-4D
PAD161	105	SX95T_M2_0	1-2G,1-4F,1-8G,16-3B,21-4D
PAD160	104	NC	
PAD158	103	RESET_PB_POR#	1-3M,1-4G,23-8E
PAD156	102	USER_LED0	
PAD154	101	USER_LED1	
PAD152	100	SYSERR#	
PAD146	98	RESET_BUFPOR#	
PAD145	97		
PAD144	96		
PAD143	95	USER_DIP0	
PAD142	94	USER_DIP1	
PAD138	92	USER_DIP2	
PAD137	91	USER_DIP3	
PAD134	88		
PAD133	87		
PAD132	86	NC	
PAD131	85	NC	
PAD125	83	NC	
PAD121	82	NC	
PAD120	81	NC	
PAD119	80	NC	
PAD118	79	NC	
PAD117	78	NC	
PAD115	77	NC	
PAD114	76	NC	

U54 — XC2C256_7VQ144C

SD/MMC/MMCPLUS CONNECTOR

J17 — SDSR13-A0-0005

4	CMD/DI	DAT0/DO	13
9	CLK/SCLK	DAT1	14
		DAT2	1
8	VDD	DAT3	2
7	VSS1	DAT4	3
11	VSS2	DAT5	5
		DAT6	10
6	SD_CD_COM	DAT7	12
15	SD_WP_COM		
		MNT1	16
		MNT2	17

BOOT_CFG0 — 1-2M,1-5G,25-1J
BOOT_CFG1 — 1-2M,1-5G,25-1J
BOOT_CFG2 — 1-2M,1-5G,25-1J

RESETS

CPU_TRST# = '1' when JTAG_TRST# = '1' and RESET_POR# = '1' else '0'; see errata sheet

SysErr will be used to drive Status LED (active H)

User DIP-Switch

Boot Configuration

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

Configuration DIP-Switch

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

U54 — XC2C256_7VQ144C

SX95T_TDO	NC	2	
	NC	3	
SX95T_TMS	NC	5	
SX95T_TCK	NC	6	
CPLD_TDO	NC	39	
		63	TDI
		65	TMS
		67	TCK
		122	TDO
RESET_PORB		143	PAD218

1-3M,1-4L,1-6G,23-9J,25-5G

roach_cpld_XC2C256_7VQ100C_configpins

XC2C256_7VQ144C

ENABLE PER_CLK CONNECTION TO CONFIGURATION I/F MUST CO-ORDINATE WITH SX95T_CCLK_0 AND MODE TO AVOID CLASH

SN74AHC1G125DCKT — U2

CLK_PERCLK — 1-2G,1-5L,24-8B,25-6F
SX95T_CCLK_0 — 1-3M,1-8G,24-7C

PLACE AT END OF DAISY CHAIN

roach_cpld_XC2C256_7VQ100C_powerpins

U54 — XC2C256_7VQ144C

VCC	VAUX	VCCIO_3	VCC_1	VCCIO_4	VCCIO_5	VCC_2	VCCIO_6	VCCIO	VCCIO_1	VCCIO_2
1	8	27	37	55	73	84	93	109	127	141

GND_3	GND_4	GND_5	GND_6	GND_7	GND_8	GND_9	GND_10	GND	GND_1	GND_2
29	36	47	62	72	89	99	99	108	123	144

PLACE NEAR CPLD POWER PINS

C473–C483 — 100NF 10V

SCT595 — U35 — 74LVC1G08 — VCC, GND

PWR_GOOD — 1-3G,1-4R,23-10G

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

11-18-2008_15:44

PATH PATH

ROACH_PPC_CPLD

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	24 OF 25

PDATA[0:31]
1-3M,1-5L

PADD[2:31]

PADD[2:0]
1-3G,1-5L,24-9B

PADD30 IS THE LSB FOR 16 BIT
WIDE BUS TRANSFERS

PADD[2:31]

NOTE:
DMA SIGNALS
IN GREEN TEXT

PADD2 IS THE MSB

CHIP SELECTS CONFIG	
CS0	NOR FLASH - U42
CS1	FPGA - U15
CS2	CPLD - U54
CS3	FPGA - U15
CS4	SELECTMAP_CS
CS5	GPIO - SX95_D_IN

SX95T_D_IN_0 — 1-2M,1-6G,1-8D,16-4B,24-7C,25-7B
POE# — 1-2G,1-5L,24-8C,25-5G,25-7B,25-7M
PR_W# — 1-2G,1-5L,24-10C,25-5G,25-6M,25-7B
PWBE_0# — 1-3G,1-5L,24-9C,25-6M,25-7B
PWBE_1# — 25-6M,25-7C
PWBE_2# — 25-7C
PWBE_3# — 25-7C
PREADY — 1-2M,1-5G,24-6C,25-7B,25-9B
PBLAST# — 25-6M,25-7C
PCS_0
PCS_1
PCS_2
SELECTMAP_CS

U1
External Slave Peripheral
A4EEPX

PERDATA31 PERDATA30 PERDATA29 PERDATA28 PERDATA27 PERDATA26 PERDATA25 PERDATA24 PERDATA23 PERDATA22 PERDATA21 PERDATA20 PERDATA19 PERDATA18 PERDATA17 PERDATA16
PERADDR31 PERADDR30 PERADDR29 PERADDR28 PERADDR27 PERADDR26 PERADDR25 PERADDR24 PERADDR23 PERADDR22 PERADDR21 PERADDR20 PERADDR19 PERADDR18 PERADDR17 PERADDR16 PERADDR15 PERADDR14 PERADDR13 PERADDR12 PERADDR11 PERADDR10 PERADDR9 PERADDR8
PCS_0 PCS_1 PCS_2 PERCS0# PERCS1#_GPIO06 PERCS2#_GPIO10 PERDEF PERWE_WP PERWE_BA# PERWE_0# PERWE_1# PERWE_2# PERWE_3# PERREADY PERBLAST#
PERADDR07_GPIO08_DMAREQ2 PERADDR06_GPIO01_DMAACK2 PERADDR05_GPIO02_EOT2_TC2 GPIO03_PERADDR04_DMAREQ3 GPIO04_PERADDR03_DMAACK3 GPIO05_PERADDR02_EOT3_TC3
DMAREQ2 DMAACK2 EOT2/TC2 DMAREQ3 DMAACK3 EOT3/TC3
EXTRESET2 PERCLK PERERR_GPIO11
R6 0R CLK_PERCLK
R134 3K3 R133 3K3 R132 3K3 R84 3K3 R83 3K3 R5 3K3 3V3
R85 1K
EXT_RESET#
EPB RESET OUTPUT
1-3G,1-5L,24-10C
CLK_PERCLK
1-2G,1-5L,24-4C,24-8B

U42
FBGA64
32Mx16 MIRROR BIT
FLASH
32Mx16
4Mx8
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21_A0MB A22_16MB A23_32MB A24_512MB A25_1GB A26_2GB BYTE#
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15/A-1
WP#/ACC RY/BY# NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11
CE# OE# WE# RESET#
VCC VSS VSS VSS VSS
3V3
R86 3K3 0402
R81 3K3 0402
R87 3K3 0402
RY_BY# — 1-3G,1-6L,24-7C
WPn — 1-2M,1-5G,24-7C
PCS_0 — 1-2G,1-5L,24-8C,25-7B,25-7M,25-10B
PORn — 1-2G,1-5L,24-10C,25-6M,25-7B,25-9B
PR_WP
RESET_PORn — 1-3G,1-4L,1-6G,23-B3,24-5M

ROUTE AS DAISY CHAIN - U1 - U15 - U2 - U54 - TERMINATION
KEEP STUBS AS SHORT AS POSSIBLE

3V3 3V3_4_1 3V3_4 3V3_4_2 3V3_3 3V3_2 3V3_1_1 3V3_1
AL12 AG14 AM19 AM21 G14 D13

PER_A[30] AE23 — PADD30
PER_A[29] AE22 — PADD29
PER_A[28] AG18 — PADD28
PER_A[27] AG12 — PADD27
PER_A[26] AG15 — PADD26
PER_A[25] AG23 — PADD25
PER_A[24] AF19 — PADD24
PER_A[23] AE12 — PADD23
PER_A[22] AG16 — PADD22
PER_A[21] AF13 — PADD21
PER_A[20] AG20 — PADD20
PER_A[19] AF23 — PADD19
PER_A[18] AH17 — PADD18
PER_A[17] AH15 — PADD17
PER_SP_A[16] L20 — PADD16
PER_SP_A[15] J22 — PADD15
PER_SP_A[14] H22 — PADD14
PER_SP_A[13] L15 — PADD13
PER_SP_A[12] L16 — PADD12
PER_SP_A[11] K22 — PADD11
PER_SP_A[10] K21 — PADD10
PER_SP_A[9] K16 — PADD9
PER_SP_A[8] J15 — PADD8
PER_SP_A[7] L21 — PADD7 DMAREQ2
PER_SP_A[6] G22 — PADD6 DMAACK2
PER_SP_A[5] K23 — PADD5 EOT2/TC2
PER_SP_A[4] K14 — PADD4 DMAREQ3
PER_SP_A[3] L14 — PADD3 DMAACK3
PER_SP_A[2] J12 — PADD2 EOT3/TC3

PCS_1 K13 — PCS_1
PCS_3 AG17 — PCS_3
PER_CS0
PER_CS1
POE# AF21 — 1-2G,1-6L,24-8C,25-5G,25-7B,25-10B
PER_OE_N
PR_W# AF20 — 1-2G,1-5L,24-10C,25-5G,25-7B,25-9B
PER_R_W_N
PWBE_1# AF14 — 25-7C,25-9B
PWBE_0# AF18 — 1-3G,1-5L,24-9C,25-7B,25-9B
PER_WBE[1]
PER_WBE[0]
PBLAST# H23 — 25-7C,25-9B
PER_B_LAST
U15
BANKS=1, 2, 4
CHIP SELECT 1

PER_D[15] AG22 — PDATA7
PER_D[14] AH22 — PDATA6
PER_D[13] AH12 — PDATA5
PER_D[12] AG13 — PDATA4
PER_D[11] AH20 — PDATA3
PER_D[10] AH19 — PDATA2
PER_D[9] AH14 — PDATA1
PER_D[8] AH13 — PDATA0
PER_D[7] AF15 — PDATA15
PER_D[6] AE16 — PDATA14
PER_D[5] AE21 — PDATA13
PER_D[4] AD20 — PDATA12
PER_D[3] AF16 — PDATA11
PER_D[2] AE17 — PDATA10
PER_D[1] AE19 — PDATA9
PER_D[0] AD19 — PDATA8
PER_D_PAR[1] AG21 NC
PER_D_PAR[0] AE13 NC
PER_INT G23 — VS_INT#
PER_READY K12 — PREADY — 1-2M,1-5G,24-6C,25-7B,25-9B
PER_CLK AH18 — CLK_PERCLK

VS_INT# — 1-4H,1-6L,23-7N

C334 470F 6V
C335 470F 6V
C330 220NF 0.3V
C331 220NF 0.3V
C332 220NF 0.3V
C333 220NF 0.3V
GND

I2C0_SCLK — 1-4B,1-6L,1-10B,2-2P,22-2F
I2C0_SDATA — 1-3B,1-6L,1-10E
EE2_BOOT_WP — 1-3M,1-5G,24-7C
EE1_WP — 1-3M,1-6G,24-7C
AT24MAC602
SCL SDA A0 A1 A2 WP GND VCC
R88 15K 0402
EE1_WP
EE2_BOOT_WP

CLK_UART_11_0592MHZ — 1-4L,1-6G,23-7G
CLK_UART_11_0592MHZ

P11 1x5 VT 0.12A H SMT
P4 1x5 VT 0.12A H SMT
SCPCE
SCPDO
SCPCLK
R74 3K3 0402
R73 3K3 0402
R76 3K3 0402
R75 3K3 0402
R77 3K3 0402
R78 3K3 0402
C651 0.1UF 0402
U41 SOT23-6 AD7414-0
STTM_ALERT — 1-4B,1-6L,23-6M
STTM_AS — 1-3M,1-6G,24-7C

U1
UART
UARTSERCLK
UART1_TX_UART0_TX UART1_RX_UART0_RX UART1_RTS#_UART0_RTS# UART1_CTS#_UART0_CTS#
UART2_TX_UART0_DTR# UART2_RX_UART0_RI# UART2_RTS#_UART0_DSR# UART2_CTS#_UART0_DCD#
UART1_TX UART1_RX PERPARB_UART1_RTS# PERPARB_UART1_CTS#
UART2_TX UART2_RX CPU_UART0_DSR# CPU_UART0_DCD#
IIC0
IIC0SCLK IIC0SDATA
IIC1_SPI
SCPCLKOUT_IIC1SCLK SCPDI_IIC1SDATA SCPDO
NAND Flash Interface
NOT USED
NFALE NFCLE NFREN# NFWEN# NFRDYBUSY# NFCE3#_PERCS3#
NC NC NC NC
PCS_3

U48 TDFN_ZA-6 PI5A3157 SX0 BO TO A
U45 TDFN_ZA-6 PI5A3157 SX0 BO TO A
U46 TDFN_ZA-6 PI5A3157 SX0 BO TO A
C652 0.1UF 0402
R82 3K3 0402
UART1_CTS#
UART2_RTS#
UART2_CTS#
RESET_CPLD# — 1-2M,1-5G,24-5C
BOOT_CFG2 — 1-2M,1-5G,24-10M
BOOT_CFG1 — 1-2M,1-5G,24-11M
BOOT_CFG0 — 1-2M,1-5G,24-11M
C656 0.1UF 0402
C655 0.1UF 0402

U44 SSOP20 ICL3225ECA
U43 SSOP20 ICL3225ECA
C192 C194 C196 C198 0.1UF 0402
C193 C195 C197 C199 0.1UF 0402
C2P C1N C2P C2N VCC VP VN T1IN R1OUT T2IN R2OUT FORCEON FORCEOFF INVALID READY GND
X_UART1_TX X_UART1_RX X_UART1_RTS# X_UART1_CTS#
X_UART2_TX X_UART2_RX X_UART2_RTS# X_UART2_CTS#
R85 10K C652
R87 10K C652
C649 0.1UF 0402
C653 0.1UF 0402

P2 DB9 FEMALE RIGHT ANGLE SHIELDED
UART Port 0

J14
HLE-105-02-G-DV
UART Port 1

ROACH/iBOB2	ROACH_PPC_NVM_SERIAL
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-18-2008_15:44	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 25 OF 25