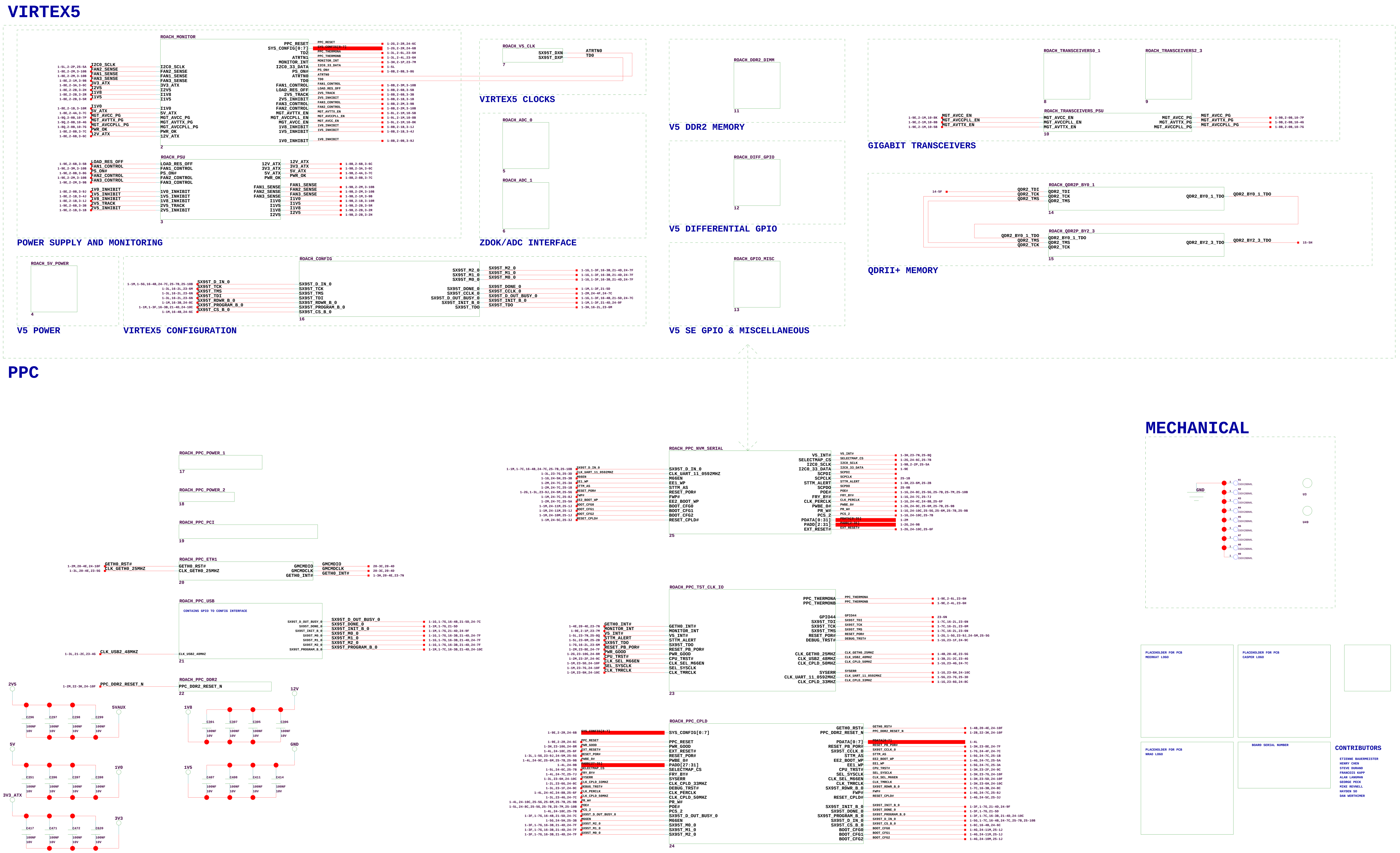

CONTRIBUTORS

ETIENNE BAUERMEISTER
HENRY CHEN
STEVE DURAND
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GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2

ROACH_TOP

COLLABORATORS:

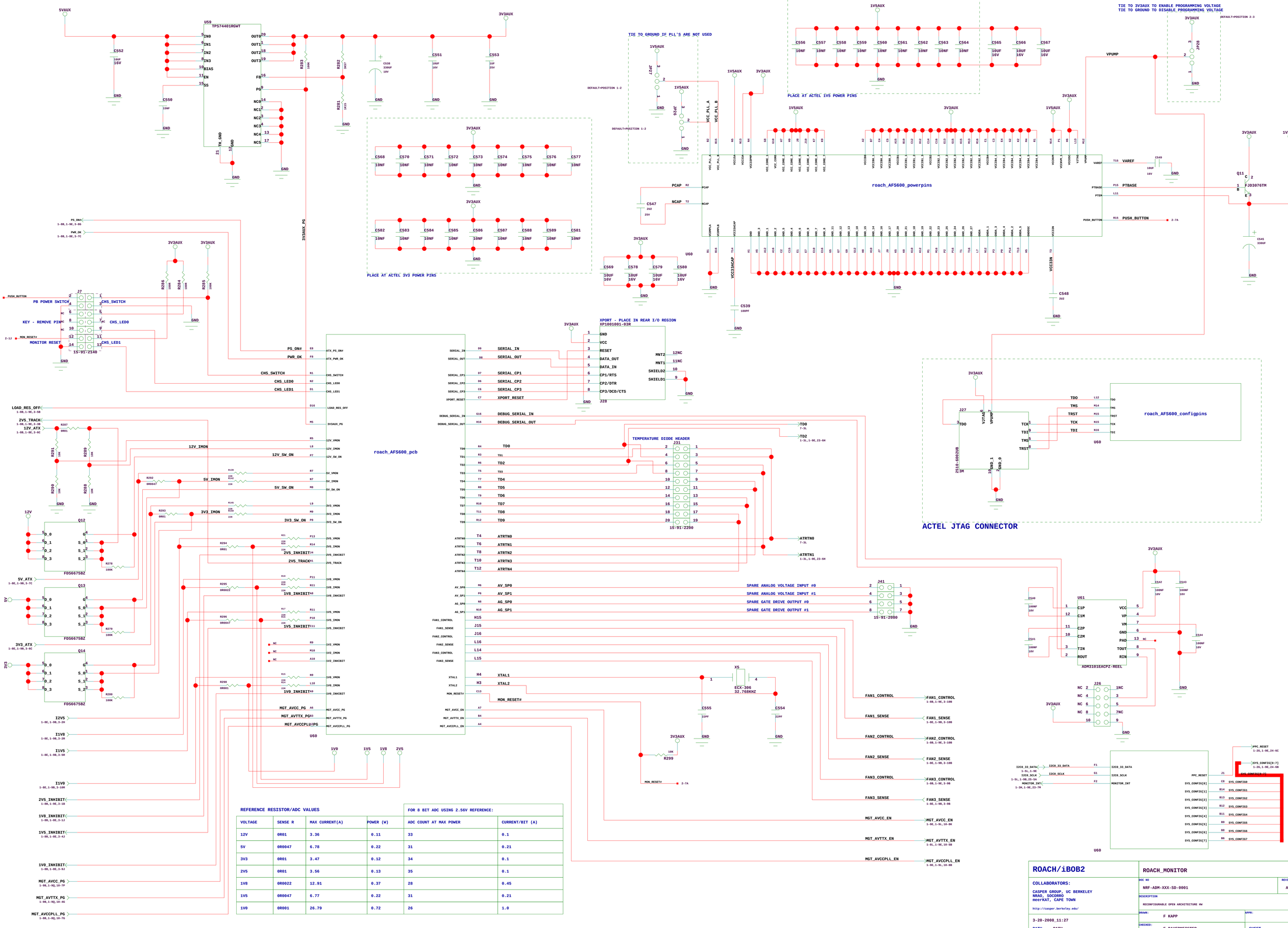
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	1 OF 25

3-20-2008_11:27

PATH PATH

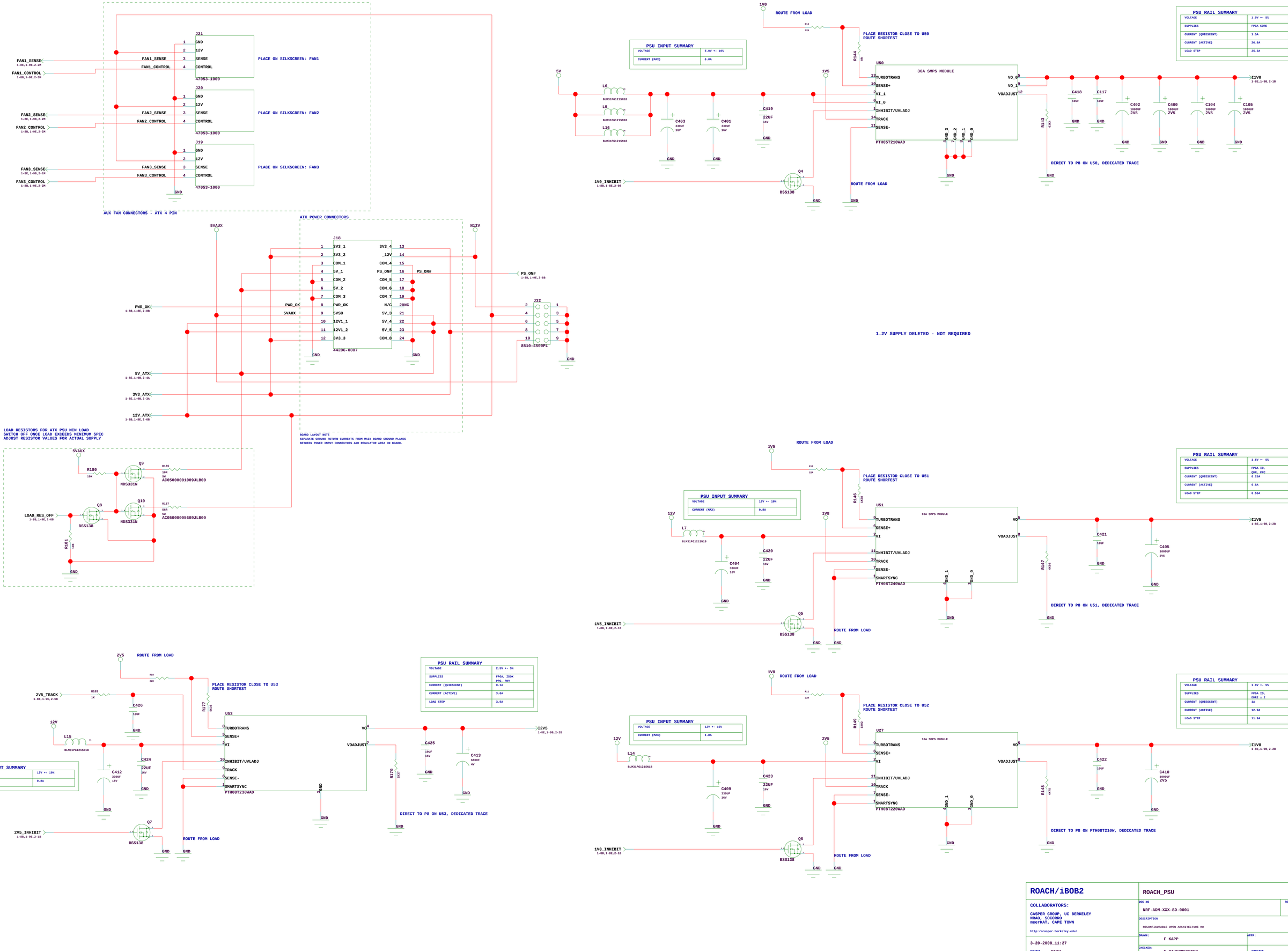


REFERENCE RESISTOR/ADC VALUES

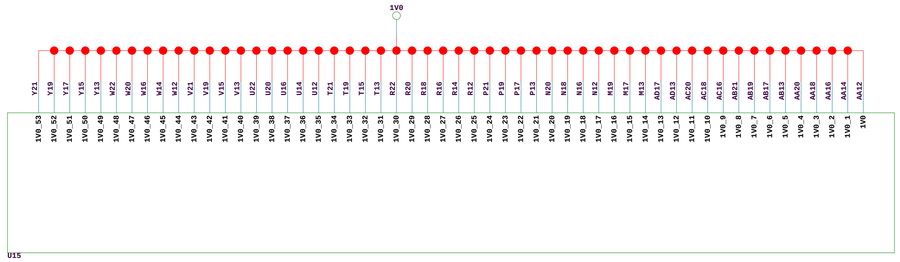
VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)
12V	0R01	3.36	0.11
5V	0R0047	6.78	0.22
3V3	0R01	3.47	0.12
2V5	0R01	3.56	0.13
1V8	0R0022	12.91	0.37
1V5	0R0047	6.77	0.22
1V0	0R001	26.79	0.72

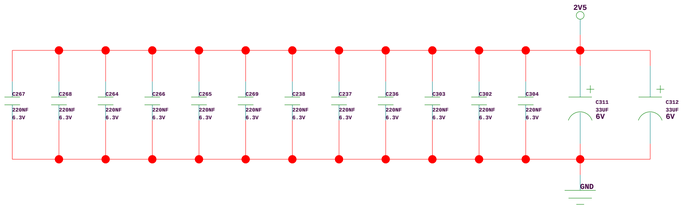
FOR 8 BIT ADC USING 2.56V REFERENCE:

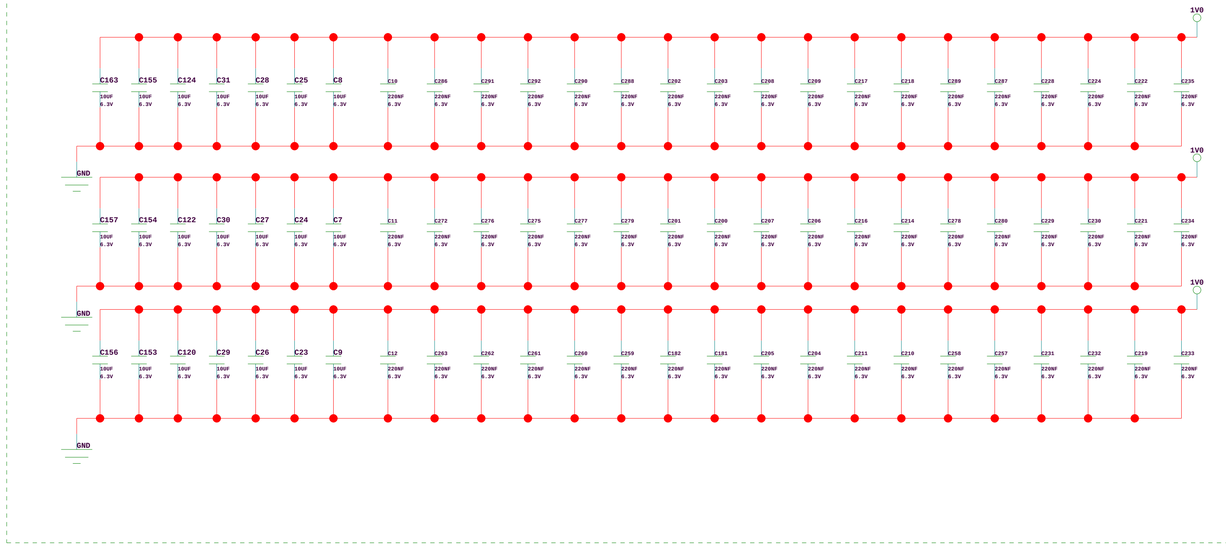
ADC COUNT AT MAX POWER	CURRENT/BIT (A)
33	0.1
31	0.21
34	0.1
35	0.1
28	0.45
31	0.21
26	1.0

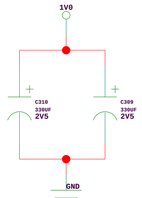


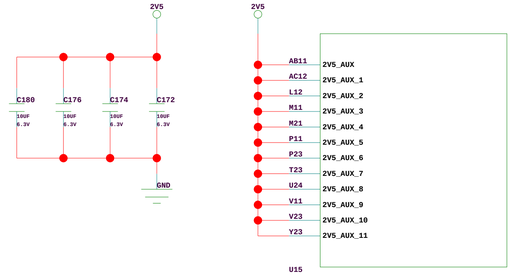
ROACH/iBOB2	ROACH_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
3-20-2008_11:27	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 3 OF 25

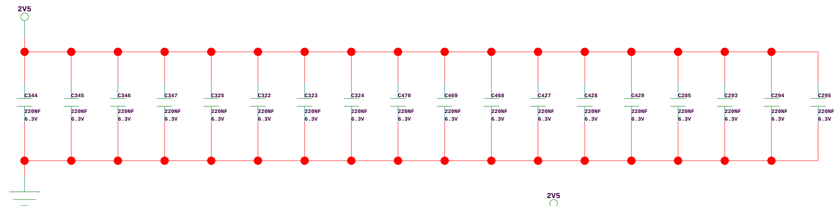


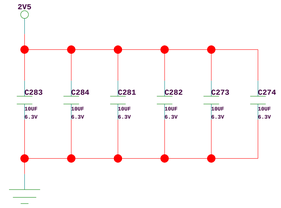


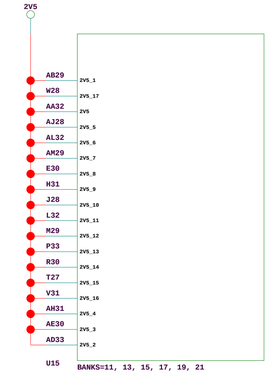


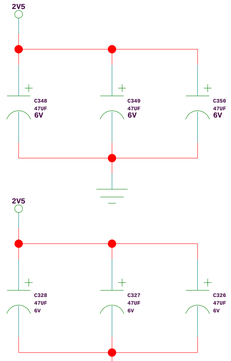


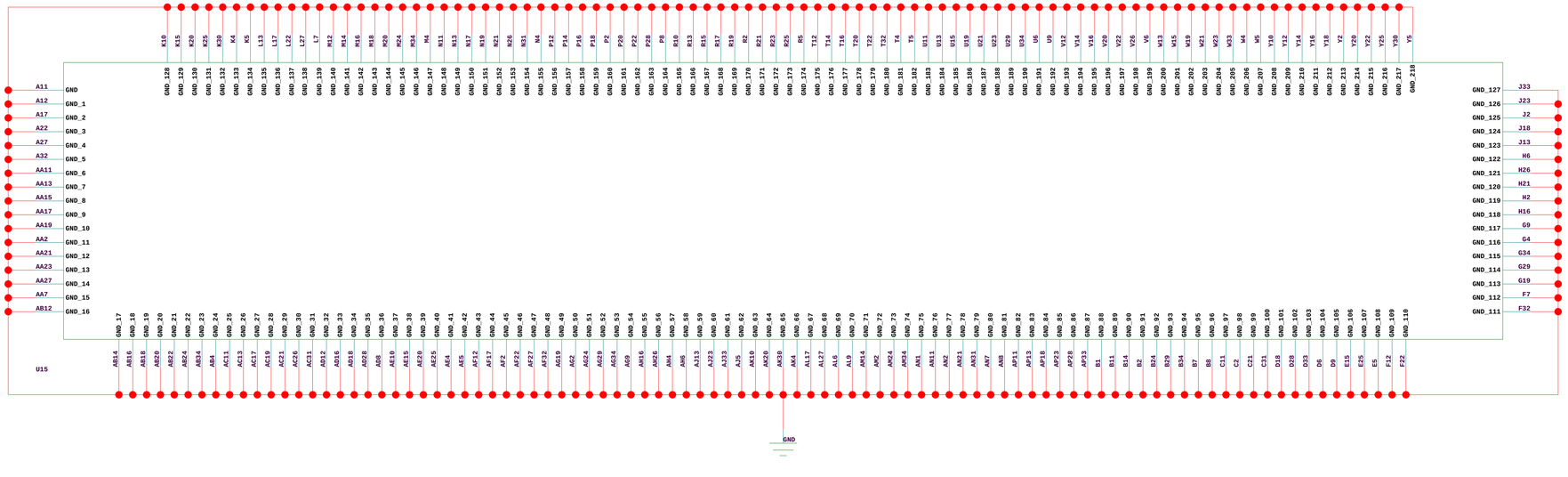




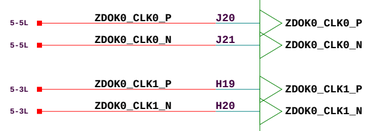


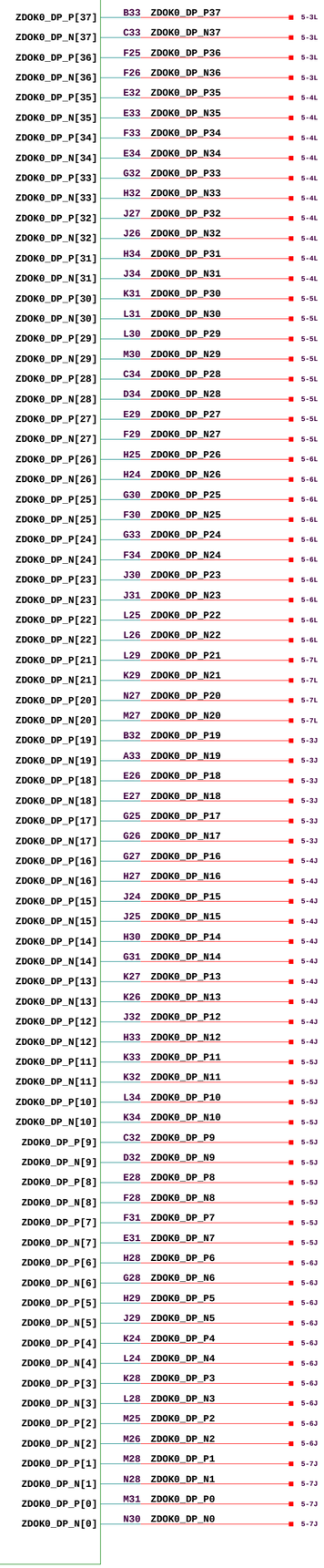


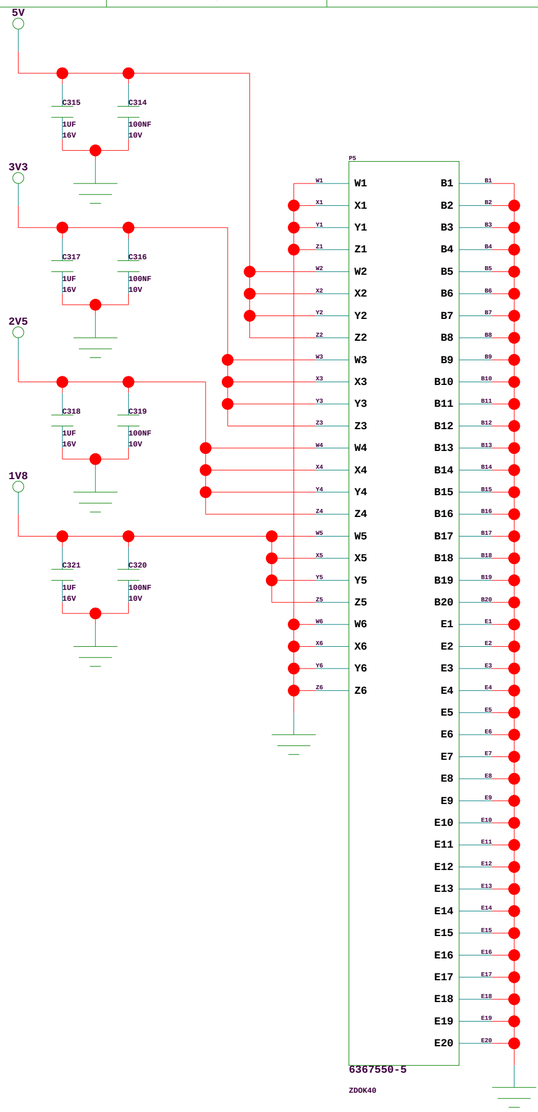


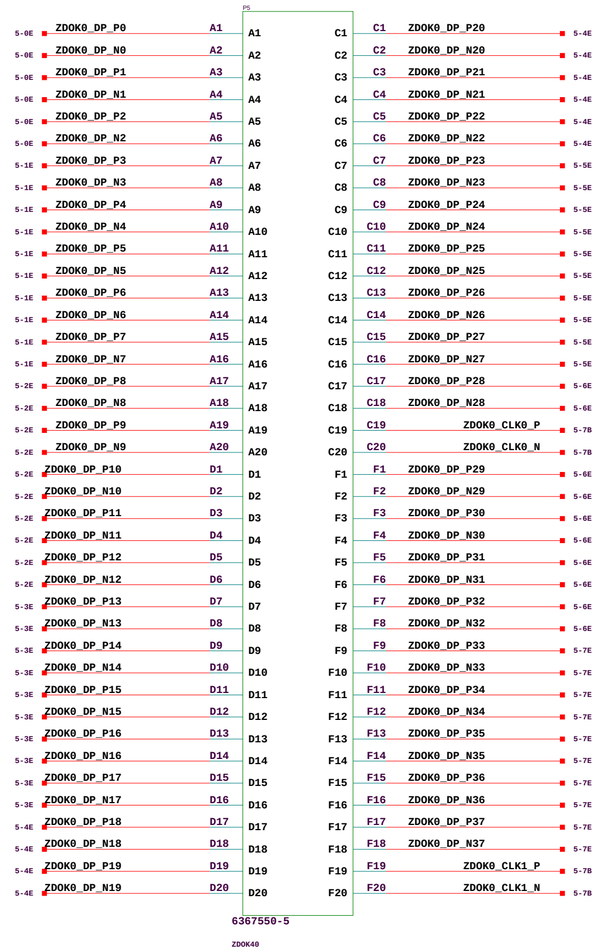


ROACH/iBOB2	ROACH_5V_POWER
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
3-20-2008_11:27 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 4 OF 25









ROACH/iBOB2	**ROACH_ADC_0**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
3-20-2008_11:27 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 5 OF 25


ZDOK1_CLK0_P H17
ZDOK1_CLK0_N H18
ZDOK1_CLK1_P K17
ZDOK1_CLK1_N L18
ZDOK1_CLK0_P
ZDOK1_CLK0_N
ZDOK1_CLK1_P
ZDOK1_CLK1_N
ZDOK1_DP_P[37] AD31 ZDOK1_DP_P37
ZDOK1_DP_N[37] AE31 ZDOK1_DP_N37
ZDOK1_DP_P[36] AF33 ZDOK1_DP_P36
ZDOK1_DP_N[36] AE33 ZDOK1_DP_N36
ZDOK1_DP_P[35] AF31 ZDOK1_DP_P35
ZDOK1_DP_N[35] AG31 ZDOK1_DP_N35
ZDOK1_DP_P[34] AG32 ZDOK1_DP_P34
ZDOK1_DP_N[34] AH32 ZDOK1_DP_N34
ZDOK1_DP_P[33] AG28 ZDOK1_DP_P33
ZDOK1_DP_N[33] AH28 ZDOK1_DP_N33
ZDOK1_DP_P[32] AF24 ZDOK1_DP_P32
ZDOK1_DP_N[32] AG25 ZDOK1_DP_N32
ZDOK1_DP_P[31] AJ30 ZDOK1_DP_P31
ZDOK1_DP_N[31] AH30 ZDOK1_DP_N31
ZDOK1_DP_P[30] AK28 ZDOK1_DP_P30
ZDOK1_DP_N[30] AK27 ZDOK1_DP_N30
ZDOK1_DP_P[29] AK26 ZDOK1_DP_P29
ZDOK1_DP_N[29] AJ27 ZDOK1_DP_N29
ZDOK1_DP_P[28] AB27 ZDOK1_DP_P28
ZDOK1_DP_N[28] AC27 ZDOK1_DP_N28
ZDOK1_DP_P[27] AD30 ZDOK1_DP_P27
ZDOK1_DP_N[27] AC29 ZDOK1_DP_N27
ZDOK1_DP_P[26] AE29 ZDOK1_DP_P26
ZDOK1_DP_N[26] AD29 ZDOK1_DP_N26
ZDOK1_DP_P[25] AG33 ZDOK1_DP_P25
ZDOK1_DP_N[25] AH33 ZDOK1_DP_N25
ZDOK1_DP_P[24] AF29 ZDOK1_DP_P24
ZDOK1_DP_N[24] AF30 ZDOK1_DP_N24
ZDOK1_DP_P[23] AG27 ZDOK1_DP_P23
ZDOK1_DP_N[23] AG26 ZDOK1_DP_N23
ZDOK1_DP_P[22] AK34 ZDOK1_DP_P22
ZDOK1_DP_N[22] AK33 ZDOK1_DP_N22
ZDOK1_DP_P[21] AL34 ZDOK1_DP_P21
ZDOK1_DP_N[21] AL33 ZDOK1_DP_N21
ZDOK1_DP_P[20] AJ25 ZDOK1_DP_P20
ZDOK1_DP_N[20] AH25 ZDOK1_DP_N20
ZDOK1_DP_P[19] AB30 ZDOK1_DP_P19
ZDOK1_DP_N[19] AC30 ZDOK1_DP_N19
ZDOK1_DP_P[18] AC28 ZDOK1_DP_P18
ZDOK1_DP_N[18] AD27 ZDOK1_DP_N18
ZDOK1_DP_P[17] AC25 ZDOK1_DP_P17
ZDOK1_DP_N[17] AC24 ZDOK1_DP_N17
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ZDOK1_DP_N[16] AF28 ZDOK1_DP_N16
ZDOK1_DP_P[15] AD24 ZDOK1_DP_P15
ZDOK1_DP_N[15] AE24 ZDOK1_DP_N15
ZDOK1_DP_P[14] AF25 ZDOK1_DP_P14
ZDOK1_DP_N[14] AF26 ZDOK1_DP_N14
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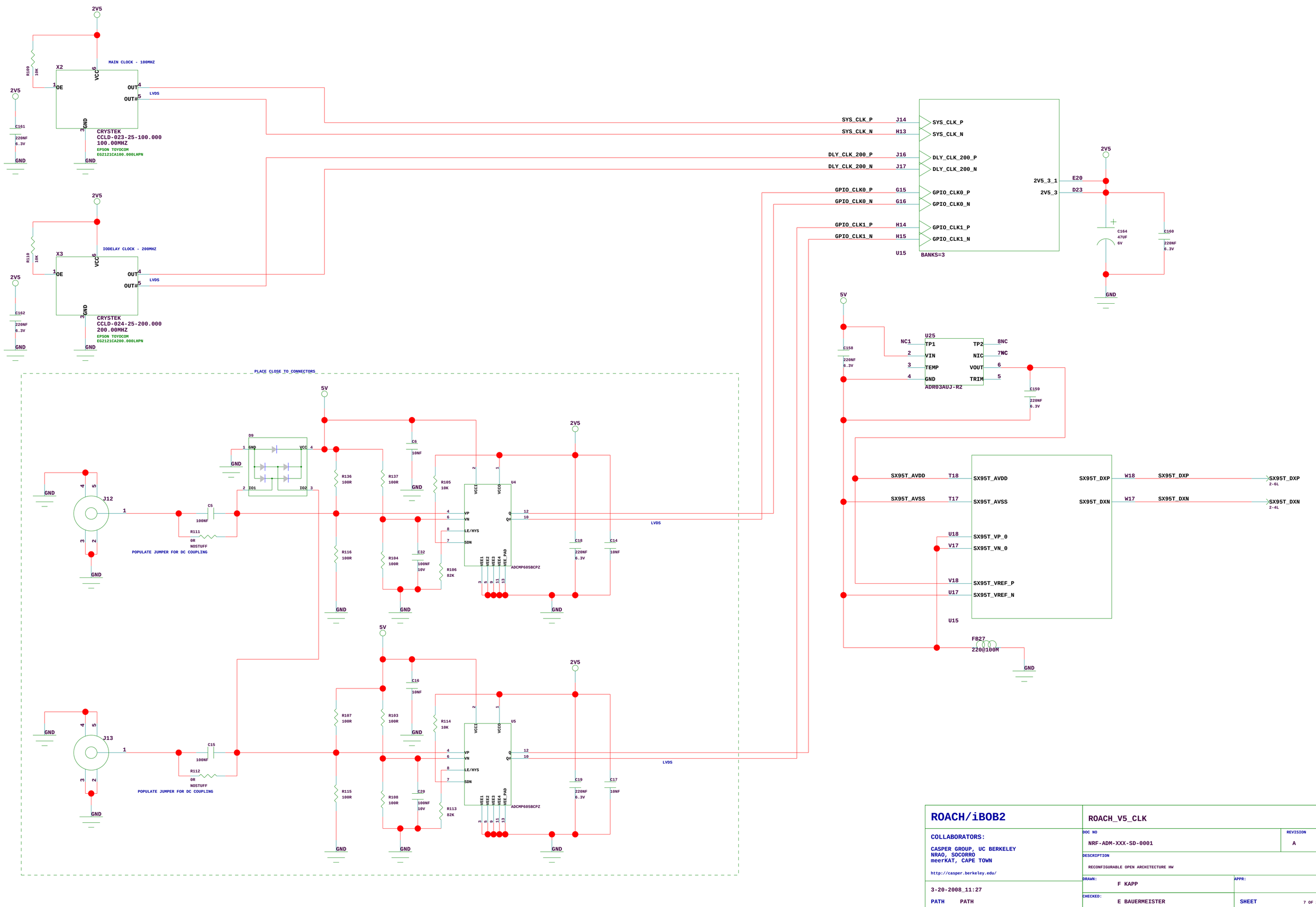
ZDOK1_DP_N[13] AG30 ZDOK1_DP_N13
ZDOK1_DP_P[12] AH27 ZDOK1_DP_P12
ZDOK1_DP_N[12] AJ26 ZDOK1_DP_N12
ZDOK1_DP_P[11] AM33 ZDOK1_DP_P11
ZDOK1_DP_N[11] AM32 ZDOK1_DP_N11
ZDOK1_DP_P[10] AN32 ZDOK1_DP_P10
ZDOK1_DP_N[10] AP32 ZDOK1_DP_N10
ZDOK1_DP_P[9] AC34 ZDOK1_DP_P9
ZDOK1_DP_N[9] AD34 ZDOK1_DP_N9
ZDOK1_DP_P[8] AD32 ZDOK1_DP_P8
ZDOK1_DP_N[8] AE32 ZDOK1_DP_N8
ZDOK1_DP_P[7] AF34 ZDOK1_DP_P7
ZDOK1_DP_N[7] AE34 ZDOK1_DP_N7
ZDOK1_DP_P[6] AD26 ZDOK1_DP_P6
ZDOK1_DP_N[6] AD25 ZDOK1_DP_N6
ZDOK1_DP_P[5] AE27 ZDOK1_DP_P5
ZDOK1_DP_N[5] AE26 ZDOK1_DP_N5
ZDOK1_DP_P[4] AH34 ZDOK1_DP_P4
ZDOK1_DP_N[4] AJ34 ZDOK1_DP_N4
ZDOK1_DP_P[3] AJ32 ZDOK1_DP_P3
ZDOK1_DP_N[3] AK32 ZDOK1_DP_N3
ZDOK1_DP_P[2] AJ31 ZDOK1_DP_P2
ZDOK1_DP_N[2] AK31 ZDOK1_DP_N2
ZDOK1_DP_P[1] AK29 ZDOK1_DP_P1
ZDOK1_DP_N[1] AJ29 ZDOK1_DP_N1
ZDOK1_DP_P[0] AN34 ZDOK1_DP_P0
ZDOK1_DP_N[0] AN33 ZDOK1_DP_N0
U15
BANKS=11, 13, 15, 17, 19, 21
5V
3V3
2V5
1V8
C337 1UF 16V
C336 100NF 10V
C339 1UF 16V
C338 100NF 10V
C340 1UF 16V
C341 100NF 10V
C343 1UF 16V
C342 100NF 10V
P7
6367550-5
ZDOK40
ZDOK1_DP_P0 A1
ZDOK1_DP_N0 A2
ZDOK1_DP_P1 A3
ZDOK1_DP_N1 A4
ZDOK1_DP_P2 A5
ZDOK1_DP_N2 A6
ZDOK1_DP_P3 A7
ZDOK1_DP_N3 A8
ZDOK1_DP_P4 A9
ZDOK1_DP_N4 A10
ZDOK1_DP_P5 A11
ZDOK1_DP_N5 A12
ZDOK1_DP_P6 A13
ZDOK1_DP_N6 A14
ZDOK1_DP_P7 A15
ZDOK1_DP_N7 A16
ZDOK1_DP_P8 A17
ZDOK1_DP_N8 A18
ZDOK1_DP_P9 A19
ZDOK1_DP_N9 A20
ZDOK1_DP_P10 D1
ZDOK1_DP_N10 D2
ZDOK1_DP_P11 D3
ZDOK1_DP_N11 D4
ZDOK1_DP_P12 D5
ZDOK1_DP_N12 D6
ZDOK1_DP_P13 D7
ZDOK1_DP_N13 D8
ZDOK1_DP_P14 D9
ZDOK1_DP_N14 D10
ZDOK1_DP_P15 D11
ZDOK1_DP_N15 D12
ZDOK1_DP_P16 D13
ZDOK1_DP_N16 D14
ZDOK1_DP_P17 D15
ZDOK1_DP_N17 D16
ZDOK1_DP_P18 D17
ZDOK1_DP_N18 D18
ZDOK1_DP_P19 D19
ZDOK1_DP_N19 D20
C1 ZDOK1_DP_P20
C2 ZDOK1_DP_N20
C3 ZDOK1_DP_P21
C4 ZDOK1_DP_N21
C5 ZDOK1_DP_P22
C6 ZDOK1_DP_N22
C7 ZDOK1_DP_P23
C8 ZDOK1_DP_N23
C9 ZDOK1_DP_P24
C10 ZDOK1_DP_N24
C11 ZDOK1_DP_P25
C12 ZDOK1_DP_N25
C13 ZDOK1_DP_P26
C14 ZDOK1_DP_N26
C15 ZDOK1_DP_P27
C16 ZDOK1_DP_N27
C17 ZDOK1_DP_P28
C18 ZDOK1_DP_N28
C19 ZDOK1_CLK0_P
C20 ZDOK1_CLK0_N
F1 ZDOK1_DP_P29
F2 ZDOK1_DP_N29
F3 ZDOK1_DP_P30
F4 ZDOK1_DP_N30
F5 ZDOK1_DP_P31
F6 ZDOK1_DP_N31
F7 ZDOK1_DP_P32
F8 ZDOK1_DP_N32
F9 ZDOK1_DP_P33
F10 ZDOK1_DP_N33
F11 ZDOK1_DP_P34
F12 ZDOK1_DP_N34
F13 ZDOK1_DP_P35
F14 ZDOK1_DP_N35
F15 ZDOK1_DP_P36
F16 ZDOK1_DP_N36
F17 ZDOK1_DP_P37
F18 ZDOK1_DP_N37
F19 ZDOK1_CLK1_P
F20 ZDOK1_CLK1_N
6367550-5
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
3-20-2008_11:27
PATH PATH
ROACH_ADC_1
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 6 OF 25



ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
3-20-2008_11:27 PATH PATH	

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB3 220@100M
FB4 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_112 AL8 MGTAVCC_126
AM8 MGTAVCC_126_1
MGTAVCCPLL_112 AM9 MGTAVCCPLL_126
MGTAVTTRX_112 AM6 MGTAVTTRX_126
MGT_REFCLK_Q3_0_P AL7 MGT_126_REF_CLK_P
MGT_REFCLK_Q3_0_N AM7 MGT_126_REF_CLK_N
MGTRX0_112_P AP6 MGTRX0_126_P
MGTRX0_112_N AP7 MGTRX0_126_N
MGTRX1_112_P AP9 MGTRX1_126_P
MGTRX1_112_N AP8 MGTRX1_126_N
U15
MGTAVTTTX_126_1 AM5 MGTAVTTTX_112
MGTAVTTTX_126 AM10
MGTTX0_126_P AN5 MGTTX0_112_P
MGTTX0_126_N AN6 MGTTX0_112_N
MGTTX1_126_P AN10 MGTTX1_112_P
MGTTX1_126_N AN9 MGTTX1_112_N
FB5 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
2V5
FB26 220@100M
X1
CCLD-023-25-156.250 156.25MHZ
OE
VCC
GND
OUT
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
U8
SY89832UMI
C68 C69 C75 C74 C73 C72 C71 C70 220NF 6.3V
MGT_REFCLK_Q1_0_P B-10D
MGT_REFCLK_Q1_0_N B-10D
MGT_REFCLK_Q1_1_P B-6D
MGT_REFCLK_Q1_1_N B-6D
MGT_REFCLK_Q1_2_P B-4D
MGT_REFCLK_Q1_2_N B-4D
MGT_REFCLK_Q1_3_P B-1D
MGT_REFCLK_Q1_3_N B-1D
C64 C65 220NF 6.3V
C66 C67 10NF 6.3V
JP6
R84 10K
3V3
OPTICAL MODULE FAULT - RED LED
R85 100R
D2
P3
FCN-268F036-G/3DB
SIG_GND1 SIG_GND2 SIG_GND3 SIG_GND4 SIG_GND5 SIG_GND6 SIG_GND7 SIG_GND8 SIG_GND9
ODIS0
FAULT0
JP4
C130 10NF
R86 10K
C131 10NF
R97 5K1
RS7 3K9
RS9 6K8
RS8 3K9
U21 MAX9032AKA
U22 SN74AHC1G08DCKR AND2
G4 AND G8 CONNECTED IN 2X2 MODULE
C127 10NF
U18 TPS2031D
R100 10K
C135 C136 C139 C91 10NF 100NF 4.7UF 16V 22UF
C129 C128 C138 C90 10NF 100NF 4.7UF 16V 22UF
R99 10K
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB11 220@100M
FB9 220@100M
FB10 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_114 AJ4 MGTAVCC_122
AK5 MGTAVCC_122_1
MGTAVCCPLL_114 AM4 MGTAVCCPLL_122
MGTAVTTRX_114 AL3 MGTAVTTRX_122
MGT_REFCLK_Q3_1_P AL5 MGT_122_REF_CLK_P
MGT_REFCLK_Q3_1_N AL4 MGT_122_REF_CLK_N
MGTRX0_114_P AL1 MGTRX0_122_P
MGTRX0_114_N AM1 MGTRX0_122_N
MGTRX1_114_P AP3 MGTRX1_122_P
MGTRX1_114_N AP2 MGTRX1_122_N
U15
MGTAVTTTX_122_1 AM3 MGTAVTTTX_114
MGTAVTTTX_122 AK3
MGTTX0_122_P AK2 MGTTX0_114_P
MGTTX0_122_N AL2 MGTTX0_114_N
MGTTX1_122_P AN4 MGTTX1_114_P
MGTTX1_122_N AN3 MGTTX1_114_N
FB8 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB17 220@100M
FB15 220@100M
FB16 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_116 AG3 MGTAVCC_118
AG4 MGTAVCC_118_1
MGTAVCCPLL_116 AH3 MGTAVCCPLL_118
MGTAVTTRX_116 AE3 MGTAVTTRX_118
MGT_REFCLK_Q3_2_P AF4 MGT_118_REF_CLK_P
MGT_REFCLK_Q3_2_N AF3 MGT_118_REF_CLK_N
MGTRX0_116_P AE1 MGTRX0_118_P
MGTRX0_116_N AF1 MGTRX0_118_N
MGTRX1_116_P AH1 MGTRX1_118_P
MGTRX1_116_N AG1 MGTRX1_118_N
U15
MGTAVTTTX_118_1 AJ3 MGTAVTTTX_116
MGTAVTTTX_118 AD3 MGTAVTTTX_116
MGTTX0_118_P AD2 MGTTX0_116_P
MGTTX0_118_N AE2 MGTTX0_116_N
MGTTX1_118_P AJ2 MGTTX1_116_P
MGTTX1_118_N AH2 MGTTX1_116_N
FB14 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB22 220@100M
FB24 220@100M
FB23 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_118 AA3 MGTAVCC_114
AA4 MGTAVCC_114_1
MGTAVCCPLL_118 AB3 MGTAVCCPLL_114
MGTAVTTRX_118 W3 MGTAVTTRX_114
MGT_REFCLK_Q3_3_P Y4 MGT_114_REF_CLK_P
MGT_REFCLK_Q3_3_N Y3 MGT_114_REF_CLK_N
MGTRX0_118_P W1 MGTRX0_114_P
MGTRX0_118_N Y1 MGTRX0_114_N
MGTRX1_118_P AB1 MGTRX1_114_P
MGTRX1_118_N AA1 MGTRX1_114_N
U15
MGTAVTTTX_114 AC3 MGTAVTTTX_114
MGTAVTTTX_114_1 V3 MGTAVTTTX_118
MGTTX0_114_P V2 MGTTX0_118_P
MGTTX0_114_N W2 MGTTX0_118_N
MGTTX1_114_P AC2 MGTTX1_118_P
MGTTX1_114_N AB2 MGTTX1_118_N
FB19 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
3-20-2008_11:27
PATH
ROACH_TRANSCEIVERS0_1
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE MK
DRAWN: F KAPP
CHECKED: E BAUERMEISTER
APPR:
SHEET 8 OF 25

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

OPTICAL MODULE FAULT - RED LED

G4 AND G8 CONNECTED IN
2X2 MODULE

CCLD-023-25-156.250
156.25MHZ

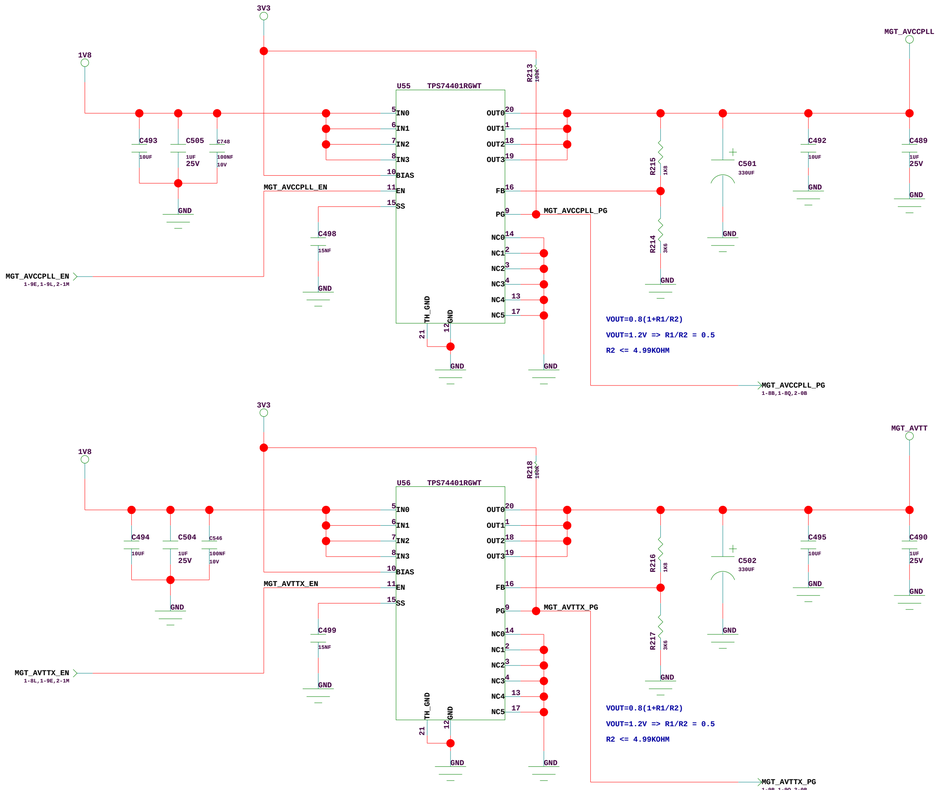
FCN-268F036-G/3DB

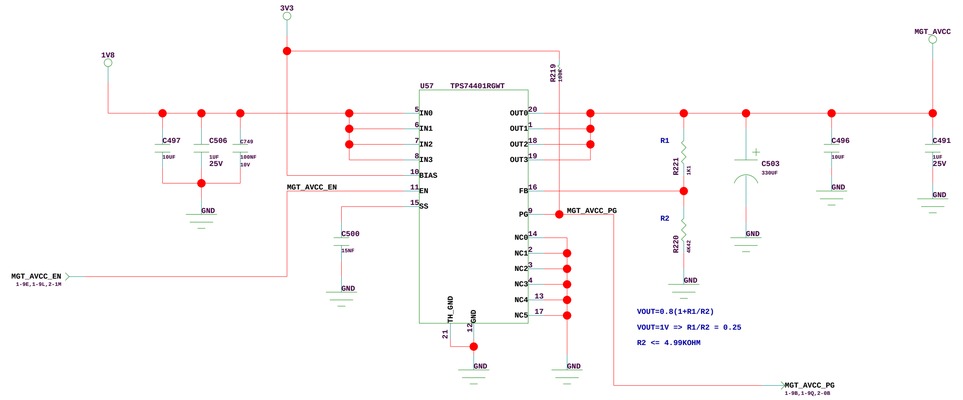
MAX9032AKA

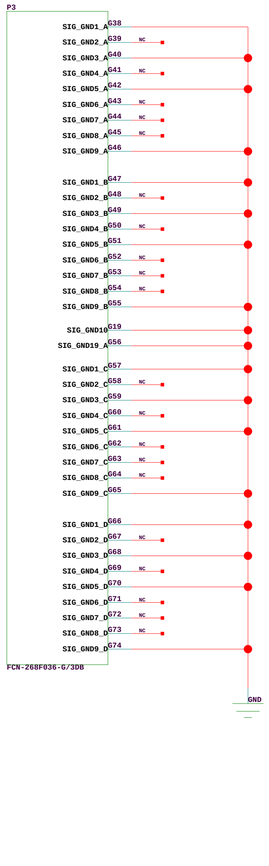
SN74AHC1G08DCKR

TPS2031D

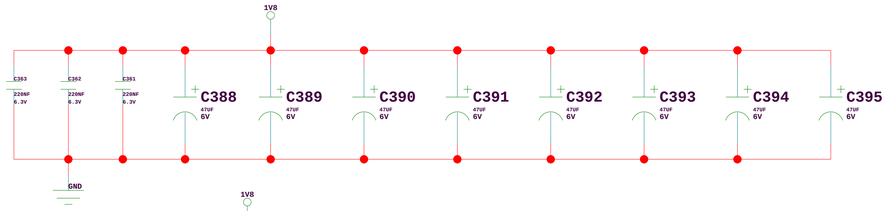
ROACH/iBOB2	**ROACH_TRANSCEIVERS2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
3-20-2008_11:27	DRAWN: F KAPP · APPR:
PATH PATH	CHECKED: E BAUERMEISTER · SHEET 9 OF 25

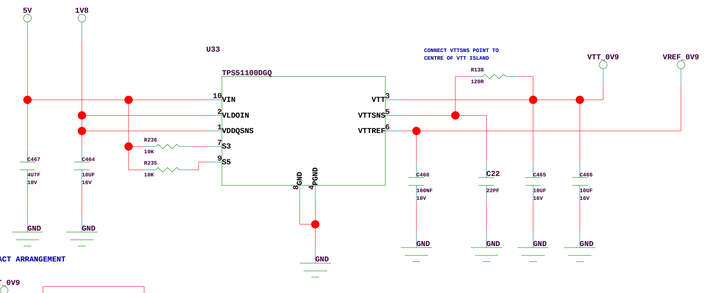




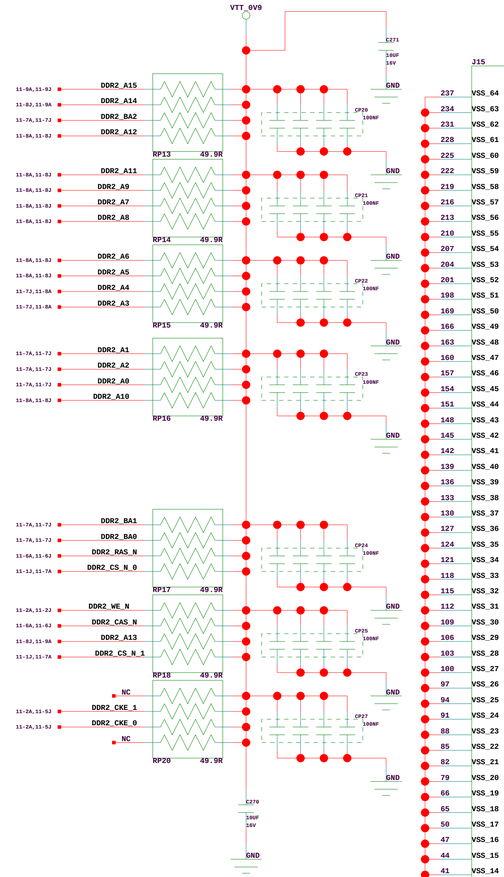


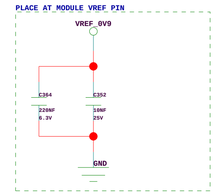
ROACH/iBOB2	ROACH_TRANSCEIVERS_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
3-20-2008_11:27	DRAWN: F KAPP · APPR:
PATH PATH	CHECKED: E BAUERMEISTER · SHEET 10 OF 25

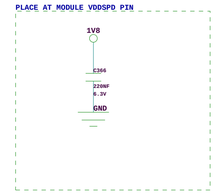


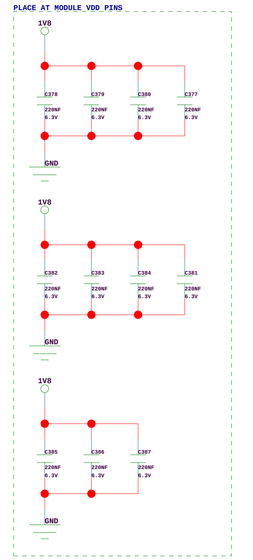


VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
PLACE ONE 10uF CAPACITOR ON EITHER END OF ISLAND

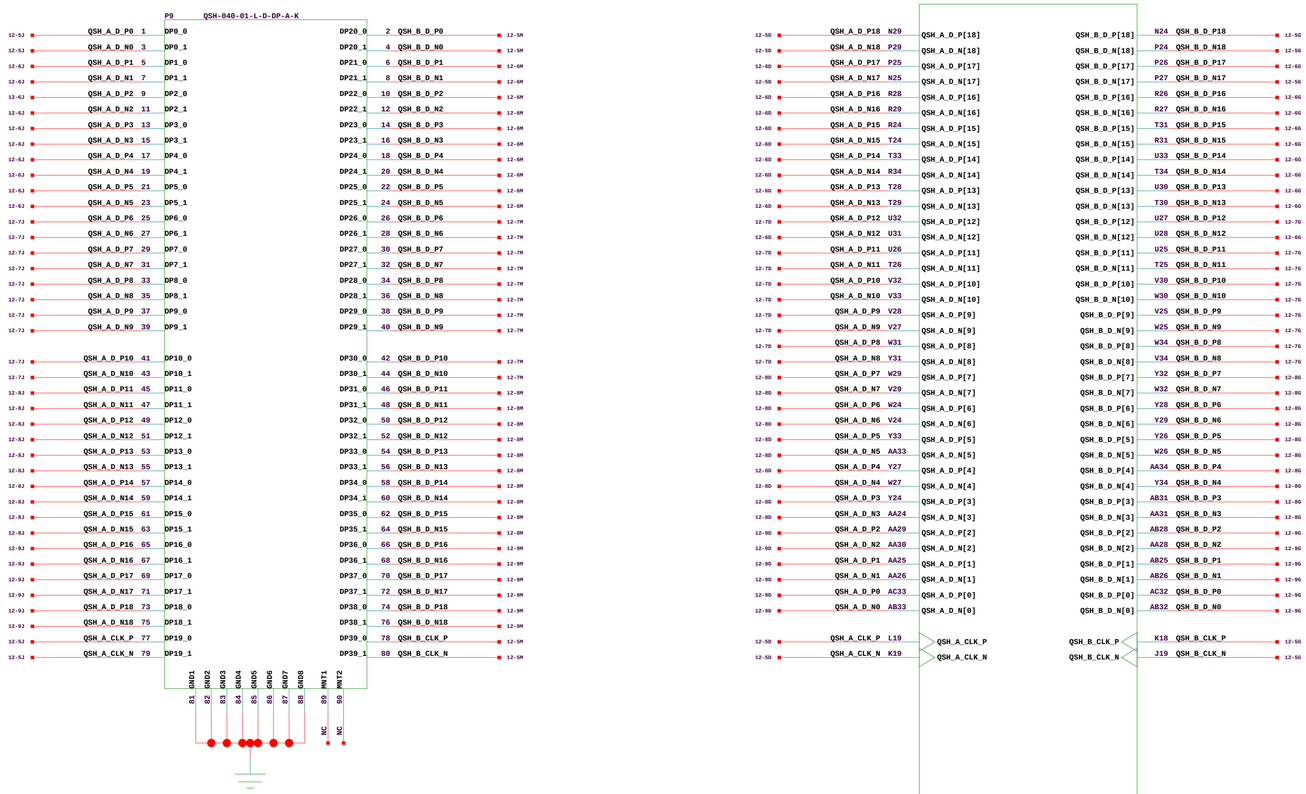








ROACH/iBOB2	ROACH_DDR2_DIMM
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE NW
3-20-2008_11:27	DRAWN: F KAPP · APPR:
PATH PATH	CHECKED: E BAUERMEISTER · SHEET 11 OF 25



ROACH/iBOB2	ROACH_DIFF_GPIO
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
3-20-2008_11:27 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 12 OF 25

GPIOLVC18[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

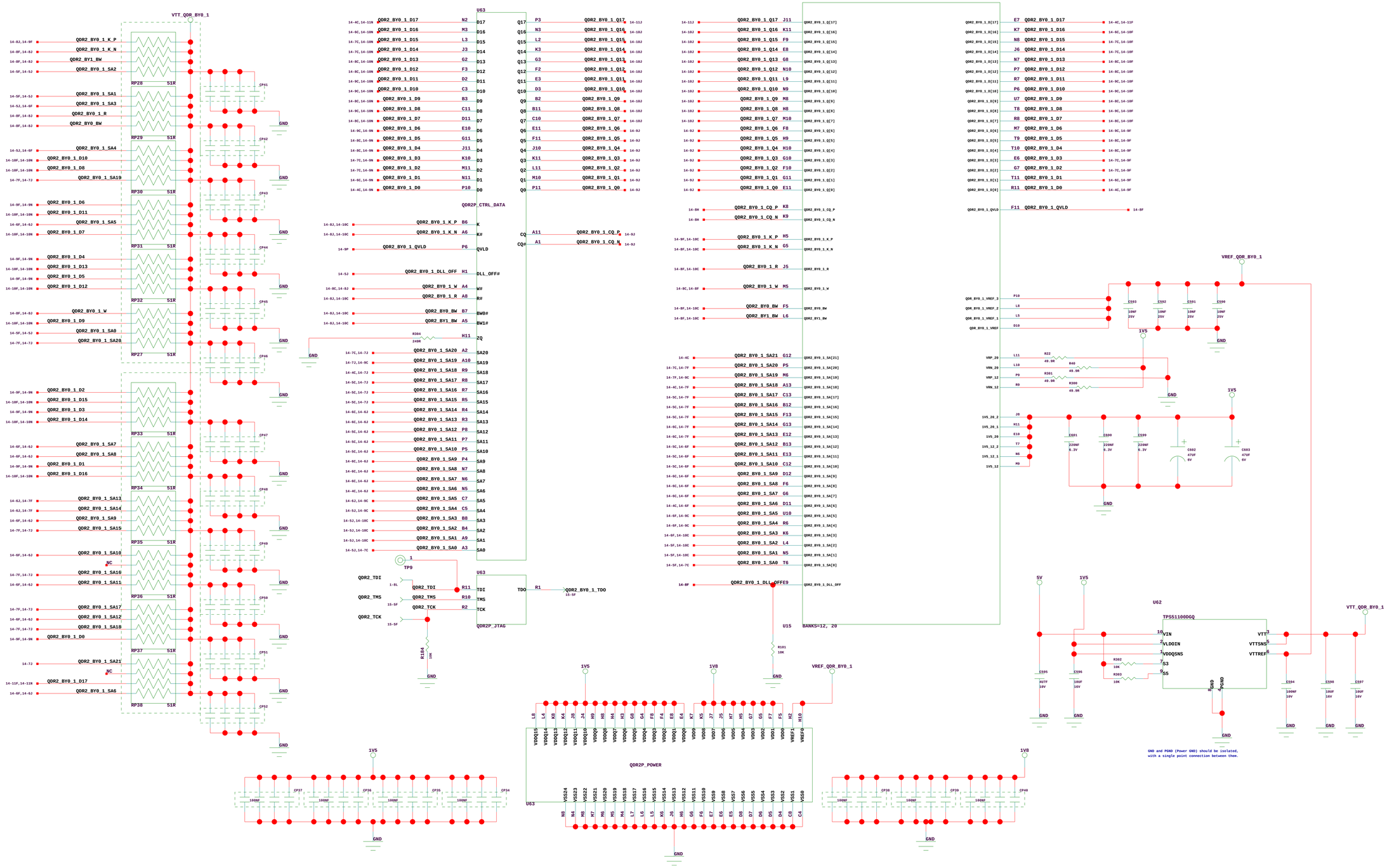
GPIOLVC25[0] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

IO VOLTAGE LEVEL SELECT

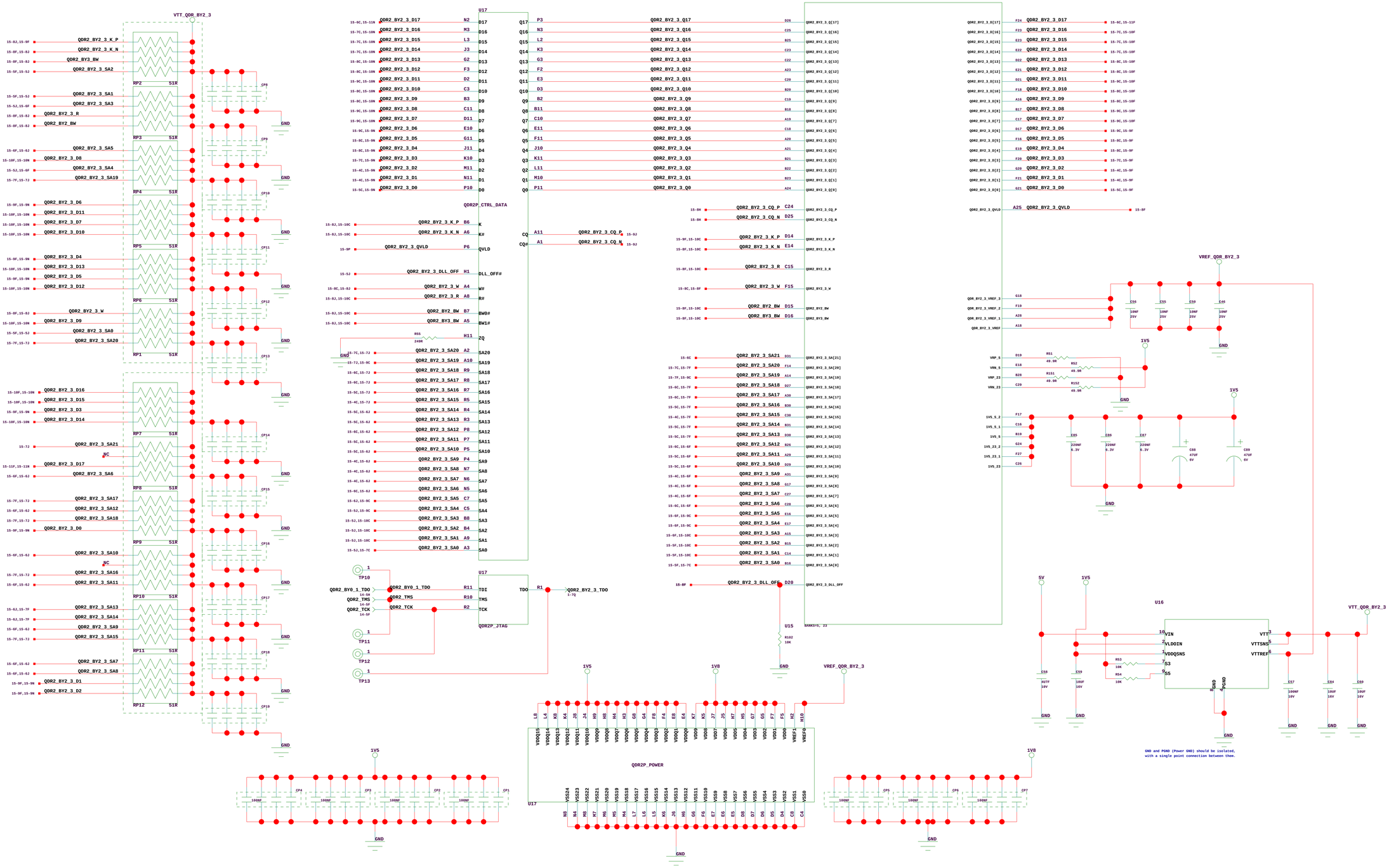
1-2: 3.3V	DEFAULT
2-3: 2.5V	

IF CR10 IS ON, CLOCK CAPABLE GPIO'S ARE OUTPUTS

ROACH/iBOB2	ROACH_GPIO_MISC
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
3-20-2008_11:27 PATH PATH	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 13 OF 25



ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
3-20-2008_11:27 PATH PATH	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
	DRAWN: F KAPP · APPR:
	CHECKED: E BAUERMEISTER · SHEET 14 OF 25

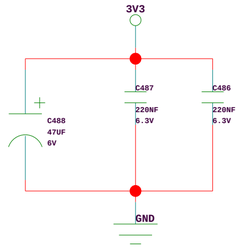


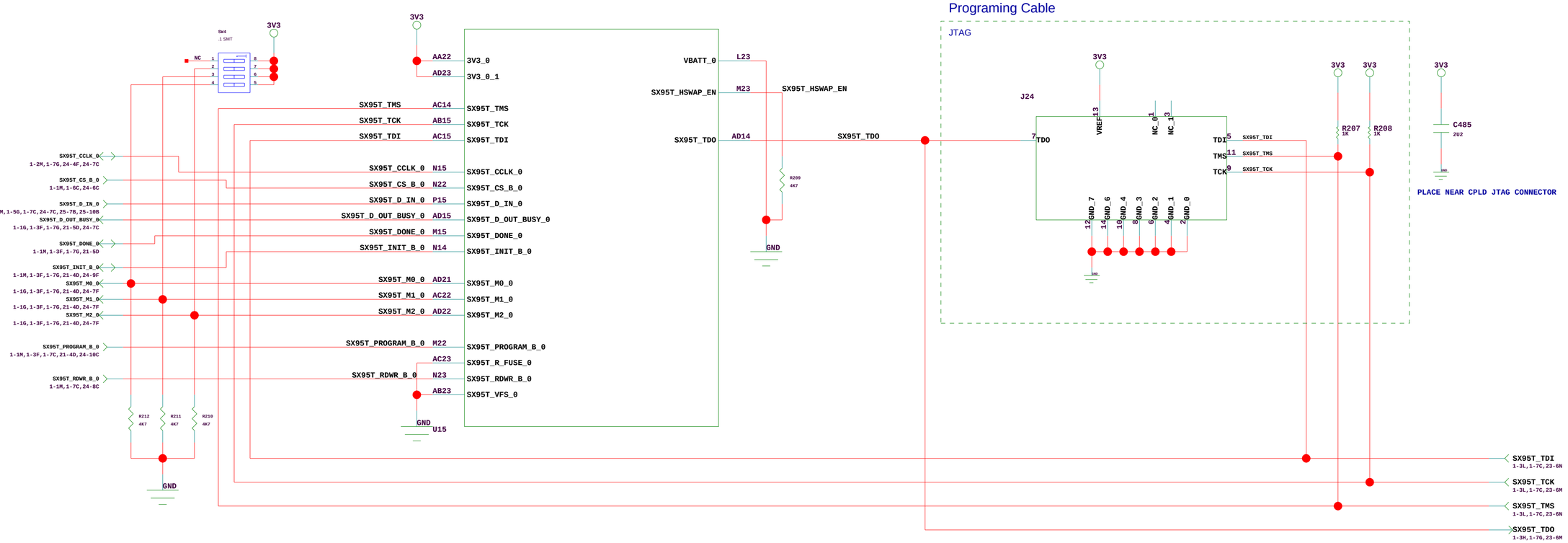
ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
3-20-2008_11:27	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 15 OF 25

TBD

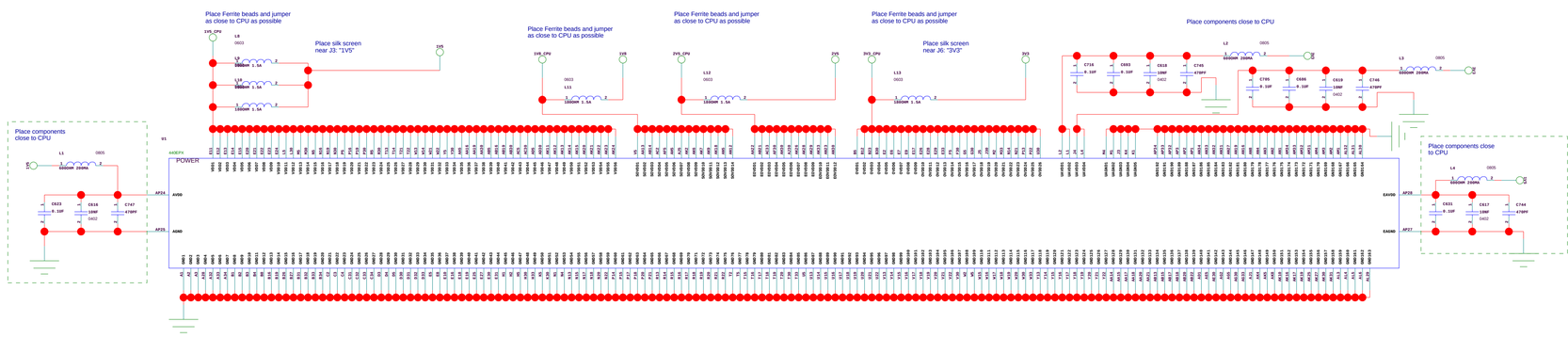
VALID CONFIGURATION MODES

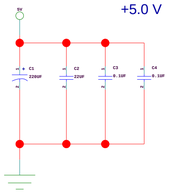
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

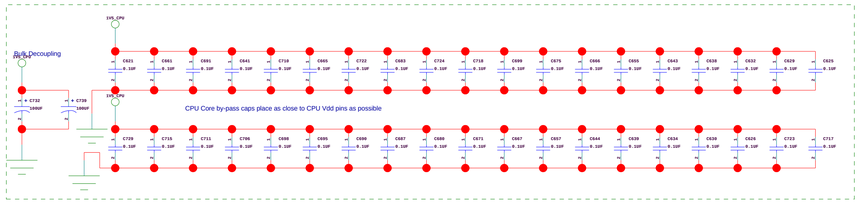


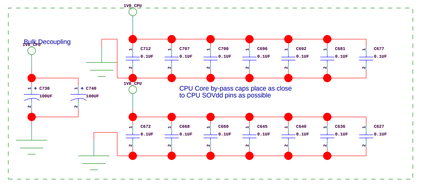


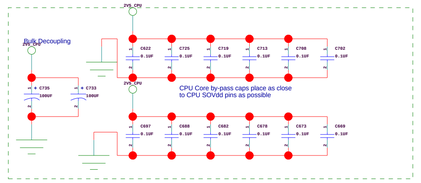
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
3-20-2008_11:27 PATH PATH	

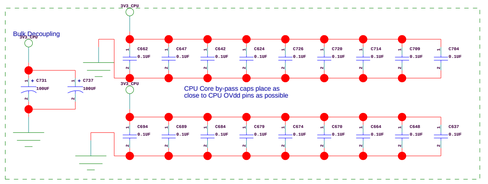


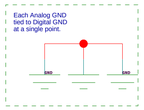










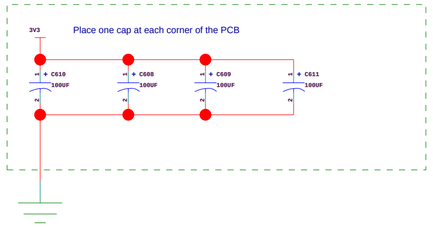


REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: **CASPER GROUP, UC BERKELEY** **NRAO, SOCORRO** **meerKAT, CAPE TOWN** http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET: 17 OF 25
3-20-2008_11:27 PATH PATH	

REMOVED 3V3 GENERATION



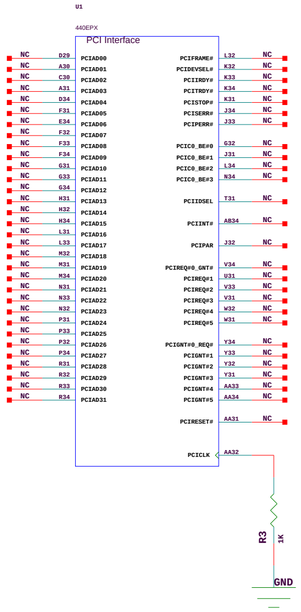
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	**ROACH_PPC_POWER_2**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 18 OF 25
3-20-2008_11:27 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
3-20-2008_11:27 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

Place nearest PHY pin 96

2V5
C533
10NF

Place nearest PHY pin 101

2V5
C534
10NF

Place nearest PHY pin 98

1V8
R233 1R
C536 22UF
C511 10NF

Place nearest PHY pin 100

1V8
R232 1R
C535 22UF
C512 10NF

Place as close to PHY CORE VDD power pins as possible

1V8
C526 10NF
C527 100NF
C525 10NF
C528 100NF
C530 10NF
C529 100NF
C531 10NF
C532 100NF

Place as close to PHY IO VDD power pins as possible

2V5
C513 10NF
C514 100NF
C515 10NF
C516 100NF
C517 10NF
C518 100NF
C519 10NF
C520 100NF
C521 10NF
C522 100NF
C523 10NF
C524 100NF

U1
440EP4
Gig-Ethernet RGMII0

U1
440EPX
Gig-Ethernet RGMII1

UNUSED SECOND ETHERNET MAC

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups. Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5

Place decoupling C as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible.

Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY

HFJ11-1G02E-L12

ETHERNET Mgt.

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

Place jumpers in line with signals

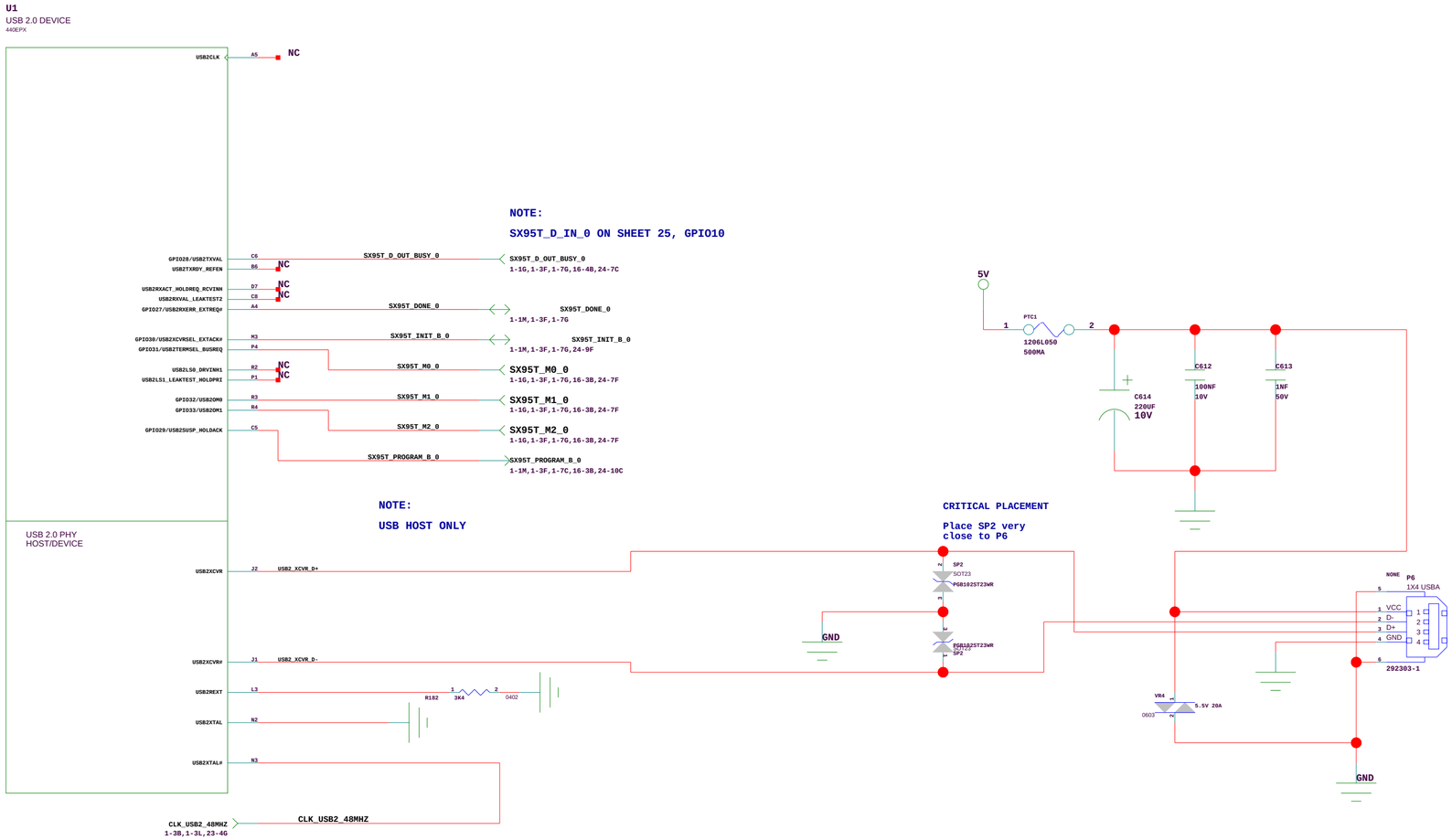
NOSTUFF

DP83865DVH

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

DUPLEX LED
L10 LED
L100 LED

ROACH/iBOB2	ROACH_PPC_ETH1
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
3-20-2008_11:27	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 20 OF 25



ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25
3-20-2008_11:27 PATH PATH	

DDR_PA[15:0]

DDR_PD[63:0]

U1

DDR SDRAM

64DEPX

DDR_PD0	A62	MEMDATA00	MEMADDR00	A95	DDR_PA0
DDR_PD1	AP22	MEMDATA01	MEMADDR01	AP4	DDR_PA1
DDR_PD2	AK59	MEMDATA02	MEMADDR02	AP5	DDR_PA2
DDR_PD3	AL28	MEMDATA03	MEMADDR03	A96	DDR_PA3
DDR_PD4	AL22	MEMDATA04	MEMADDR04	AP6	DDR_PA4
DDR_PD5	AK62	MEMDATA05	MEMADDR05	A98	DDR_PA5
DDR_PD6	AK61	MEMDATA06	MEMADDR06	AL7	DDR_PA6
DDR_PD7	AP21	MEMDATA07	MEMADDR07	AN7	DDR_PA7
DDR_PD8	AP39	MEMDATA08	MEMADDR08	AN7	DDR_PA8
DDR_PD9	AL18	MEMDATA09	MEMADDR09	AP7	DDR_PA9
DDR_PD10	AK17	MEMDATA10	MEMADDR10	AL2	DDR_PA10
DDR_PD11	AP17	MEMDATA11	MEMADDR11	AL8	DDR_PA11
DDR_PD12	AN20	MEMDATA12	MEMADDR12	AP8	DDR_PA12
DDR_PD13	AP18	MEMDATA13	MEMADDR13	AN4	DDR_PA13
DDR_PD14	AK18	MEMDATA14			
DDR_PD15	AP16	MEMDATA15	BA0	A23	DDR_PBA0
DDR_PD16	AM18	MEMDATA16	BA1	A93	DDR_PBA1
DDR_PD17	AP19	MEMDATA17	BA2	AP9	DDR_PBA2
DDR_PD18	AL15	MEMDATA18			
DDR_PD19	AP14	MEMDATA19	RAS#	A24	DDR_PRAS#
DDR_PD20	AL17	MEMDATA20	CAS#	A94	DDR_PCAS#
DDR_PD21	AM17	MEMDATA21	WE#	A22	DDR_PWE#
DDR_PD22	AK15	MEMDATA22			
DDR_PD23	AM15	MEMDATA23	DM0	AL21	DDR_PDM0
DDR_PD24	AP13	MEMDATA24	DM1	AP18	DDR_PDM1
DDR_PD25	AK13	MEMDATA25	DM2	AP15	DDR_PDM2
DDR_PD26	AP12	MEMDATA26	DM3	AL14	DDR_PDM3
DDR_PD27	AL12	MEMDATA27	DM4	A04	DDR_PDM4
DDR_PD28	AM14	MEMDATA28	DM5	A03	DDR_PDM5
DDR_PD29	AK14	MEMDATA29	DM6	Y3	DDR_PDM6
DDR_PD30	AL13	MEMDATA30	DM7	U3	DDR_PDM7
DDR_PD31	AM12	MEMDATA31	DM8	AN18	DDR_PDM8
DDR_PD32	AF3	MEMDATA32			
DDR_PD33	AF1	MEMDATA33	DQS0	AM21	DDR_PDQS0
DDR_PD34	AD4	MEMDATA34	DQS1	AM19	DDR_PDQS1
DDR_PD35	AD3	MEMDATA35	DQS2	AL16	DDR_PDQS2
DDR_PD36	AB3	MEMDATA36	DQS3	AM13	DDR_PDQS3
DDR_PD37	AF2	MEMDATA37	DQS4	A02	DDR_PDQS4
DDR_PD38	AE2	MEMDATA38	DQS5	A04	DDR_PDQS5
DDR_PD39	AE1	MEMDATA39	DQS6	W3	DDR_PDQS6
DDR_PD40	AC3	MEMDATA40	DQS7	Y4	DDR_PDQS7
DDR_PD41	AC1	MEMDATA41	DQS8	AP10	DDR_PDQS8
DDR_PD42	AA4	MEMDATA42			
DDR_PD43	AA3	MEMDATA43	MEMODT0	A03	DDR_PODT0
DDR_PD44	AD2	MEMDATA44	MEMODT1	A01	DDR_PODT1
DDR_PD45	AC4	MEMDATA45			
DDR_PD46	AB1	MEMDATA46	BANKSEL#0	AN2	DDR_PCS0#
DDR_PD47	AB2	MEMDATA47	BANKSEL#1	A91	DDR_PCS1#
DDR_PD48	Y3	MEMDATA48			
DDR_PD49	Y2	MEMDATA49	MEMCLKEN	AN9	DDR_PCKE
DDR_PD50	Y4	MEMDATA50			
DDR_PD51	V3	MEMDATA51	MEMCLKOUT	AL1	DDR_CLKOUT
DDR_PD52	AA2	MEMDATA52			
DDR_PD53	AA1	MEMDATA53	MEMCLKOUT#	AM1	DDR_CLKOUT#
DDR_PD54	W3	MEMDATA54			
DDR_PD55	W1	MEMDATA55			
DDR_PD56	V1	MEMDATA56			
DDR_PD57	U2	MEMDATA57			
DDR_PD58	T4	MEMDATA58			
DDR_PD59	R1	MEMDATA59			
DDR_PD60	V3	MEMDATA60			
DDR_PD61	T1	MEMDATA61			
DDR_PD62	T3	MEMDATA62			
DDR_PD63	T2	MEMDATA63			

ECC0	AM11	PPC_ECC0	22-9F
ECC1	AL11	PPC_ECC1	22-9F
ECC2	AN9	PPC_ECC2	22-9F
ECC3	AL9	PPC_ECC3	22-10F
ECC4	AM11	PPC_ECC4	22-10F
ECC5	AN11	PPC_ECC5	22-10F
ECC6	AM10	PPC_ECC6	22-10F
ECC7	AP9	PPC_ECC7	22-10F

DDR2 Clock line must be 500ps longer than Address/Command lines
To compensate for additional loading when using unbuffered DIMM's
See P84 of PPC440EPx for more information

Place parts
as close to
CPU as possible

DDR_VREF_0V9

1V8

5V

GND

U32

TPS51100DGQ

DDR_VTT

R6 120R

R230 10K

R229 10K

C459 4U7F 10V

C456 10UF 16V

C453 100NF 10V

C21 22PF

C457 10UF 16V

C458 10UF 16V

J8

DDR_PDQ63	236	DDR2_DIMM_DQ[63]	
DDR_PDQ62	235	DDR2_DIMM_DQ[62]	
DDR_PDQ61	230	DDR2_DIMM_DQ[61]	
DDR_PDQ60	229	DDR2_DIMM_DQ[60]	
DDR_PDQ59	117	DDR2_DIMM_DQ[59]	
DDR_PDQ58	116	DDR2_DIMM_DQ[58]	
DDR_PDQ57	111	DDR2_DIMM_DQ[57]	
DDR_PDQ56	110	DDR2_DIMM_DQ[56]	
DDR_PDQ55	227	DDR2_DIMM_DQ[55]	
DDR_PDQ54	226	DDR2_DIMM_DQ[54]	
DDR_PDQ53	218	DDR2_DIMM_DQ[53]	
DDR_PDQ52	217	DDR2_DIMM_DQ[52]	
DDR_PDQ51	108	DDR2_DIMM_DQ[51]	
DDR_PDQ50	107	DDR2_DIMM_DQ[50]	
DDR_PDQ49	99	DDR2_DIMM_DQ[49]	
DDR_PDQ48	98	DDR2_DIMM_DQ[48]	
DDR_PDQ47	215	DDR2_DIMM_DQ[47]	
DDR_PDQ46	214	DDR2_DIMM_DQ[46]	
DDR_PDQ45	209	DDR2_DIMM_DQ[45]	
DDR_PDQ44	208	DDR2_DIMM_DQ[44]	
DDR_PDQ43	96	DDR2_DIMM_DQ[43]	
DDR_PDQ42	95	DDR2_DIMM_DQ[42]	
DDR_PDQ41	90	DDR2_DIMM_DQ[41]	
DDR_PDQ40	89	DDR2_DIMM_DQ[40]	
DDR_PDQ39	206	DDR2_DIMM_DQ[39]	
DDR_PDQ38	205	DDR2_DIMM_DQ[38]	
DDR_PDQ37	200	DDR2_DIMM_DQ[37]	
DDR_PDQ36	199	DDR2_DIMM_DQ[36]	
DDR_PDQ35	87	DDR2_DIMM_DQ[35]	
DDR_PDQ34	86	DDR2_DIMM_DQ[34]	
DDR_PDQ33	81	DDR2_DIMM_DQ[33]	
DDR_PDQ32	80	DDR2_DIMM_DQ[32]	
DDR_PDQ31	159	DDR2_DIMM_DQ[31]	
DDR_PDQ30	158	DDR2_DIMM_DQ[30]	
DDR_PDQ29	153	DDR2_DIMM_DQ[29]	
DDR_PDQ28	152	DDR2_DIMM_DQ[28]	
DDR_PDQ27	40	DDR2_DIMM_DQ[27]	
DDR_PDQ26	39	DDR2_DIMM_DQ[26]	
DDR_PDQ25	34	DDR2_DIMM_DQ[25]	
DDR_PDQ24	33	DDR2_DIMM_DQ[24]	
DDR_PDQ23	150	DDR2_DIMM_DQ[23]	
DDR_PDQ22	149	DDR2_DIMM_DQ[22]	
DDR_PDQ21	144	DDR2_DIMM_DQ[21]	
DDR_PDQ20	143	DDR2_DIMM_DQ[20]	
DDR_PDQ19	31	DDR2_DIMM_DQ[19]	
DDR_PDQ18	30	DDR2_DIMM_DQ[18]	
DDR_PDQ17	25	DDR2_DIMM_DQ[17]	
DDR_PDQ16	24	DDR2_DIMM_DQ[16]	
DDR_PDQ15	141	DDR2_DIMM_DQ[15]	
DDR_PDQ14	140	DDR2_DIMM_DQ[14]	
DDR_PDQ13	132	DDR2_DIMM_DQ[13]	
DDR_PDQ12	131	DDR2_DIMM_DQ[12]	
DDR_PDQ11	22	DDR2_DIMM_DQ[11]	
DDR_PDQ10	21	DDR2_DIMM_DQ[10]	
DDR_PDQ9	13	DDR2_DIMM_DQ[9]	
DDR_PDQ8	12	DDR2_DIMM_DQ[8]	
DDR_PDQ7	129	DDR2_DIMM_DQ[7]	
DDR_PDQ6	128	DDR2_DIMM_DQ[6]	
DDR_PDQ5	123	DDR2_DIMM_DQ[5]	
DDR_PDQ4	122	DDR2_DIMM_DQ[4]	
DDR_PDQ3	10	DDR2_DIMM_DQ[3]	
DDR_PDQ2	9	DDR2_DIMM_DQ[2]	
DDR_PDQ1	4	DDR2_DIMM_DQ[1]	
DDR_PDQ0	3	DDR2_DIMM_DQ[0]	

PPC_ECC7	168	DDR2_DIMM_CB7	
PPC_ECC6	167	DDR2_DIMM_CB6	
PPC_ECC5	162	DDR2_DIMM_CB5	
PPC_ECC4	161	DDR2_DIMM_CB4	
PPC_ECC3	49	DDR2_DIMM_CB3	
PPC_ECC2	48	DDR2_DIMM_CB2	
PPC_ECC1	43	DDR2_DIMM_CB1	
PPC_ECC0	42	DDR2_DIMM_CB0	
	101	DDR2_DIMM_SA2	
	240	DDR2_DIMM_SA1	
	239	DDR2_DIMM_SA0	
PPC_DDR2_DIMM_SCL	120	DDR2_DIMM_SCL	
PPC_DDR2_DIMM_SDA	119	DDR2_DIMM_SDA	

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R228 4K7

R227 4K7

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA1	22-9D,22-10L
DDR2_DIMM_BA[1]	190	DDR_PBA2	22-9L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-7L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	NC	
DDR2_DIMM_CK_N[2]	221	NC	
DDR2_DIMM_CK_P[1]	137	NC	
DDR2_DIMM_CK_N[1]	138	NC	
DDR2_DIMM_CK_P[0]	185	DDR_CLKOUT	
DDR2_DIMM_CK_N[0]	186	DDR_CLKOUT#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-8D,22-11L
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-8D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D
PAR_OUT	55	PPC_DDR2_ERROR	1
PAR_IN	68	PAR_IN	TP4
			1
			TP5

R226 4K7

PPC_DDR2_RESET_N

1-2R,1-2M,24-10F

C455 5PF 50V

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

DDR_VTT

22-6K,22-8D	DDR_PCKE	
	DDR_PA15	
	DDR_PA14	
22-8K,22-9D	DDR_PBA1	
	DDR_PA12	
	DDR_PA11	
	DDR_PA9	
	NC	
	DDR_PA7	
	DDR_PA8	
	DDR_PA6	
	DDR_PA5	
	DDR_PA4	
	DDR_PA3	
	DDR_PA1	
	DDR_PA2	
22-8K,22-9D	DDR_PA0	
22-8K,22-9D	DDR_PBA2	
22-8K,22-9D	DDR_PA10	
22-8K,22-9D	DDR_PBA0	
22-7K,22-9D	DDR_PRAS#	
22-3K,22-9D	DDR_PWE#	
22-3K,22-9D	DDR_PCS0#	
22-8K,22-9D	DDR_PCAS#	
22-3K,22-9D	DDR_PCS1#	
22-9D	DDR_PODT0	
	DDR_PA13	
22-8D	DDR_PODT1	

RP24 RP23 RP22 RP21 RP25 RP26 RP19

CP26 CP28 CP29 CP30 CP32 CP31 CP33

GND

J8

	237	VSS_64	
	234	VSS_63	
	231	VSS_62	
	228	VSS_61	
	225	VSS_60	
	222	VSS_59	
	219	VSS_58	
	216	VSS_57	
	213	VSS_56	
	210	VSS_55	
	207	VSS_54	
	204	VSS_53	
	201	VSS_52	
	198	VSS_51	
	169	VSS_50	
	166	VSS_49	
	163	VSS_48	
	160	VSS_47	
	157	VSS_46	
	154	VSS_45	
	151	VSS_44	
	148	VSS_43	
	145	VSS_42	
	142	VSS_41	
	139	VSS_40	
	136	VSS_39	
	133	VSS_38	
	130	VSS_37	
	127	VSS_36	
	124	VSS_35	
	121	VSS_34	
	118	VSS_33	
	115	VSS_32	
	112	VSS_31	
	109	VSS_30	
	106	VSS_29	
	103	VSS_28	
	100	VSS_27	
	97	VSS_26	
	94	VSS_25	
	91	VSS_24	
	88	VSS_23	
	85	VSS_22	
	82	VSS_21	
	79	VSS_20	
	66	VSS_19	
	65	VSS_18	
	50	VSS_17	
	47	VSS_16	
	44	VSS_15	
	41	VSS_14	
	38	VSS_13	
	35	VSS_12	
	32	VSS_11	
	29	VSS_10	
	26	VSS_9	
	23	VSS_8	
	20	VSS_7	
	17	VSS_6	
	14	VSS_5	
	11	VSS_4	
	8	VSS_3	
	5	VSS_2	
	2	VSS_1	

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DDR_VREF_0V9

VREF 1

1V8

VDDSPD 238

VDD_11	197	1V8
VDD_10	189	
VDD_9	187	
VDD_8	184	
VDD_7	178	
VDD_6	172	
VDD_5	69	
VDD_4	67	
VDD_3	64	
VDD_2	59	
VDD_1	53	
VDDQ_11	194	1V8
VDDQ_10	191	
VDDQ_9	181	
VDDQ_8	175	
VDDQ_7	170	
VDDQ_6	78	
VDDQ_5	75	
VDDQ_4	72	
VDDQ_3	62	
VDDQ_2	56	
VDDQ_1	51	

DDR_VREF_0V9

1V8

C432 100NF 10V
C433 10NF 25V
C454 100NF 10V
C434 10NF 25V
C430 100NF 10V
C443 10NF 25V
C431 100NF 10V
C444 10NF 25V
C436 100NF 10V
C445 10NF 25V
C435 100NF 10V
C446 10NF 25V
C438 100NF 10V
C451 10NF 25V
C437 100NF 10V
C452 10NF 25V
C439 100NF 10V
C449 10NF 25V
C440 100NF 10V
C450 10NF 25V
C441 100NF 10V
C448 10NF 25V
C442 100NF 10V
C447 10NF 25V

GND

PLACE NEAREST DDR2 MODULE PINS

ROACH/iBOB2		ROACH_PPC_DDR2	
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/		DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
		DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
3-20-2008_11:27		DRAWN: F KAPP	APPR:
PATH PATH		CHECKED: E BAUERMEISTER	SHEET 22 OF 25

PWR_GOOD
1-2G,1-3H,24-8R

3V3

PWR_GOOD monitors the +1.0v, 1V5, 1V8, 2V5, and 3V3 supplies

U31
SOT-23-5
MIC2779A-29

RESET_PORH
1-2D,1-3L,1-5G,24-9M,25-5G

RESET_PB_POR#
1-2M,1-3H,24-7F

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_3V3_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz

U9
SOIC-8
CY22381FX_8211

SEL_SYSCLK
1-1M,1-3H,24-10F

CLK_UART_11_0592MHZ
1-1L,1-5G,25-3D

CLK_SYS_33MHZ

CLK_CPLD_33MHZ
1-1G,1-2L,24-8C

U1
440EPX
PPC440EPX-NTA533T

SYSTEM
INTERRUPTS

CLK_TMRCLK
1-1M,1-3H,24-10C

SYSERR
1-1G,1-3L,24-10C

PPC_THERMONA
1-3L,1-9E,2-6L

PPC_THERMONB
1-3L,1-9E,2-4L

IRQ0-9 have programmable polarity per section 10.5.7 (UIC0_PR) 440ep user manual

MONITOR_INT
1-3H,1-9E,2-1P

VS_INT#
1-3H,1-5L,25-8Q

STTM_ALERT
1-3H,1-5L,25-2B

GPIO44
1-3L

SX95T_TDI
1-3L,1-7C,16-2L

SX95T_TCK
1-3L,1-7C,16-2L

SX95T_TMS
1-3L,1-7C,16-2L

SX95T_TDO
1-3H,1-7G,16-2L

NO POP
RO1 - RO5

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible

U24
CY22392FXA_8211

CLK_SEL_M66EN
1-1M,1-3H,24-10F

CLK_GETH0_25MHZ
1-3L,1-4B,20-4E

CLK_USB2_48MHZ
1-3B,1-3L,21-8D

CLK_CPLD_50MHZ
1-1G,1-3L,24-7C

TRACE & JTAG CONNECTORS

Critical placement and routing of the Trace connector and nets. Up to CPU frequency/4

U1
440EPX
RiscWatch JTAG

CPU_TDO
CPU_TDI
CPU_TCK
CPU_TMS
CPU_HALT#

DEBUG_TRST#
1-1G,1-3L,24-9C

R26 is for current limiting and should be <100 Ohms.

TRACE PORT

J1
25PH F SMT

TMC_CLK
VCC_JTAG

CPU_TRST#
1-2M,1-3H,24-9C

ROACH/iBOB2	ROACH_PPC_TST_CLK_IO
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
3-20-2008_11:27	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 23 OF 25

SD/MMC/MMCPLUS CONNECTOR

J17

SDSR13-A0-0005

RESETS

CPU_TRST# = '1' when JTAG_TRST# = '1' and RESET_PORW = '1' else '0'; see errata sheet

Boot Configuration

SysErr will be used to drive Status LED (active H)

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

roach_cpld_XC2C256_7VQ100C_pcb

U54 XC2C256_7VQ144C

roach_cpld_XC2C256_7VQ100C_configpins

U54 XC2C256_7VQ144C

Xilinx Programing Cable

JTAG

ENABLE PER_CLK CONNECTION TO CONFIGURATION I/F MUST CO-ORDINATE WITH SX95T_CCLK_0 AND MODE TO AVOID CLASH

SN74AHC1G125DCKT

PLACE AT END OF DAISY CHAIN

roach_cpld_XC2C256_7VQ100C_powerpins

PLACE NEAR CPLD POWER PINS

PLACE NEAR CPLD JTAG CONNECTOR

ROACH/iBOB2	**ROACH_PPC_CPLD**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
3-20-2008_11:27; PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 24 OF 25

ROACH/iBOB2	ROACH_PPC_NVM_SERIAL
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
3-20-2008_11:27 PATH PATH	DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET 25 OF 25