

**KAROO ARRAY TELESCOPE, NRF**

UNIT 12, LONSDALE BUILDING  
LONSDALE WAY, PINELANDS, 7405  
SOUTH AFRICA

TITLE

**ROACH\_TOP**

SIZE

**A2**

DWG NO

NRF-ADM-XXX-SD-0001

REV

**A**

CHECKED BY

<PUT NAME HERE>

DRAWN BY

FRANCOIS KAPP

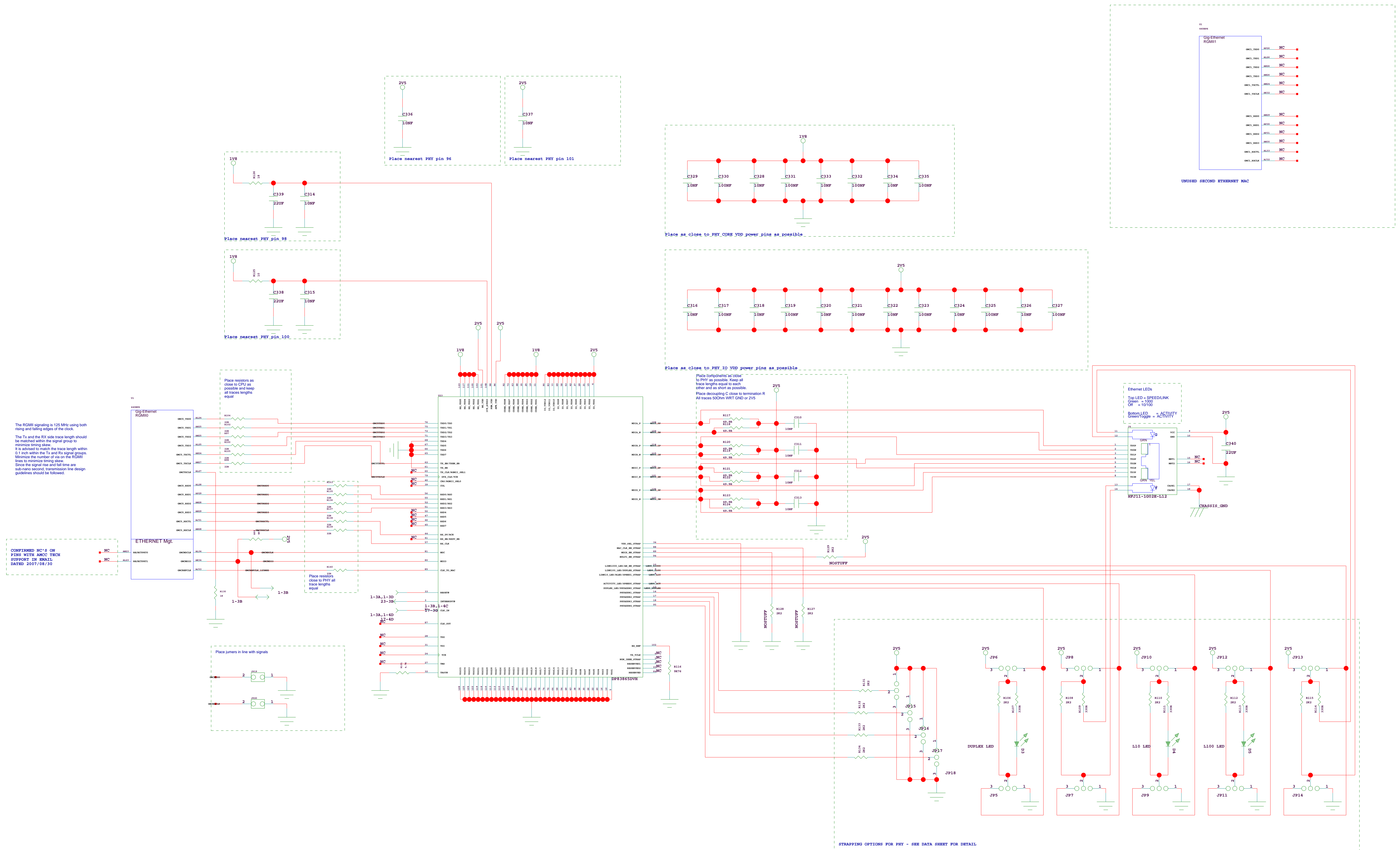
SCALE

NTS

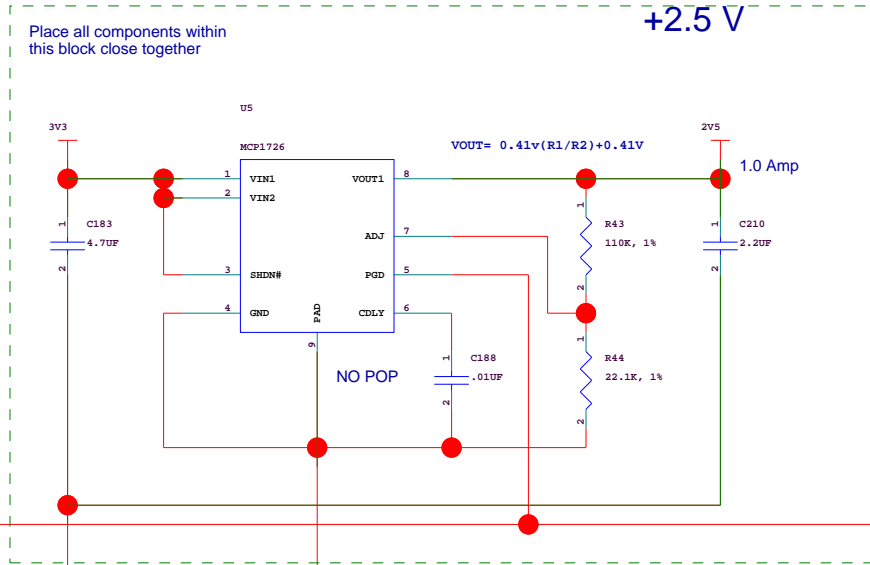
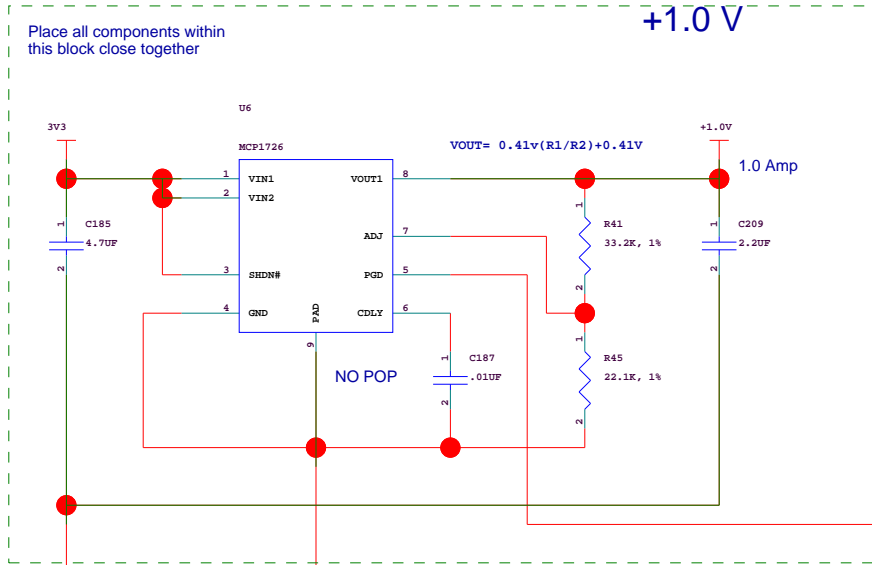
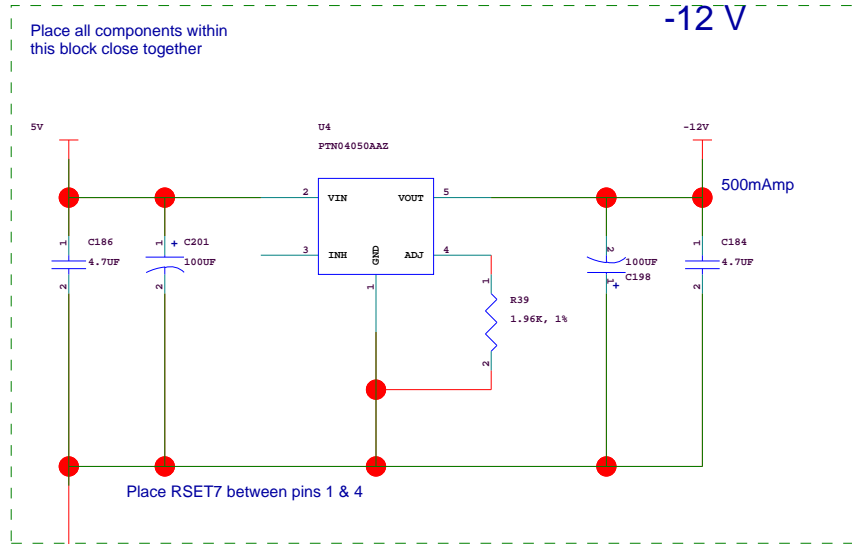
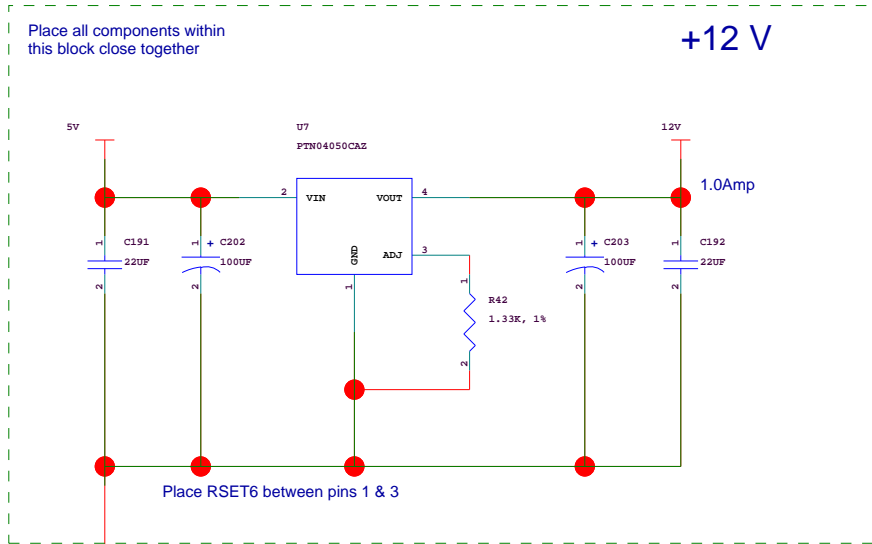
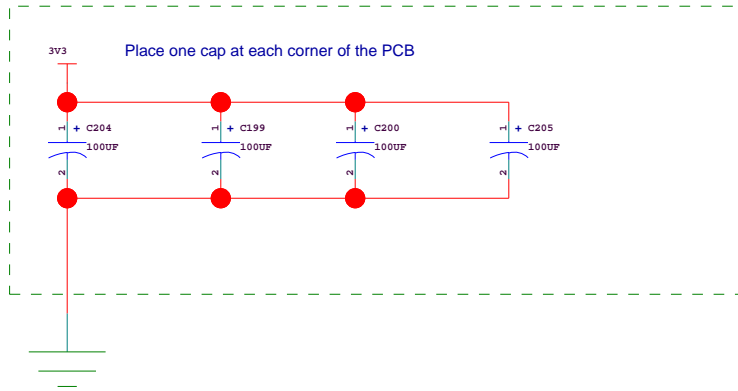
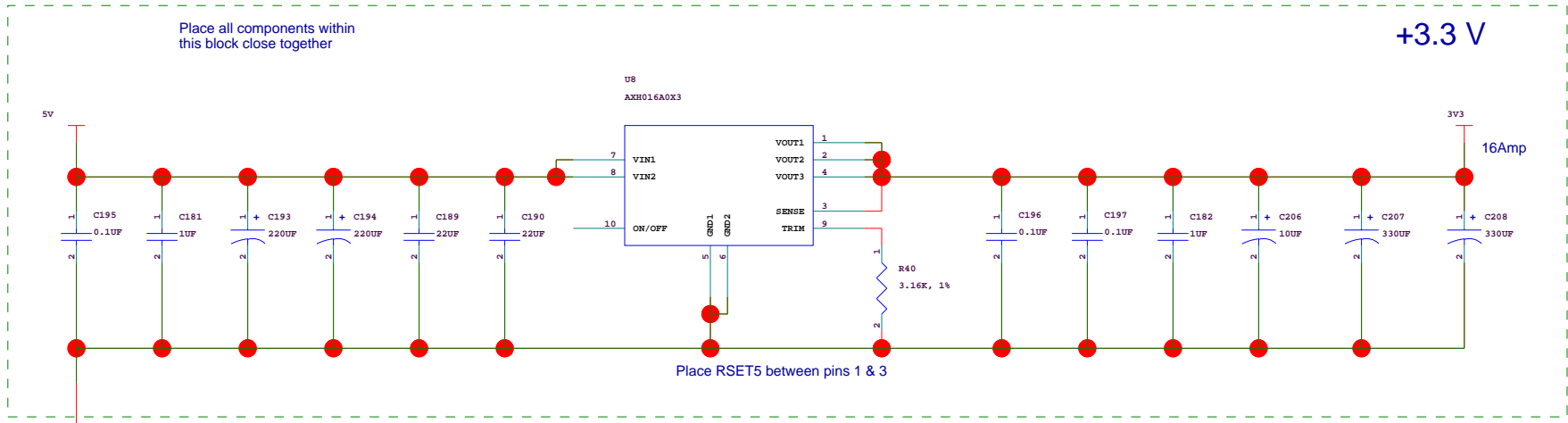
SHEET

1 of 1


9-27-2007\_19:00







1-3C,1-4C,1-4D  
13-5C,17-1D  
23-2E

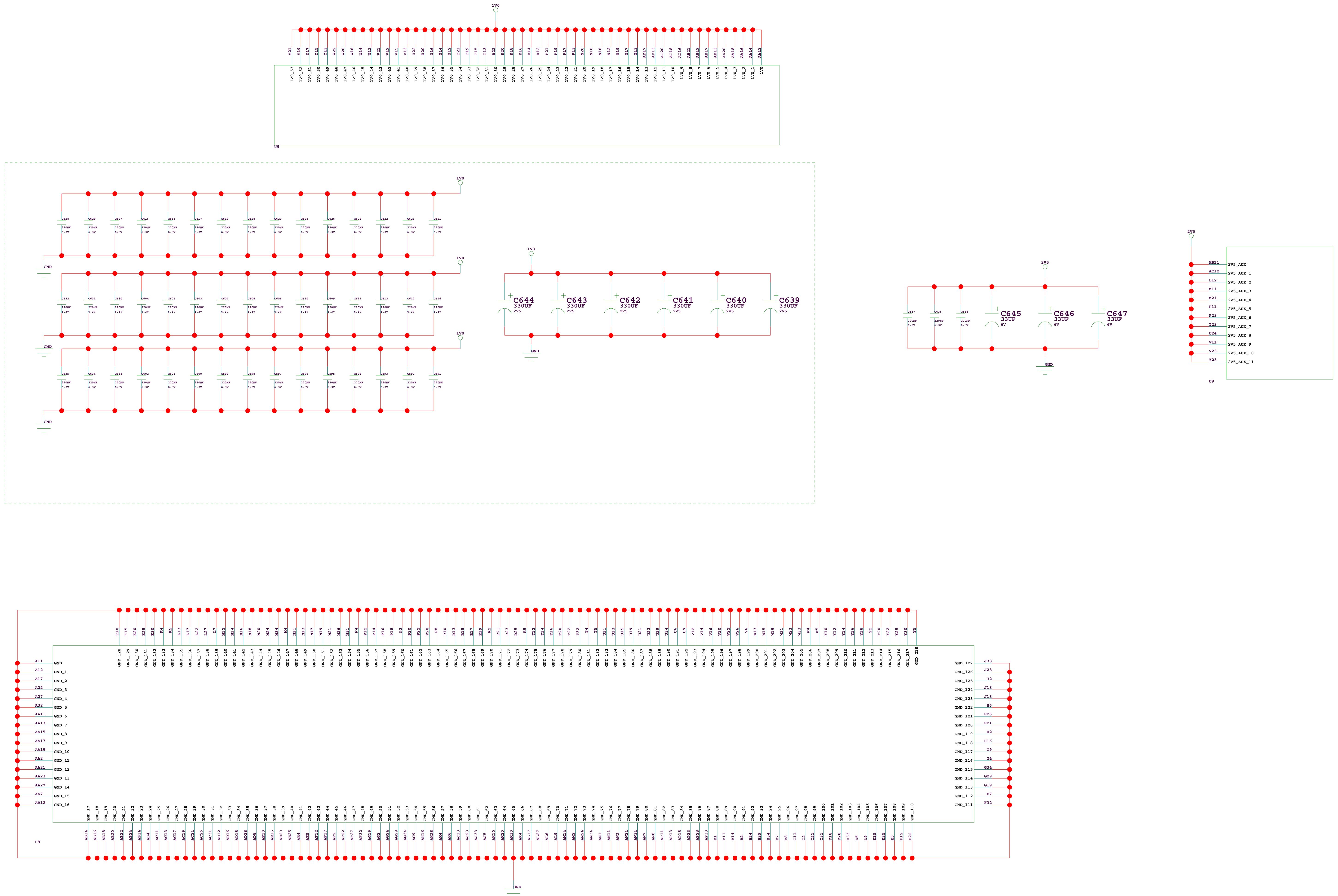


KAROO ARRAY TELESCOPE, NRF  
UNIT 12, LONSDALE BUILDING  
LONSDALE WAY, PINELANDS, 7405  
SOUTH AFRICA

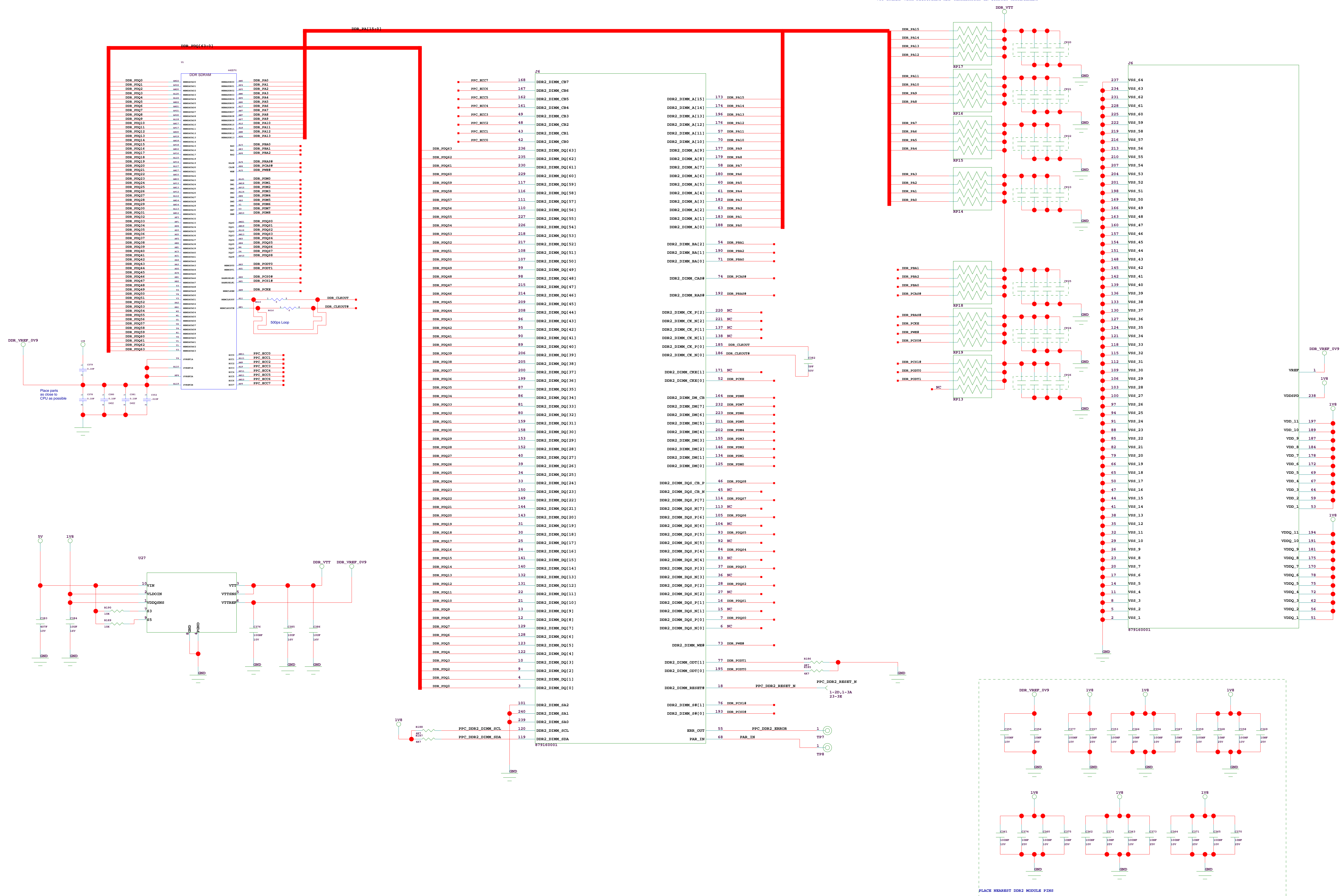
TITLE

ROACH\_PPC\_POWER\_2

CHECKED BY <PUT NAME HERE>	SIZE <b>A2</b>	DWG NO <PUT DRAWING NUMBER HERE>	REV <b>0</b>
DRAWN BY <PUT NAME HERE>	SCALE NTS	SHEET 1 of 1	9-27-2007_19:00



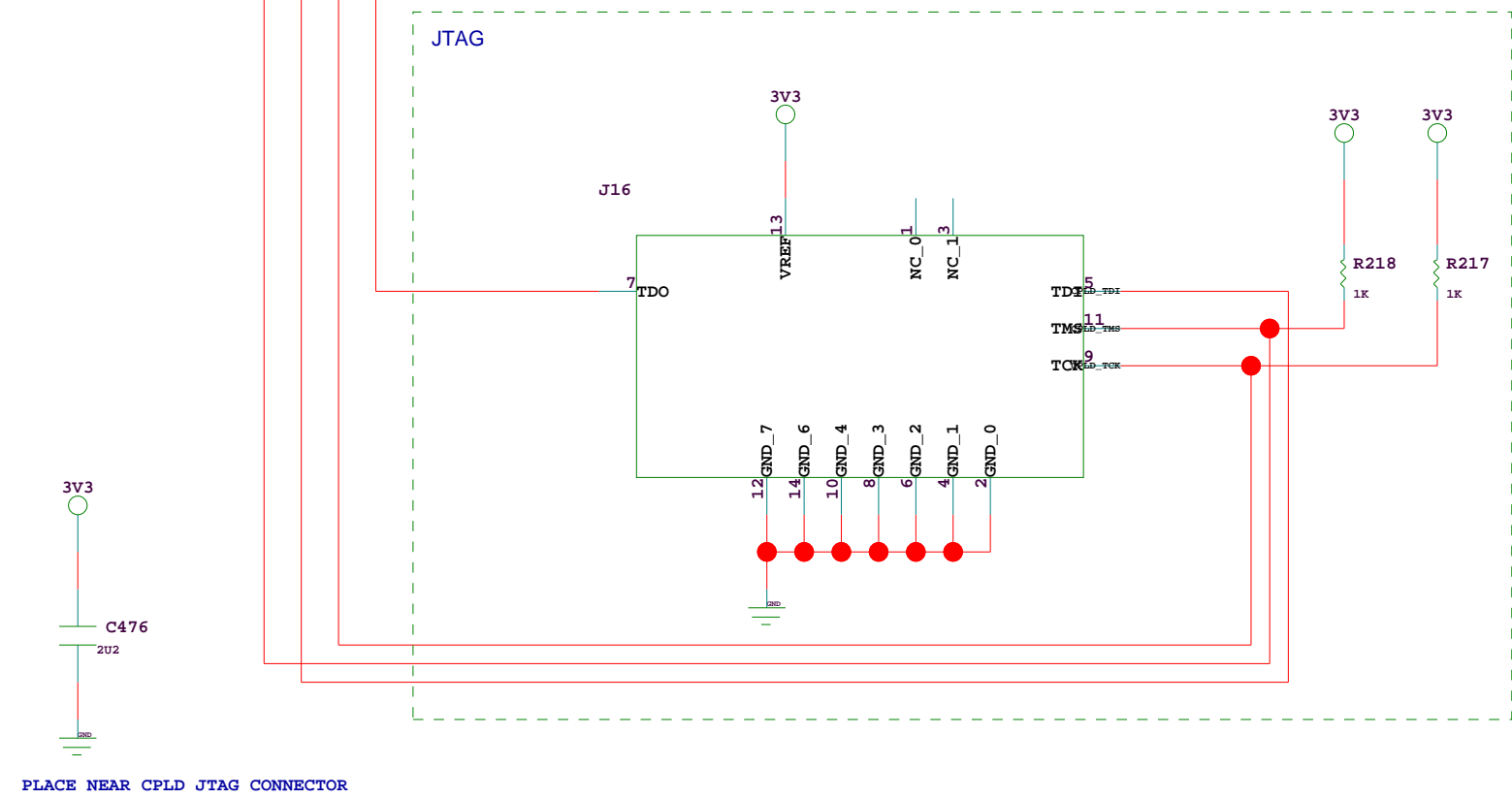
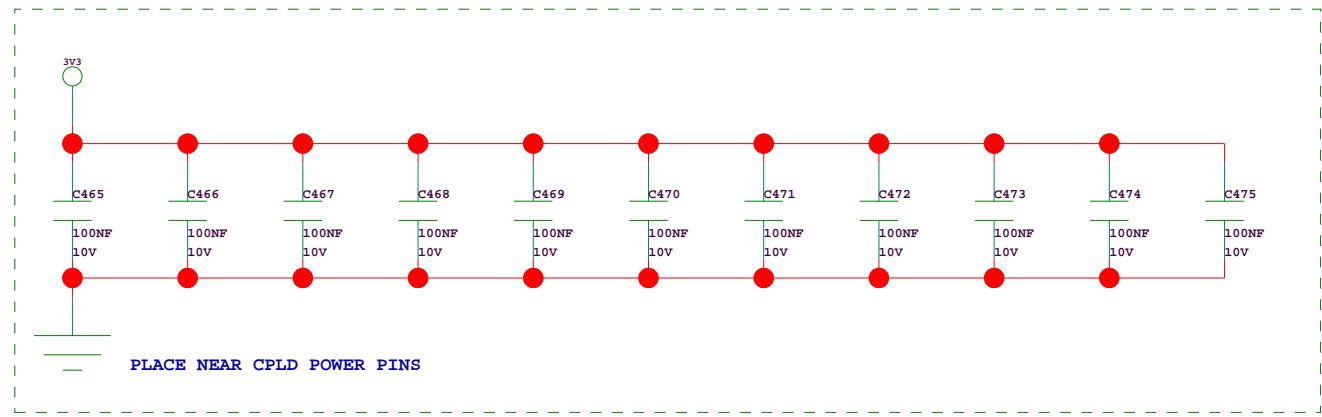










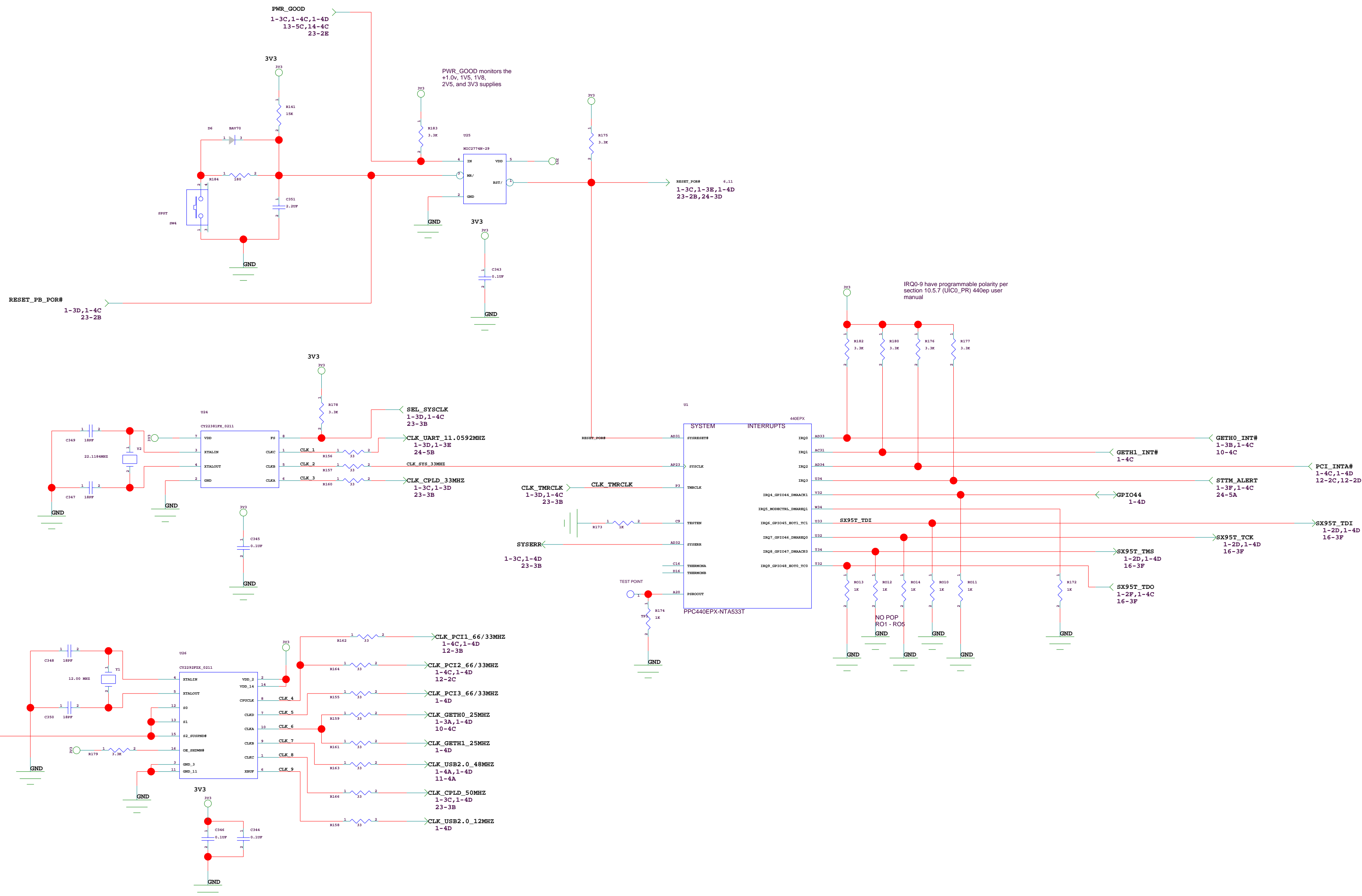


Critical Placement and Route  
Clock Rules:

Clock Rules:  
CLK\_UART\_11.0592MHz = as short as possible  
CLK\_SYS\_33MHz = as short as possible  
CLK\_CPLD\_33MHz = CLK\_SYS\_33MHz

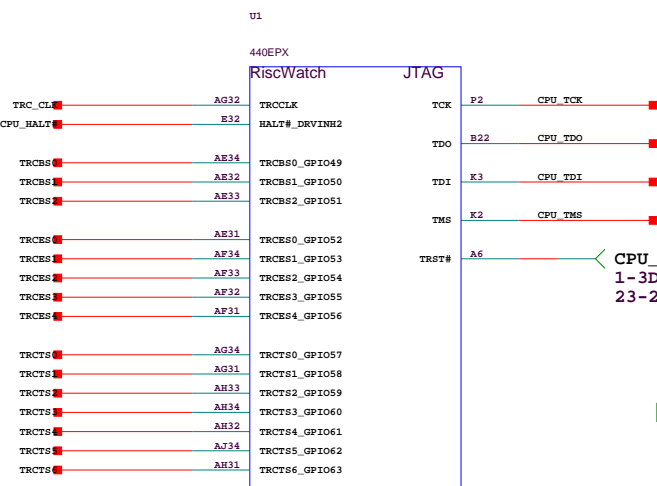
Critical Placement and Route  
Clock Rules:

Clock Rules:  
CLK\_PC13\_66/33MHz = as short as possible  
CLK\_PC12\_66/33MHz = CLK\_PC13\_66/33MHz  
CLK\_PC11\_66/33MHz = CLK\_PC12\_66/33MHz + 2.5°  
CLK\_GETH0\_25MHz = as short as possible  
CLK\_GETH1\_25MHz = CLK\_GETH0\_25MHz  
CLK\_CPLD\_50MHz = as short as possible  
CLK\_USB2\_0\_48MHz = as short as possible  
CLK\_USB2\_0\_12MHz = as short as possible

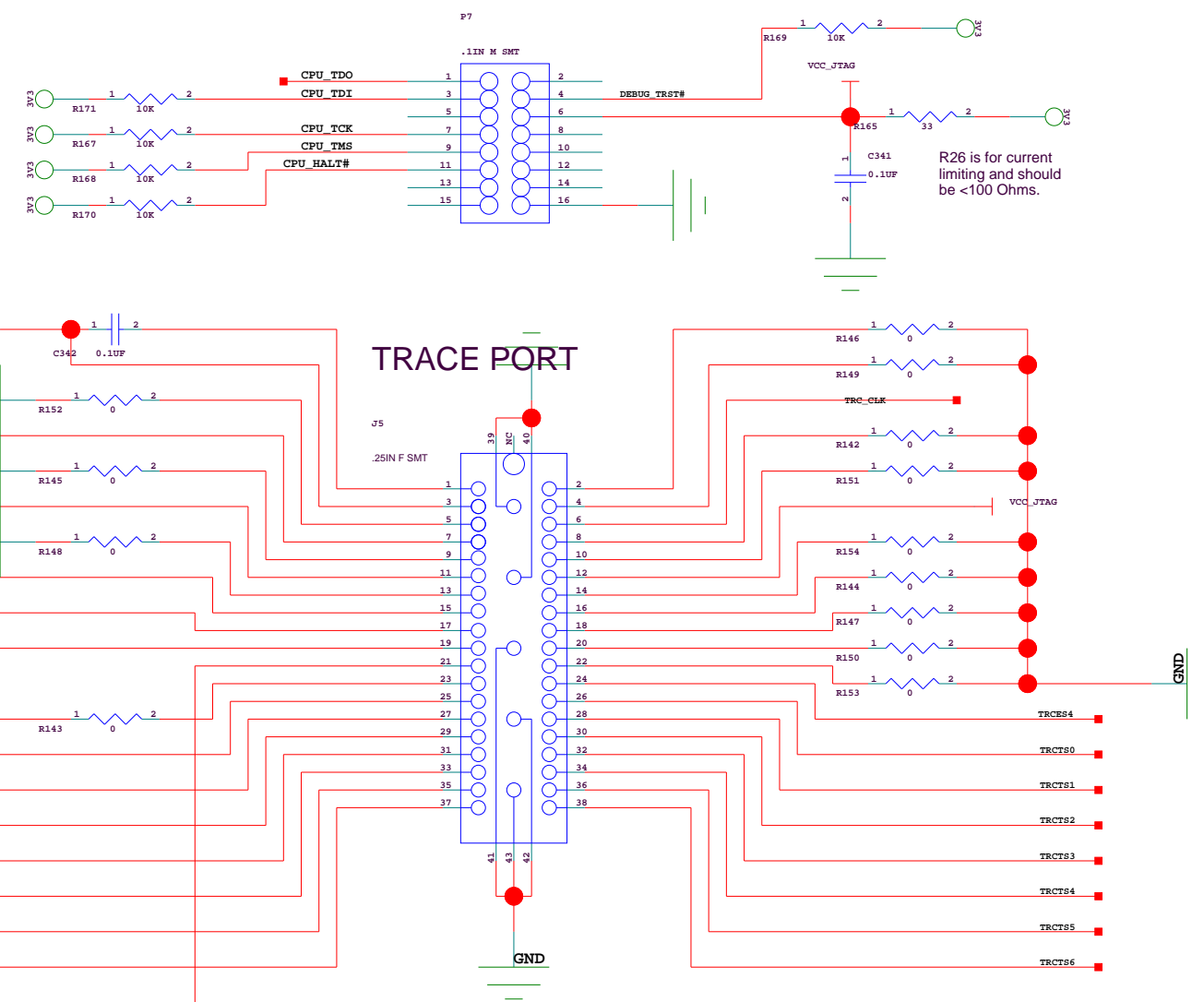


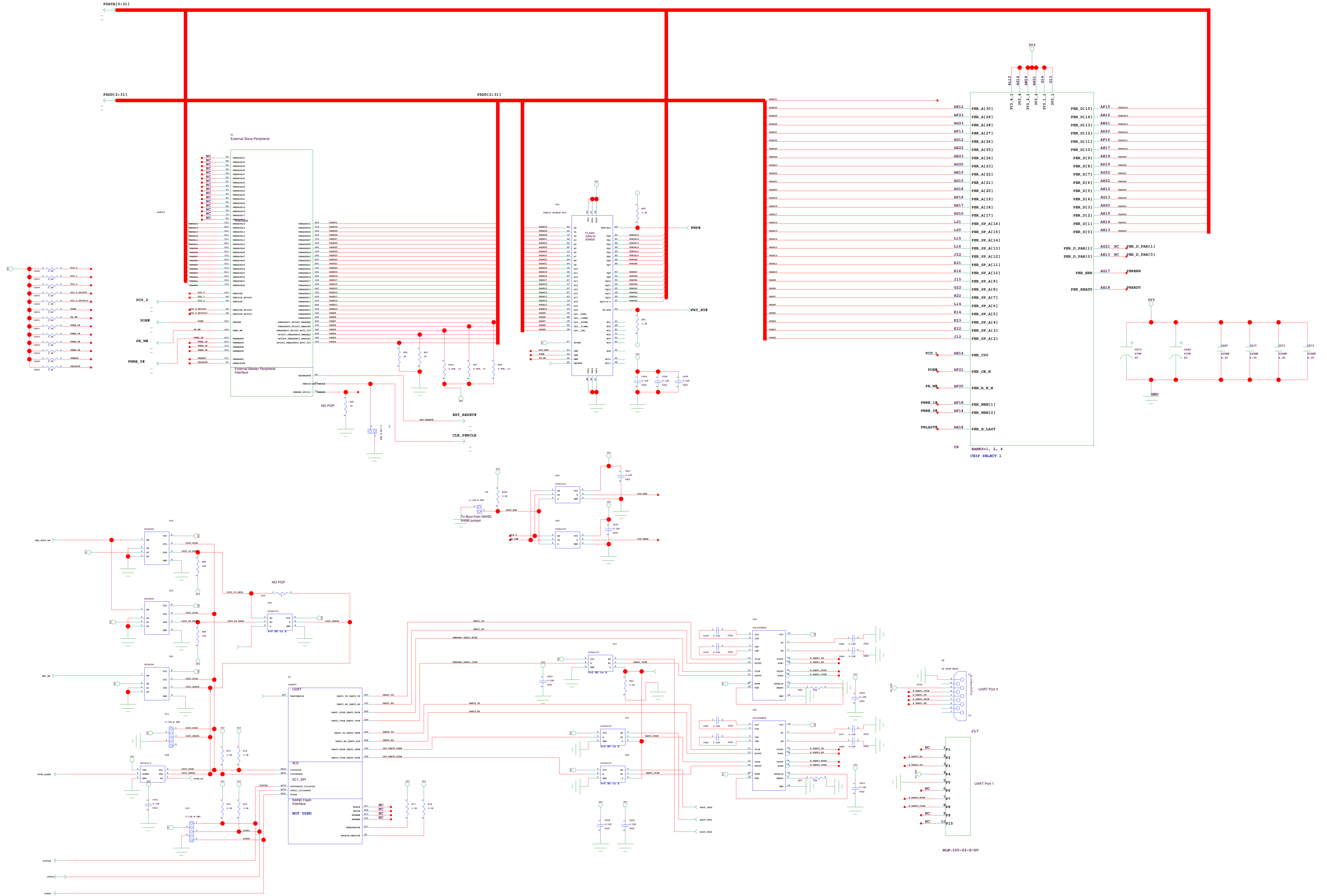
TRACE & JTAG CONNECTORS

Critical placement and routing  
of the Trace connector and nets.  
Up to CPU frequency!

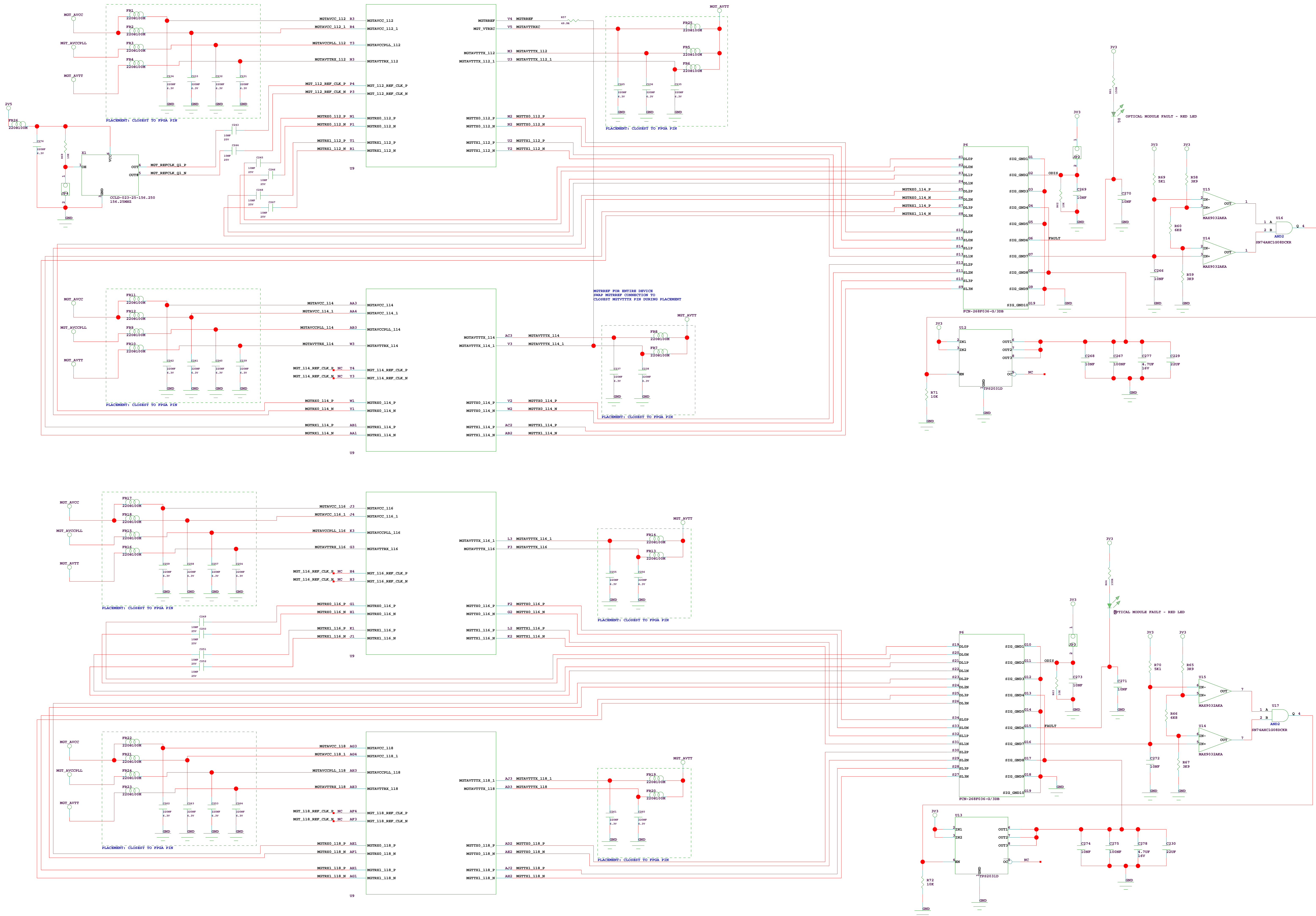


DEBUG\_TRST#  
1-3C,1-4D  
23-2B

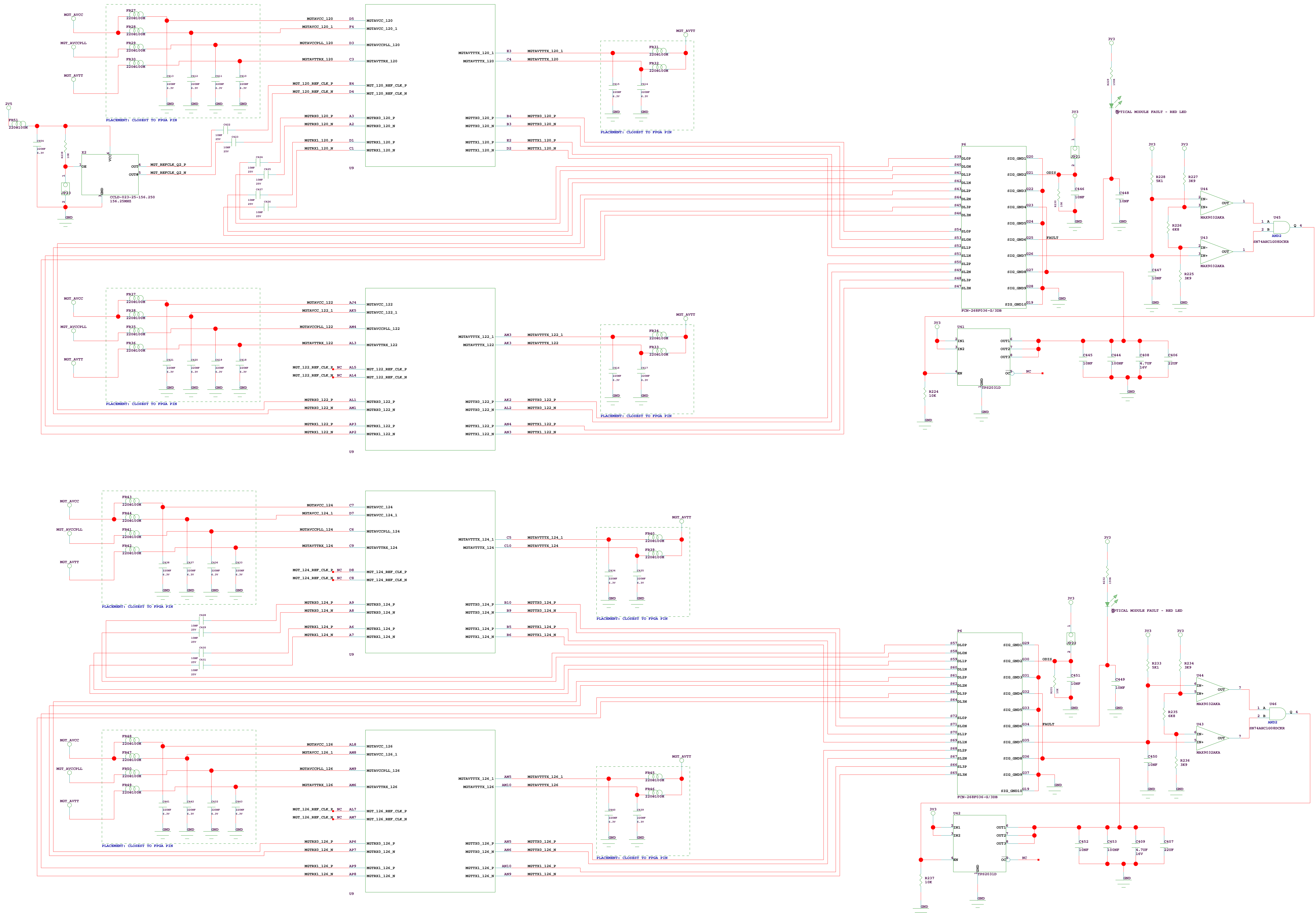


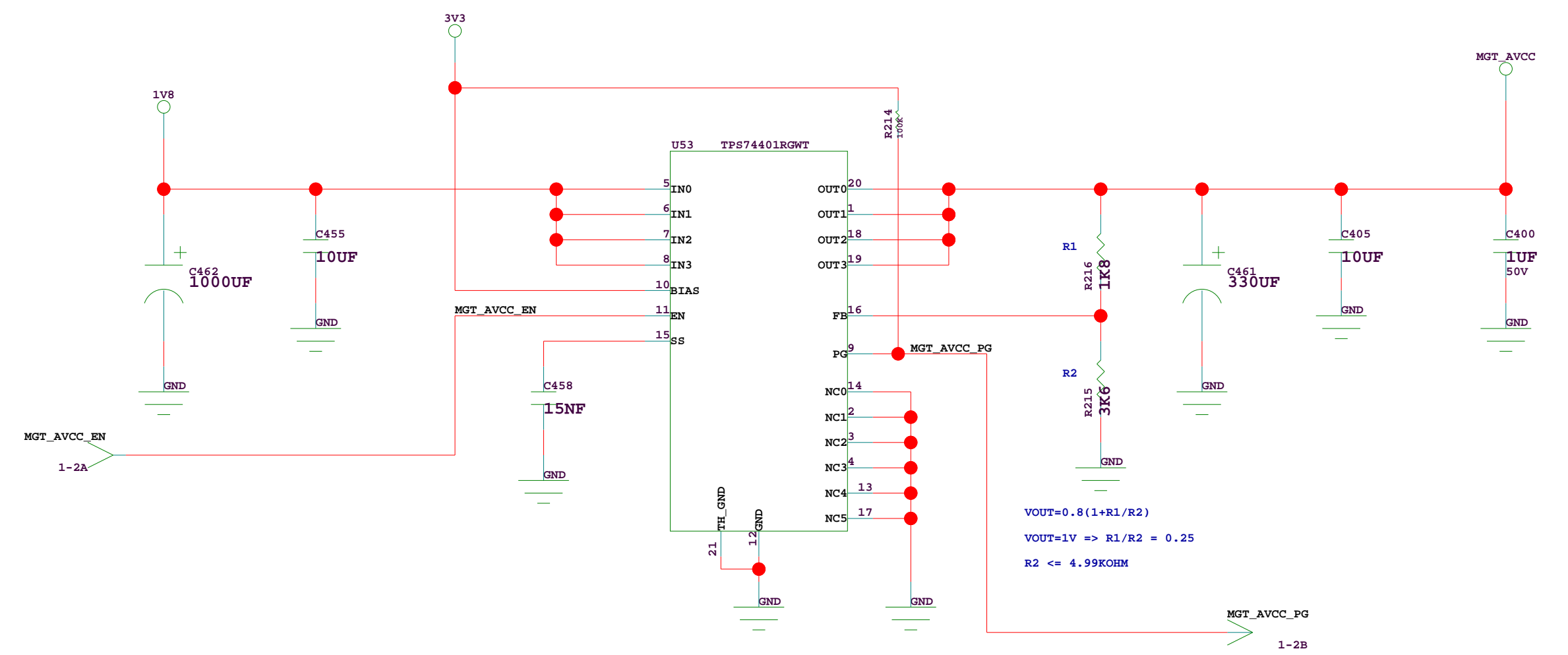
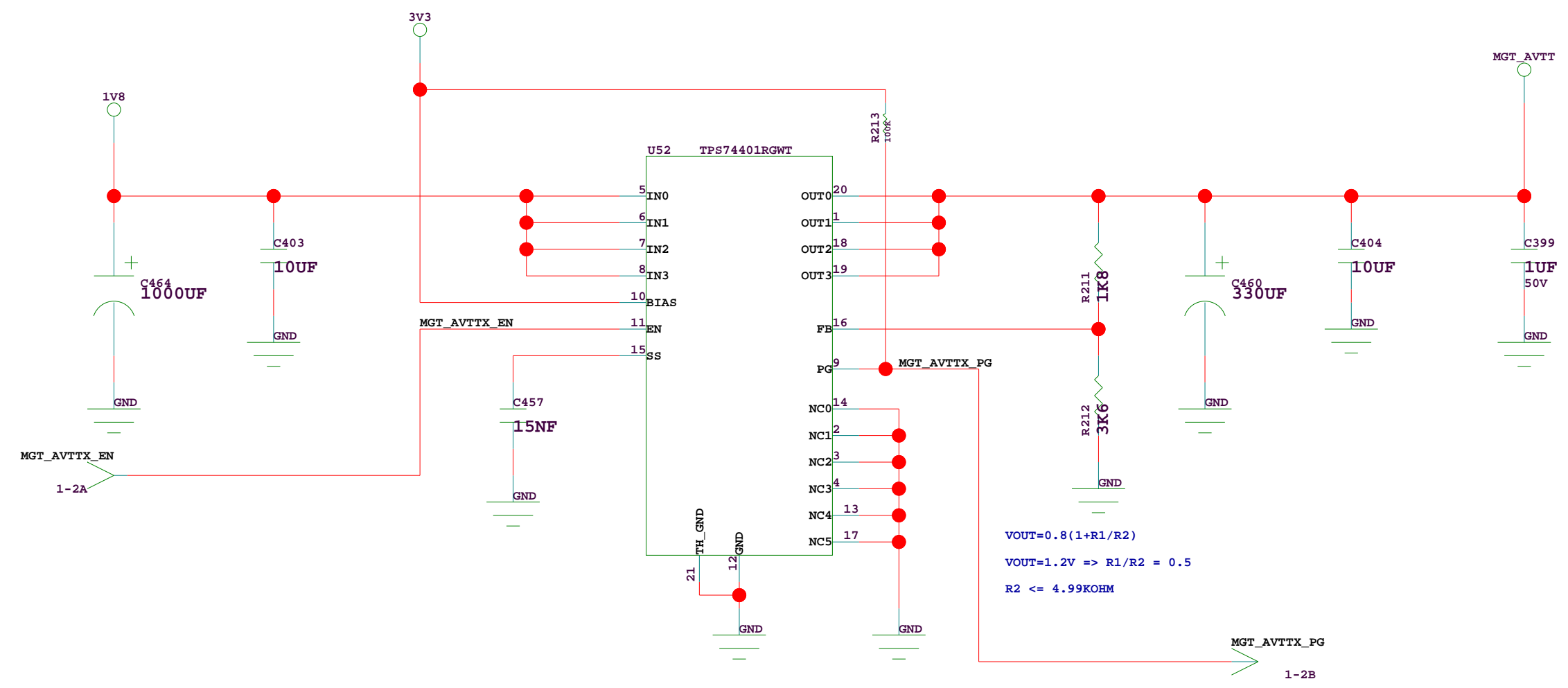
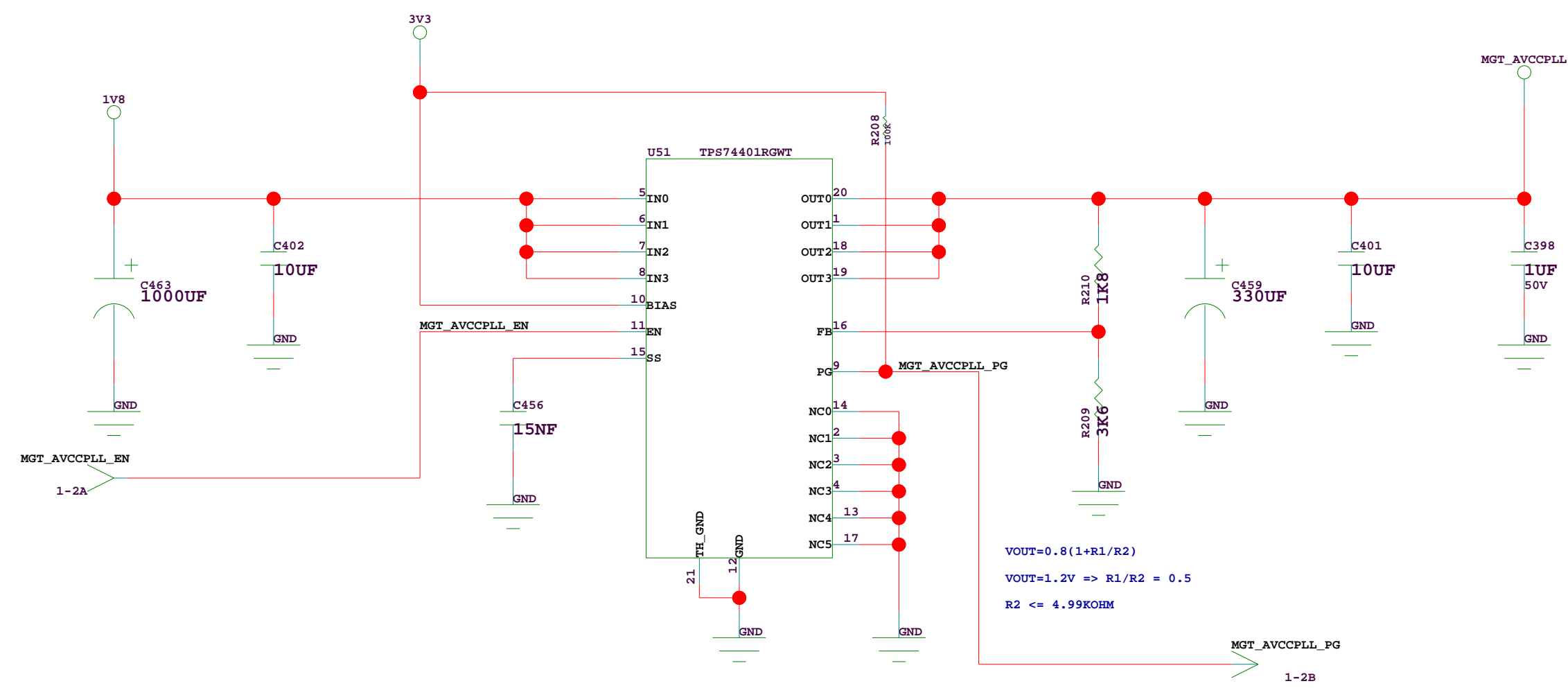


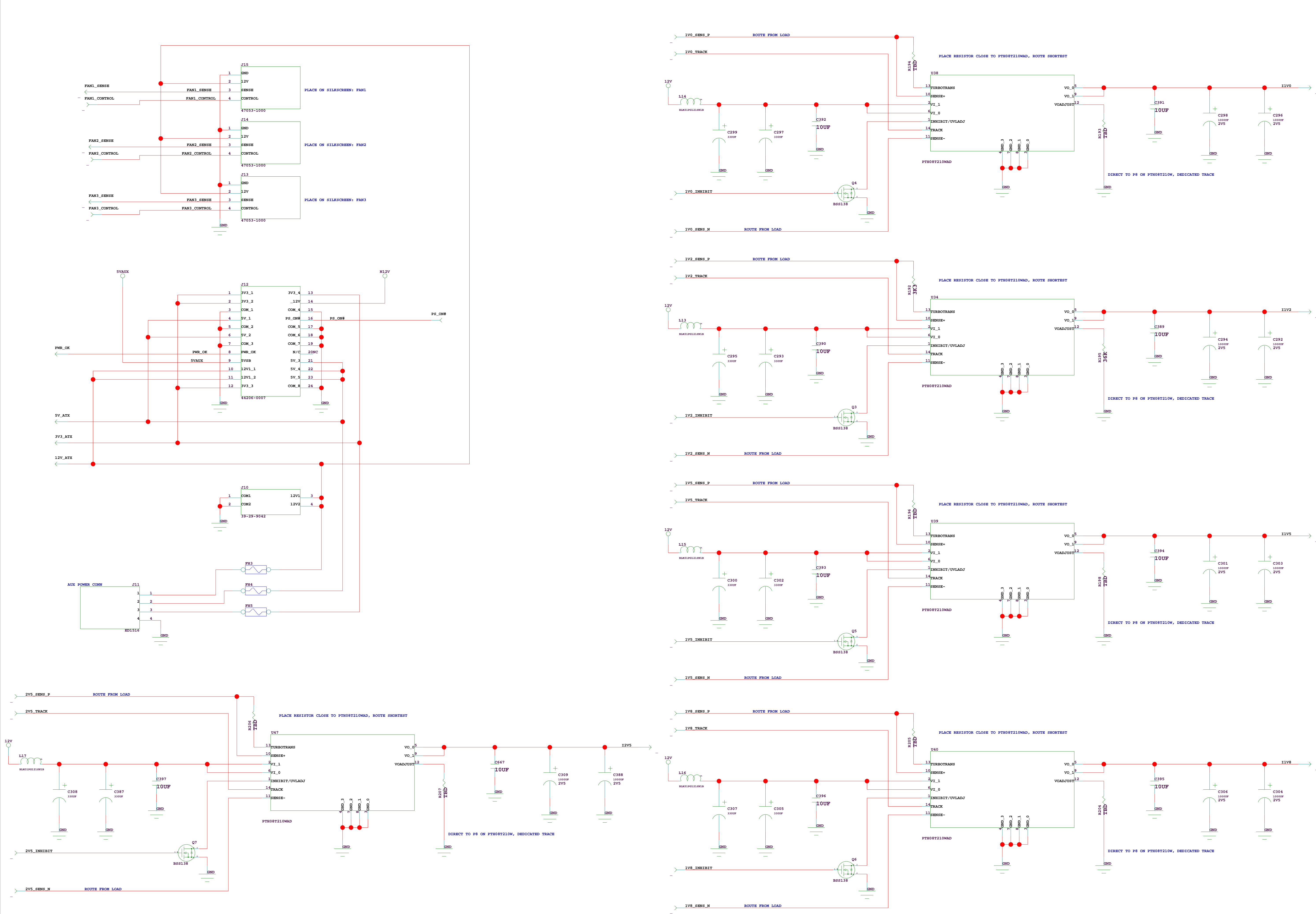




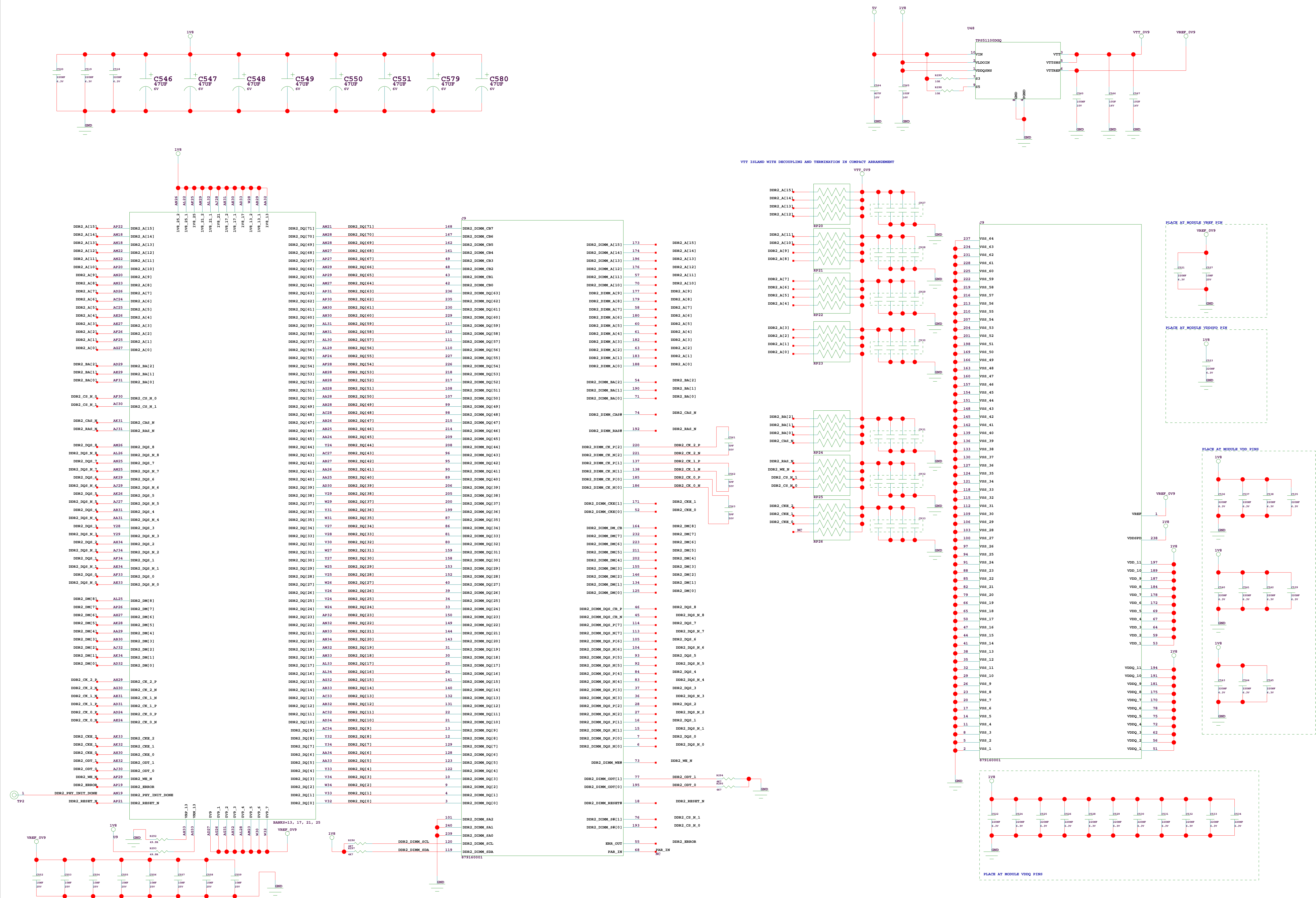




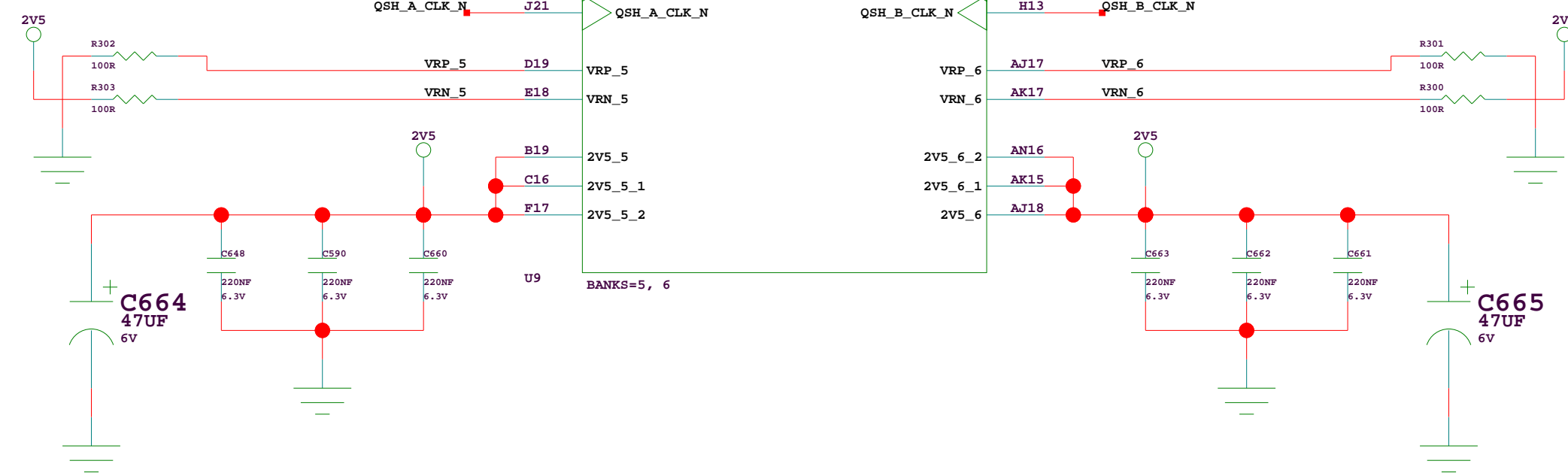
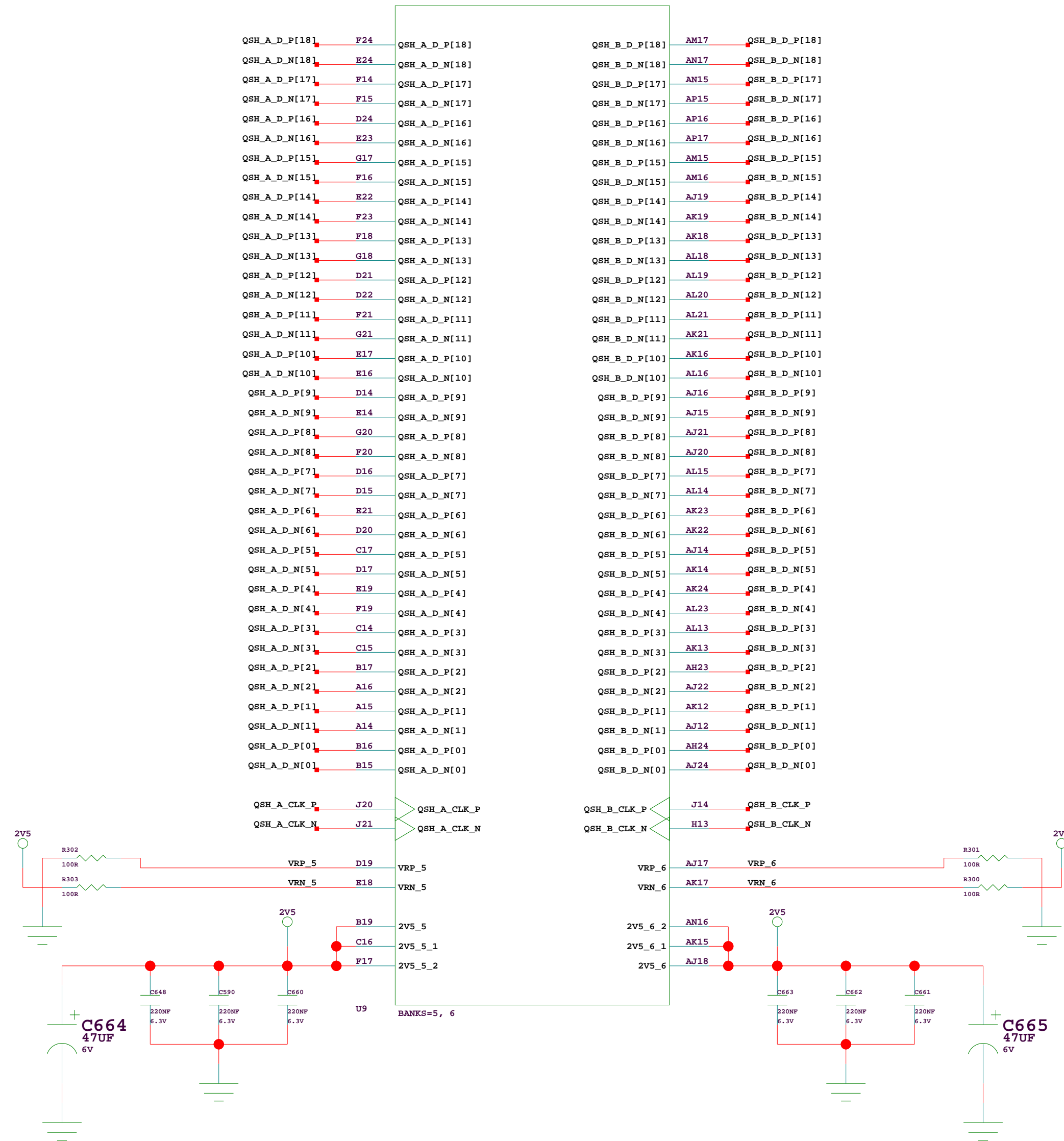
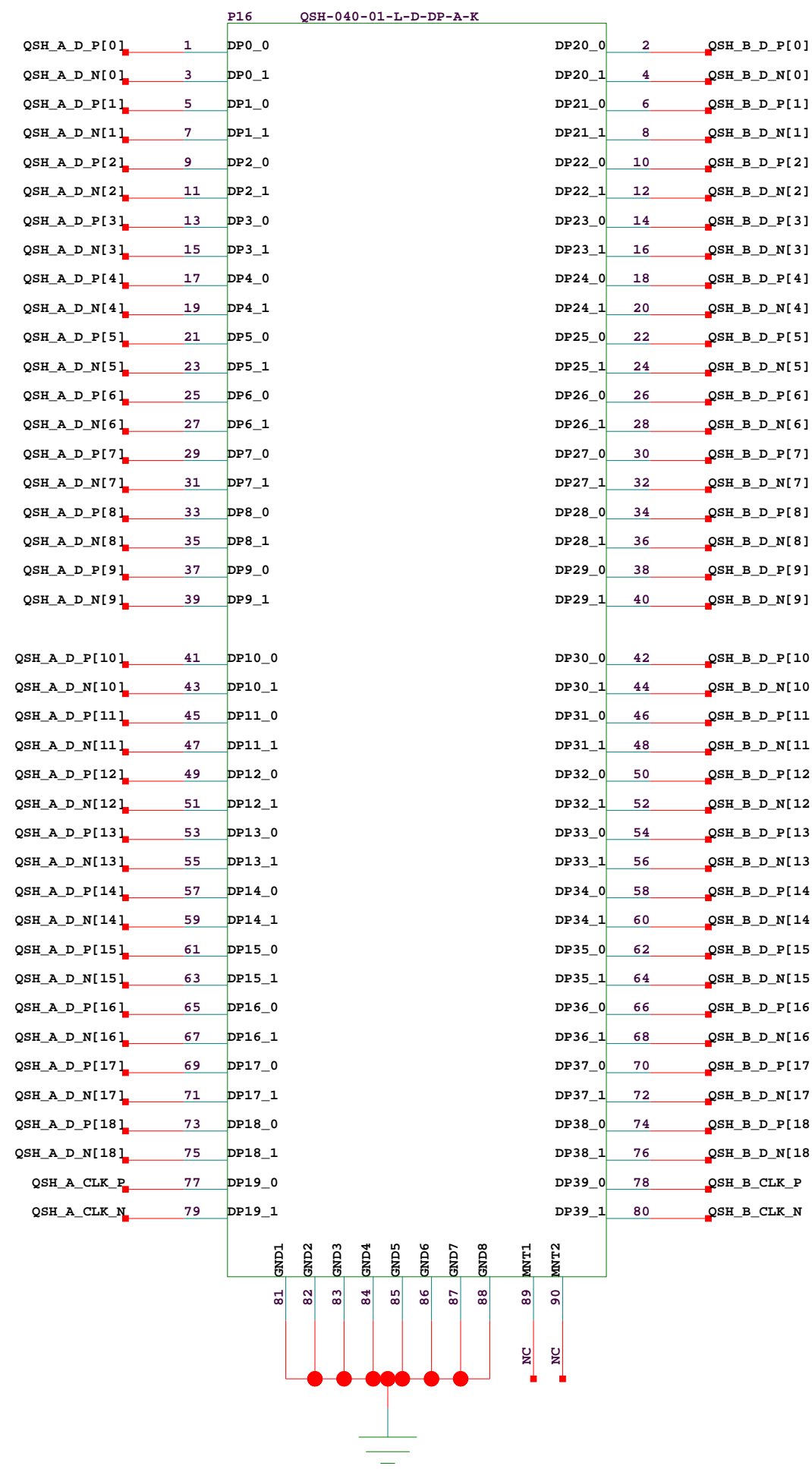


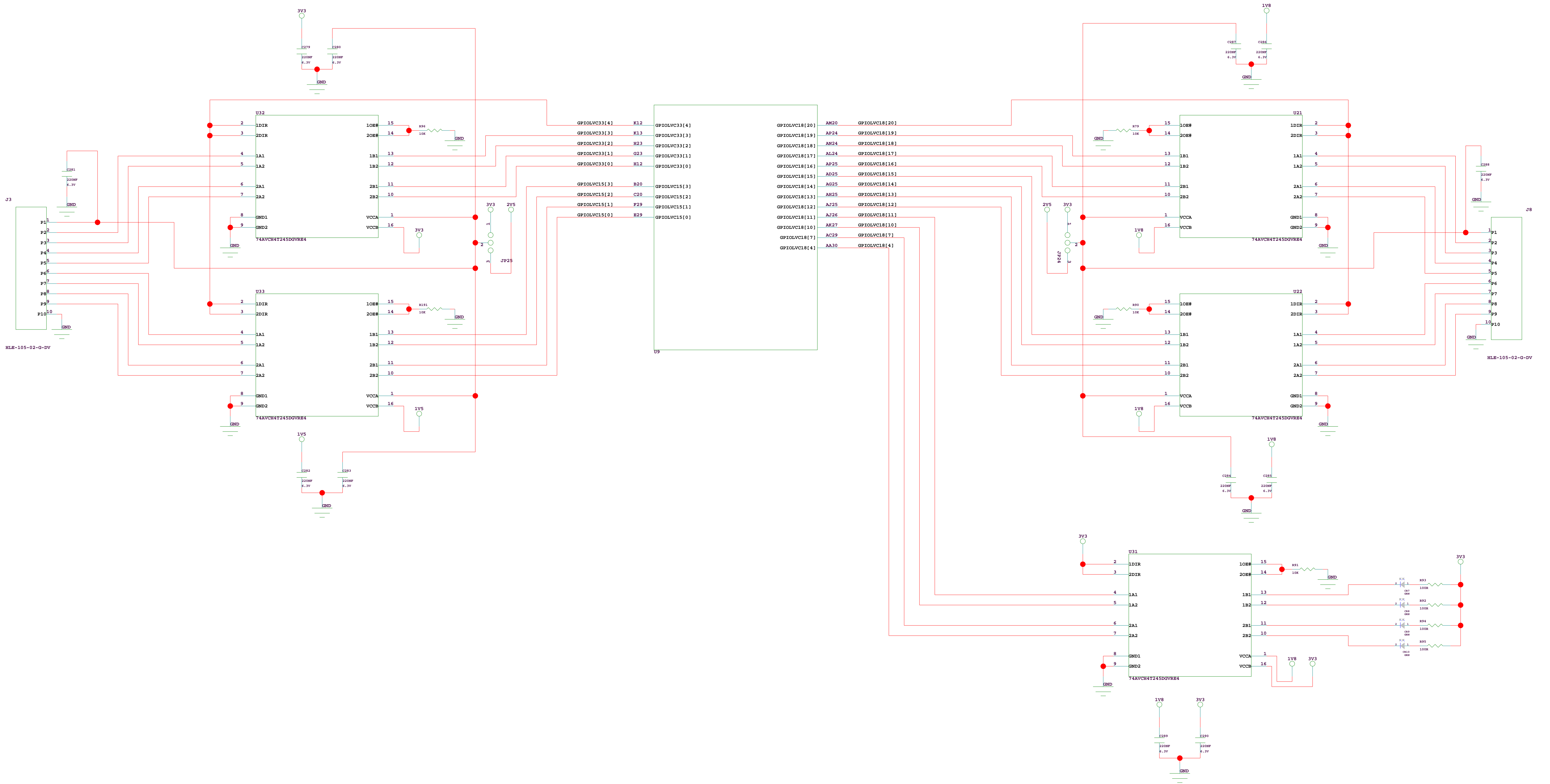








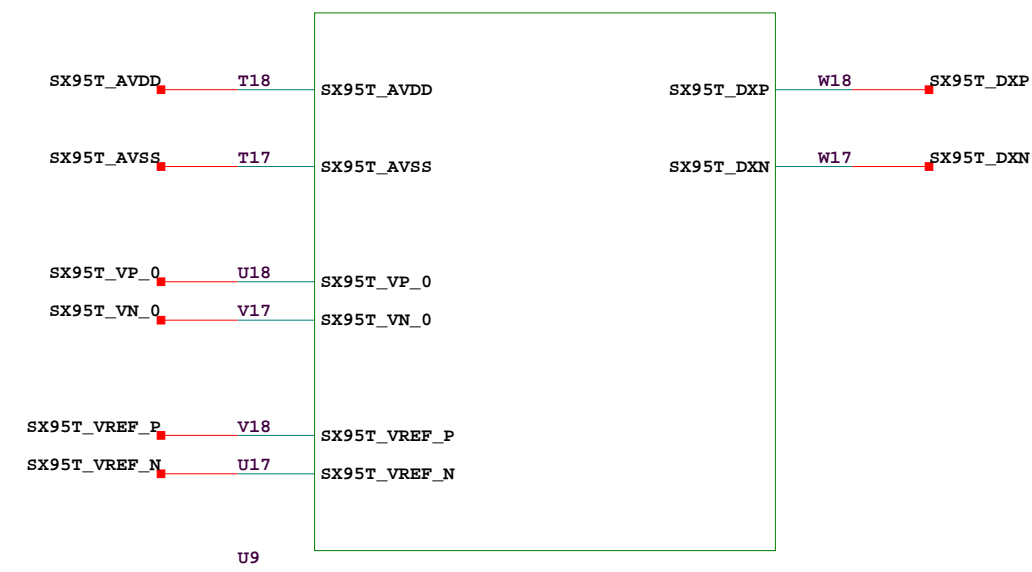
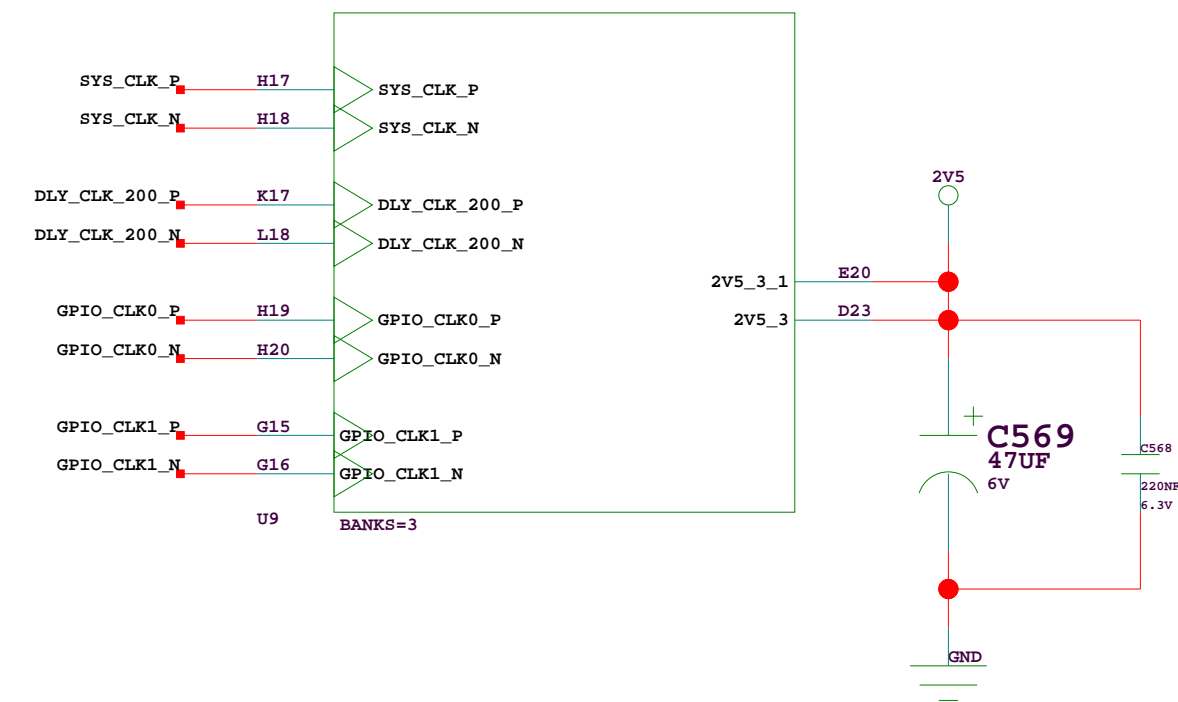


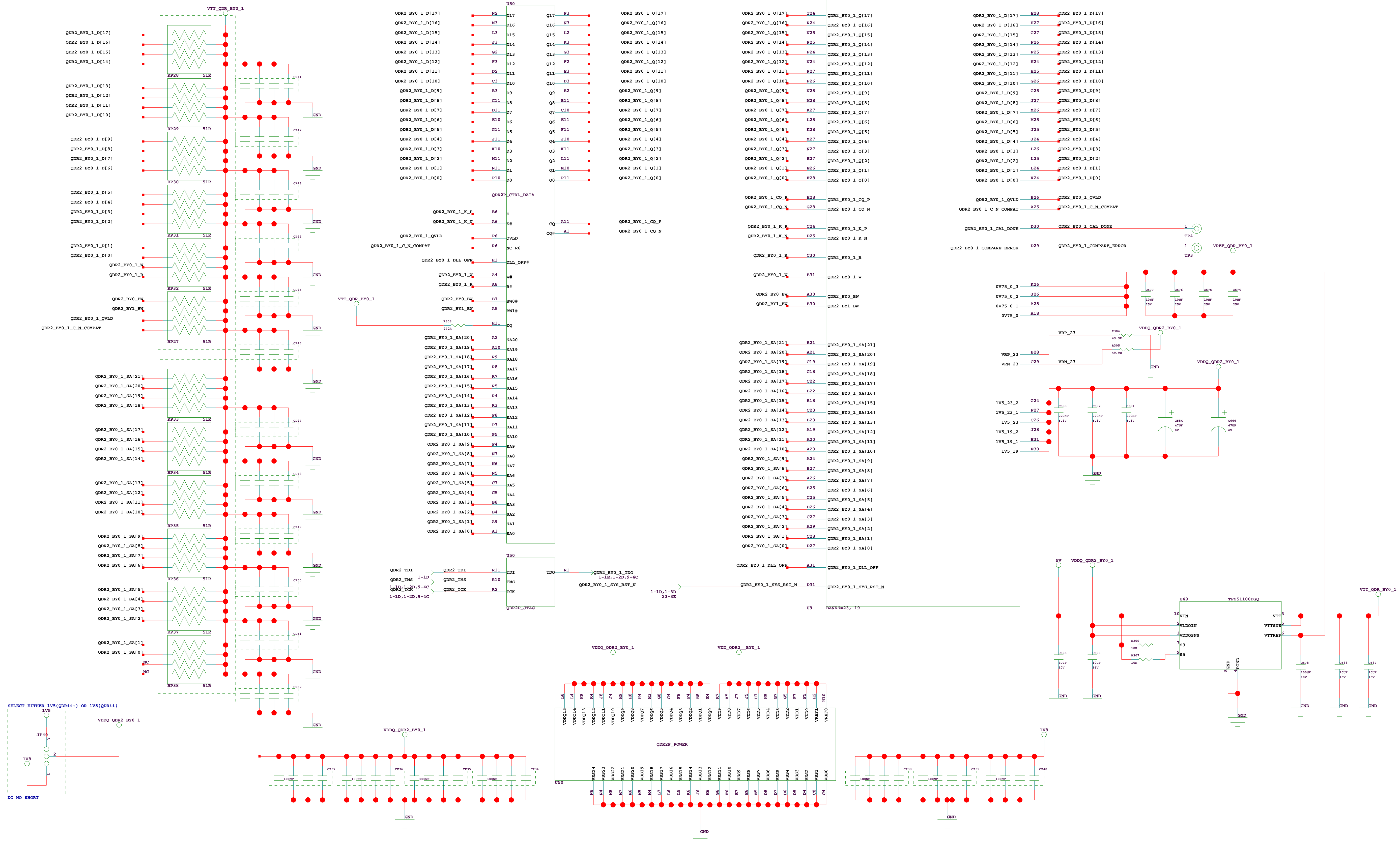


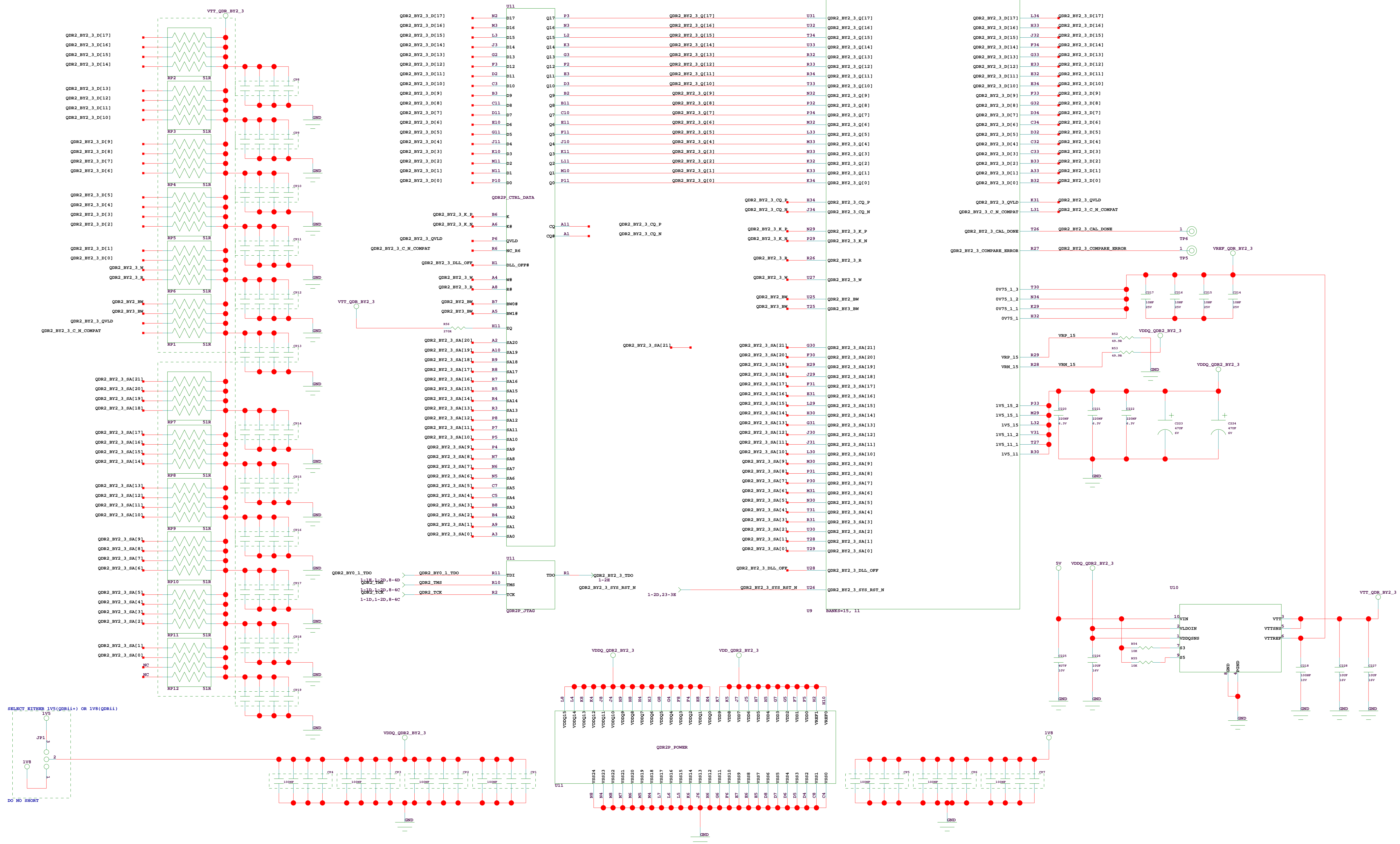












**TBD**

VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
Master JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

