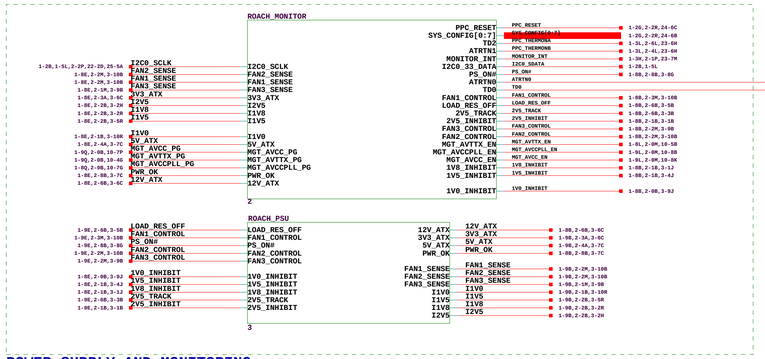
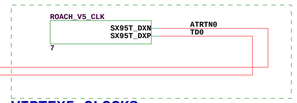
VIRTEX5

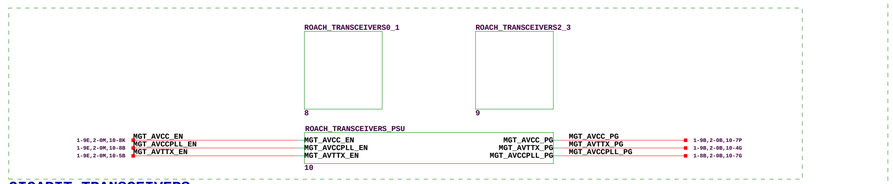


POWER SUPPLY AND MONITORING

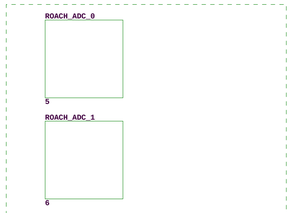


VIRTEX5 CLOCKS

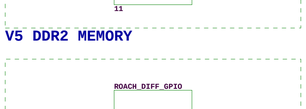
V5 DDR2 MEMORY



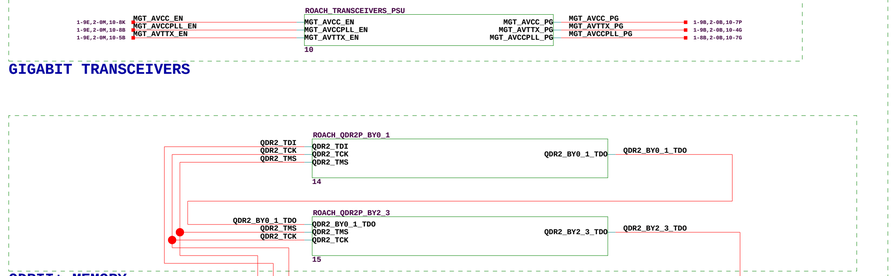
GIGABIT TRANSCEIVERS



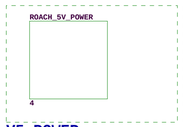
ZDOK/ADC INTERFACE



V5 DIFFERENTIAL GPIO



QDRII+ MEMORY

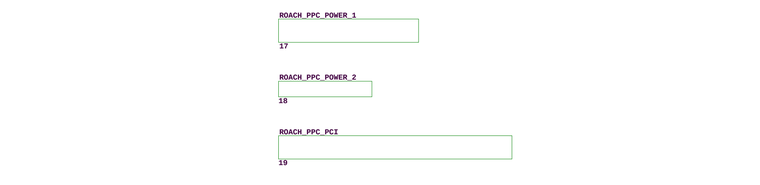


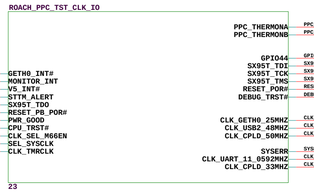
V5 POWER

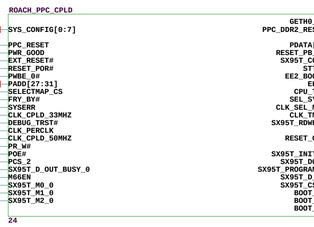
VIRTEX5 CONFIGURATION

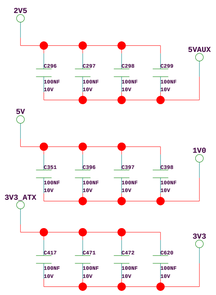
V5 SE GPIO & MISCELLANEOUS

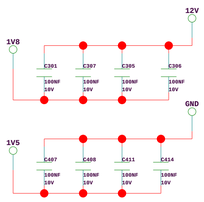
PPC











MECHANICAL

BOARD FIDUCIALS

LOGO'S

PLACEHOLDER FOR PCB
MEERKAT LOGO

PLACEHOLDER FOR PCB
CASPER LOGO

PLACEHOLDER FOR PCB
ROACH LOGO

PLACEHOLDER FOR PCB
NRAO LOGO

BOARD SERIAL NUMBER

CONTRIBUTORS

ETIENNE BAUERMEISTER
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STEVE DURAND
FRANCOIS KAPP
ALAN LANGMAN
GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

6-9-2008_14:27

PATH PATH

ROACH_TOP

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 1 OF 25

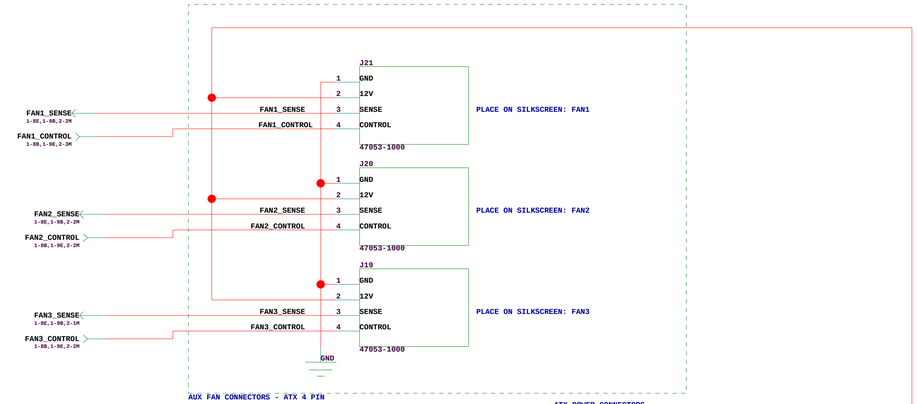
REFERENCE RESISTOR/ADC VALUES

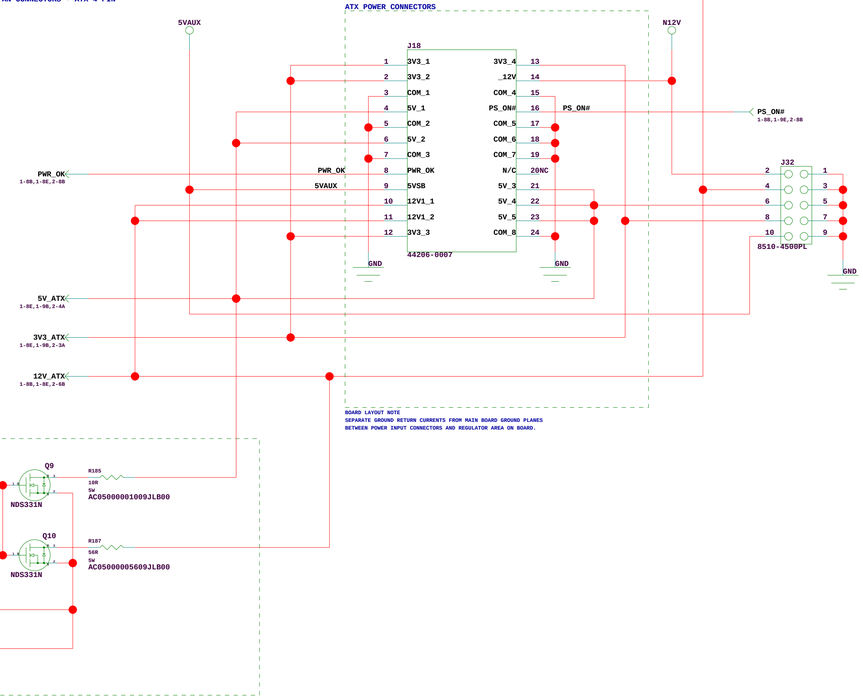
VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)
12V	0R01	3.36	0.11
5V	0R0047	6.78	0.22
3V3	0R01	3.47	0.12
2V5	0R01	3.56	0.13
1V8	0R0022	12.91	0.37
1V5	0R0047	6.77	0.22
1V0	0R001	26.79	0.72

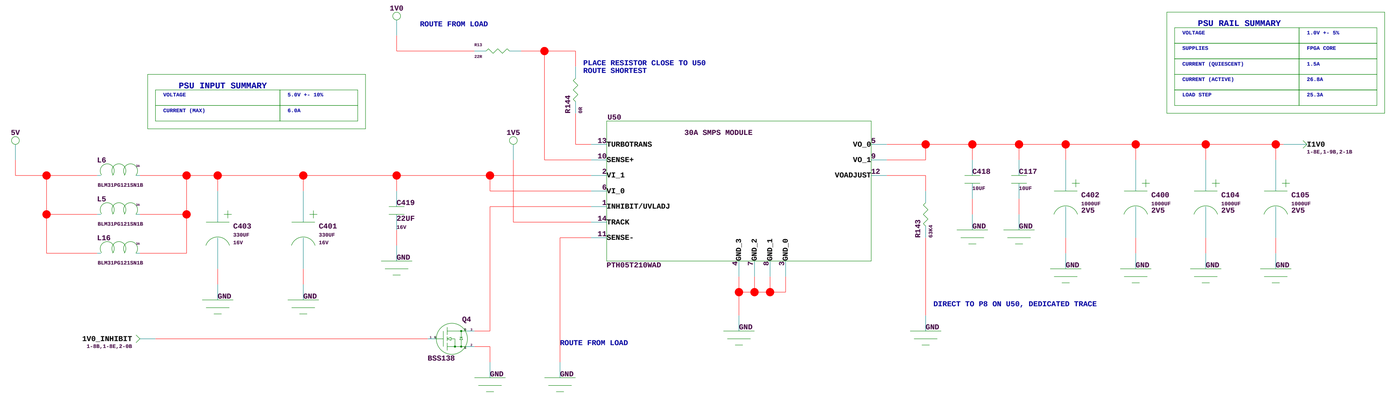
FOR 8 BIT ADC USING 2.56V REFERENCE:

ADC COUNT AT MAX POWER	CURRENT/BIT (A)
33	0.1
31	0.21
34	0.1
35	0.1
28	0.45
31	0.21
26	1.0

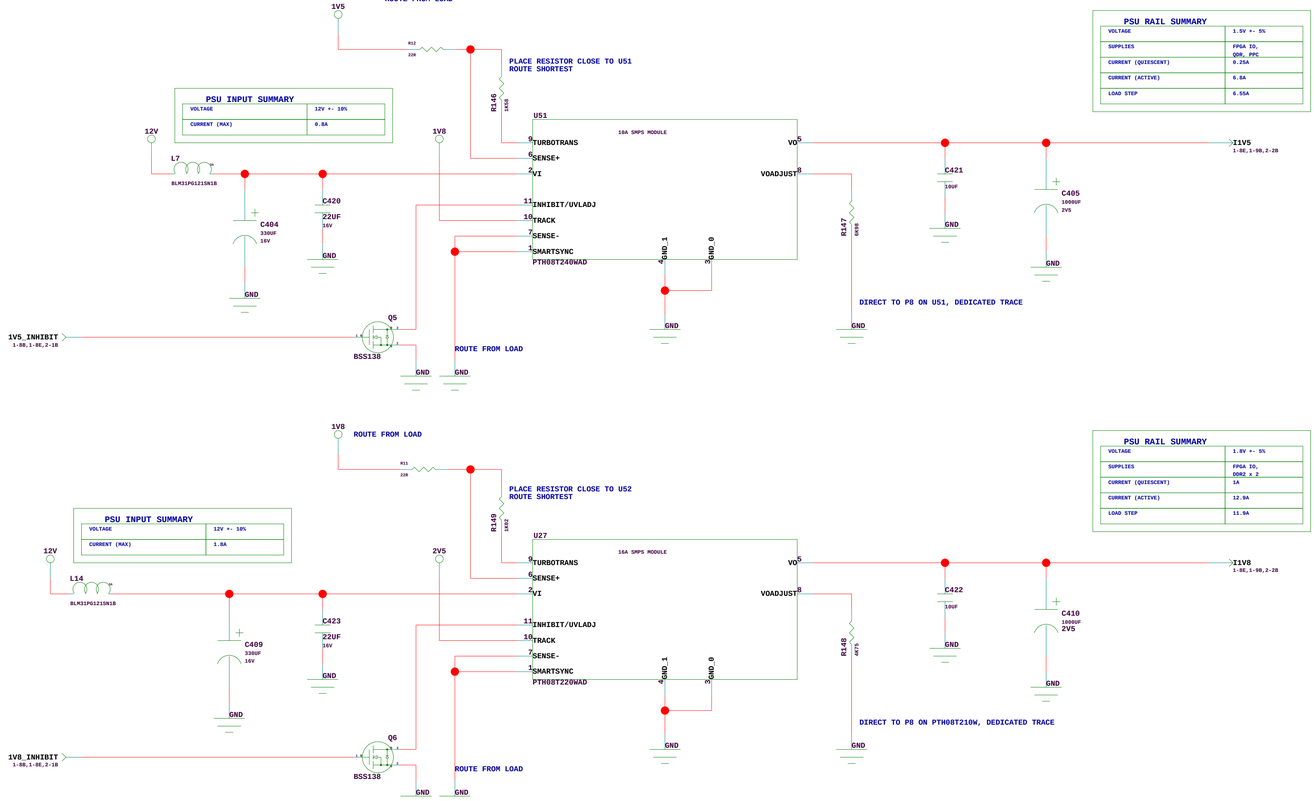
ROACH/iBOB2	ROACH_MONITOR
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-9-2008_14:27	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 2 OF 25

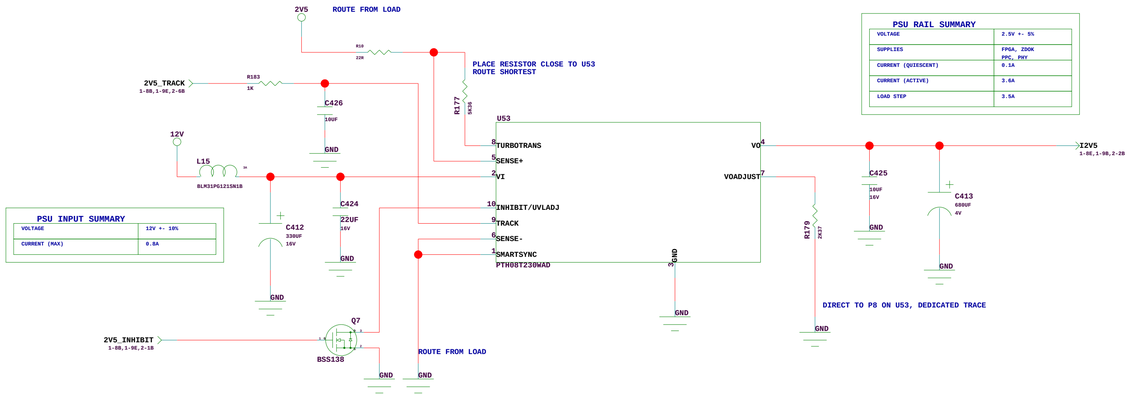




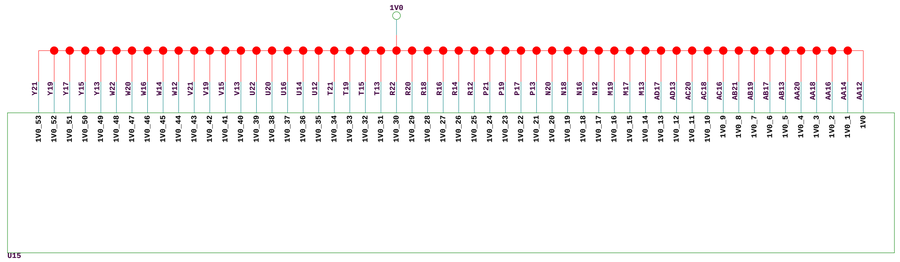


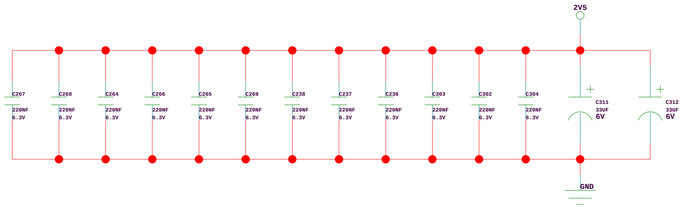
1.2V SUPPLY DELETED - NOT REQUIRED

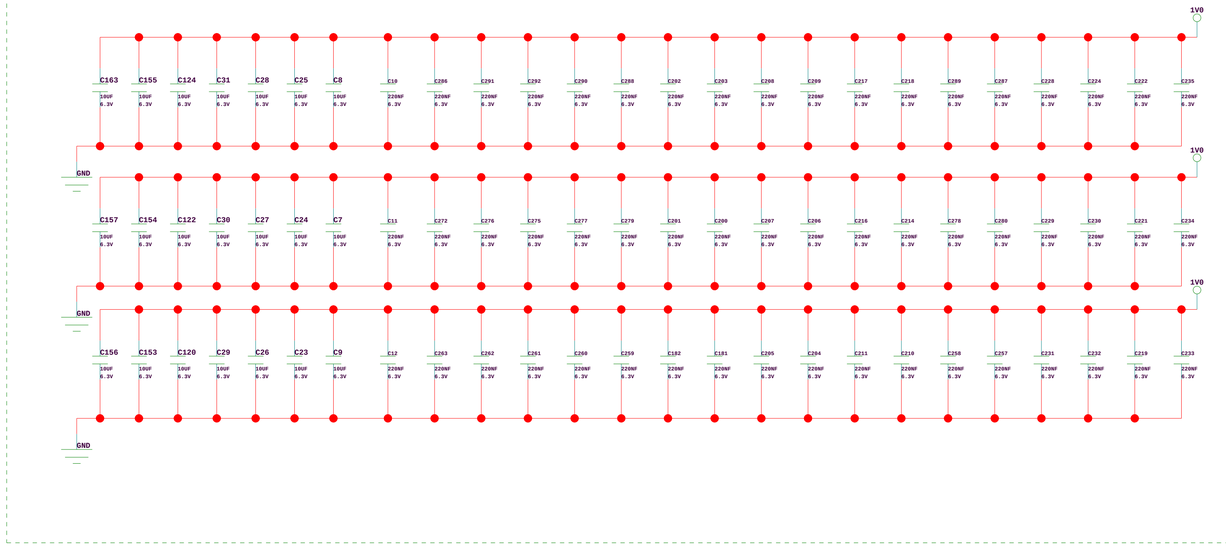


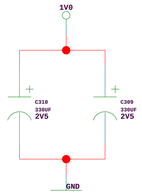


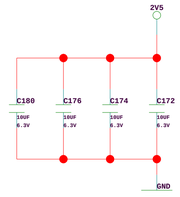
ROACH/iBOB2	ROACH_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-9-2008_14:27	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 3 OF 25

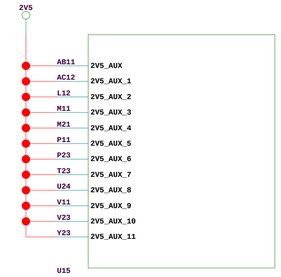


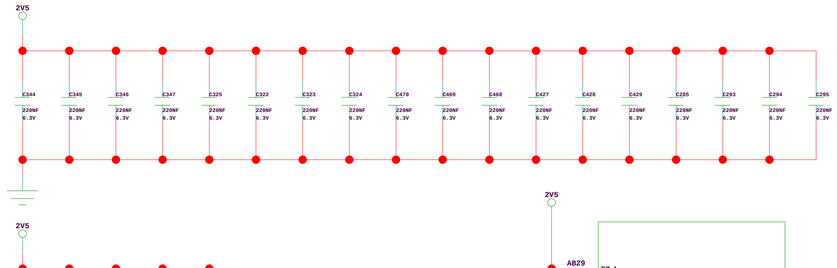


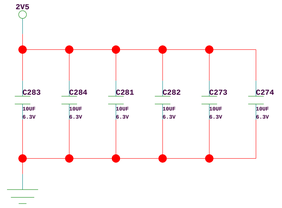


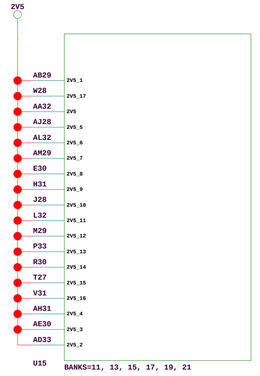


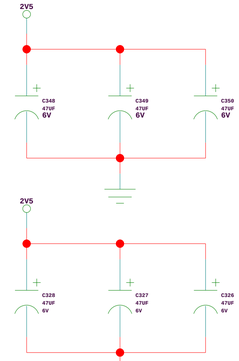


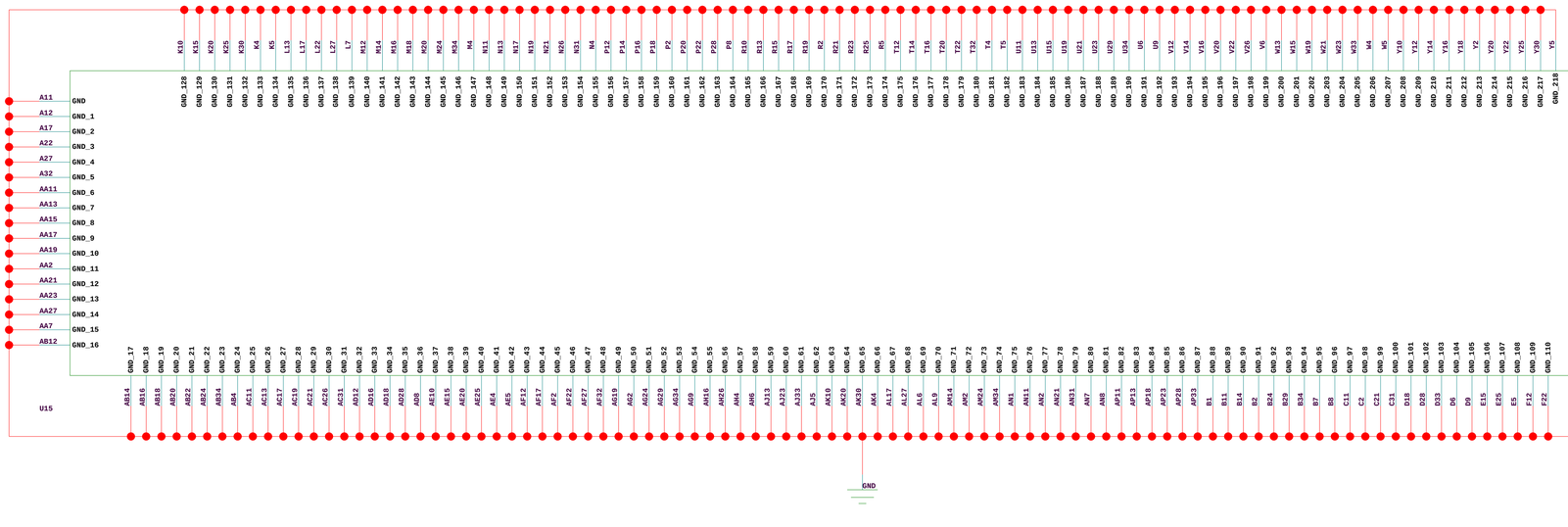












ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
6-9-2008_14:27 PATH PATH	

| | | |

	A	B	C	D	E	F	G	H	J	K	L	M

U15

6-5L	ZDOK1_CLK0_P	H17	ZDOK1_CLK0_P
6-5L	ZDOK1_CLK0_N	H18	ZDOK1_CLK0_N
6-3L	ZDOK1_CLK1_P	K17	ZDOK1_CLK1_P
6-3L	ZDOK1_CLK1_N	L18	ZDOK1_CLK1_N

ZDOK1_DP_P[37]	AD31	ZDOK1_DP_P37	6-3L
ZDOK1_DP_N[37]	AE31	ZDOK1_DP_N37	6-3L
ZDOK1_DP_P[36]	AF33	ZDOK1_DP_P36	6-3L
ZDOK1_DP_N[36]	AE33	ZDOK1_DP_N36	6-3L
ZDOK1_DP_P[35]	AF31	ZDOK1_DP_P35	6-4L
ZDOK1_DP_N[35]	AG31	ZDOK1_DP_N35	6-4L
ZDOK1_DP_P[34]	AG32	ZDOK1_DP_P34	6-4L
ZDOK1_DP_N[34]	AH32	ZDOK1_DP_N34	6-4L
ZDOK1_DP_P[33]	AG28	ZDOK1_DP_P33	6-4L
ZDOK1_DP_N[33]	AH28	ZDOK1_DP_N33	6-4L
ZDOK1_DP_P[32]	AF24	ZDOK1_DP_P32	6-4L
ZDOK1_DP_N[32]	AG25	ZDOK1_DP_N32	6-4L
ZDOK1_DP_P[31]	AJ30	ZDOK1_DP_P31	6-4L
ZDOK1_DP_N[31]	AH30	ZDOK1_DP_N31	6-4L
ZDOK1_DP_P[30]	AK28	ZDOK1_DP_P30	6-5L
ZDOK1_DP_N[30]	AK27	ZDOK1_DP_N30	6-5L
ZDOK1_DP_P[29]	AK26	ZDOK1_DP_P29	6-5L
ZDOK1_DP_N[29]	AJ27	ZDOK1_DP_N29	6-5L
ZDOK1_DP_P[28]	AB27	ZDOK1_DP_P28	6-5L
ZDOK1_DP_N[28]	AC27	ZDOK1_DP_N28	6-5L
ZDOK1_DP_P[27]	AD30	ZDOK1_DP_P27	6-5L
ZDOK1_DP_N[27]	AC29	ZDOK1_DP_N27	6-5L
ZDOK1_DP_P[26]	AE29	ZDOK1_DP_P26	6-6L
ZDOK1_DP_N[26]	AD29	ZDOK1_DP_N26	6-6L
ZDOK1_DP_P[25]	AG33	ZDOK1_DP_P25	6-6L
ZDOK1_DP_N[25]	AH33	ZDOK1_DP_N25	6-6L
ZDOK1_DP_P[24]	AF29	ZDOK1_DP_P24	6-6L
ZDOK1_DP_N[24]	AF30	ZDOK1_DP_N24	6-6L
ZDOK1_DP_P[23]	AG27	ZDOK1_DP_P23	6-6L
ZDOK1_DP_N[23]	AG26	ZDOK1_DP_N23	6-6L
ZDOK1_DP_P[22]	AK34	ZDOK1_DP_P22	6-6L
ZDOK1_DP_N[22]	AK33	ZDOK1_DP_N22	6-6L
ZDOK1_DP_P[21]	AL34	ZDOK1_DP_P21	6-7L
ZDOK1_DP_N[21]	AL33	ZDOK1_DP_N21	6-7L
ZDOK1_DP_P[20]	AJ25	ZDOK1_DP_P20	6-7L
ZDOK1_DP_N[20]	AH25	ZDOK1_DP_N20	6-7L
ZDOK1_DP_P[19]	AB30	ZDOK1_DP_P19	6-3J
ZDOK1_DP_N[19]	AC30	ZDOK1_DP_N19	6-3J
ZDOK1_DP_P[18]	AC28	ZDOK1_DP_P18	6-3J
ZDOK1_DP_N[18]	AD27	ZDOK1_DP_N18	6-3J
ZDOK1_DP_P[17]	AC25	ZDOK1_DP_P17	6-3J
ZDOK1_DP_N[17]	AC24	ZDOK1_DP_N17	6-3J
ZDOK1_DP_P[16]	AE28	ZDOK1_DP_P16	6-4J
ZDOK1_DP_N[16]	AF28	ZDOK1_DP_N16	6-4J
ZDOK1_DP_P[15]	AD24	ZDOK1_DP_P15	6-4J
ZDOK1_DP_N[15]	AE24	ZDOK1_DP_N15	6-4J
ZDOK1_DP_P[14]	AF25	ZDOK1_DP_P14	6-4J
ZDOK1_DP_N[14]	AF26	ZDOK1_DP_N14	6-4J
ZDOK1_DP_P[13]	AH29	ZDOK1_DP_P13	6-4J
ZDOK1_DP_N[13]	AG30	ZDOK1_DP_N13	6-4J
ZDOK1_DP_P[12]	AH27	ZDOK1_DP_P12	6-4J
ZDOK1_DP_N[12]	AJ26	ZDOK1_DP_N12	6-4J
ZDOK1_DP_P[11]	AM33	ZDOK1_DP_P11	6-5J
ZDOK1_DP_N[11]	AM32	ZDOK1_DP_N11	6-5J
ZDOK1_DP_P[10]	AN32	ZDOK1_DP_P10	6-5J
ZDOK1_DP_N[10]	AP32	ZDOK1_DP_N10	6-5J
ZDOK1_DP_P[9]	AC34	ZDOK1_DP_P9	6-5J
ZDOK1_DP_N[9]	AD34	ZDOK1_DP_N9	6-5J
ZDOK1_DP_P[8]	AD32	ZDOK1_DP_P8	6-5J
ZDOK1_DP_N[8]	AE32	ZDOK1_DP_N8	6-5J
ZDOK1_DP_P[7]	AF34	ZDOK1_DP_P7	6-5J
ZDOK1_DP_N[7]	AE34	ZDOK1_DP_N7	6-5J
ZDOK1_DP_P[6]	AD26	ZDOK1_DP_P6	6-6J
ZDOK1_DP_N[6]	AD25	ZDOK1_DP_N6	6-6J
ZDOK1_DP_P[5]	AE27	ZDOK1_DP_P5	6-6J
ZDOK1_DP_N[5]	AE26	ZDOK1_DP_N5	6-6J
ZDOK1_DP_P[4]	AH34	ZDOK1_DP_P4	6-6J
ZDOK1_DP_N[4]	AJ34	ZDOK1_DP_N4	6-6J
ZDOK1_DP_P[3]	AJ32	ZDOK1_DP_P3	6-6J
ZDOK1_DP_N[3]	AK32	ZDOK1_DP_N3	6-6J
ZDOK1_DP_P[2]	AJ31	ZDOK1_DP_P2	6-6J
ZDOK1_DP_N[2]	AK31	ZDOK1_DP_N2	6-6J
ZDOK1_DP_P[1]	AK29	ZDOK1_DP_P1	6-7J
ZDOK1_DP_N[1]	AJ29	ZDOK1_DP_N1	6-7J
ZDOK1_DP_P[0]	AN34	ZDOK1_DP_P0	6-7J
ZDOK1_DP_N[0]	AN33	ZDOK1_DP_N0	6-7J

BANKS=11, 13, 15, 17, 19, 21

5V
3V3
2V5
1V8

C337 1UF 16V
C336 100NF 10V
C339 1UF 16V
C338 100NF 10V
C340 1UF 16V
C341 100NF 10V
C343 1UF 16V
C342 100NF 10V

P7

W1	W1	B1	B1
X1	X1	B2	B2
Y1	Y1	B3	B3
Z1	Z1	B4	B4
W2	W2	B5	B5
X2	X2	B6	B6
Y2	Y2	B7	B7
Z2	Z2	B8	B8
W3	W3	B9	B9
X3	X3	B10	B10
Y3	Y3	B11	B11
Z3	Z3	B12	B12
W4	W4	B13	B13
X4	X4	B14	B14
Y4	Y4	B15	B15
Z4	Z4	B16	B16
W5	W5	B17	B17
X5	X5	B18	B18
Y5	Y5	B19	B19
Z5	Z5	B20	B20
W6	W6	E1	E1
X6	X6	E2	E2
Y6	Y6	E3	E3
Z6	Z6	E4	E4
		E5	E5
		E6	E6
		E7	E7
		E8	E8
		E9	E9
		E10	E10
		E11	E11
		E12	E12
		E13	E13
		E14	E14
		E15	E15
		E16	E16
		E17	E17
		E18	E18
		E19	E19
		E20	E20

6367550-5

ZDOK40

P7

6-0E	ZDOK1_DP_P0	A1	A1	C1	ZDOK1_DP_P20
6-0E	ZDOK1_DP_N0	A2	A2	C2	ZDOK1_DP_N20
6-0E	ZDOK1_DP_P1	A3	A3	C3	ZDOK1_DP_P21
6-0E	ZDOK1_DP_N1	A4	A4	C4	ZDOK1_DP_N21
6-0E	ZDOK1_DP_P2	A5	A5	C5	ZDOK1_DP_P22
6-0E	ZDOK1_DP_N2	A6	A6	C6	ZDOK1_DP_N22
6-1E	ZDOK1_DP_P3	A7	A7	C7	ZDOK1_DP_P23
6-1E	ZDOK1_DP_N3	A8	A8	C8	ZDOK1_DP_N23
6-1E	ZDOK1_DP_P4	A9	A9	C9	ZDOK1_DP_P24
6-1E	ZDOK1_DP_N4	A10	A10	C10	ZDOK1_DP_N24
6-1E	ZDOK1_DP_P5	A11	A11	C11	ZDOK1_DP_P25
6-1E	ZDOK1_DP_N5	A12	A12	C12	ZDOK1_DP_N25
6-1E	ZDOK1_DP_P6	A13	A13	C13	ZDOK1_DP_P26
6-1E	ZDOK1_DP_N6	A14	A14	C14	ZDOK1_DP_N26
6-1E	ZDOK1_DP_P7	A15	A15	C15	ZDOK1_DP_P27
6-1E	ZDOK1_DP_N7	A16	A16	C16	ZDOK1_DP_N27
6-2E	ZDOK1_DP_P8	A17	A17	C17	ZDOK1_DP_P28
6-2E	ZDOK1_DP_N8	A18	A18	C18	ZDOK1_DP_N28
6-2E	ZDOK1_DP_P9	A19	A19	C19	ZDOK1_CLK0_P 6-7B
6-2E	ZDOK1_DP_N9	A20	A20	C20	ZDOK1_CLK0_N 6-7B
6-2E	ZDOK1_DP_P10	D1	D1	F1	ZDOK1_DP_P29 6-6E
6-2E	ZDOK1_DP_N10	D2	D2	F2	ZDOK1_DP_N29 6-6E
6-2E	ZDOK1_DP_P11	D3	D3	F3	ZDOK1_DP_P30 6-6E
6-2E	ZDOK1_DP_N11	D4	D4	F4	ZDOK1_DP_N30 6-6E
6-2E	ZDOK1_DP_P12	D5	D5	F5	ZDOK1_DP_P31 6-6E
6-2E	ZDOK1_DP_N12	D6	D6	F6	ZDOK1_DP_N31 6-6E
6-3E	ZDOK1_DP_P13	D7	D7	F7	ZDOK1_DP_P32 6-6E
6-3E	ZDOK1_DP_N13	D8	D8	F8	ZDOK1_DP_N32 6-6E
6-3E	ZDOK1_DP_P14	D9	D9	F9	ZDOK1_DP_P33 6-7E
6-3E	ZDOK1_DP_N14	D10	D10	F10	ZDOK1_DP_N33 6-7E
6-3E	ZDOK1_DP_P15	D11	D11	F11	ZDOK1_DP_P34 6-7E
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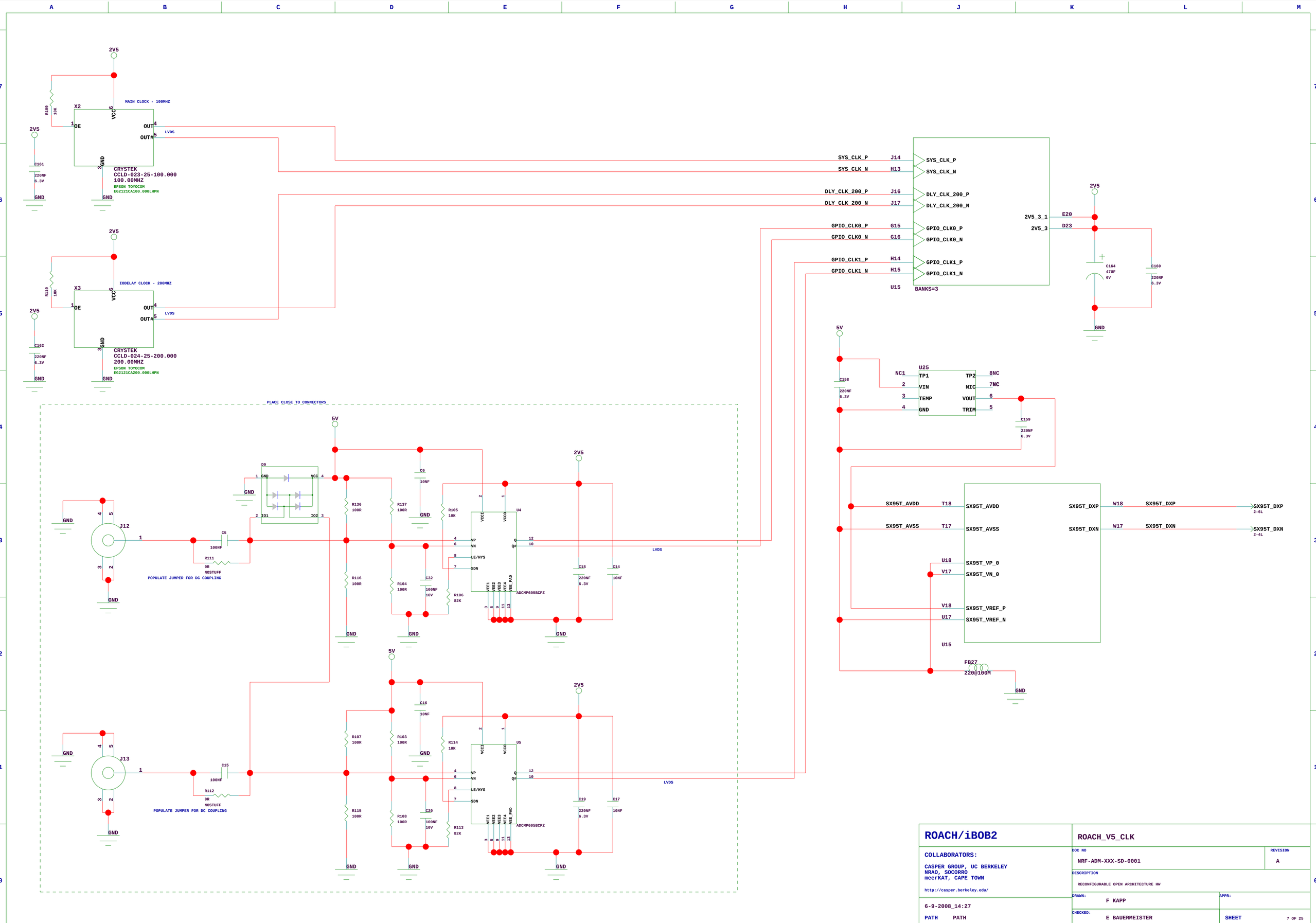
6-3E	ZDOK1_DP_P16	D13	D13	F13	ZDOK1_DP_P35 6-7E
6-3E	ZDOK1_DP_N16	D14	D14	F14	ZDOK1_DP_N35 6-7E
6-3E	ZDOK1_DP_P17	D15	D15	F15	ZDOK1_DP_P36 6-7E
6-3E	ZDOK1_DP_N17	D16	D16	F16	ZDOK1_DP_N36 6-7E
6-4E	ZDOK1_DP_P18	D17	D17	F17	ZDOK1_DP_P37 6-7E
6-4E	ZDOK1_DP_N18	D18	D18	F18	ZDOK1_DP_N37 6-7E
6-4E	ZDOK1_DP_P19	D19	D19	F19	ZDOK1_CLK1_P 6-7B
6-4E	ZDOK1_DP_N19	D20	D20	F20	ZDOK1_CLK1_N 6-7B

6367550-5

ROACH/iBOB2	**ROACH_ADC_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 6 OF 25
6-9-2008_14:27 PATH PATH	



ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

6-9-2008_14:27

PATH PATH

ROACH_V5_CLK

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

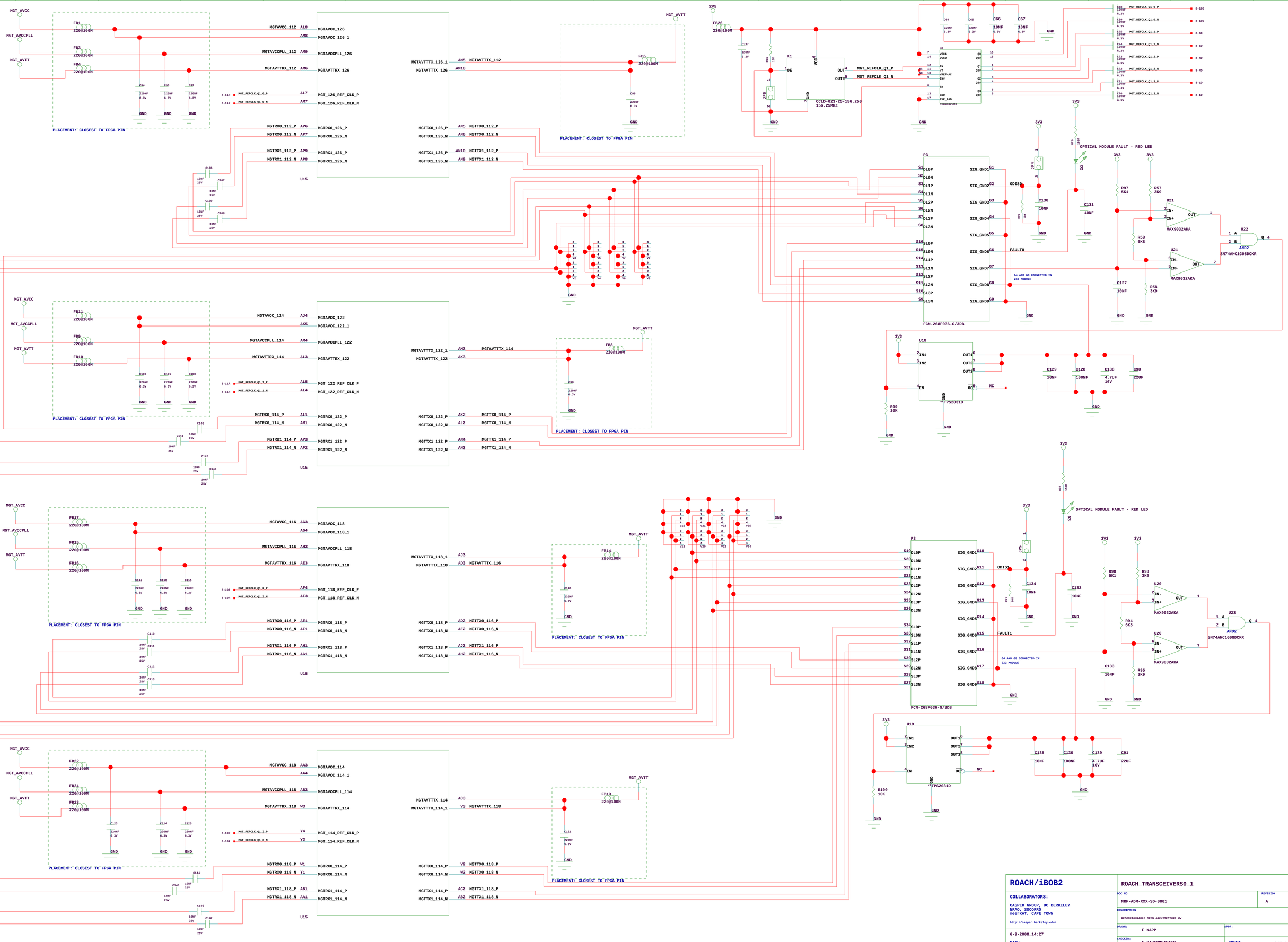
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 7 OF 25



ROACH/iBOB2	**ROACH_TRANSCEIVERS0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-9-2008_14:27	DRAWN: F KAPP
PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET: 8 OF 25

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

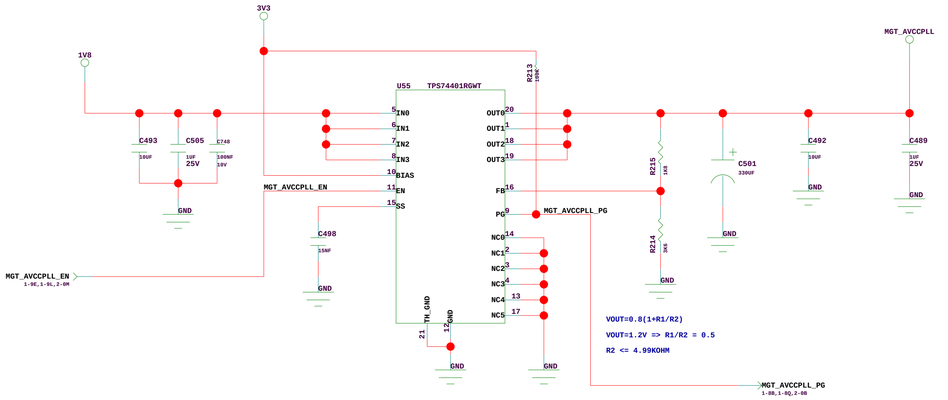
G4 AND G8 CONNECTED IN 2X2 MODULE

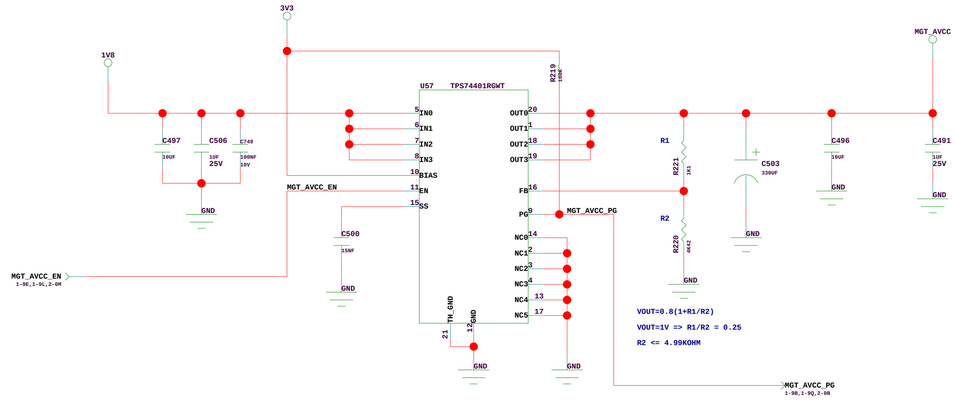
OPTICAL MODULE FAULT - RED LED

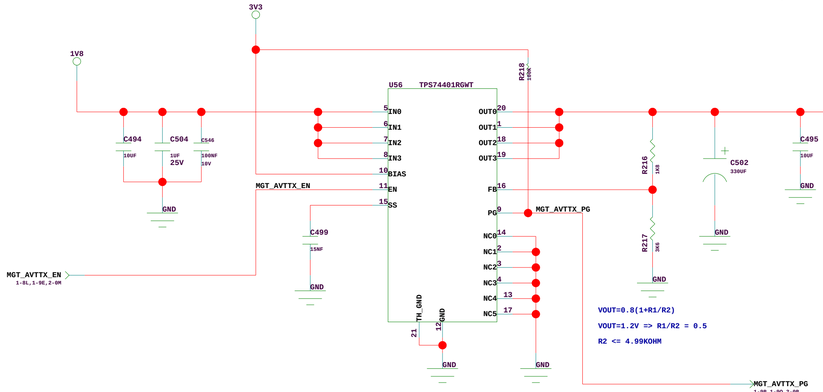
CCLD-023-25-156.250 156.25MHZ

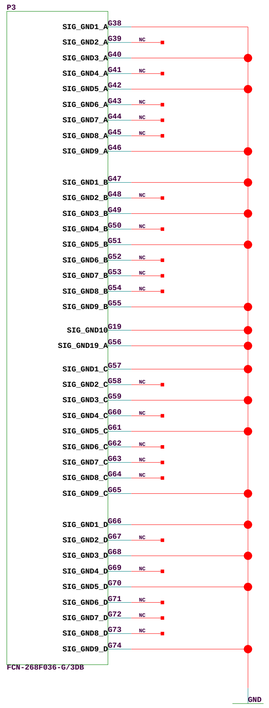
FCN-268F036-G/3DB

ROACH/iBOB2	ROACH_TRANSCEIVERS2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-9-2008_14:27	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 9 OF 25

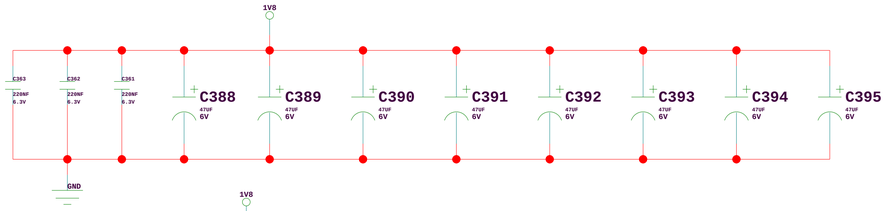


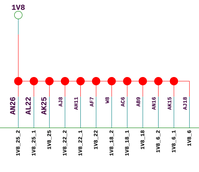


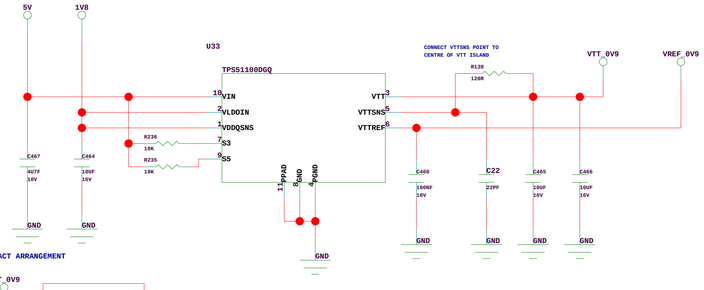




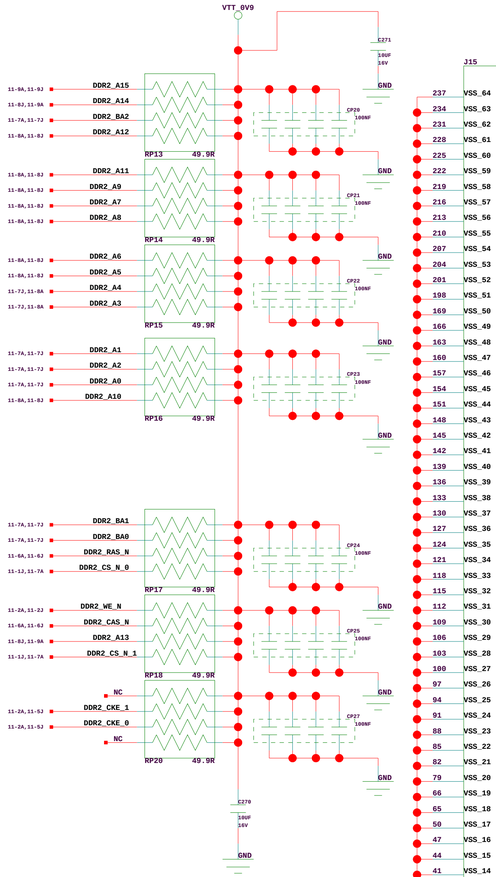
ROACH/iBOB2	**ROACH_TRANSCEIVERS_PSU**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 10 OF 25
6-9-2008_14:27 PATH PATH	

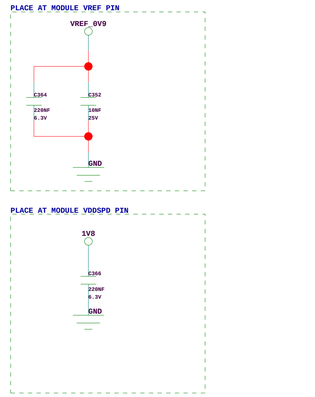


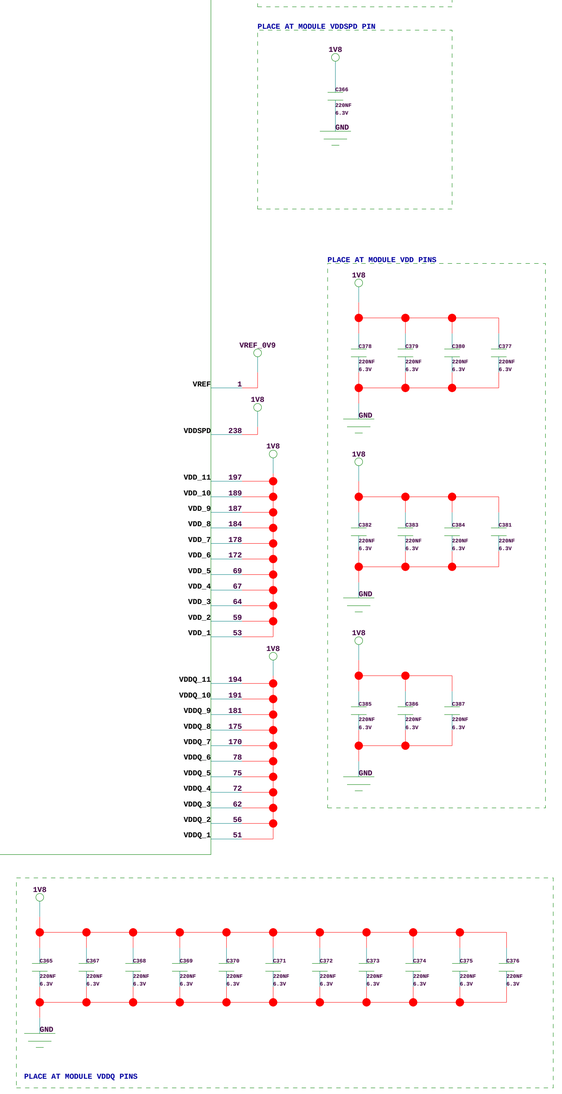


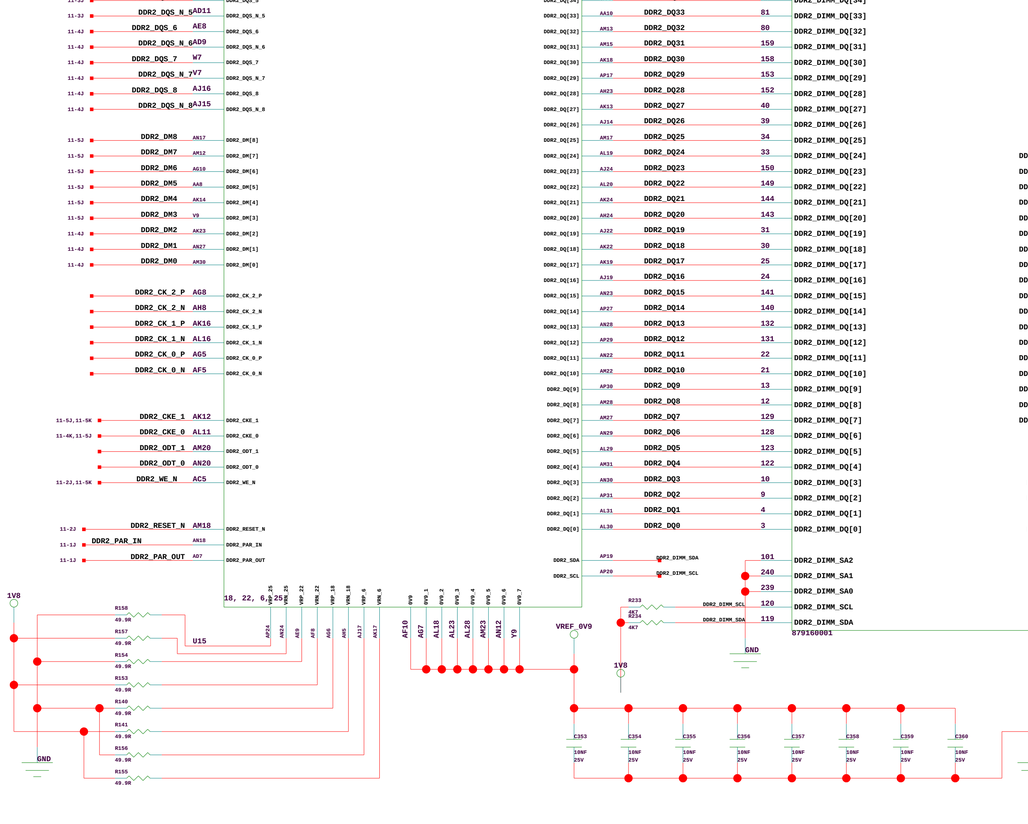


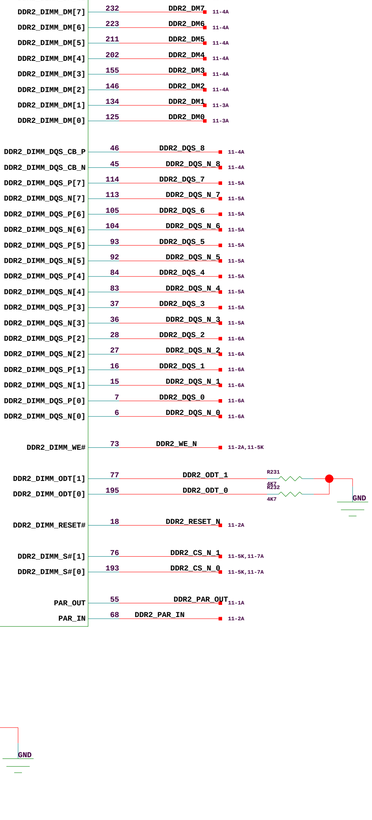
VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
PLACE ONE 10uF CAPACITOR ON EITHER END OF ISLAND











ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

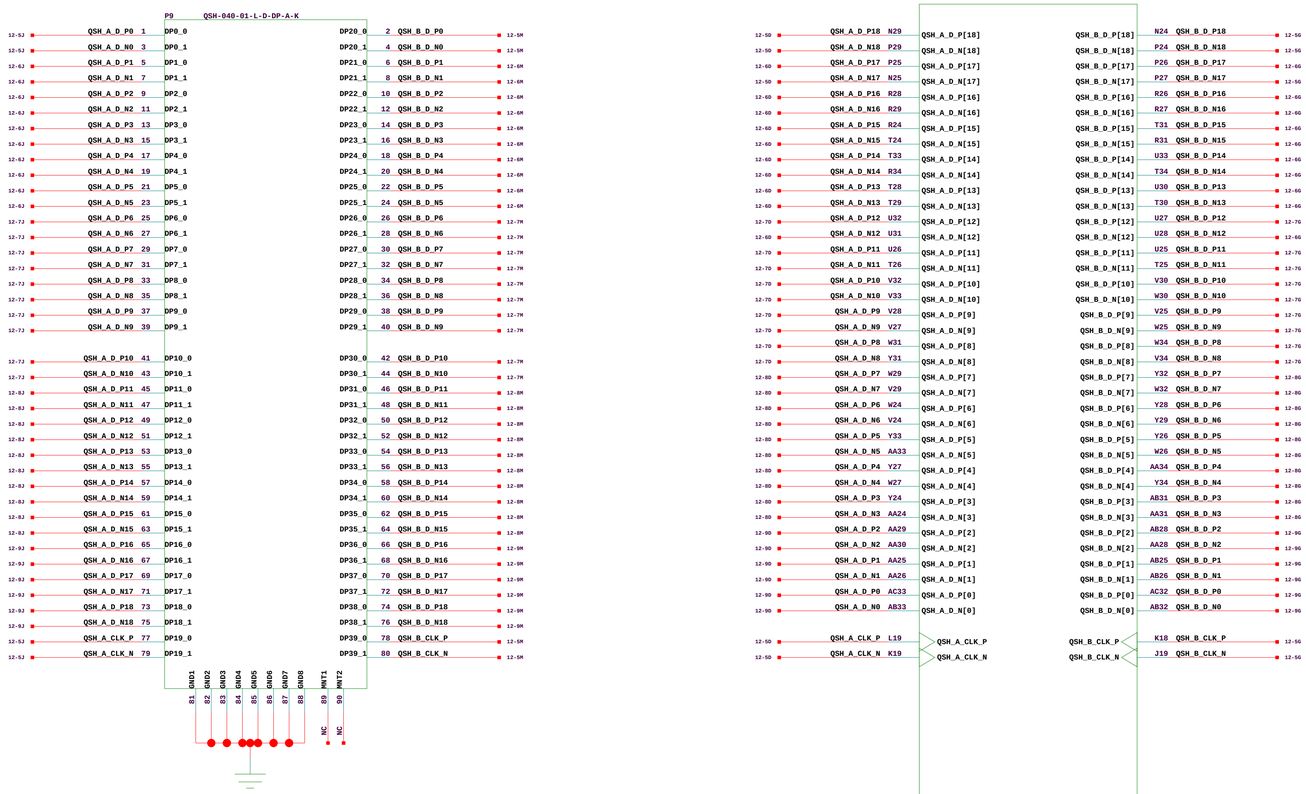
http://casper.berkeley.edu/

6-9-2008_14:27

PATH PATH

ROACH_DDR2_DIMM

DOC NO: NRF-ADM-XXX-SD-0001
REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE NW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 11 OF 25



ROACH/iBOB2

ROACH_DIFF_GPIO

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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6-9-2008_14:27

PATH PATH

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

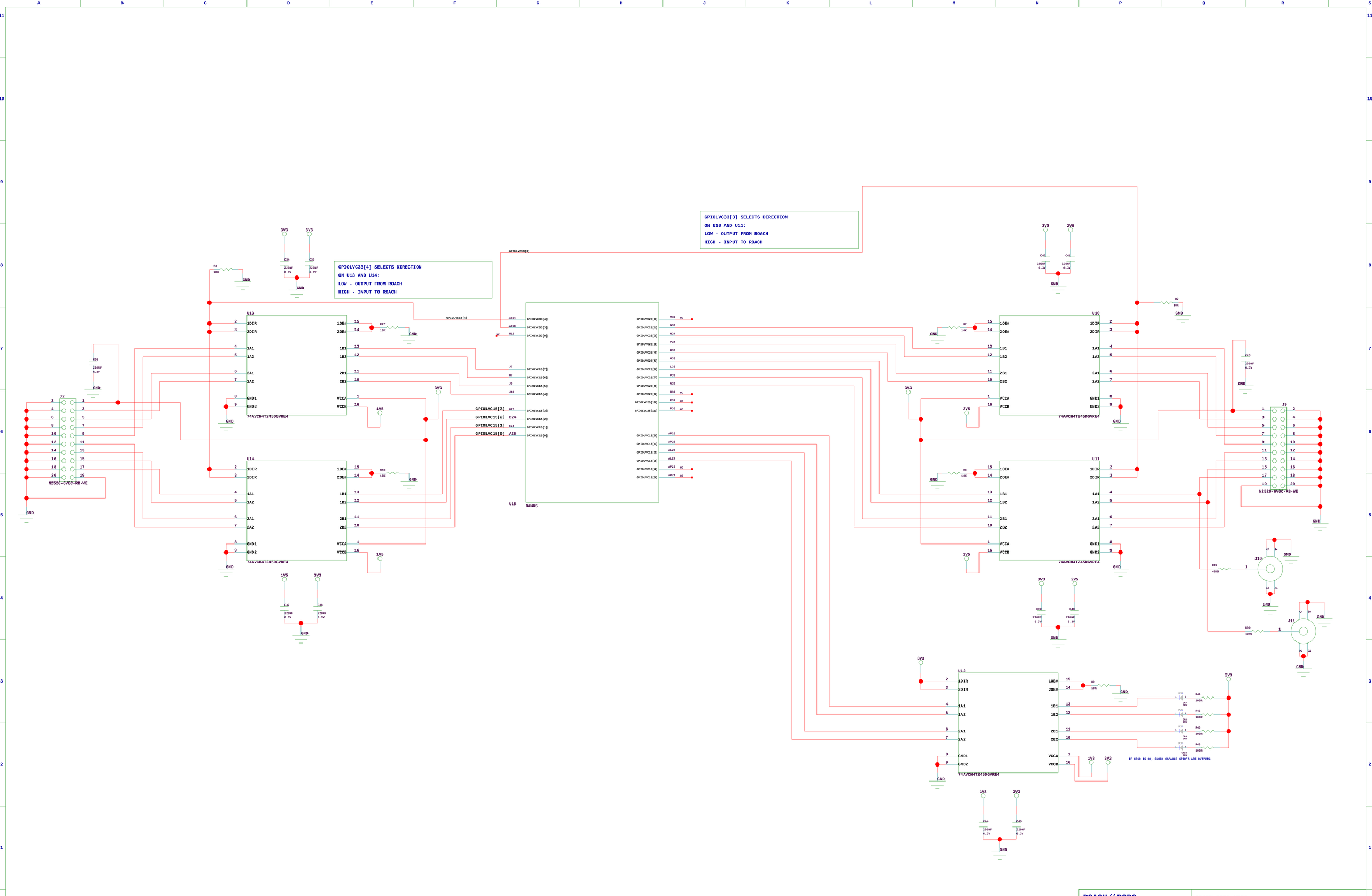
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW

DRAWN: F KAPP

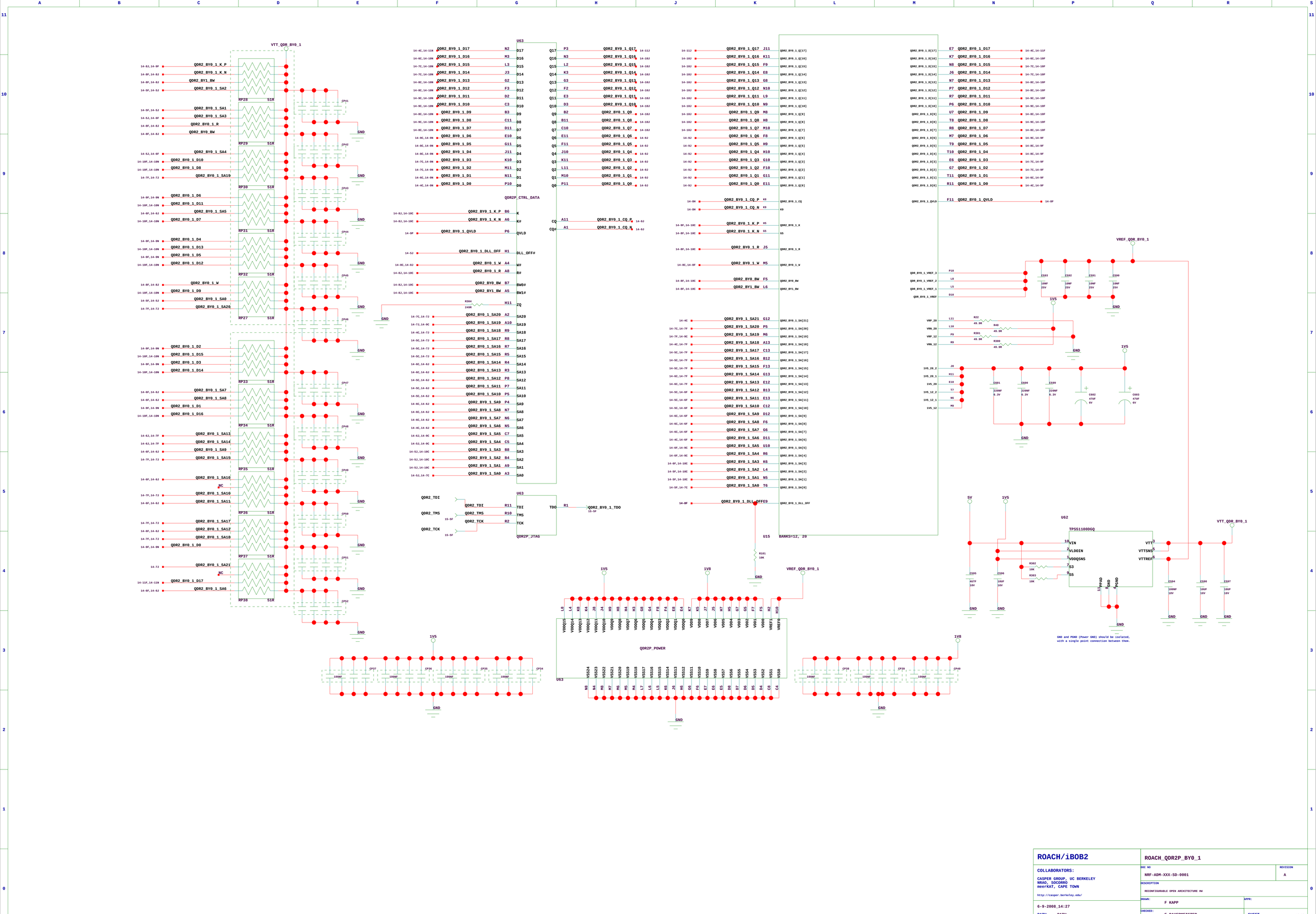
APPR:

CHECKED: E BAUERMEISTER

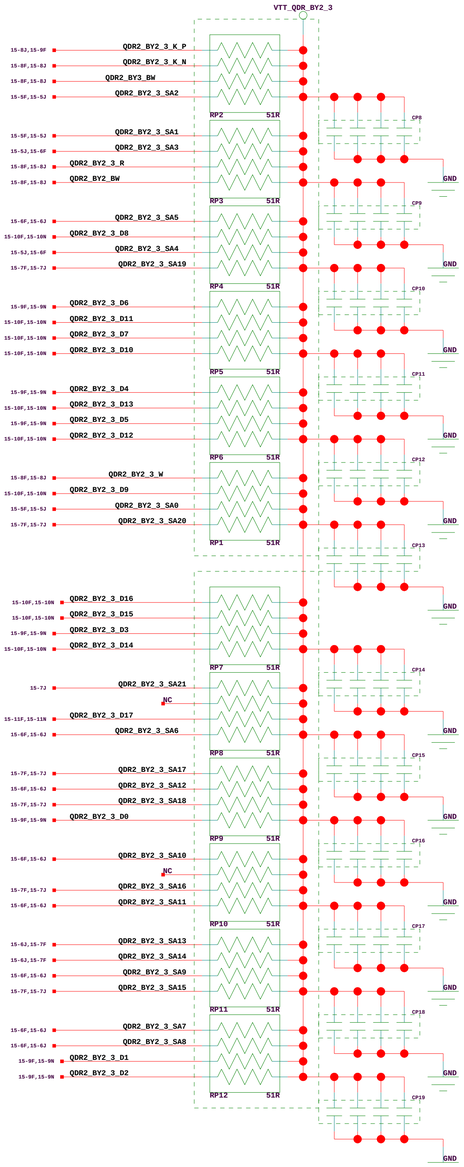
SHEET 12 OF 25

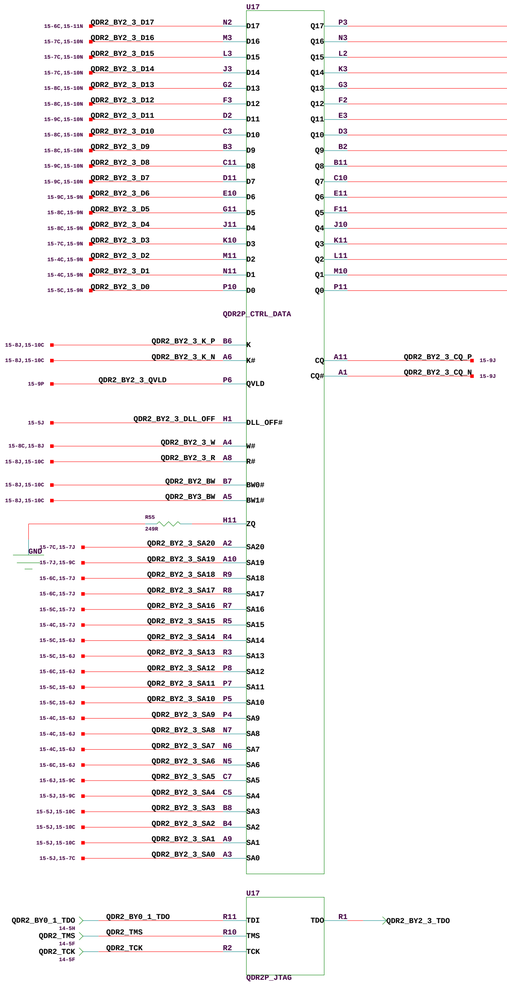


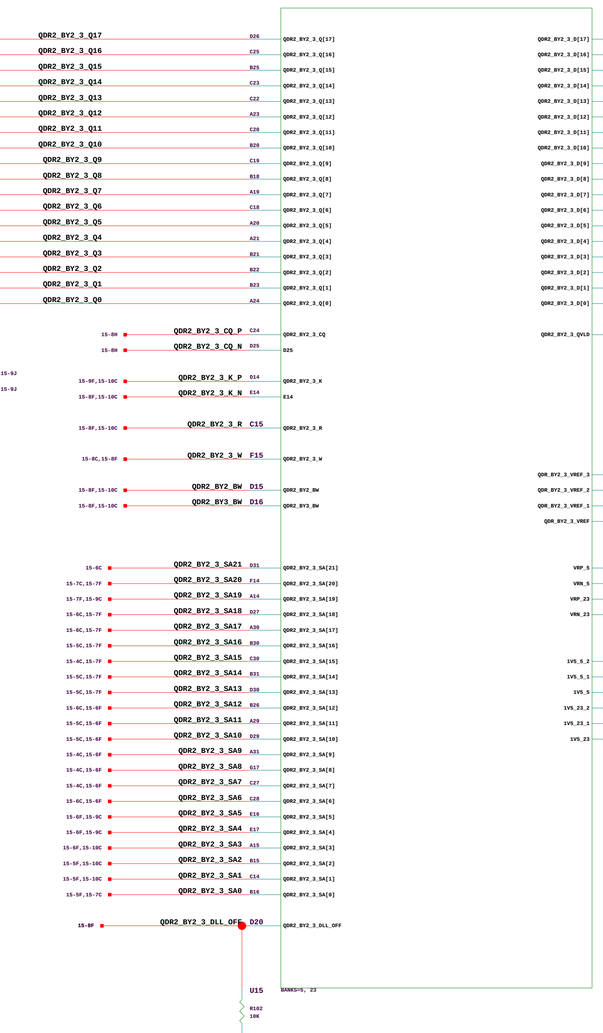
ROACH/iBOB2	**ROACH_GPIO_MISC**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-9-2008_14:27 PATH PATH	DRAWN: F KAPP — APPR:
	CHECKED: E BAUERMEISTER — SHEET 13 OF 25

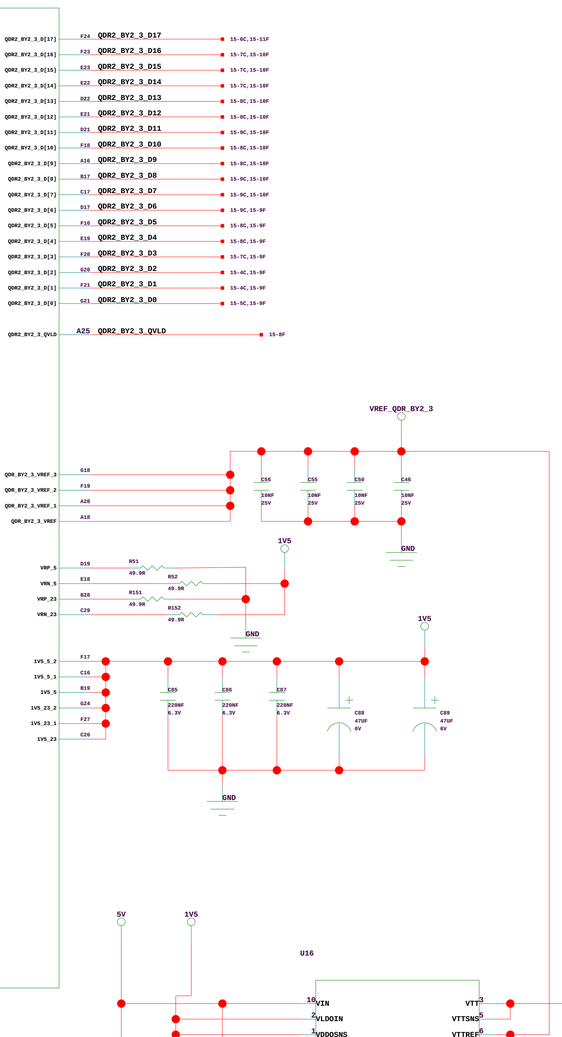


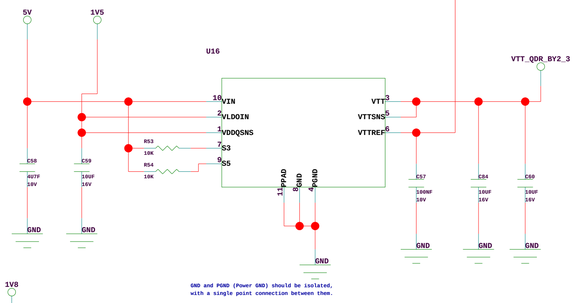
ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP CHECKED: E BAUERMEISTER APPR:
6-9-2008_14:27 PATH PATH	SHEET 14 OF 25

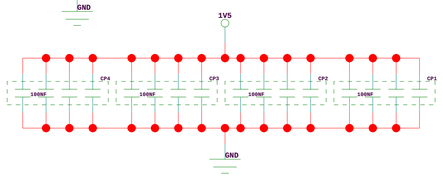


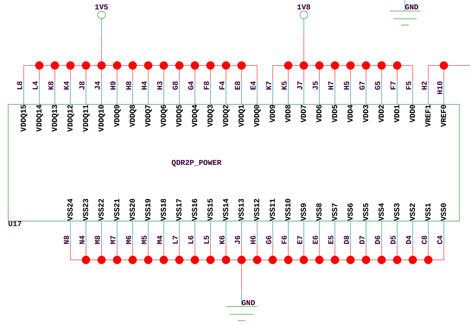


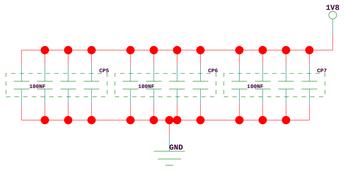








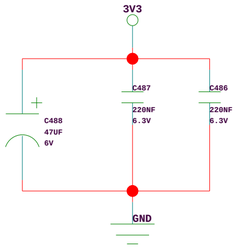


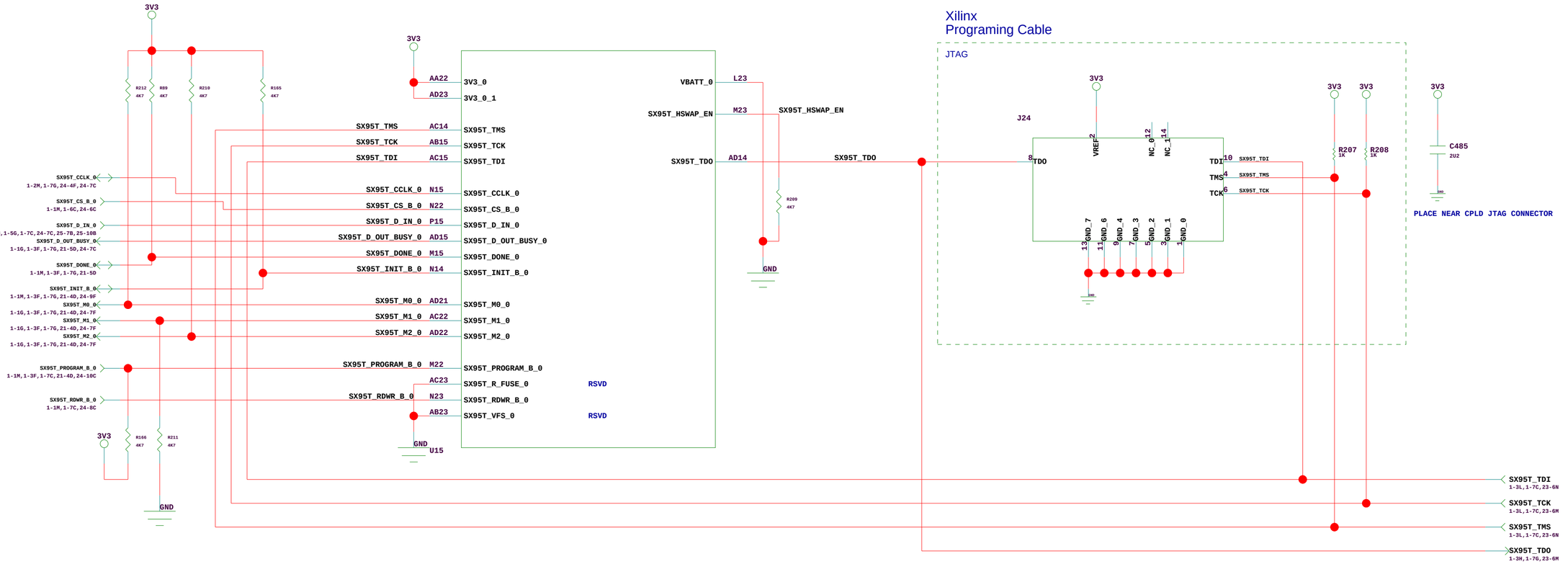


ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-9-2008_14:27	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 15 OF 25

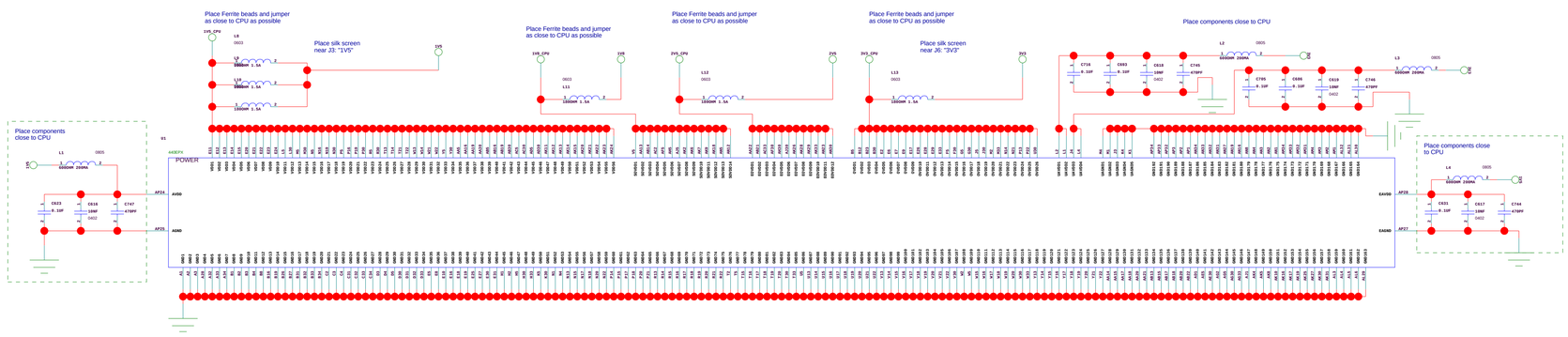
TBD

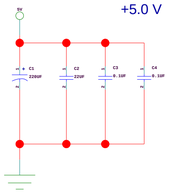
VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

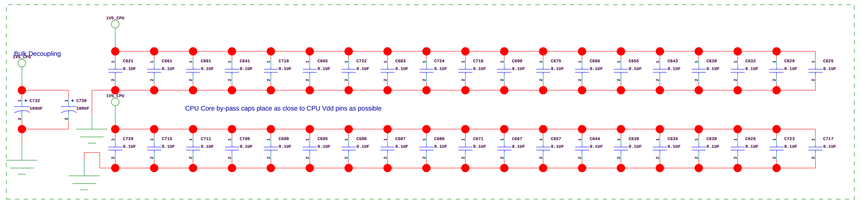


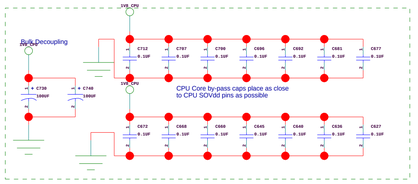


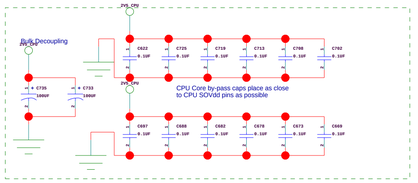
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
6-9-2008_14:27 PATH PATH	

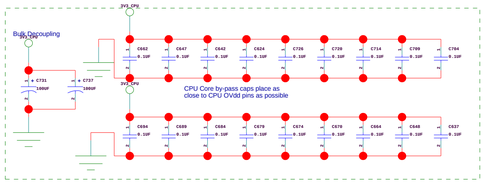


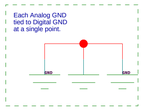










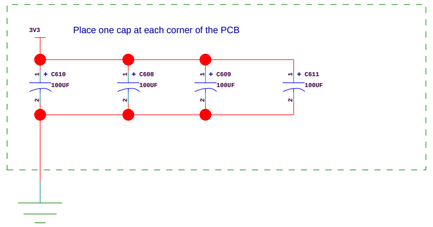


REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: **CASPER GROUP, UC BERKELEY** **NRAO, SOCORRO** **meerKAT, CAPE TOWN** http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MK
6-9-2008_14:27 PATH PATH	DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET 17 OF 25

REMOVED 3V3 GENERATION



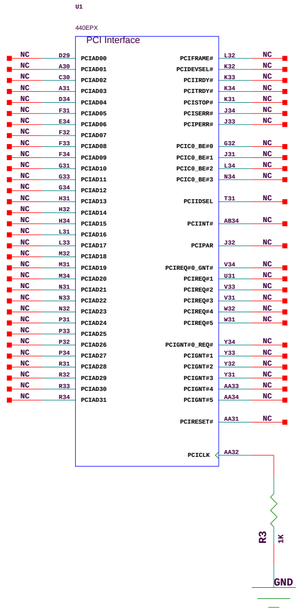
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET 18 OF 25
6-9-2008_14:27 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-9-2008_14:27 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

Place nearest PHY pin 96

Place nearest PHY pin 101

Place nearest PHY pin 98

Place nearest PHY pin 100

Place as close to PHY CORE VDD power pins as possible

Place as close to PHY IO VDD power pins as possible

Gig-Ethernet RGMII1

UNUSED SECOND ETHERNET MAC

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups. Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

Place resistors as close to CPU as possible and keep all traces lengths equal

Gig-Ethernet RGMII0

ETHERNET Mgt.

Place resistors close to PHY all trace lengths equal

Place jumpers in line with signals

Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5

Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

Bottom LED
Green/Toggle = ACTIVITY

HFJ11-1G02E-L12

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

NOSTUFF

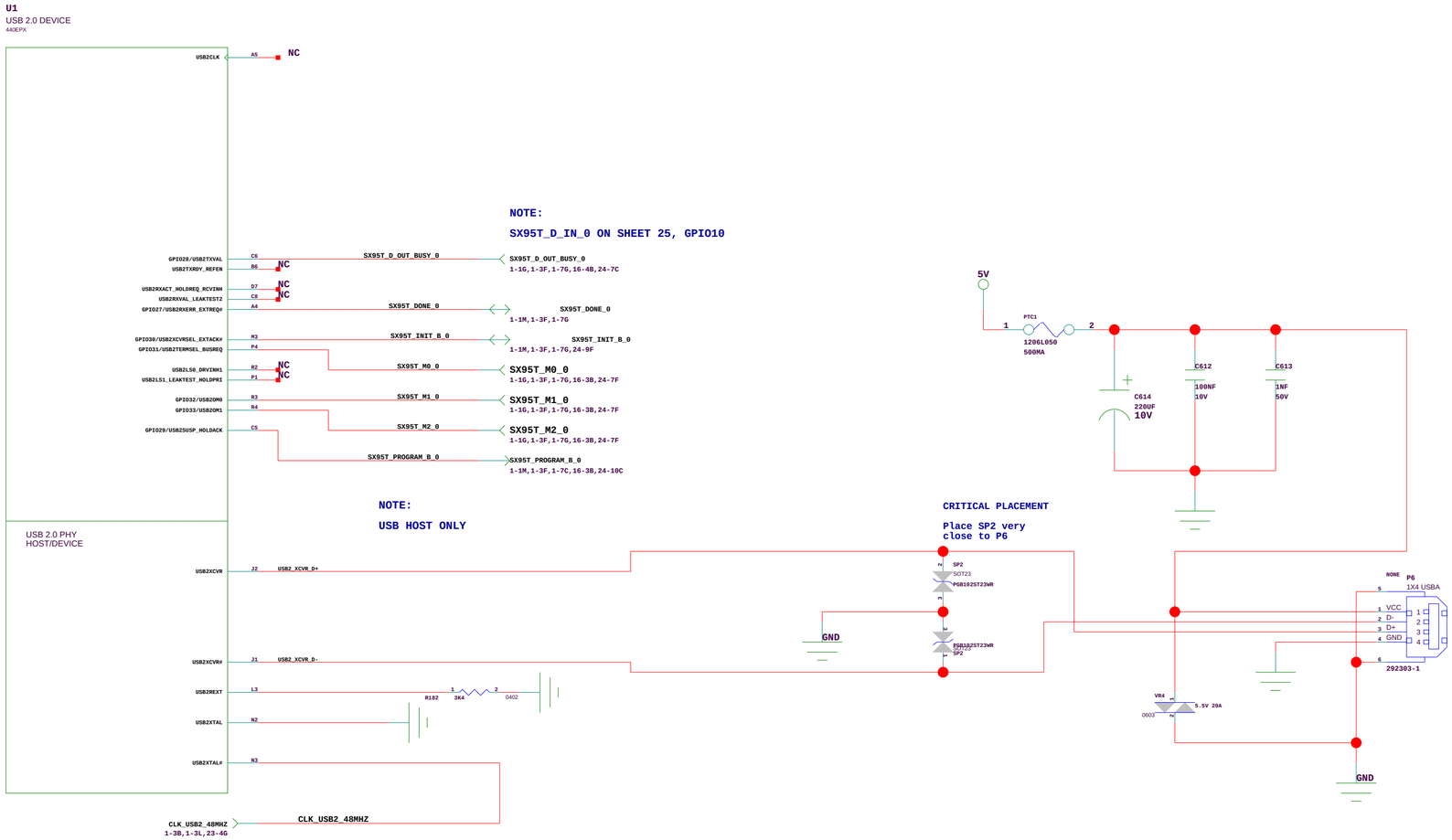
DUPLEX LED

L10 LED

L100 LED

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

ROACH/iBOB2	**ROACH_PPC_ETH1**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-9-2008_14:27	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 20 OF 25



ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25
6-9-2008_14:27 PATH PATH	

DDR_PA[15:0]

DDR_PD[63:0]

U1

DDR SDRAM

44OEPX

DDR_PD0	AB2	MEMDATA00	MEMADDR00
DDR_PD1	AF2	MEMDATA01	MEMADDR01
DDR_PD2	AK5	MEMDATA02	MEMADDR02
DDR_PD3	AL28	MEMDATA03	MEMADDR03
DDR_PD4	AL22	MEMDATA04	MEMADDR04
DDR_PD5	AK22	MEMDATA05	MEMADDR05
DDR_PD6	AK21	MEMDATA06	MEMADDR06
DDR_PD7	AF21	MEMDATA07	MEMADDR07
DDR_PD8	AF28	MEMDATA08	MEMADDR08
DDR_PD9	AL18	MEMDATA09	MEMADDR09
DDR_PD10	AK17	MEMDATA10	MEMADDR10
DDR_PD11	AF17	MEMDATA11	MEMADDR11
DDR_PD12	AK26	MEMDATA12	MEMADDR12
DDR_PD13	AF18	MEMDATA13	MEMADDR13
DDR_PD14	AK18	MEMDATA14	
DDR_PD15	AF16	MEMDATA15	BA0
DDR_PD16	AK16	MEMDATA16	BA1
DDR_PD17	AF15	MEMDATA17	BA2
DDR_PD18	AL15	MEMDATA18	
DDR_PD19	AF14	MEMDATA19	RAS#
DDR_PD20	AL17	MEMDATA20	CAS#
DDR_PD21	AK17	MEMDATA21	WE#
DDR_PD22	AK15	MEMDATA22	
DDR_PD23	AK15	MEMDATA23	DM0
DDR_PD24	AF13	MEMDATA24	DM1
DDR_PD25	AK13	MEMDATA25	DM2
DDR_PD26	AF12	MEMDATA26	DM3
DDR_PD27	AL12	MEMDATA27	DM4
DDR_PD28	AK14	MEMDATA28	DM5
DDR_PD29	AK14	MEMDATA29	DM6
DDR_PD30	AL13	MEMDATA30	DM7
DDR_PD31	AK12	MEMDATA31	DM8
DDR_PD32	AF3	MEMDATA32	
DDR_PD33	AF1	MEMDATA33	DQS0
DDR_PD34	AD4	MEMDATA34	DQS1
DDR_PD35	AD3	MEMDATA35	DQS2
DDR_PD36	AB3	MEMDATA36	DQS3
DDR_PD37	AF2	MEMDATA37	DQS4
DDR_PD38	AE2	MEMDATA38	DQS5
DDR_PD39	AE1	MEMDATA39	DQS6
DDR_PD40	AC3	MEMDATA40	DQS7
DDR_PD41	AC1	MEMDATA41	DQS8
DDR_PD42	AA4	MEMDATA42	
DDR_PD43	AA3	MEMDATA43	MEMDT0
DDR_PD44	AD2	MEMDATA44	MEMDT1
DDR_PD45	AC4	MEMDATA45	
DDR_PD46	AB1	MEMDATA46	BANKSEL#0
DDR_PD47	AB2	MEMDATA47	BANKSEL#1
DDR_PD48	Y3	MEMDATA48	
DDR_PD49	Y2	MEMDATA49	MEMCLKEN
DDR_PD50	Y4	MEMDATA50	
DDR_PD51	V3	MEMDATA51	MEMCLKOUT
DDR_PD52	AA2	MEMDATA52	
DDR_PD53	AA1	MEMDATA53	MEMCLKOUT#
DDR_PD54	W3	MEMDATA54	
DDR_PD55	W1	MEMDATA55	
DDR_PD56	V1	MEMDATA56	
DDR_PD57	U2	MEMDATA57	
DDR_PD58	T4	MEMDATA58	
DDR_PD59	R1	MEMDATA59	
DDR_PD60	V3	MEMDATA60	
DDR_PD61	V1	MEMDATA61	
DDR_PD62	T3	MEMDATA62	
DDR_PD63	T1	MEMDATA63	

		SVREF1A	
	AL10	SVREF1B	
	AF4	SVREF2A	
	AL19	SVREF2B	

DDR_PA0	AM5	MEMADDR00	
DDR_PA1	AP4	MEMADDR01	
DDR_PA2	AP5	MEMADDR02	
DDR_PA3	AM6	MEMADDR03	
DDR_PA4	AP6	MEMADDR04	
DDR_PA5	AN6	MEMADDR05	
DDR_PA6	AL7	MEMADDR06	
DDR_PA7	AN7	MEMADDR07	
DDR_PA8	AM7	MEMADDR08	
DDR_PA9	AP7	MEMADDR09	
DDR_PA10	AL2	MEMADDR10	
DDR_PA11	AL8	MEMADDR11	
DDR_PA12	AN3	MEMADDR12	
DDR_PA13	AN4	MEMADDR13	
DDR_PBA0	AJ3		
DDR_PBA1	AN3		
DDR_PBA2	AP8		
DDR_PRAS#	AJ4		
DDR_PCAS#	AN4		
DDR_PWE#	AJ2		
DDR_PDM0	AL21		
DDR_PDM1	AP18		
DDR_PDM2	AP15		
DDR_PDM3	AL14		
DDR_PDM4	AD4		
DDR_PDM5	AB3		
DDR_PDM6	Y3		
DDR_PDM7	Y2		
DDR_PDM8	AP10		
DDR_PODT0	AN3		
DDR_PODT1	AN1		
DDR_PCS0#	AN2		
DDR_PCS1#	AM1		
DDR_PCKE	AN9		
DDR_CLKOUT	AL1		
DDR_CLKOUT#	AM1		

PPC_ECC0	AM11	ECC0	
PPC_ECC1	AL11	ECC1	
PPC_ECC2	AN9	ECC2	
PPC_ECC3	AL9	ECC3	
PPC_ECC4	AM11	ECC4	
PPC_ECC5	AN11	ECC5	
PPC_ECC6	AM10	ECC6	
PPC_ECC7	AP9	ECC7	

Place parts as close to CPU as possible

5V

1V8

DDR_VREF_0V9

DDR_VTT

U32

TPS51100DGQ

R230 10K

R229 10K

R6 120R

C459 4U7F 10V

C456 10UF 16V

C453 100NF 10V

C21 22PF

C457 10UF 16V

C458 10UF 16V

C155 100NF 10V

C154 100NF 10V

C152 100NF 10V

C148 10NF 0402

C149 0.1UF 0402

C151 0.1UF 0402

C150 0.1UF 0402

DDR2 Clock line must be 500ps longer than Address/Command lines
To compensate for additional loading when using unbuffered DIMM's
See P84 of PPC440EPx for more information

J8

DDR2_DIMM

PPC_ECC7	22-6D	168	DDR2_DIMM_CB7
PPC_ECC6	22-6D	167	DDR2_DIMM_CB6
PPC_ECC5	22-7D	162	DDR2_DIMM_CB5
PPC_ECC4	22-7D	161	DDR2_DIMM_CB4
PPC_ECC3	22-7D	49	DDR2_DIMM_CB3
PPC_ECC2	22-7D	48	DDR2_DIMM_CB2
PPC_ECC1	22-7D	43	DDR2_DIMM_CB1
PPC_ECC0	22-7D	42	DDR2_DIMM_CB0
DDR_PDQ63		236	DDR2_DIMM_DQ[63]
DDR_PDQ62		235	DDR2_DIMM_DQ[62]
DDR_PDQ61		230	DDR2_DIMM_DQ[61]
DDR_PDQ60		229	DDR2_DIMM_DQ[60]
DDR_PDQ59		117	DDR2_DIMM_DQ[59]
DDR_PDQ58		116	DDR2_DIMM_DQ[58]
DDR_PDQ57		111	DDR2_DIMM_DQ[57]
DDR_PDQ56		110	DDR2_DIMM_DQ[56]
DDR_PDQ55		227	DDR2_DIMM_DQ[55]
DDR_PDQ54		226	DDR2_DIMM_DQ[54]
DDR_PDQ53		218	DDR2_DIMM_DQ[53]
DDR_PDQ52		217	DDR2_DIMM_DQ[52]
DDR_PDQ51		108	DDR2_DIMM_DQ[51]
DDR_PDQ50		107	DDR2_DIMM_DQ[50]
DDR_PDQ49		99	DDR2_DIMM_DQ[49]
DDR_PDQ48		98	DDR2_DIMM_DQ[48]
DDR_PDQ47		215	DDR2_DIMM_DQ[47]
DDR_PDQ46		214	DDR2_DIMM_DQ[46]
DDR_PDQ45		209	DDR2_DIMM_DQ[45]
DDR_PDQ44		208	DDR2_DIMM_DQ[44]
DDR_PDQ43		96	DDR2_DIMM_DQ[43]
DDR_PDQ42		95	DDR2_DIMM_DQ[42]
DDR_PDQ41		90	DDR2_DIMM_DQ[41]
DDR_PDQ40		89	DDR2_DIMM_DQ[40]
DDR_PDQ39		206	DDR2_DIMM_DQ[39]
DDR_PDQ38		205	DDR2_DIMM_DQ[38]
DDR_PDQ37		200	DDR2_DIMM_DQ[37]
DDR_PDQ36		199	DDR2_DIMM_DQ[36]
DDR_PDQ35		87	DDR2_DIMM_DQ[35]
DDR_PDQ34		86	DDR2_DIMM_DQ[34]
DDR_PDQ33		81	DDR2_DIMM_DQ[33]
DDR_PDQ32		80	DDR2_DIMM_DQ[32]
DDR_PDQ31		159	DDR2_DIMM_DQ[31]
DDR_PDQ30		158	DDR2_DIMM_DQ[30]
DDR_PDQ29		153	DDR2_DIMM_DQ[29]
DDR_PDQ28		152	DDR2_DIMM_DQ[28]
DDR_PDQ27		40	DDR2_DIMM_DQ[27]
DDR_PDQ26		39	DDR2_DIMM_DQ[26]
DDR_PDQ25		34	DDR2_DIMM_DQ[25]
DDR_PDQ24		33	DDR2_DIMM_DQ[24]
DDR_PDQ23		150	DDR2_DIMM_DQ[23]
DDR_PDQ22		149	DDR2_DIMM_DQ[22]
DDR_PDQ21		144	DDR2_DIMM_DQ[21]
DDR_PDQ20		143	DDR2_DIMM_DQ[20]
DDR_PDQ19		31	DDR2_DIMM_DQ[19]
DDR_PDQ18		30	DDR2_DIMM_DQ[18]
DDR_PDQ17		25	DDR2_DIMM_DQ[17]
DDR_PDQ16		24	DDR2_DIMM_DQ[16]
DDR_PDQ15		141	DDR2_DIMM_DQ[15]
DDR_PDQ14		140	DDR2_DIMM_DQ[14]
DDR_PDQ13		132	DDR2_DIMM_DQ[13]
DDR_PDQ12		131	DDR2_DIMM_DQ[12]
DDR_PDQ11		22	DDR2_DIMM_DQ[11]
DDR_PDQ10		21	DDR2_DIMM_DQ[10]
DDR_PDQ9		13	DDR2_DIMM_DQ[9]
DDR_PDQ8		12	DDR2_DIMM_DQ[8]
DDR_PDQ7		129	DDR2_DIMM_DQ[7]
DDR_PDQ6		128	DDR2_DIMM_DQ[6]
DDR_PDQ5		123	DDR2_DIMM_DQ[5]
DDR_PDQ4		122	DDR2_DIMM_DQ[4]
DDR_PDQ3		10	DDR2_DIMM_DQ[3]
DDR_PDQ2		9	DDR2_DIMM_DQ[2]
DDR_PDQ1		4	DDR2_DIMM_DQ[1]
DDR_PDQ0		3	DDR2_DIMM_DQ[0]
		101	DDR2_DIMM_SA2
		240	DDR2_DIMM_SA1
		239	DDR2_DIMM_SA0
		120	DDR2_DIMM_SCL
		119	DDR2_DIMM_SDA

879160001

I2C0_SCLK
1-2B,1-5L,1-9B,2-2P,25-5A

I2C0_SDATA
1-2B,1-5L,1-9C

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA1	22-9D,22-10L
DDR2_DIMM_BA[1]	190	DDR_PBA2	22-8L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-7L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	NC	
DDR2_DIMM_CK_N[2]	221	NC	
DDR2_DIMM_CK_P[1]	137	NC	
DDR2_DIMM_CK_N[1]	138	NC	
DDR2_DIMM_CK_P[0]	185	DDR_CLKOUT	
DDR2_DIMM_CK_N[0]	186	DDR_CLKOUT#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-8D,22-11L
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-8D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-71,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-71,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-71,22-8D
PAR_OUT	55	PPC_DDR2_ERROR	1
PAR_IN	68	PAR_IN	1

R226 4K7

PPC_DDR2_RESET_N
1-2B,1-2M,24-10F

C455 5PF 50V

TP4

TP5

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

DDR_VTT

22-6K,22-8D	DDR_PCKE	RP24
	DDR_PA15	
	DDR_PA14	
22-8K,22-9D	DDR_PBA1	
	DDR_PA12	RP23
	DDR_PA11	
	DDR_PA9	
	NC	
	DDR_PA7	RP22
	DDR_PA8	
	DDR_PA6	
	DDR_PA5	
	DDR_PA4	RP21
	DDR_PA3	
	DDR_PA1	
	DDR_PA2	
22-8K,22-9D	DDR_PA0	RP25
	DDR_PBA2	
	DDR_PA10	
22-8K,22-9D	DDR_PBA0	
22-7K,22-9D	DDR_PRAS#	RP26
22-3K,22-9D	DDR_PWE#	
22-3K,22-9D	DDR_PCS0#	
22-8K,22-9D	DDR_PCAS#	
22-3K,22-8D	DDR_PCS1#	RP19
22-8D	DDR_PODT0	
	DDR_PA13	
22-8D	DDR_PODT1	

CP26 CP28 CP29 CP30 CP32 CP31 CP33

GND

J8

879160001

	237	VSS_64	
	234	VSS_63	
	231	VSS_62	
	228	VSS_61	
	225	VSS_60	
	222	VSS_59	
	219	VSS_58	
	216	VSS_57	
	213	VSS_56	
	210	VSS_55	
	207	VSS_54	
	204	VSS_53	
	201	VSS_52	
	198	VSS_51	
	169	VSS_50	
	166	VSS_49	
	163	VSS_48	
	160	VSS_47	
	157	VSS_46	
	154	VSS_45	
	151	VSS_44	
	148	VSS_43	
	145	VSS_42	
	142	VSS_41	
	139	VSS_40	
	136	VSS_39	
	133	VSS_38	
	130	VSS_37	
	127	VSS_36	
	124	VSS_35	
	121	VSS_34	
	118	VSS_33	
	115	VSS_32	
	112	VSS_31	
	109	VSS_30	
	106	VSS_29	
	103	VSS_28	
	100	VSS_27	
	97	VSS_26	
	94	VSS_25	
	91	VSS_24	
	88	VSS_23	
	85	VSS_22	
	82	VSS_21	
	79	VSS_20	
	66	VSS_19	
	65	VSS_18	
	50	VSS_17	
	47	VSS_16	
	44	VSS_15	
	41	VSS_14	
	38	VSS_13	
	35	VSS_12	
	32	VSS_11	
	29	VSS_10	
	26	VSS_9	
	23	VSS_8	
	20	VSS_7	
	17	VSS_6	
	14	VSS_5	
	11	VSS_4	
	8	VSS_3	
	5	VSS_2	
	2	VSS_1	

DDR_VREF_0V9

VREF 1

3V3

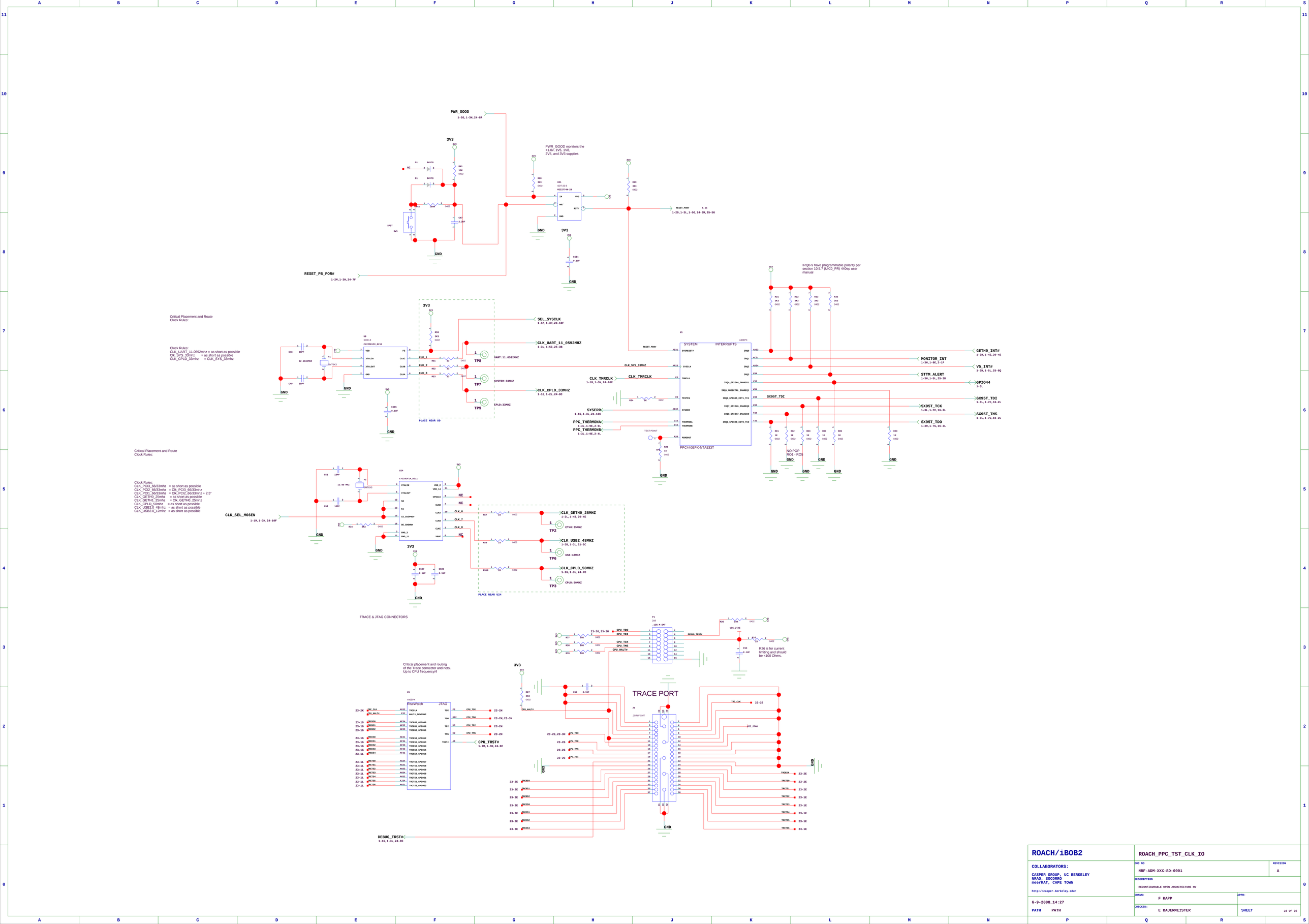
VDDSPD 238

1V8

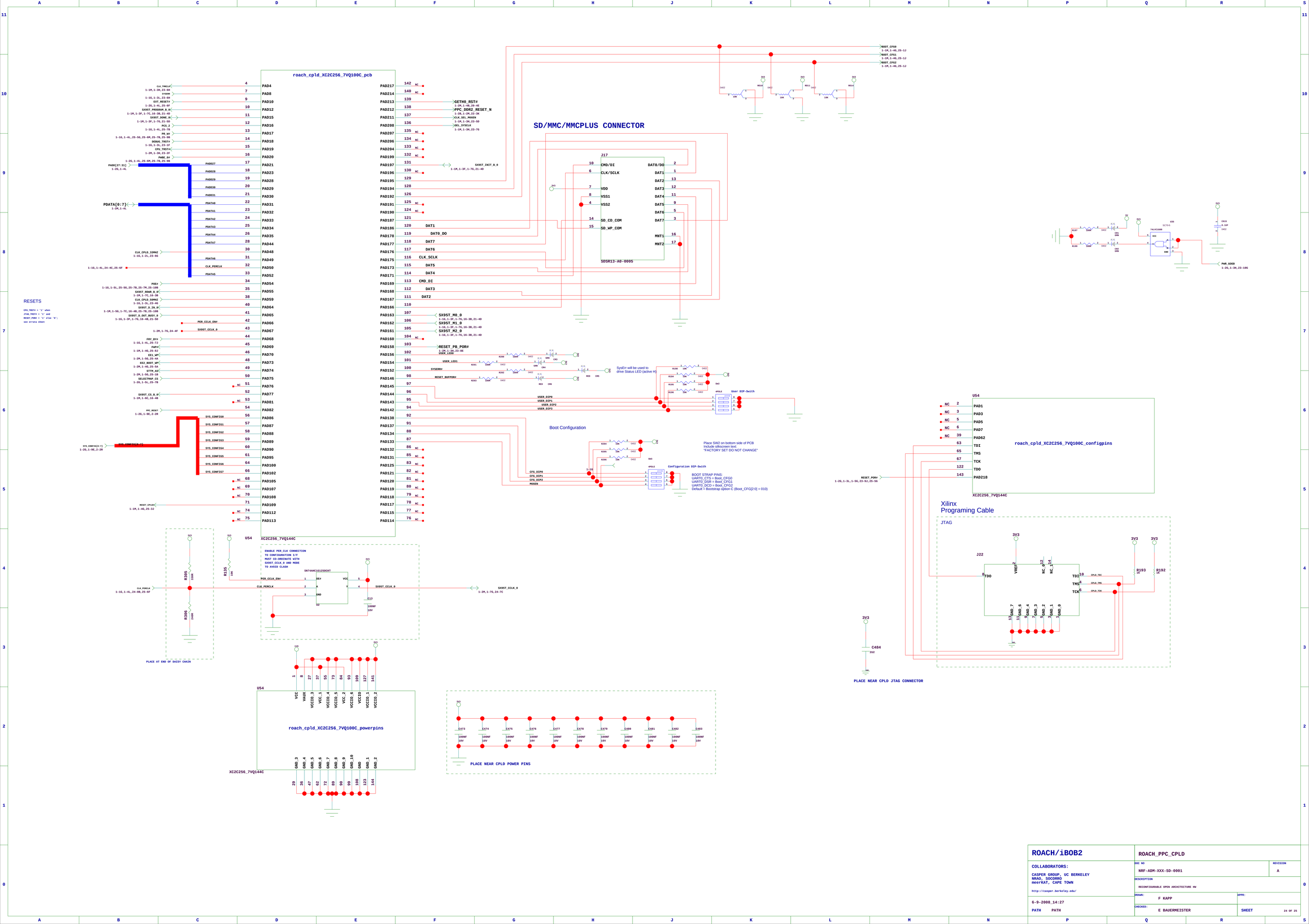
	197	VDD_11
	189	VDD_10
	187	VDD_9
	184	VDD_8
	178	VDD_7
	172	VDD_6
	69	VDD_5
	67	VDD_4
	64	VDD_3
	59	VDD_2
	53	VDD_1
	194	VDDQ_11
	191	VDDQ_10
	181	VDDQ_9
	175	VDDQ_8
	170	VDDQ_7
	78	VDDQ_6
	75	VDDQ_5
	72	VDDQ_4
	62	VDDQ_3
	56	VDDQ_2
	51	VDDQ_1

PLACE NEAREST DDR2 MODULE PINS

| | | |



ROACH/iBOB2	**ROACH_PPC_TST_CLK_IO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-9-2008_14:27	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 23 OF 25



ROACH/iBOB2	**ROACH_PPC_CPLD**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-9-2008_14:27	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 24 OF 25

PDATA[0:31]
1-2M,1-4L

PADD[2:31]

PADD[2:2]
1-2G,1-4L,24-9B

PADD30 IS THE LSB FOR 16 BIT
WIDE BUS TRANSFERS

NOTE:
DMA SIGNALS
IN GREEN TEXT

PADD2 IS THE MSB

CHIP SELECTS CONFIG	
CS0	NOR FLASH - U42
CS1	FPGA - U15
CS2	CPLD - U54
CS3	FPGA - U15
CS4	SELECTMAP_CS
CS5	GPIO - SX95_D_IN

U1
External Slave Peripheral
A403FPX

PERDATA[31:0]
PERADDR[31:0]
PERBA[2:0]
PERCS0
PERCS1#_GPIO06
PERCS2#
PERCS4#_GPIO09
PERCS5#_GPIO10
PEROE#
PERWE_WP
PERWE_BY#
PERWE_1#
PERWE_0#
PERWE1#
PERWE2#
PERWE3#
PERREADY
PERBLAST#
PERDBG0067_GPIO00_DMAREQ2
PERADDR06_GPIO01_DMAACK2
PERADDR05_GPIO02_EOT2_TC2
GPIO03_PERADDR04_DMAREQ3
GPIO04_PERADDR03_DMAACK3
GPIO05_PERADDR02_EOT3_TC3
EXTRESET2
PERCLK
PERERR_GPIO11
CLK_PERCLK
EXT_RESET#
EPB RESET OUTPUT
1-2G,1-4L,24-10C
CLK_PERCLK
1-1G,1-4L,24-4C,24-8B

U42
FBGA64
32Mx16 MIRROR BIT
FLASH
32Mx16
4Mx8B

PWR#
1-1M,1-4G,24-7C
RST_BTN#
1-1G,1-4L,24-7C

U44
SSOP20
ICL3225ECA
U43
SSOP20
ICL3225ECA

P2
DSUB9FEMALE 180 HOLE
RF BOOB MALE
UART Port 0

J14
UART Port 1
HLE-105-02-G-DV

PADD30	AE23	PER_A[30]
PADD29	AE22	PER_A[29]
PADD28	AG18	PER_A[28]
PADD27	AG12	PER_A[27]
PADD26	AG15	PER_A[26]
PADD25	AG23	PER_A[25]
PADD24	AF19	PER_A[24]
PADD23	AE12	PER_A[23]
PADD22	AG16	PER_A[22]
PADD21	AF13	PER_A[21]
PADD20	AG20	PER_A[20]
PADD19	AF23	PER_A[19]
PADD18	AH17	PER_A[18]
PADD17	AH15	PER_A[17]
PADD16	L20	PER_SP_A[16]
PADD15	J22	PER_SP_A[15]
PADD14	H22	PER_SP_A[14]
PADD13	L15	PER_SP_A[13]
PADD12	L16	PER_SP_A[12]
PADD11	K22	PER_SP_A[11]
PADD10	K21	PER_SP_A[10]
PADD9	K16	PER_SP_A[9]
PADD8	J15	PER_SP_A[8]
PADD7 (DMAREQ2)	L21	PER_SP_A[7]
PADD6 (DMAACK2)	G22	PER_SP_A[6]
PADD5 (EOT2/TC2)	K23	PER_SP_A[5]
PADD4 (DMAREQ3)	K14	PER_SP_A[4]
PADD3 (DMAACK3)	L14	PER_SP_A[3]
PADD2 (EOT3/TC3)	J12	PER_SP_A[2]
PCS_1	K13	PER_CS0
PCS_3	AG17	PER_CS1
POE#	AF21	PER_OE_N
PR_W#	AF20	PER_R_W_N
PWBE_1#	AF14	PER_WBE[1]
PWBE_0#	AF18	PER_WBE[0]
PBLAST#	H23	PER_B_LAST

PER_D[15]	AG22	PDATA15
PER_D[14]	AH22	PDATA14
PER_D[13]	AH12	PDATA13
PER_D[12]	AG13	PDATA12
PER_D[11]	AH20	PDATA11
PER_D[10]	AH19	PDATA10
PER_D[9]	AH14	PDATA9
PER_D[8]	AH13	PDATA8
PER_D[7]	AF15	PDATA7
PER_D[6]	AE16	PDATA6
PER_D[5]	AE21	PDATA5
PER_D[4]	AD20	PDATA4
PER_D[3]	AF16	PDATA3
PER_D[2]	AE17	PDATA2
PER_D[1]	AE19	PDATA1
PER_D[0]	AD19	PDATA0
PER_D_PAR[1]	AG21	NC
PER_D_PAR[0]	AE13	NC
PER_INT	G23	V5_INT#
PER_READY	K12	PREADY
PER_CLK	AH18	CLK_PERCLK

BANKS=1, 2, 4
CHIP SELECT 1
U15

ROUTE AS DAISY CHAIN - U1 - U15 - U54 - TERMINATION
KEEP STUBS AS SHORT AS POSSIBLE

I2C0_SCLK
1-2B,1-5L,1-9B,2-2P,22-2D
I2C0_SDATA
1-2B,1-5L,1-9E

EE2_BOOT_WP
1-2M,1-4G,24-7C
EE1_WP
1-2M,1-5G,24-7C
AT24C04N-10SU-1.8

CLK_UART_11_0592MHZ
1-3L,1-5G,23-7G

STTM_ALERT
1-3M,1-5L,23-6M
STTM_AS
1-2M,1-5G,24-7C
AD7414-0

U1
UART
UARTSERCLK
UART1_TX_UART0_TX
UART1_RX_UART0_RX
UART1_RTS#_UART0_RTS#
UART1_CTS#_UART0_CTS#
UART2_TX_UART0_DTR#
UART2_RX_UART0_RI#
UART2_RTS#_UART0_DSR#
UART2_CTS#_UART0_DCD#
UART1_TX
UART1_RX
UART2_TX
UART2_RX
CPU_UART0_DSR#
CPU_UART0_DCD#
IIC0
IIC0SCLK
IIC0SDATA
IIC1_SPI
SCPCLKOUT_IIC1SCLK
SCPDI_IIC1SDATA
SCPDO
NAND Flash
Interface
NOT USED
NFALE
NFCLE
NFREN#
NFWEN#
NFRDYBUSY#
NFCE3#_PERCS3#
PCS_3

UART1_TX
UART1_RX
PERPARB_UART1_RTS#
PERPARB_UART1_CTS#
UART2_TX
UART2_RX
RESET_CPLD#
1-1M,1-4G,24-5C
BOOT_CFG2
1-1M,1-4G,24-10M
BOOT_CFG1
1-1M,1-4G,24-11M
BOOT_CFG0
1-1M,1-4G,24-11M

1-1G,1-5L,24-8C,25-7B,25-7M,25-10B
PORF
1-1G,1-4L,24-10C,25-6M,25-7B,25-9B
PR_WP
RESET_PORF
1-2G,1-3L,1-5G,23-8J,24-5M

CS0	NOR FLASH - U42
CS1	FPGA - U15
CS2	CPLD - U54
CS3	FPGA - U15
CS4	SELECTMAP_CS
CS5	GPIO - SX95_D_IN

ROACH/iBOB2	ROACH_PPC_NVM_SERIAL
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-9-2008_14:27	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 25 OF 25