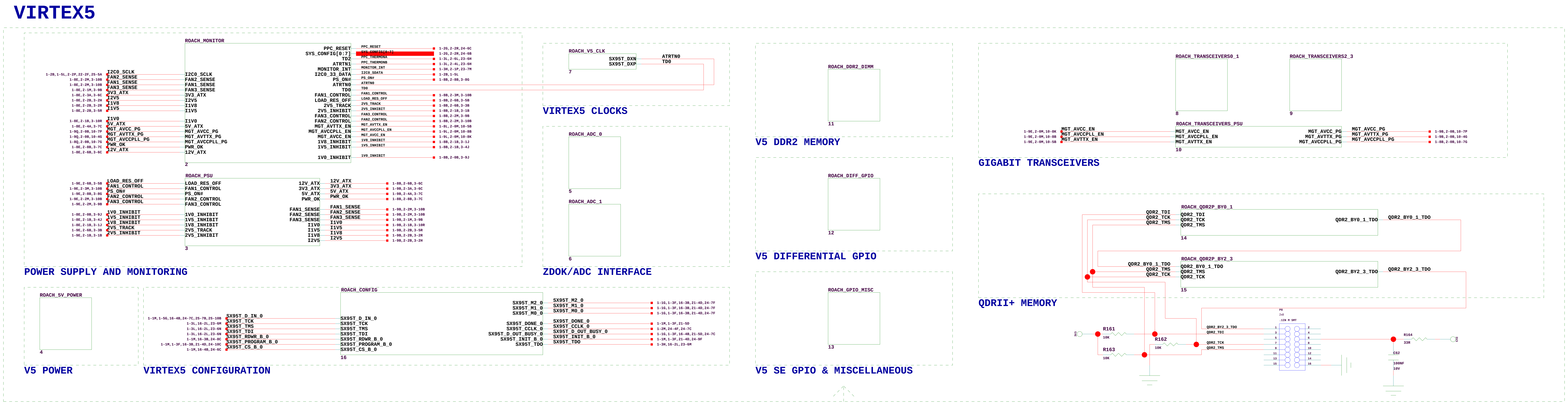
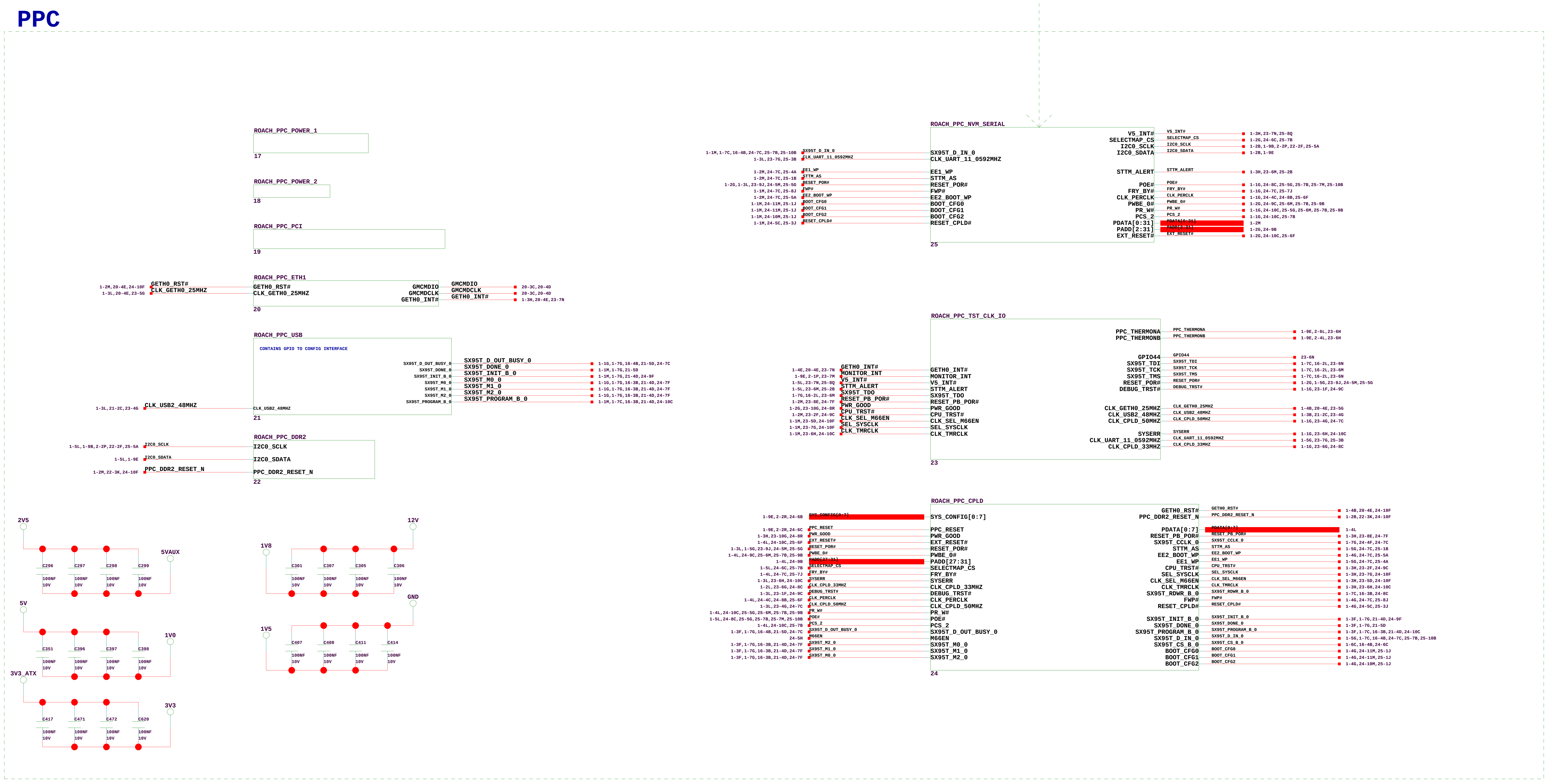
VIRTEX5

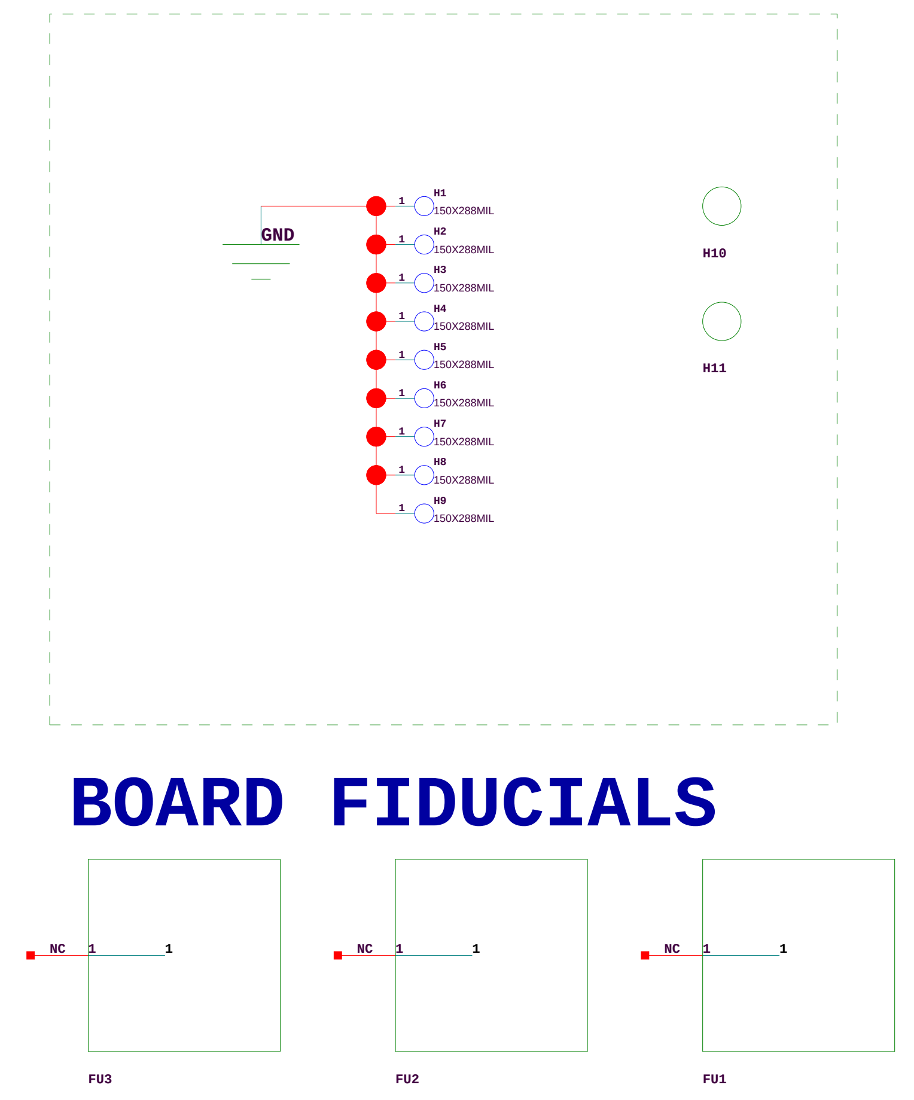

ROACH_MONITOR
2
ROACH_PSU
3
POWER SUPPLY AND MONITORING
ROACH_V5_CLK
7
VIRTEX5 CLOCKS
ROACH_ADC_0
5
ROACH_ADC_1
6
ZDOK/ADC INTERFACE
ROACH_DDR2_DIMM
11
V5 DDR2 MEMORY
ROACH_DIFF_GPIO
12
V5 DIFFERENTIAL GPIO
ROACH_GPIO_MISC
13
V5 SE GPIO & MISCELLANEOUS
ROACH_TRANSCEIVERS0_1
8
ROACH_TRANSCEIVERS2_3
9
ROACH_TRANSCEIVERS_PSU
10
GIGABIT TRANSCEIVERS
ROACH_QDR2P_BY0_1
14
ROACH_QDR2P_BY2_3
15
QDRII+ MEMORY
ROACH_5V_POWER
4
V5 POWER
ROACH_CONFIG
16
VIRTEX5 CONFIGURATION
R161
10K
R162
10K
R163
10K
R164
330
C62
100NF
10V
I2C0_SCLK
FAN2_SENSE
FAN1_SENSE
FAN3_SENSE
3V3_ATX
I2V5
I1V8
I1V5
I1V0
5V_ATX
MGT_AVCC_PG
MGT_AVTTX_PG
MGT_AVCCPLL_PG
PWR_OK
12V_ATX
PPC_RESET
SYS_CONFIG[0:7]
TD2
ATRTN1
MONITOR_INT
I2C0_33_SDATA
PS_ON#
ATRTN0
TDO
FAN1_CONTROL
LOAD_RES_OFF
2V5_TRACK
2V5_INHIBIT
FAN3_CONTROL
FAN2_CONTROL
MGT_AVTTX_EN
MGT_AVCCPLL_EN
MGT_AVCC_EN
1V8_INHIBIT
1V5_INHIBIT
1V0_INHIBIT
SX95T_DXN
SX95T_DXP
QDR2_BY0_1_TDO
QDR2_BY2_3_TDO
QDR2_TDI
QDR2_TCK
QDR2_TMS
SX95T_D_IN_0
SX95T_TCK
SX95T_TMS
SX95T_TDI
SX95T_RDWR_B_0
SX95T_PROGRAM_B_0
SX95T_CS_B_0
SX95T_M2_0
SX95T_M1_0
SX95T_M0_0
SX95T_DONE_0
SX95T_CCLK_0
SX95T_D_OUT_BUSY_0
SX95T_INIT_B_0
SX95T_TDO

PPC


ROACH_PPC_POWER_1
17
ROACH_PPC_POWER_2
18
ROACH_PPC_PCI
19
ROACH_PPC_ETH1
20
ROACH_PPC_USB
CONTAINS GPIO TO CONFIG INTERFACE
21
ROACH_PPC_DDR2
22
ROACH_PPC_NVM_SERIAL
25
ROACH_PPC_TST_CLK_IO
23
ROACH_PPC_CPLD
24
GETH0_RST#
CLK_GETH0_25MHZ
GMCMDIO
GMCMDCLK
GETH0_INT#
CLK_USB2_48MHZ
I2C0_SCLK
I2C0_SDATA
PPC_DDR2_RESET_N
V5_INT#
SELECTMAP_CS
STTM_ALERT
POE#
FRY_BY#
CLK_PERCLK
PWBE_0#
PR_W#
PCS_2
PDATA[0:31]
PADD[2:31]
EXT_RESET#
PPC_THERMONA
PPC_THERMONB
GPIO44
CLK_GETH0_25MHZ
CLK_USB2_48MHZ
CLK_CPLD_50MHZ
SYSERR
CLK_UART_11_0592MHZ
CLK_CPLD_33MHZ
SYS_CONFIG[0:7]
PPC_RESET
PWR_GOOD
EXT_RESET#
RESET_POR#
PADD[27:31]
BOOT_CFG0
BOOT_CFG1
BOOT_CFG2
2V5
5VAUX
5V
1V0
3V3_ATX
3V3
1V8
12V
1V5
GND
C296
C297
C298
C299
C351
C396
C397
C398
C417
C471
C472
C620
C301
C307
C305
C306
C407
C408
C411
C414
100NF
10V

MECHANICAL

BOARD FIDUCIALS


GND
M10
M11
NC
1
FU3
FU2
FU1

LOGO'S

PLACEHOLDER FOR PCB
MEERKAT LOGO

PLACEHOLDER FOR PCB
CASPER LOGO

PLACEHOLDER FOR PCB
ROACH LOGO

PLACEHOLDER FOR PCB
NRAO LOGO

BOARD SERIAL NUMBER

CONTRIBUTORS

ETIENNE BAUERMEISTER
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ROACH/iBOB2	ROACH_TOP
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-19-2008_14:43	DRAWN: F KAPP APPR:
PATH PATH	CHECKED: E BAUERMEISTER SHEET 1 OF 25

U59
TPS74401RGWT
5VAUX
3V3AUX
1V5AUX
GND
TIE TO GROUND IF PLL'S ARE NOT USED
DEFAULT=POSITION 1-2
PLACE AT ACTEL 1V5 POWER PINS
PLACE AT ACTEL 3V3 POWER PINS
TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE
DEFAULT=POSITION 2-3
JP26
JP27
JP28
roach_AFS600_powerpins
VAREF
PTBASE
PUSH_BUTTON
Q11
FJD3076TM
PB POWER SWITCH
KEY - REMOVE PIN
MONITOR RESET
CHS_SWITCH
CHS_LED0
CHS_LED1
J7
15-91-2140
XPORT - PLACE IN REAR I/O REGION
XP1001001-03R
J28
SERIAL_IN
SERIAL_OUT
SERIAL_CP1
SERIAL_CP2
SERIAL_CP3
XPORT_RESET
DEBUG_SERIAL_IN
DEBUG_SERIAL_OUT
roach_AFS600_pcb
TEMPERATURE DIODE HEADER
J31
15-91-2200
ACTEL JTAG CONNECTOR
J27
roach_AFS600_configpins
U60
12V_IMON
12V_SW_ON
5V_IMON
5V_SW_ON
3V3_IMON
3V3_SW_ON
2V5_INHIBIT
2V5_TRACK
1V8_INHIBIT
1V5_INHIBIT
1V0_INHIBIT
Q12
Q13
Q14
FDS6675BZ
ATRTN0
ATRTN1
SPARE ANALOG VOLTAGE INPUT #0
SPARE ANALOG VOLTAGE INPUT #1
SPARE GATE DRIVE OUTPUT #0
SPARE GATE DRIVE OUTPUT #1
J41
15-91-2080
U61
ADM3101EACPZ-REEL
J26
X5
ECX-306
32.768KHZ
U3
TL7700CPSR
FAN1_CONTROL
FAN1_SENSE
FAN2_CONTROL
FAN2_SENSE
FAN3_CONTROL
FAN3_SENSE
MGT_AVCC_EN
MGT_AVTTX_EN
MGT_AVCCPLL_EN
MGT_AVCC_PG
MGT_AVTTX_PG
MGT_AVCCPLL_PG
PS_ON#
PWR_OK
LOAD_RES_OFF
I2V5
I1V8
I1V5
I1V0
PPC_RESET
SYS_CONFIG[0:7]
I2C0_33_DATA
I2C0_SCLK
MONITOR_INT

REFERENCE RESISTOR/ADC VALUES

FOR 8 BIT ADC USING 2.56V REFERENCE:

VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)	ADC COUNT AT MAX POWER	CURRENT/BIT (A)
12V	0R01	3.36	0.11	33	0.1
5V	0R0047	6.78	0.22	31	0.21
3V3	0R01	3.47	0.12	34	0.1
2V5	0R01	3.56	0.13	35	0.1
1V8	0R0022	12.91	0.37	28	0.45
1V5	0R0047	6.77	0.22	31	0.21
1V0	0R001	26.79	0.72	26	1.0

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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6-19-2008_14:43

PATH PATH

ROACH_MONITOR

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	2 OF 25

AUX FAN CONNECTORS - ATX 4 PIN
FAN1_SENSE 1-8E,1-9B,2-2M
FAN1_CONTROL 1-8B,1-9E,2-3M
FAN2_SENSE 1-8E,1-9B,2-2M
FAN2_CONTROL 1-8B,1-9E,2-2M
FAN3_SENSE 1-8E,1-9B,2-1M
FAN3_CONTROL 1-8B,1-9E,2-2M
J21 47053-1000
J20 47053-1000
J19 47053-1000
1 GND
2 12V
3 SENSE
4 CONTROL
PLACE ON SILKSCREEN: FAN1
PLACE ON SILKSCREEN: FAN2
PLACE ON SILKSCREEN: FAN3
ATX POWER CONNECTORS
5VAUX
N12V
J18 44206-0007
3V3_1, 3V3_2, COM_1, 5V_1, COM_2, 5V_2, COM_3, PWR_OK, 5VSB, 12V1_1, 12V1_2, 3V3_3
3V3_4, -12V, COM_4, PS_ON#, COM_5, COM_6, COM_7, N/C, 5V_3, 5V_4, 5V_5, COM_8
20NC
PS_ON# 1-8B,1-9E,2-8B
PWR_OK 1-8B,1-9E,2-8B
J32 8510-4500PL
5V_ATX 1-8E,1-9B,2-4A
3V3_ATX 1-8E,1-9B,2-3A
12V_ATX 1-8B,1-8E,2-6B
BOARD LAYOUT NOTE
SEPARATE GROUND RETURN CURRENTS FROM MAIN BOARD GROUND PLANES
BETWEEN POWER INPUT CONNECTORS AND REGULATOR AREA ON BOARD.
LOAD RESISTORS FOR ATX PSU MIN LOAD
SWITCH OFF ONCE LOAD EXCEEDS MINIMUM SPEC
ADJUST RESISTOR VALUES FOR ACTUAL SUPPLY
R180 10K
Q9 NDS331N
R185 10R 5W AC05000001009JLB00
Q10 NDS331N
R187 56R 5W AC05000005609JLB00
LOAD_RES_OFF 1-8B,1-9E,2-6B
Q8 BSS138
R181 10K
GND
1V0
ROUTE FROM LOAD
R13 22R
PLACE RESISTOR CLOSE TO U50
ROUTE SHORTEST
R144
5V
1V5
L6 BLM31PG121SN1B 3A
L5 BLM31PG121SN1B 3A
L16 BLM31PG121SN1B 3A
C403 330UF 16V
C401 330UF 16V
C419 22UF 16V
U50 30A SMPS MODULE
13 TURBOTRANS
10 SENSE+
2 VI_1
6 VI_0
1 INHIBIT/UVLADJ
14 TRACK
11 SENSE-
PTH05T210WAD
GND_3 GND_2 GND_1 GND_0
VO_0 VO_1 VOADJUST
R143
C418 10UF
C117 10UF
C402 1000UF 2V5
C400 1000UF 2V5
C104 1000UF 2V5
C105 1000UF 2V5
I1V0 1-8E,1-9B,2-1B
DIRECT TO P8 ON U50, DEDICATED TRACE
1V0_INHIBIT 1-8B,1-9E,2-9B
Q4 BSS138
ROUTE FROM LOAD
1.2V SUPPLY DELETED - NOT REQUIRED
1V5
ROUTE FROM LOAD
R12 22R
PLACE RESISTOR CLOSE TO U51
ROUTE SHORTEST
R146
12V
L7 BLM31PG121SN1B 3A
1V8
C404 330UF 16V
C420 22UF 16V
U51 10A SMPS MODULE
9 TURBOTRANS
6 SENSE+
2 VI
11 INHIBIT/UVLADJ
10 TRACK
7 SENSE-
1 SMARTSYNC
PTH08T240WAD
VO VOADJUST
R147
C421 10UF
C405 1000UF 2V5
I1V5 1-8E,1-9B,2-2B
DIRECT TO P8 ON U51, DEDICATED TRACE
1V5_INHIBIT 1-8B,1-9E,2-1B
Q5 BSS138
ROUTE FROM LOAD
1V8
ROUTE FROM LOAD
R11 22R
PLACE RESISTOR CLOSE TO U52
ROUTE SHORTEST
R149
12V
L14 BLM31PG121SN1B 3A
2V5
C409 330UF 16V
C423 22UF 16V
U27 16A SMPS MODULE
PTH08T220WAD
R148
C422 10UF
C410 1000UF 2V5
I1V8 1-8E,1-9B,2-2B
DIRECT TO P8 ON PTH08T210W, DEDICATED TRACE
1V8_INHIBIT 1-8B,1-9E,2-1B
Q6 BSS138
ROUTE FROM LOAD
2V5
ROUTE FROM LOAD
R10 22R
PLACE RESISTOR CLOSE TO U53
ROUTE SHORTEST
R177
2V5_TRACK 1-8B,1-9E,2-6B
R183 1K
C426 10UF
12V
L15 BLM31PG121SN1B 3A
C412 330UF 16V
C424 22UF 16V
U53
PTH08T230WAD
C425 10UF 16V
C413 680UF 4V
R179
I2V5 1-8E,1-9B,2-2B
DIRECT TO P8 ON U53, DEDICATED TRACE
2V5_INHIBIT 1-8B,1-9E,2-1B
Q7 BSS138
ROUTE FROM LOAD

PSU INPUT SUMMARY

VOLTAGE	5.0V +- 10%
CURRENT (MAX)	6.0A

PSU RAIL SUMMARY

VOLTAGE	1.0V +- 5%
SUPPLIES	FPGA CORE
CURRENT (QUIESCENT)	1.5A
CURRENT (ACTIVE)	26.8A
LOAD STEP	25.3A

PSU INPUT SUMMARY

VOLTAGE	12V +- 10%
CURRENT (MAX)	0.8A

PSU RAIL SUMMARY

VOLTAGE	1.5V +- 5%
SUPPLIES	FPGA IO, QDR, PPC
CURRENT (QUIESCENT)	0.25A
CURRENT (ACTIVE)	6.8A
LOAD STEP	6.55A

PSU RAIL SUMMARY

VOLTAGE	2.5V +- 5%
SUPPLIES	FPGA, ZDOK PPC, PHY
CURRENT (QUIESCENT)	0.1A
CURRENT (ACTIVE)	3.6A
LOAD STEP	3.5A

PSU INPUT SUMMARY

VOLTAGE	12V +- 10%
CURRENT (MAX)	1.8A

PSU RAIL SUMMARY

VOLTAGE	1.8V +- 5%
SUPPLIES	FPGA IO, DDR2 x 2
CURRENT (QUIESCENT)	1A
CURRENT (ACTIVE)	12.9A
LOAD STEP	11.9A

PSU INPUT SUMMARY

VOLTAGE	12V +- 10%
CURRENT (MAX)	0.8A

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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6-19-2008_14:43

PATH PATH

ROACH_PSU

DOC NO NRF-ADM-XXX-SD-0001

REVISION A

DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

1V0
U15
2V5
GND
C311 330UF 6V
C312 330UF 6V
220NF 6.3V
10UF 6.3V
C310 330UF 2V5
C309 330UF 2V5
C180
C176
C174
C172
AB11 2V5_AUX
AC12 2V5_AUX_1
L12 2V5_AUX_2
M11 2V5_AUX_3
M21 2V5_AUX_4
P11 2V5_AUX_5
P23 2V5_AUX_6
T23 2V5_AUX_7
U24 2V5_AUX_8
V11 2V5_AUX_9
V23 2V5_AUX_10
Y23 2V5_AUX_11
C163
C155
C124
C31
C28
C25
C8
C157
C154
C122
C30
C27
C24
C7
C156
C153
C120
C29
C26
C23
C9
C283
C284
C281
C282
C273
C274
C348 47UF 6V
C349 47UF 6V
C350 47UF 6V
C328 47UF 6V
C327 47UF 6V
C326 47UF 6V
AB29 2V5_1
W28 2V5_17
AA32 2V5
AJ28 2V5_5
AL32 2V5_6
AM29 2V5_7
E30 2V5_8
H31 2V5_9
J28 2V5_10
L32 2V5_11
M29 2V5_12
P33 2V5_13
R30 2V5_14
T27 2V5_15
V31 2V5_16
AH31 2V5_4
AE30 2V5_3
AD33 2V5_2
BANKS=11, 13, 15, 17, 19, 21
A11 GND
A12 GND_1
A17 GND_2
A22 GND_3
A27 GND_4
A32 GND_5
AA11 GND_6
AA13 GND_7
AA15 GND_8
AA17 GND_9
AA19 GND_10
AA2 GND_11
AA21 GND_12
AA23 GND_13
AA27 GND_14
AA7 GND_15
AB12 GND_16
GND_127 J33
GND_126 J23
GND_125 J2
GND_124 J18
GND_123 J13
GND_122 H6
GND_121 H26
GND_120 H21
GND_119 H2
GND_118 H16
GND_117 G9
GND_116 G4
GND_115 G34
GND_114 G29
GND_113 G19
GND_112 F7
GND_111 F32

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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6-19-2008_14:43

PATH PATH

ROACH_5V_POWER

DOC NO
NRF-ADM-XXX-SD-0001

REVISION
A

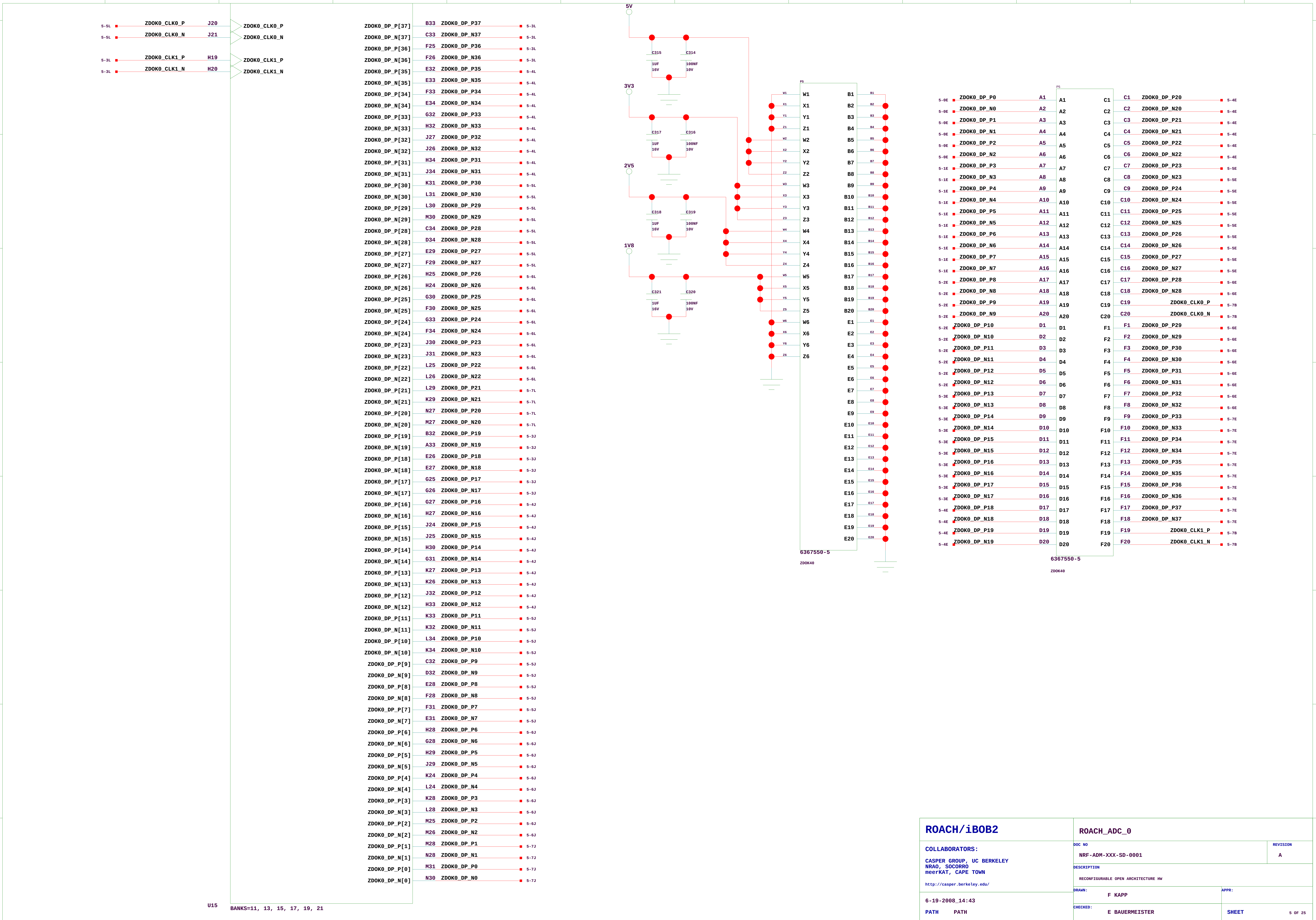
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 4 OF 25


U15
BANKS=11, 13, 15, 17, 19, 21
5-5L ZDOK0_CLK0_P J20 ZDOK0_CLK0_P
5-5L ZDOK0_CLK0_N J21 ZDOK0_CLK0_N
5-3L ZDOK0_CLK1_P H19 ZDOK0_CLK1_P
5-3L ZDOK0_CLK1_N H20 ZDOK0_CLK1_N
ZDOK0_DP_P[37] B33 ZDOK0_DP_P37 5-3L
ZDOK0_DP_N[37] C33 ZDOK0_DP_N37 5-3L
ZDOK0_DP_P[36] F25 ZDOK0_DP_P36 5-3L
ZDOK0_DP_N[36] F26 ZDOK0_DP_N36 5-3L
ZDOK0_DP_P[35] E32 ZDOK0_DP_P35 5-4L
ZDOK0_DP_N[35] E33 ZDOK0_DP_N35 5-4L
ZDOK0_DP_P[34] F33 ZDOK0_DP_P34 5-4L
ZDOK0_DP_N[34] E34 ZDOK0_DP_N34 5-4L
ZDOK0_DP_P[33] G32 ZDOK0_DP_P33 5-4L
ZDOK0_DP_N[33] H32 ZDOK0_DP_N33 5-4L
ZDOK0_DP_P[32] J27 ZDOK0_DP_P32 5-4L
ZDOK0_DP_N[32] J26 ZDOK0_DP_N32 5-4L
ZDOK0_DP_P[31] H34 ZDOK0_DP_P31 5-4L
ZDOK0_DP_N[31] J34 ZDOK0_DP_N31 5-4L
ZDOK0_DP_P[30] K31 ZDOK0_DP_P30 5-5L
ZDOK0_DP_N[30] L31 ZDOK0_DP_N30 5-5L
ZDOK0_DP_P[29] L30 ZDOK0_DP_P29 5-5L
ZDOK0_DP_N[29] M30 ZDOK0_DP_N29 5-5L
ZDOK0_DP_P[28] C34 ZDOK0_DP_P28 5-5L
ZDOK0_DP_N[28] D34 ZDOK0_DP_N28 5-5L
ZDOK0_DP_P[27] E29 ZDOK0_DP_P27 5-5L
ZDOK0_DP_N[27] F29 ZDOK0_DP_N27 5-5L
ZDOK0_DP_P[26] H25 ZDOK0_DP_P26 5-6L
ZDOK0_DP_N[26] H24 ZDOK0_DP_N26 5-6L
ZDOK0_DP_P[25] G30 ZDOK0_DP_P25 5-6L
ZDOK0_DP_N[25] F30 ZDOK0_DP_N25 5-6L
ZDOK0_DP_P[24] G33 ZDOK0_DP_P24 5-6L
ZDOK0_DP_N[24] F34 ZDOK0_DP_N24 5-6L
ZDOK0_DP_P[23] J30 ZDOK0_DP_P23 5-6L
ZDOK0_DP_N[23] J31 ZDOK0_DP_N23 5-6L
ZDOK0_DP_P[22] L25 ZDOK0_DP_P22 5-6L
ZDOK0_DP_N[22] L26 ZDOK0_DP_N22 5-6L
ZDOK0_DP_P[21] L29 ZDOK0_DP_P21 5-7L
ZDOK0_DP_N[21] K29 ZDOK0_DP_N21 5-7L
ZDOK0_DP_P[20] N27 ZDOK0_DP_P20 5-7L
ZDOK0_DP_N[20] M27 ZDOK0_DP_N20 5-7L
ZDOK0_DP_P[19] B32 ZDOK0_DP_P19 5-3J
ZDOK0_DP_N[19] A33 ZDOK0_DP_N19 5-3J
ZDOK0_DP_P[18] E26 ZDOK0_DP_P18 5-3J
ZDOK0_DP_N[18] E27 ZDOK0_DP_N18 5-3J
ZDOK0_DP_P[17] G25 ZDOK0_DP_P17 5-3J
ZDOK0_DP_N[17] G26 ZDOK0_DP_N17 5-3J
ZDOK0_DP_P[16] G27 ZDOK0_DP_P16 5-4J
ZDOK0_DP_N[16] H27 ZDOK0_DP_N16 5-4J
ZDOK0_DP_P[15] J24 ZDOK0_DP_P15 5-4J
ZDOK0_DP_N[15] J25 ZDOK0_DP_N15 5-4J
ZDOK0_DP_P[14] H30 ZDOK0_DP_P14 5-4J
ZDOK0_DP_N[14] G31 ZDOK0_DP_N14 5-4J
ZDOK0_DP_P[13] K27 ZDOK0_DP_P13 5-4J
ZDOK0_DP_N[13] K26 ZDOK0_DP_N13 5-4J
ZDOK0_DP_P[12] J32 ZDOK0_DP_P12 5-4J
ZDOK0_DP_N[12] H33 ZDOK0_DP_N12 5-4J
ZDOK0_DP_P[11] K33 ZDOK0_DP_P11 5-5J
ZDOK0_DP_N[11] K32 ZDOK0_DP_N11 5-5J
ZDOK0_DP_P[10] L34 ZDOK0_DP_P10 5-5J
ZDOK0_DP_N[10] K34 ZDOK0_DP_N10 5-5J
ZDOK0_DP_P[9] C32 ZDOK0_DP_P9 5-5J
ZDOK0_DP_N[9] D32 ZDOK0_DP_N9 5-5J
ZDOK0_DP_P[8] E28 ZDOK0_DP_P8 5-5J
ZDOK0_DP_N[8] F28 ZDOK0_DP_N8 5-5J
ZDOK0_DP_P[7] F31 ZDOK0_DP_P7 5-5J
ZDOK0_DP_N[7] E31 ZDOK0_DP_N7 5-5J
ZDOK0_DP_P[6] H28 ZDOK0_DP_P6 5-6J
ZDOK0_DP_N[6] G28 ZDOK0_DP_N6 5-6J
ZDOK0_DP_P[5] H29 ZDOK0_DP_P5 5-6J
ZDOK0_DP_N[5] J29 ZDOK0_DP_N5 5-6J
ZDOK0_DP_P[4] K24 ZDOK0_DP_P4 5-6J
ZDOK0_DP_N[4] L24 ZDOK0_DP_N4 5-6J
ZDOK0_DP_P[3] K28 ZDOK0_DP_P3 5-6J
ZDOK0_DP_N[3] L28 ZDOK0_DP_N3 5-6J
ZDOK0_DP_P[2] M25 ZDOK0_DP_P2 5-6J
ZDOK0_DP_N[2] M26 ZDOK0_DP_N2 5-6J
ZDOK0_DP_P[1] M28 ZDOK0_DP_P1 5-7J
ZDOK0_DP_N[1] N28 ZDOK0_DP_N1 5-7J
ZDOK0_DP_P[0] M31 ZDOK0_DP_P0 5-7J
ZDOK0_DP_N[0] N30 ZDOK0_DP_N0 5-7J
5V
3V3
2V5
1V8
C315 1UF 16V
C314 100NF 10V
C317 1UF 16V
C316 100NF 10V
C318 1UF 16V
C319 100NF 10V
C321 1UF 16V
C320 100NF 10V
P5
W1 X1 Y1 Z1 W2 X2 Y2 Z2 W3 X3 Y3 Z3 W4 X4 Y4 Z4 W5 X5 Y5 Z5 W6 X6 Y6 Z6
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20
E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20
6367550-5
ZDOK40
P5
5-0E ZDOK0_DP_P0 A1
5-0E ZDOK0_DP_N0 A2
5-0E ZDOK0_DP_P1 A3
5-0E ZDOK0_DP_N1 A4
5-0E ZDOK0_DP_P2 A5
5-0E ZDOK0_DP_N2 A6
5-1E ZDOK0_DP_P3 A7
5-1E ZDOK0_DP_N3 A8
5-1E ZDOK0_DP_P4 A9
5-1E ZDOK0_DP_N4 A10
5-1E ZDOK0_DP_P5 A11
5-1E ZDOK0_DP_N5 A12
5-1E ZDOK0_DP_P6 A13
5-1E ZDOK0_DP_N6 A14
5-1E ZDOK0_DP_P7 A15
5-1E ZDOK0_DP_N7 A16
5-2E ZDOK0_DP_P8 A17
5-2E ZDOK0_DP_N8 A18
5-2E ZDOK0_DP_P9 A19
5-2E ZDOK0_DP_N9 A20
5-2E ZDOK0_DP_P10 D1
5-2E ZDOK0_DP_N10 D2
5-2E ZDOK0_DP_P11 D3
5-2E ZDOK0_DP_N11 D4
5-2E ZDOK0_DP_P12 D5
5-2E ZDOK0_DP_N12 D6
5-3E ZDOK0_DP_P13 D7
5-3E ZDOK0_DP_N13 D8
5-3E ZDOK0_DP_P14 D9
5-3E ZDOK0_DP_N14 D10
5-3E ZDOK0_DP_P15 D11
5-3E ZDOK0_DP_N15 D12
5-3E ZDOK0_DP_P16 D13
5-3E ZDOK0_DP_N16 D14
5-3E ZDOK0_DP_P17 D15
5-3E ZDOK0_DP_N17 D16
5-4E ZDOK0_DP_P18 D17
5-4E ZDOK0_DP_N18 D18
5-4E ZDOK0_DP_P19 D19
5-4E ZDOK0_DP_N19 D20
C1 ZDOK0_DP_P20 5-4E
C2 ZDOK0_DP_N20 5-4E
C3 ZDOK0_DP_P21 5-4E
C4 ZDOK0_DP_N21 5-4E
C5 ZDOK0_DP_P22 5-4E
C6 ZDOK0_DP_N22 5-4E
C7 ZDOK0_DP_P23 5-5E
C8 ZDOK0_DP_N23 5-5E
C9 ZDOK0_DP_P24 5-5E
C10 ZDOK0_DP_N24 5-5E
C11 ZDOK0_DP_P25 5-5E
C12 ZDOK0_DP_N25 5-5E
C13 ZDOK0_DP_P26 5-5E
C14 ZDOK0_DP_N26 5-5E
C15 ZDOK0_DP_P27 5-5E
C16 ZDOK0_DP_N27 5-5E
C17 ZDOK0_DP_P28 5-6E
C18 ZDOK0_DP_N28 5-6E
C19 ZDOK0_CLK0_P 5-7B
C20 ZDOK0_CLK0_N 5-7B
F1 ZDOK0_DP_P29 5-6E
F2 ZDOK0_DP_N29 5-6E
F3 ZDOK0_DP_P30 5-6E
F4 ZDOK0_DP_N30 5-6E
F5 ZDOK0_DP_P31 5-6E
F6 ZDOK0_DP_N31 5-6E
F7 ZDOK0_DP_P32 5-6E
F8 ZDOK0_DP_N32 5-6E
F9 ZDOK0_DP_P33 5-7E
F10 ZDOK0_DP_N33 5-7E
F11 ZDOK0_DP_P34 5-7E
F12 ZDOK0_DP_N34 5-7E
F13 ZDOK0_DP_P35 5-7E
F14 ZDOK0_DP_N35 5-7E
F15 ZDOK0_DP_P36 5-7E
F16 ZDOK0_DP_N36 5-7E
F17 ZDOK0_DP_P37 5-7E
F18 ZDOK0_DP_N37 5-7E
F19 ZDOK0_CLK1_P 5-7B
F20 ZDOK0_CLK1_N 5-7B
6367550-5
ZDOK40
A B C D E F G H J K L M
7 6 5 4 3 2 1 0

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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6-19-2008_14:43

PATH PATH

ROACH_ADC_0

DOC NO
NRF-ADM-XXX-SD-0001

REVISION
A

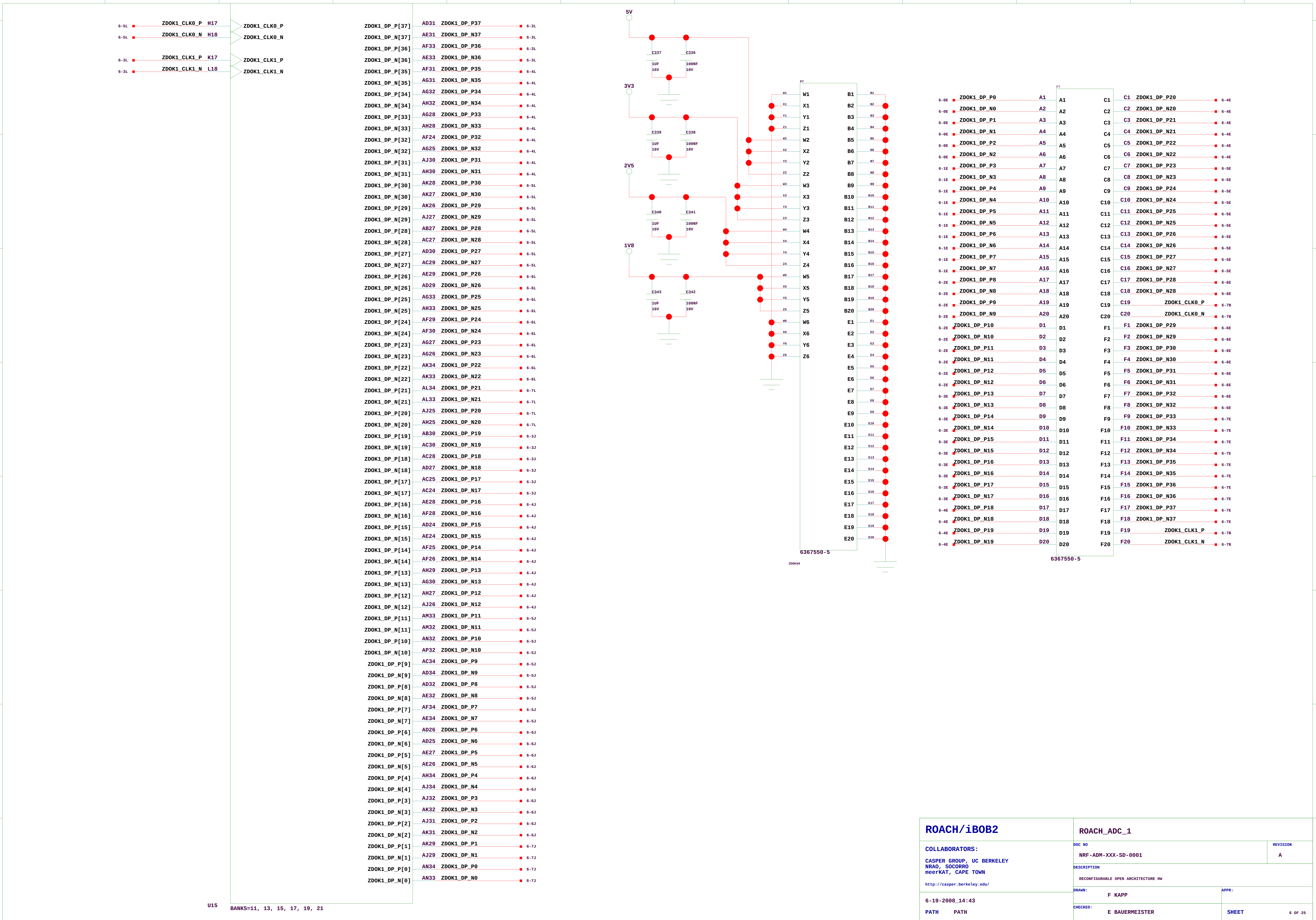
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 5 OF 25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6-5L ZDOK1_CLK0_N H18
6-3L ZDOK1_CLK1_P K17
6-3L ZDOK1_CLK1_N L18
ZDOK1_CLK0_P
ZDOK1_CLK0_N
ZDOK1_CLK1_P
ZDOK1_CLK1_N
ZDOK1_DP_P[37] AD31 ZDOK1_DP_P37 6-3L
ZDOK1_DP_N[37] AE31 ZDOK1_DP_N37 6-3L
ZDOK1_DP_P[36] AF33 ZDOK1_DP_P36 6-3L
ZDOK1_DP_N[36] AE33 ZDOK1_DP_N36 6-3L
ZDOK1_DP_P[35] AF31 ZDOK1_DP_P35 6-4L
ZDOK1_DP_N[35] AG31 ZDOK1_DP_N35 6-4L
ZDOK1_DP_P[34] AG32 ZDOK1_DP_P34 6-4L
ZDOK1_DP_N[34] AH32 ZDOK1_DP_N34 6-4L
ZDOK1_DP_P[33] AG28 ZDOK1_DP_P33 6-4L
ZDOK1_DP_N[33] AH28 ZDOK1_DP_N33 6-4L
ZDOK1_DP_P[32] AF24 ZDOK1_DP_P32 6-4L
ZDOK1_DP_N[32] AG25 ZDOK1_DP_N32 6-4L
ZDOK1_DP_P[31] AJ30 ZDOK1_DP_P31 6-4L
ZDOK1_DP_N[31] AH30 ZDOK1_DP_N31 6-4L
ZDOK1_DP_P[30] AK28 ZDOK1_DP_P30 6-5L
ZDOK1_DP_N[30] AK27 ZDOK1_DP_N30 6-5L
ZDOK1_DP_P[29] AK26 ZDOK1_DP_P29 6-5L
ZDOK1_DP_N[29] AJ27 ZDOK1_DP_N29 6-5L
ZDOK1_DP_P[28] AB27 ZDOK1_DP_P28 6-5L
ZDOK1_DP_N[28] AC27 ZDOK1_DP_N28 6-5L
ZDOK1_DP_P[27] AD30 ZDOK1_DP_P27 6-5L
ZDOK1_DP_N[27] AC29 ZDOK1_DP_N27 6-5L
ZDOK1_DP_P[26] AE29 ZDOK1_DP_P26 6-6L
ZDOK1_DP_N[26] AD29 ZDOK1_DP_N26 6-6L
ZDOK1_DP_P[25] AG33 ZDOK1_DP_P25 6-6L
ZDOK1_DP_N[25] AH33 ZDOK1_DP_N25 6-6L
ZDOK1_DP_P[24] AF29 ZDOK1_DP_P24 6-6L
ZDOK1_DP_N[24] AF30 ZDOK1_DP_N24 6-6L
ZDOK1_DP_P[23] AG27 ZDOK1_DP_P23 6-6L
ZDOK1_DP_N[23] AG26 ZDOK1_DP_N23 6-6L
ZDOK1_DP_P[22] AK34 ZDOK1_DP_P22 6-6L
ZDOK1_DP_N[22] AK33 ZDOK1_DP_N22 6-6L
ZDOK1_DP_P[21] AL34 ZDOK1_DP_P21 6-7L
ZDOK1_DP_N[21] AL33 ZDOK1_DP_N21 6-7L
ZDOK1_DP_P[20] AJ25 ZDOK1_DP_P20 6-7L
ZDOK1_DP_N[20] AH25 ZDOK1_DP_N20 6-7L
ZDOK1_DP_P[19] AB30 ZDOK1_DP_P19 6-3J
ZDOK1_DP_N[19] AC30 ZDOK1_DP_N19 6-3J
ZDOK1_DP_P[18] AC28 ZDOK1_DP_P18 6-3J
ZDOK1_DP_N[18] AD27 ZDOK1_DP_N18 6-3J
ZDOK1_DP_P[17] AC25 ZDOK1_DP_P17 6-3J
ZDOK1_DP_N[17] AC24 ZDOK1_DP_N17 6-3J
ZDOK1_DP_P[16] AE28 ZDOK1_DP_P16 6-4J
ZDOK1_DP_N[16] AF28 ZDOK1_DP_N16 6-4J
ZDOK1_DP_P[15] AD24 ZDOK1_DP_P15 6-4J
ZDOK1_DP_N[15] AE24 ZDOK1_DP_N15 6-4J
ZDOK1_DP_P[14] AF25 ZDOK1_DP_P14 6-4J
ZDOK1_DP_N[14] AF26 ZDOK1_DP_N14 6-4J
ZDOK1_DP_P[13] AH29 ZDOK1_DP_P13 6-4J
ZDOK1_DP_N[13] AG30 ZDOK1_DP_N13 6-4J
ZDOK1_DP_P[12] AH27 ZDOK1_DP_P12 6-4J
ZDOK1_DP_N[12] AJ26 ZDOK1_DP_N12 6-4J
ZDOK1_DP_P[11] AM33 ZDOK1_DP_P11 6-5J
ZDOK1_DP_N[11] AM32 ZDOK1_DP_N11 6-5J
ZDOK1_DP_P[10] AN32 ZDOK1_DP_P10 6-5J
ZDOK1_DP_N[10] AP32 ZDOK1_DP_N10 6-5J
ZDOK1_DP_P[9] AC34 ZDOK1_DP_P9 6-5J
ZDOK1_DP_N[9] AD34 ZDOK1_DP_N9 6-5J
ZDOK1_DP_P[8] AD32 ZDOK1_DP_P8 6-5J
ZDOK1_DP_N[8] AE32 ZDOK1_DP_N8 6-5J
ZDOK1_DP_P[7] AF34 ZDOK1_DP_P7 6-5J
ZDOK1_DP_N[7] AE34 ZDOK1_DP_N7 6-5J
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ZDOK1_DP_N[6] AD25 ZDOK1_DP_N6 6-6J
ZDOK1_DP_P[5] AE27 ZDOK1_DP_P5 6-6J
ZDOK1_DP_N[5] AE26 ZDOK1_DP_N5 6-6J
ZDOK1_DP_P[4] AH34 ZDOK1_DP_P4 6-6J
ZDOK1_DP_N[4] AJ34 ZDOK1_DP_N4 6-6J
ZDOK1_DP_P[3] AJ32 ZDOK1_DP_P3 6-6J
ZDOK1_DP_N[3] AK32 ZDOK1_DP_N3 6-6J
ZDOK1_DP_P[2] AJ31 ZDOK1_DP_P2 6-6J
ZDOK1_DP_N[2] AK31 ZDOK1_DP_N2 6-6J
ZDOK1_DP_P[1] AK29 ZDOK1_DP_P1 6-7J
ZDOK1_DP_N[1] AJ29 ZDOK1_DP_N1 6-7J
ZDOK1_DP_P[0] AN34 ZDOK1_DP_P0 6-7J
ZDOK1_DP_N[0] AN33 ZDOK1_DP_N0 6-7J
U15
BANKS=11, 13, 15, 17, 19, 21
5V
C337 1UF 16V
C336 100NF 10V
3V3
C339 1UF 16V
C338 100NF 10V
2V5
C340 1UF 16V
C341 100NF 10V
1V8
C343 1UF 16V
C342 100NF 10V
P7
W1 X1 Y1 Z1 W2 X2 Y2 Z2 W3 X3 Y3 Z3 W4 X4 Y4 Z4 W5 X5 Y5 Z5 W6 X6 Y6 Z6
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20
E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20
6367550-5
ZDOK40
P7
6-0E ZDOK1_DP_P0 A1
6-0E ZDOK1_DP_N0 A2
6-0E ZDOK1_DP_P1 A3
6-0E ZDOK1_DP_N1 A4
6-0E ZDOK1_DP_P2 A5
6-0E ZDOK1_DP_N2 A6
6-1E ZDOK1_DP_P3 A7
6-1E ZDOK1_DP_N3 A8
6-1E ZDOK1_DP_P4 A9
6-1E ZDOK1_DP_N4 A10
6-1E ZDOK1_DP_P5 A11
6-1E ZDOK1_DP_N5 A12
6-1E ZDOK1_DP_P6 A13
6-1E ZDOK1_DP_N6 A14
6-1E ZDOK1_DP_P7 A15
6-1E ZDOK1_DP_N7 A16
6-2E ZDOK1_DP_P8 A17
6-2E ZDOK1_DP_N8 A18
6-2E ZDOK1_DP_P9 A19
6-2E ZDOK1_DP_N9 A20
6-2E ZDOK1_DP_P10 D1
6-2E ZDOK1_DP_N10 D2
6-2E ZDOK1_DP_P11 D3
6-2E ZDOK1_DP_N11 D4
6-2E ZDOK1_DP_P12 D5
6-2E ZDOK1_DP_N12 D6
6-3E ZDOK1_DP_P13 D7
6-3E ZDOK1_DP_N13 D8
6-3E ZDOK1_DP_P14 D9
6-3E ZDOK1_DP_N14 D10
6-3E ZDOK1_DP_P15 D11
6-3E ZDOK1_DP_N15 D12
6-3E ZDOK1_DP_P16 D13
6-3E ZDOK1_DP_N16 D14
6-3E ZDOK1_DP_P17 D15
6-3E ZDOK1_DP_N17 D16
6-4E ZDOK1_DP_P18 D17
6-4E ZDOK1_DP_N18 D18
6-4E ZDOK1_DP_P19 D19
6-4E ZDOK1_DP_N19 D20
C1 ZDOK1_DP_P20 6-4E
C2 ZDOK1_DP_N20 6-4E
C3 ZDOK1_DP_P21 6-4E
C4 ZDOK1_DP_N21 6-4E
C5 ZDOK1_DP_P22 6-4E
C6 ZDOK1_DP_N22 6-4E
C7 ZDOK1_DP_P23 6-5E
C8 ZDOK1_DP_N23 6-5E
C9 ZDOK1_DP_P24 6-5E
C10 ZDOK1_DP_N24 6-5E
C11 ZDOK1_DP_P25 6-5E
C12 ZDOK1_DP_N25 6-5E
C13 ZDOK1_DP_P26 6-5E
C14 ZDOK1_DP_N26 6-5E
C15 ZDOK1_DP_P27 6-5E
C16 ZDOK1_DP_N27 6-5E
C17 ZDOK1_DP_P28 6-6E
C18 ZDOK1_DP_N28 6-6E
C19 ZDOK1_CLK0_P 6-7B
C20 ZDOK1_CLK0_N 6-7B
F1 ZDOK1_DP_P29 6-6E
F2 ZDOK1_DP_N29 6-6E
F3 ZDOK1_DP_P30 6-6E
F4 ZDOK1_DP_N30 6-6E
F5 ZDOK1_DP_P31 6-6E
F6 ZDOK1_DP_N31 6-6E
F7 ZDOK1_DP_P32 6-6E
F8 ZDOK1_DP_N32 6-6E
F9 ZDOK1_DP_P33 6-7E
F10 ZDOK1_DP_N33 6-7E
F11 ZDOK1_DP_P34 6-7E
F12 ZDOK1_DP_N34 6-7E
F13 ZDOK1_DP_P35 6-7E
F14 ZDOK1_DP_N35 6-7E
F15 ZDOK1_DP_P36 6-7E
F16 ZDOK1_DP_N36 6-7E
F17 ZDOK1_DP_P37 6-7E
F18 ZDOK1_DP_N37 6-7E
F19 ZDOK1_CLK1_P 6-7B
F20 ZDOK1_CLK1_N 6-7B
6367550-5

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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6-19-2008_14:43

PATH PATH

ROACH_ADC_1

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

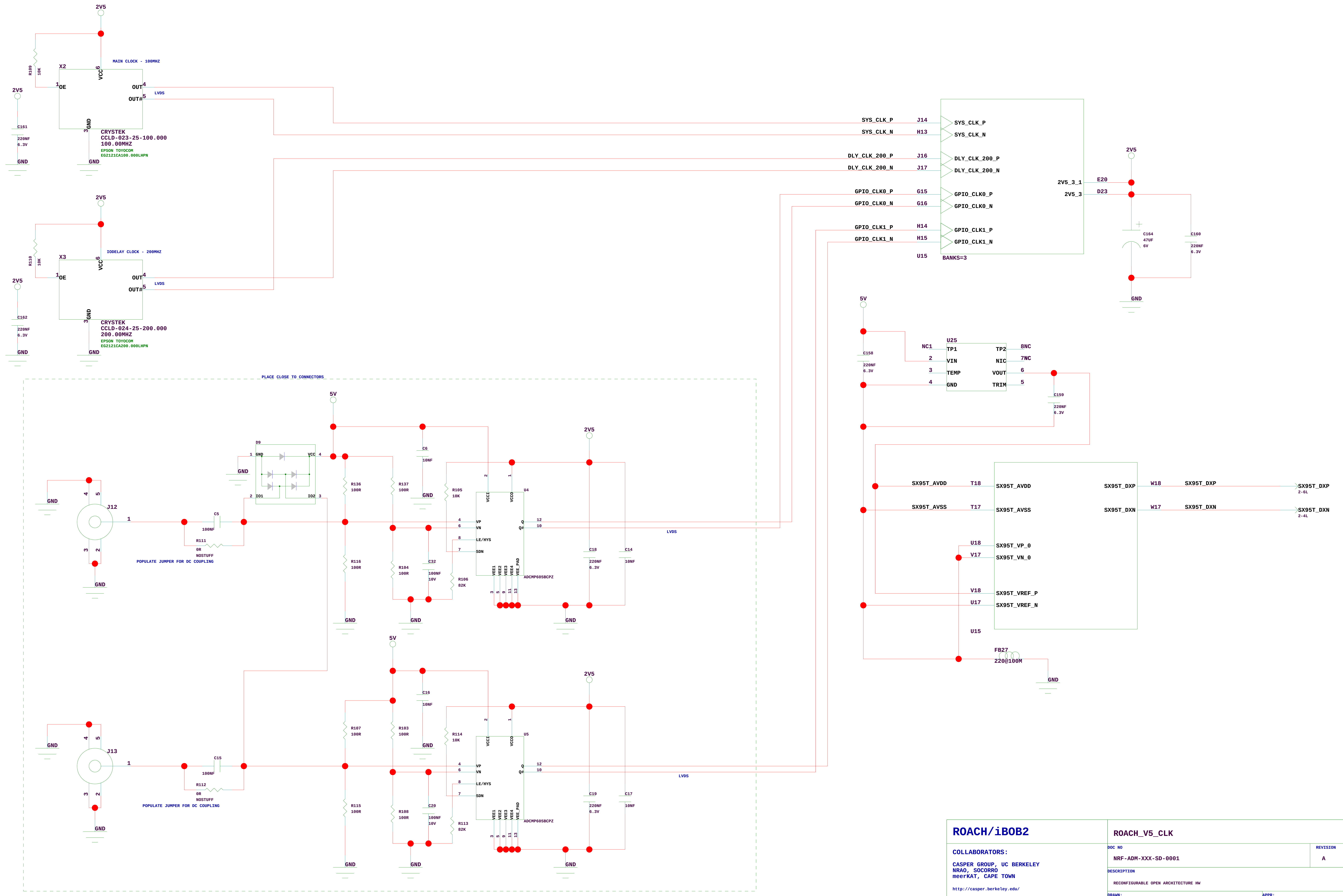
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 6 OF 25


2V5
R109
10K
X2
1 OE
VCC 6
MAIN CLOCK - 100MHZ
OUT 4
OUT# 5
LVDS
C161
220NF
6.3V
GND
3 GND
CRYSTEK
CCLD-023-25-100.000
100.00MHZ
EPSON TOYOCOM
EG2121CA100.000LHPN
R110
10K
X3
IODELAY CLOCK - 200MHZ
C162
CRYSTEK
CCLD-024-25-200.000
200.00MHZ
EG2121CA200.000LHPN
SYS_CLK_P J14
SYS_CLK_N H13
DLY_CLK_200_P J16
DLY_CLK_200_N J17
GPIO_CLK0_P G15
GPIO_CLK0_N G16
GPIO_CLK1_P H14
GPIO_CLK1_N H15
U15
BANKS=3
2V5_3_1 E20
2V5_3 D23
C164
47UF
6V
C160
220NF
6.3V
5V
C158
U25
NC1 TP1
2 VIN
3 TEMP
4 GND
TP2 8NC
NIC 7NC
VOUT 6
TRIM 5
C159
SX95T_AVDD T18
SX95T_AVSS T17
U18 SX95T_VP_0
V17 SX95T_VN_0
V18 SX95T_VREF_P
U17 SX95T_VREF_N
SX95T_DXP W18
SX95T_DXN W17
SX95T_DXP 2-6L
SX95T_DXN 2-4L
FB27
220@100M
PLACE CLOSE TO CONNECTORS
J12
1
D9
1 GND
VCC 4
2 IO1
IO2 3
C5
100NF
R111
0R
NOSTUFF
POPULATE JUMPER FOR DC COUPLING
C6
10NF
R136 100R
R137 100R
R116 100R
R104 100R
R105 10K
R106 82K
C32
100NF
10V
U4
VCCI
VCCO
VP
VN
LE/HYS
SDN
Q 12
Q# 10
VEE1 VEE2 VEE3 VEE4 VEE_PAD
3 5 9 11 13
ADCMP605BCPZ
C18
220NF
6.3V
C14
10NF
J13
C15
R112
C16
R107 100R
R103 100R
R114 10K
R115 100R
R108 100R
R113 82K
C20
U5
C19
C17

ROAACH/iBOB2

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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PATH PATH

ROACH_V5_CLK

DOC NO
NRF-ADM-XXX-SD-0001

REVISION
A

DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 7 OF 25

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
PLACEMENT: CLOSEST TO FPGA PIN
U15
MGTAVCC_126
MGTAVCC_126_1
MGTAVCCPLL_126
MGTAVTTRX_126
MGT_126_REF_CLK_P
MGT_126_REF_CLK_N
MGTRX0_126_P
MGTRX0_126_N
MGTRX1_126_P
MGTRX1_126_N
MGTAVTTTX_126_1
MGTAVTTTX_126
MGTTX0_126_P
MGTTX0_126_N
MGTTX1_126_P
MGTTX1_126_N
MGTAVCC_122
MGTAVCC_122_1
MGTAVCCPLL_122
MGTAVTTRX_122
MGT_122_REF_CLK_P
MGT_122_REF_CLK_N
MGTRX0_122_P
MGTRX0_122_N
MGTRX1_122_P
MGTRX1_122_N
MGTAVTTTX_122_1
MGTAVTTTX_122
MGTTX0_122_P
MGTTX0_122_N
MGTTX1_122_P
MGTTX1_122_N
MGTAVCC_118
MGTAVCC_118_1
MGTAVCCPLL_118
MGTAVTTRX_118
MGT_118_REF_CLK_P
MGT_118_REF_CLK_N
MGTRX0_118_P
MGTRX0_118_N
MGTRX1_118_P
MGTRX1_118_N
MGTAVTTTX_118_1
MGTAVTTTX_118
MGTTX0_118_P
MGTTX0_118_N
MGTTX1_118_P
MGTTX1_118_N
MGTAVCC_114
MGTAVCC_114_1
MGTAVCCPLL_114
MGTAVTTRX_114
MGT_114_REF_CLK_P
MGT_114_REF_CLK_N
MGTRX0_114_P
MGTRX0_114_N
MGTRX1_114_P
MGTRX1_114_N
MGTAVTTTX_114
MGTAVTTTX_114_1
MGTTX0_114_P
MGTTX0_114_N
MGTTX1_114_P
MGTTX1_114_N
2V5
FB26
220@100M
X1
OE
VCC
OUT
OUT#
GND
JP6
CCLD-023-25-156.250
156.25MHZ
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
SY89832UMI
3V3
P3
FCN-268F036-G/3DB
SIG_GND1
SIG_GND2
SIG_GND3
SIG_GND4
SIG_GND5
SIG_GND6
SIG_GND7
SIG_GND8
SIG_GND9
ODIS0
ODIS1
FAULT0
FAULT1
G4 AND G8 CONNECTED IN
2X2 MODULE
OPTICAL MODULE FAULT - RED LED
U21
U20
MAX9032AKA
U22
U23
AND2
SN74AHC1G08DCKR
U18
U19
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
TPS2031D
R99
R100
10K
C129
C128
C138
C90
C135
C136
C139
C91
10NF
100NF
4.7UF
16V
22UF
GND

ROACH/iBOB2

ROACH_TRANSCEIVERS0_1

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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PATH

DOC NO	REVISION
NRF-ADM-XXX-SD-0001	A

DESCRIPTION

RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN:	F KAPP	APPR:	
CHECKED:	E BAUERMEISTER	SHEET	8 OF 25

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB28 220@100M
FB30 220@100M
FB31 220@100M
MGTAVCC_120
MGTAVCCPLL_120
MGTAVTTRX_120
MGTAVCC_112
MGTAVCC_112_1
MGTAVCCPLL_112
MGTAVTTRX_112
MGT_112_REF_CLK_P
MGT_112_REF_CLK_N
MGTRX0_112_P
MGTRX0_112_N
MGTRX1_112_P
MGTRX1_112_N
U15
PLACEMENT: CLOSEST TO FPGA PIN
MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT
MGTRREF
MGT_VTRXC
V4 MGTRREF
V5 MGTAVTTRXC
R56 49.9R
FB25 220@100M
FB32 220@100M
MGTAVTTTX_112
MGTAVTTTX_112_1
M3
U3 MGTAVTTTX_120
C126 220NF 6.3V
C173 220NF 6.3V
GND
MGTTX0_112_P
MGTTX0_112_N
MGTTX1_112_P
MGTTX1_112_N
M2 MGTTX0_120_P
N2 MGTTX0_120_N
U2 MGTTX1_120_P
T2 MGTTX1_120_N
2V5
FB52 220@100M
C248 220NF 6.3V
R131 10K
X4
OE
VCC
OUT
OUT#
GND
JP9
CCLD-023-25-156.250
156.25MHZ
MGT_REFCLK_Q2_P
MGT_REFCLK_Q2_N
C79 220NF 6.3V
C78 220NF 6.3V
C76 10NF 6.3V
C77 10NF 6.3V
U26
VCC1
VCC2
IN
VT
VREF-AC
IN#
EN
EXP_PAD
NC
Q0
Q0#
Q1
Q1#
Q2
Q2#
Q3
Q3#
SY89832UMI
C103 100NF 6.3V MGT_REFCLK_Q2_0_P 9-10D
C99 100NF 6.3V MGT_REFCLK_Q2_0_N 9-10D
C80 100NF 6.3V MGT_REFCLK_Q2_1_P 9-6D
C81 100NF 6.3V MGT_REFCLK_Q2_1_N 9-6D
C82 100NF 6.3V MGT_REFCLK_Q2_2_P 9-4D
C83 100NF 6.3V MGT_REFCLK_Q2_2_N 9-4D
C95 100NF 6.3V MGT_REFCLK_Q2_3_P 9-1D
C97 100NF 6.3V MGT_REFCLK_Q2_3_N 9-1D
3V3
R122 150R
OPTICAL MODULE FAULT - RED LED
D4
JP7
P3
DL0P
DL0N
DL1P
DL1N
DL2P
DL2N
DL3P
DL3N
SL0P
SL0N
SL1P
SL1N
SL2P
SL2N
SL3P
SL3N
SIG_GND1
SIG_GND2
SIG_GND3
SIG_GND4
SIG_GND5
SIG_GND6
SIG_GND7
SIG_GND8
SIG_GND9
ODIS2
FAULT2
R123 10K
C240 10NF
C242 10NF
G4 AND G6 CONNECTED IN
2X2 MODULE
FCN-268F036-G/3DB
R121 5K1
R120 3K9
R119 6K8
R118 3K9
U34
IN-
IN+
OUT
MAX9032AKA
U36
AND2
SN74AHC1G08DCKR
C241 10NF
HIGH-SPEED DIFFERENTIAL VIAS
V35
V34
V37
V39
V36
V1
V38
V40
C183 10NF 25V
C184 10NF 25V
C186 10NF 25V
C185 10NF 25V
FB38 220@100M
FB36 220@100M
FB37 220@100M
MGTAVCC_122
MGTAVCCPLL_122
MGTAVTTRX_122
MGTAVCC_116
MGTAVCC_116_1
MGTAVCCPLL_116
MGTAVTTRX_116
C179 220NF 6.3V
C178 220NF 6.3V
C177 220NF 6.3V
MGT_REFCLK_Q2_1_P
MGT_REFCLK_Q2_1_N
MGT_116_REF_CLK_P
MGT_116_REF_CLK_N
MGTRX0_122_P
MGTRX0_122_N
MGTRX1_122_P
MGTRX1_122_N
MGTRX0_116_P
MGTRX0_116_N
MGTRX1_116_P
MGTRX1_116_N
MGTAVTTTX_116_1
MGTAVTTTX_116
MGTAVTTTX_122
FB35 220@100M
C175 220NF 6.3V
MGTTX0_116_P
MGTTX0_116_N
MGTTX1_116_P
MGTTX1_116_N
MGTTX0_122_P
MGTTX0_122_N
MGTTX1_122_P
MGTTX1_122_N
C251 10NF 25V
C252 10NF 25V
C250 10NF 25V
C249 10NF 25V
U28
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
TPS2031D
R117 10K
C239 10NF
C227 100NF
C167 4.7UF 16V
C165 22UF
FB44 220@100M
FB42 220@100M
FB43 220@100M
MGTAVCC_124
MGTAVCCPLL_124
MGTAVTTRX_124
MGTAVCC_120
MGTAVCC_120_1
MGTAVCCPLL_120
MGTAVTTRX_120
C220 220NF 6.3V
C215 220NF 6.3V
C212 220NF 6.3V
MGT_REFCLK_Q2_2_P
MGT_REFCLK_Q2_2_N
MGT_120_REF_CLK_P
MGT_120_REF_CLK_N
MGTRX0_124_P
MGTRX0_124_N
MGTRX1_124_P
MGTRX1_124_N
MGTRX0_120_P
MGTRX0_120_N
MGTRX1_120_P
MGTRX1_120_N
MGTAVTTTX_120_1
MGTAVTTTX_120
MGTAVTTTX_124
FB41 220@100M
C213 220NF 6.3V
MGTTX0_124_P
MGTTX0_124_N
MGTTX1_124_P
MGTTX1_124_N
MGTTX0_120_P
MGTTX0_120_N
MGTTX1_120_P
MGTTX1_120_N
C187 10NF 25V
C188 10NF 25V
C189 10NF 25V
C190 10NF 25V
V49
V51
V53
V55
V50
V52
V54
V56
R125 150R
R124 10K
C245 10NF
C243 10NF
ODIS3
FAULT3
R126 5K1
R127 3K9
R128 6K8
R129 3K9
U30
U37
C244 10NF
FB49 220@100M
FB51 220@100M
FB50 220@100M
MGTAVCC_126
MGTAVCCPLL_126
MGTAVTTRX_126
MGTAVCC_124
MGTAVCC_124_1
MGTAVCCPLL_124
MGTAVTTRX_124
C225 220NF 6.3V
C191 220NF 6.3V
C226 220NF 6.3V
MGT_REFCLK_Q2_3_P
MGT_REFCLK_Q2_3_N
MGT_124_REF_CLK_P
MGT_124_REF_CLK_N
MGTRX0_126_P
MGTRX0_126_N
MGTRX1_126_P
MGTRX1_126_N
MGTRX0_124_P
MGTRX0_124_N
MGTRX1_124_P
MGTRX1_124_N
MGTAVTTTX_124_1
MGTAVTTTX_124
MGTAVTTTX_126
FB46 220@100M
C223 220NF 6.3V
MGTTX0_126_P
MGTTX0_126_N
MGTTX1_126_P
MGTTX1_126_N
MGTTX0_124_P
MGTTX0_124_N
MGTTX1_124_P
MGTTX1_124_N
C256 10NF 25V
C255 10NF 25V
C254 10NF 25V
C253 10NF 25V
U29
TPS2031D
R130 10K
C246 10NF
C247 100NF
C168 4.7UF 16V
C166 22UF

ROACH/iBOB2

ROACH_TRANSCEIVERS2_3

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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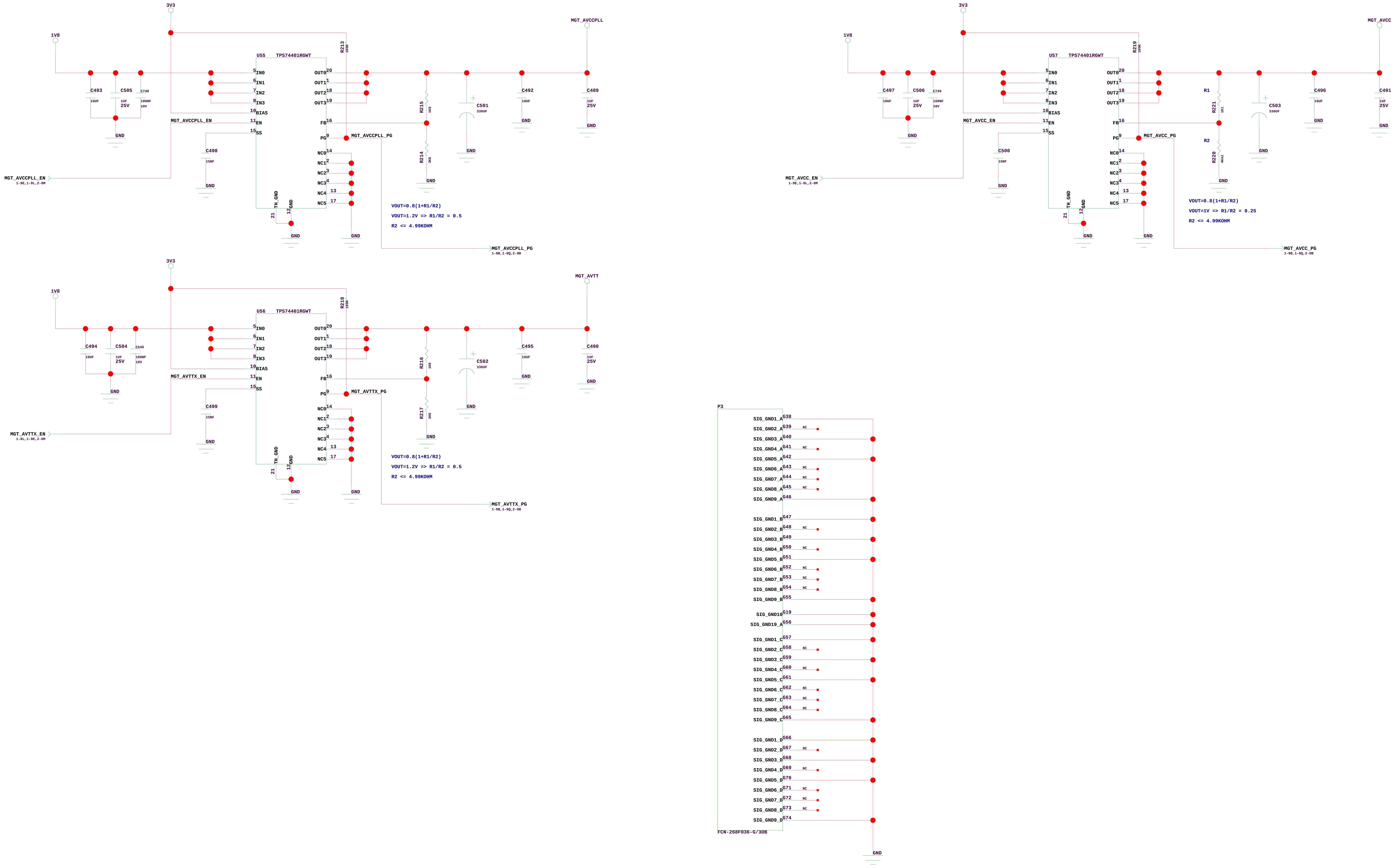
PATH PATH

DOC NO	REVISION
NRF-ADM-XXX-SD-0001	A

DESCRIPTION

RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN:	F KAPP	APPR:	
CHECKED:	E BAUERMEISTER	SHEET	9 OF 25


3V3
1V8
MGT_AVCCPLL
U55 TPS74401RGWT
5 IN0
6 IN1
7 IN2
8 IN3
10 BIAS
11 EN
15 SS
OUT0 20
OUT1 1
OUT2 18
OUT3 19
FB 16
PG 9
NC0 14
NC1 2
NC2 3
NC3 4
NC4 13
NC5 17
TH_GND 21
GND 12
R213 100K
C493 10UF
C505 1UF 25V
C748 100NF 10V
MGT_AVCCPLL_EN
C498 15NF
R215 1K8
R214 3K6
C501 330UF
C492 10UF
C489 1UF 25V
MGT_AVCCPLL_PG
MGT_AVCCPLL_EN 1-9E,1-9L,2-0M
MGT_AVCCPLL_PG 1-8B,1-8Q,2-0B
GND
VOUT=0.8(1+R1/R2)
VOUT=1.2V => R1/R2 = 0.5
R2 <= 4.99KOHM
3V3
1V8
MGT_AVCC
U57 TPS74401RGWT
R219 100K
C497 10UF
C506 1UF 25V
C749 100NF 10V
MGT_AVCC_EN
C500 15NF
R1
R221 1K1
R2
R220 4K42
C503 330UF
C496 10UF
C491 1UF 25V
MGT_AVCC_PG
MGT_AVCC_EN 1-9E,1-9L,2-0M
MGT_AVCC_PG 1-9B,1-9Q,2-0B
VOUT=0.8(1+R1/R2)
VOUT=1V => R1/R2 = 0.25
R2 <= 4.99KOHM
3V3
1V8
MGT_AVTT
U56 TPS74401RGWT
R218 100K
C494 10UF
C504 1UF 25V
C546 100NF 10V
MGT_AVTTX_EN
C499 15NF
R216 1K8
R217 3K6
C502 330UF
C495 10UF
C490 1UF 25V
MGT_AVTTX_PG
MGT_AVTTX_EN 1-8L,1-9E,2-0M
MGT_AVTTX_PG 1-9B,1-9Q,2-0B
VOUT=0.8(1+R1/R2)
VOUT=1.2V => R1/R2 = 0.5
R2 <= 4.99KOHM
P3
SIG_GND1_A G38
SIG_GND2_A G39 NC
SIG_GND3_A G40
SIG_GND4_A G41 NC
SIG_GND5_A G42
SIG_GND6_A G43 NC
SIG_GND7_A G44 NC
SIG_GND8_A G45 NC
SIG_GND9_A G46
SIG_GND1_B G47
SIG_GND2_B G48 NC
SIG_GND3_B G49
SIG_GND4_B G50 NC
SIG_GND5_B G51
SIG_GND6_B G52 NC
SIG_GND7_B G53 NC
SIG_GND8_B G54 NC
SIG_GND9_B G55
SIG_GND10 G19
SIG_GND19_A G56
SIG_GND1_C G57
SIG_GND2_C G58 NC
SIG_GND3_C G59
SIG_GND4_C G60 NC
SIG_GND5_C G61
SIG_GND6_C G62 NC
SIG_GND7_C G63 NC
SIG_GND8_C G64 NC
SIG_GND9_C G65
SIG_GND1_D G66
SIG_GND2_D G67 NC
SIG_GND3_D G68
SIG_GND4_D G69 NC
SIG_GND5_D G70
SIG_GND6_D G71 NC
SIG_GND7_D G72 NC
SIG_GND8_D G73 NC
SIG_GND9_D G74
FCN-268F036-G/3DB
GND

ROACH/iBOB2

ROACH_TRANSCEIVERS_PSU

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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PATH PATH

DOC NO
NRF-ADM-XXX-SD-0001

REVISION
A

DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 10 OF 25

1V8
C388
C389
C390
C391
C392
C393
C394
C395
47UF
6V
C363
C362
C361
220NF
6.3V
GND
5V
U33
TPS51100DGQ
VIN
VLDOIN
VDDQSNS
S3
S5
VTT
VTTSNS
VTTREF
PPAD
PGND
R236
R235
10K
C467
4U7F
10V
C464
10UF
16V
C460
100NF
C22
22PF
C465
C466
R138
120R
CONNECT VTTSNS POINT TO CENTRE OF VTT ISLAND
VTT_0V9
VREF_0V9
VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
PLACE ONE 10uF CAPACITOR ON EITHER END OF ISLAND
C271
RP13
RP14
RP15
RP16
RP17
RP18
RP20
49.9R
CP20
CP21
CP22
CP23
CP24
CP25
CP27
100NF
C279
J15
879160001
PLACE AT MODULE VREF PIN
C364
C352
PLACE AT MODULE VDDSPD PIN
C366
PLACE AT MODULE VDD PINS
C378
C379
C380
C377
C382
C383
C384
C381
C385
C386
C387
VREF
VDDSPD
PLACE AT MODULE VDDQ PINS
C365
C367
C368
C369
C370
C371
C372
C373
C374
C375
C376
U15
R158
R157
R154
R153
R140
R141
R156
R155
49.9R
C353
C354
C355
C356
C357
C358
C359
C360
10NF
25V
R233
R234
4K7
R231
R232
C461
C462
C463
5PF
50V
DDR2_DIMM_SDA
DDR2_DIMM_SCL
DDR2_DIMM_RESET#
PAR_OUT
PAR_IN
NC

ROACH/iBOB2

ROACH_DDR2_DIMM

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
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DOC NO	REVISION
NRF-ADM-XXX-SD-0001	A

DESCRIPTION

RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

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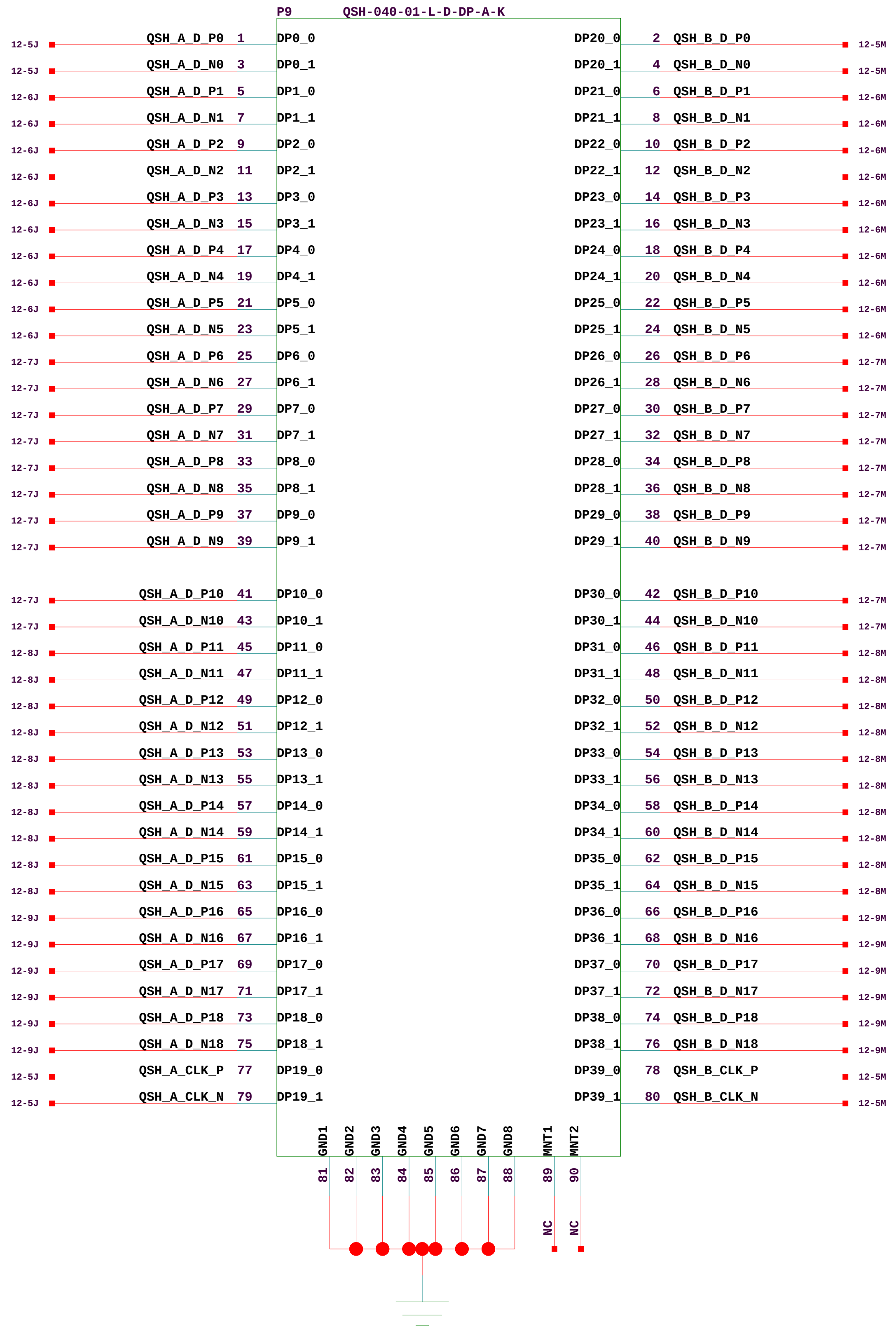
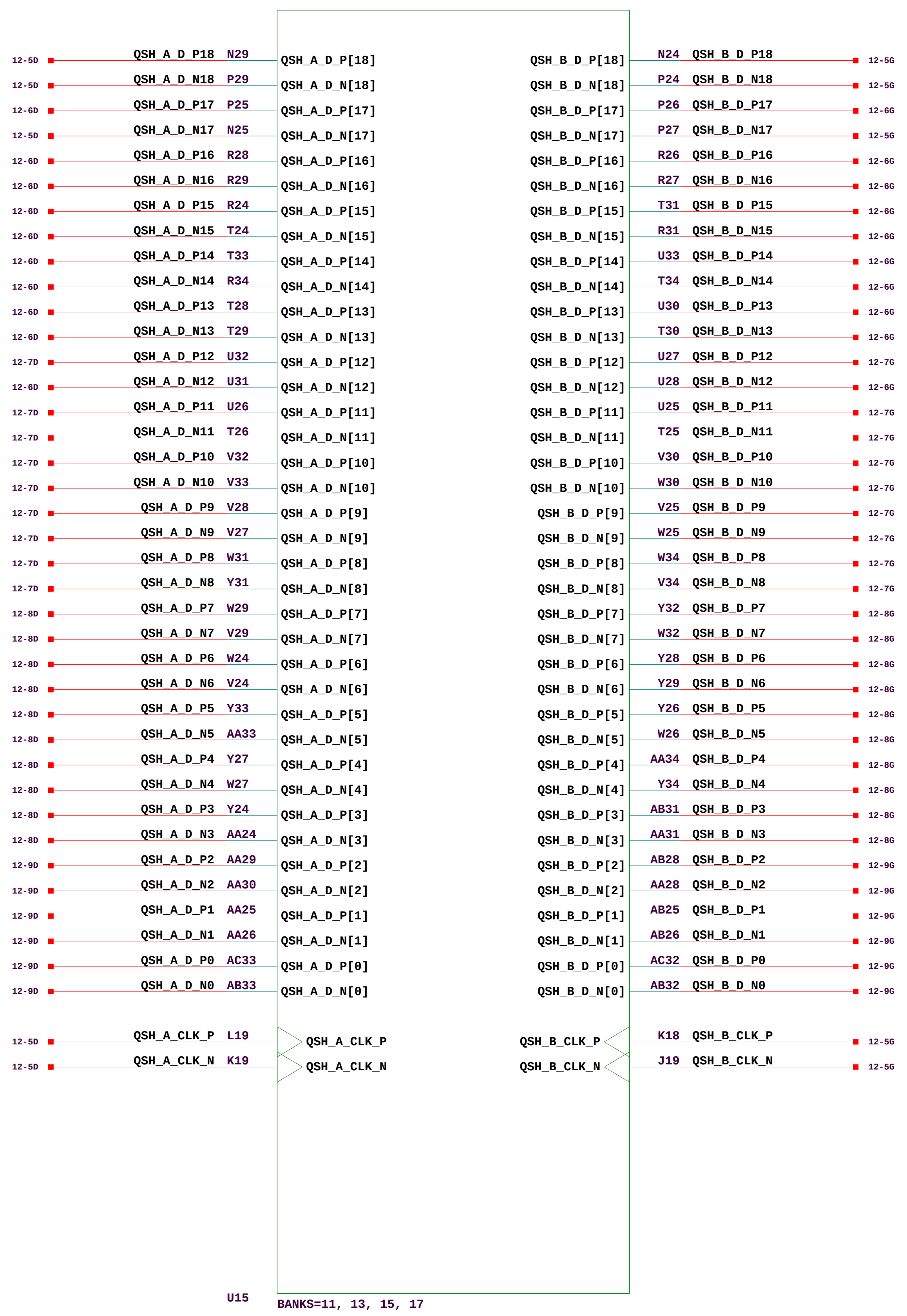
SHEET 11 OF 25


P9 QSH-040-01-L-D-DP-A-K
12-5J QSH_A_D_P0 1 DP0_0 | DP20_0 2 QSH_B_D_P0 12-5M
12-5J QSH_A_D_N0 3 DP0_1 | DP20_1 4 QSH_B_D_N0 12-5M
12-6J QSH_A_D_P1 5 DP1_0 | DP21_0 6 QSH_B_D_P1 12-6M
12-6J QSH_A_D_N1 7 DP1_1 | DP21_1 8 QSH_B_D_N1 12-6M
12-6J QSH_A_D_P2 9 DP2_0 | DP22_0 10 QSH_B_D_P2 12-6M
12-6J QSH_A_D_N2 11 DP2_1 | DP22_1 12 QSH_B_D_N2 12-6M
12-6J QSH_A_D_P3 13 DP3_0 | DP23_0 14 QSH_B_D_P3 12-6M
12-6J QSH_A_D_N3 15 DP3_1 | DP23_1 16 QSH_B_D_N3 12-6M
12-6J QSH_A_D_P4 17 DP4_0 | DP24_0 18 QSH_B_D_P4 12-6M
12-6J QSH_A_D_N4 19 DP4_1 | DP24_1 20 QSH_B_D_N4 12-6M
12-6J QSH_A_D_P5 21 DP5_0 | DP25_0 22 QSH_B_D_P5 12-6M
12-6J QSH_A_D_N5 23 DP5_1 | DP25_1 24 QSH_B_D_N5 12-6M
12-7J QSH_A_D_P6 25 DP6_0 | DP26_0 26 QSH_B_D_P6 12-7M
12-7J QSH_A_D_N6 27 DP6_1 | DP26_1 28 QSH_B_D_N6 12-7M
12-7J QSH_A_D_P7 29 DP7_0 | DP27_0 30 QSH_B_D_P7 12-7M
12-7J QSH_A_D_N7 31 DP7_1 | DP27_1 32 QSH_B_D_N7 12-7M
12-7J QSH_A_D_P8 33 DP8_0 | DP28_0 34 QSH_B_D_P8 12-7M
12-7J QSH_A_D_N8 35 DP8_1 | DP28_1 36 QSH_B_D_N8 12-7M
12-7J QSH_A_D_P9 37 DP9_0 | DP29_0 38 QSH_B_D_P9 12-7M
12-7J QSH_A_D_N9 39 DP9_1 | DP29_1 40 QSH_B_D_N9 12-7M
12-7J QSH_A_D_P10 41 DP10_0 | DP30_0 42 QSH_B_D_P10 12-7M
12-7J QSH_A_D_N10 43 DP10_1 | DP30_1 44 QSH_B_D_N10 12-7M
12-8J QSH_A_D_P11 45 DP11_0 | DP31_0 46 QSH_B_D_P11 12-8M
12-8J QSH_A_D_N11 47 DP11_1 | DP31_1 48 QSH_B_D_N11 12-8M
12-8J QSH_A_D_P12 49 DP12_0 | DP32_0 50 QSH_B_D_P12 12-8M
12-8J QSH_A_D_N12 51 DP12_1 | DP32_1 52 QSH_B_D_N12 12-8M
12-8J QSH_A_D_P13 53 DP13_0 | DP33_0 54 QSH_B_D_P13 12-8M
12-8J QSH_A_D_N13 55 DP13_1 | DP33_1 56 QSH_B_D_N13 12-8M
12-8J QSH_A_D_P14 57 DP14_0 | DP34_0 58 QSH_B_D_P14 12-8M
12-8J QSH_A_D_N14 59 DP14_1 | DP34_1 60 QSH_B_D_N14 12-8M
12-8J QSH_A_D_P15 61 DP15_0 | DP35_0 62 QSH_B_D_P15 12-8M
12-8J QSH_A_D_N15 63 DP15_1 | DP35_1 64 QSH_B_D_N15 12-8M
12-9J QSH_A_D_P16 65 DP16_0 | DP36_0 66 QSH_B_D_P16 12-9M
12-9J QSH_A_D_N16 67 DP16_1 | DP36_1 68 QSH_B_D_N16 12-9M
12-9J QSH_A_D_P17 69 DP17_0 | DP37_0 70 QSH_B_D_P17 12-9M
12-9J QSH_A_D_N17 71 DP17_1 | DP37_1 72 QSH_B_D_N17 12-9M
12-9J QSH_A_D_P18 73 DP18_0 | DP38_0 74 QSH_B_D_P18 12-9M
12-9J QSH_A_D_N18 75 DP18_1 | DP38_1 76 QSH_B_D_N18 12-9M
12-5J QSH_A_CLK_P 77 DP19_0 | DP39_0 78 QSH_B_CLK_P 12-5M
12-5J QSH_A_CLK_N 79 DP19_1 | DP39_1 80 QSH_B_CLK_N 12-5M
GND1 81
GND2 82
GND3 83
GND4 84
GND5 85
GND6 86
GND7 87
GND8 88
MNT1 89 NC
MNT2 90 NC


12-5D QSH_A_D_P18 N29 QSH_A_D_P[18] | QSH_B_D_P[18] N24 QSH_B_D_P18 12-5G
12-5D QSH_A_D_N18 P29 QSH_A_D_N[18] | QSH_B_D_N[18] P24 QSH_B_D_N18 12-5G
12-6D QSH_A_D_P17 P25 QSH_A_D_P[17] | QSH_B_D_P[17] P26 QSH_B_D_P17 12-6G
12-5D QSH_A_D_N17 N25 QSH_A_D_N[17] | QSH_B_D_N[17] P27 QSH_B_D_N17 12-5G
12-6D QSH_A_D_P16 R28 QSH_A_D_P[16] | QSH_B_D_P[16] R26 QSH_B_D_P16 12-6G
12-6D QSH_A_D_N16 R29 QSH_A_D_N[16] | QSH_B_D_N[16] R27 QSH_B_D_N16 12-6G
12-6D QSH_A_D_P15 R24 QSH_A_D_P[15] | QSH_B_D_P[15] T31 QSH_B_D_P15 12-6G
12-6D QSH_A_D_N15 T24 QSH_A_D_N[15] | QSH_B_D_N[15] R31 QSH_B_D_N15 12-6G
12-6D QSH_A_D_P14 T33 QSH_A_D_P[14] | QSH_B_D_P[14] U33 QSH_B_D_P14 12-6G
12-6D QSH_A_D_N14 R34 QSH_A_D_N[14] | QSH_B_D_N[14] T34 QSH_B_D_N14 12-6G
12-6D QSH_A_D_P13 T28 QSH_A_D_P[13] | QSH_B_D_P[13] U30 QSH_B_D_P13 12-6G
12-6D QSH_A_D_N13 T29 QSH_A_D_N[13] | QSH_B_D_N[13] T30 QSH_B_D_N13 12-6G
12-7D QSH_A_D_P12 U32 QSH_A_D_P[12] | QSH_B_D_P[12] U27 QSH_B_D_P12 12-7G
12-6D QSH_A_D_N12 U31 QSH_A_D_N[12] | QSH_B_D_N[12] U28 QSH_B_D_N12 12-6G
12-7D QSH_A_D_P11 U26 QSH_A_D_P[11] | QSH_B_D_P[11] U25 QSH_B_D_P11 12-7G
12-7D QSH_A_D_N11 T26 QSH_A_D_N[11] | QSH_B_D_N[11] T25 QSH_B_D_N11 12-7G
12-7D QSH_A_D_P10 V32 QSH_A_D_P[10] | QSH_B_D_P[10] V30 QSH_B_D_P10 12-7G
12-7D QSH_A_D_N10 V33 QSH_A_D_N[10] | QSH_B_D_N[10] W30 QSH_B_D_N10 12-7G
12-7D QSH_A_D_P9 V28 QSH_A_D_P[9] | QSH_B_D_P[9] V25 QSH_B_D_P9 12-7G
12-7D QSH_A_D_N9 V27 QSH_A_D_N[9] | QSH_B_D_N[9] W25 QSH_B_D_N9 12-7G
12-7D QSH_A_D_P8 W31 QSH_A_D_P[8] | QSH_B_D_P[8] W34 QSH_B_D_P8 12-7G
12-7D QSH_A_D_N8 Y31 QSH_A_D_N[8] | QSH_B_D_N[8] V34 QSH_B_D_N8 12-7G
12-8D QSH_A_D_P7 W29 QSH_A_D_P[7] | QSH_B_D_P[7] Y32 QSH_B_D_P7 12-8G
12-8D QSH_A_D_N7 V29 QSH_A_D_N[7] | QSH_B_D_N[7] W32 QSH_B_D_N7 12-8G
12-8D QSH_A_D_P6 W24 QSH_A_D_P[6] | QSH_B_D_P[6] Y28 QSH_B_D_P6 12-8G
12-8D QSH_A_D_N6 V24 QSH_A_D_N[6] | QSH_B_D_N[6] Y29 QSH_B_D_N6 12-8G
12-8D QSH_A_D_P5 Y33 QSH_A_D_P[5] | QSH_B_D_P[5] Y26 QSH_B_D_P5 12-8G
12-8D QSH_A_D_N5 AA33 QSH_A_D_N[5] | QSH_B_D_N[5] W26 QSH_B_D_N5 12-8G
12-8D QSH_A_D_P4 Y27 QSH_A_D_P[4] | QSH_B_D_P[4] AA34 QSH_B_D_P4 12-8G
12-8D QSH_A_D_N4 W27 QSH_A_D_N[4] | QSH_B_D_N[4] Y34 QSH_B_D_N4 12-8G
12-8D QSH_A_D_P3 Y24 QSH_A_D_P[3] | QSH_B_D_P[3] AB31 QSH_B_D_P3 12-8G
12-8D QSH_A_D_N3 AA24 QSH_A_D_N[3] | QSH_B_D_N[3] AA31 QSH_B_D_N3 12-8G
12-9D QSH_A_D_P2 AA29 QSH_A_D_P[2] | QSH_B_D_P[2] AB28 QSH_B_D_P2 12-9G
12-9D QSH_A_D_N2 AA30 QSH_A_D_N[2] | QSH_B_D_N[2] AA28 QSH_B_D_N2 12-9G
12-9D QSH_A_D_P1 AA25 QSH_A_D_P[1] | QSH_B_D_P[1] AB25 QSH_B_D_P1 12-9G
12-9D QSH_A_D_N1 AA26 QSH_A_D_N[1] | QSH_B_D_N[1] AB26 QSH_B_D_N1 12-9G
12-9D QSH_A_D_P0 AC33 QSH_A_D_P[0] | QSH_B_D_P[0] AC32 QSH_B_D_P0 12-9G
12-9D QSH_A_D_N0 AB33 QSH_A_D_N[0] | QSH_B_D_N[0] AB32 QSH_B_D_N0 12-9G
12-5D QSH_A_CLK_P L19 QSH_A_CLK_P | QSH_B_CLK_P K18 QSH_B_CLK_P 12-5G
12-5D QSH_A_CLK_N K19 QSH_A_CLK_N | QSH_B_CLK_N J19 QSH_B_CLK_N 12-5G
U15
BANKS=11, 13, 15, 17

ROACH/iBOB2

ROACH_DIFF_GPIO

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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DOC NO	REVISION
NRF-ADM-XXX-SD-0001	A

DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP
APPR:

CHECKED: E BAUERMEISTER

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PATH PATH

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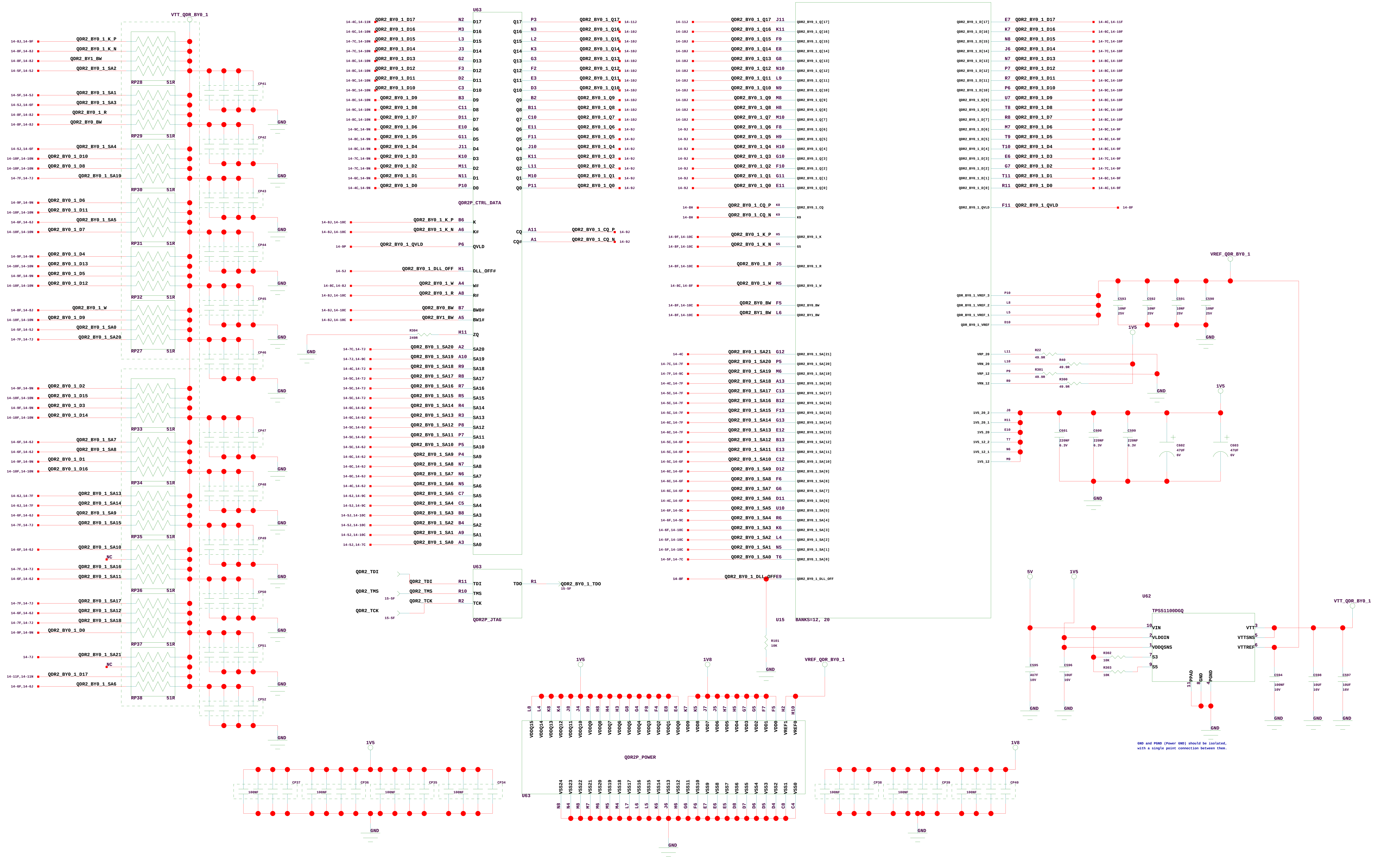
U13
U14
U10
U11
U12
U15
BANKS
74AVCH4T245DGVRE4
1DIR
2DIR
1OE#
2OE#
1A1
1A2
2A1
2A2
1B1
1B2
2B1
2B2
GND1
GND2
VCCA
VCCB
J2
N2520-6V0C-RB-WE
J9
J10
J11
R1
R2
R7
R8
R9
R47
R48
10K
R49
R50
499R
R43
R44
R45
R46
100R
CR7
CR8
CR9
CR10
GRN
C34
C35
C36
C37
C38
C39
C40
C41
C42
C43
C44
C45
220NF
6.3V
3V3
2V5
1V5
1V8
GND
NC
GPIOLVC33[4]
GPIOLVC33[3]
GPIOLVC33[0]
GPIOLVC15[7]
GPIOLVC15[6]
GPIOLVC15[5]
GPIOLVC15[4]
GPIOLVC15[3]
GPIOLVC15[2]
GPIOLVC15[1]
GPIOLVC15[0]
GPIOLVC25[0]
GPIOLVC25[1]
GPIOLVC25[2]
GPIOLVC25[3]
GPIOLVC25[4]
GPIOLVC25[5]
GPIOLVC25[6]
GPIOLVC25[7]
GPIOLVC25[8]
GPIOLVC25[9]
GPIOLVC25[10]
GPIOLVC25[11]
GPIOLVC18[0]
GPIOLVC18[1]
GPIOLVC18[2]
GPIOLVC18[3]
GPIOLVC18[4]
GPIOLVC18[5]
AE14
AE18
H12
J7
H7
J9
J10
B27
D24
E24
A26
M32
N33
N34
P34
R33
M33
L33
P32
N32
R32
P31
P30
AP26
AP25
AL25
AL24
AP22
AP21

GPIOLVC33[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

GPIOLVC33[3] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

IF CR10 IS ON, CLOCK CAPABLE GPIO'S ARE OUTPUTS

ROACH/iBOB2	ROACH_GPIO_MISC
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO NRF-ADM-XXX-SD-0001 — REVISION A DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
6-19-2008_14:43	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 13 OF 25


VTT_QDR_BY0_1
QDR2_BY0_1_K_P
QDR2_BY0_1_K_N
QDR2_BY1_BW
QDR2_BY0_1_SA2
QDR2_BY0_1_SA1
QDR2_BY0_1_SA3
QDR2_BY0_1_R
QDR2_BY0_BW
RP28 51R
RP29 51R
RP30 51R
RP31 51R
RP32 51R
RP27 51R
RP33 51R
RP34 51R
RP35 51R
RP36 51R
RP37 51R
RP38 51R
CP41
CP42
CP43
CP44
CP45
CP46
CP47
CP48
CP49
CP50
CP51
CP52
GND
NC
U63
QDR2P_CTRL_DATA
QDR2P_JTAG
QDR2P_POWER
QDR2_BY0_1_QVLD
QDR2_BY0_1_DLL_OFF
QDR2_BY0_1_W
QDR2_BY0_1_R
QDR2_BY0_1_CQ_P
QDR2_BY0_1_CQ_N
R304
249R
QDR2_TDI
QDR2_TMS
QDR2_TCK
QDR2_BY0_1_TDO
U15 BANKS=12, 20
R101 10K
VREF_QDR_BY0_1
1V5
1V8
5V
CP34
CP35
CP36
CP37
CP38
CP39
CP40
100NF
C590
C591
C592
C593
10NF 25V
R22 49.9R
R40 49.9R
R301 49.9R
R300 49.9R
C599
C600
C601
220NF 6.3V
C602 47UF 6V
C603 47UF 6V
U62
TPS51100DGQ
VIN
VLDOIN
VDDQSNS
S3
S5
VTT
VTTSNS
VTTREF
PPAD
GND
PGND
R302 10K
R303 10K
C595 4U7F 10V
C596 10UF 16V
C594 100NF 10V
C598 10UF 16V
C597 10UF 16V
GND and PGND (Power GND) should be isolated,
with a single point connection between them.

ROACH/iBOB2

ROACH_QDR2P_BY0_1

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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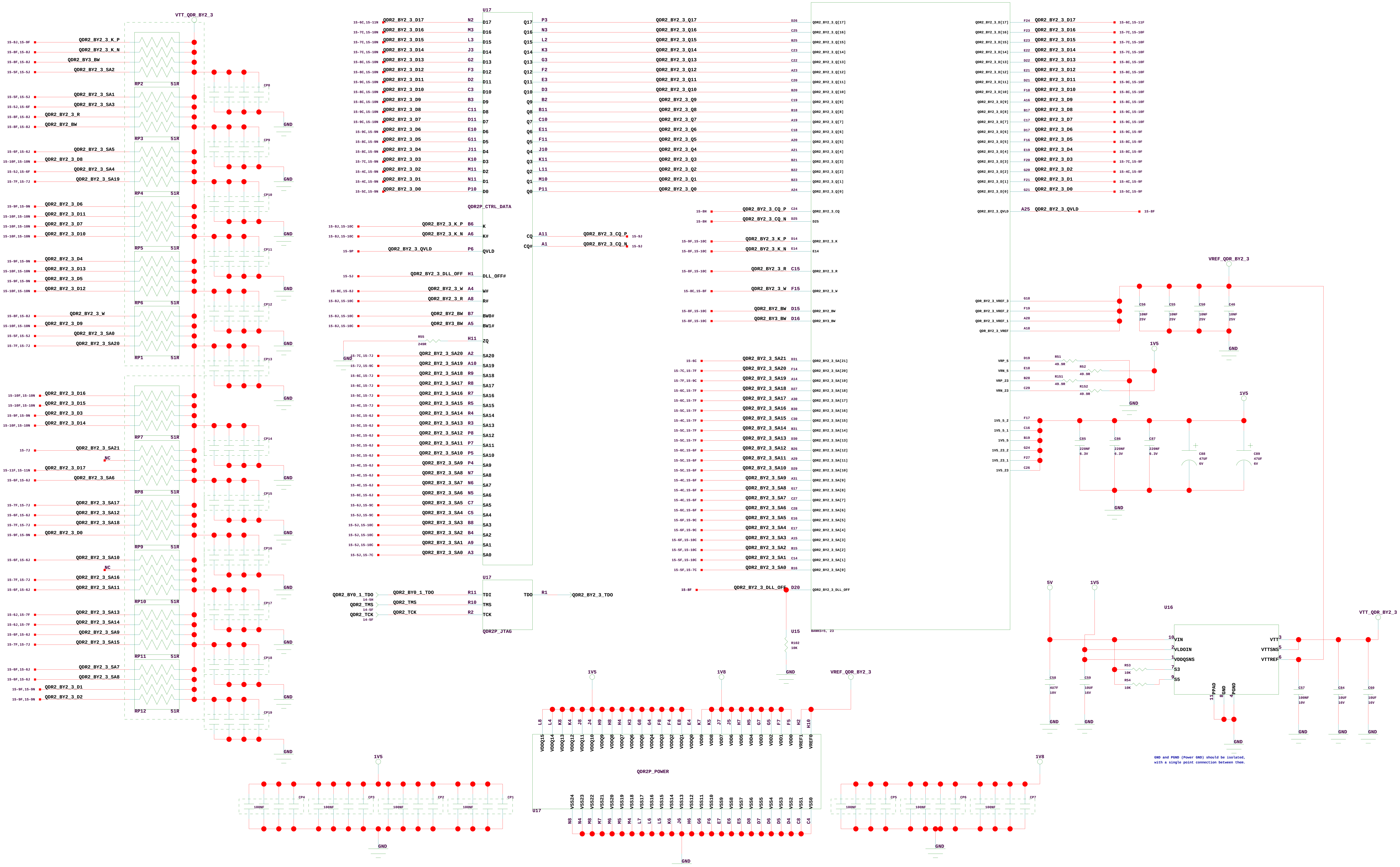
PATH PATH

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	14 OF 25


VTT_QDR_BY2_3
U17
QDR2P_CTRL_DATA
QDR2P_JTAG
QDR2P_POWER
U15
U16
VREF_QDR_BY2_3
VTT_QDR_BY2_3
RP1 51R
RP2 51R
RP3 51R
RP4 51R
RP5 51R
RP6 51R
RP7 51R
RP8 51R
RP9 51R
RP10 51R
RP11 51R
RP12 51R
R55 249R
R102 10K
R53 10K
R54 10K
R51 49.9R
R52 49.9R
R151 49.9R
R152 49.9R
C56 10NF 25V
C55 10NF 25V
C50 10NF 25V
C46 10NF 25V
C85 220NF 6.3V
C86 220NF 6.3V
C87 220NF 6.3V
C88 47UF 6V
C89 47UF 6V
C58 4U7F 10V
C59 10UF 16V
C57 100NF 10V
C84 10UF 16V
C60 10UF 16V
CP1 100NF
CP2 100NF
CP3 100NF
CP4 100NF
CP5 100NF
CP6 100NF
CP7 100NF
VIN
VLDOIN
VDDQSNS
S3
S5
VTT
VTTSNS
VTTREF
PPAD
GND
PGND
5V
1V5
1V8
GND
BANKS=5, 23
QDR2_BY2_3_K_P
QDR2_BY2_3_K_N
QDR3_BY2_BW
QDR2_BY2_3_R
QDR2_BY2_BW
QDR2_BY2_3_W
QDR2_BY2_3_QVLD
QDR2_BY2_3_DLL_OFF
QDR2_BY2_3_CQ_P
QDR2_BY2_3_CQ_N
QDR2_BY0_1_TDO
QDR2_TMS
QDR2_TCK
QDR2_BY2_3_TDO
QDR2_BY2_3_D0 … QDR2_BY2_3_D17
QDR2_BY2_3_Q0 … QDR2_BY2_3_Q17
QDR2_BY2_3_SA0 … QDR2_BY2_3_SA21
NC

GND and PGND (Power GND) should be isolated, with a single point connection between them.

ROACH/iBOB2

ROACH_QDR2P_BY2_3

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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DOC NO NRF-ADM-XXX-SD-0001

REVISION A

DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

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PATH PATH

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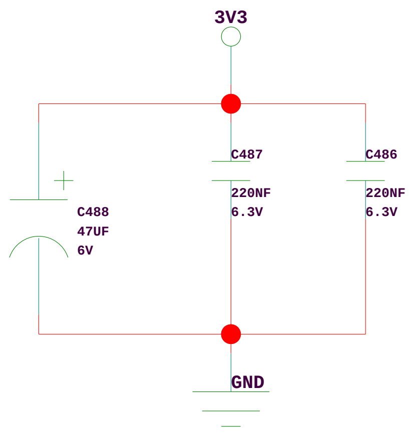
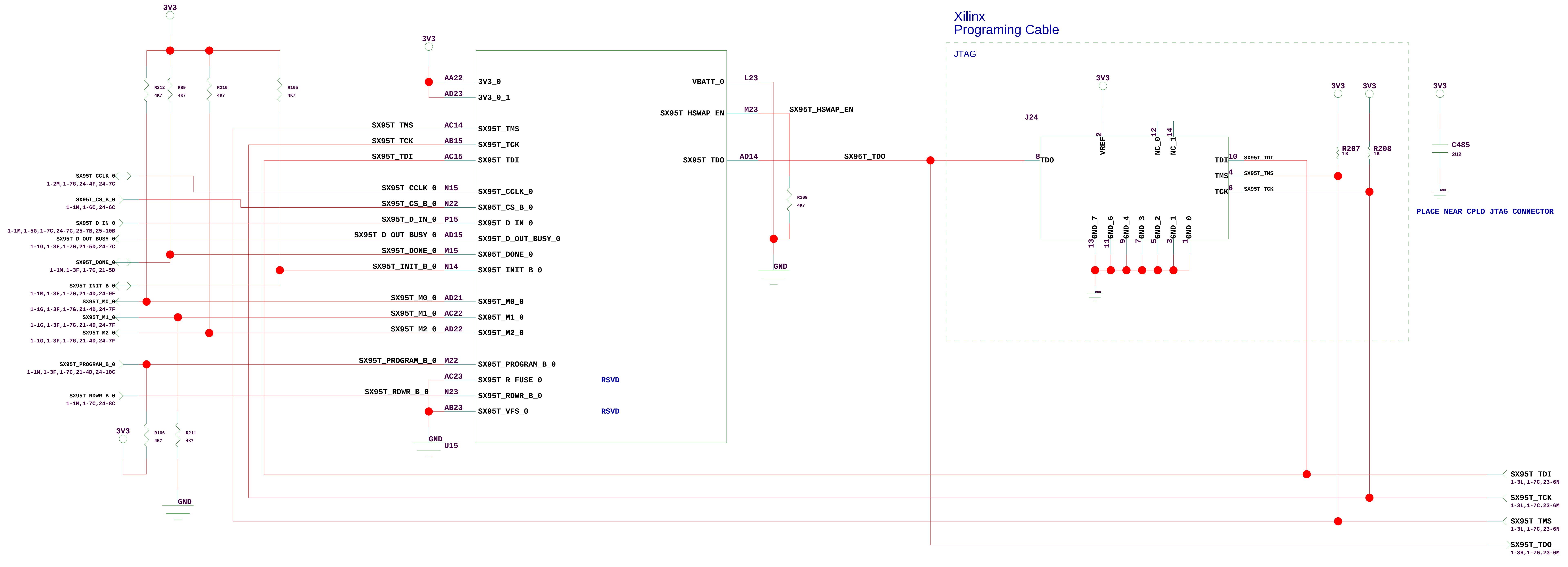
TBD

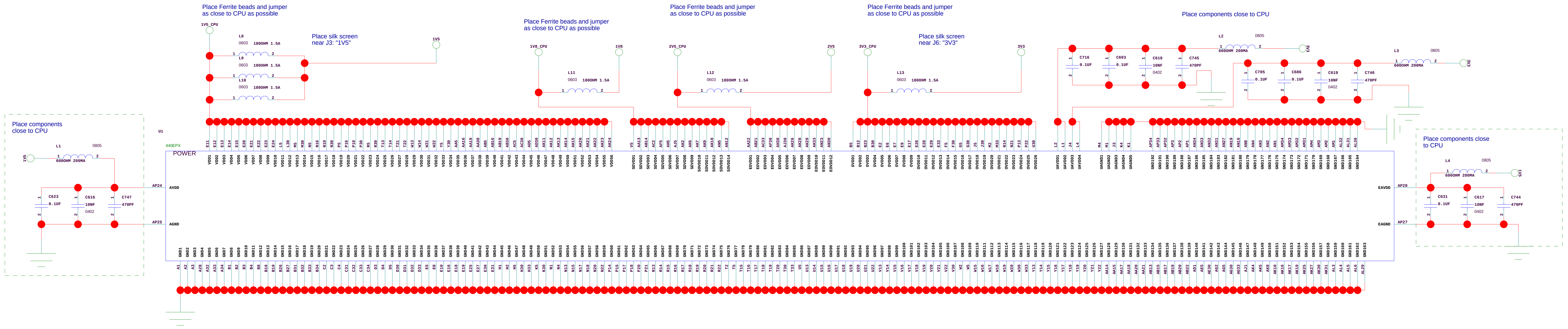
VALID CONFIGURATION MODES

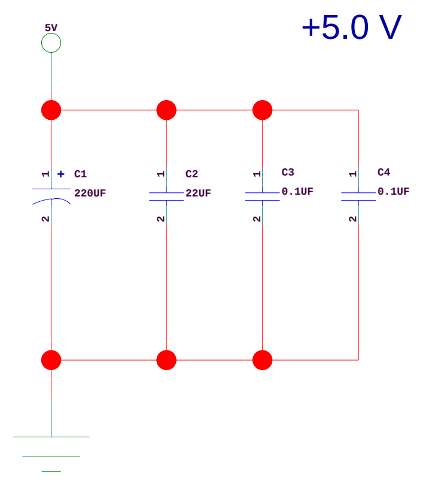
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

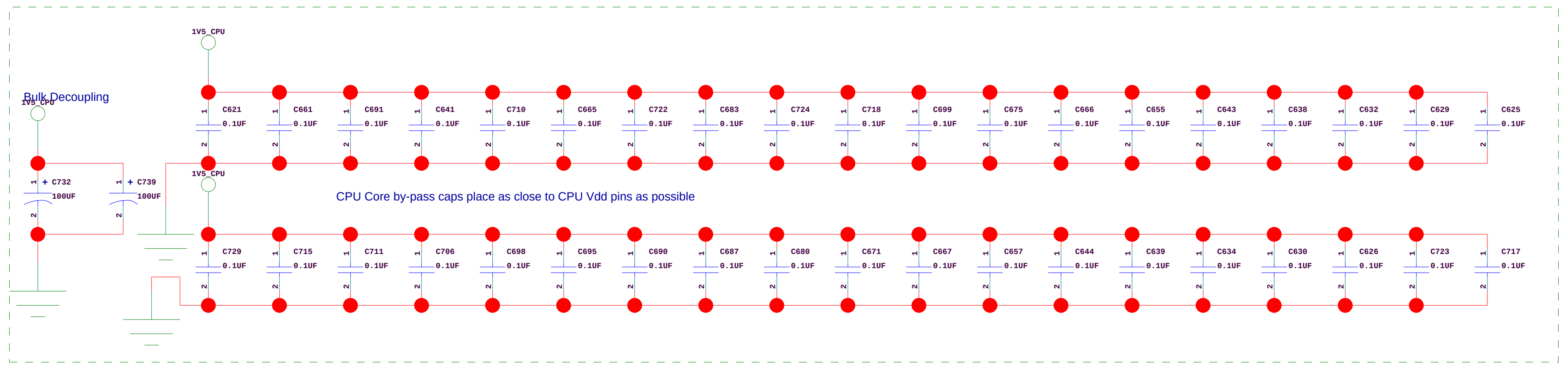

3V3
C487
220NF
6.3V
C486
220NF
6.3V
C488
47UF
6V
GND

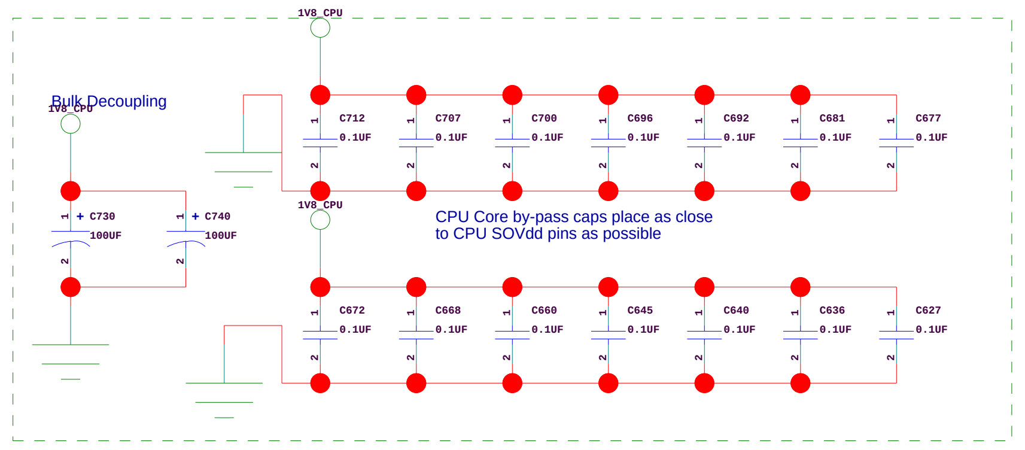

3V3
R212
4K7
R89
4K7
R210
4K7
R165
4K7
3V3
AA22
AD23
3V3_0
3V3_0_1
SX95T_TMS
AC14
SX95T_TMS
SX95T_TCK
AB15
SX95T_TCK
SX95T_TDI
AC15
SX95T_TDI
SX95T_CCLK_0
1-2M,1-7G,24-4F,24-7C
SX95T_CCLK_0
N15
SX95T_CCLK_0
SX95T_CS_B_0
1-1M,1-6C,24-6C
SX95T_CS_B_0
N22
SX95T_CS_B_0
SX95T_D_IN_0
1-1M,1-5G,1-7C,24-7C,25-7B,25-10B
SX95T_D_IN_0
P15
SX95T_D_IN_0
SX95T_D_OUT_BUSY_0
1-1G,1-3F,1-7G,21-5D,24-7C
SX95T_D_OUT_BUSY_0
AD15
SX95T_D_OUT_BUSY_0
SX95T_DONE_0
1-1M,1-3F,1-7G,21-5D
SX95T_DONE_0
M15
SX95T_DONE_0
SX95T_INIT_B_0
1-1M,1-3F,1-7G,21-4D,24-9F
SX95T_INIT_B_0
N14
SX95T_INIT_B_0
SX95T_M0_0
1-1G,1-3F,1-7G,21-4D,24-7F
SX95T_M0_0
AD21
SX95T_M0_0
SX95T_M1_0
1-1G,1-3F,1-7G,21-4D,24-7F
SX95T_M1_0
AC22
SX95T_M1_0
SX95T_M2_0
1-1G,1-3F,1-7G,21-4D,24-7F
SX95T_M2_0
AD22
SX95T_M2_0
SX95T_PROGRAM_B_0
1-1M,1-3F,1-7C,21-4D,24-10C
SX95T_PROGRAM_B_0
M22
SX95T_PROGRAM_B_0
AC23
SX95T_R_FUSE_0
RSVD
SX95T_RDWR_B_0
1-1M,1-7C,24-8C
SX95T_RDWR_B_0
N23
SX95T_RDWR_B_0
AB23
SX95T_VFS_0
RSVD
3V3
R166
4K7
R211
4K7
GND
GND
U15
VBATT_0
L23
SX95T_HSWAP_EN
M23
SX95T_HSWAP_EN
SX95T_TDO
AD14
SX95T_TDO
R209
4K7
GND
Xilinx
Programing Cable
JTAG
J24
3V3
8
TDO
2
VREF
12
NC_0
14
NC_1
TDI
10
TMS
4
TCK
6
SX95T_TDI
SX95T_TMS
SX95T_TCK
13
GND_7
11
GND_6
9
GND_4
7
GND_3
5
GND_2
3
GND_1
1
GND_0
GND
3V3
3V3
R207
1K
R208
1K
3V3
C485
2U2
GND
PLACE NEAR CPLD JTAG CONNECTOR
SX95T_TDI
1-3L,1-7C,23-6N
SX95T_TCK
1-3L,1-7C,23-6M
SX95T_TMS
1-3L,1-7C,23-6N
SX95T_TDO
1-3H,1-7G,23-6M

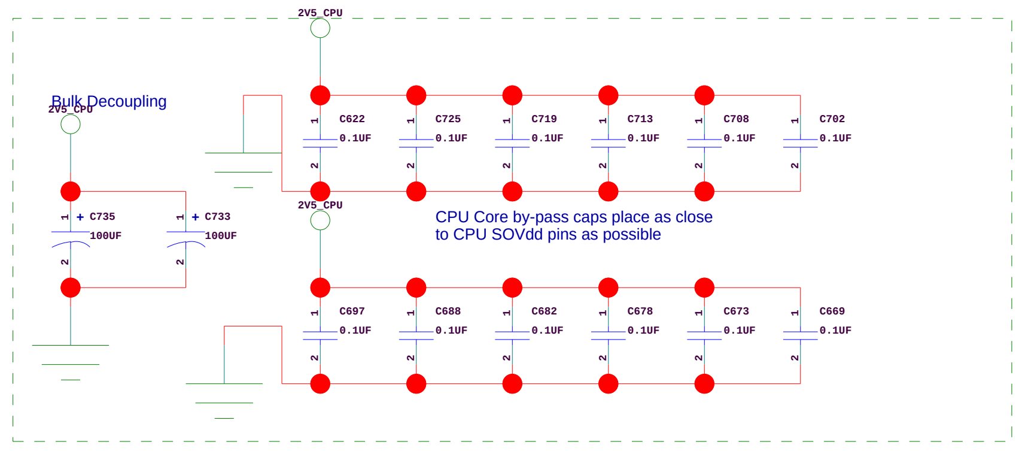
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-19-2008_14:43	DRAWN: F KAPP APPR:
PATH PATH	CHECKED: E BAUERMEISTER SHEET 16 OF 25

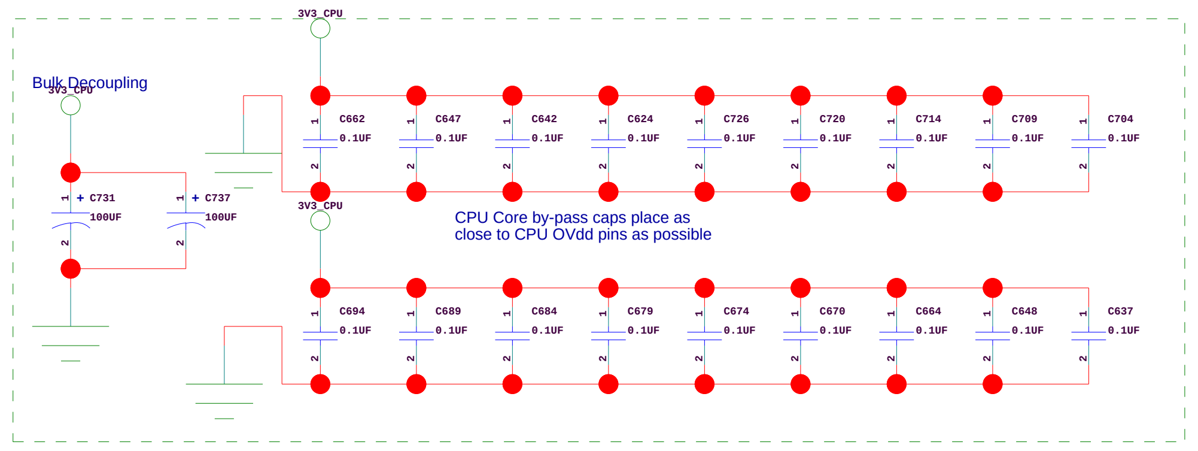

Place Ferrite beads and jumper as close to CPU as possible
Place silk screen near J3: "1V5"
Place Ferrite beads and jumper as close to CPU as possible
Place Ferrite beads and jumper as close to CPU as possible
Place Ferrite beads and jumper as close to CPU as possible
Place silk screen near J6: "3V3"
Place components close to CPU
Place components close to CPU
Place components close to CPU
440EPx
POWER
AVDD
AGND
EAVDD
EAGND

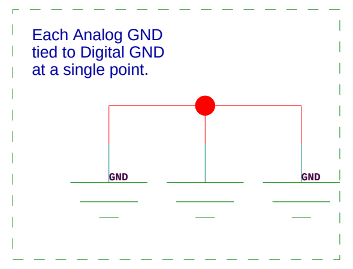

+5.0 V
5V
C1 220UF
C2 22UF
C3 0.1UF
C4 0.1UF


Bulk Decoupling
1V5_CPU
C732 1000UF
C730 100UF
CPU Core by-pass caps place as close to CPU Vdd pins as possible


Bulk Decoupling
1V8_CPU
CPU Core by-pass caps place as close to CPU SOVdd pins as possible


Bulk Decoupling
2V5_CPU
CPU Core by-pass caps place as close to CPU SOVdd pins as possible


Bulk Decoupling
3V3_CPU
CPU Core by-pass caps place as close to CPU OVdd pins as possible

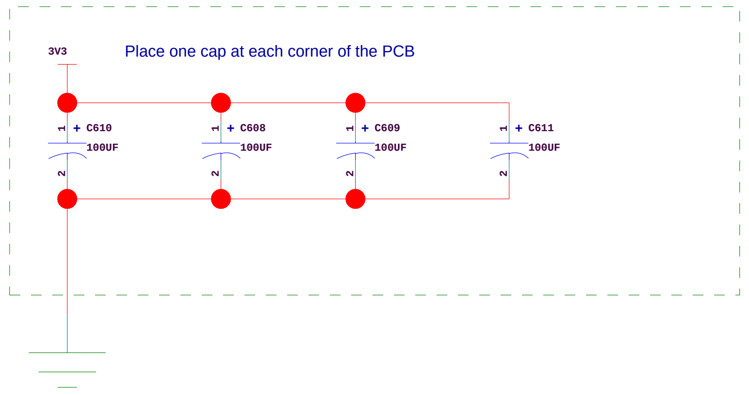

Each Analog GND tied to Digital GND at a single point.
GND
GND

REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	ROACH_PPC_POWER_1
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO NRF-ADM-XXX-SD-0001 REVISION A DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
6-19-2008_14:43 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 17 OF 25

REMOVED 3V3 GENERATION


Place one cap at each corner of the PCB
3V3
1
+ C610
100UF
2
1
+ C608
100UF
2
1
+ C609
100UF
2
1
+ C611
100UF
2

REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
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PATH PATH

ROACH_PPC_POWER_2

DOC NO
NRF-ADM-XXX-SD-0001

REVISION
A

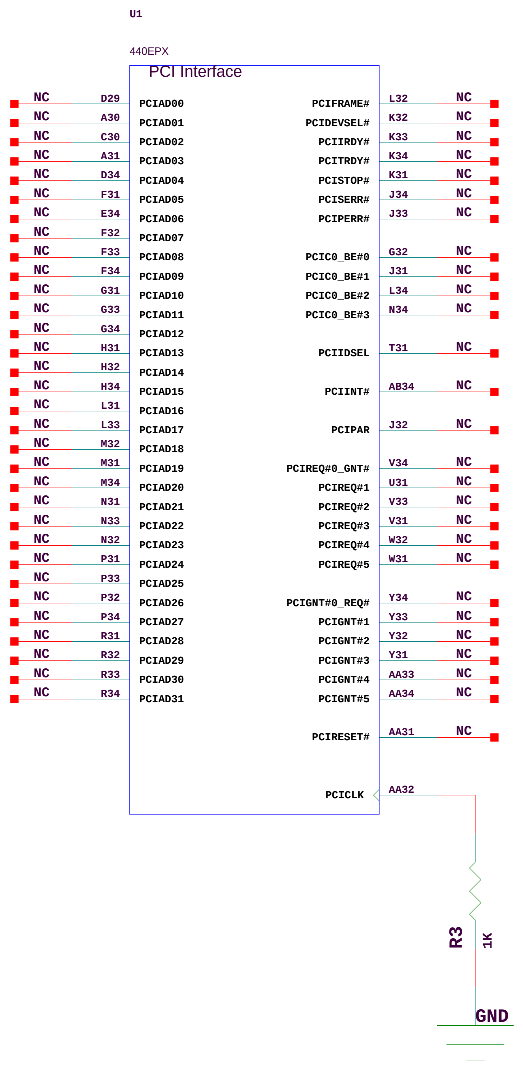
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN:
F KAPP

APPR:

CHECKED:
E BAUERMEISTER

SHEET
18 OF 25


U1
440EPX
PCI Interface
NC
D29
PCIAD00
NC
A30
PCIAD01
NC
C30
PCIAD02
NC
A31
PCIAD03
NC
D34
PCIAD04
NC
F31
PCIAD05
NC
E34
PCIAD06
NC
F32
PCIAD07
NC
F33
PCIAD08
NC
F34
PCIAD09
NC
G31
PCIAD10
NC
G33
PCIAD11
NC
G34
PCIAD12
NC
H31
PCIAD13
NC
H32
PCIAD14
NC
H34
PCIAD15
NC
L31
PCIAD16
NC
L33
PCIAD17
NC
M32
PCIAD18
NC
M31
PCIAD19
NC
M34
PCIAD20
NC
N31
PCIAD21
NC
N33
PCIAD22
NC
N32
PCIAD23
NC
P31
PCIAD24
NC
P33
PCIAD25
NC
P32
PCIAD26
NC
P34
PCIAD27
NC
R31
PCIAD28
NC
R32
PCIAD29
NC
R33
PCIAD30
NC
R34
PCIAD31
PCIFRAME#
L32
NC
PCIDEVSEL#
K32
NC
PCIIRDY#
K33
NC
PCITRDY#
K34
NC
PCISTOP#
K31
NC
PCISERR#
J34
NC
PCIPERR#
J33
NC
PCIC0_BE#0
G32
NC
PCIC0_BE#1
J31
NC
PCIC0_BE#2
L34
NC
PCIC0_BE#3
N34
NC
PCIIDSEL
T31
NC
PCIINT#
AB34
NC
PCIPAR
J32
NC
PCIREQ#0_GNT#
V34
NC
PCIREQ#1
U31
NC
PCIREQ#2
V33
NC
PCIREQ#3
V31
NC
PCIREQ#4
W32
NC
PCIREQ#5
W31
NC
PCIGNT#0_REQ#
Y34
NC
PCIGNT#1
Y33
NC
PCIGNT#2
Y32
NC
PCIGNT#3
Y31
NC
PCIGNT#4
AA33
NC
PCIGNT#5
AA34
NC
PCIRESET#
AA31
NC
PCICLK
AA32
R3
1K
GND

PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	ROACH_PPC_PCI	
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO NRF-ADM-XXX-SD-0001	REVISION A
	DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW	
6-19-2008_14:43	DRAWN: F KAPP	APPR:
PATH PATH	CHECKED: E BAUERMEISTER	SHEET 19 OF 25

U1
440EPX
Gig-Ethernet
RGMII0
ETHERNET MgL
GMC0_TXD0
GMC0_TXD1
GMC0_TXD2
GMC0_TXD3
GMC0_TXCTL
GMC0_TXCLK
GMCTXCLK
GMC0_RXD0
GMC0_RXD1
GMC0_RXD2
GMC0_RXD3
GMC0_RXCTL
GMC0_RXCLK
GMCMDCLK
GMCMDIO
GMCREFCLK
REJECTPKT0
REJECTPKT1
AM23
AL23
NC
R241
R239
R222
R237
R242
R223
22R
R240
R272
R273
R274
R275
R276
R277
R224
4K7
R267
1K
GMC0RXD0
GMC0RXD1
GMC0RXD2
GMC0RXD3
GMC0RXCTL
GMC0RXCLK
GMCREFCLK_125MHZ
GMCMDCLK
1-4E,20-3C
GMCMDIO
1-4E,20-3C
GETH0_RST#
1-2M,1-4B,24-10F
GETH0_INT#
1-3H,1-4E,23-7N
CLK_GETH0_25MHZ
1-3L,1-4B,23-5G
1-4E,20-4D
1-4E,20-4D
JP24
JP25
1V8
2V5
R263
R262
1R
C536
22UF
C511
10NF
C535
22UF
C512
10NF
C533
10NF
C534
10NF
C526
C527
C525
C528
C530
C529
C531
C532
C513
C514
C515
C516
C517
C518
C519
C520
C521
C522
C523
C524
100NF
U58
DP83865DVH
TXD0/TX0
TXD1/TX1
TXD2/TX2
TXD3/TX3
TX_EN/TXER
TX_CLK/RGMII_SEL1
GTX_CLK/TCK
CRS/RGMII_SEL0
COL
RXD0/RX0
RXD1/RX1
RXD2/RX2
RXD3/RX3
RX_DV/RCK
RX_ER/RXDV_ER
RX_CLK
MDC
MDIO
CLK_TO_MAC
RESET#
INTERRUPT#
CLK_IN
CLK_OUT
TDO
TDI
TCK
TMS
TRST#
MDIX_0P
MDIX_0N
MDIX_1P
MDIX_1N
MDIX_2P
MDIX_2N
MDIX_3P
MDIX_3N
R254
R255
R257
R256
R258
R259
R260
R261
49.9R
C507
C508
C509
C510
VDD_SEL_STRAP
MAC_CLK_EN_STRAP
MDIX_EN_STRAP
MULTI_EN_STRAP
LINK1000_LED/AN_EN_STRAP
LINK100_LED/DUPLEX_STRAP
LINK10_LED/MLED/SPEED1_STRAP
ACTIVITY_LED/SPEED0_STRAP
DUPLEX_LED/PHYADDR0_STRAP
PHYADDR1_STRAP
PHYADDR2_STRAP
PHYADDR3_STRAP
PHYADDR4_STRAP
LED_L1000
LED_L100
LED_L10
LED_ACT
LED_DUPLEX
R266
2K2
NOSTUFF
R265
R264
BG_REF
TX_TCLK
NON_IEEE_STRAP
RESERVED
R253
9K76
J25
HFJ11-1G02E-L12
GRN
YEL
G
Y
TD0P
TD0N
TD1P
TD2P
TD2N
TD1N
TD3P
TD3N
VCC
GND
MNT1
MNT2
CASE1
CASE2
C537
22UF
GND
Gig-Ethernet
RGMII1
GMC1_TXD0
GMC1_TXD1
GMC1_TXD2
GMC1_TXD3
GMC1_TXCTL
GMC1_TXCLK
GMC1_RXD0
GMC1_RXD1
GMC1_RXD2
GMC1_RXD3
GMC1_RXCTL
GMC1_RXCLK
JP10
JP11
JP12
JP13
JP14
JP15
JP16
JP17
JP18
JP19
JP20
JP21
JP22
JP23
R268
R269
R270
R271
R243
R244
R245
R246
R247
R248
R249
R250
R251
R252
330R
D6
D7
D8
D9
DUPLEX LED
L10 LED
L100 LED

Place nearest PHY pin 98

Place nearest PHY pin 100

Place nearest PHY pin 96

Place nearest PHY pin 101

Place as close to PHY CORE VDD power pins as possible

Place as close to PHY IO VDD power pins as possible

UNUSED SECOND ETHERNET MAC

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.
Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

CONFIRMED NC'S ON
PINS WITH AMCC TECH
SUPPORT IN EMAIL
DATED 2007/08/30

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place jumers in line with signals

Place components as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible.

Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5

Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

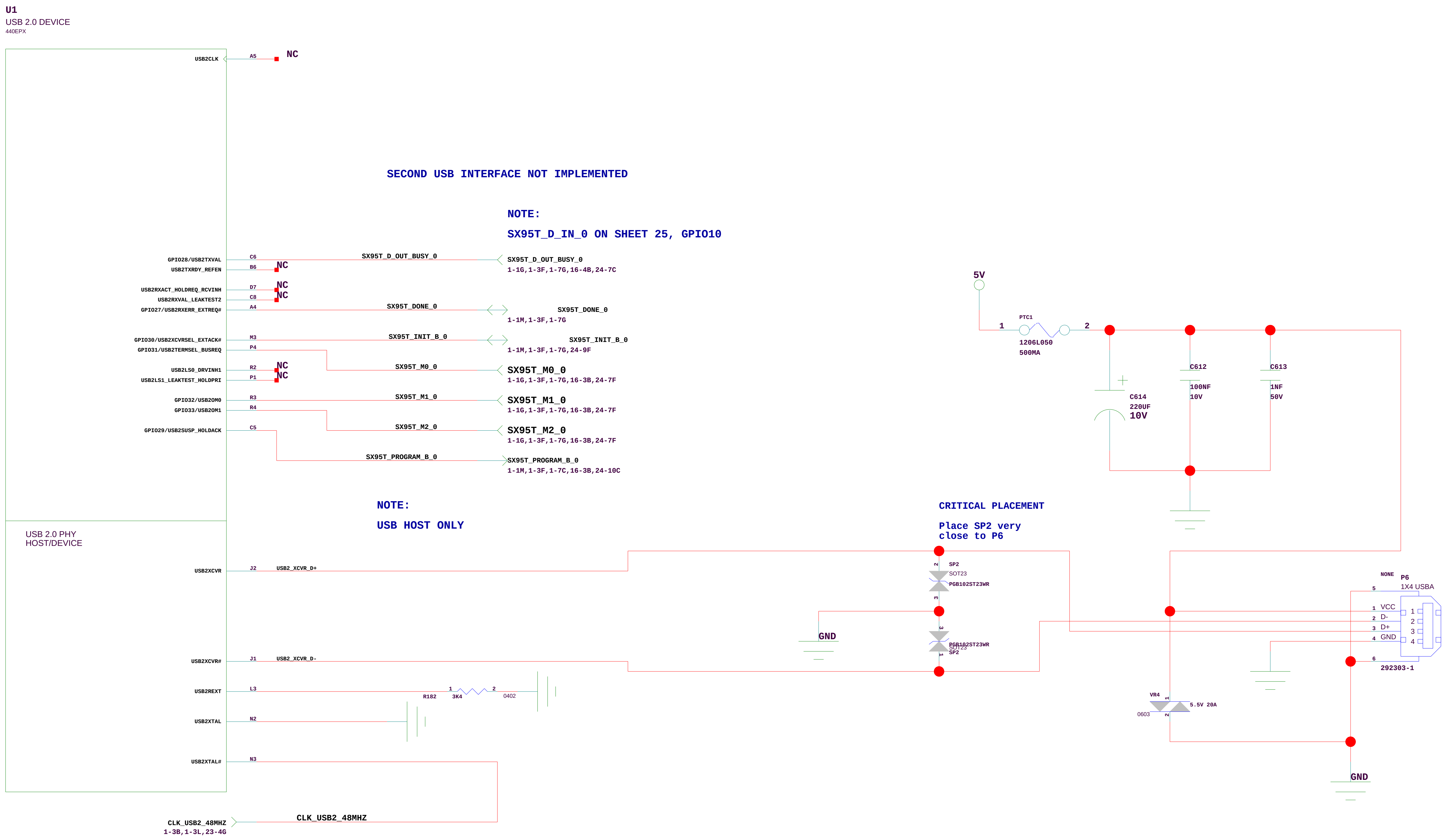
Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

JUMPER DEFAULTS

JP10, JP11	2 - 3	PHY ADD0 = 1
JP12, JP13	1 - 2	Adertised Modes 1000BASE-T, 100BASE-TX, 10BASE-T
JP14, JP15	1 - 2	
JP16, JP17	2 - 3	FULL DUPLEX
JP18, JP19	2 - 3	AUTO NEGOTIATION ENABLED
JP20-23	1 - 2	PHY ADD4:1 = 1111

ROACH/iBOB2	ROACH_PPC_ETH1	
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO NRF-ADM-XXX-SD-0001	REVISION A
	DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW	
6-19-2008_14:43	DRAWN: F KAPP	APPR:
PATH PATH	CHECKED: E BAUERMEISTER	SHEET 20 OF 25


U1
USB 2.0 DEVICE
440EPX
USB2CLK
A5
NC
GPIO28/USB2TXVAL
C6
SX95T_D_OUT_BUSY_0
SX95T_D_OUT_BUSY_0
1-1G,1-3F,1-7G,16-4B,24-7C
USB2TXRDY_REFEN
B6
NC
USB2RXACT_HOLDREQ_RCVINH
D7
NC
USB2RXVAL_LEAKTEST2
C8
NC
GPIO27/USB2RXERR_EXTREQ#
A4
SX95T_DONE_0
SX95T_DONE_0
1-1M,1-3F,1-7G
GPIO30/USB2XCVRSEL_EXTACK#
M3
SX95T_INIT_B_0
SX95T_INIT_B_0
1-1M,1-3F,1-7G,24-9F
GPIO31/USB2TERMSEL_BUSREQ
P4
SX95T_M0_0
SX95T_M0_0
1-1G,1-3F,1-7G,16-3B,24-7F
USB2LS0_DRVINH1
R2
NC
USB2LS1_LEAKTEST_HOLDPRI
P1
NC
GPIO32/USB2OM0
R3
SX95T_M1_0
SX95T_M1_0
1-1G,1-3F,1-7G,16-3B,24-7F
GPIO33/USB2OM1
R4
SX95T_M2_0
SX95T_M2_0
1-1G,1-3F,1-7G,16-3B,24-7F
GPIO29/USB2SUSP_HOLDACK
C5
SX95T_PROGRAM_B_0
SX95T_PROGRAM_B_0
1-1M,1-3F,1-7C,16-3B,24-10C
USB 2.0 PHY
HOST/DEVICE
USB2XCVR
J2
USB2_XCVR_D+
USB2XCVR#
J1
USB2_XCVR_D-
USB2REXT
L3
R182
1
3K4
2
0402
USB2XTAL
N2
USB2XTAL#
N3
CLK_USB2_48MHZ
1-3B,1-3L,23-4G
CLK_USB2_48MHZ
5V
PTC1
1
2
1206L050
500MA
C614
220UF
10V
C612
100NF
10V
C613
1NF
50V
SP2
SOT23
PGB102ST23WR
2
3
GND
3
1
PGB102ST23WR
SOT23
SP2
VR4
1
2
0603
5.5V 20A
NONE
P6
1X4 USBA
5
1 VCC
2 D-
3 D+
4 GND
1
2
3
4
6
292303-1
GND

SECOND USB INTERFACE NOT IMPLEMENTED

NOTE:

SX95T_D_IN_0 ON SHEET 25, GPIO10

NOTE:

USB HOST ONLY

CRITICAL PLACEMENT

Place SP2 very
close to P6

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
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PATH PATH

ROACH_PPC_USB

DOC NO
NRF-ADM-XXX-SD-0001

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DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

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CHECKED: E BAUERMEISTER

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VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
DDR_VTT
DDR_PA[15:0]
DDR_PDQ[63:0]
PPC_ECC[7:0]
DDR SDRAM
J8
RP24
RP23
RP22
RP21
RP25
RP26
RP19
DDR_VREF_0V9
Place parts as close to CPU as possible
U32
TPS51100DGQ
VIN
VLDOIN
VDDQSNS
S3
S5
VTT
VTTSNS
VTTREF
PGND
U6
CDCU877ARHAT
I2C0_SCLK
I2C0_SDATA
PPC_DDR2_RESET_N
PPC_DDR2_ERROR
TP4
TP5
879160001
PLACE NEAREST DDR2 MODULE PINS

PowerPC DRAM Interface:

DDR2 240 pin DIMM

72 bit ECC

Unbuffered and Registered DIMMs supported

Up to 2GB supported

CAS Latencies: 2, 2..5 or 3

Clock Frequencies: 133MHz to 166MHz

Single Ended Strobes

PPC DDR2 LAYOUT NOTES

ROUTE ALL DDR CLOCKS AS LENGTH MATCHED ONLY

ROUTE DDR_PCLKOUT NETS 500PS LONGER THAN ADDR, CMD CTRL SIGNAL NETS
To compensate for additional loading when using unbuffered DIMM's
See P84 of PPC440EPx for more information

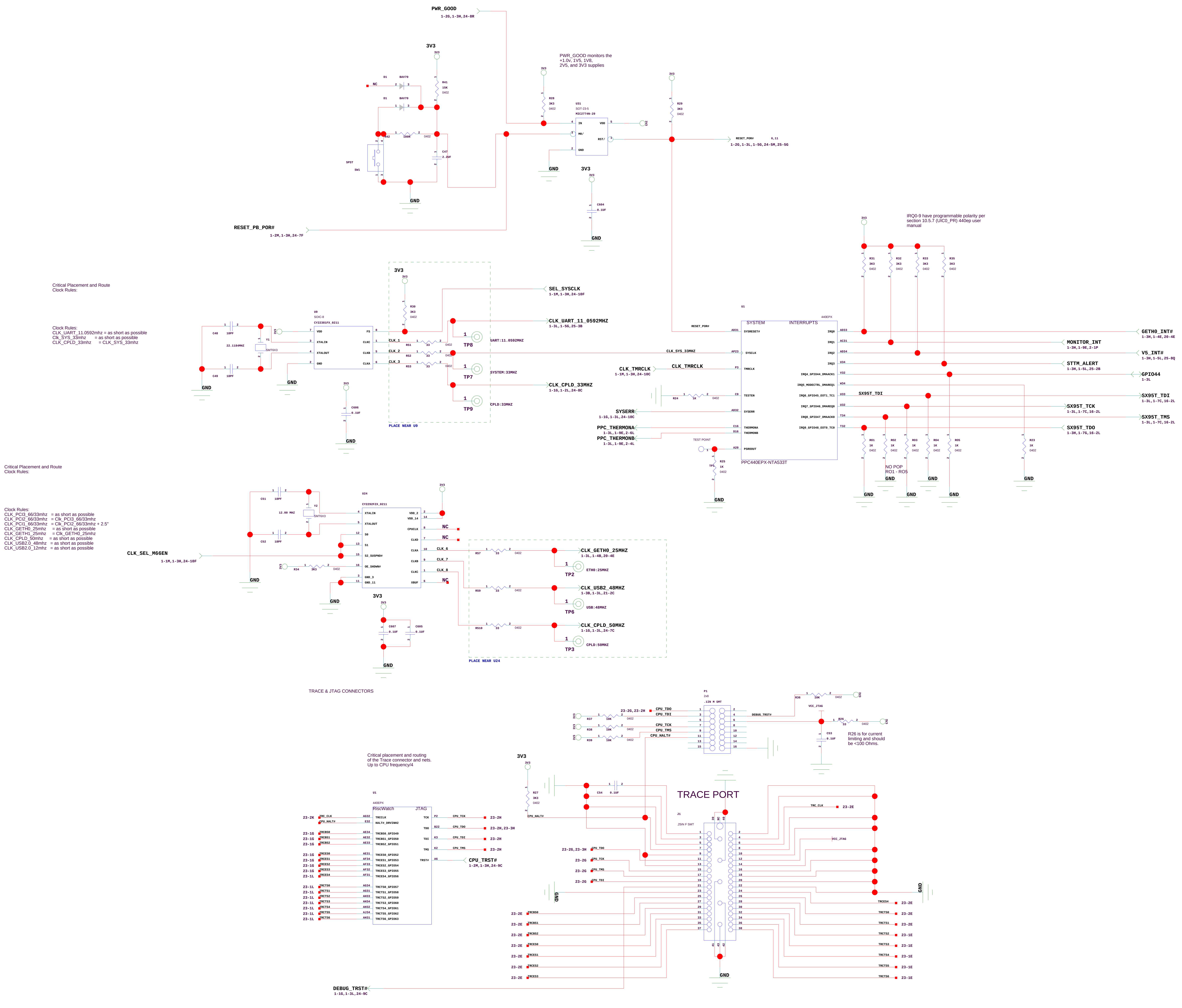
DDR_PCLKOUT NETS CAN BE SWAPPED ON CLOCK BUFFER FOR ROUTING

FBOUT NETS LENGTH MATCHED TO DDR_PCLKn NETS

ALL DQ, DQS, DM, ADDR, CMD AND CTRL LINES LENGTH MATCHED

U6 THERMAL TAB TO BE CONNECTED TO GND PLANE WITH THERMAL VIAS

ROACH/iBOB2	**ROACH_PPC_DDR2**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-19-2008_14:43 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 22 OF 25


PWR_GOOD
1-2G,1-3H,24-8R
3V3
RESET_PB_POR#
1-2M,1-3H,24-7F
RESET_POR#
1-2G,1-3L,1-5G,24-5M,25-5G
SW1
U31
MIC2774N-29
GND
SEL_SYSCLK
1-1M,1-3H,24-10F
CLK_UART_11_0592MHZ
1-3L,1-5G,25-3B
CLK_CPLD_33MHZ
1-1G,1-2L,24-8C
TP8
TP7
TP9
UART:11.0592MHZ
SYSTEM:33MHZ
CPLD:33MHZ
PLACE NEAR U9
U9
CY2305IFX_0211
Y1
22.1184MHZ
CLK_TMRCLK
1-1M,1-3H,24-10C
SYSERR
1-1G,1-3L,24-10C
PPC_THERMONA
1-3L,1-9E,2-6L
PPC_THERMONB
1-3L,1-9E,2-4L
CLK_SYS_33MHZ
SYSTEM
INTERRUPTS
440EPX
PPC440EPX-NTA533T
TEST POINT
GETH0_INT#
1-3H,1-4E,28-4E
MONITOR_INT
1-3H,1-9E,2-1P
V5_INT#
1-3H,1-5L,25-8Q
STTM_ALERT
1-3H,1-5L,25-2B
GPIO44
1-3L
SX95T_TDI
1-3L,1-7C,16-2L
SX95T_TCK
1-3L,1-7C,16-2L
SX95T_TMS
1-3L,1-7C,16-2L
SX95T_TDO
1-3H,1-7G,16-2L
CLK_SEL_M66EN
1-1M,1-3H,24-10F
U24
CY2305IFX_0211
12.00 MHZ
NC
CLK_GETH0_25MHZ
1-3L,1-4B,28-4E
CLK_USB2_48MHZ
1-3B,1-3L,21-2C
CLK_CPLD_50MHZ
1-1G,1-3L,24-7C
TP2
TP6
TP3
ETH0:25MHZ
USB:48MHZ
CPLD:50MHZ
PLACE NEAR U24
P1
2x8
CPU_TDO
CPU_TDI
CPU_TCK
CPU_TMS
CPU_HALTV
DEBUG_TRST#
VCC_JTAG
U1
440EPX
RiscWatch
JTAG
CPU_TRST#
1-2M,1-3H,24-9C
DEBUG_TRST#
1-1G,1-3L,24-9C
J2
TRC_CLK
23-2E
23-1E

PWR_GOOD monitors the +1.0v, 1V5, 1V8, 2V5, and 3V3 supplies

IRQ0-9 have programmable polarity per section 10.5.7 (UIC0_PR) 440ep user manual

NO POP
R01 - R05

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_SYS_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible

TRACE & JTAG CONNECTORS

R26 is for current limiting and should be <100 Ohms.

Critical placement and routing of the Trace connector and nets. Up to CPU frequency/4

TRACE PORT

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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PATH PATH

ROACH_PPC_TST_CLK_IO

DOC NO
NRF-ADM-XXX-SD-0001

REVISION
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DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

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roach_cpld_XC2C256_7VQ100C_pcb
U54
XC2C256_7VQ144C
SD/MMC/MMCPLUS CONNECTOR
J17
CMD/DI
CLK/SCLK
VDD
VSS1
VSS2
SD_CD_COM
SD_WP_COM
DAT0/DO
DAT1
DAT2
DAT3
DAT4
DAT5
DAT6
DAT7
MNT1
MNT2
SDSR13-A0-0005
BOOT_CFG0
BOOT_CFG1
BOOT_CFG2
PADD[27:31]
PDATA[0:7]
SYS_CONFIG[0:7]
CLK_CPLD_33MHZ
POE#
SX95T_RDWR_B_0
CLK_CPLD_50MHZ
SX95T_D_IN_0
SX95T_D_OUT_BUSY_0
FRY_BY#
FWP#
EE1_WP
EE2_BOOT_WP
STTM_AS
SELECTMAP_CS
SX95T_CS_B_0
PPC_RESET
RESET_CPLD#
PER_CCLK_EN#
SX95T_CCLK_0
GETH0_RST#
PPC_DDR2_RESET_N
CLK_SEL_M66EN
SEL_SYSCLK
SX95T_INIT_B_0
SX95T_M0_0
SX95T_M1_0
SX95T_M2_0
RESET_PB_POR#
USER_LED0
USER_LED1
SYSERR#
RESET_BUFPOR#
USER_DIP0
USER_DIP1
USER_DIP2
USER_DIP3
CFG_DIP0
CFG_DIP1
CFG_DIP2
M66EN
SW2
4POLE
User DIP-Swith
SW3
4POLE
Configuration DIP-Swith
R194
R195
R196
R198
R204
R205
R206
10K
0402
RED
CR5
3V3
1V8
SN74AHC1G125DCKT
OE#
VCC
A
Y
GND
U2
C13
100NF
10V
R305
R306
R135
roach_cpld_XC2C256_7VQ100C_powerpins
roach_cpld_XC2C256_7VQ100C_configpins
TDI
TMS
TCK
TDO
PAD218
RESET_POR#
PWR_GOOD
TALVC1G08
J22
VREF
R193
R192
C484
2U2
C473
C474
C475
C476
C477
C478
C479
C480
C481
C482
C483

RESETS

CPU_TRST# = '1' when
JTAG_TRST# = '1' and
RESET_POR# = '1' else '0';
see errata sheet

SysErr will be used to
drive Status LED (active H)

Boot Configuration

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

ENABLE PER_CLK CONNECTION
TO CONFIGURATION I/F
MUST CO-ORDINATE WITH
SX95T_CCLK_0 AND MODE
TO AVOID CLASH

PLACE AT END OF DAISY CHAIN

Xilinx
Programing Cable

JTAG

PLACE NEAR CPLD JTAG CONNECTOR

PLACE NEAR CPLD POWER PINS

ROACH/iBOB2

ROACH_PPC_CPLD

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

DOC NO	REVISION
NRF-ADM-XXX-SD-0001	A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

6-19-2008_14:43

PATH PATH

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 24 OF 25

PDATA[0:31]
PADD[2:31]
PADD30 IS THE LSB FOR 16 BIT WIDE BUS TRANSFERS
NOTE: DMA SIGNALS IN GREEN TEXT
PADD2 IS THE MSB
External Slave Peripheral
External Master Peripheral Interface
EPB RESET OUTPUT
EXT_RESET#
CLK_PERCLK
ROUTE AS DAISY CHAIN - U1 - U15 - U2 - U54 - TERMINATION
KEEP STUBS AS SHORT AS POSSIBLE
RESET_POR#
FLASH 32Mx16
I2C0_SCLK
I2C0_SDATA
EE2_BOOT_WP
EE1_WP
AT24C04N-10SU-1.8
CLK_UART_11_0592MHZ
STTM_ALERT
STTM_LOAD
UART
IIC0
IIC1_SPI
NAND Flash Interface
NOT USED
UART Port 0
UART Port 1
J14
HLE-105-02-G-DV
BOOT_CFG2
BOOT_CFG1
BOOT_CFG0
RESET_CPLD#
U15
BANKS=1, 2, 4
CHIP SELECT 1
PER_CLK
PER_INT
PER_READY
3V3
GND

CHIP SELECTS CONFIG

CS0	NOR FLASH - U42
CS1	FPGA - U15
CS2	CPLD - U54
CS3	FPGA - U15
CS4	SELECTMAP_CS
CS5	GPIO - SX95_D_IN

ROACH/iBOB2

ROACH_PPC_NVM_SERIAL

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