

KAROO ARRAY TELESCOPE, NRF

UNIT 12, LONSDALE BUILDING
LONSDALE WAY, PINELANDS, 7405
SOUTH AFRICA

TITLE

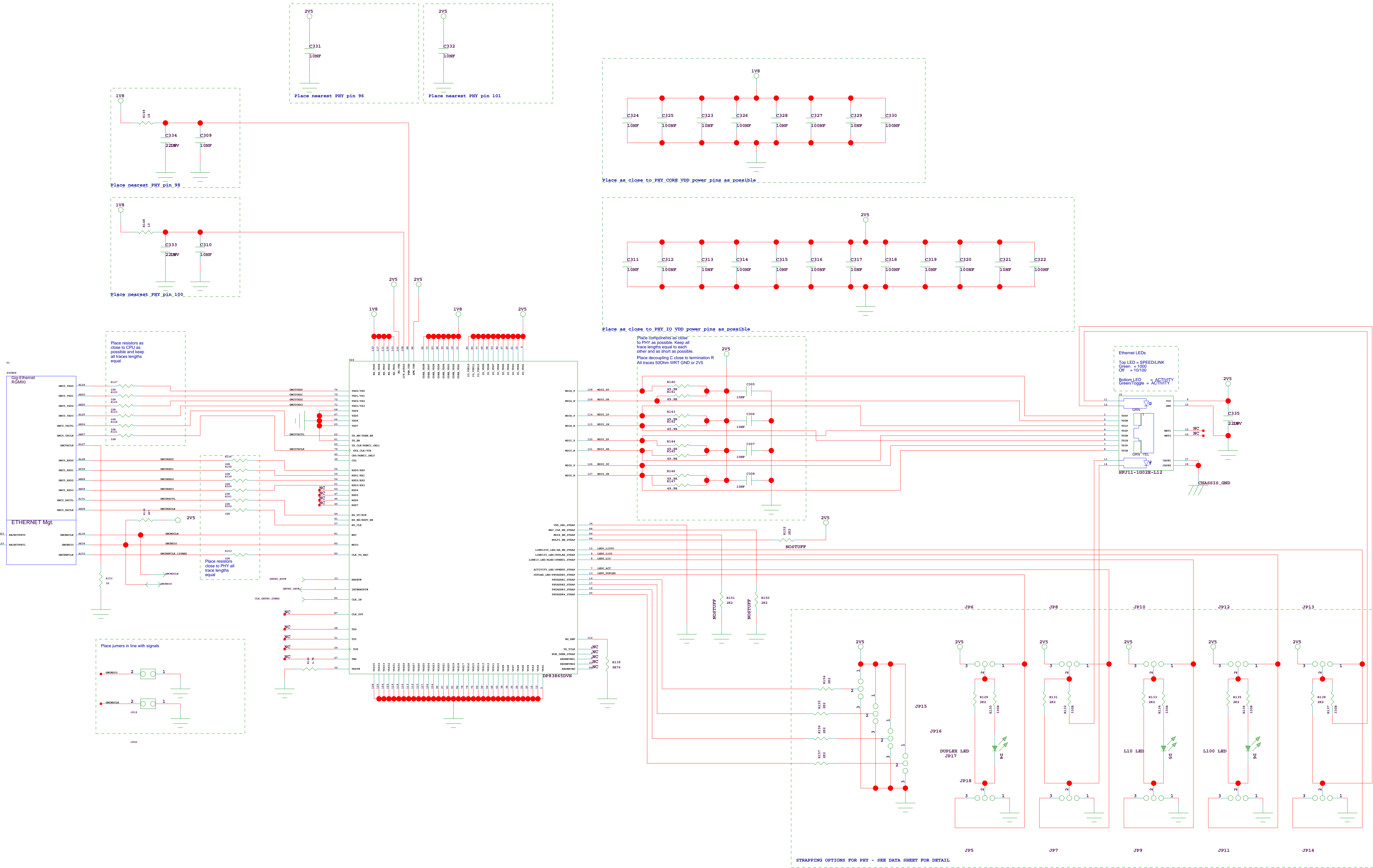
ROACH_TOP

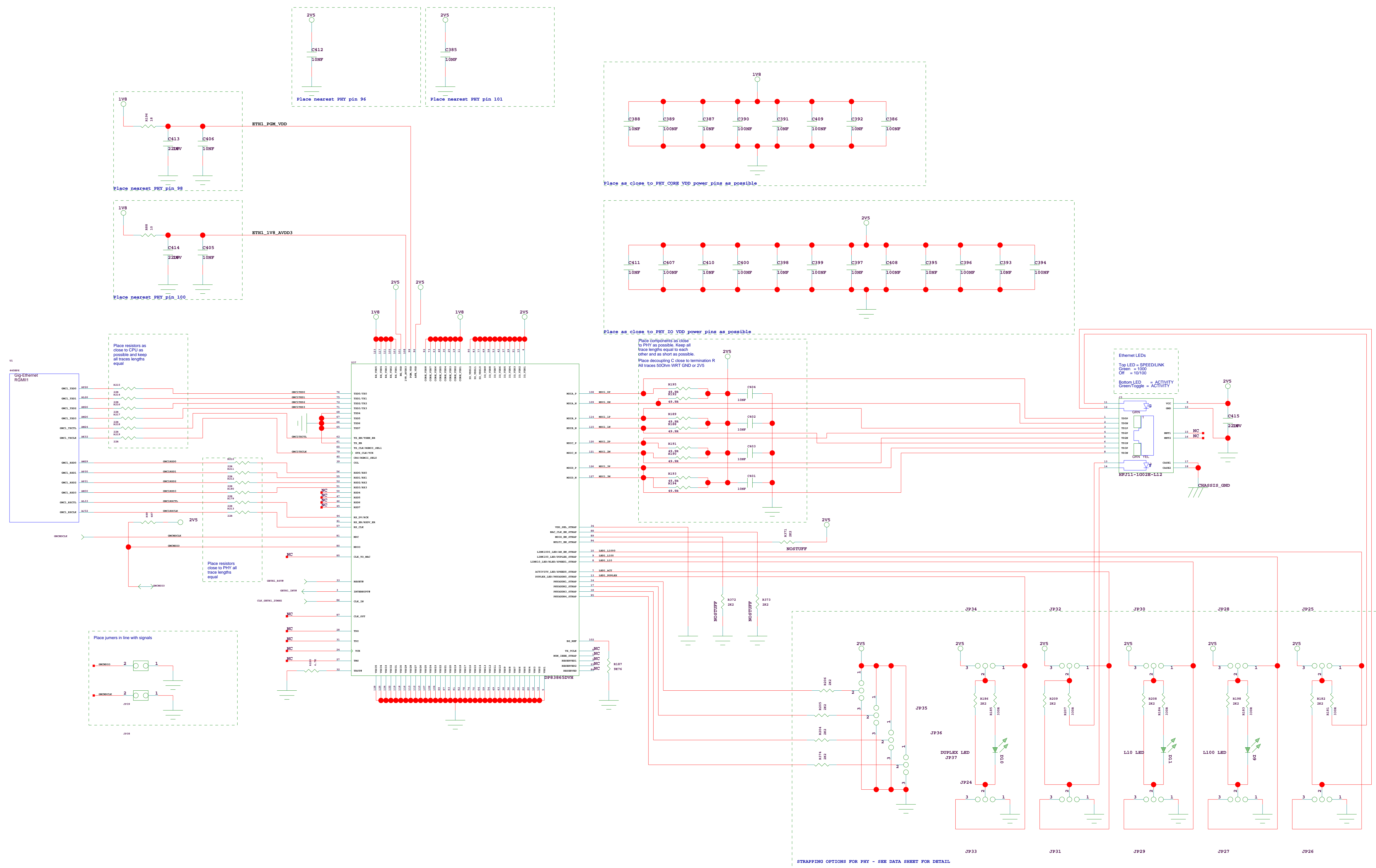
SIZE	DWG NO	REV
A2	NRF-ADM-XXX-SD-0001	A
CHECKED BY	<PUT NAME HERE>	
DRAWN BY	FRANCOIS KAPP	
SCALE	SHEET	of
NTS	1	1

9-12-2007_15:53

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.
The Tx and the Rx side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.
Minimize the number of vias on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30





F

E

D

C

B

A

F

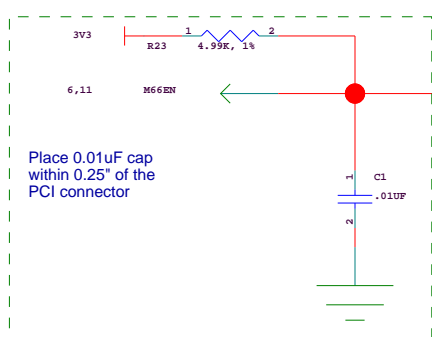
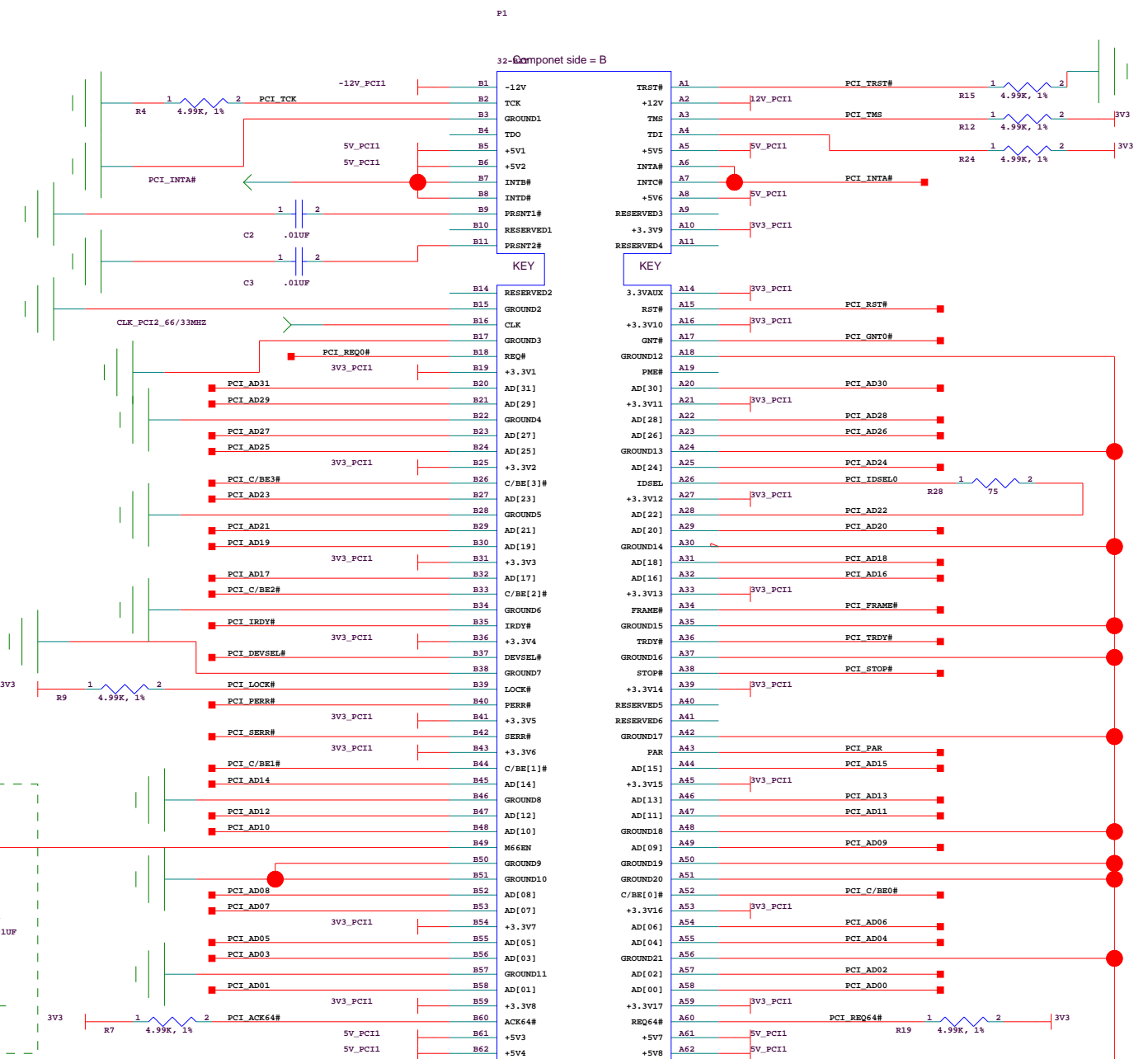
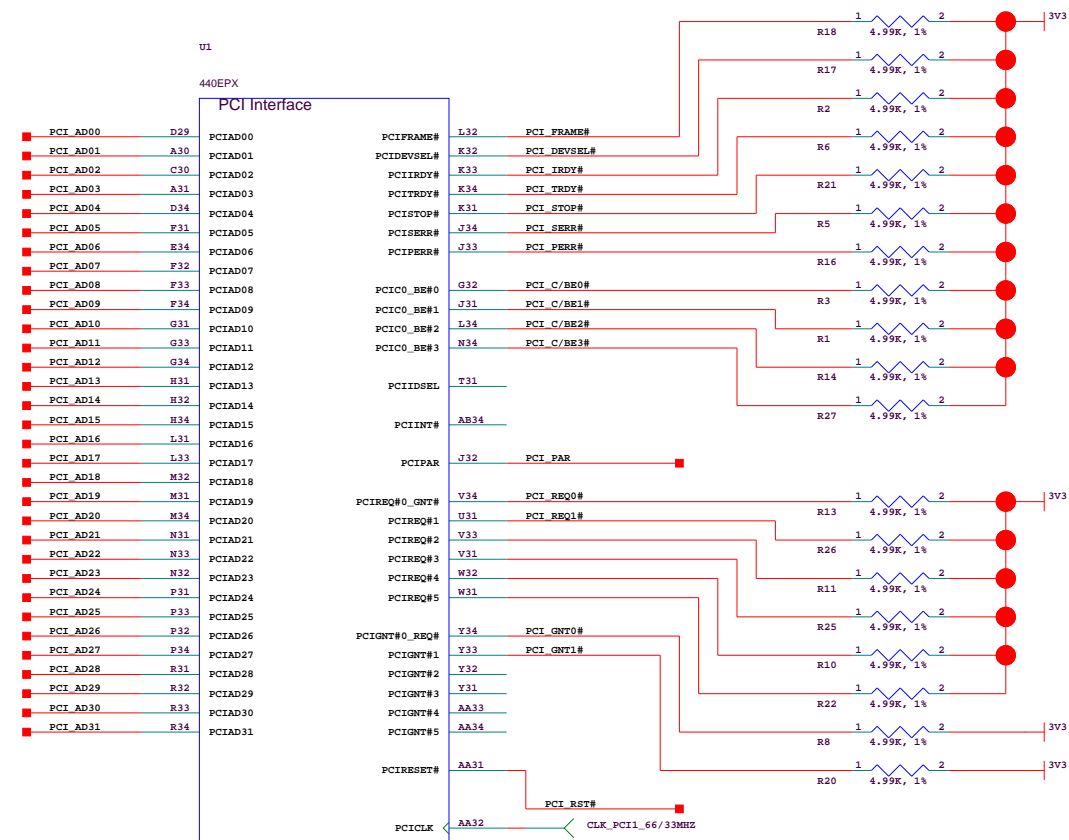
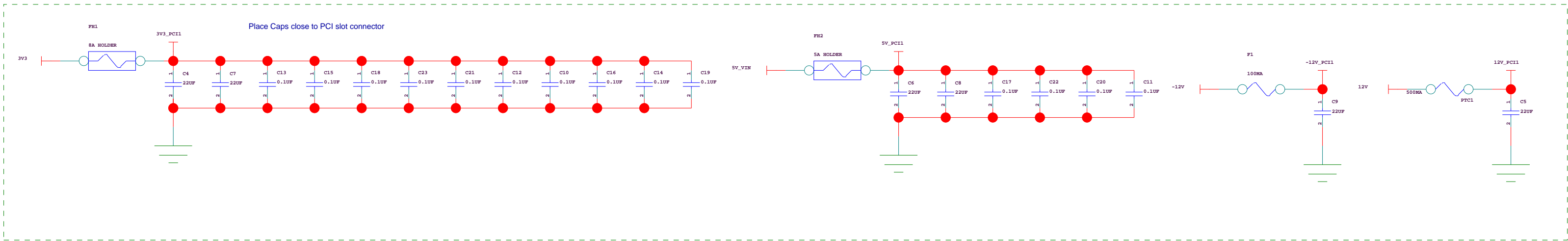
E

D

C

B


A



PCI SLOT_0

Include silkscreen text:
"SUPPORTS 3V3 IO ONLY"

Optional PRSNT signals are not used, max 25W is available		
PRSNT1#	PRSNT2#	Expansion Configuration
Open	Open	No expansion board present
Ground	Open	Expansion board present, 25 W maximum
Open	Ground	Expansion board present, 15 W maximum
Ground	Ground	Expansion board present, 7.5 W maximum



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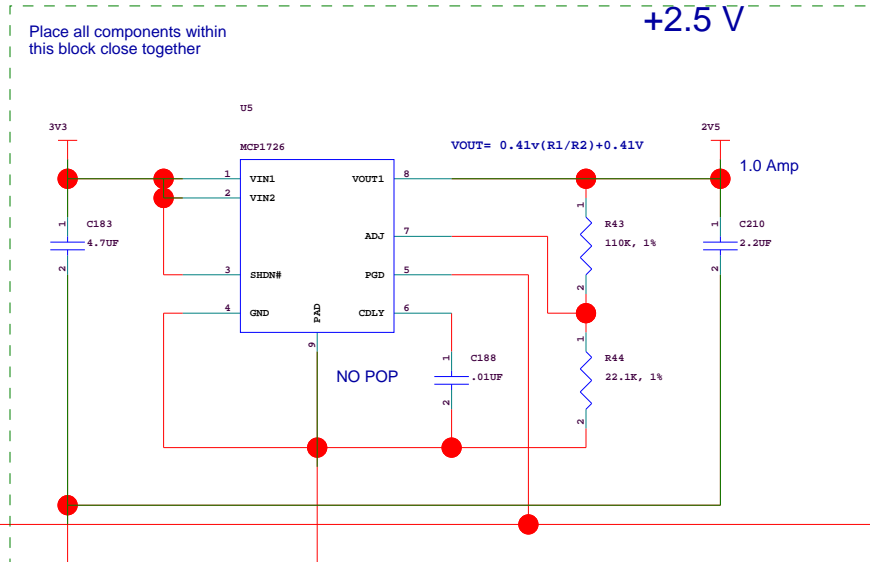
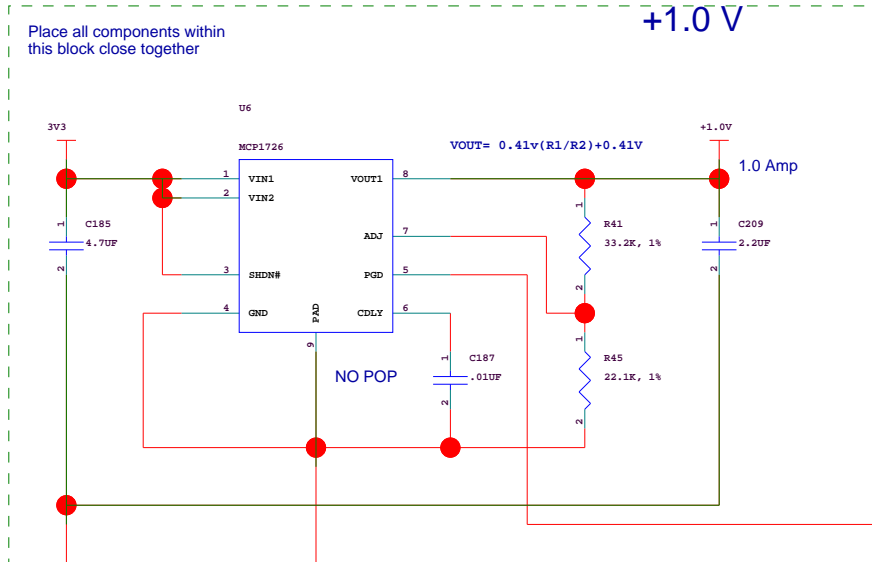
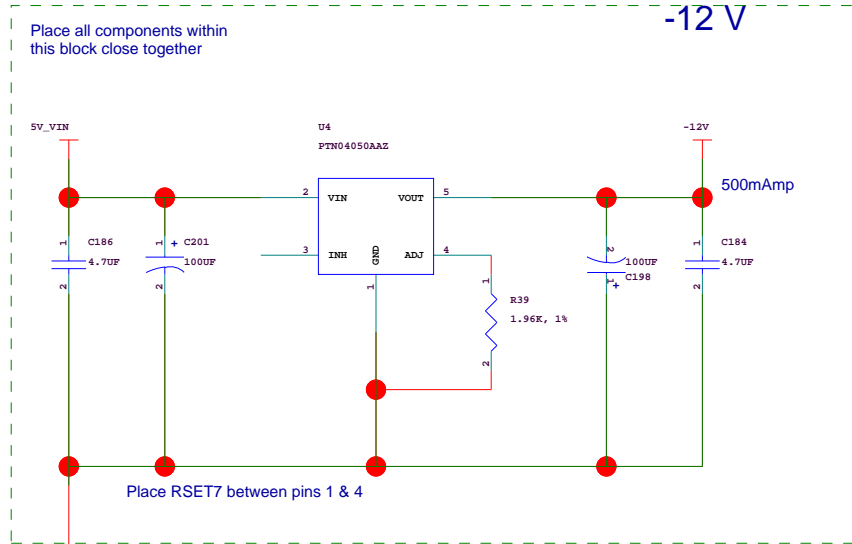
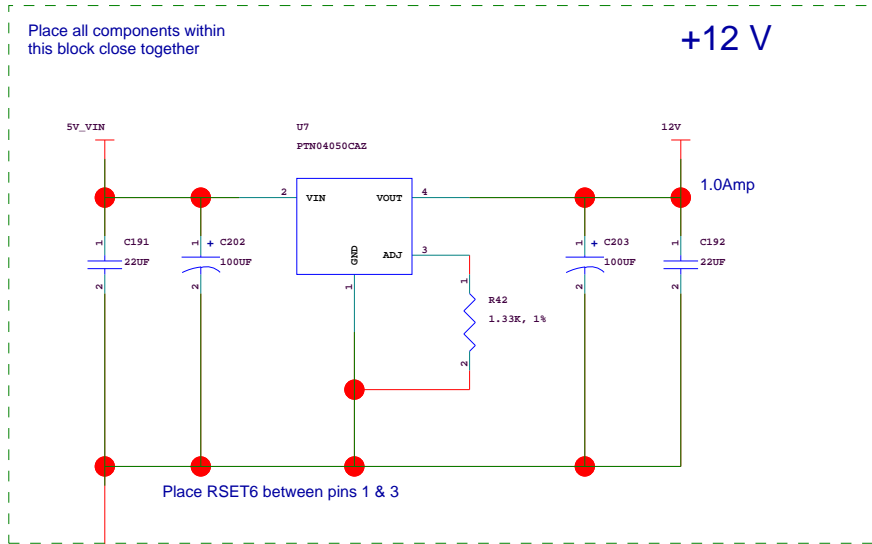
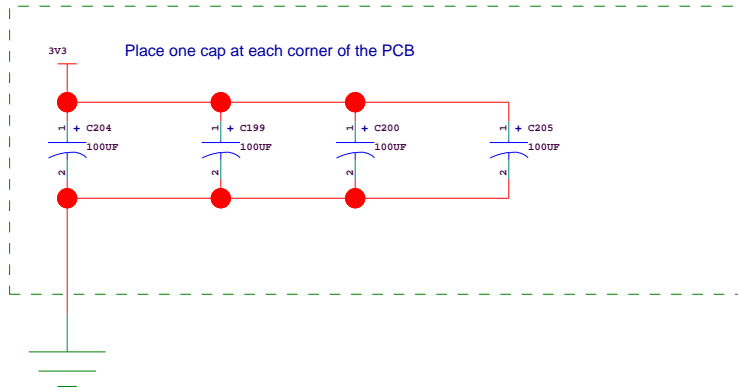
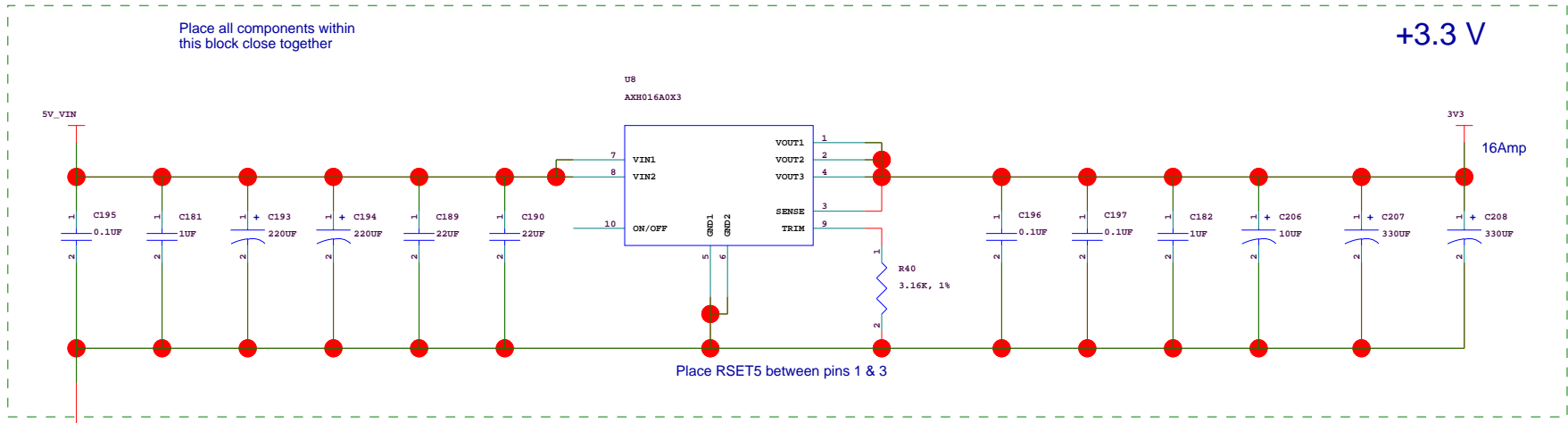
ROACH_PPC_PCI

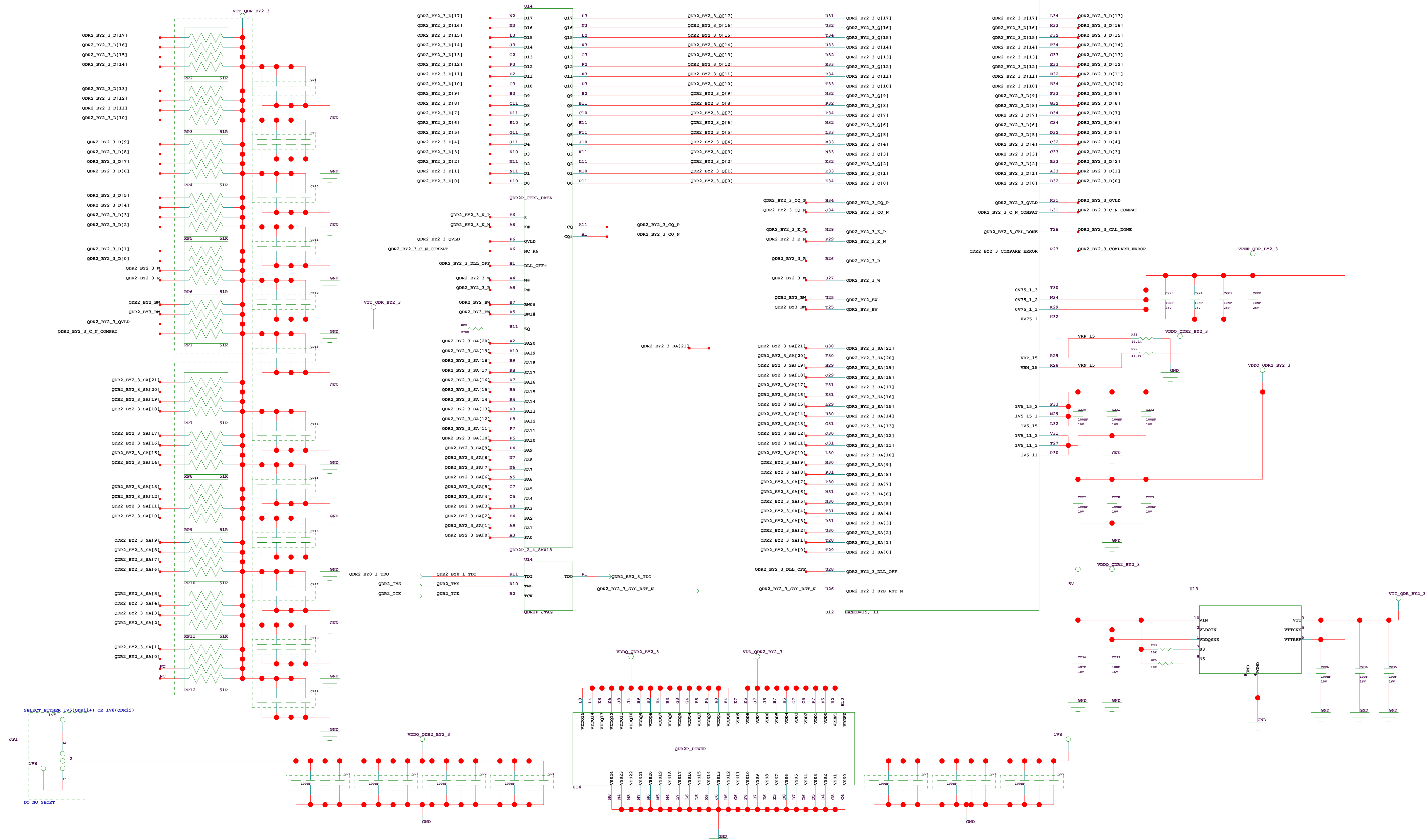
SIZE A2
SCALE NTS

DWG NO
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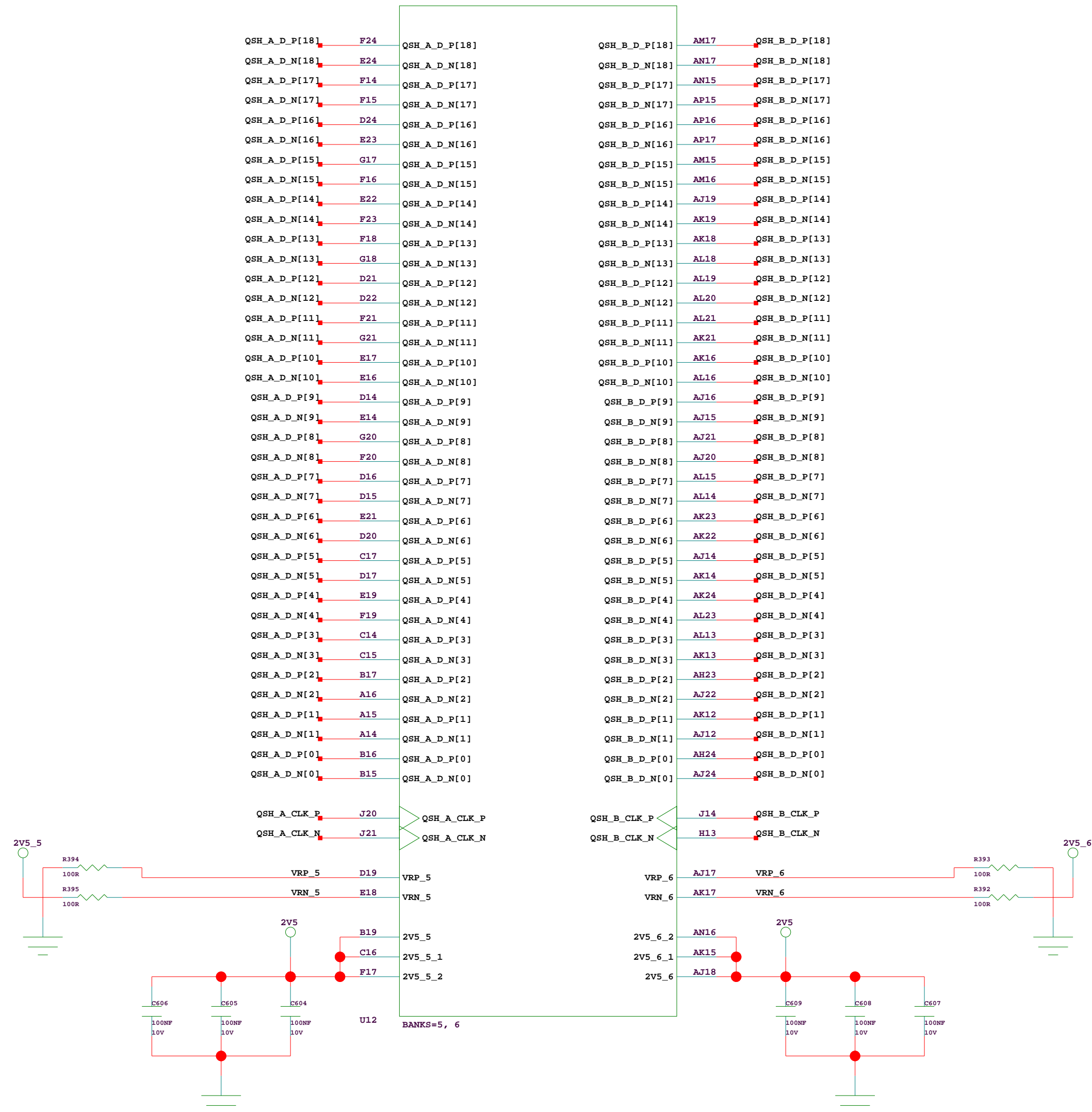
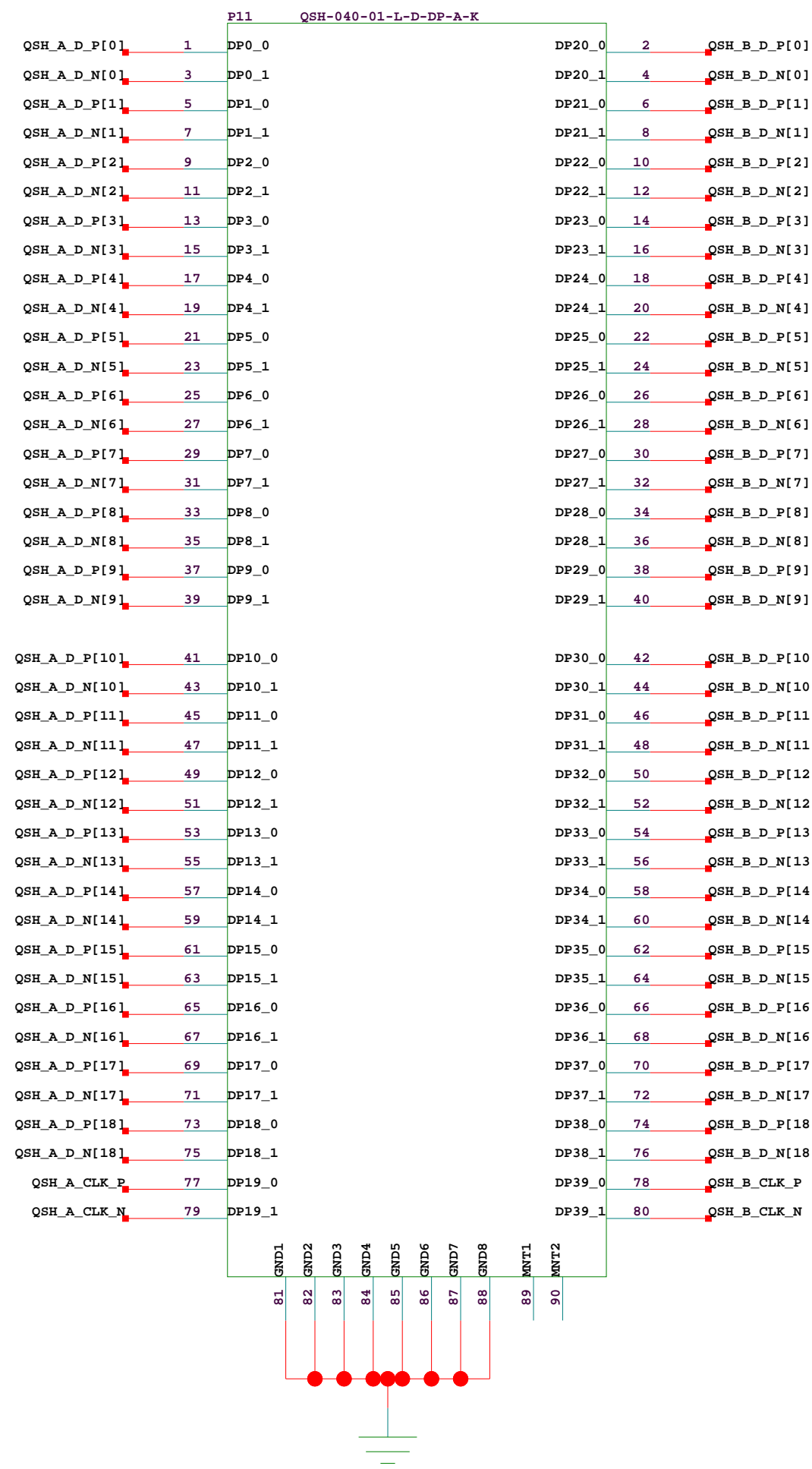
REV
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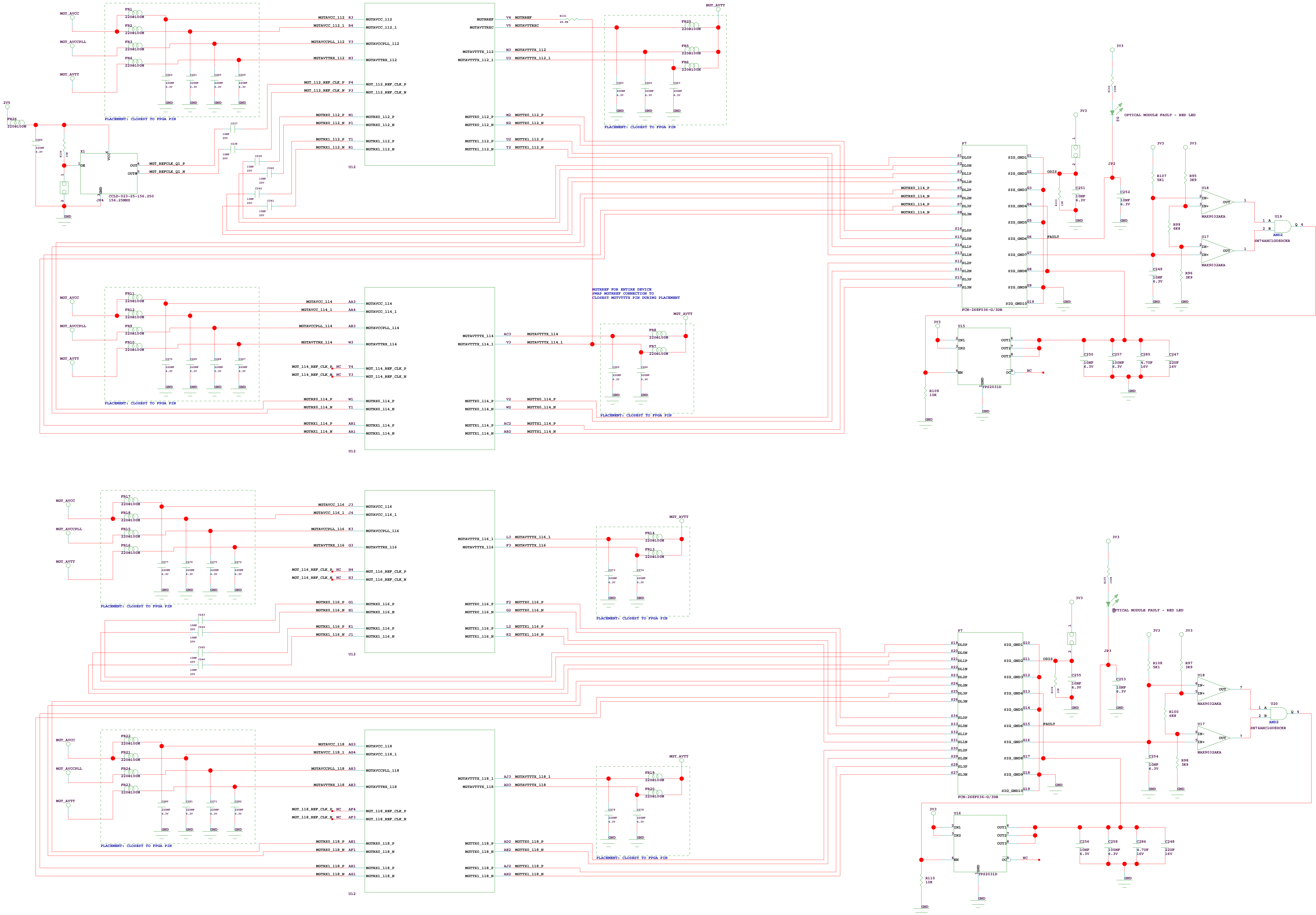
9-11-2007_15:45

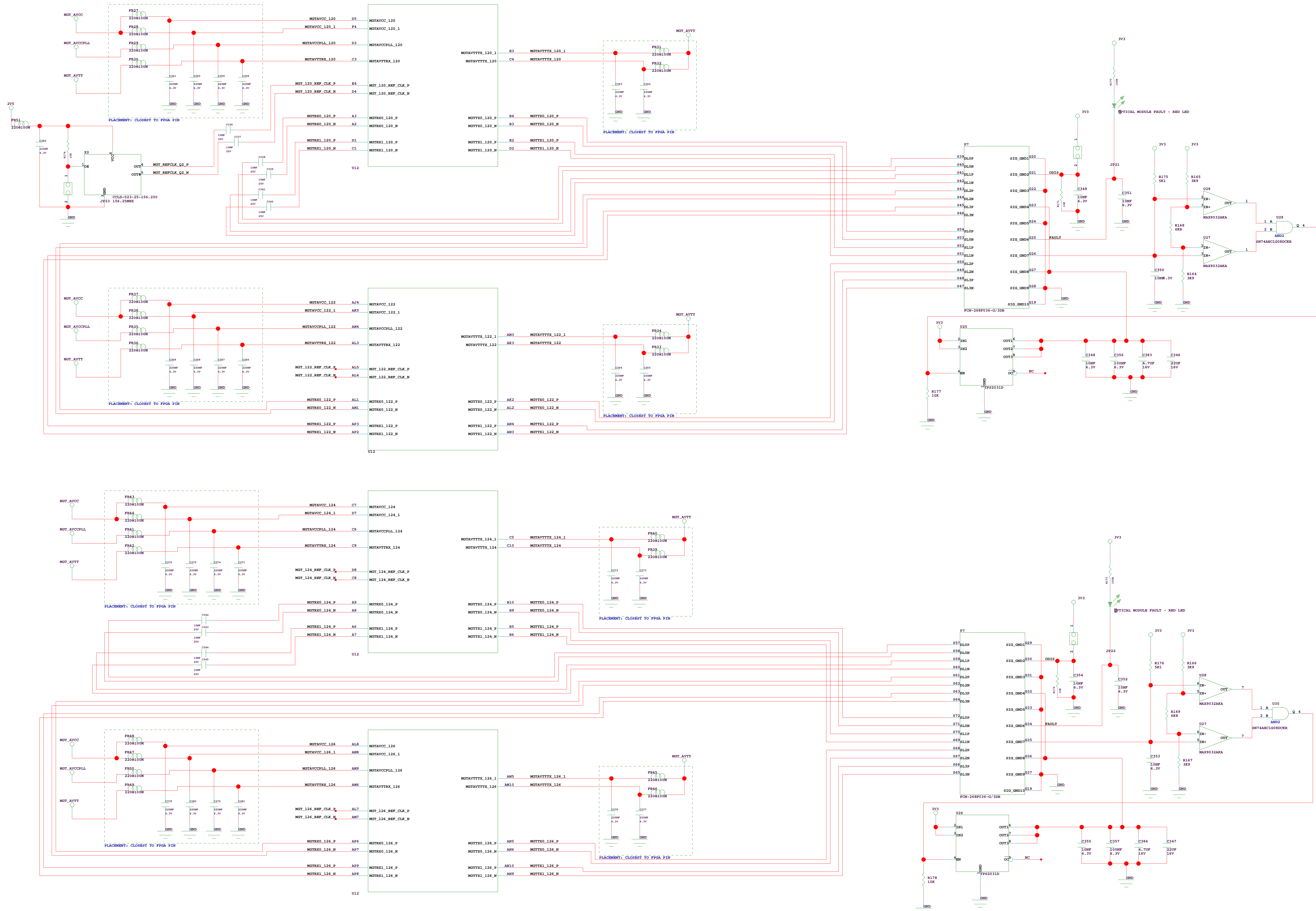


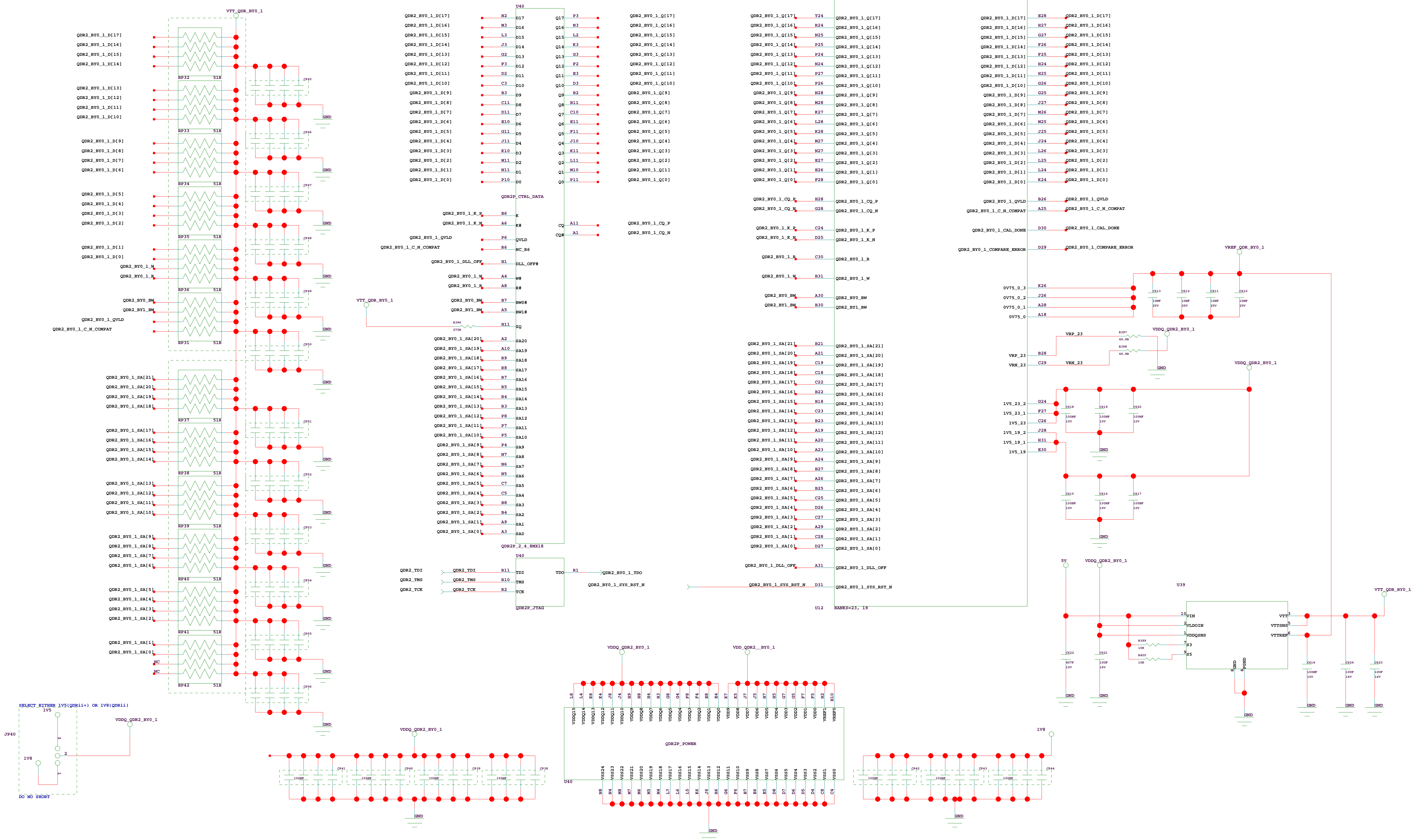


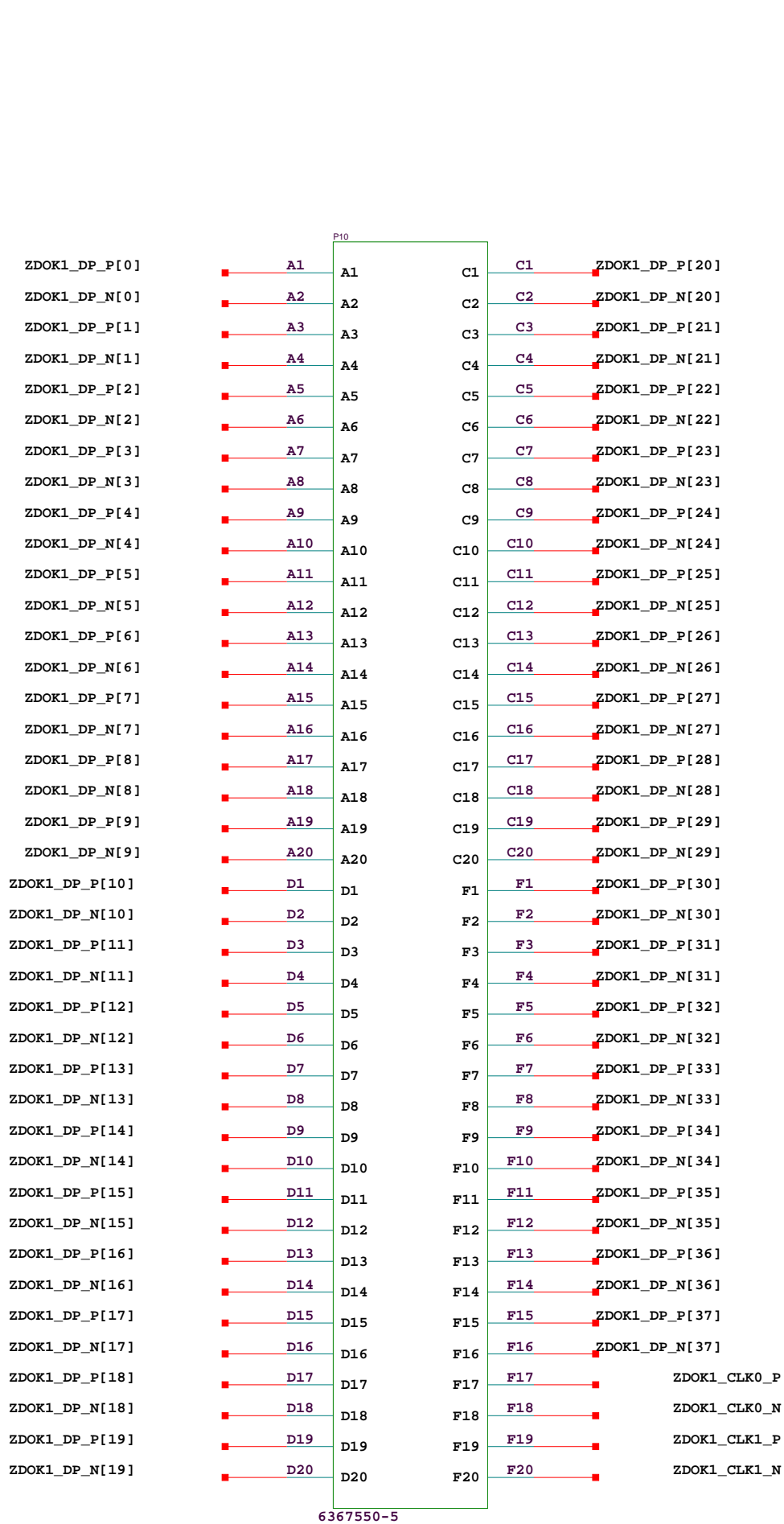
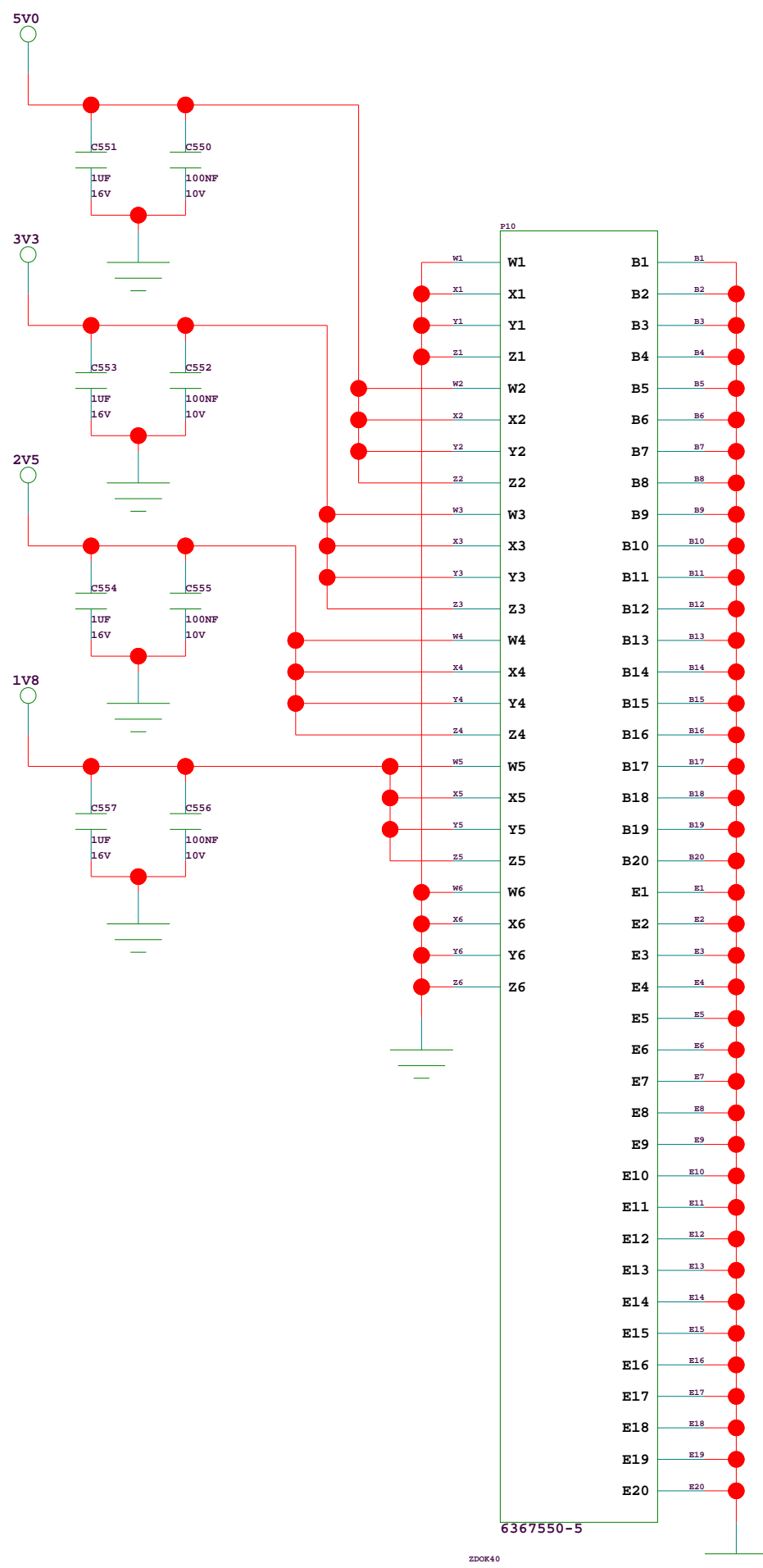
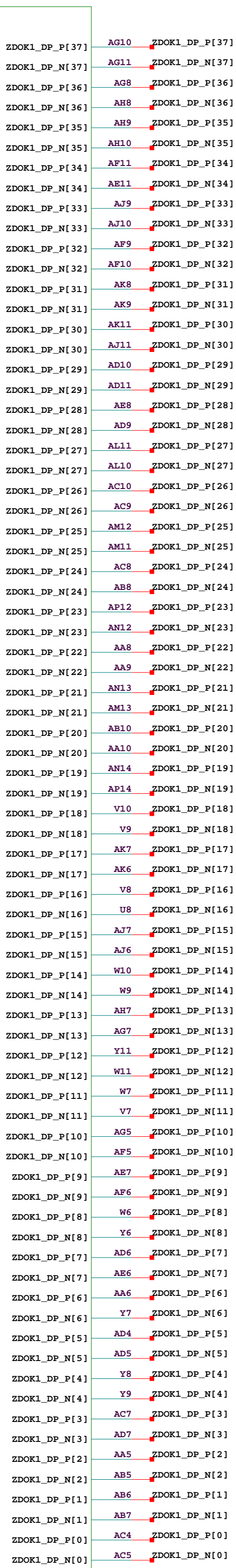
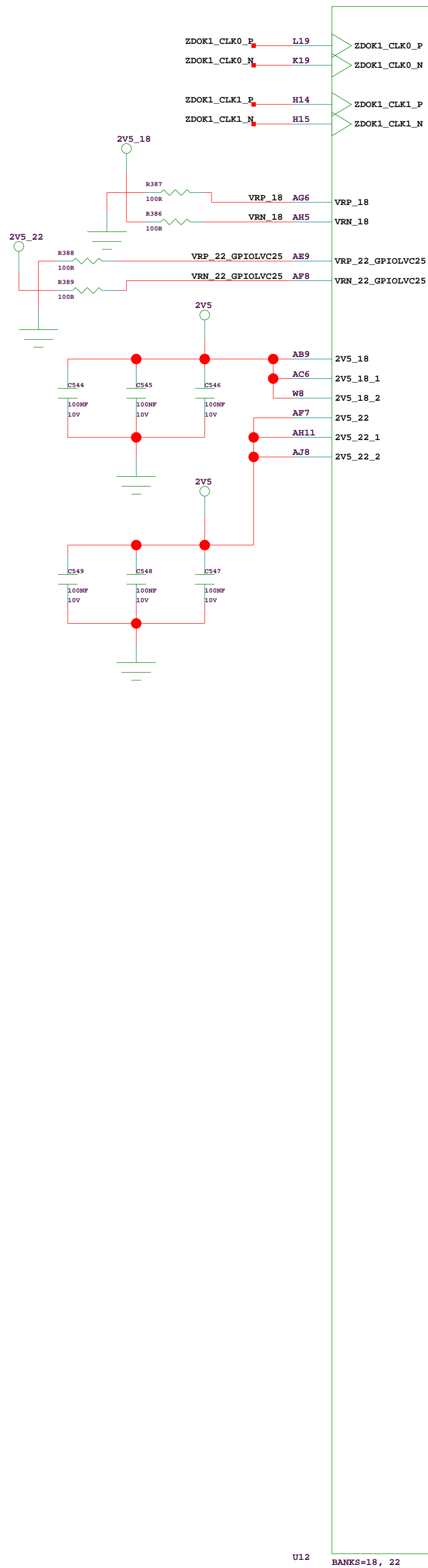


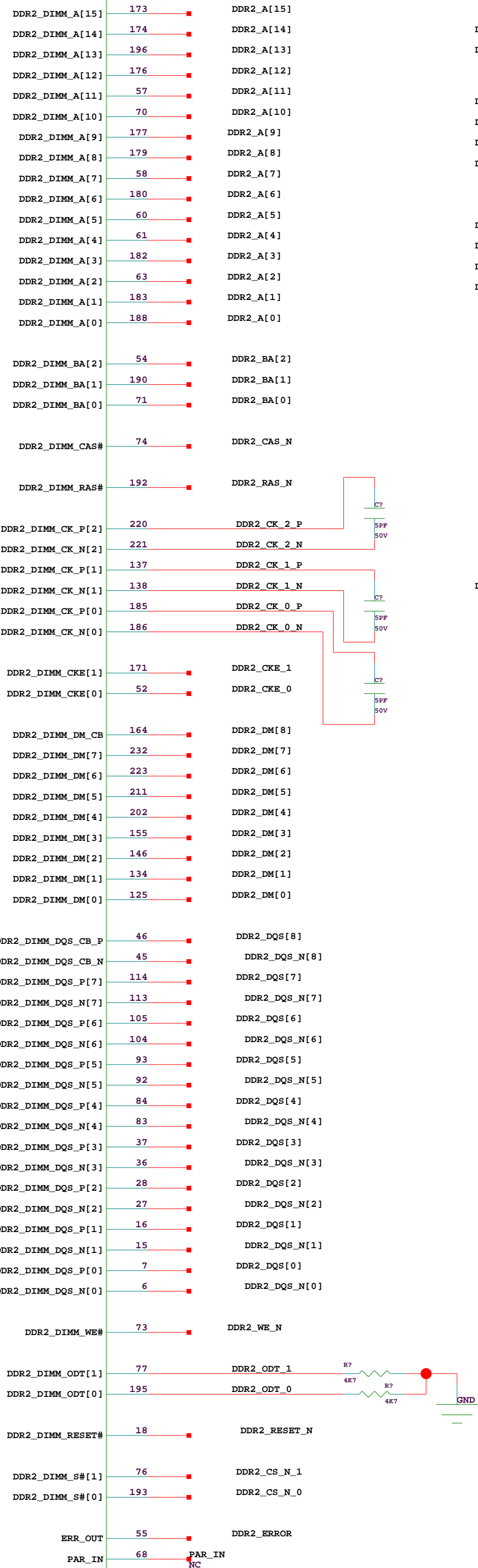
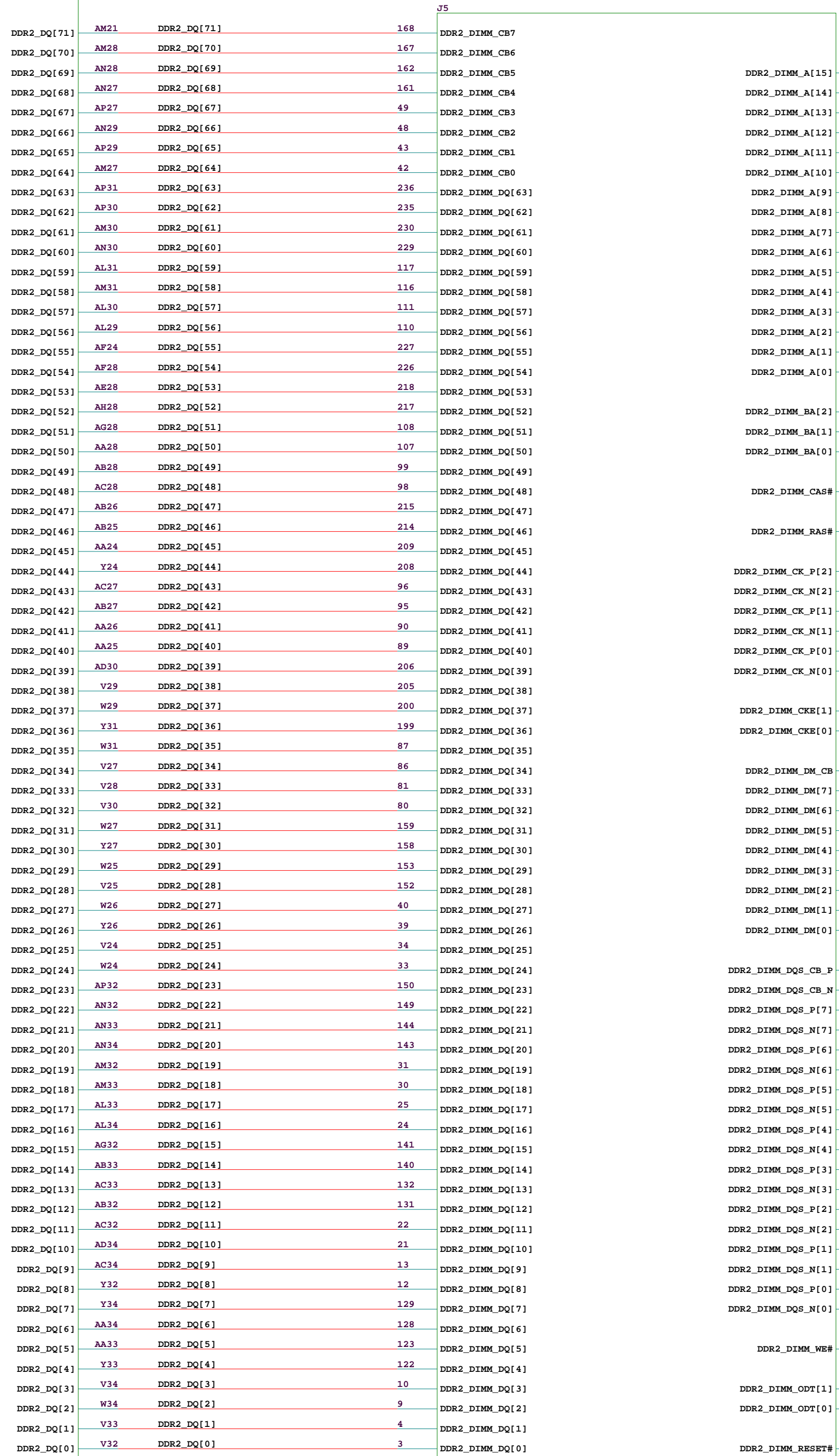
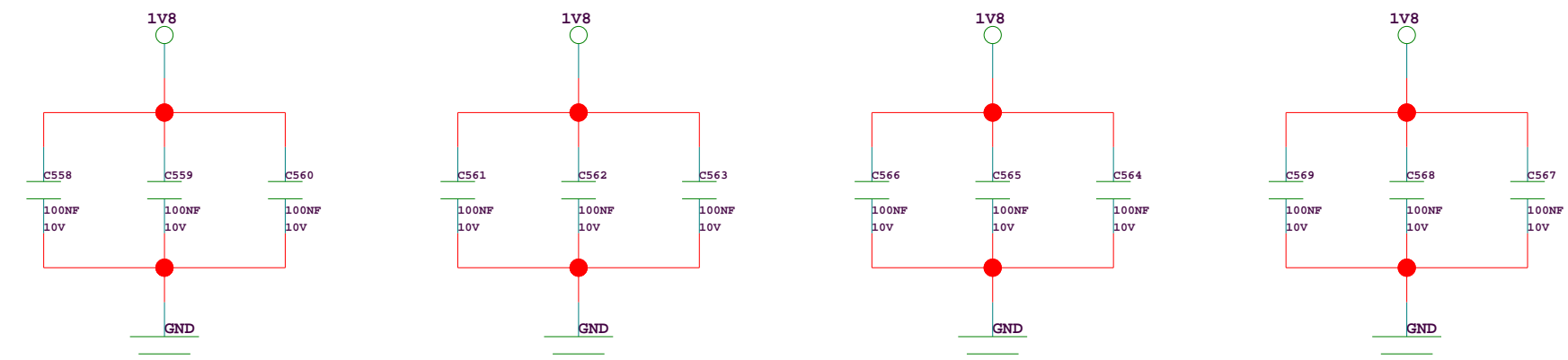




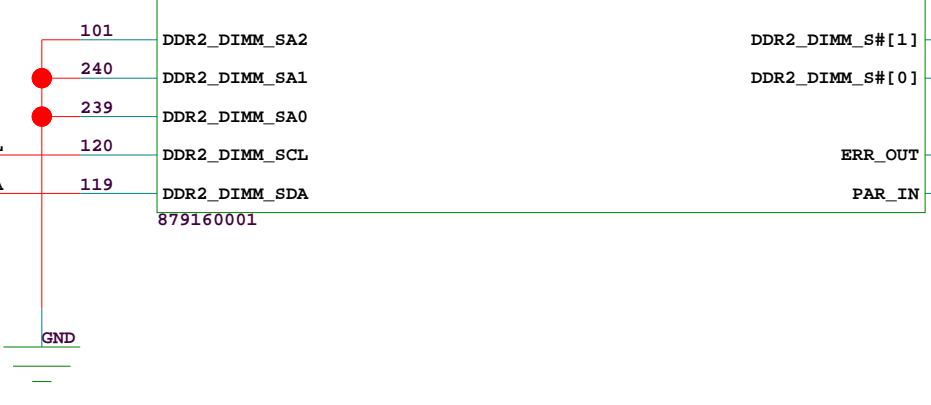
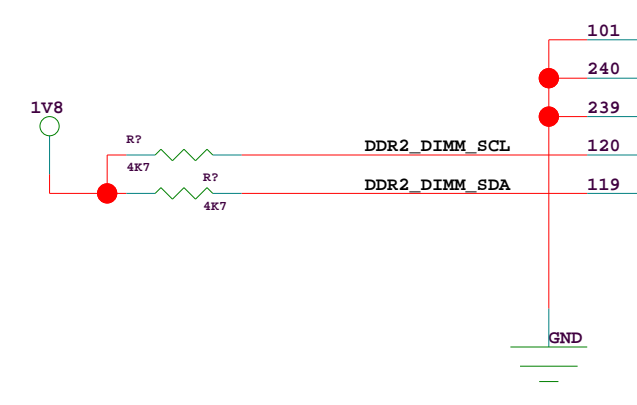
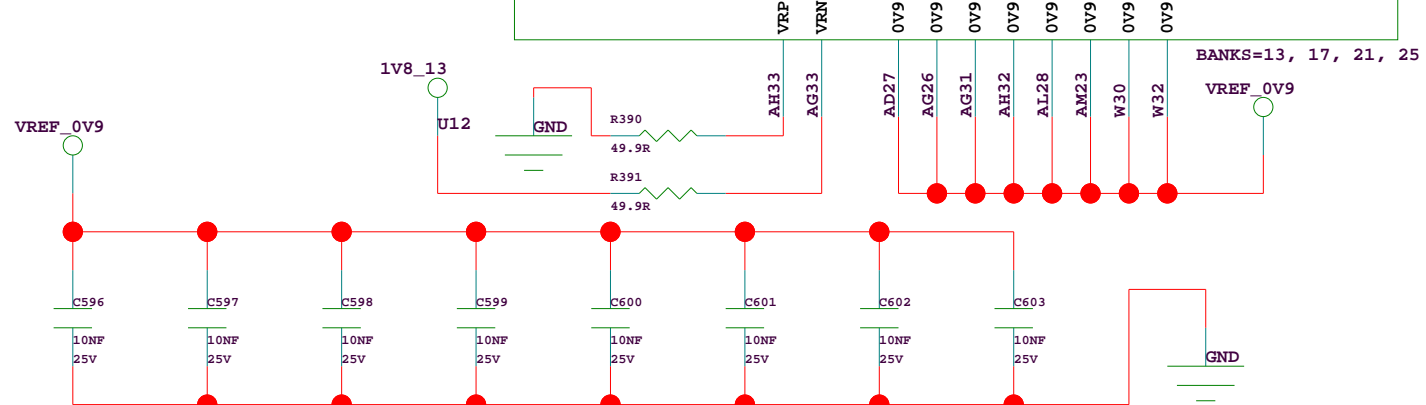
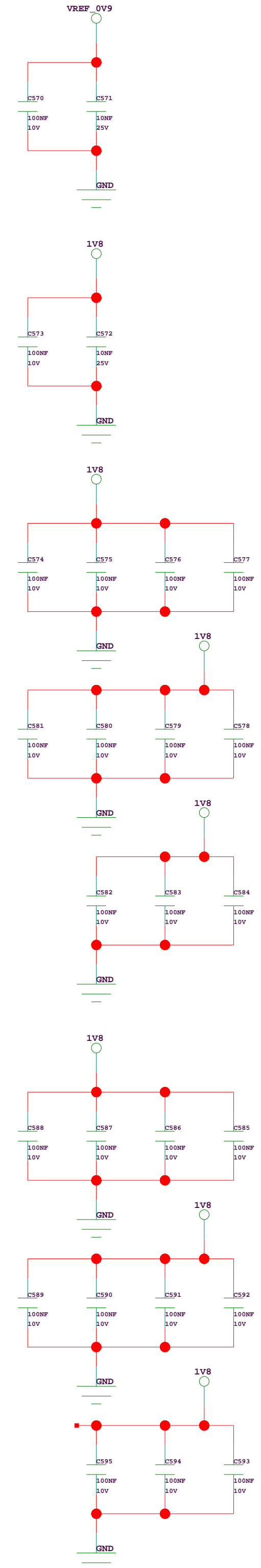
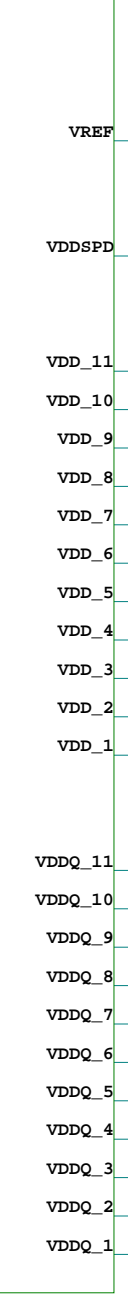
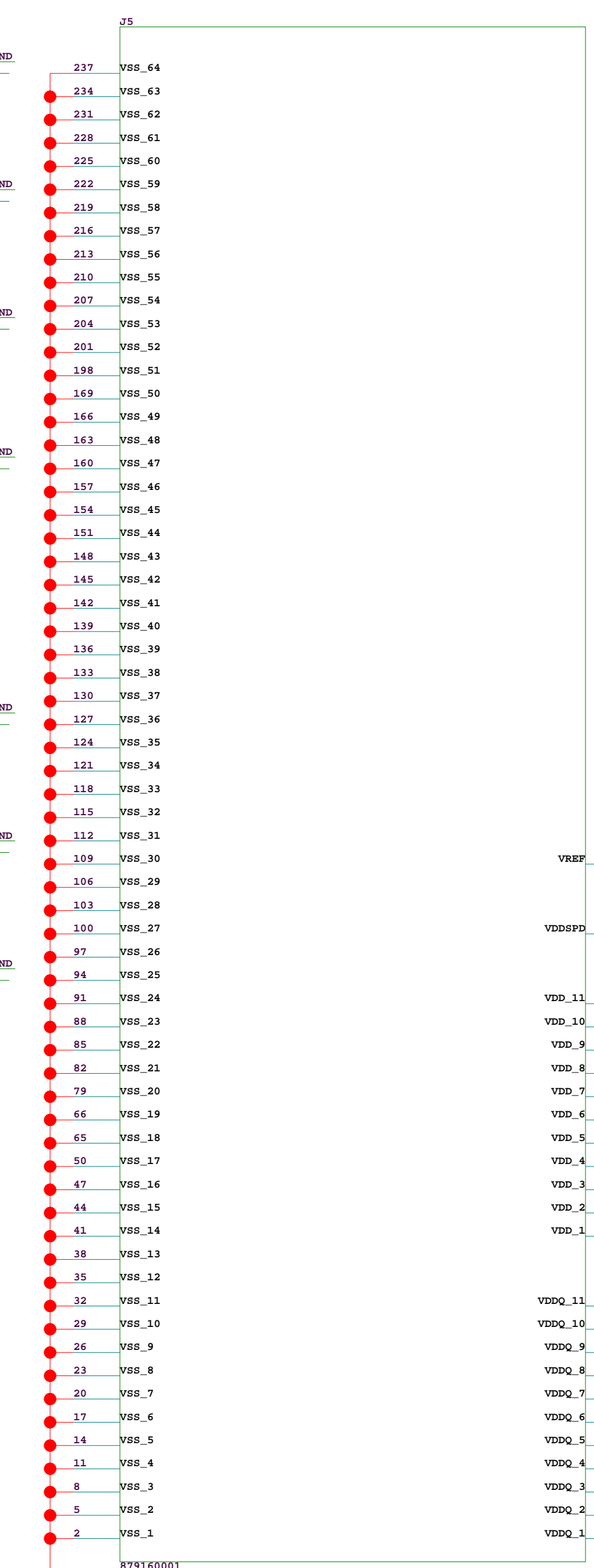
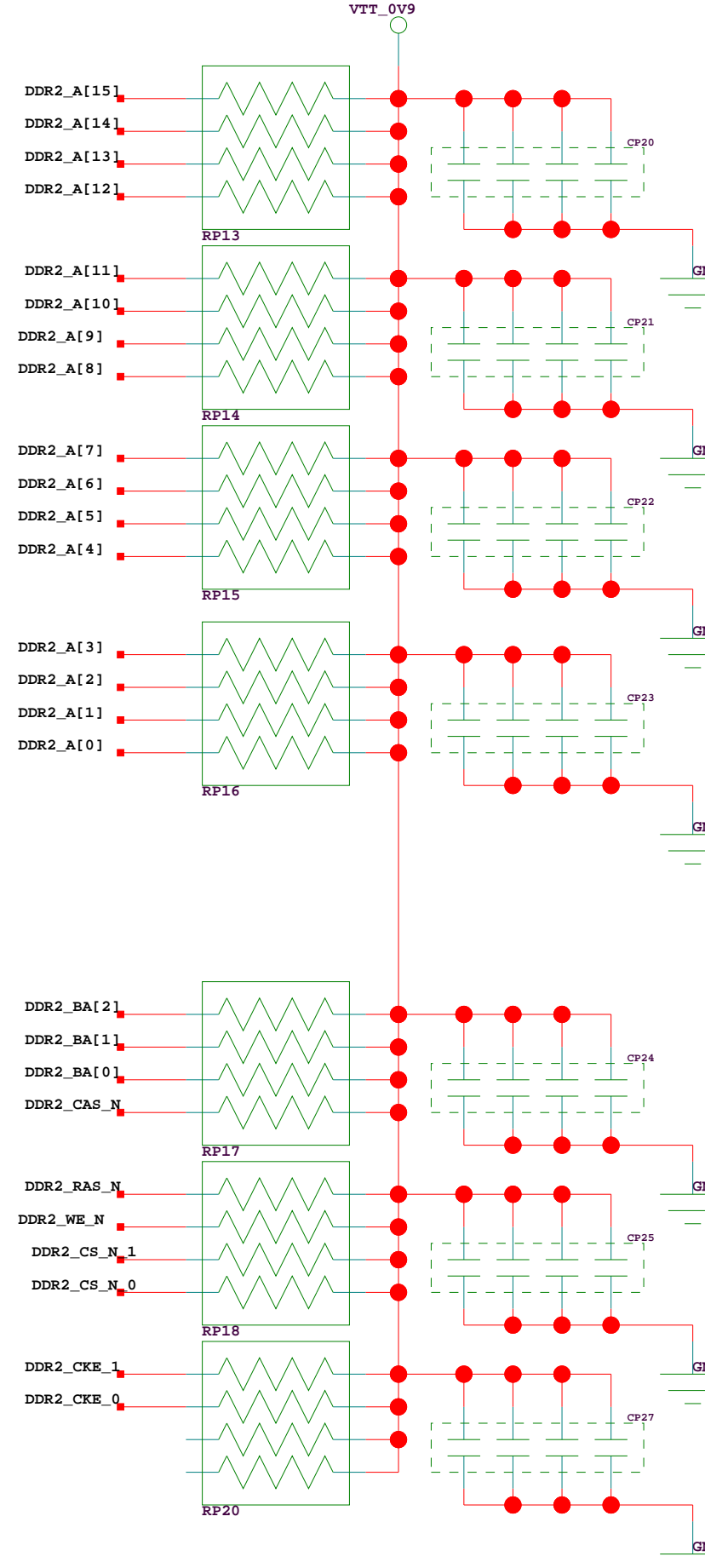


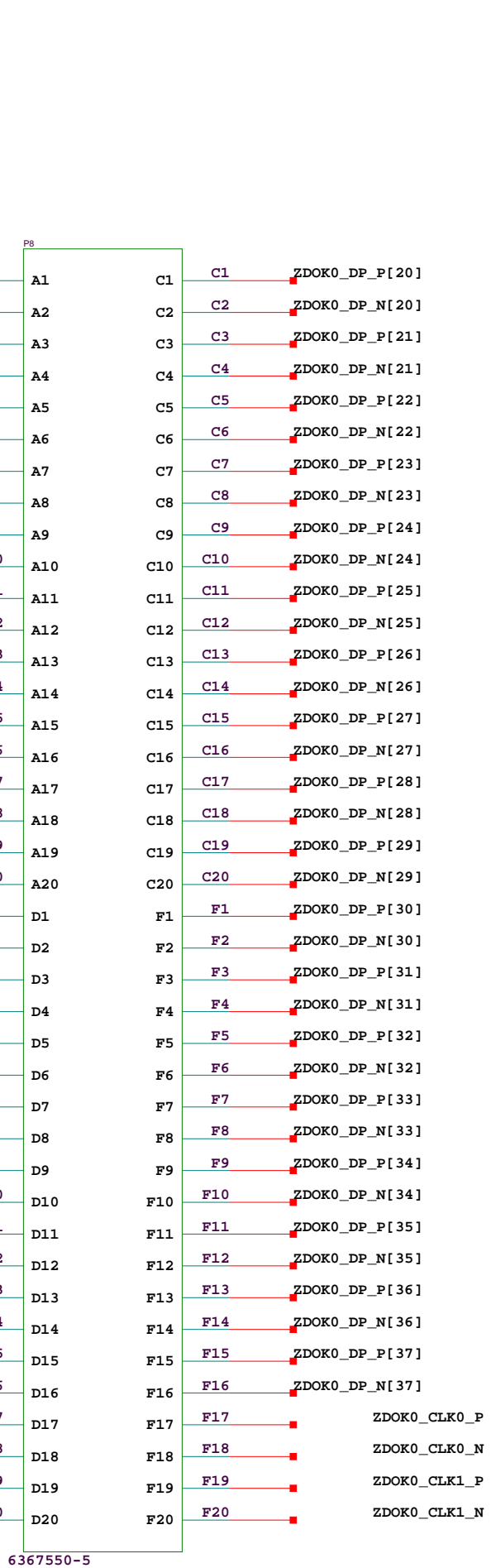
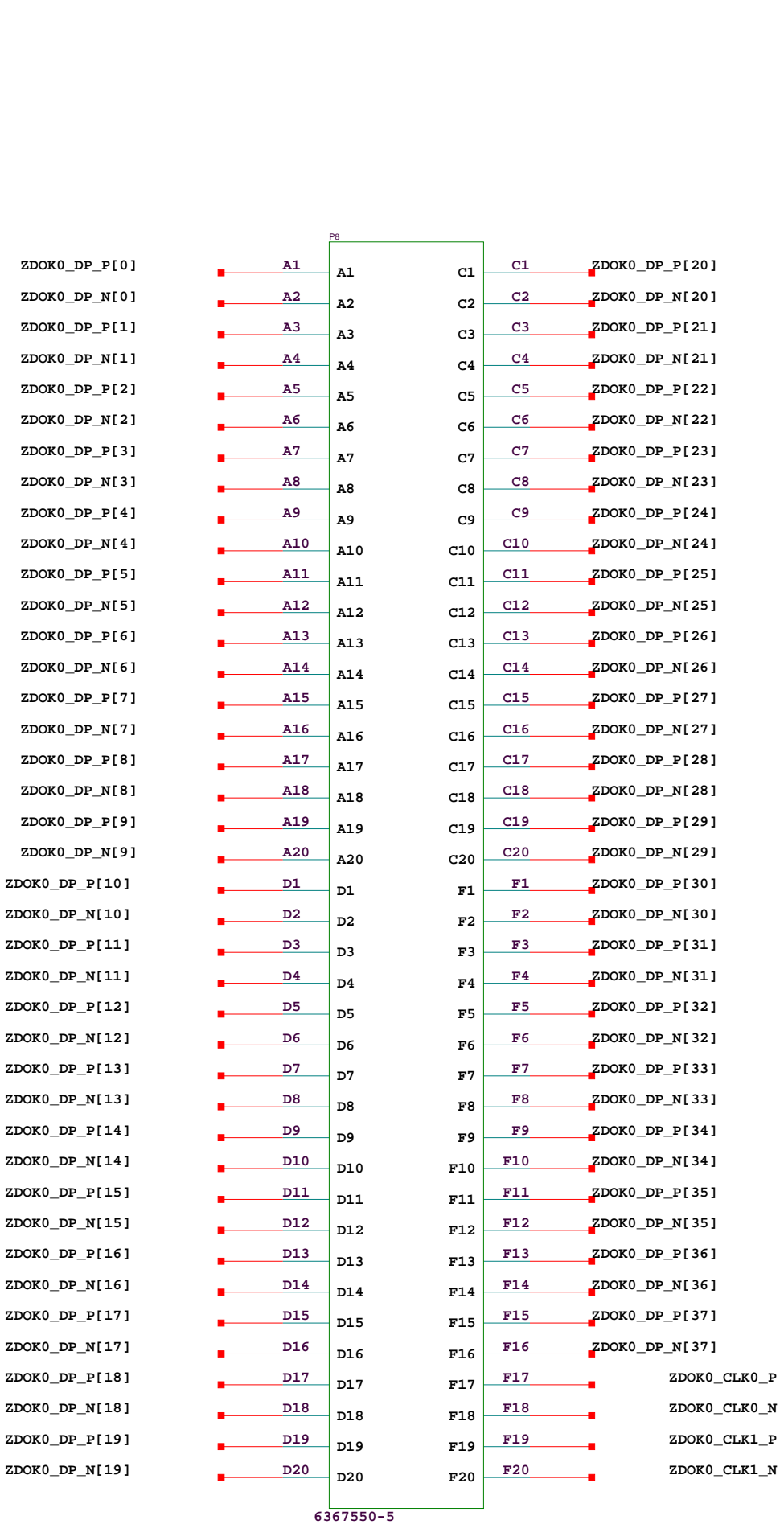
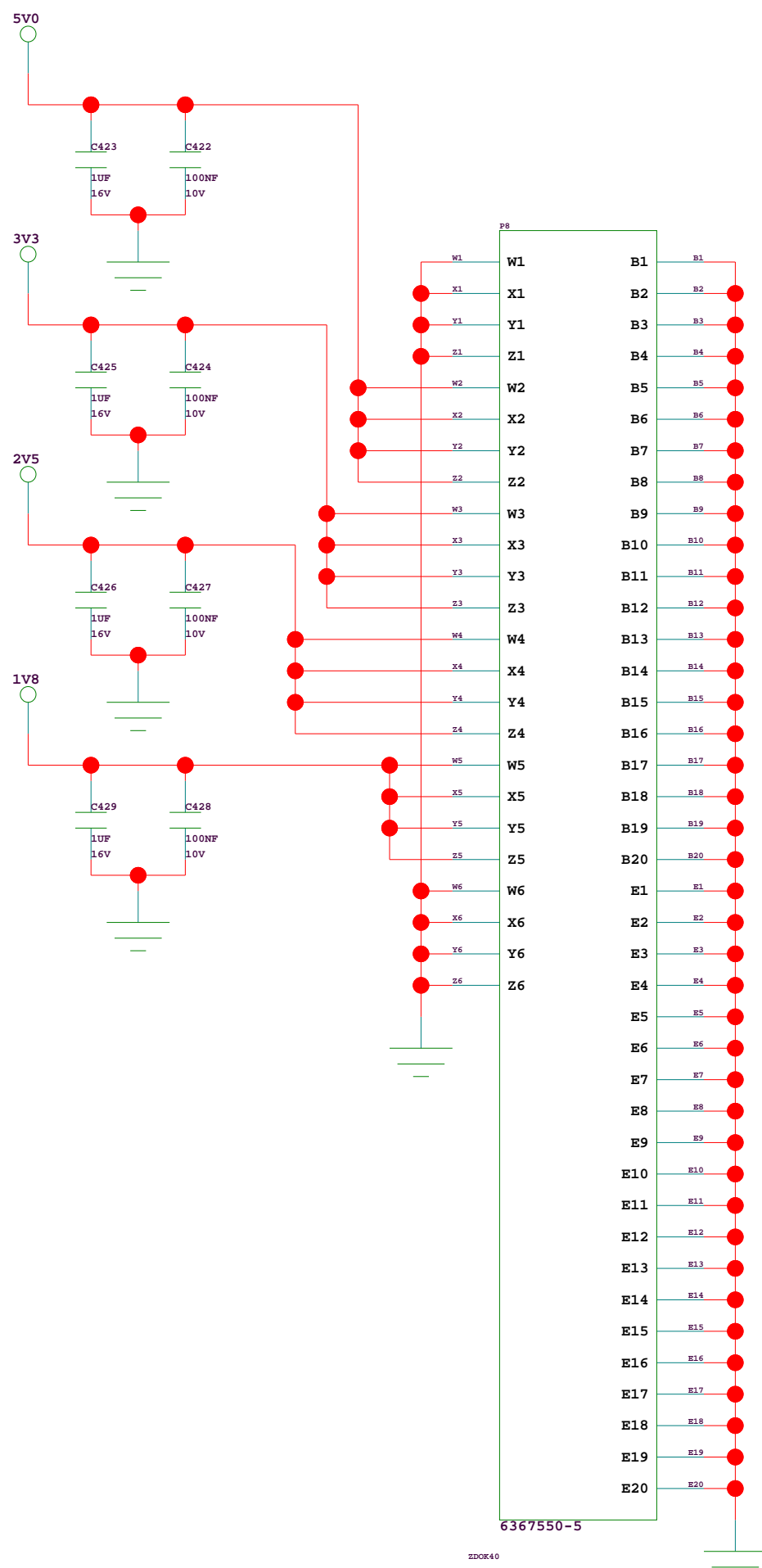
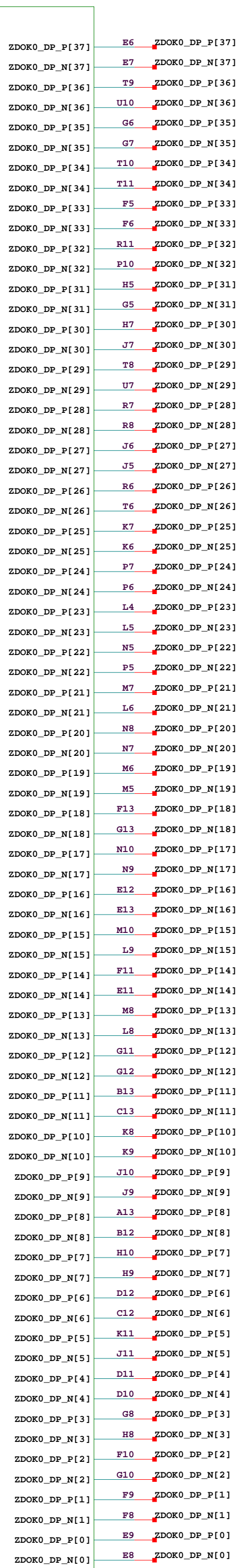
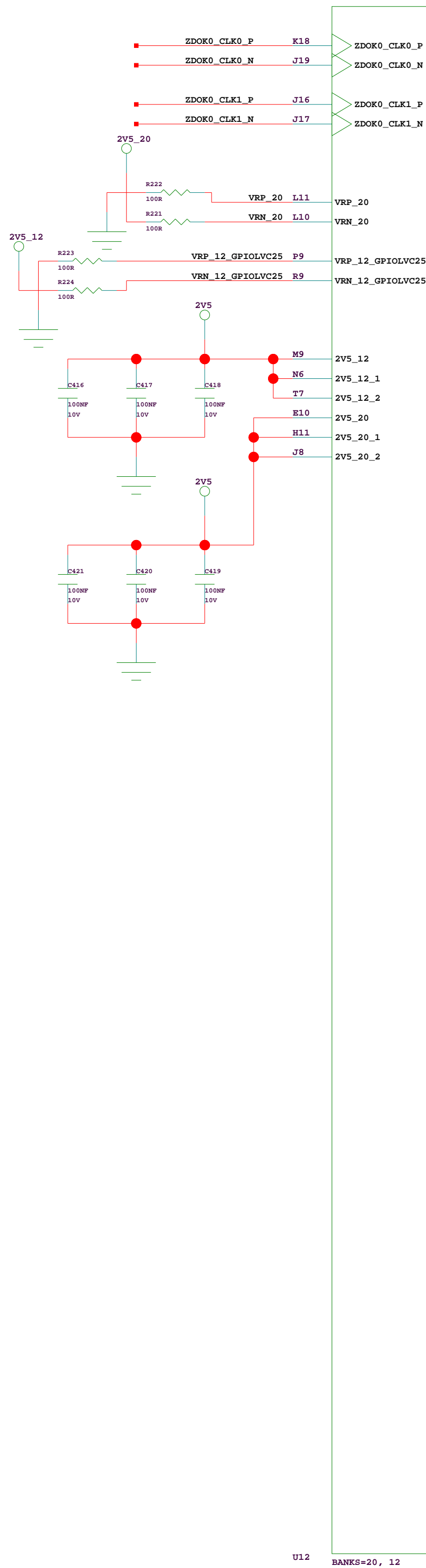






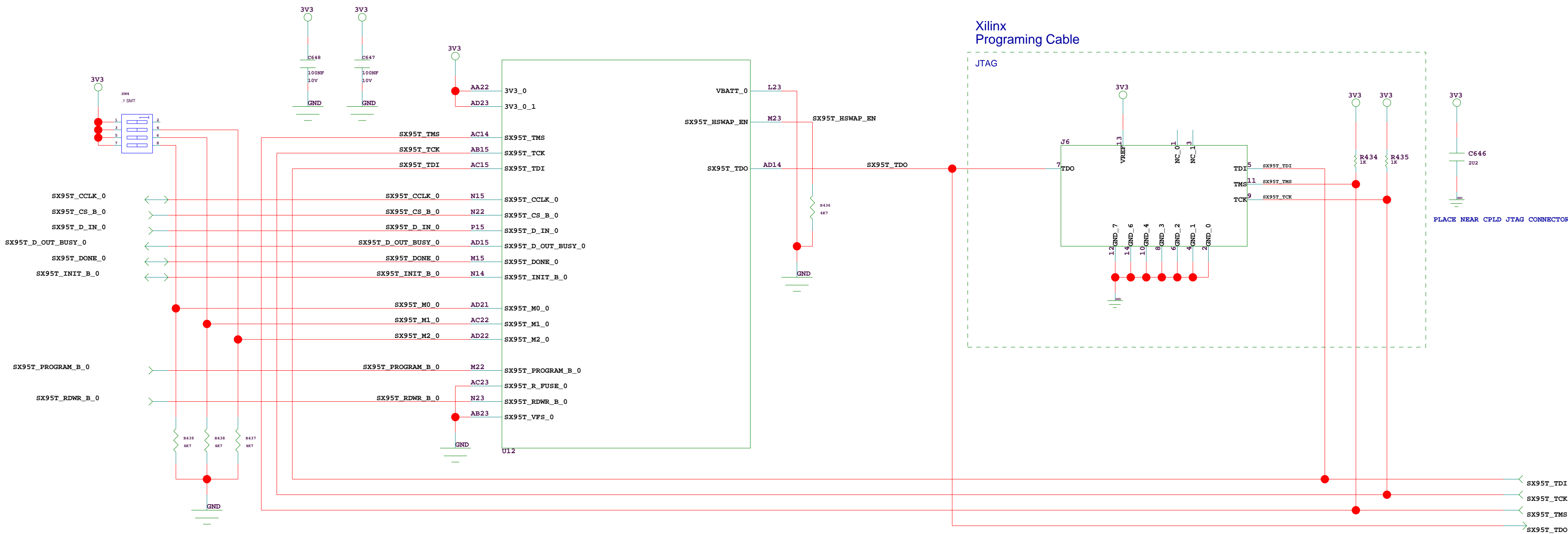
VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

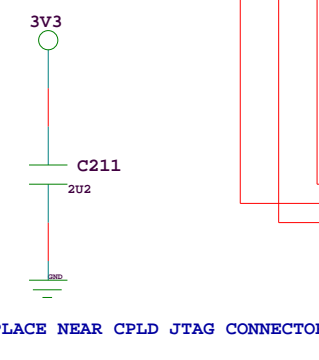
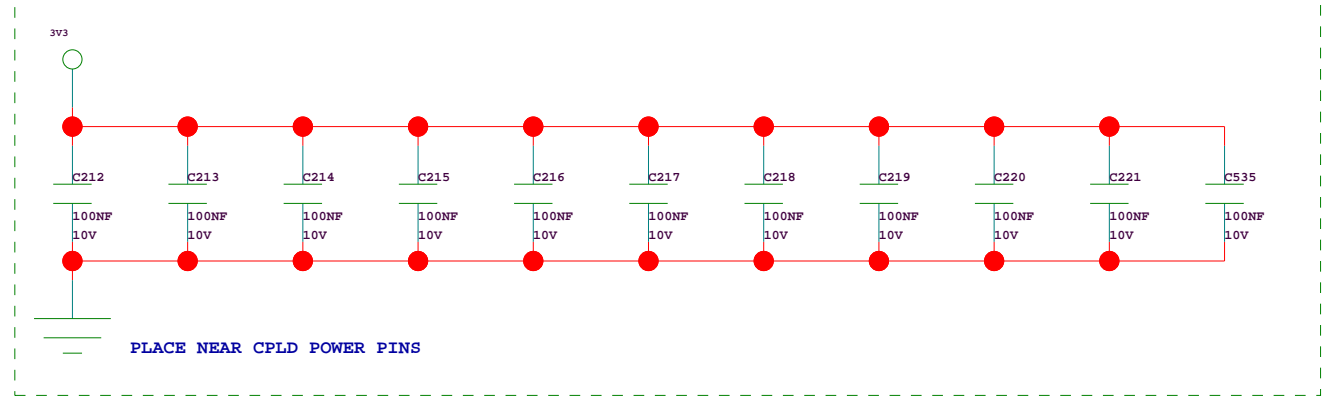
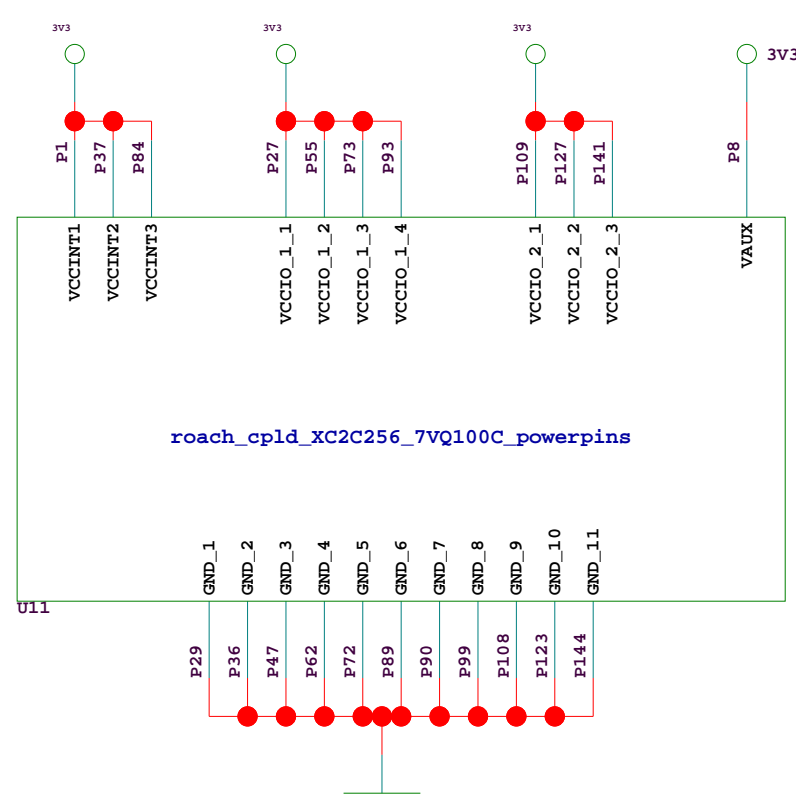
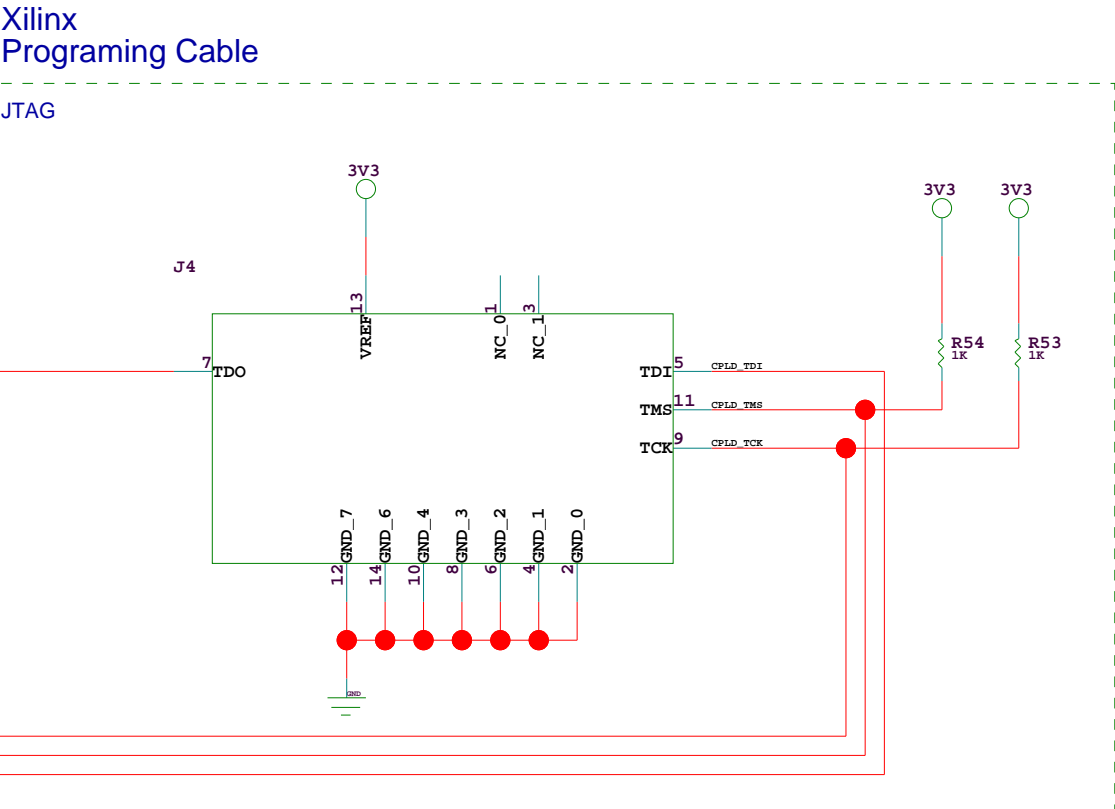
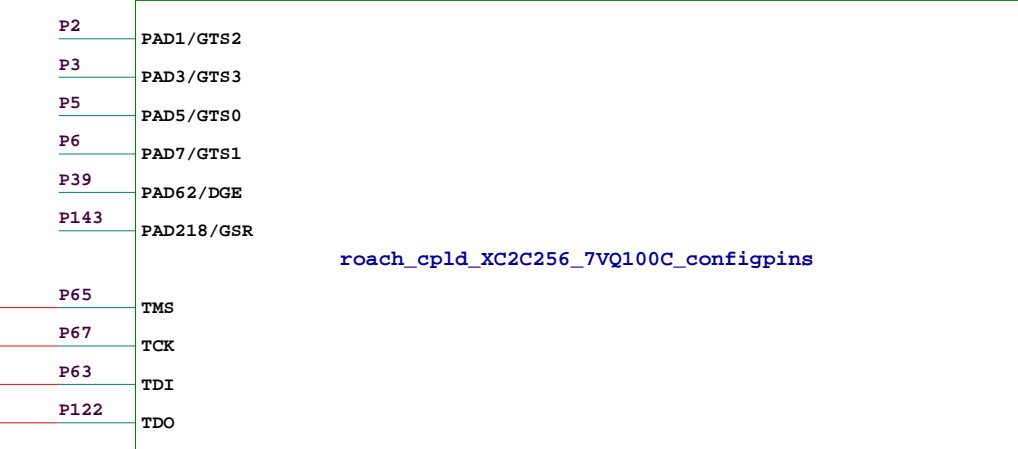
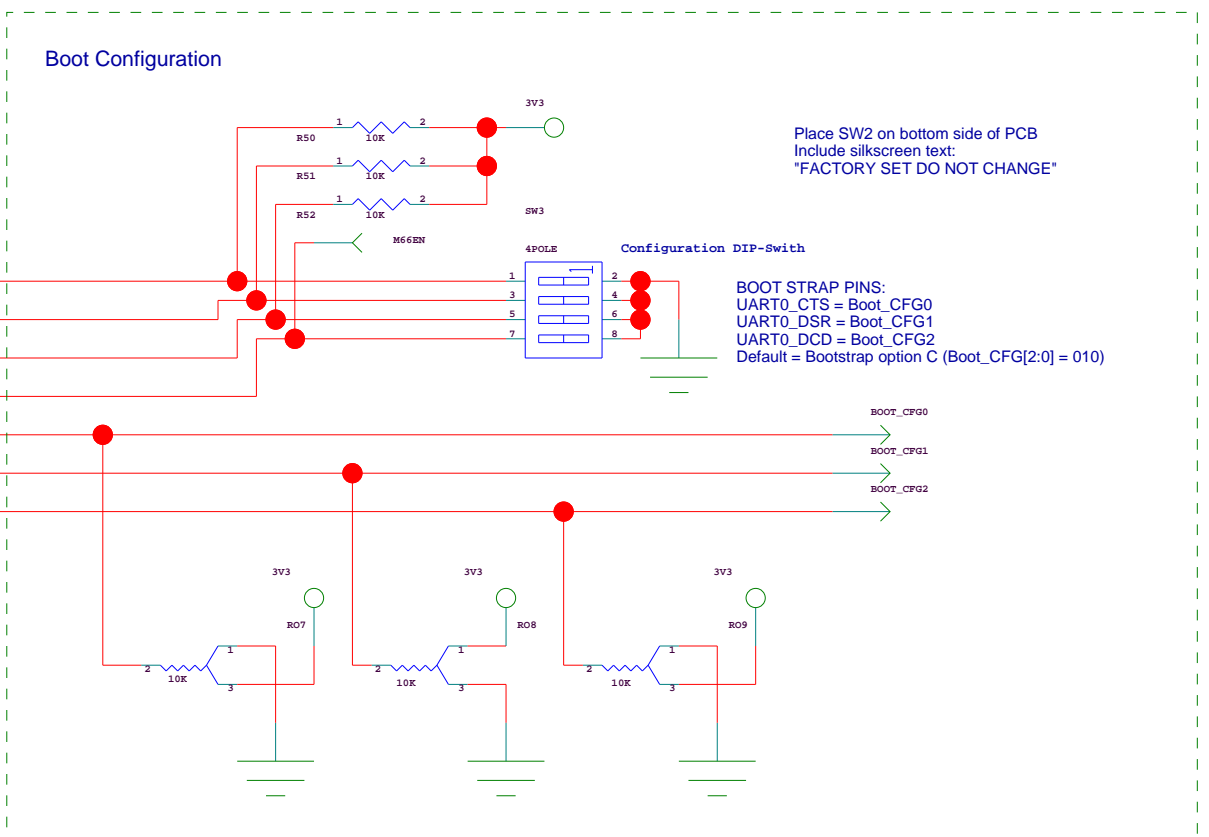
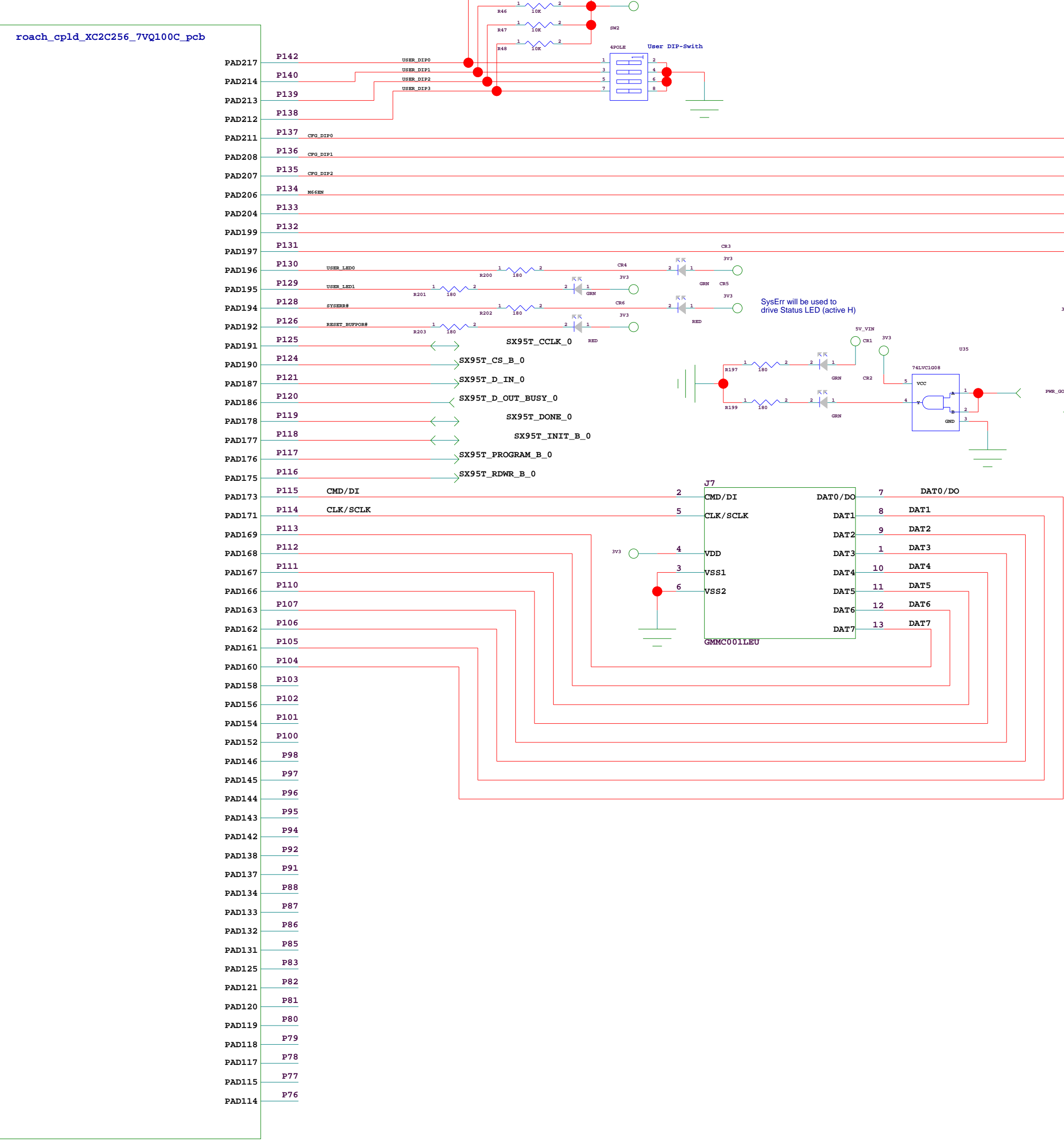
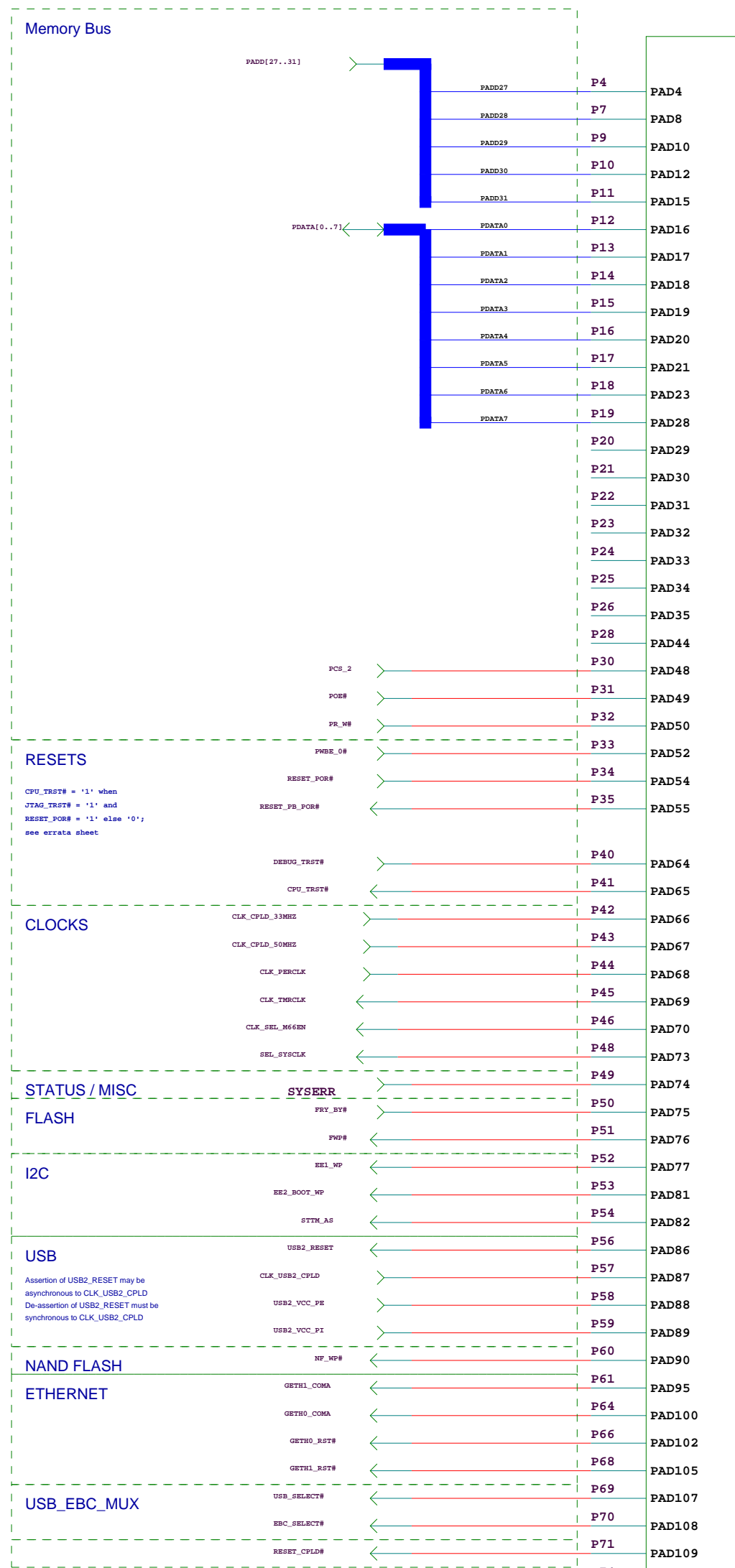




TBD

VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input



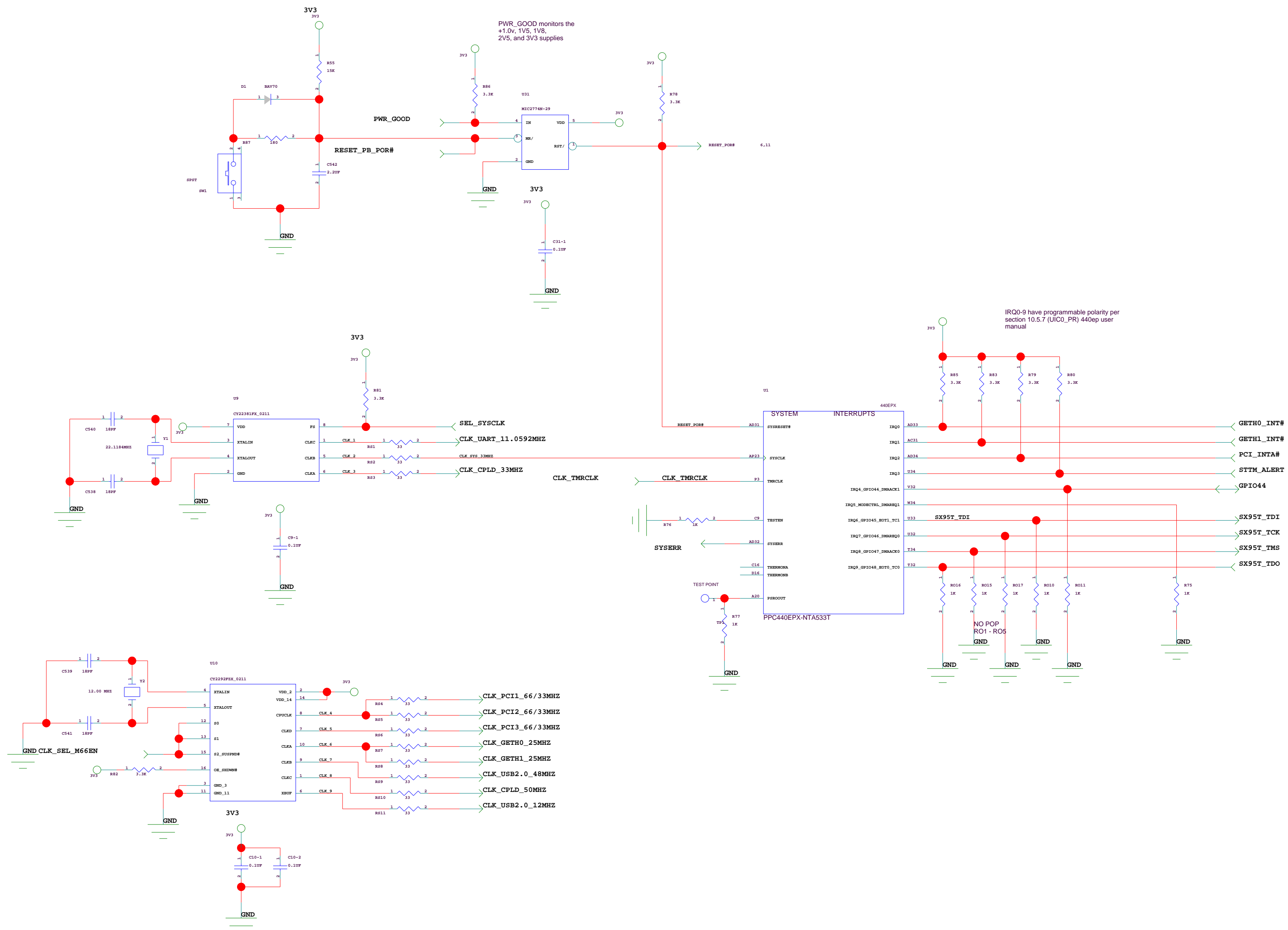


Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART 11.0592mhz = as short as possible
CLK_SYS_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PC13_66/33mhz = as short as possible
CLK_PC12_66/33mhz = CLK_PC13_66/33mhz
CLK_PC11_66/33mhz = CLK_PC12_66/33mhz + 2.5°
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = CLK_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2_0_48mhz = as short as possible
CLK_USB2_0_12mhz = as short as possible



TRACE & JTAG CONNECTORS

Critical placement and routing
of the Trace connector and nets.
Up to CPU frequency!

