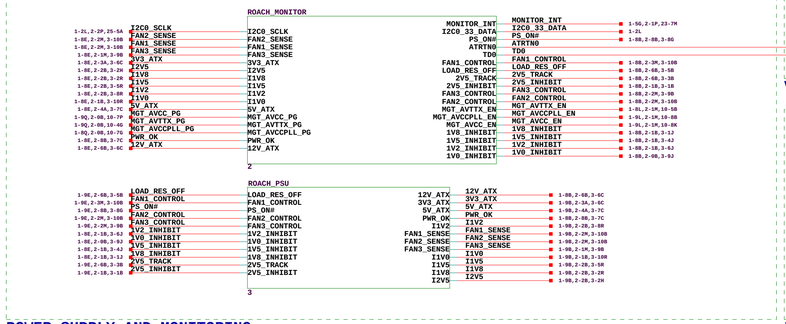
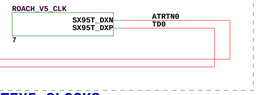
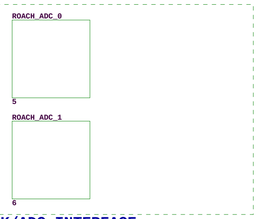
VIRTEX5

POWER SUPPLY AND MONITORING



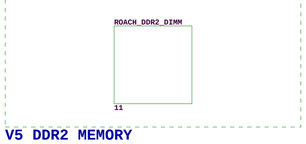
VIRTEX5 CLOCKS



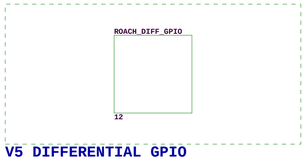


ZDOK/ADC INTERFACE

V5 DDR2 MEMORY

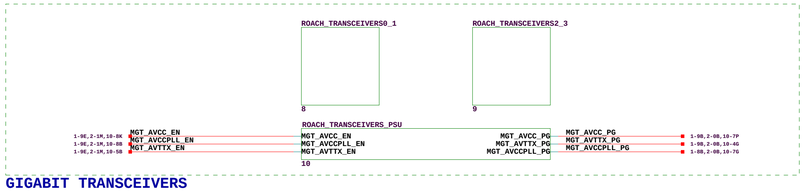


V5 DIFFERENTIAL GPIO

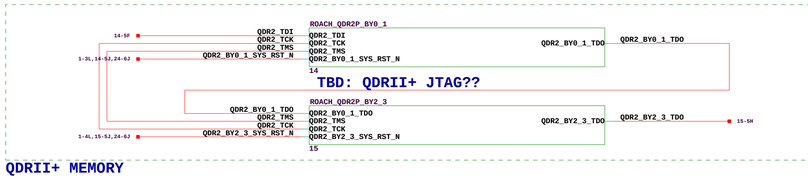


V5 SE GPIO & MISCELLANEOUS

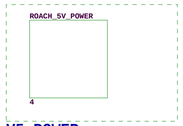
GIGABIT TRANSCEIVERS



QDRII+ MEMORY

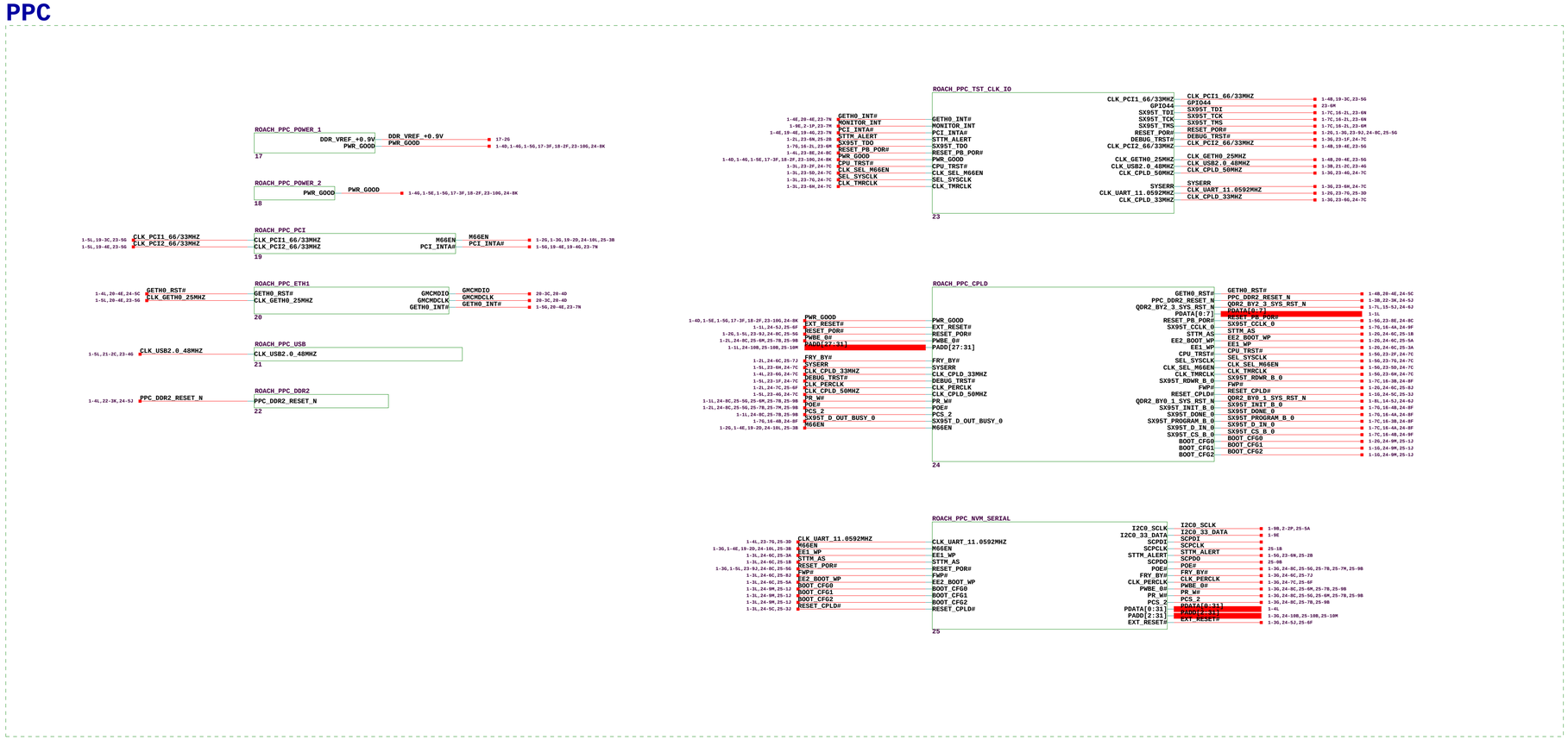


V5 POWER

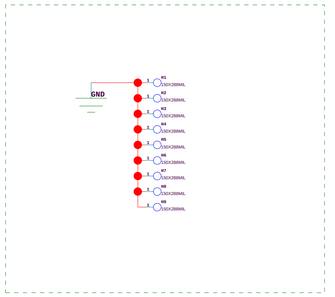


VIRTEX5 CONFIGURATION

PPC



MECHANICAL



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ROACH/iBOB2	**ROACH_TOP**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_15:15	DRAWN: F KAPP · APPR:
PATH PATH	CHECKED: E BAUERMEISTER · SHEET 1 OF 25

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

TIE TO GROUND IF PLL'S ARE NOT USED

PLACE AT ACTEL 1V5 POWER PINS

PLACE AT ACTEL 3V3 POWER PINS

roach_AFS600_powerpins

roach_AFS600_configpins

roach_AFS600_pcb

PUSH BUTTON POWER SWITCH

XPORT - PLACE IN REAR I/O REGION

TEMPERATURE DIODE HEADER

ACTEL JTAG CONNECTOR

MONITOR RESET

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

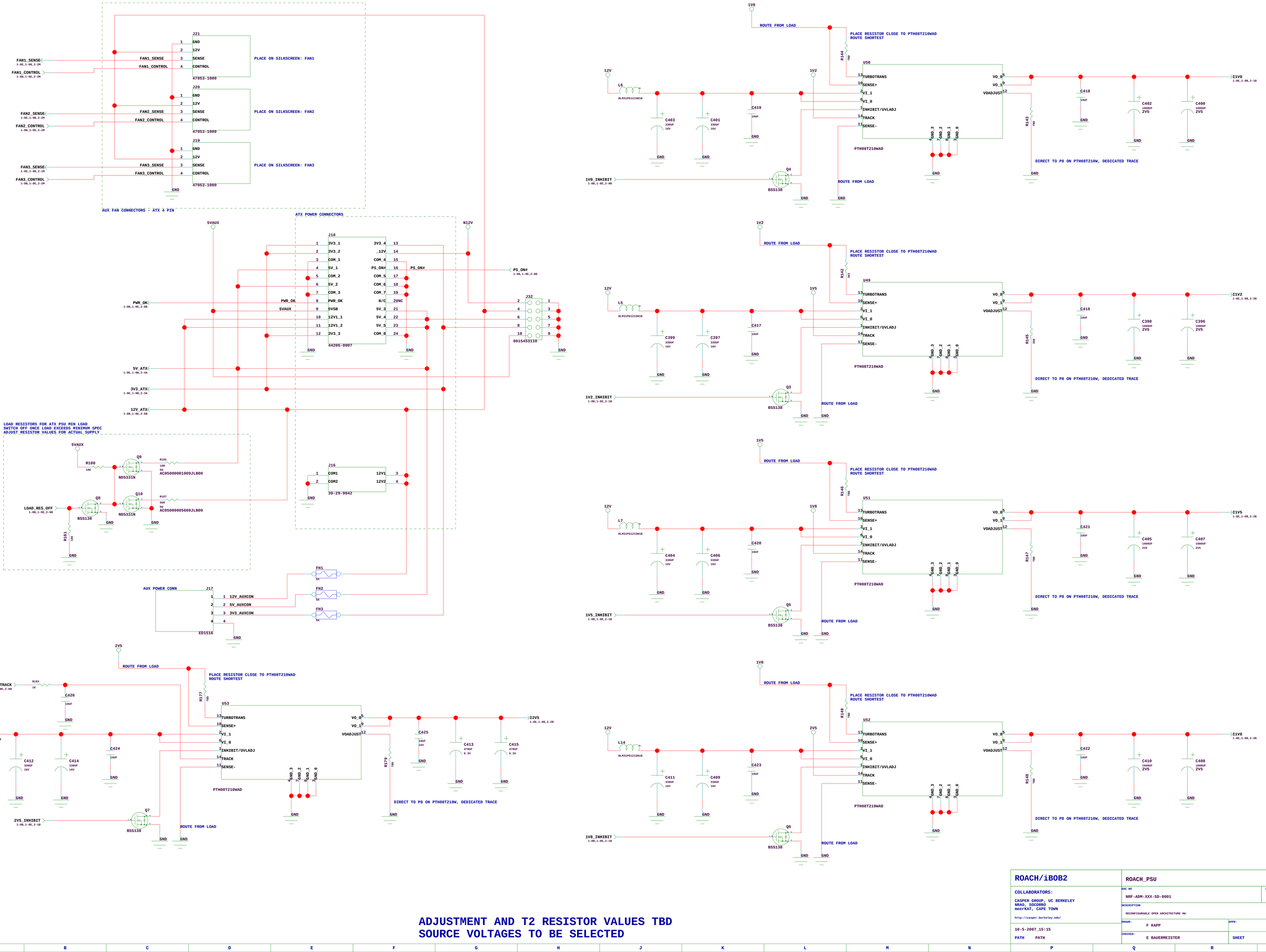
http://casper.berkeley.edu/

10-5-2007_15:15

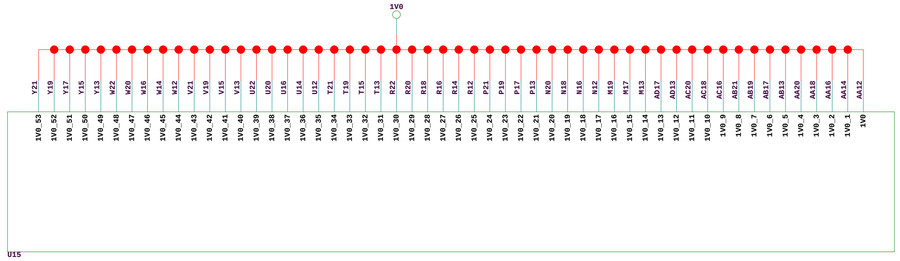
PATH PATH

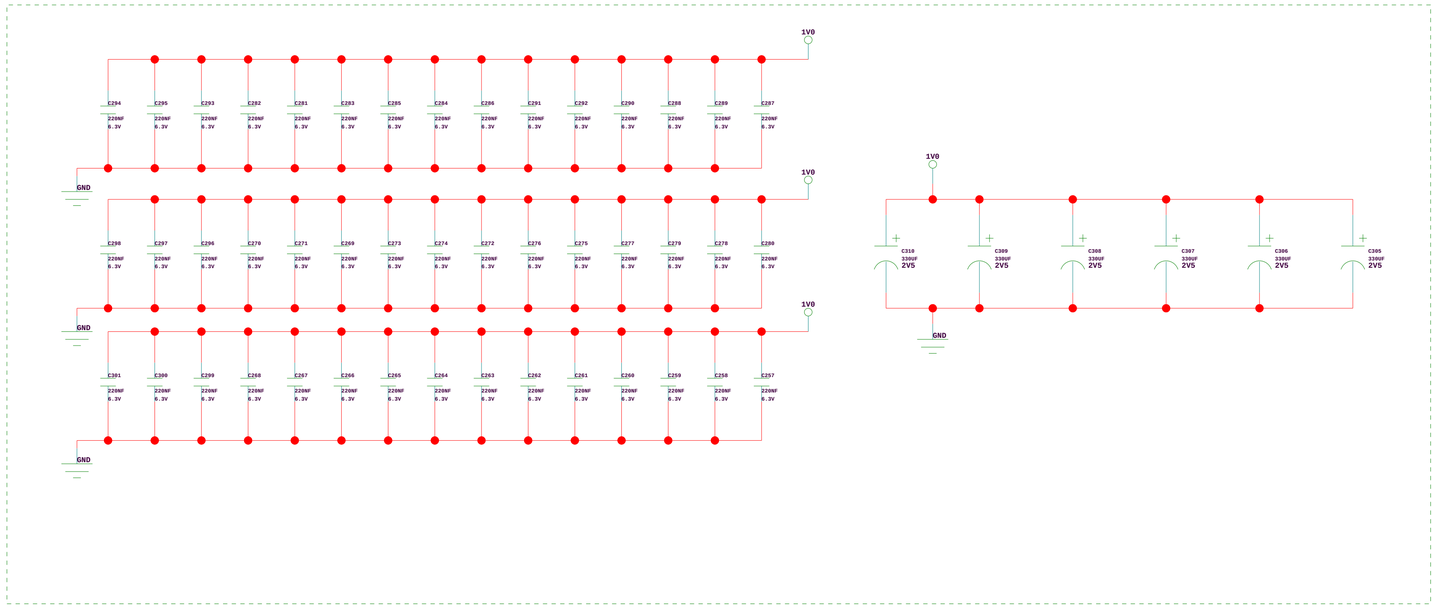
ROACH_MONITOR

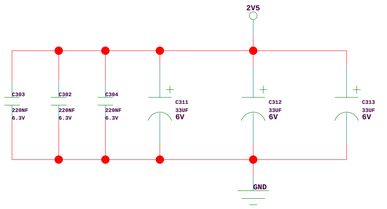
DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	2 OF 25

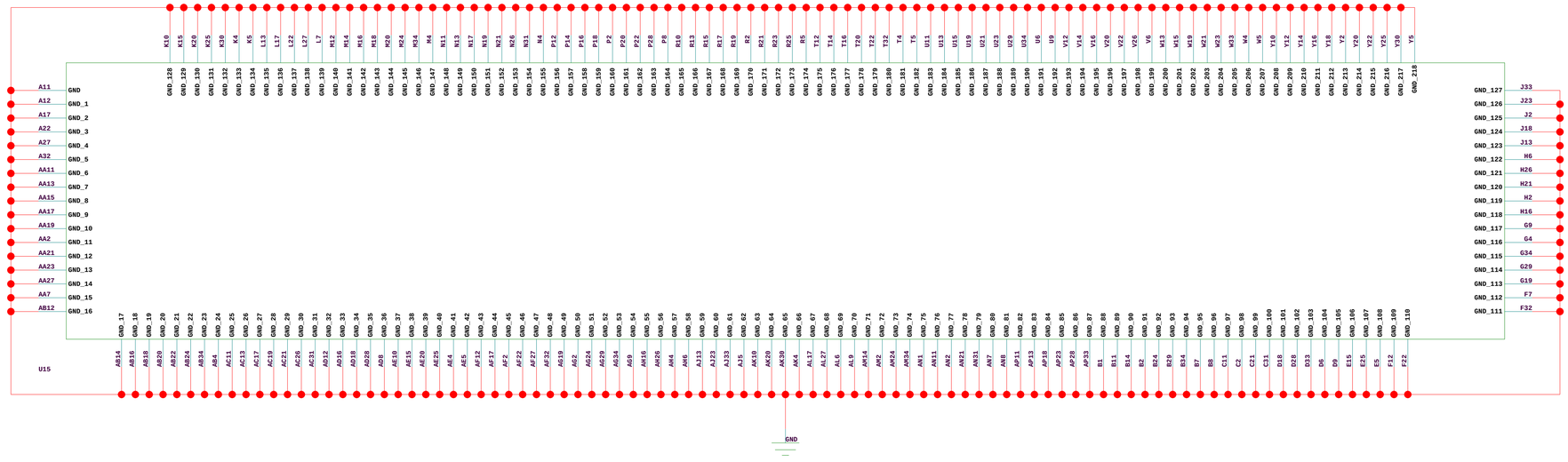


ROACH/iBOB2	ROACH_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE RW
10-5-2007_15:15 PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 3 OF 25

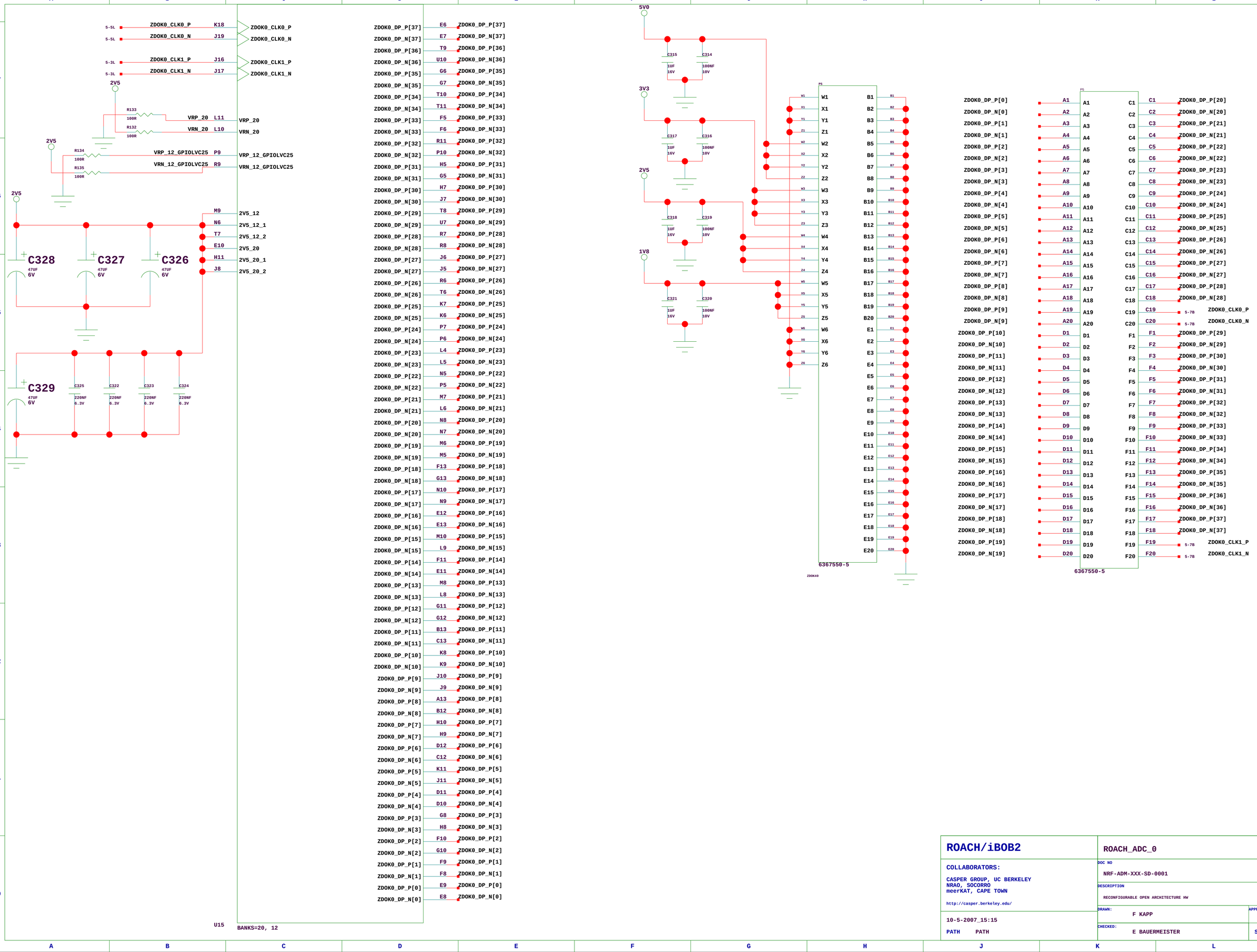








ROACH/iBOB2	**ROACH_5V_POWER**	
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
10-5-2007_15:15 PATH PATH	DRAWN: F KAPP	APPR:
	CHECKED: E BAUERMEISTER	SHEET: 4 OF 25



ROACH/iBOB2	**ROACH_ADC_0**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 5 OF 25
10-5-2007_15:15 PATH PATH	

ZDOK1_CLK0_P 6-7L → L19 → ZDOK1_CLK0_P
ZDOK1_CLK0_N 6-7L → K19 → ZDOK1_CLK0_N
ZDOK1_CLK1_P 6-7L → H14 → ZDOK1_CLK1_P
ZDOK1_CLK1_N 6-7L → H15 → ZDOK1_CLK1_N

2V5
R137 100R → VRP_18 AG6 → VRP_18
R136 100R → VRN_18 AH5 → VRN_18

2V5
R138 100R → VRP_22_GPIOLVC25 AE9 → VRP_22_GPIOLVC25
R139 100R → VRN_22_GPIOLVC25 AF8 → VRN_22_GPIOLVC25

2V5
C348 47UF 6V
C349 47UF 6V
C350 47UF 6V
AB9 → 2V5_18
AC6 → 2V5_18_1
W8 → 2V5_18_2
AF7 → 2V5_22
AH11 → 2V5_22_1
AJ8 → 2V5_22_2

C351 47UF 6V
C344 220NF 6.3V
C345 220NF 6.3V
C346 220NF 6.3V
C347 220NF 6.3V

ZDOK1_DP_P[37]	AG10	ZDOK1_DP_P[37]
ZDOK1_DP_N[37]	AG11	ZDOK1_DP_N[37]
ZDOK1_DP_P[36]	AG8	ZDOK1_DP_P[36]
ZDOK1_DP_N[36]	AH8	ZDOK1_DP_N[36]
ZDOK1_DP_P[35]	AH9	ZDOK1_DP_P[35]
ZDOK1_DP_N[35]	AH10	ZDOK1_DP_N[35]
ZDOK1_DP_P[34]	AF11	ZDOK1_DP_P[34]
ZDOK1_DP_N[34]	AE11	ZDOK1_DP_N[34]
ZDOK1_DP_P[33]	AJ9	ZDOK1_DP_P[33]
ZDOK1_DP_N[33]	AJ10	ZDOK1_DP_N[33]
ZDOK1_DP_P[32]	AF9	ZDOK1_DP_P[32]
ZDOK1_DP_N[32]	AF10	ZDOK1_DP_N[32]
ZDOK1_DP_P[31]	AK8	ZDOK1_DP_P[31]
ZDOK1_DP_N[31]	AK9	ZDOK1_DP_N[31]
ZDOK1_DP_P[30]	AK11	ZDOK1_DP_P[30]
ZDOK1_DP_N[30]	AJ11	ZDOK1_DP_N[30]
ZDOK1_DP_P[29]	AD10	ZDOK1_DP_P[29]
ZDOK1_DP_N[29]	AD11	ZDOK1_DP_N[29]
ZDOK1_DP_P[28]	AE8	ZDOK1_DP_P[28]
ZDOK1_DP_N[28]	AD9	ZDOK1_DP_N[28]
ZDOK1_DP_P[27]	AL11	ZDOK1_DP_P[27]
ZDOK1_DP_N[27]	AL10	ZDOK1_DP_N[27]
ZDOK1_DP_P[26]	AC10	ZDOK1_DP_P[26]
ZDOK1_DP_N[26]	AC9	ZDOK1_DP_N[26]
ZDOK1_DP_P[25]	AM12	ZDOK1_DP_P[25]
ZDOK1_DP_N[25]	AM11	ZDOK1_DP_N[25]
ZDOK1_DP_P[24]	AC8	ZDOK1_DP_P[24]
ZDOK1_DP_N[24]	AB8	ZDOK1_DP_N[24]
ZDOK1_DP_P[23]	AP12	ZDOK1_DP_P[23]
ZDOK1_DP_N[23]	AN12	ZDOK1_DP_N[23]
ZDOK1_DP_P[22]	AA8	ZDOK1_DP_P[22]
ZDOK1_DP_N[22]	AA9	ZDOK1_DP_N[22]
ZDOK1_DP_P[21]	AN13	ZDOK1_DP_P[21]
ZDOK1_DP_N[21]	AM13	ZDOK1_DP_N[21]
ZDOK1_DP_P[20]	AB10	ZDOK1_DP_P[20]
ZDOK1_DP_N[20]	AA10	ZDOK1_DP_N[20]
ZDOK1_DP_P[19]	AN14	ZDOK1_DP_P[19]
ZDOK1_DP_N[19]	AP14	ZDOK1_DP_N[19]
ZDOK1_DP_P[18]	V10	ZDOK1_DP_P[18]
ZDOK1_DP_N[18]	V9	ZDOK1_DP_N[18]
ZDOK1_DP_P[17]	AK7	ZDOK1_DP_P[17]
ZDOK1_DP_N[17]	AK6	ZDOK1_DP_N[17]
ZDOK1_DP_P[16]	V8	ZDOK1_DP_P[16]
ZDOK1_DP_N[16]	U8	ZDOK1_DP_N[16]
ZDOK1_DP_P[15]	AJ7	ZDOK1_DP_P[15]
ZDOK1_DP_N[15]	AJ6	ZDOK1_DP_N[15]
ZDOK1_DP_P[14]	W10	ZDOK1_DP_P[14]
ZDOK1_DP_N[14]	W9	ZDOK1_DP_N[14]
ZDOK1_DP_P[13]	AH7	ZDOK1_DP_P[13]
ZDOK1_DP_N[13]	AG7	ZDOK1_DP_N[13]
ZDOK1_DP_P[12]	Y11	ZDOK1_DP_P[12]
ZDOK1_DP_N[12]	W11	ZDOK1_DP_N[12]
ZDOK1_DP_P[11]	W7	ZDOK1_DP_P[11]
ZDOK1_DP_N[11]	V7	ZDOK1_DP_N[11]
ZDOK1_DP_P[10]	AG5	ZDOK1_DP_P[10]
ZDOK1_DP_N[10]	AF5	ZDOK1_DP_N[10]
ZDOK1_DP_P[9]	AE7	ZDOK1_DP_P[9]
ZDOK1_DP_N[9]	AF6	ZDOK1_DP_N[9]
ZDOK1_DP_P[8]	W6	ZDOK1_DP_P[8]
ZDOK1_DP_N[8]	Y6	ZDOK1_DP_N[8]
ZDOK1_DP_P[7]	AD6	ZDOK1_DP_P[7]
ZDOK1_DP_N[7]	AE6	ZDOK1_DP_N[7]
ZDOK1_DP_P[6]	AA6	ZDOK1_DP_P[6]
ZDOK1_DP_N[6]	Y7	ZDOK1_DP_N[6]
ZDOK1_DP_P[5]	AD4	ZDOK1_DP_P[5]
ZDOK1_DP_N[5]	AD5	ZDOK1_DP_N[5]
ZDOK1_DP_P[4]	Y8	ZDOK1_DP_P[4]
ZDOK1_DP_N[4]	Y9	ZDOK1_DP_N[4]
ZDOK1_DP_P[3]	AC7	ZDOK1_DP_P[3]
ZDOK1_DP_N[3]	AD7	ZDOK1_DP_N[3]
ZDOK1_DP_P[2]	AA5	ZDOK1_DP_P[2]
ZDOK1_DP_N[2]	AB5	ZDOK1_DP_N[2]
ZDOK1_DP_P[1]	AB6	ZDOK1_DP_P[1]
ZDOK1_DP_N[1]	AB7	ZDOK1_DP_N[1]
ZDOK1_DP_P[0]	AC4	ZDOK1_DP_P[0]
ZDOK1_DP_N[0]	AC5	ZDOK1_DP_N[0]

U15
BANKS=18, 22

5V0
C337 1UF 16V
C336 100NF 10V
3V3
C339 1UF 16V
C338 100NF 10V
2V5
C340 1UF 16V
C341 100NF 10V
1V8
C343 1UF 16V
C342 100NF 10V

P7 — 6367550-5

W1	W1	B1
X1	X1	B2
Y1	Y1	B3
Z1	Z1	B4
W2	W2	B5
X2	X2	B6
Y2	Y2	B7
Z2	Z2	B8
W3	W3	B9
X3	X3	B10
Y3	Y3	B11
Z3	Z3	B12
W4	W4	B13
X4	X4	B14
Y4	Y4	B15
Z4	Z4	B16
W5	W5	B17
X5	X5	B18
Y5	Y5	B19
Z5	Z5	B20
W6	W6	E1
X6	X6	E2
Y6	Y6	E3
Z6	Z6	E4
		E5
		E6
		E7
		E8
		E9
		E10
		E11
		E12
		E13
		E14
		E15
		E16
		E17
		E18
		E19
		E20

ZDOK49

ZDOK1_DP_P[0]	A1	A1
ZDOK1_DP_N[0]	A2	A2
ZDOK1_DP_P[1]	A3	A3
ZDOK1_DP_N[1]	A4	A4
ZDOK1_DP_P[2]	A5	A5
ZDOK1_DP_N[2]	A6	A6
ZDOK1_DP_P[3]	A7	A7
ZDOK1_DP_N[3]	A8	A8
ZDOK1_DP_P[4]	A9	A9
ZDOK1_DP_N[4]	A10	A10
ZDOK1_DP_P[5]	A11	A11
ZDOK1_DP_N[5]	A12	A12
ZDOK1_DP_P[6]	A13	A13
ZDOK1_DP_N[6]	A14	A14
ZDOK1_DP_P[7]	A15	A15
ZDOK1_DP_N[7]	A16	A16
ZDOK1_DP_P[8]	A17	A17
ZDOK1_DP_N[8]	A18	A18
ZDOK1_DP_P[9]	A19	A19
ZDOK1_DP_N[9]	A20	A20
ZDOK1_DP_P[10]	D1	D1
ZDOK1_DP_N[10]	D2	D2
ZDOK1_DP_P[11]	D3	D3
ZDOK1_DP_N[11]	D4	D4
ZDOK1_DP_P[12]	D5	D5
ZDOK1_DP_N[12]	D6	D6
ZDOK1_DP_P[13]	D7	D7
ZDOK1_DP_N[13]	D8	D8
ZDOK1_DP_P[14]	D9	D9
ZDOK1_DP_N[14]	D10	D10
ZDOK1_DP_P[15]	D11	D11
ZDOK1_DP_N[15]	D12	D12
ZDOK1_DP_P[16]	D13	D13
ZDOK1_DP_N[16]	D14	D14
ZDOK1_DP_P[17]	D15	D15
ZDOK1_DP_N[17]	D16	D16
ZDOK1_DP_P[18]	D17	D17
ZDOK1_DP_N[18]	D18	D18
ZDOK1_DP_P[19]	D19	D19
ZDOK1_DP_N[19]	D20	D20

P7 — 6367550-5

C1	C1	ZDOK1_DP_P[20]
C2	C2	ZDOK1_DP_N[20]
C3	C3	ZDOK1_DP_P[21]
C4	C4	ZDOK1_DP_N[21]
C5	C5	ZDOK1_DP_P[22]
C6	C6	ZDOK1_DP_N[22]
C7	C7	ZDOK1_DP_P[23]
C8	C8	ZDOK1_DP_N[23]
C9	C9	ZDOK1_DP_P[24]
C10	C10	ZDOK1_DP_N[24]
C11	C11	ZDOK1_DP_P[25]
C12	C12	ZDOK1_DP_N[25]
C13	C13	ZDOK1_DP_P[26]
C14	C14	ZDOK1_DP_N[26]
C15	C15	ZDOK1_DP_P[27]
C16	C16	ZDOK1_DP_N[27]
C17	C17	ZDOK1_DP_P[28]
C18	C18	ZDOK1_DP_N[28]
C19	6-7B	ZDOK1_CLK0_P
C20	6-7B	ZDOK1_CLK0_N
F1	F1	ZDOK1_DP_P[29]
F2	F2	ZDOK1_DP_N[29]
F3	F3	ZDOK1_DP_P[30]
F4	F4	ZDOK1_DP_N[30]
F5	F5	ZDOK1_DP_P[31]
F6	F6	ZDOK1_DP_N[31]
F7	F7	ZDOK1_DP_P[32]
F8	F8	ZDOK1_DP_N[32]
F9	F9	ZDOK1_DP_P[33]
F10	F10	ZDOK1_DP_N[33]
F11	F11	ZDOK1_DP_P[34]
F12	F12	ZDOK1_DP_N[34]
F13	F13	ZDOK1_DP_P[35]
F14	F14	ZDOK1_DP_N[35]
F15	F15	ZDOK1_DP_P[36]
F16	F16	ZDOK1_DP_N[36]
F17	F17	ZDOK1_DP_P[37]
F18	F18	ZDOK1_DP_N[37]
F19	6-7B	ZDOK1_CLK1_P
F20	6-7B	ZDOK1_CLK1_N

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

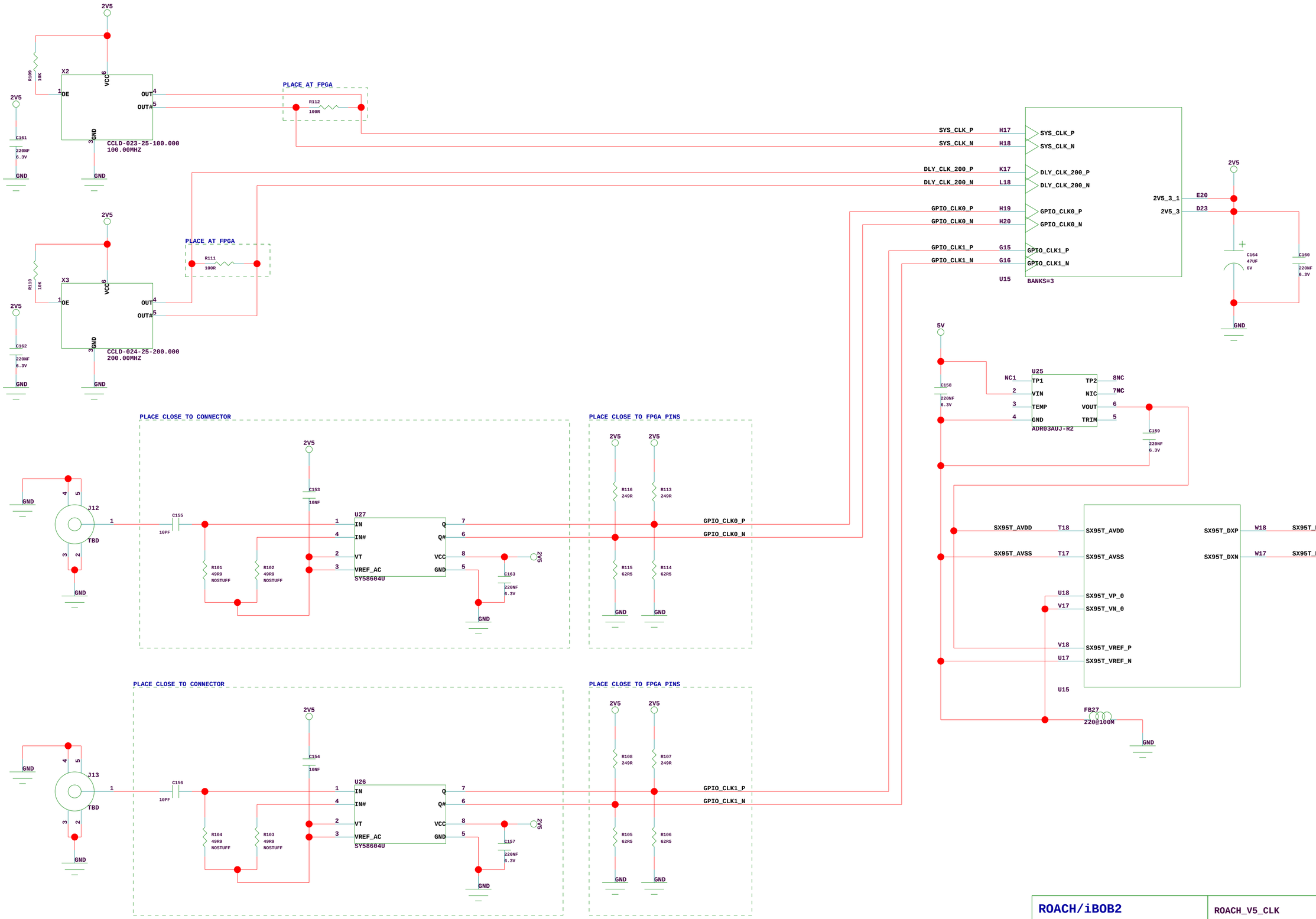
http://casper.berkeley.edu/

10-5-2007_15:15

PATH PATH

ROACH_ADC_1

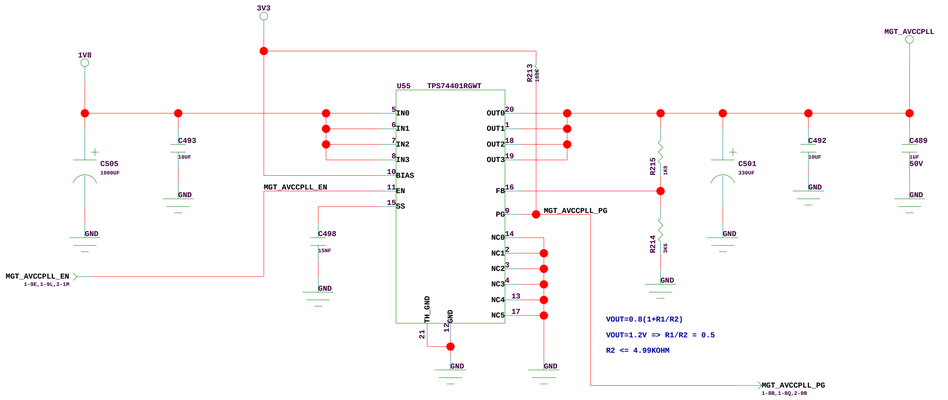
DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 6 OF 25

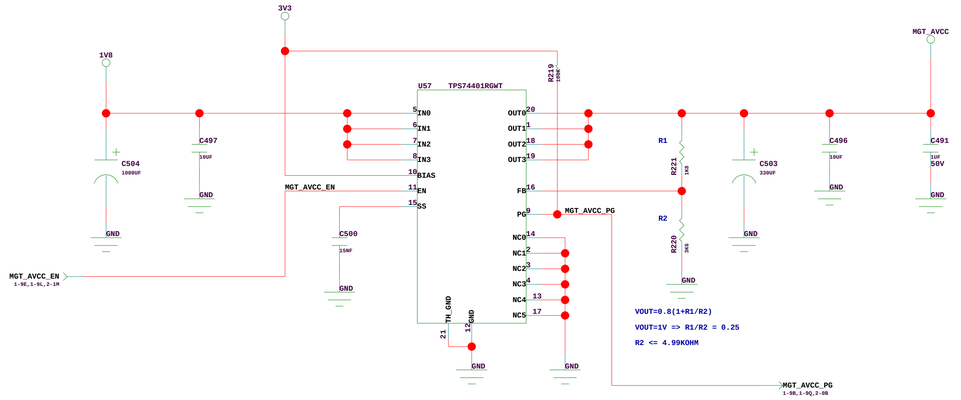


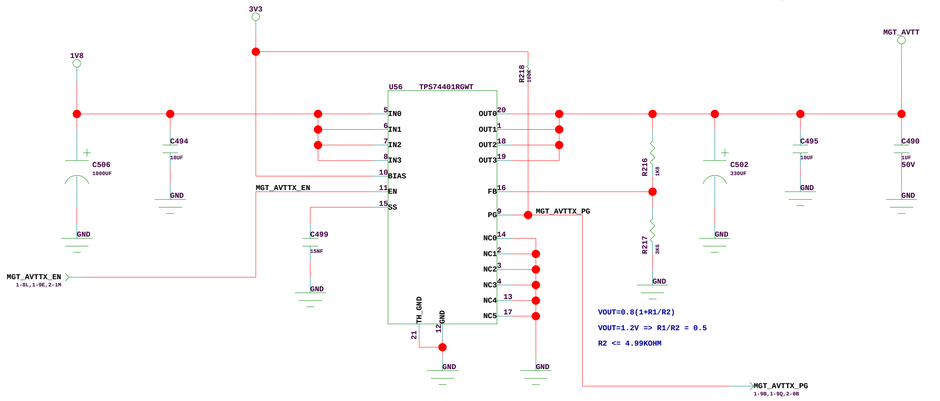
ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
10-5-2007_15:15 PATH PATH	

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB2 220@100M
FB3 220@100M
FB4 220@100M
C95 220NF 6.3V
C94 220NF 6.3V
C93 220NF 6.3V
C92 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_112 R3 MGTAVCC_112
MGTAVCC_112_1 R4 MGTAVCC_112_1
MGTAVCCPLL_112 T3 MGTAVCCPLL_112
MGTAVTTRX_112 N3 MGTAVTTRX_112
MGT_112_REF_CLK_P P4 MGT_112_REF_CLK_P
MGT_112_REF_CLK_N P3 MGT_112_REF_CLK_N
MGTRX0_112_P N1 MGTRX0_112_P
MGTRX0_112_N P1 MGTRX0_112_N
MGTRX1_112_P T1 MGTRX1_112_P
MGTRX1_112_N R1 MGTRX1_112_N
U15
MGTRREF V4 MGTRREF
MGT_VTRXC V5 MGTAVTTRXC
MGTAVTTTX_112 M3 MGTAVTTTX_112
MGTAVTTTX_112_1 U3 MGTAVTTTX_112_1
MGTTX0_112_P M2 MGTTX0_112_P
MGTTX0_112_N N2 MGTTX0_112_N
MGTTX1_112_P U2 MGTTX1_112_P
MGTTX1_112_N T2 MGTTX1_112_N
R56 49.9R
MGT_AVTT
FB25 220@100M
FB5 220@100M
FB6 220@100M
C126 220NF 6.3V
C97 220NF 6.3V
C96 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
2V5
FB26 220@100M
C137 220NF 6.3V
R84 10K
X1
CCLD-023-25-156.250
156.25MHZ
JP6
C104 10NF 25V
C105 10NF 25V
C106 10NF 25V
C107 10NF 25V
C109 10NF 25V
C108 10NF 25V
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
MGTAVTTTX_114 AC3 MGTAVTTTX_114
MGTAVTTTX_114_1 V3 MGTAVTTTX_114_1
MGTTX0_114_P V2 MGTTX0_114_P
MGTTX0_114_N W2 MGTTX0_114_N
MGTTX1_114_P AC2 MGTTX1_114_P
MGTTX1_114_N AB2 MGTTX1_114_N
FB8 220@100M
FB7 220@100M
C98 220NF 6.3V
C99 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT
MGTAVCC_114 AA3 MGTAVCC_114
MGTAVCC_114_1 AA4 MGTAVCC_114_1
MGTAVCCPLL_114 AB3 MGTAVCCPLL_114
MGTAVTTRX_114 W3 MGTAVTTRX_114
MGT_114_REF_CLK_P NC Y4 MGT_114_REF_CLK_P
MGT_114_REF_CLK_N NC Y3 MGT_114_REF_CLK_N
MGTRX0_114_P W1 MGTRX0_114_P
MGTRX0_114_N Y1 MGTRX0_114_N
MGTRX1_114_P AB1 MGTRX1_114_P
MGTRX1_114_N AA1 MGTRX1_114_N
C140 10NF 25V
C141 10NF 25V
C142 10NF 25V
C143 10NF 25V
MGTAVTTTX_118_1 AJ3 MGTAVTTTX_118_1
MGTAVTTTX_118 AD3 MGTAVTTTX_118
MGTTX0_118_P AD2 MGTTX0_118_P
MGTTX0_118_N AE2 MGTTX0_118_N
MGTTX1_118_P AJ2 MGTTX1_118_P
MGTTX1_118_N AH2 MGTTX1_118_N
FB19 220@100M
FB20 220@100M
C122 220NF 6.3V
C121 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_116 J3 MGTAVCC_116
MGTAVCC_116_1 J4 MGTAVCC_116_1
MGTAVCCPLL_116 K3 MGTAVCCPLL_116
MGTAVTTRX_116 G3 MGTAVTTRX_116
MGT_116_REF_CLK_P NC H4 MGT_116_REF_CLK_P
MGT_116_REF_CLK_N NC H3 MGT_116_REF_CLK_N
MGTRX0_116_P G1 MGTRX0_116_P
MGTRX0_116_N H1 MGTRX0_116_N
MGTRX1_116_P K1 MGTRX1_116_P
MGTRX1_116_N J1 MGTRX1_116_N
MGTTX0_116_P F2 MGTTX0_116_P
MGTTX0_116_N G2 MGTTX0_116_N
MGTTX1_116_P L2 MGTTX1_116_P
MGTTX1_116_N K2 MGTTX1_116_N
FB17 220@100M
FB18 220@100M
FB15 220@100M
FB16 220@100M
C120 220NF 6.3V
C119 220NF 6.3V
C118 220NF 6.3V
C115 220NF 6.3V
C110 10NF 25V
C111 10NF 25V
C112 10NF 25V
C113 10NF 25V
L3 MGTAVTTTX_116_1
F3 MGTAVTTTX_116
FB14 220@100M
FB13 220@100M
C116 220NF 6.3V
C117 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_118 AG3 MGTAVCC_118
MGTAVCC_118_1 AG4 MGTAVCC_118_1
MGTAVCCPLL_118 AH3 MGTAVCCPLL_118
MGTAVTTRX_118 AE3 MGTAVTTRX_118
MGT_118_REF_CLK_P NC AF4 MGT_118_REF_CLK_P
MGT_118_REF_CLK_N NC AF3 MGT_118_REF_CLK_N
MGTRX0_118_P AE1 MGTRX0_118_P
MGTRX0_118_N AF1 MGTRX0_118_N
MGTRX1_118_P AH1 MGTRX1_118_P
MGTRX1_118_N AG1 MGTRX1_118_N
C144 10NF 25V
C145 10NF 25V
C146 10NF 25V
C147 10NF 25V
FB22 220@100M
FB21 220@100M
FB24 220@100M
FB23 220@100M
C123 220NF 6.3V
C124 220NF 6.3V
C114 220NF 6.3V
C125 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
P3
FCN-268F036-G/3DB
S1 DL0P
S2 DL0N
S3 DL1P
S4 DL1N
S5 DL2P
S6 DL2N
S7 DL3P
S8 DL3N
S16 SL0P
S15 SL0N
S14 SL1P
S13 SL1N
S12 SL2P
S11 SL2N
S10 SL3P
S9 SL3N
S19 DL0P
S20 DL0N
S21 DL1P
S22 DL1N
S23 DL2P
S24 DL2N
S25 DL3P
S26 DL3N
S34 SL0P
S33 SL0N
S32 SL1P
S31 SL1N
S30 SL2P
S29 SL2N
S28 SL3P
S27 SL3N
SIG_GND1 G1
SIG_GND2 G2
SIG_GND3 G3
SIG_GND4 G4
SIG_GND5 G5
SIG_GND6 G6
SIG_GND7 G7
SIG_GND8 G8
SIG_GND9 G9
SIG_GND10 G19
SIG_GND1 G10
SIG_GND2 G11
SIG_GND3 G12
SIG_GND4 G13
SIG_GND5 G14
SIG_GND6 G15
SIG_GND7 G16
SIG_GND8 G17
SIG_GND9 G18
SIG_GND10 G19
ODIS
FAULT
JP4
JP5
R50 10K
R51 10K
C130 10NF
C134 10NF
3V3
R79 150R
D2
OPTICAL MODULE FAULT - RED LED
C131 10NF
C132 10NF
R97 5K1
R98 5K1
RS7 3K9
R93 3K9
R59 6K8
R94 6K8
RS8 3K9
R95 3K9
U21 MAX9032AKA
U20 MAX9032AKA
U22 AND2 SN74AHC1G08DCKR
U23 AND2 SN74AHC1G08DCKR
C127 10NF
C133 10NF
U18
U19
TPS2031D
R99 10K
R100 10K
C129 10NF
C128 100NF
C138 4.7UF 16V
C90 22UF
C135 10NF
C136 100NF
C139 4.7UF 16V
C91 22UF
R82 150R

ROACH/iBOB2	ROACH_TRANSCEIVERS0_1
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
10-5-2007_15:15	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET: 8 OF 25







ROACH/iBOB2

ROACH_TRANSCEIVERS_PSU

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

10-5-2007_15:15

PATH PATH

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

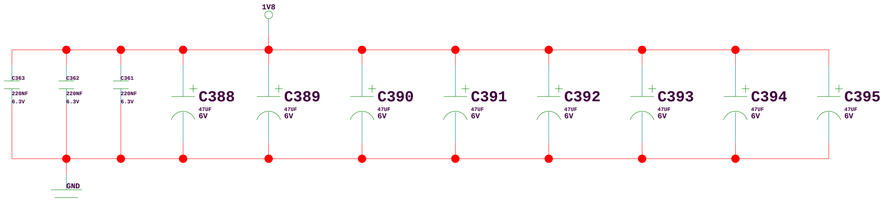
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

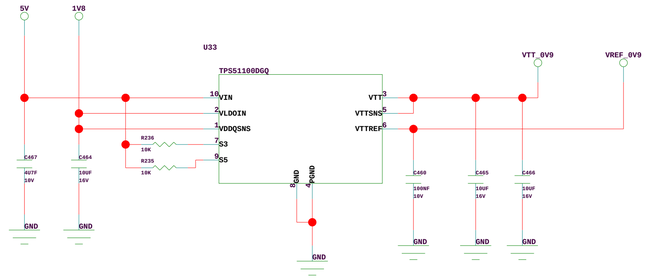
DRAWN: F KAPP

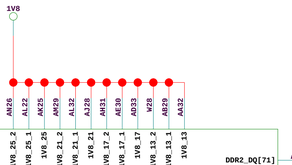
APPR:

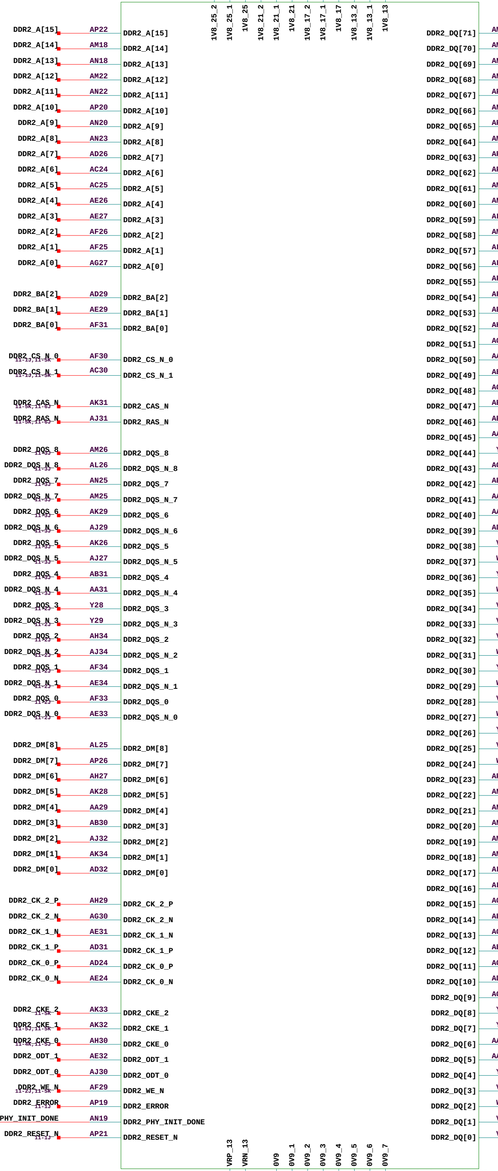
CHECKED: E BAUERMEISTER

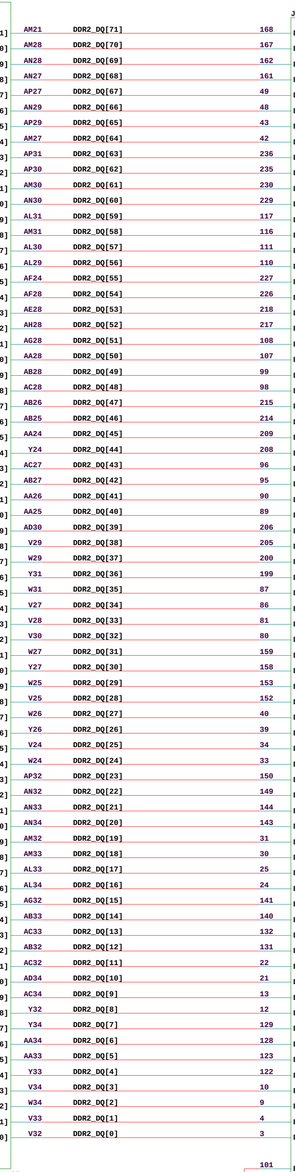
SHEET 10 OF 25

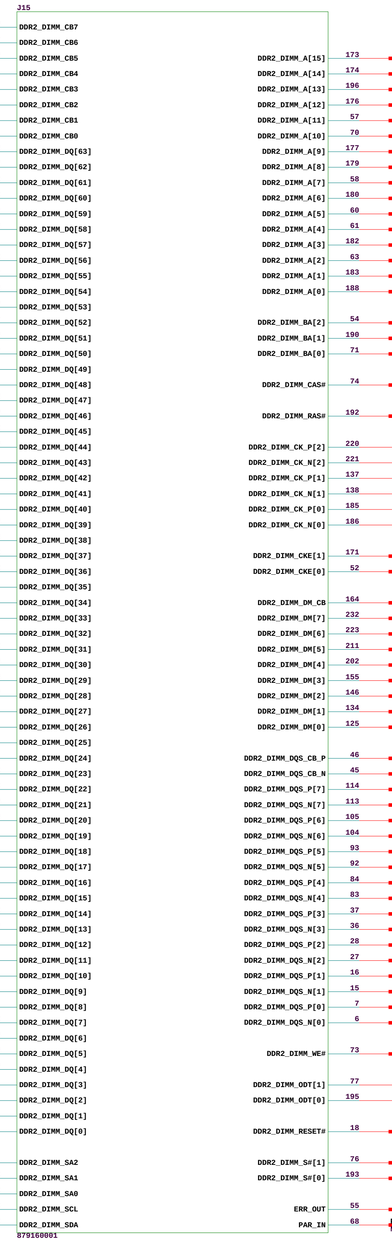


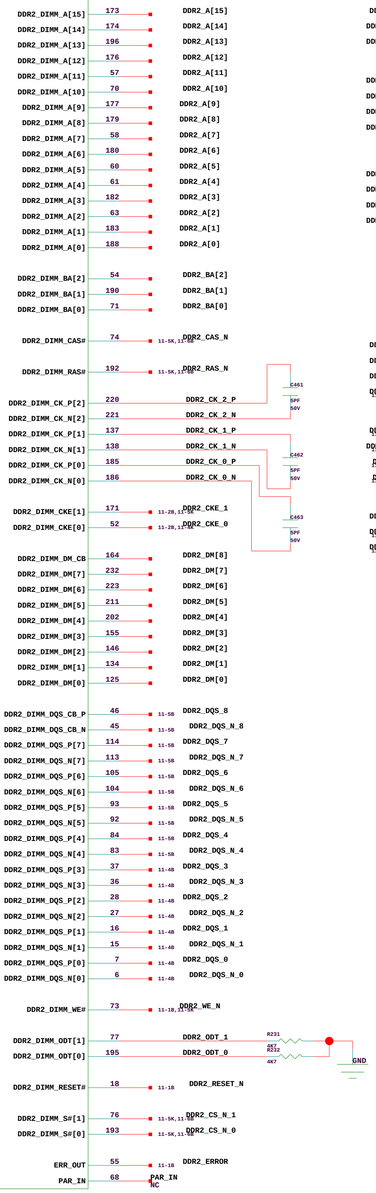


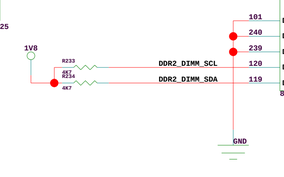




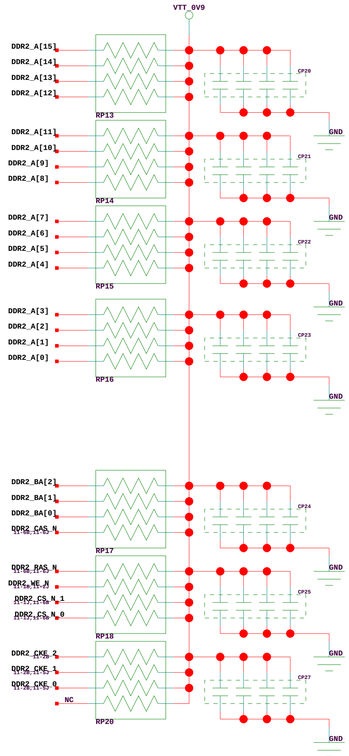


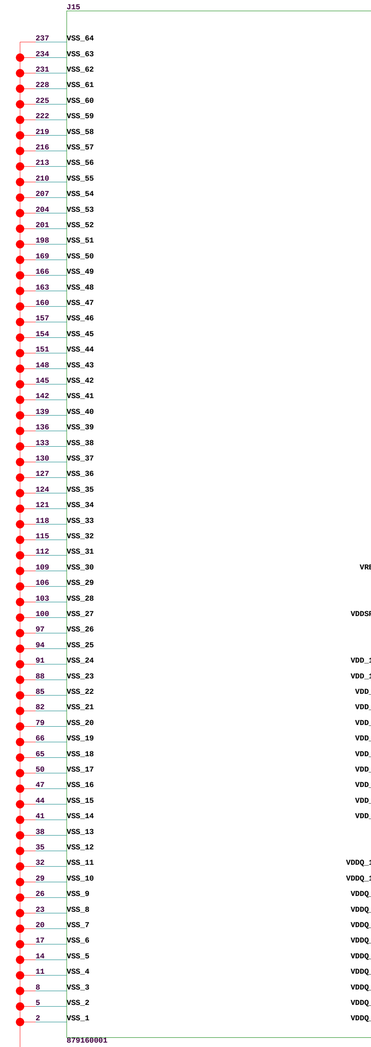




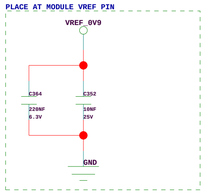


VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

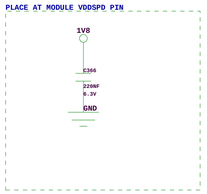




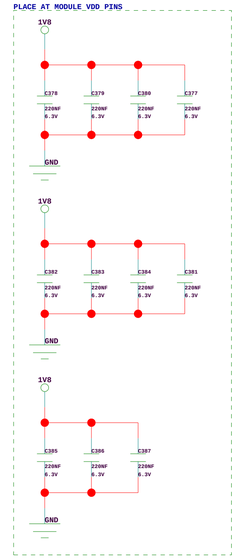
PLACE AT MODULE VREF PIN



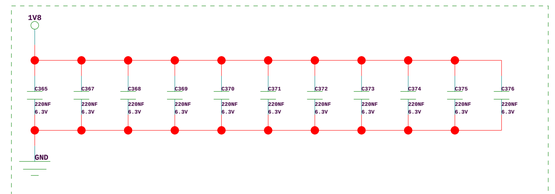
PLACE AT MODULE VDDSPD PIN



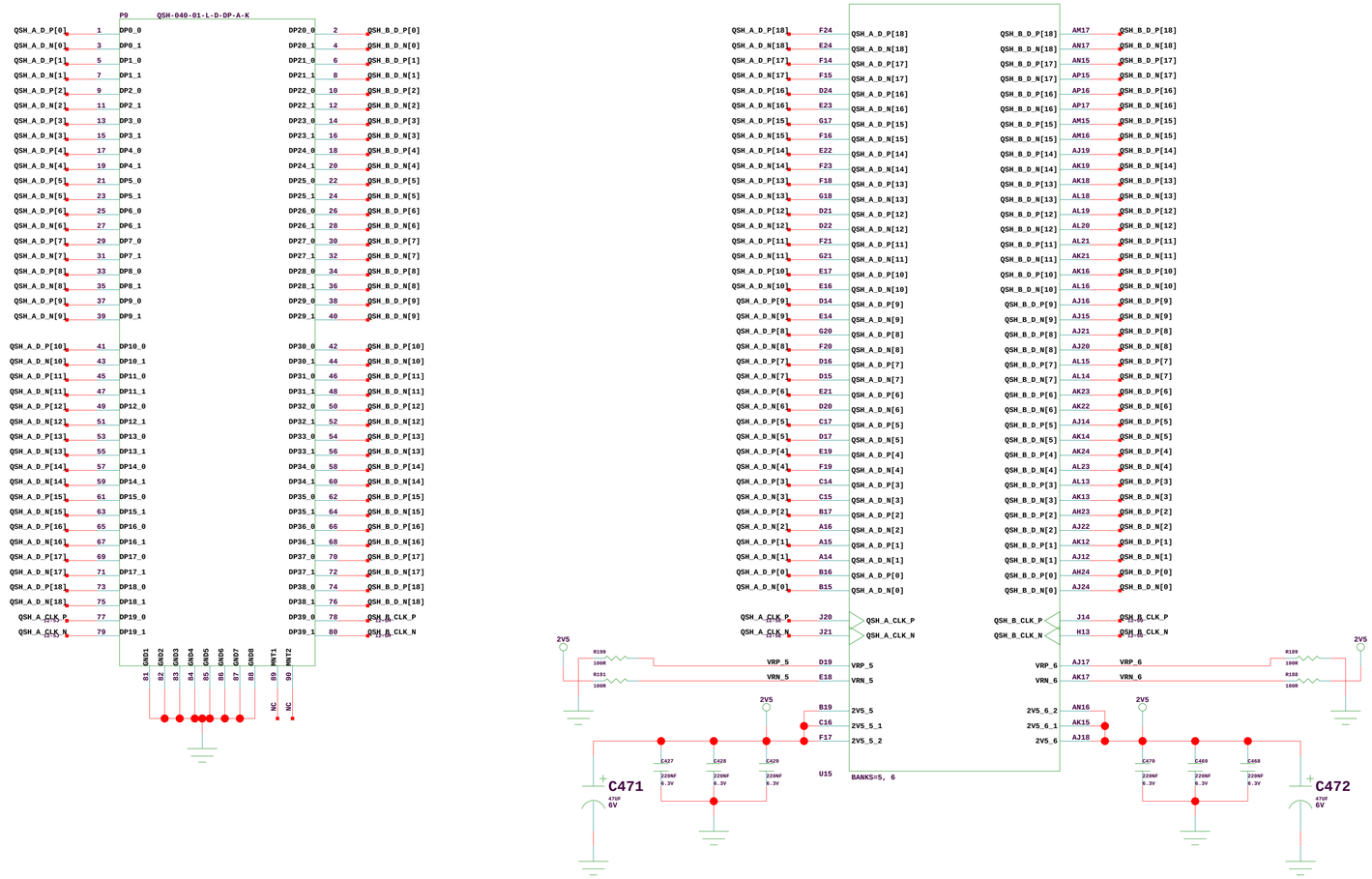
PLACE AT MODULE VDD PINS



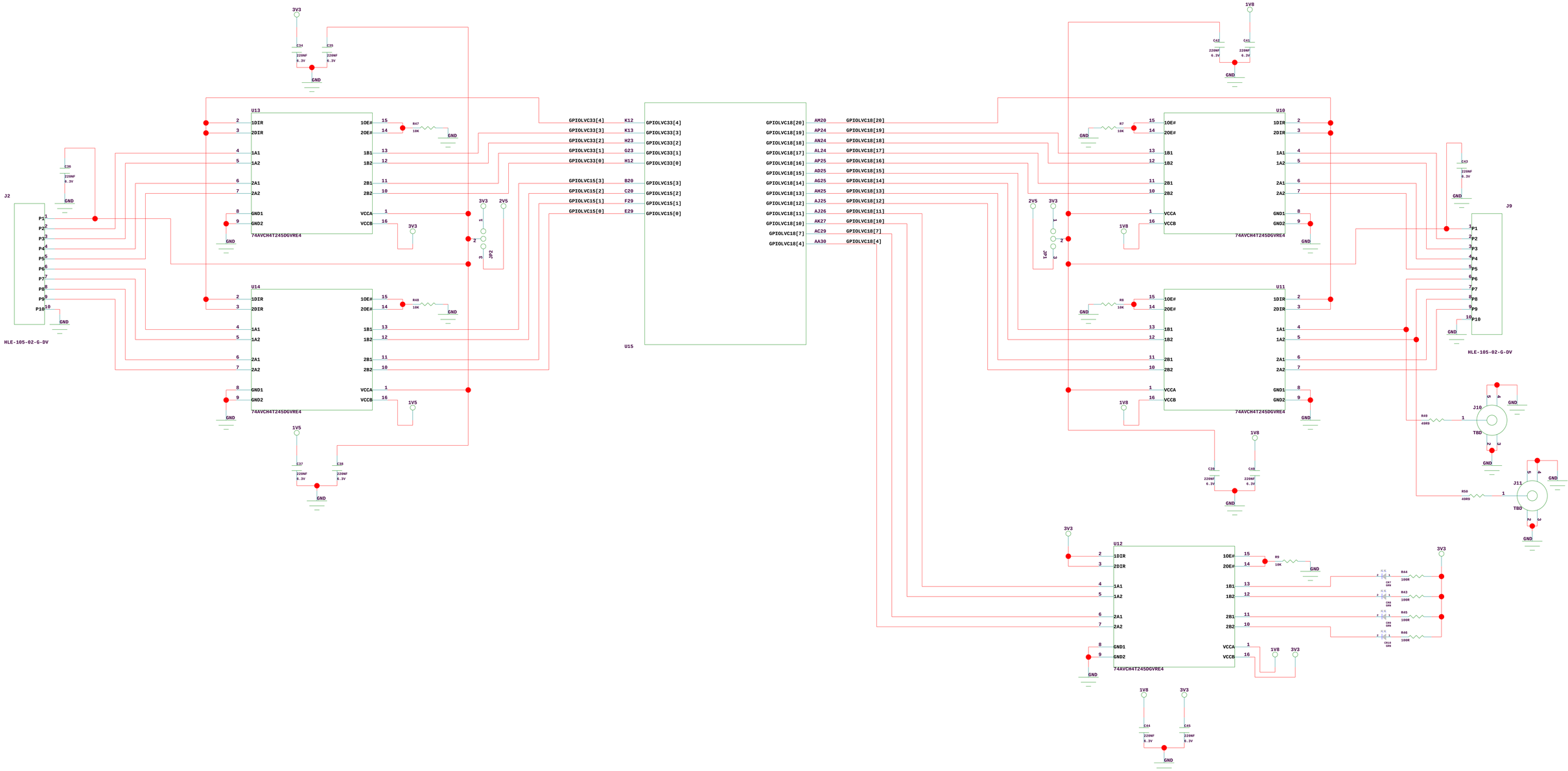
PLACE AT MODULE VDDQ PINS



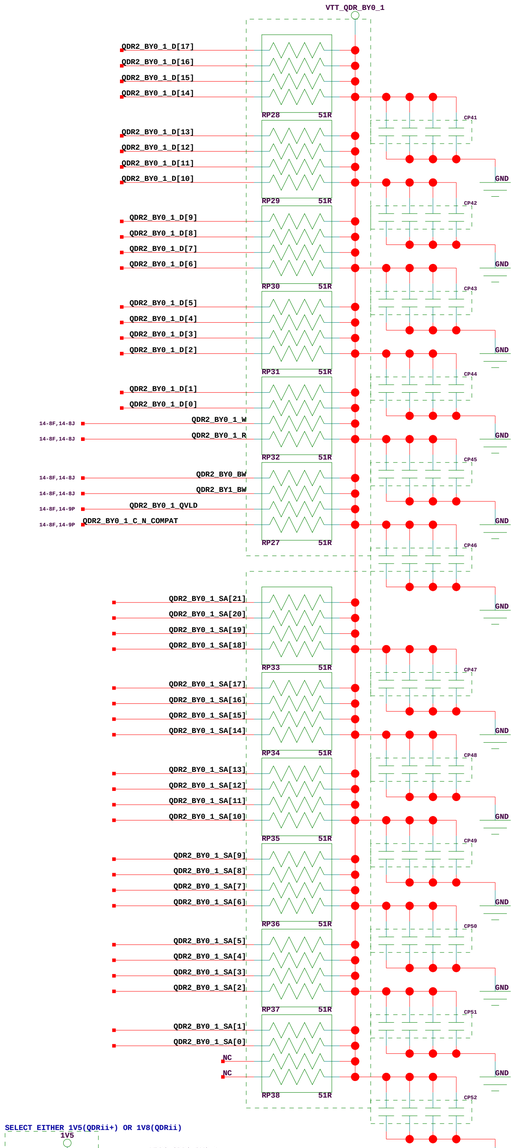
ROACH/iBOB2	**ROACH_DDR2_DIMM**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_15:15 PATH PATH	DRAWN: F KAPP APPR:
	CHECKED: E BAUERMEISTER SHEET 11 OF 25

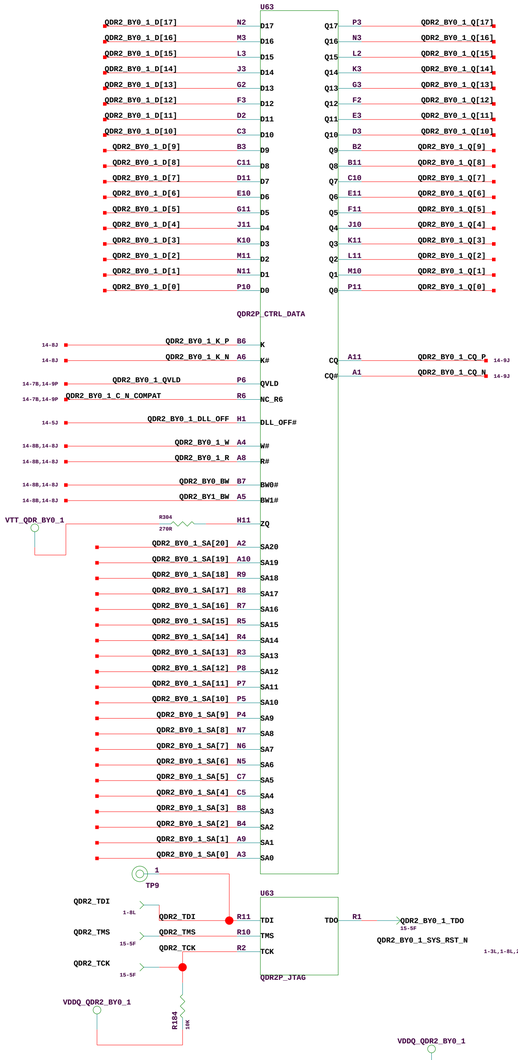


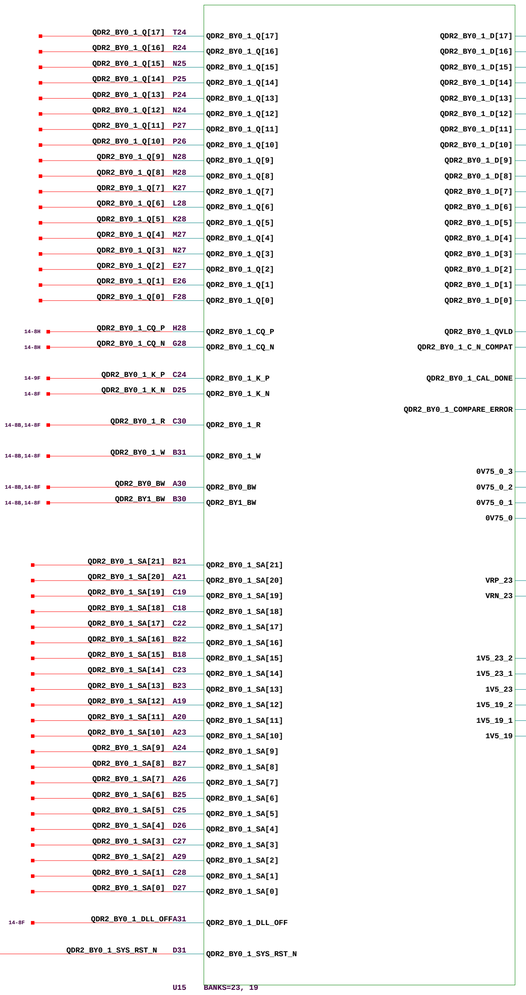
ROACH/iBOB2	**ROACH_DIFF_GPIO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_15:15 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 12 OF 25

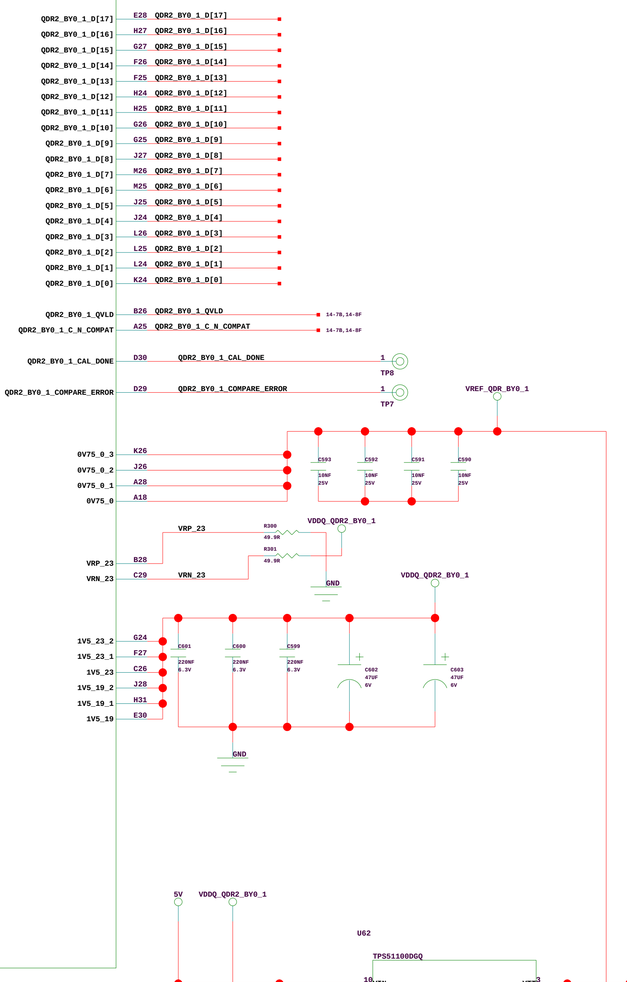


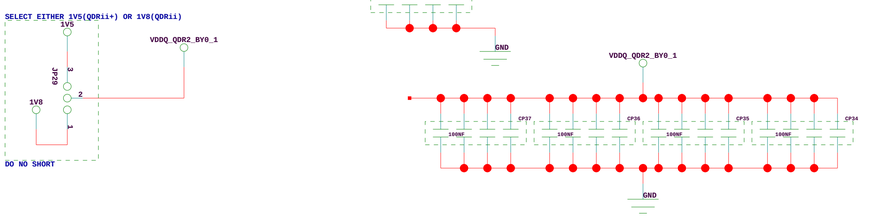
ROACH/iBOB2	**ROACH_GPIO_MISC**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 13 OF 25
10-5-2007_15:15 PATH PATH	

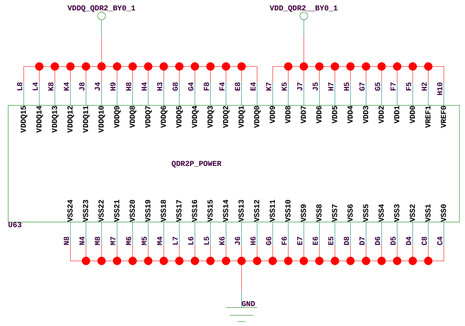


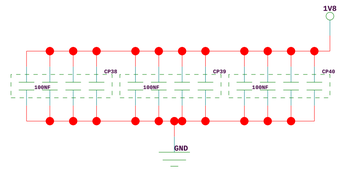


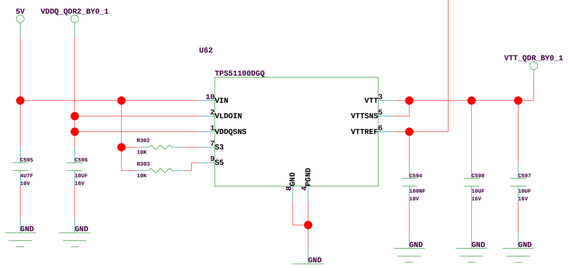




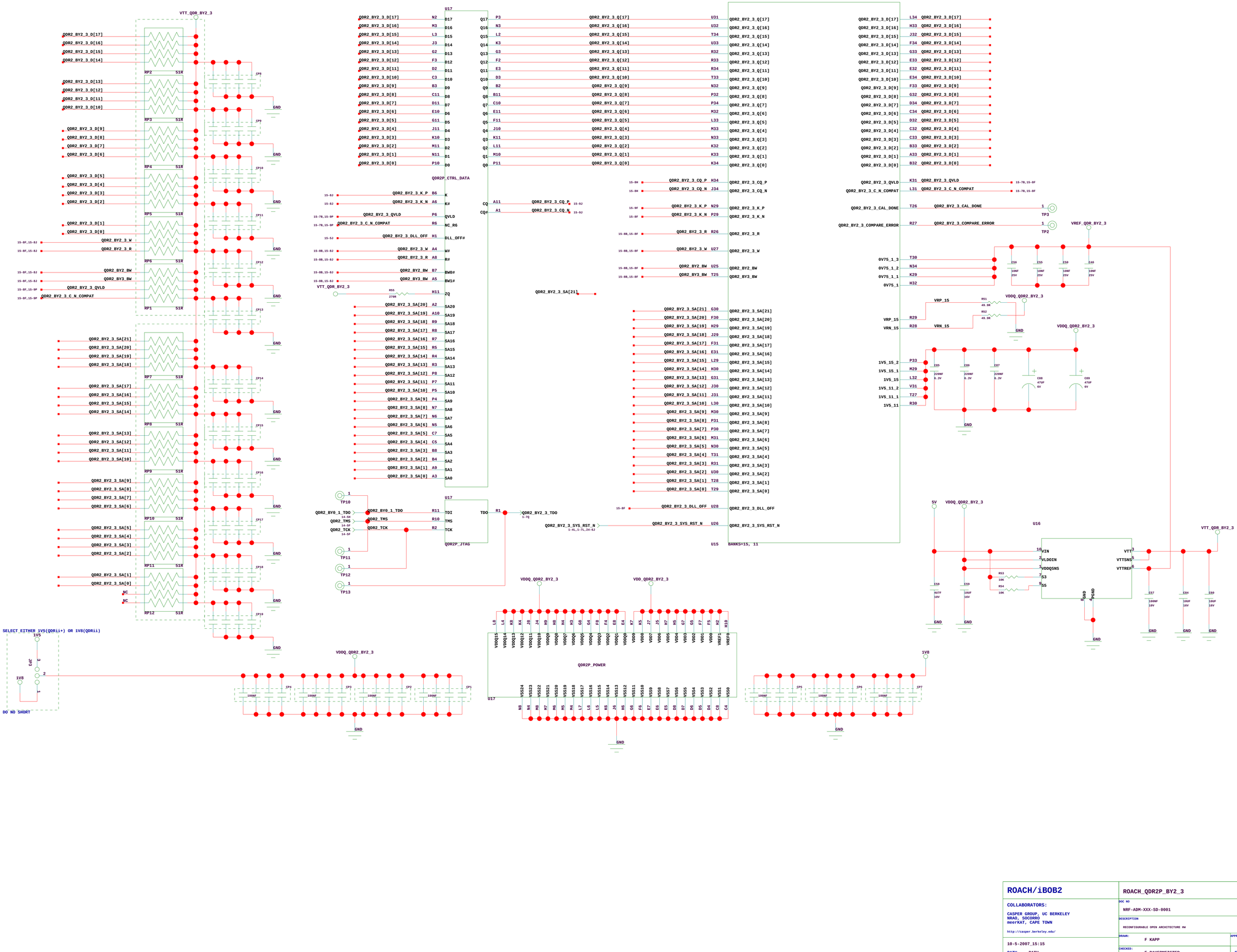








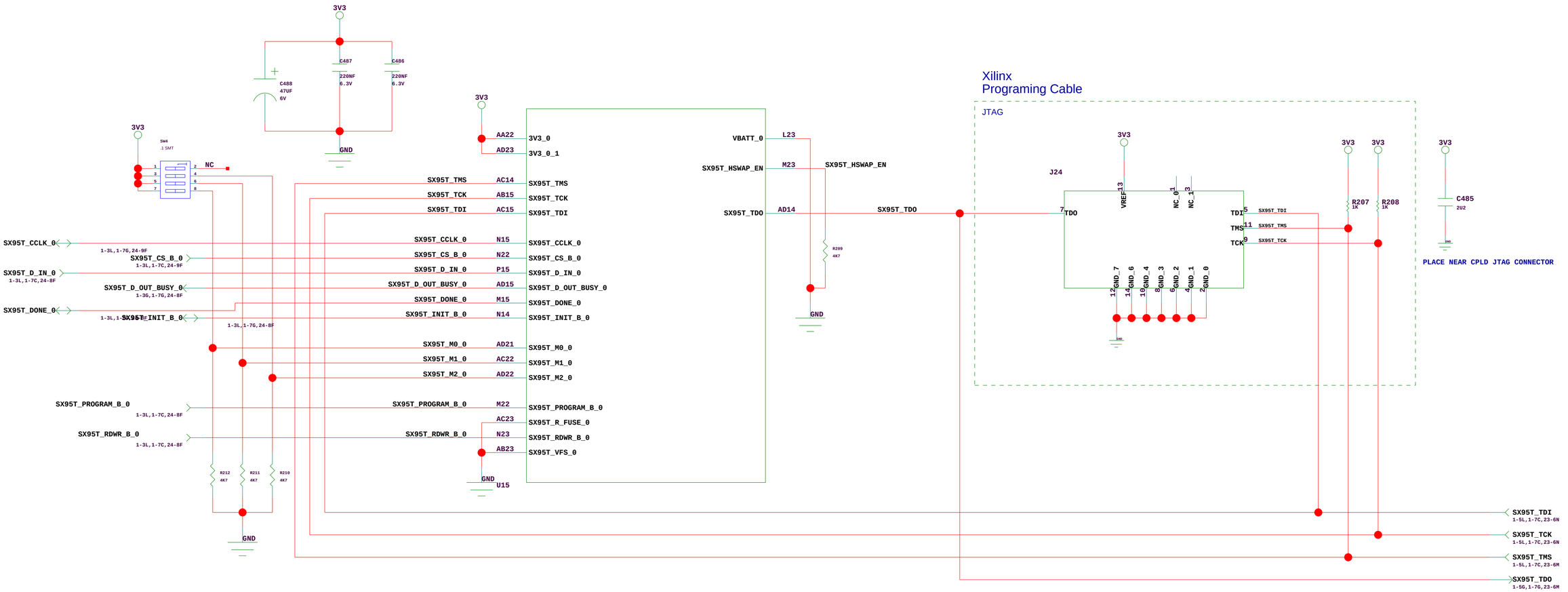
ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 14 OF 25
10-5-2007_15:15 PATH PATH	



ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_15:15	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 15 OF 25

TBD

VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input



ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
10-5-2007_15:15 PATH PATH	

Place components close to CPU

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J3: "1V5"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J4: "1V8"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J5: "2V5"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J6: "3V3"

Place components close to CPU

Place components close to CPU

Place components close to CPU

+5.0 V

Alternate power input terminal
Two 10A fuses result in 16A rating

Bulk Decoupling

CPU Core by-pass caps place as close to CPU Vdd pins as possible

Bulk Decoupling

CPU Core by-pass caps place as close to CPU SOVdd pins as possible

Bulk Decoupling

CPU Core by-pass caps place as close to CPU DVdd pins as possible

+1.8 V

Place all components within this block close together

~2.9Amp

~3.6Amp

Place these 4 caps close to DDR parts

VOUT= 0.6v(1+R1/R2)

PWR_GOOD

1-4D,1-4G,1-5E,1-5G,18-2F,23-19G,24-8K

+1.5 V

VOUT= 0.6v(1+R1/R2)
PLLLPF = VIN = 750khz

Each Analog GND tied to Digital GND at a single point.

Place all components within this block close together

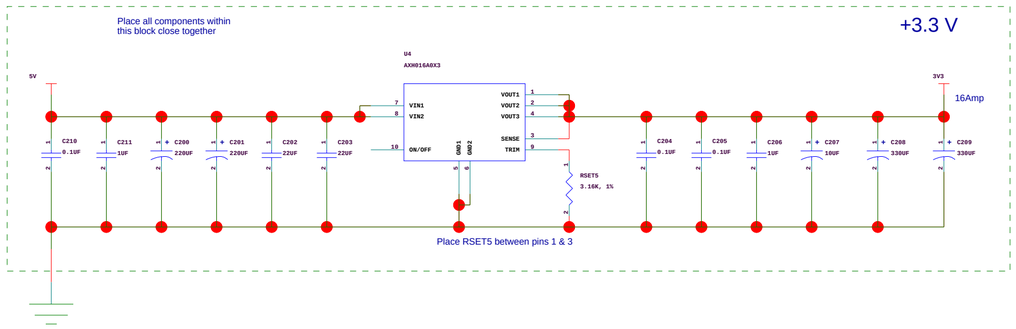
+0.9 V

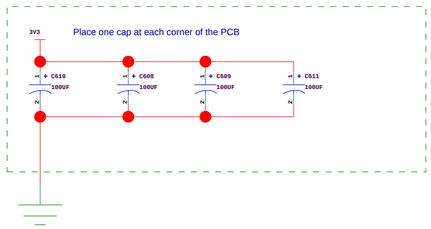
Use 25mil trace

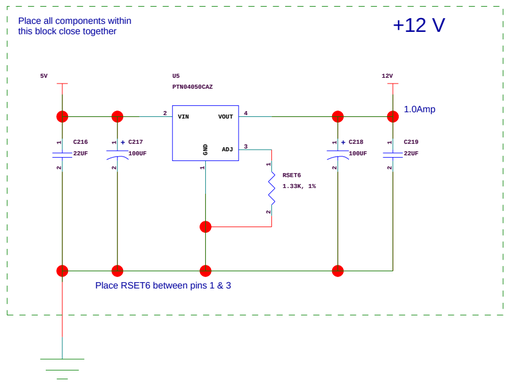
VTT_+0.9V
1-5E

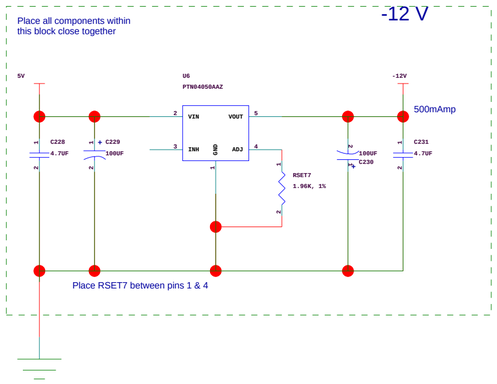
VTT island by-pass caps place evenly across VTT island
(1 cap for every 2 signals terminated)
(1 Tantalum Cap on each end of island)
VTT regulator placed at center of VTT island

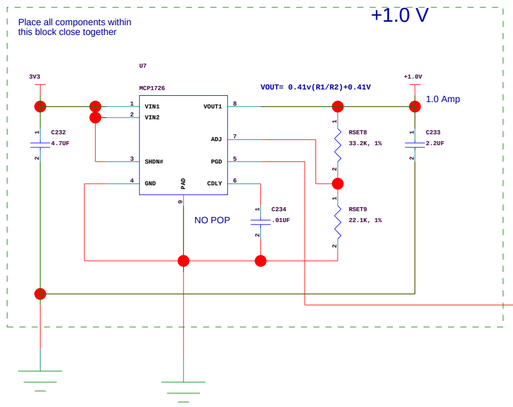
ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_15:15	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 17 OF 25

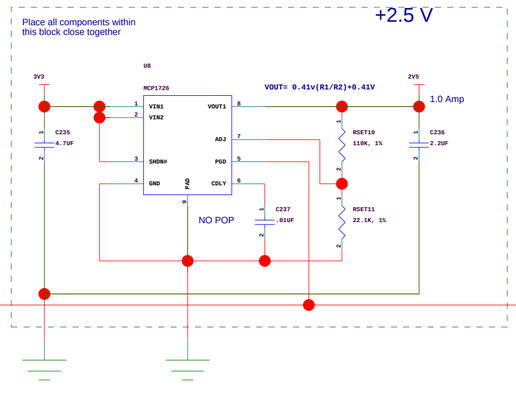


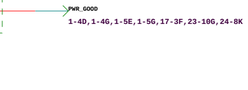




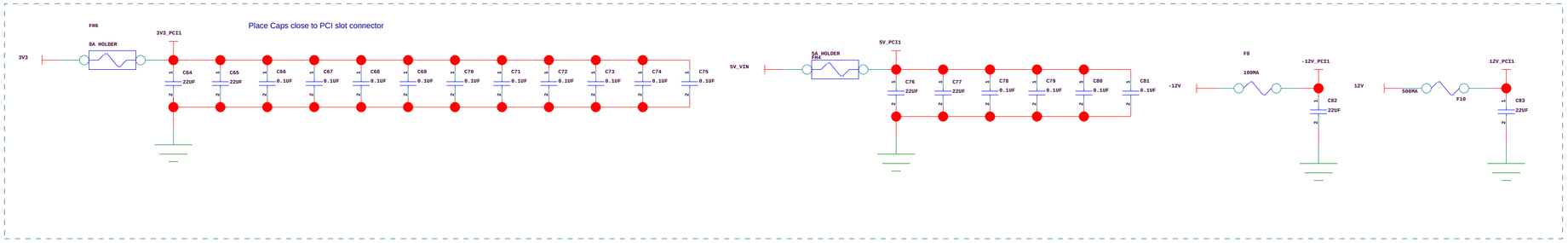


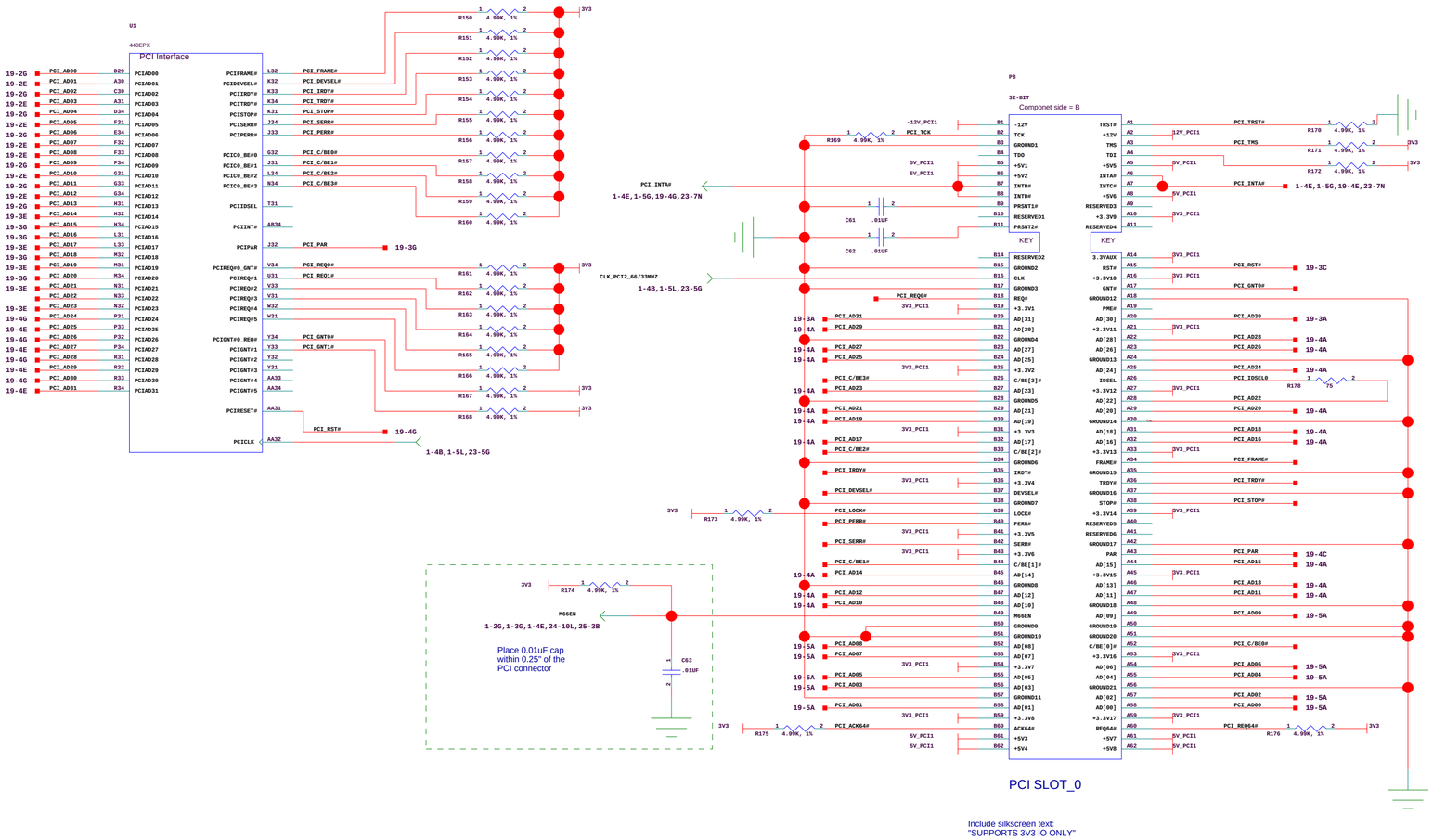






ROACH/iBOB2	**ROACH_PPC_POWER_2**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 18 OF 25
10-5-2007_15:15 PATH PATH	





PCI SLOT_0

Include silkscreen text:
"SUPPORTS 3V3 IO ONLY"

Optional PRSNT signals are not used, max 25W is available

PRSNT1#	PRSNT2#	Expansion Configuration
Open	Open	No expansion board present
Ground	Open	Expansion board present, 25 W maximum
Open	Ground	Expansion board present, 15 W maximum
Ground	Ground	Expansion board present, 7.5 W maximum

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

10-5-2007_15:15

PATH PATH

ROACH_PPC_PCI

DOC NO	REVISION
NRF-ADM-XXX-SD-0001	A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN:	APPR:
F KAPP	
CHECKED: E BAUERMEISTER	SHEET 19 OF 25

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups. Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

Place nearest PHY pin 96

Place nearest PHY pin 101

Place nearest PHY pin 98

Place nearest PHY pin 100

Place as close to PHY CORE VDD power pins as possible

Place as close to PHY IO VDD power pins as possible

UNUSED SECOND ETHERNET MAC

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place jumpers in line with signals

Place decoupling C close to termination R All traces 50Ohm WRT GND or 2V5

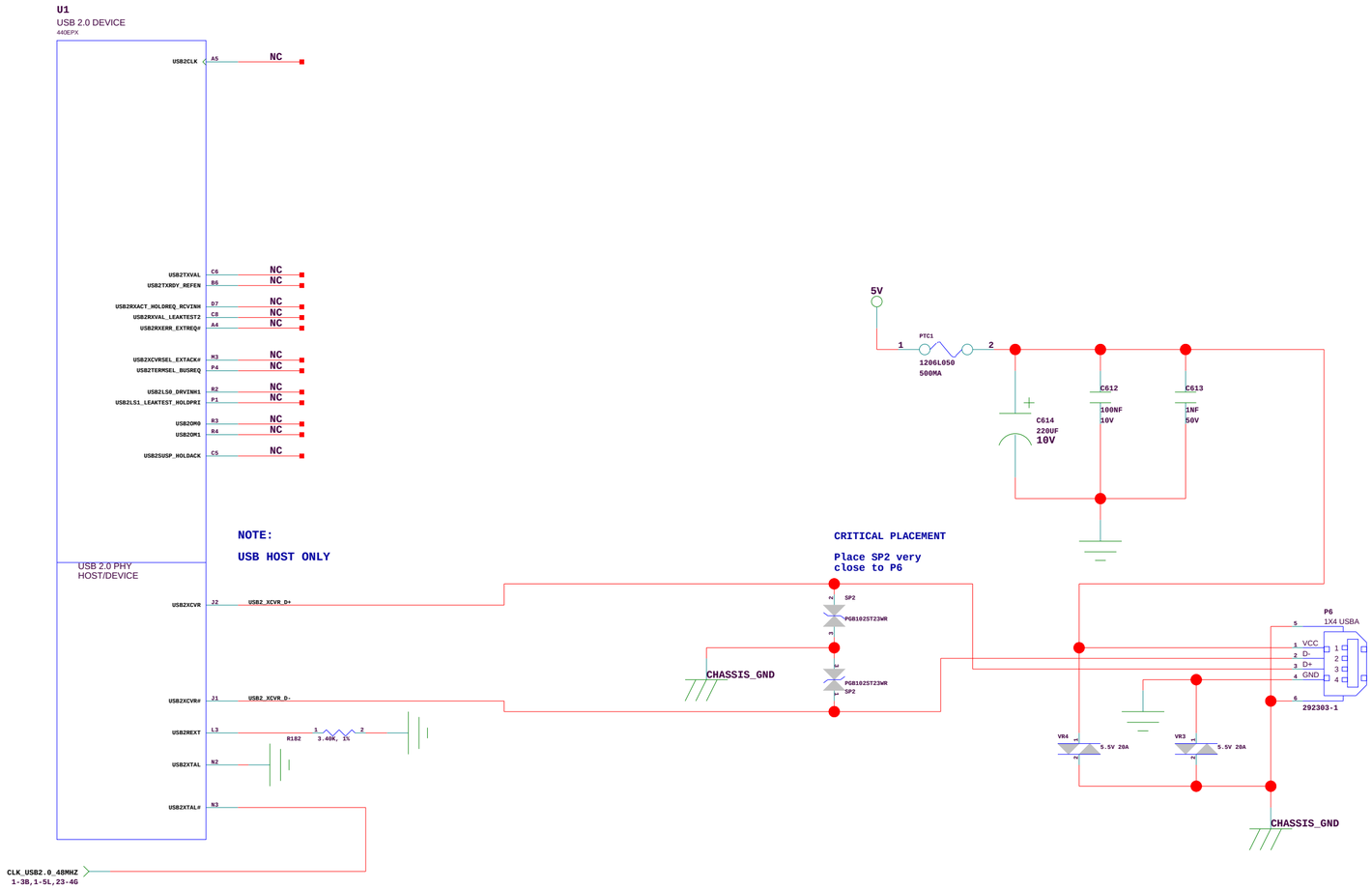
Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

ROACH/iBOB2	ROACH_PPC_ETH1
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_15:15	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 20 OF 25



ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25
10-5-2007_15:15 PATH PATH	

DDR_PA[15:0]

DDR_PD0[63:0]

U1

DDR SDRAM

64DEPX

DDR_PD0	AB2	MEMDATA00	MEMADDR00
DDR_PD1	AF2	MEMDATA01	MEMADDR01
DDR_PD2	AK5	MEMDATA02	MEMADDR02
DDR_PD3	AL28	MEMDATA03	MEMADDR03
DDR_PD4	AL22	MEMDATA04	MEMADDR04
DDR_PD5	AK2	MEMDATA05	MEMADDR05
DDR_PD6	AK1	MEMDATA06	MEMADDR06
DDR_PD7	AP21	MEMDATA07	MEMADDR07
DDR_PD8	AP28	MEMDATA08	MEMADDR08
DDR_PD9	AL18	MEMDATA09	MEMADDR09
DDR_PD10	AK17	MEMDATA10	MEMADDR10
DDR_PD11	AF17	MEMDATA11	MEMADDR11
DDR_PD12	AK26	MEMDATA12	MEMADDR12
DDR_PD13	AF18	MEMDATA13	MEMADDR13
DDR_PD14	AK18	MEMDATA14	
DDR_PD15	AF16	MEMDATA15	
DDR_PD16	AK16	MEMDATA16	
DDR_PD17	AF15	MEMDATA17	
DDR_PD18	AL15	MEMDATA18	
DDR_PD19	AF14	MEMDATA19	
DDR_PD20	AL17	MEMDATA20	
DDR_PD21	AK17	MEMDATA21	
DDR_PD22	AK15	MEMDATA22	
DDR_PD23	AK15	MEMDATA23	
DDR_PD24	AF13	MEMDATA24	
DDR_PD25	AK13	MEMDATA25	
DDR_PD26	AF12	MEMDATA26	
DDR_PD27	AL12	MEMDATA27	
DDR_PD28	AK14	MEMDATA28	
DDR_PD29	AK14	MEMDATA29	
DDR_PD30	AL13	MEMDATA30	
DDR_PD31	AK12	MEMDATA31	
DDR_PD32	AF3	MEMDATA32	
DDR_PD33	AF1	MEMDATA33	
DDR_PD34	AD4	MEMDATA34	
DDR_PD35	AD3	MEMDATA35	
DDR_PD36	AB3	MEMDATA36	
DDR_PD37	AF2	MEMDATA37	
DDR_PD38	AE2	MEMDATA38	
DDR_PD39	AE1	MEMDATA39	
DDR_PD40	AC3	MEMDATA40	
DDR_PD41	AC1	MEMDATA41	
DDR_PD42	AA4	MEMDATA42	
DDR_PD43	AA3	MEMDATA43	
DDR_PD44	AD2	MEMDATA44	
DDR_PD45	AC4	MEMDATA45	
DDR_PD46	AB1	MEMDATA46	
DDR_PD47	AB2	MEMDATA47	
DDR_PD48	Y3	MEMDATA48	
DDR_PD49	Y2	MEMDATA49	
DDR_PD50	Y4	MEMDATA50	
DDR_PD51	V3	MEMDATA51	
DDR_PD52	AA2	MEMDATA52	
DDR_PD53	AA1	MEMDATA53	
DDR_PD54	W3	MEMDATA54	
DDR_PD55	W1	MEMDATA55	
DDR_PD56	V1	MEMDATA56	
DDR_PD57	U2	MEMDATA57	
DDR_PD58	T4	MEMDATA58	
DDR_PD59	R1	MEMDATA59	
DDR_PD60	V3	MEMDATA60	
DDR_PD61	V1	MEMDATA61	
DDR_PD62	T3	MEMDATA62	
DDR_PD63	T1	MEMDATA63	

DDR_PA0	AM5	MEMADDR00	
DDR_PA1	AP4	MEMADDR01	
DDR_PA2	AP5	MEMADDR02	
DDR_PA3	AM6	MEMADDR03	
DDR_PA4	AP6	MEMADDR04	
DDR_PA5	AM8	MEMADDR05	
DDR_PA6	AL7	MEMADDR06	
DDR_PA7	AN7	MEMADDR07	
DDR_PA8	AN8	MEMADDR08	
DDR_PA9	AP7	MEMADDR09	
DDR_PA10	AL2	MEMADDR10	
DDR_PA11	AL8	MEMADDR11	
DDR_PA12	AN3	MEMADDR12	
DDR_PA13	AN4	MEMADDR13	
DDR_PBA0	AJ1	BA0	
DDR_PBA1	AN3	BA1	
DDR_PBA2	AP8	BA2	
DDR_PRAS#	AJ4	RAS#	
DDR_PCAS#	AN4	CAS#	
DDR_PWE#	AJ2	WE#	
DDR_PDM0	AL21	DM0	
DDR_PDM1	AP18	DM1	
DDR_PDM2	AP15	DM2	
DDR_PDM3	AL14	DM3	
DDR_PDM4	AD4	DM4	
DDR_PDM5	AB3	DM5	
DDR_PDM6	Y3	DM6	
DDR_PDM7	V3	DM7	
DDR_PDM8	AN18	DM8	
DDR_PDQS0	AM21	DQS0	
DDR_PDQS1	AM19	DQS1	
DDR_PDQS2	AL16	DQS2	
DDR_PDQS3	AM13	DQS3	
DDR_PDQS4	AB3	DQS4	
DDR_PDQS5	AB4	DQS5	
DDR_PDQS6	W3	DQS6	
DDR_PDQS7	Y3	DQS7	
DDR_PDQS8	AP10	DQS8	
DDR_PODT0	AN3	MEMDT0	
DDR_PODT1	AG1	MEMDT1	
DDR_PCS0#	AN2	BANKSELA0	
DDR_PCS1#	AM1	BANKSELA1	
DDR_PCKE	AN9	MEMCKE0	
DDR_CLKOUT	AL1	MEMCLKOUT	
DDR_CLKOUT#	AM1	MEMCLKOUT#	

PPC_ECC9	AM11	ECC8	
PPC_ECC1	AL11	ECC1	
PPC_ECC2	AN9	ECC2	
PPC_ECC3	AL9	ECC3	
PPC_ECC4	AM11	ECC4	
PPC_ECC5	AN11	ECC5	
PPC_ECC6	AM10	ECC6	
PPC_ECC7	AP9	ECC7	

22-9F			
22-9F			
22-9F			
22-10F			
22-10F			
22-10F			
22-10F			
22-10F			

22-8K,22-8L			
22-8K,22-8L			
22-8K,22-8L			
22-7K,22-7L			
22-7L,22-8K			
22-3K,22-7L			
22-5K			
22-6K			
22-6K			
22-6K			
22-6K			
22-6K			
22-6K			
22-4K			
22-4K			
22-4K			
22-4K			
22-5K			
22-5K			
22-5K			
22-7L			
22-6L			
22-3K,22-7L			
22-3K,22-7L			
22-6K,22-7L			

DDR_CLKOUT

DDR_CLKOUT#

R813

500ps Loop

DDR_VREF_0V9

VR

C158 0.10F

C148 0.10F

C151 0.10F 0402

C152 0.10F 0402

C148 0.01UF

Place parts as close to CPU as possible

U32

5V

1V8

DDR_VTT

DDR_VREF_0V9

VIN

VLDOIN

VDDQSNS

S3

S5

VTT

VTTSNS

VTTREF

GND

PGND

R230 10K

R229 10K

C459 .01UF 10V

C456 .10UF 16V

C453 .100NF 10V

C457 .10UF 16V

C458 .10UF 16V

J8

879160001

PPC_ECC7	22-6D	168	DDR2_DIMM_CB7
PPC_ECC6	22-6D	167	DDR2_DIMM_CB6
PPC_ECC5	22-7D	162	DDR2_DIMM_CB5
PPC_ECC4	22-7D	161	DDR2_DIMM_CB4
PPC_ECC3	22-7D	49	DDR2_DIMM_CB3
PPC_ECC2	22-7D	48	DDR2_DIMM_CB2
PPC_ECC1	22-7D	43	DDR2_DIMM_CB1
PPC_ECC0	22-7D	42	DDR2_DIMM_CB0
DDR_PDQ63		236	DDR2_DIMM_DQ[63]
DDR_PDQ62		235	DDR2_DIMM_DQ[62]
DDR_PDQ61		230	DDR2_DIMM_DQ[61]
DDR_PDQ60		229	DDR2_DIMM_DQ[60]
DDR_PDQ59		117	DDR2_DIMM_DQ[59]
DDR_PDQ58		116	DDR2_DIMM_DQ[58]
DDR_PDQ57		111	DDR2_DIMM_DQ[57]
DDR_PDQ56		110	DDR2_DIMM_DQ[56]
DDR_PDQ55		227	DDR2_DIMM_DQ[55]
DDR_PDQ54		226	DDR2_DIMM_DQ[54]
DDR_PDQ53		218	DDR2_DIMM_DQ[53]
DDR_PDQ52		217	DDR2_DIMM_DQ[52]
DDR_PDQ51		108	DDR2_DIMM_DQ[51]
DDR_PDQ50		107	DDR2_DIMM_DQ[50]
DDR_PDQ49		99	DDR2_DIMM_DQ[49]
DDR_PDQ48		98	DDR2_DIMM_DQ[48]
DDR_PDQ47		215	DDR2_DIMM_DQ[47]
DDR_PDQ46		214	DDR2_DIMM_DQ[46]
DDR_PDQ45		209	DDR2_DIMM_DQ[45]
DDR_PDQ44		208	DDR2_DIMM_DQ[44]
DDR_PDQ43		96	DDR2_DIMM_DQ[43]
DDR_PDQ42		95	DDR2_DIMM_DQ[42]
DDR_PDQ41		90	DDR2_DIMM_DQ[41]
DDR_PDQ40		89	DDR2_DIMM_DQ[40]
DDR_PDQ39		206	DDR2_DIMM_DQ[39]
DDR_PDQ38		205	DDR2_DIMM_DQ[38]
DDR_PDQ37		200	DDR2_DIMM_DQ[37]
DDR_PDQ36		199	DDR2_DIMM_DQ[36]
DDR_PDQ35		87	DDR2_DIMM_DQ[35]
DDR_PDQ34		86	DDR2_DIMM_DQ[34]
DDR_PDQ33		81	DDR2_DIMM_DQ[33]
DDR_PDQ32		80	DDR2_DIMM_DQ[32]
DDR_PDQ31		159	DDR2_DIMM_DQ[31]
DDR_PDQ30		158	DDR2_DIMM_DQ[30]
DDR_PDQ29		153	DDR2_DIMM_DQ[29]
DDR_PDQ28		152	DDR2_DIMM_DQ[28]
DDR_PDQ27		40	DDR2_DIMM_DQ[27]
DDR_PDQ26		39	DDR2_DIMM_DQ[26]
DDR_PDQ25		34	DDR2_DIMM_DQ[25]
DDR_PDQ24		33	DDR2_DIMM_DQ[24]
DDR_PDQ23		150	DDR2_DIMM_DQ[23]
DDR_PDQ22		149	DDR2_DIMM_DQ[22]
DDR_PDQ21		144	DDR2_DIMM_DQ[21]
DDR_PDQ20		143	DDR2_DIMM_DQ[20]
DDR_PDQ19		31	DDR2_DIMM_DQ[19]
DDR_PDQ18		30	DDR2_DIMM_DQ[18]
DDR_PDQ17		25	DDR2_DIMM_DQ[17]
DDR_PDQ16		24	DDR2_DIMM_DQ[16]
DDR_PDQ15		141	DDR2_DIMM_DQ[15]
DDR_PDQ14		140	DDR2_DIMM_DQ[14]
DDR_PDQ13		132	DDR2_DIMM_DQ[13]
DDR_PDQ12		131	DDR2_DIMM_DQ[12]
DDR_PDQ11		22	DDR2_DIMM_DQ[11]
DDR_PDQ10		21	DDR2_DIMM_DQ[10]
DDR_PDQ9		13	DDR2_DIMM_DQ[9]
DDR_PDQ8		12	DDR2_DIMM_DQ[8]
DDR_PDQ7		129	DDR2_DIMM_DQ[7]
DDR_PDQ6		128	DDR2_DIMM_DQ[6]
DDR_PDQ5		123	DDR2_DIMM_DQ[5]
DDR_PDQ4		122	DDR2_DIMM_DQ[4]
DDR_PDQ3		10	DDR2_DIMM_DQ[3]
DDR_PDQ2		9	DDR2_DIMM_DQ[2]
DDR_PDQ1		4	DDR2_DIMM_DQ[1]
DDR_PDQ0		3	DDR2_DIMM_DQ[0]
		101	DDR2_DIMM_SA2
		240	DDR2_DIMM_SA1
		239	DDR2_DIMM_SA0
		120	DDR2_DIMM_SCL
		119	DDR2_DIMM_SDA

1V8

R228 4K7

R227 4K7

PPC_DDR2_DIMM_SCL

PPC_DDR2_DIMM_SDA

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA1	22-8L,22-9D
DDR2_DIMM_BA[1]	190	DDR_PBA2	22-8L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-8L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	NC	
DDR2_DIMM_CK_N[2]	221	NC	
DDR2_DIMM_CK_P[1]	137	NC	
DDR2_DIMM_CK_N[1]	138	NC	
DDR2_DIMM_CK_P[0]	185	DDR_CLKOUT	
DDR2_DIMM_CK_N[0]	186	DDR_CLKOUT#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-7L,22-8D
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-9D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D
ERR_OUT	55	PPC_DDR2_ERROR	
PAR_IN	68	PAR_IN	

C455 .5PF 50V

R226 4K7

PPC_DDR2_RESET_N

1-3B,1-4L,24-5J

TP4

TP5

DDR_VTT

RP24 RP23 RP22 RP21

DDR_PA15 DDR_PA14 DDR_PA13 DDR_PA12

DDR_PA11 DDR_PA10 DDR_PA9 DDR_PA8

DDR_PA7 DDR_PA6 DDR_PA5 DDR_PA4

DDR_PA3 DDR_PA2 DDR_PA1 DDR_PA0

CP26 CP28 CP29 CP30

GND

RP25 RP26 RP19

22-8K,22-9D DDR_PBA1

22-8K,22-9D DDR_PBA2

22-8K,22-9D DDR_PBA0

22-8K,22-9D DDR_PCAS#

22-7K,22-9D DDR_PRAS#

22-6K,22-8D DDR_PCKE

22-3K,22-9D DDR_PWE#

22-3K,22-8D DDR_PCS0#

22-3K,22-8D DDR_PCS1#

22-8D DDR_PODT0

22-8D DDR_PODT1

NC

CP32 CP31 CP33

J8

879160001

VSS_64	237		
VSS_63	234		
VSS_62	231		
VSS_61	228		
VSS_60	225		
VSS_59	222		
VSS_58	219		
VSS_57	216		
VSS_56	213		
VSS_55	210		
VSS_54	207		
VSS_53	204		
VSS_52	201		
VSS_51	198		
VSS_50	169		
VSS_49	166		
VSS_48	163		
VSS_47	160		
VSS_46	157		
VSS_45	154		
VSS_44	151		
VSS_43	148		
VSS_42	145		
VSS_41	142		
VSS_40	139		
VSS_39	136		
VSS_38	133		
VSS_37	130		
VSS_36	127		
VSS_35	124		
VSS_34	121		
VSS_33	118		
VSS_32	115		
VSS_31	112		
VSS_30	109		
VSS_29	106		
VSS_28	103		
VSS_27	100		
VSS_26	97		
VSS_25	94		
VSS_24	91		
VSS_23	88		
VSS_22	85		
VSS_21	82		
VSS_20	79		
VSS_19	66		
VSS_18	65		
VSS_17	50		
VSS_16	47		
VSS_15	44		
VSS_14	41		
VSS_13	38		
VSS_12	35		
VSS_11	32		
VSS_10	29		
VSS_9	26		
VSS_8	23		
VSS_7	20		
VSS_6	17		
VSS_5	14		
VSS_4	11		
VSS_3	8		
VSS_2	5		
VSS_1	2		
		1	VREF
		238	VDDSPD
		197	VDD_11
		189	VDD_10
		187	VDD_9
		184	VDD_8
		178	VDD_7
		172	VDD_6
		69	VDD_5
		67	VDD_4
		64	VDD_3
		59	VDD_2
		53	VDD_1
		194	VDDQ_11
		191	VDDQ_10
		181	VDDQ_9
		175	VDDQ_8
		170	VDDQ_7
		78	VDDQ_6
		75	VDDQ_5
		72	VDDQ_4
		62	VDDQ_3
		56	VDDQ_2
		51	VDDQ_1

DDR_VREF_0V9

1V8

C432 C433 C454 C434 C430 C443 C431 C444 C436 C445 C435 C446 .100NF 10V .10NF 25V

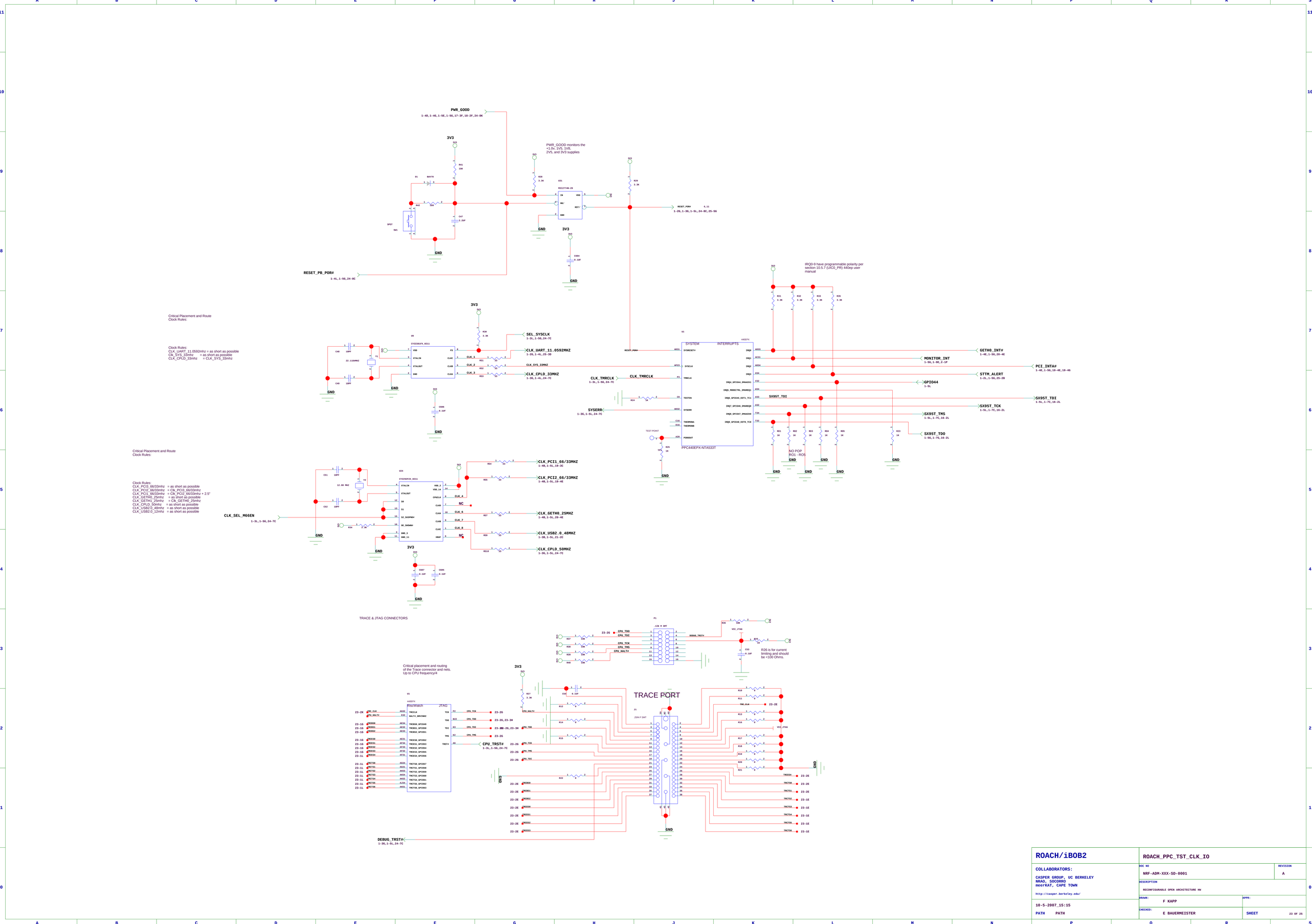
C438 C451 C437 C452 C439 C449 C440 C450 C441 C448 C442 C447 .100NF 10V .10NF 25V

GND

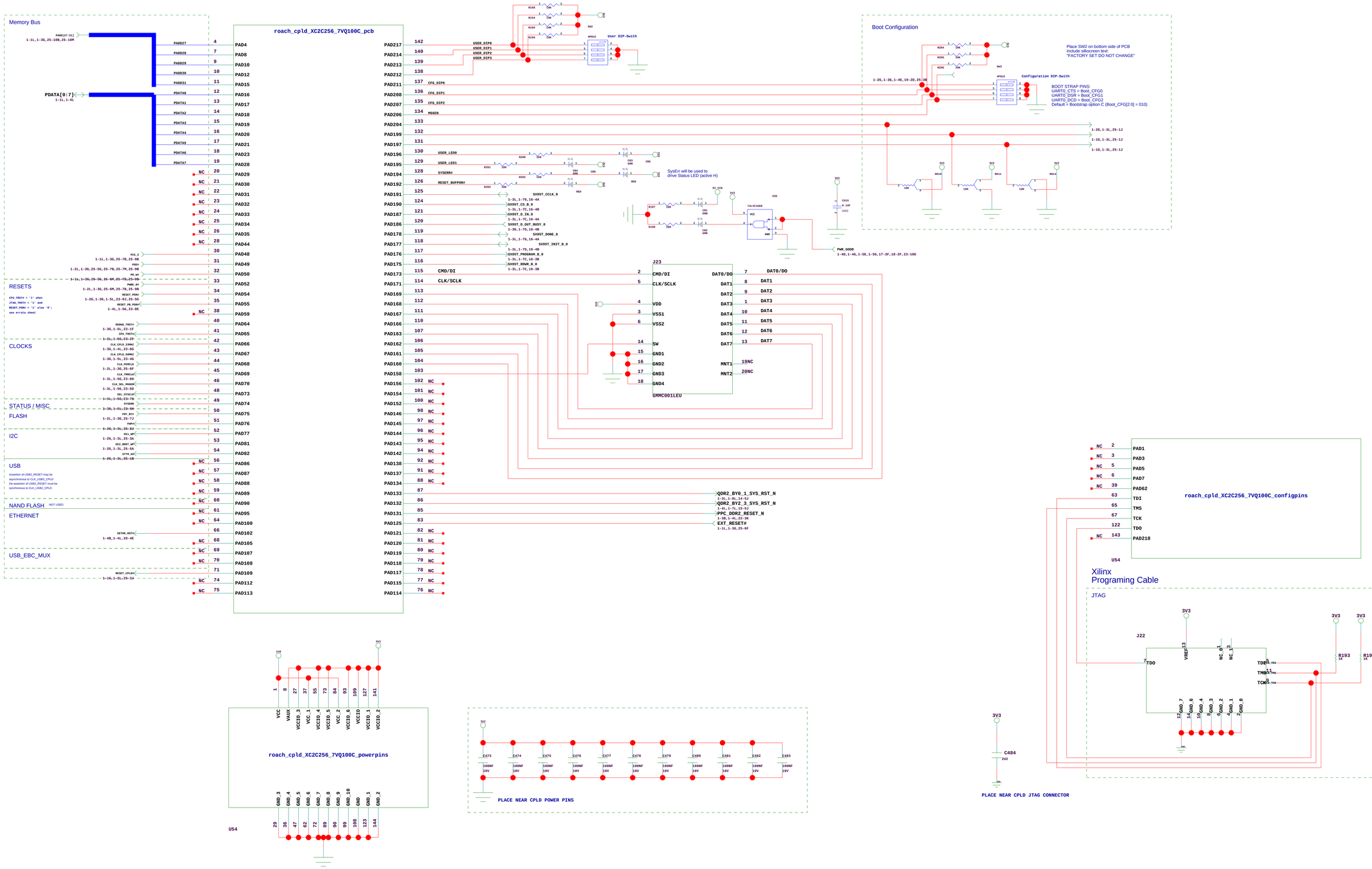
PLACE NEAREST DDR2 MODULE PINS

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

ROACH/iBOB2	ROACH_PPC_DDR2
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_15:15	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 22 OF 25



ROACH/iBOB2	**ROACH_PPC_TST_CLK_IO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_15:15 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 23 OF 25



ROACH/iBOB2	**ROACH_PPC_CPLD**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_15:15 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 24 OF 25

PDATA[0:31]
1-1i,1-4L

1-PADDE2cG2i,25-10B
1-1i,1-3G,24-10B,25-10B,25-10M

PADD[2:31]

3V3

PCS_0 — 25-5G,25-8C
PCS_1 — 25-7C,25-7M
PCS_2 — 1-1i,1-3G,24-8C,25-7B
PCS_4_GPIO09 — 25-7C
PCS_5_GPIO010 — 25-7C
POE# — 1-21,1-3G,24-8C,25-5G,25-7M,25-9B
PR_W# — 1-1i,1-3G,24-8C,25-5G,25-6M,25-9B
PWBE_0# — 1-21,1-3G,24-8C,25-6M,25-9B
PWBE_1# — 25-6M,25-7C
PWBE_2# — 25-7C
PWBE_3# — 25-7C
PREADY — 25-7C,25-8Q
PBLASTF — 25-6M,25-7C

U1 External Slave Peripheral
AXEEPX

NC ×32
PERDATA31 PERDATA30 PERDATA29 PERDATA28 PERDATA27 PERDATA26 PERDATA25 PERDATA24 PERDATA23 PERDATA22 PERDATA21 PERDATA20 PERDATA19 PERDATA18 PERDATA17 PERDATA16
PERDATA15 PERDATA14 PERDATA13 PERDATA12 PERDATA11 PERDATA10 PERDATA9 PERDATA8 PERDATA7 PERDATA6 PERDATA5 PERDATA4 PERDATA3 PERDATA2 PERDATA1 PERDATA0

PERADDR31 PERADDR30 PERADDR29 PERADDR28 PERADDR27 PERADDR26 PERADDR25 PERADDR24 PERADDR23 PERADDR22 PERADDR21 PERADDR20 PERADDR19 PERADDR18 PERADDR17 PERADDR16 PERADDR15 PERADDR14 PERADDR13 PERADDR12 PERADDR11 PERADDR10 PERADDR9 PERADDR8 PERADDR7 PERADDR6 PERADDR5 PERADDR4 PERADDR3 PERADDR2
PERADDR7_GPIO08_DMAREQ3 PERADDR6_GPIO01_DMAACK3 PERADDR5_GPIO02_EOT2_TC2 GPIO03_PERADDR04_DMAREQ2 GPIO04_PERADDR03_DMAACK2 GPIO05_PERADDR02_EOT1_TC1

25-5G,25-10B PCS_0 — PERCS0#
25-7M,25-10B PCS_1 — PERCS1#_GPIO06
PCS_2 — PERCS2#
25-9B PCS_4_GPIO09 — PERCS4#_GPIO09
25-9B PCS_5_GPIO010 — PERCS5#_GPIO10
POE# — PEROE#
PR_W# — PERWR_WF
PWBE_0# PERBE0# — PWBE_1# PERBE1# — PWBE_2# PERBE2# — PWBE_3# PERBE3#
PREADY — PEREADY
PBLASTF — PERBLAST#

EXTRESET2 — EXTRESET#
PERCLK — CLK_PERCLK
PERERR_GPIO11 — PERERR

External Master Peripheral Interface

25-8Q — PERACK#
NO POP
R85 1K
J7 6 PIN 0.1" SMT

EXT_RESET# — EXT_RESET# 1-1i,1-3G,24-5J
CLK_PERCLK — CLK_PERCLK 1-21,1-3G,24-7C

R84 1K
R83 1K
R86 4.99K, 1%
R87 4.99K, 1%
R88 4.99K, 1%

U42 FLASH 32Mx16 45AN8
3V3 — R89 3.3K — FWP0 1-20,1-3L,24-6C
PADD[2:31] — A0–A25
WP#/ACC — R84
DQ0–DQ15 — PDATA15–PDATA0
BY/RY# — R81 3.3K — RY_BY# 1-21,1-3G,24-6C
BYTE# — R82 3.3K — RESET_CPLD# 1-1G,1-3L,24-5C
CE# OE# WE# RESET# — VCC VIO VSS
C654 0.1UF 0402 — C656 0.1UF 0402 — C659 0.1UF 0402

U41 ADT7414-R
VDD ALERT GND — SCL SDA A0
I2C0_SCLK — I2C0_SCLK 1-21,1-9B,2-2P
I2C0_33_DATA — I2C0_33_DATA 1-2L,1-9E
STTM_ALERT 1-21,1-9G,23-6N
STTM_A5 1-20,1-3L,24-6C

P11 0.12A H SMT
P4 0.12A H SMT
R73 3.3K — R74 3.3K — R75 3.3K — R76 3.3K
SCPCLK — SCPDI — SCPDO
SCPCLK 1-2L — SCPDI 1-2L — SCPDO 1-2L

U5 4AEEPX
UART
UARTSERCLK — CLK_UART_11.0592MHZ 1-20,1-4L,23-7G

UART1_TX_SHRT0_TX — UART1_TX
UART1_RX_SHRT0_RX — UART1_RX
UART1_RTS#_SHRT0_RTS# — PERPARB_UART1_RTS#
UART1_CTS#_SHRT0_CTS# — PERPARB_UART1_CTS#
UART2_TX_SHRT0_DTR# — UART2_TX
UART2_RX_SHRT0_RI# — UART2_RX
UART2_RTS#_SHRT0_DSR# — CPU_SHRT0_DSR#
UART2_CTS#_SHRT0_DCD# — CPU_SHRT0_DCD#

IIC0
IIC0SCLK — IIC0SDATA
IIC1_SPI
SCPCLKDVNT_IIC1SCLK — SCPDI_IIC1SDATA — SCPD0

NAND Flash Interface
NOT USED
NFALE NFCLE NFREN# NFWEN# — NC NC NC NC
NFRDYBUSY# — R77 3.3K
NFCE3#_PERCS3# — R78 3.3K

U40 P15A3157
U41 P15A3157
U45 P15A3157
U46 P15A3157
VCC A B GND — B0 B1 S
SHD BD TO A
UART1_CTS# — R82 3.3K
UART2_RTS# — R80 3.3K
UART2_CTS# — R79 3.3K

U44 ICL3225ECA
U43 ICL3225ECA
C1P C2P C1N C2N VCC VP VN T1IN T2IN R1OUT R2OUT FORCEON FORCEOFF INVALID READY GND
C192 0.1UF 0402 — C194 0.1UF 0402 — C193 0.1UF 0402 — C195 0.1UF 0402
C196 0.1UF 0402 — C198 0.1UF 0402 — C197 0.1UF 0402 — C199 0.1UF 0402
C652 0.1UF 0402 — C651 0.1UF 0402 — C649 0.1UF 0402 — C653 0.1UF 0402
R85 10K — R87 10K
X_UART1_TX X_UART1_RX X_UART1_RTS# X_UART1_CTS# X_UART2_TX X_UART2_RX X_UART2_RTS# X_UART2_CTS#
5V_VIN — CTRL

P2 9P DSUB MALE — UART Port 0
J14 — UART Port 1
NC P1 P2 P3 P4 P5 NC P6 P7 P8 NC P9 NC P10
HLE-105-02-G-DV

BOOT_CFG2 1-1G,1-3L,24-9M
BOOT_CFG1 1-1G,1-3L,24-9M
BOOT_CFG0 1-2G,1-3L,24-9M

I2C0_SCLK 1-21,1-9B,2-2P
I2C0_33_DATA 1-2L,1-9E
EE2_BOOT_WP 1-2G,1-3L,24-6C
EE1_WP 1-2G,1-3L,24-6C
M66EN 1-2G,1-3G,1-4E,19-2D,24-10L
A7140B8 — VCC WP SCL SDA A2 A1 A0 GND
R88 15K — R89 15K
NO POP — R69 — U47 P15A3157 — I2C0_SDATA

PDBY 1-21,1-3G,24-8C,25-5G,25-7B,25-7M
PR_WF 1-1i,1-3G,24-8C,25-5G,25-6M,25-7B
PWBE_0# 1-21,1-3G,24-8C,25-6M,25-7B
PWBE_1# 25-6M,25-7C
PWBE_2# 25-7C
PWBE_3# 25-7C
PREADY 25-7C,25-8Q
PBLASTF 25-6M,25-7C

25-8C,25-10B PCS_0
1-21,1-3G,24-8C,25-7B,25-7M,25-9B PDBY
1-1i,1-3G,24-8C,25-6M,25-7B,25-9B PR_WF
RESET_PORb 1-2G,1-3G,1-5L,23-9J,24-8C

U15 PER_A[30:2] PER_SP_A[16:2] PER_CS0 PER_OE_N PER_R_W_N PER_WBE[1] PER_WBE[0] PER_B_LAST
PER_D[15:0] PER_D_PAR[1] PER_D_PAR[0] PER_ERR PER_READY
BANKS=1, 2, 4
CHIP SELECT 1

3V3_4 3V3_3 3V3_2 3V3_1 3V3_5 — AL12 AG14 AM19 AM21 G14 D13

C334 470F 6V — C335 470F 6V — C330 220NF 0.3V — C331 220NF 0.3V — C332 220NF 0.3V — C333 220NF 0.3V
GND

ROACH/iBOB2	ROACH_PPC_NVM_SERIAL
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-5-2007_15:15	DRAWN: F KAPP · APPR:
PATH PATH	CHECKED: E BAUERMEISTER · SHEET 25 OF 25