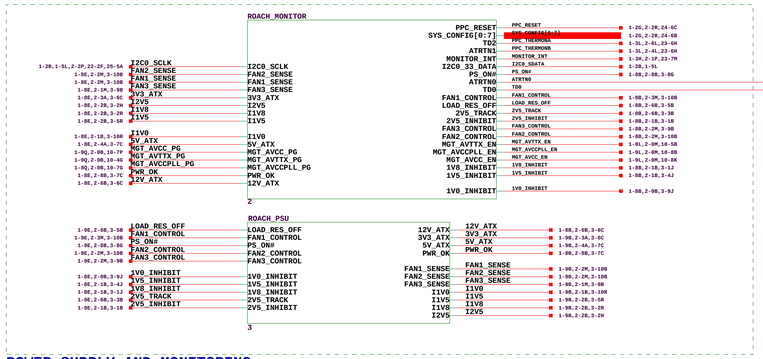
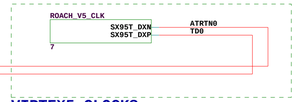
VIRTEX5

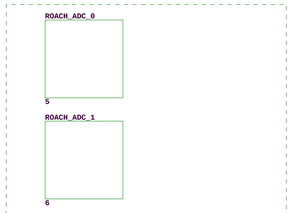
POWER SUPPLY AND MONITORING



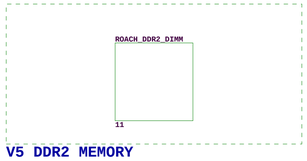
VIRTEX5 CLOCKS



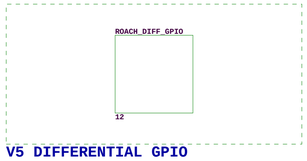
ZDOK/ADC INTERFACE



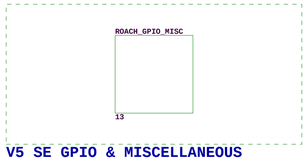
V5 DDR2 MEMORY



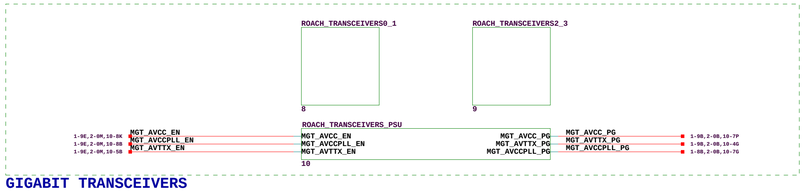
V5 DIFFERENTIAL GPIO



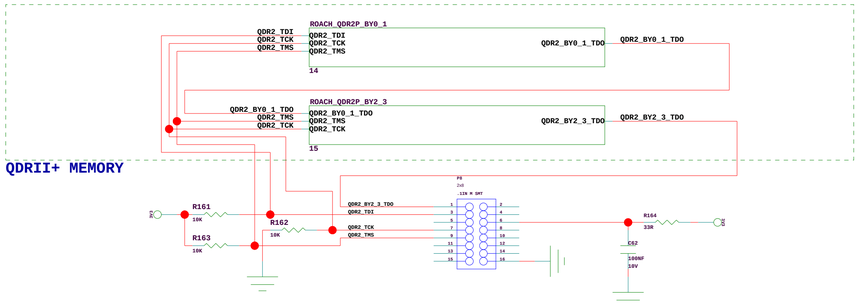
V5 SE GPIO & MISCELLANEOUS



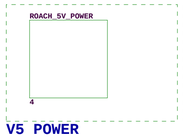
GIGABIT TRANSCEIVERS



QDRII+ MEMORY



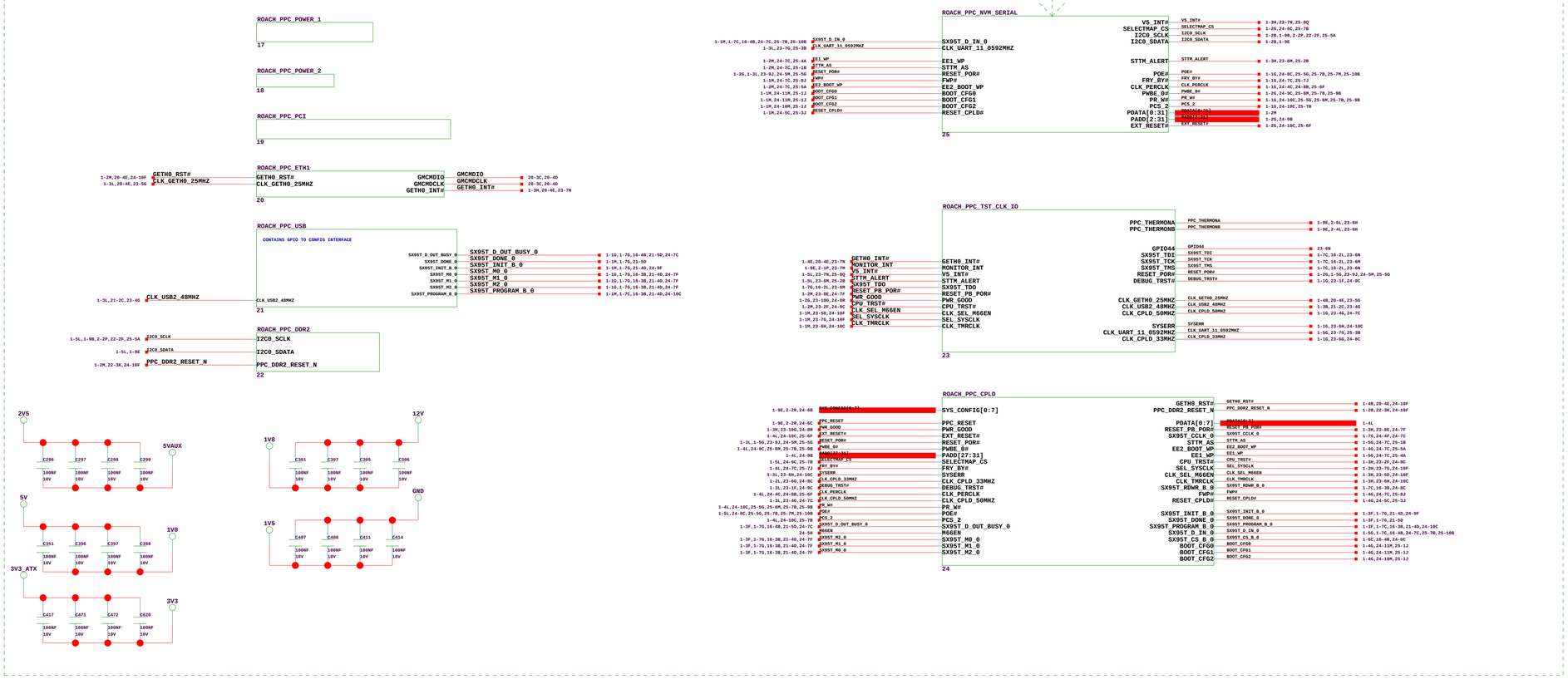
V5 POWER



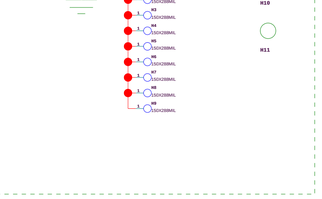
VIRTEX5 CONFIGURATION

V5 SE GPIO & MISCELLANEOUS

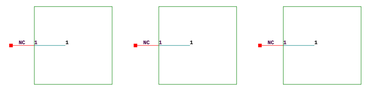
PPC



MECHANICAL



BOARD FIDUCIALS



LOGO'S

PLACEHOLDER FOR PCB
MEERKAT LOGO

PLACEHOLDER FOR PCB
CASPER LOGO

PLACEHOLDER FOR PCB
ROACH LOGO

PLACEHOLDER FOR PCB
NRAO LOGO

BOARD SERIAL NUMBER

CONTRIBUTORS

ETIENNE BAUERMEISTER
HENRY CHEN
STEVE DURAND
FRANCOIS KAPP
ALAN LANGMAN
GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

6-20-2008_10:20

PATH PATH

ROACH_TOP	
DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 1 OF 25

roach_AFS600_pcb

PLACE AT ACTEL 3V3 POWER PINS

PLACE AT ACTEL 1V5 POWER PINS

roach_AFS600_powerpins

TIE TO GROUND IF PLL'S ARE NOT USED

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

roach_AFS600_configpins

XPORT - PLACE IN REAR I/O REGION
XP1001001-03R

TEMPERATURE DIODE HEADER

ACTEL JTAG CONNECTOR

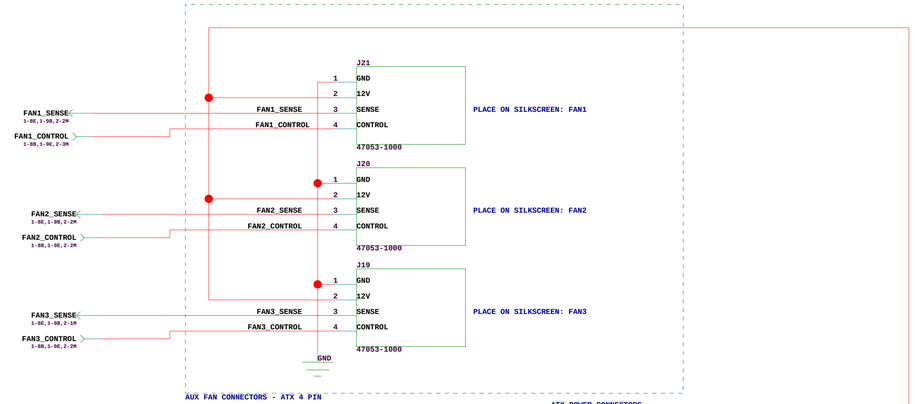
PB POWER SWITCH

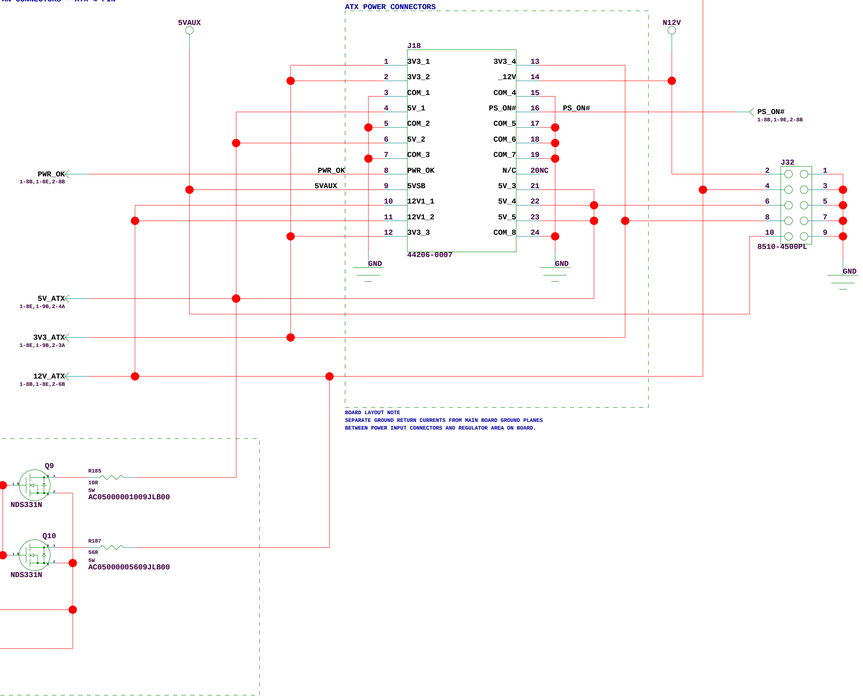
KEY - REMOVE PIN

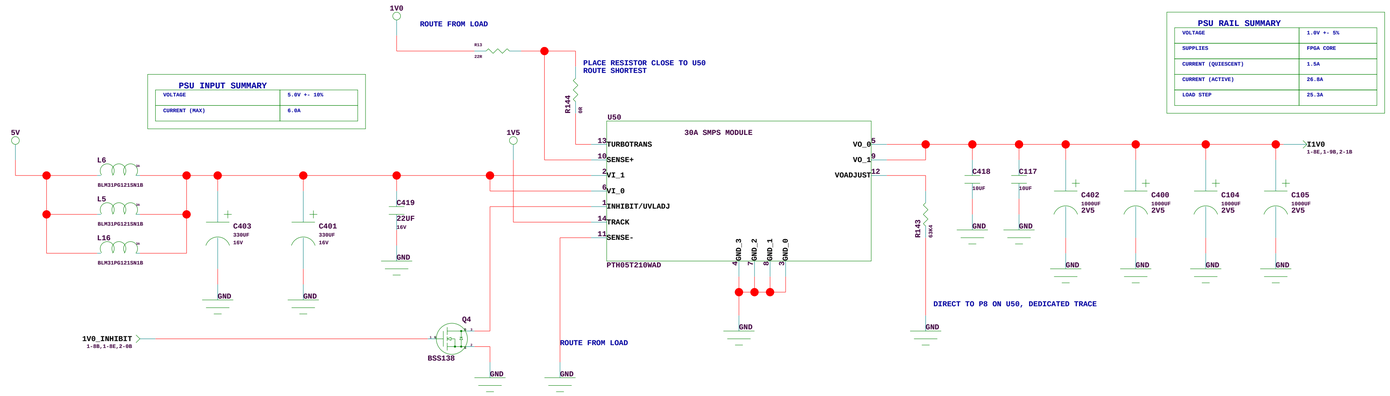
MONITOR RESET

REFERENCE RESISTOR/ADC VALUES				FOR 8 BIT ADC USING 2.56V REFERENCE:	
VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)	ADC COUNT AT MAX POWER	CURRENT/BIT (A)
12V	0R01	3.36	0.11	33	0.1
5V	0R0047	6.78	0.22	31	0.21
3V3	0R01	3.47	0.12	34	0.1
2V5	0R01	3.56	0.13	35	0.1
1V8	0R0022	12.91	0.37	28	0.45
1V5	0R0047	6.77	0.22	31	0.21
1V0	0R001	26.79	0.72	26	1.0

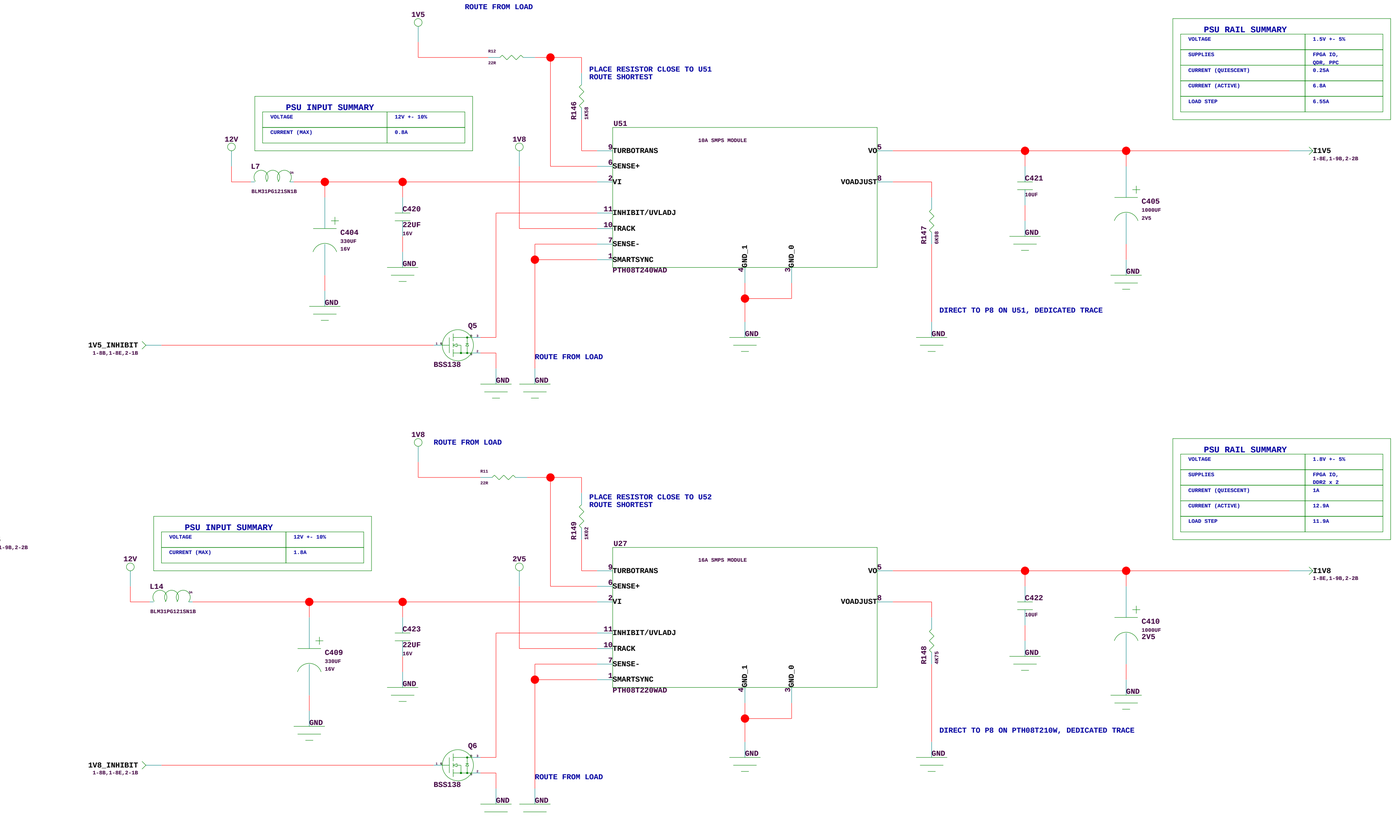
ROACH/iBOB2	ROACH_MONITOR
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A; DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-20-2008_10:20; PATH PATH	DRAWN: F KAPP; APPR: ; CHECKED: E BAUERMEISTER; SHEET 2 OF 25

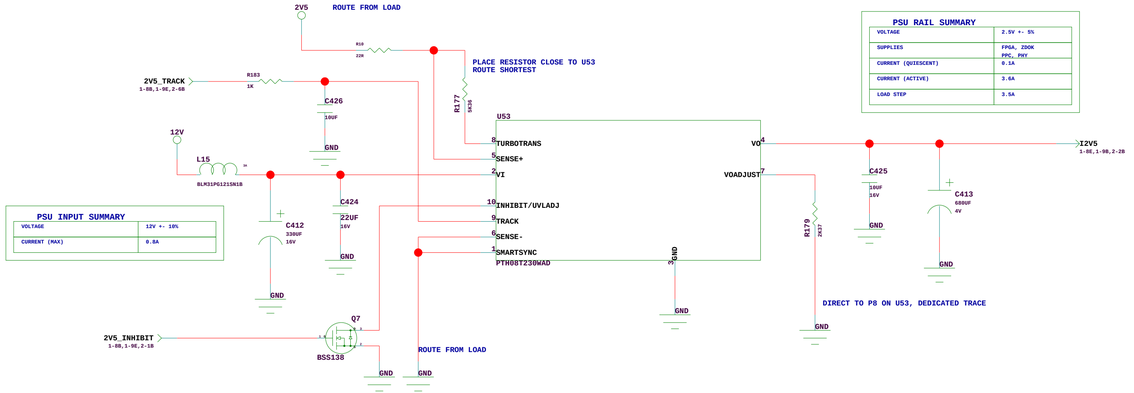




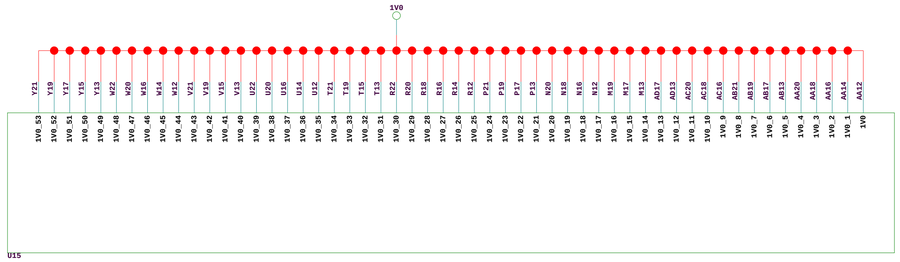


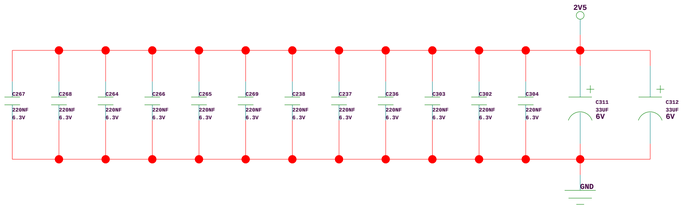
1.2V SUPPLY DELETED - NOT REQUIRED

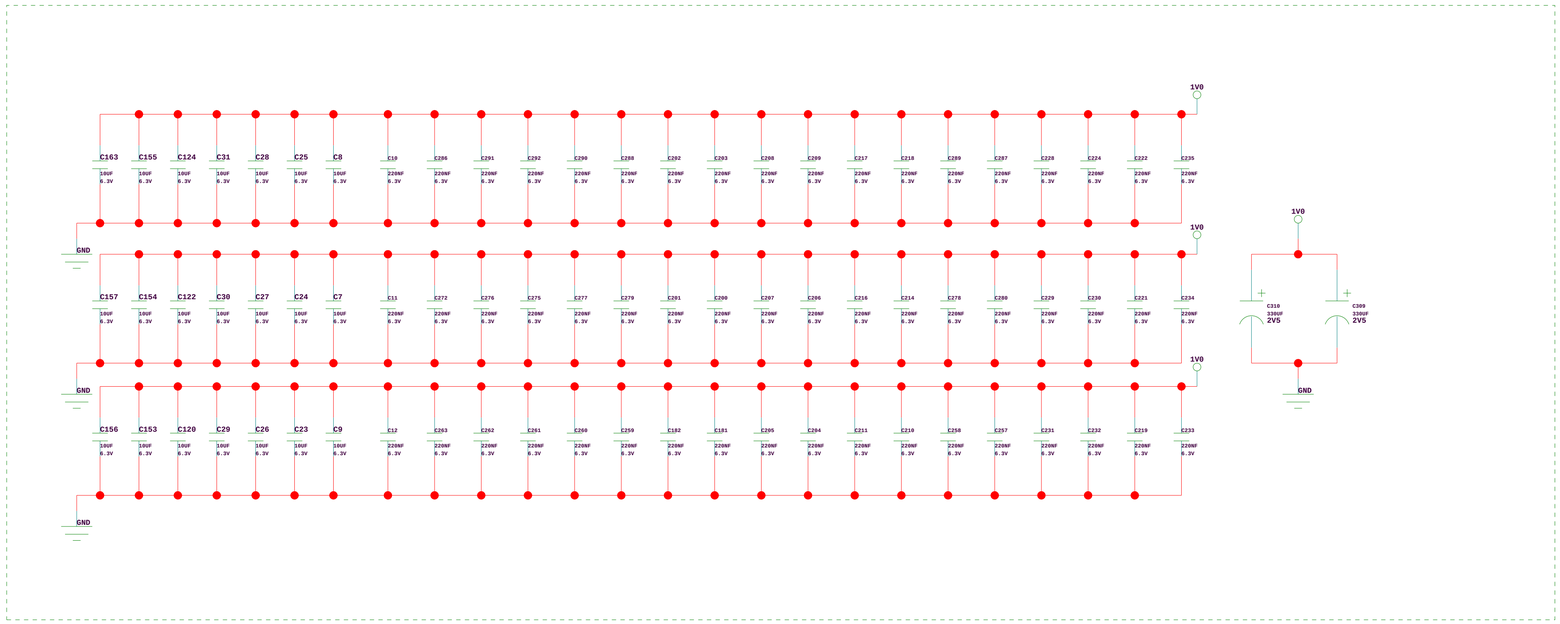


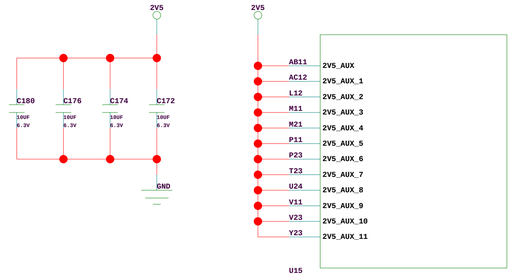


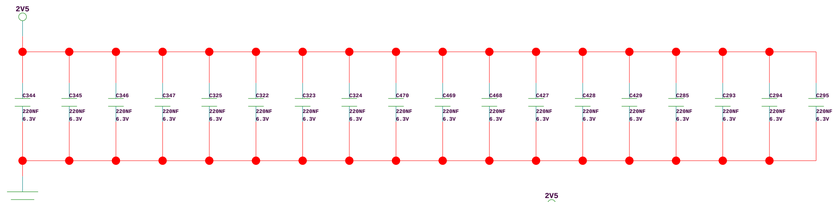
ROACH/iBOB2	ROACH_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-20-2008_10:20; PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 3 OF 25

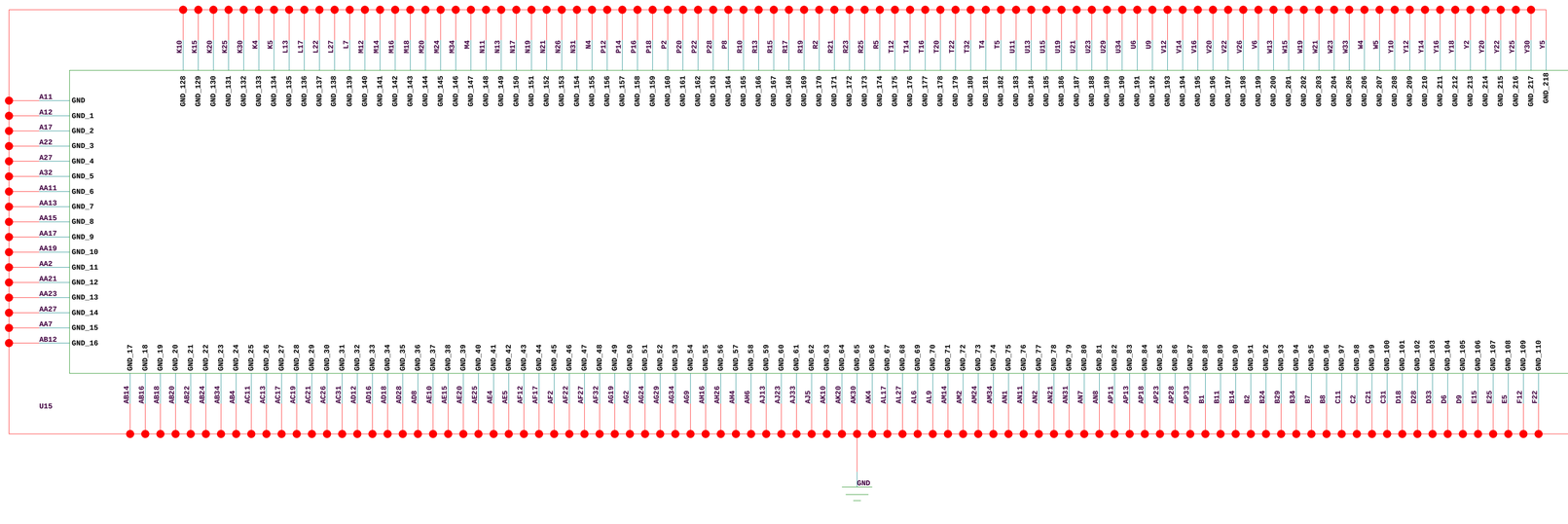


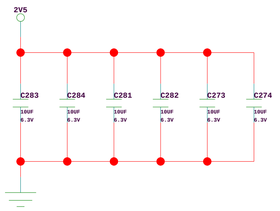


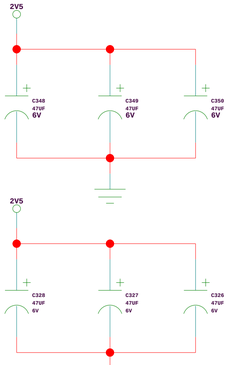












ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
6-20-2008_10:20 PATH PATH	

5-5L	ZDOK0_CLK0_P	J20	ZDOK0_CLK0_P
5-5L	ZDOK0_CLK0_N	J21	ZDOK0_CLK0_N
5-3L	ZDOK0_CLK1_P	H19	ZDOK0_CLK1_P
5-3L	ZDOK0_CLK1_N	H20	ZDOK0_CLK1_N

ZDOK0_DP_P[37]	B33	ZDOK0_DP_P37	5-3L
ZDOK0_DP_N[37]	C33	ZDOK0_DP_N37	5-3L
ZDOK0_DP_P[36]	F25	ZDOK0_DP_P36	5-3L
ZDOK0_DP_N[36]	F26	ZDOK0_DP_N36	5-3L
ZDOK0_DP_P[35]	E32	ZDOK0_DP_P35	5-4L
ZDOK0_DP_N[35]	E33	ZDOK0_DP_N35	5-4L
ZDOK0_DP_P[34]	F33	ZDOK0_DP_P34	5-4L
ZDOK0_DP_N[34]	E34	ZDOK0_DP_N34	5-4L
ZDOK0_DP_P[33]	G32	ZDOK0_DP_P33	5-4L
ZDOK0_DP_N[33]	H32	ZDOK0_DP_N33	5-4L
ZDOK0_DP_P[32]	J27	ZDOK0_DP_P32	5-4L
ZDOK0_DP_N[32]	J26	ZDOK0_DP_N32	5-4L
ZDOK0_DP_P[31]	H34	ZDOK0_DP_P31	5-4L
ZDOK0_DP_N[31]	J34	ZDOK0_DP_N31	5-4L
ZDOK0_DP_P[30]	K31	ZDOK0_DP_P30	5-5L
ZDOK0_DP_N[30]	L31	ZDOK0_DP_N30	5-5L
ZDOK0_DP_P[29]	L30	ZDOK0_DP_P29	5-5L
ZDOK0_DP_N[29]	M30	ZDOK0_DP_N29	5-5L
ZDOK0_DP_P[28]	C34	ZDOK0_DP_P28	5-5L
ZDOK0_DP_N[28]	D34	ZDOK0_DP_N28	5-5L
ZDOK0_DP_P[27]	E29	ZDOK0_DP_P27	5-5L
ZDOK0_DP_N[27]	F29	ZDOK0_DP_N27	5-5L
ZDOK0_DP_P[26]	H25	ZDOK0_DP_P26	5-6L
ZDOK0_DP_N[26]	H24	ZDOK0_DP_N26	5-6L
ZDOK0_DP_P[25]	G30	ZDOK0_DP_P25	5-6L
ZDOK0_DP_N[25]	F30	ZDOK0_DP_N25	5-6L
ZDOK0_DP_P[24]	G33	ZDOK0_DP_P24	5-6L
ZDOK0_DP_N[24]	F34	ZDOK0_DP_N24	5-6L
ZDOK0_DP_P[23]	J30	ZDOK0_DP_P23	5-6L
ZDOK0_DP_N[23]	J31	ZDOK0_DP_N23	5-6L
ZDOK0_DP_P[22]	L25	ZDOK0_DP_P22	5-6L
ZDOK0_DP_N[22]	L26	ZDOK0_DP_N22	5-6L
ZDOK0_DP_P[21]	L29	ZDOK0_DP_P21	5-7L
ZDOK0_DP_N[21]	K29	ZDOK0_DP_N21	5-7L
ZDOK0_DP_P[20]	N27	ZDOK0_DP_P20	5-7L
ZDOK0_DP_N[20]	M27	ZDOK0_DP_N20	5-7L
ZDOK0_DP_P[19]	B32	ZDOK0_DP_P19	5-3J
ZDOK0_DP_N[19]	A33	ZDOK0_DP_N19	5-3J
ZDOK0_DP_P[18]	E26	ZDOK0_DP_P18	5-3J
ZDOK0_DP_N[18]	E27	ZDOK0_DP_N18	5-3J
ZDOK0_DP_P[17]	G25	ZDOK0_DP_P17	5-3J
ZDOK0_DP_N[17]	G26	ZDOK0_DP_N17	5-3J
ZDOK0_DP_P[16]	G27	ZDOK0_DP_P16	5-4J
ZDOK0_DP_N[16]	H27	ZDOK0_DP_N16	5-4J
ZDOK0_DP_P[15]	J24	ZDOK0_DP_P15	5-4J
ZDOK0_DP_N[15]	J25	ZDOK0_DP_N15	5-4J
ZDOK0_DP_P[14]	H30	ZDOK0_DP_P14	5-4J
ZDOK0_DP_N[14]	G31	ZDOK0_DP_N14	5-4J
ZDOK0_DP_P[13]	K27	ZDOK0_DP_P13	5-4J
ZDOK0_DP_N[13]	K26	ZDOK0_DP_N13	5-4J
ZDOK0_DP_P[12]	J32	ZDOK0_DP_P12	5-4J
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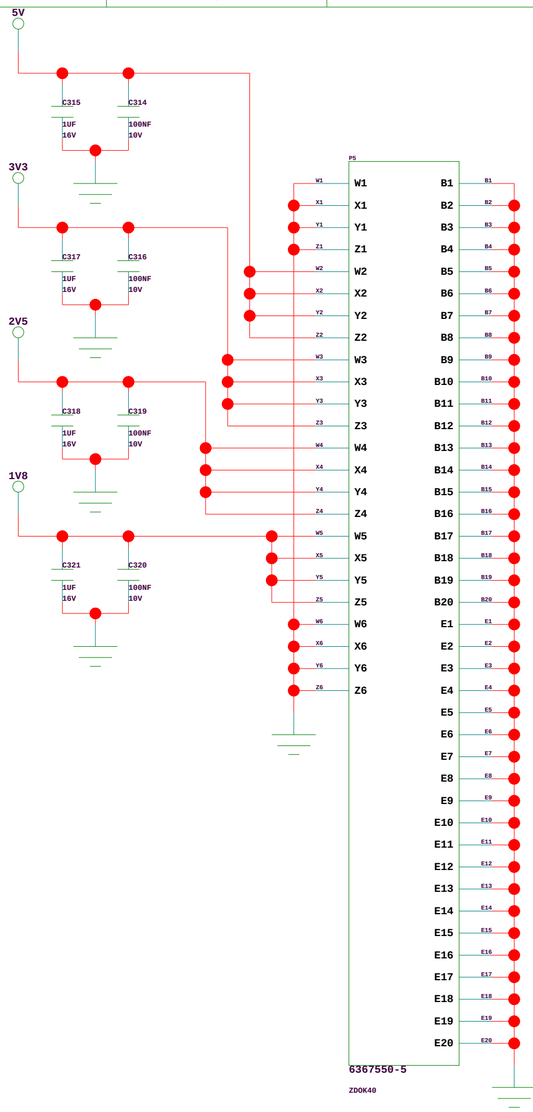
ZDOK0_DP_P[11]	K33	ZDOK0_DP_P11	5-5J
ZDOK0_DP_N[11]	K32	ZDOK0_DP_N11	5-5J
ZDOK0_DP_P[10]	L34	ZDOK0_DP_P10	5-5J
ZDOK0_DP_N[10]	K34	ZDOK0_DP_N10	5-5J
ZDOK0_DP_P[9]	C32	ZDOK0_DP_P9	5-5J
ZDOK0_DP_N[9]	D32	ZDOK0_DP_N9	5-5J
ZDOK0_DP_P[8]	E28	ZDOK0_DP_P8	5-5J
ZDOK0_DP_N[8]	F28	ZDOK0_DP_N8	5-5J
ZDOK0_DP_P[7]	F31	ZDOK0_DP_P7	5-5J
ZDOK0_DP_N[7]	E31	ZDOK0_DP_N7	5-5J
ZDOK0_DP_P[6]	H28	ZDOK0_DP_P6	5-6J
ZDOK0_DP_N[6]	G28	ZDOK0_DP_N6	5-6J
ZDOK0_DP_P[5]	H29	ZDOK0_DP_P5	5-6J
ZDOK0_DP_N[5]	J29	ZDOK0_DP_N5	5-6J
ZDOK0_DP_P[4]	K24	ZDOK0_DP_P4	5-6J
ZDOK0_DP_N[4]	L24	ZDOK0_DP_N4	5-6J
ZDOK0_DP_P[3]	K28	ZDOK0_DP_P3	5-6J
ZDOK0_DP_N[3]	L28	ZDOK0_DP_N3	5-6J
ZDOK0_DP_P[2]	M25	ZDOK0_DP_P2	5-6J
ZDOK0_DP_N[2]	M26	ZDOK0_DP_N2	5-6J
ZDOK0_DP_P[1]	M28	ZDOK0_DP_P1	5-7J
ZDOK0_DP_N[1]	N28	ZDOK0_DP_N1	5-7J
ZDOK0_DP_P[0]	M31	ZDOK0_DP_P0	5-7J
ZDOK0_DP_N[0]	N30	ZDOK0_DP_N0	5-7J

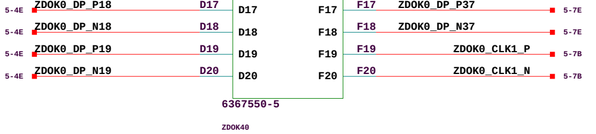
U15

BANKS=11, 13, 15, 17, 19, 21



5-0E	ZDOK0_DP_P0	A1	A1
5-0E	ZDOK0_DP_N0	A2	A2
5-0E	ZDOK0_DP_P1	A3	A3
5-0E	ZDOK0_DP_N1	A4	A4
5-0E	ZDOK0_DP_P2	A5	A5
5-0E	ZDOK0_DP_N2	A6	A6
5-1E	ZDOK0_DP_P3	A7	A7
5-1E	ZDOK0_DP_N3	A8	A8
5-1E	ZDOK0_DP_P4	A9	A9
5-1E	ZDOK0_DP_N4	A10	A10
5-1E	ZDOK0_DP_P5	A11	A11
5-1E	ZDOK0_DP_N5	A12	A12
5-1E	ZDOK0_DP_P6	A13	A13
5-1E	ZDOK0_DP_N6	A14	A14
5-1E	ZDOK0_DP_P7	A15	A15
5-1E	ZDOK0_DP_N7	A16	A16
5-2E	ZDOK0_DP_P8	A17	A17
5-2E	ZDOK0_DP_N8	A18	A18
5-2E	ZDOK0_DP_P9	A19	A19
5-2E	ZDOK0_DP_N9	A20	A20
5-2E	ZDOK0_DP_P10	D1	D1
5-2E	ZDOK0_DP_N10	D2	D2
5-2E	ZDOK0_DP_P11	D3	D3
5-2E	ZDOK0_DP_N11	D4	D4
5-2E	ZDOK0_DP_P12	D5	D5
5-2E	ZDOK0_DP_N12	D6	D6
5-3E	ZDOK0_DP_P13	D7	D7
5-3E	ZDOK0_DP_N13	D8	D8
5-3E	ZDOK0_DP_P14	D9	D9
5-3E	ZDOK0_DP_N14	D10	D10
5-3E	ZDOK0_DP_P15	D11	D11
5-3E	ZDOK0_DP_N15	D12	D12
5-3E	ZDOK0_DP_P16	D13	D13
5-3E	ZDOK0_DP_N16	D14	D14
5-3E	ZDOK0_DP_P17	D15	D15
5-3E	ZDOK0_DP_N17	D16	D16
5-4E	ZDOK0_DP_P18	D17	D17
5-4E	ZDOK0_DP_N18	D18	D18
5-4E	ZDOK0_DP_P19	D19	D19
5-4E	ZDOK0_DP_N19	D20	D20

C1	C1	ZDOK0_DP_P20	5-4E
C2	C2	ZDOK0_DP_N20	5-4E
C3	C3	ZDOK0_DP_P21	5-4E
C4	C4	ZDOK0_DP_N21	5-4E
C5	C5	ZDOK0_DP_P22	5-4E
C6	C6	ZDOK0_DP_N22	5-4E
C7	C7	ZDOK0_DP_P23	5-5E
C8	C8	ZDOK0_DP_N23	5-5E
C9	C9	ZDOK0_DP_P24	5-5E
C10	C10	ZDOK0_DP_N24	5-5E
C11	C11	ZDOK0_DP_P25	5-5E
C12	C12	ZDOK0_DP_N25	5-5E
C13	C13	ZDOK0_DP_P26	5-5E
C14	C14	ZDOK0_DP_N26	5-5E
C15	C15	ZDOK0_DP_P27	5-5E
C16	C16	ZDOK0_DP_N27	5-5E
C17	C17	ZDOK0_DP_P28	5-6E
C18	C18	ZDOK0_DP_N28	5-6E
C19	C19	ZDOK0_CLK0_P	5-7B
C20	C20	ZDOK0_CLK0_N	5-7B
F1	F1	ZDOK0_DP_P29	5-6E
F2	F2	ZDOK0_DP_N29	5-6E
F3	F3	ZDOK0_DP_P30	5-6E
F4	F4	ZDOK0_DP_N30	5-6E
F5	F5	ZDOK0_DP_P31	5-6E
F6	F6	ZDOK0_DP_N31	5-6E
F7	F7	ZDOK0_DP_P32	5-6E
F8	F8	ZDOK0_DP_N32	5-6E
F9	F9	ZDOK0_DP_P33	5-7E
F10	F10	ZDOK0_DP_N33	5-7E
F11	F11	ZDOK0_DP_P34	5-7E
F12	F12	ZDOK0_DP_N34	5-7E
F13	F13	ZDOK0_DP_P35	5-7E
F14	F14	ZDOK0_DP_N35	5-7E
F15	F15	ZDOK0_DP_P36	5-7E
F16	F16	ZDOK0_DP_N36	5-7E
F17	F17	ZDOK0_DP_P37	5-7E
F18	F18	ZDOK0_DP_N37	5-7E
F19	F19	ZDOK0_CLK1_P	5-7B
F20	F20	ZDOK0_CLK1_N	5-7B



ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

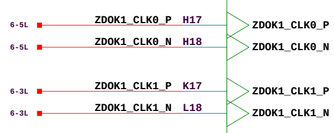
6-20-2008_10:20

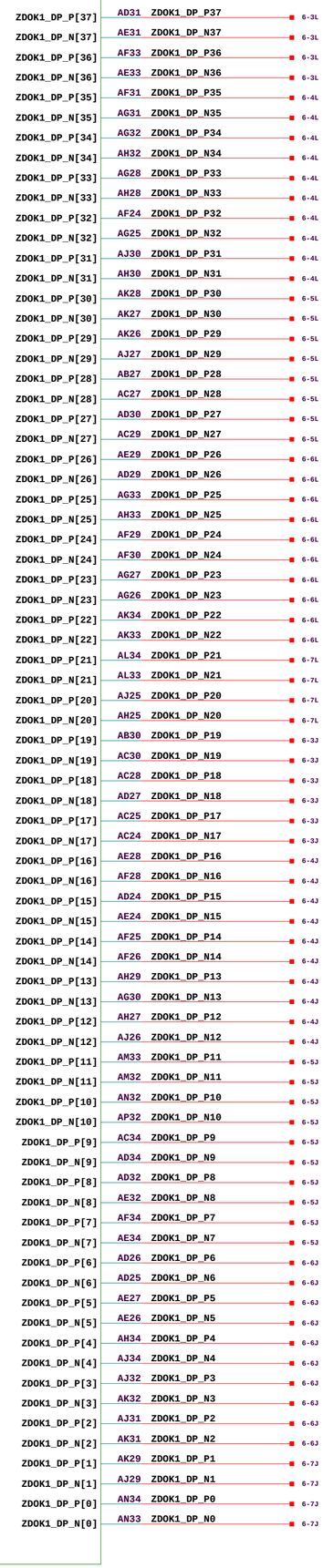
PATH PATH

ROACH_ADC_0

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	5 OF 25

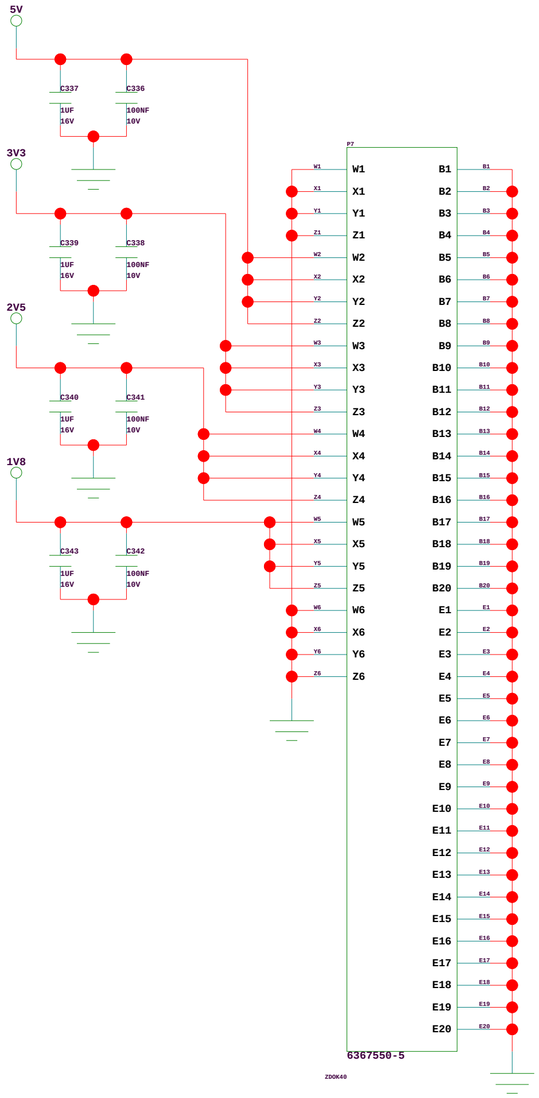
	A		B		C		D		E		F		G		H		J		K		L		M		
7																									7
6																									6
5																									5
4																									4
3																									3
2																									2
1																									1
0																									0

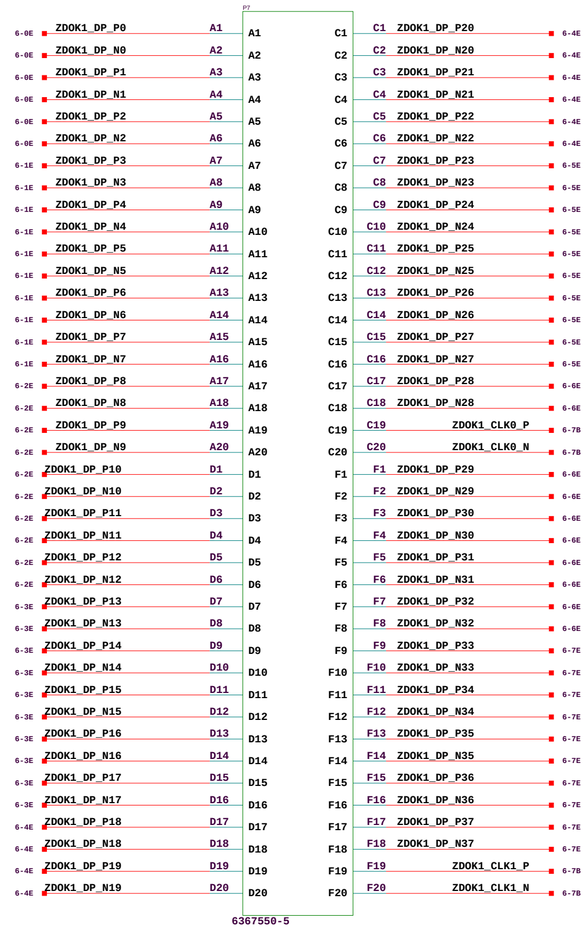




U15

BANKS=11, 13, 15, 17, 19, 21





ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

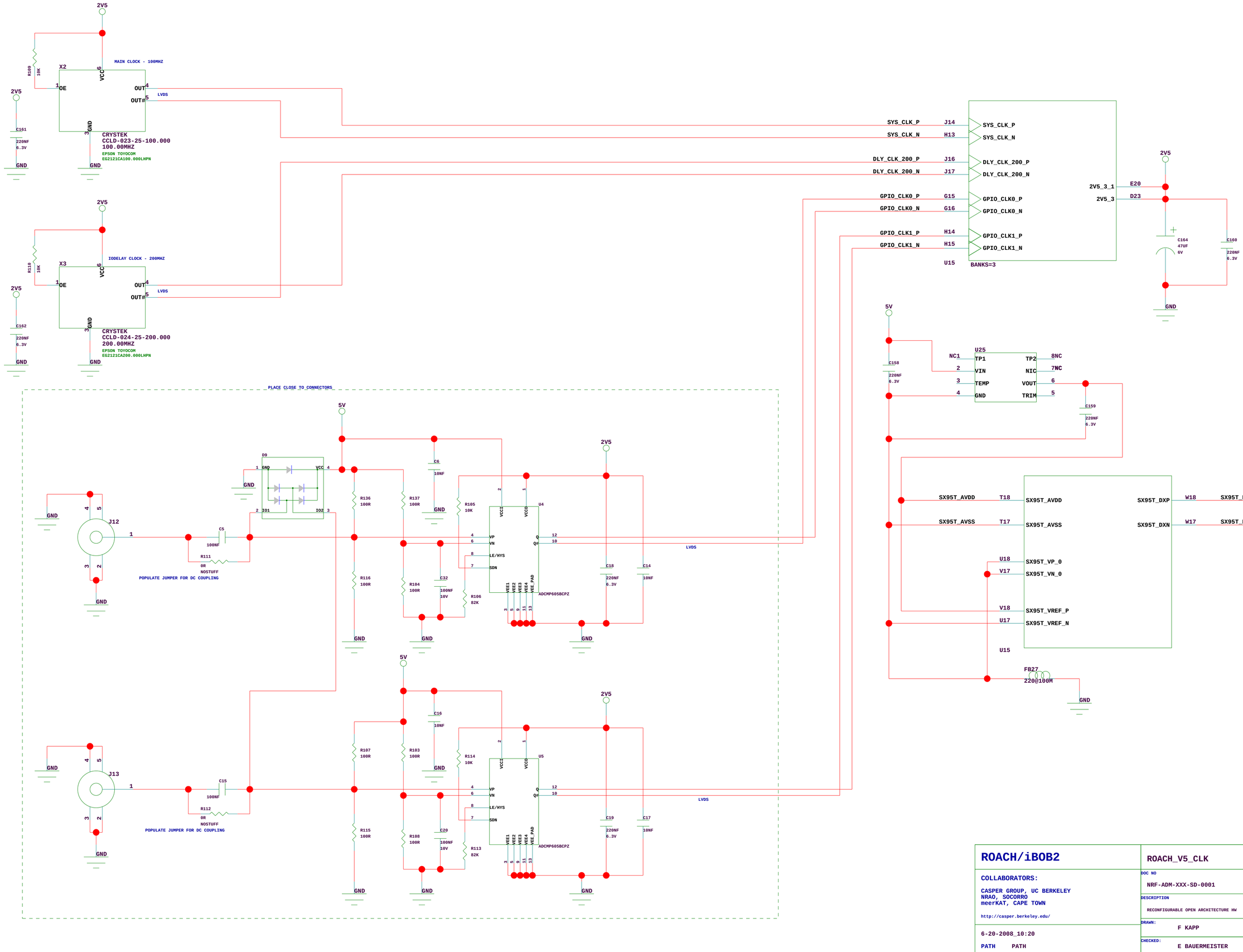
http://casper.berkeley.edu/

6-20-2008_10:20

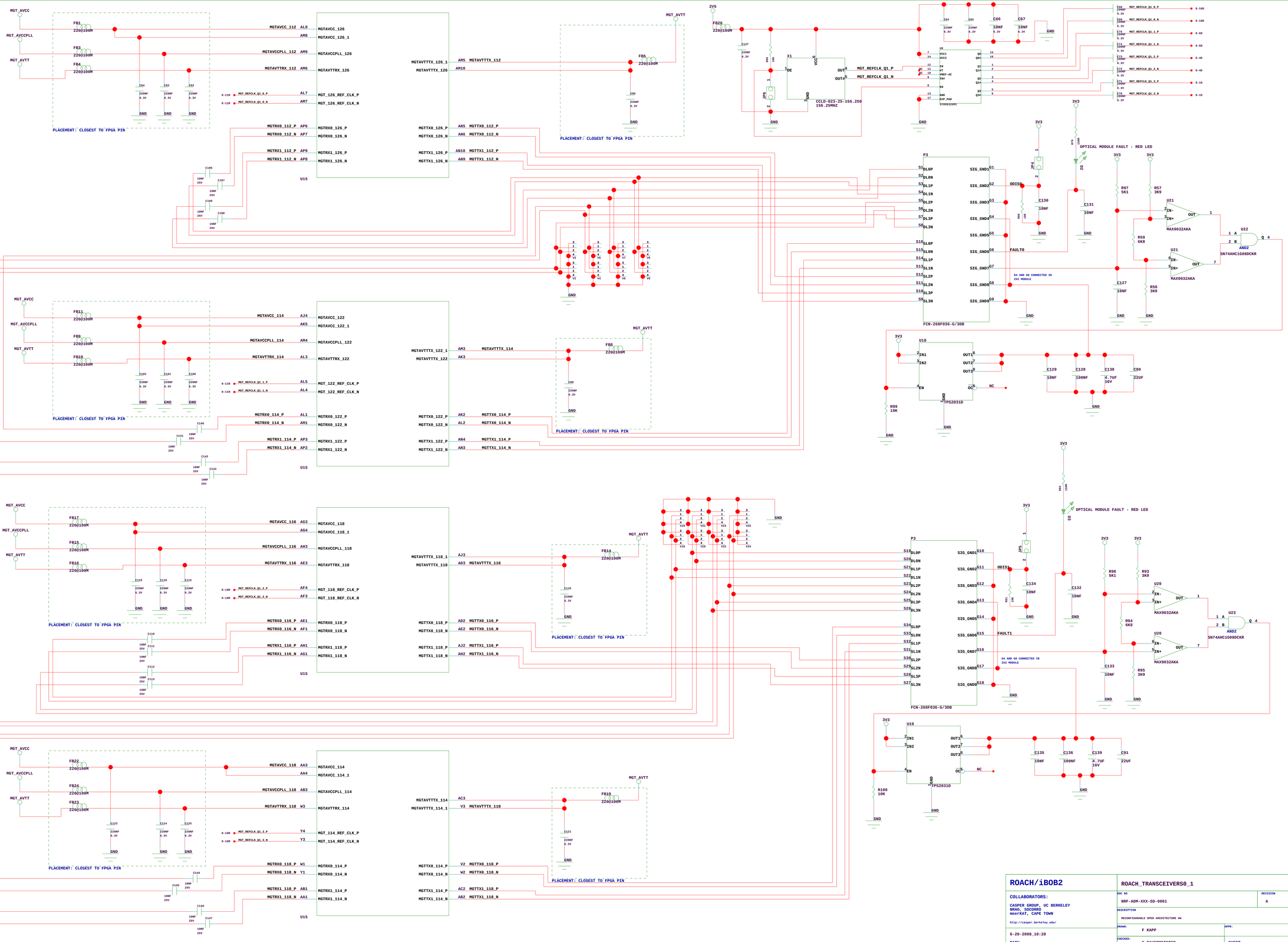
PATH PATH

ROACH_ADC_1

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	6 OF 25



ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
6-20-2008_10:20 PATH PATH	


MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB3 220@100M
FB4 220@100M
MGTAVCC_112 AL8 MGTAVCC_126
AM8 MGTAVCC_126_1
MGTAVCCPLL_112 AM9 MGTAVCCPLL_126
MGTAVTTRX_112 AM6 MGTAVTTRX_126
C84 220NF 6.3V
C93 220NF 6.3V
C92 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
8-11R MGT_REFCLK_Q1_0_P AL7 MGT_126_REF_CLK_P
8-11R MGT_REFCLK_Q1_0_N AM7 MGT_126_REF_CLK_N
MGTRX0_112_P AP6 MGTRX0_126_P
MGTRX0_112_N AP7 MGTRX0_126_N
MGTRX1_112_P AP9 MGTRX1_126_P
MGTRX1_112_N AP8 MGTRX1_126_N
U15
C106 10NF 25V
C107 10NF 25V
C109 10NF 25V
C108 10NF 25V
MGTAVTTTX_126_1 AM5 MGTAVTTTX_112
MGTAVTTTX_126 AM10
MGTTX0_126_P AN5 MGTTX0_112_P
MGTTX0_126_N AN6 MGTTX0_112_N
MGTTX1_126_P AN10 MGTTX1_112_P
MGTTX1_126_N AN9 MGTTX1_112_N
MGT_AVTT
FB5 220@100M
C96 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
V1 V2 V3 V4 V5 V6 V7 V8
GND
2V5
FB26 220@100M
C137 220NF 6.3V
R84 10K
X1
OE
VCC
OUT
GND
CCLD-023-25-156.250
156.25MHZ
JP6
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
VB VCC1 VCC2 IN VT VREF-AC CRF EN GND EXP_PAD
SY89832UMI
C64 220NF 6.3V
C65 220NF 6.3V
C66 10NF 6.3V
C67 10NF 6.3V
C68 100NF 6.3V
C69 100NF 6.3V
C75 100NF 6.3V
C74 100NF 6.3V
C73 100NF 6.3V
C72 100NF 6.3V
C71 100NF 6.3V
C70 100NF 6.3V
Q0 Q0# Q1 Q1# Q2 Q2# Q3 Q3#
MGT_REFCLK_Q1_0_P
MGT_REFCLK_Q1_0_N
MGT_REFCLK_Q1_1_P
MGT_REFCLK_Q1_1_N
MGT_REFCLK_Q1_2_P
MGT_REFCLK_Q1_2_N
MGT_REFCLK_Q1_3_P
MGT_REFCLK_Q1_3_N
8-10D
8-6D
8-4D
8-1D
P3
FCN-268F036-G/3DB
SIG_GND1 SIG_GND2 SIG_GND3 SIG_GND4 SIG_GND5 SIG_GND6 SIG_GND7 SIG_GND8 SIG_GND9
ODIS0
FAULT0
G4 AND G8 CONNECTED IN 2X2 MODULE
JP4
R85 10K
C130 10NF
C131 10NF
3V3
R79 100R
D2
OPTICAL MODULE FAULT - RED LED
R97 5K1
RS7 3K9
RS9 6K8
RS8 3K9
U21 MAX9032AKA
U22 AND2 SN74AHC1G08DCKR
C127 10NF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB11 220@100M
FB9 220@100M
FB10 220@100M
MGTAVCC_114 AJ4 MGTAVCC_122
AK5 MGTAVCC_122_1
MGTAVCCPLL_114 AM4 MGTAVCCPLL_122
MGTAVTTRX_114 AL3 MGTAVTTRX_122
C102 220NF 6.3V
C101 220NF 6.3V
C100 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
8-11R MGT_REFCLK_Q3_1_P AL5 MGT_122_REF_CLK_P
8-11R MGT_REFCLK_Q3_1_N AL4 MGT_122_REF_CLK_N
MGTRX0_114_P AL1 MGTRX0_122_P
MGTRX0_114_N AM1 MGTRX0_122_N
MGTRX1_114_P AP3 MGTRX1_122_P
MGTRX1_114_N AP2 MGTRX1_122_N
U15
C140 10NF 25V
C141 10NF 25V
C142 10NF 25V
C143 10NF 25V
MGTAVTTTX_122_1 AM3 MGTAVTTTX_114
MGTAVTTTX_122 AK3
MGTTX0_122_P AK2 MGTTX0_114_P
MGTTX0_122_N AL2 MGTTX0_114_N
MGTTX1_122_P AN4 MGTTX1_114_P
MGTTX1_122_N AN3 MGTTX1_114_N
MGT_AVTT
FB8 220@100M
C99 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
3V3
U18 TPS2031D
R99 10K
C129 10NF
C128 100NF
C138 4.7UF 16V
C90 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB17 220@100M
FB15 220@100M
FB16 220@100M
MGTAVCC_116 AG3 MGTAVCC_118
AG4 MGTAVCC_118_1
MGTAVCCPLL_116 AH3 MGTAVCCPLL_118
MGTAVTTRX_116 AE3 MGTAVTTRX_118
C119 220NF 6.3V
C118 220NF 6.3V
C115 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
8-10R MGT_REFCLK_Q3_2_P AF4 MGT_118_REF_CLK_P
8-10R MGT_REFCLK_Q3_2_N AF3 MGT_118_REF_CLK_N
MGTRX0_116_P AE1 MGTRX0_118_P
MGTRX0_116_N AF1 MGTRX0_118_N
MGTRX1_116_P AH1 MGTRX1_118_P
MGTRX1_116_N AG1 MGTRX1_118_N
U15
C110 10NF 25V
C111 10NF 25V
C112 10NF 25V
C113 10NF 25V
MGTAVTTTX_118_1 AJ3
MGTAVTTTX_118 AD3 MGTAVTTTX_116
MGTTX0_118_P AD2 MGTTX0_116_P
MGTTX0_118_N AE2 MGTTX0_116_N
MGTTX1_118_P AJ2 MGTTX1_116_P
MGTTX1_118_N AH2 MGTTX1_116_N
MGT_AVTT
FB14 220@100M
C116 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
V18 V20 V21 V22 V23 V24 V25
GND
P3
FCN-268F036-G/3DB
SIG_GND1 SIG_GND2 SIG_GND3 SIG_GND4 SIG_GND5 SIG_GND6 SIG_GND7 SIG_GND8 SIG_GND9
ODIS1
FAULT1
G4 AND G8 CONNECTED IN 2X2 MODULE
JP5
R91 10K
C134 10NF
C132 10NF
3V3
R82 100R
D3
OPTICAL MODULE FAULT - RED LED
R98 5K1
R93 3K9
R94 6K8
R95 3K9
U20 MAX9032AKA
U23 AND2 SN74AHC1G08DCKR
C133 10NF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB22 220@100M
FB24 220@100M
FB23 220@100M
MGTAVCC_118 AA3 MGTAVCC_114
AA4 MGTAVCC_114_1
MGTAVCCPLL_118 AB3 MGTAVCCPLL_114
MGTAVTTRX_118 W3 MGTAVTTRX_114
C123 220NF 6.3V
C114 220NF 6.3V
C125 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
8-10R MGT_REFCLK_Q3_3_P Y4 MGT_114_REF_CLK_P
8-10R MGT_REFCLK_Q3_3_N Y3 MGT_114_REF_CLK_N
MGTRX0_118_P W1 MGTRX0_114_P
MGTRX0_118_N Y1 MGTRX0_114_N
MGTRX1_118_P AB1 MGTRX1_114_P
MGTRX1_118_N AA1 MGTRX1_114_N
U15
C144 10NF 25V
C145 10NF 25V
C146 10NF 25V
C147 10NF 25V
MGTAVTTTX_114 AC3
MGTAVTTTX_114_1 V3 MGTAVTTTX_118
MGTTX0_114_P V2 MGTTX0_118_P
MGTTX0_114_N W2 MGTTX0_118_N
MGTTX1_114_P AC2 MGTTX1_118_P
MGTTX1_114_N AB2 MGTTX1_118_N
MGT_AVTT
FB19 220@100M
C121 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
3V3
U19 TPS2031D
R100 10K
C135 10NF
C136 100NF
C139 4.7UF 16V
C91 22UF
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
6-20-2008_10:20
PATH
ROACH_TRANSCEIVERS0_1
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE MK
DRAWN: F KAPP
CHECKED: E BAUERMEISTER
APPR:
SHEET 8 OF 25

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

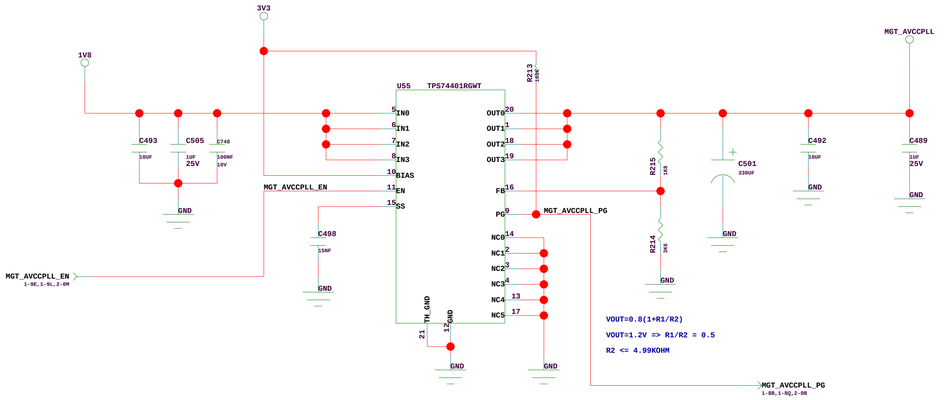
G4 AND G8 CONNECTED IN 2X2 MODULE

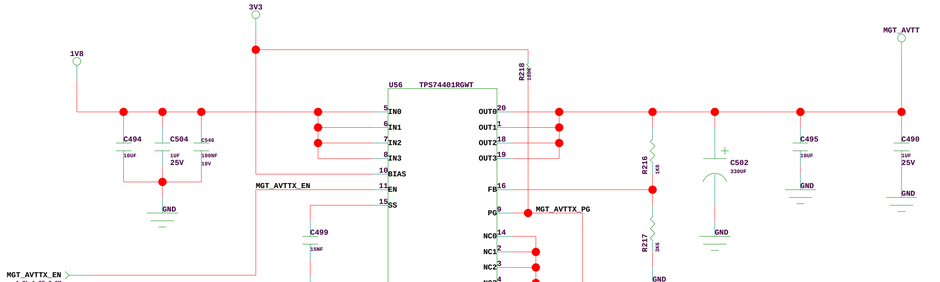
OPTICAL MODULE FAULT - RED LED

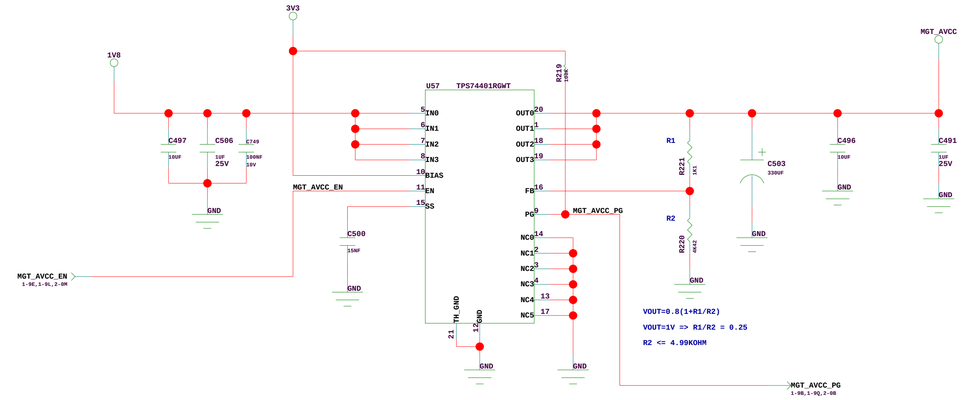
CCLD-023-25-156.250
156.25MHZ

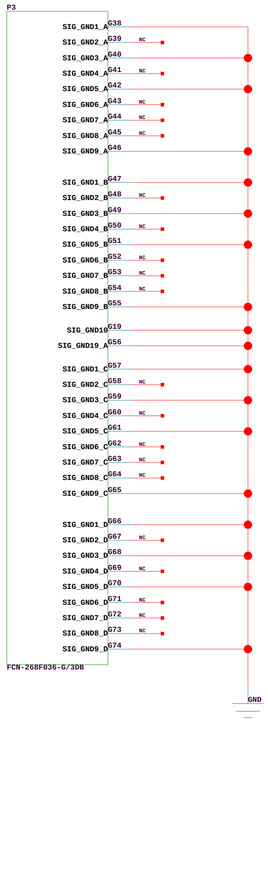
FCN-268F036-G/3DB

ROACH/iBOB2	ROACH_TRANSCEIVERS2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-20-2008_10:20	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 9 OF 25

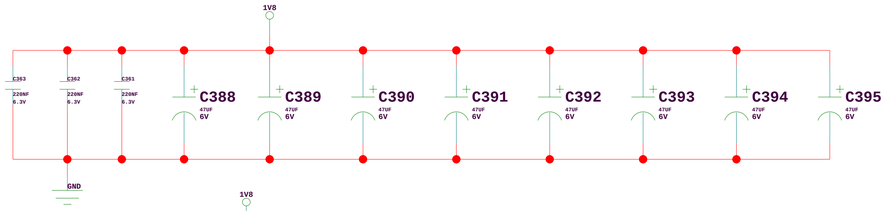


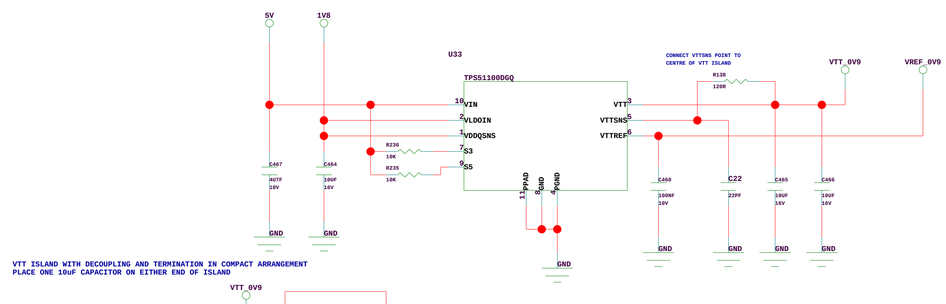




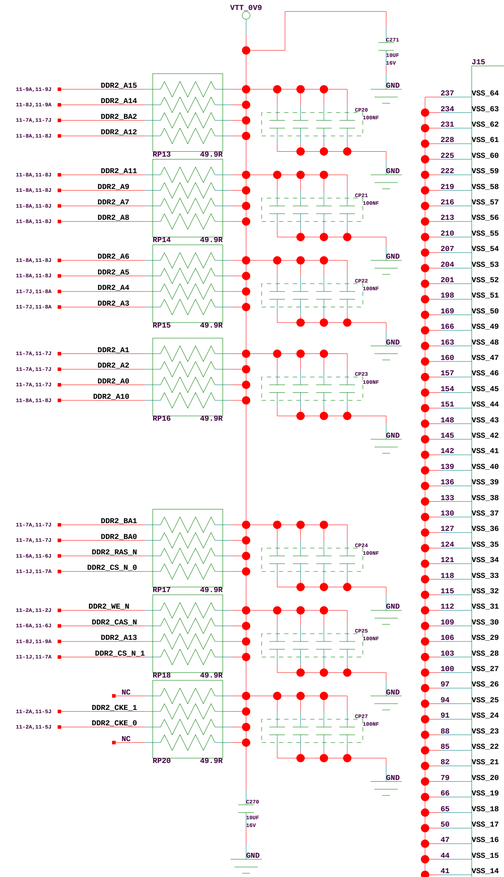


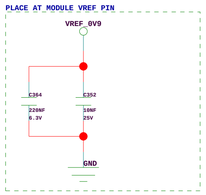
ROACH/iBOB2	ROACH_TRANSCEIVERS_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-20-2008_10:20	DRAWN: F KAPP · APPR:
PATH PATH	CHECKED: E BAUERMEISTER · SHEET 10 OF 25

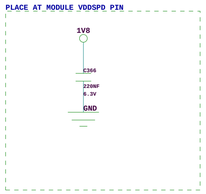


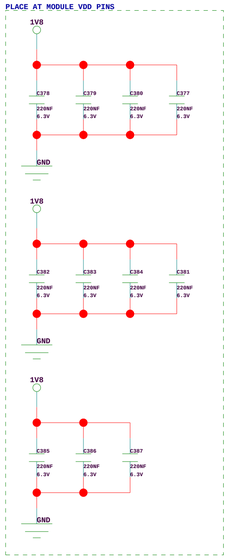


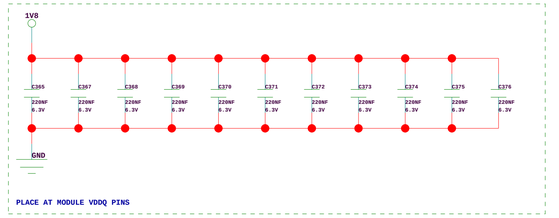
VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
PLACE ONE 10uF CAPACITOR ON EITHER END OF ISLAND



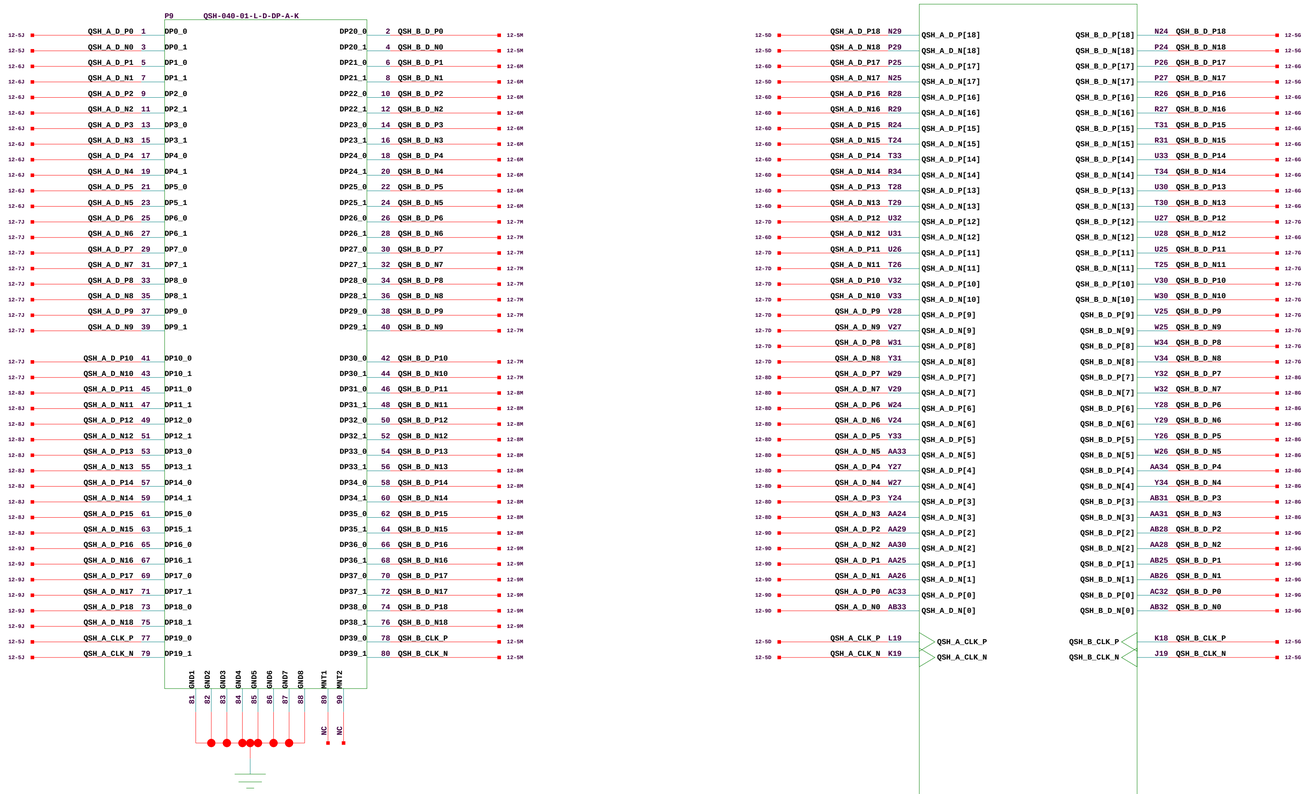




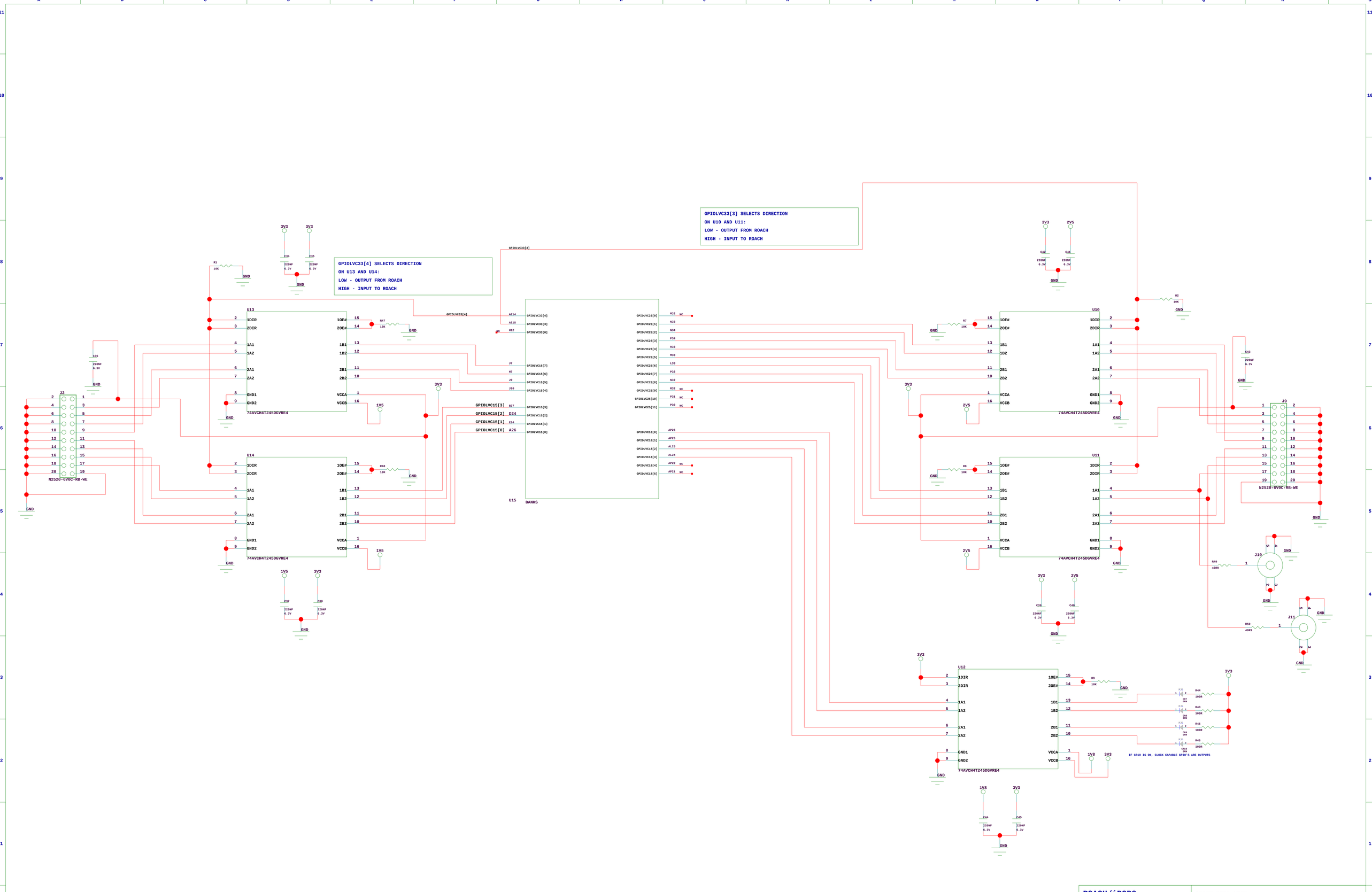




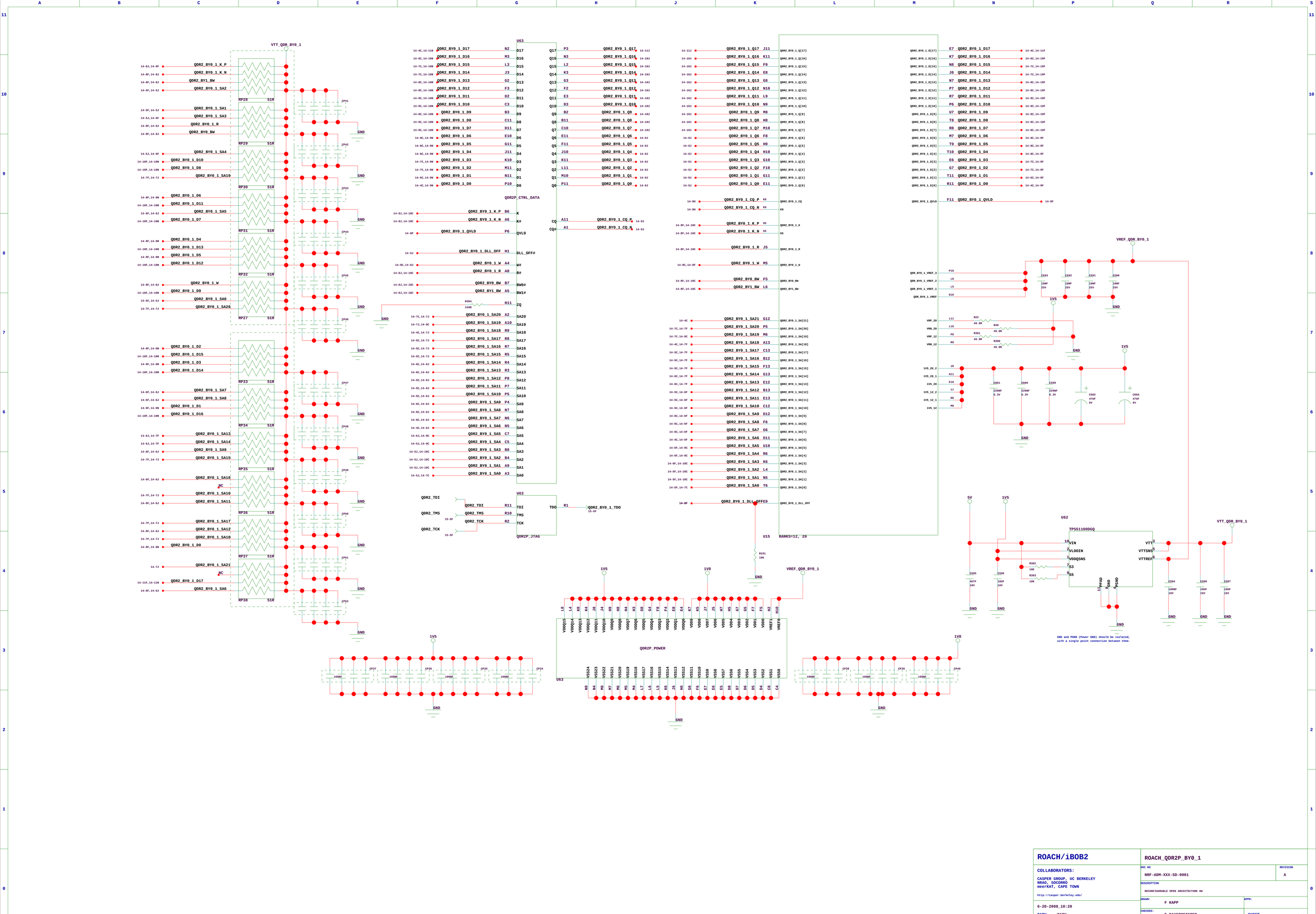
ROACH/iBOB2	ROACH_DDR2_DIMM
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE NW
6-20-2008_10:20	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 11 OF 25



ROACH/iBOB2	**ROACH_DIFF_GPIO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
6-20-2008_10:20 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 12 OF 25



ROACH/iBOB2	**ROACH_GPIO_MISC**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-20-2008_10:20 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 13 OF 25



ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS:	DOC NO: NRF-ADM-XXX-SD-0001
CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN	REVISION: A
http://casper.berkeley.edu/	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-20-2008_10:20	DRAWN: F KAPP APPR:
PATH PATH	CHECKED: E BAUERMEISTER SHEET 14 OF 25

VTT_QDR_BY2_3

RP1 51R
RP2 51R
RP3 51R
RP4 51R
RP5 51R
RP6 51R
RP7 51R
RP8 51R
RP9 51R
RP10 51R
RP11 51R
RP12 51R

15-8J,15-9F QDR2_BY2_3_K_P
15-8F,15-8J QDR2_BY2_3_K_N
15-8F,15-8J QDR3_BY3_BW
15-5F,15-5J QDR2_BY2_3_SA2
15-5F,15-5J QDR2_BY2_3_SA1
15-5J,15-6F QDR2_BY2_3_SA3
15-8F,15-8J QDR2_BY2_3_R
15-8F,15-8J QDR2_BY2_BW
15-6F,15-6J QDR2_BY2_3_SA5
15-10F,15-10N QDR2_BY2_3_D8
15-5J,15-6F QDR2_BY2_3_SA4
15-7F,15-7J QDR2_BY2_3_SA19
15-9F,15-9N QDR2_BY2_3_D6
15-10F,15-10N QDR2_BY2_3_D11
15-10F,15-10N QDR2_BY2_3_D7
15-10F,15-10N QDR2_BY2_3_D10
15-9F,15-9N QDR2_BY2_3_D4
15-10F,15-10N QDR2_BY2_3_D13
15-9F,15-9N QDR2_BY2_3_D5
15-10F,15-10N QDR2_BY2_3_D12
15-8F,15-8J QDR2_BY2_3_W
15-10F,15-10N QDR2_BY2_3_D9
15-5F,15-5J QDR2_BY2_3_SA0
15-7F,15-7J QDR2_BY2_3_SA20
15-10F,15-10N QDR2_BY2_3_D16
15-10F,15-10N QDR2_BY2_3_D15
15-9F,15-9N QDR2_BY2_3_D3
15-10F,15-10N QDR2_BY2_3_D14
15-7J QDR2_BY2_3_SA21
NC
15-11F,15-11N QDR2_BY2_3_D17
15-6F,15-6J QDR2_BY2_3_SA6
15-7F,15-7J QDR2_BY2_3_SA17
15-6F,15-6J QDR2_BY2_3_SA12
15-7F,15-7J QDR2_BY2_3_SA18
15-9F,15-9N QDR2_BY2_3_D0
15-6F,15-6J QDR2_BY2_3_SA10
NC
15-7F,15-7J QDR2_BY2_3_SA16
15-6F,15-6J QDR2_BY2_3_SA11
15-6J,15-7F QDR2_BY2_3_SA13
15-6J,15-7F QDR2_BY2_3_SA14
15-6F,15-6J QDR2_BY2_3_SA9
15-7F,15-7J QDR2_BY2_3_SA15
15-6F,15-6J QDR2_BY2_3_SA7
15-6F,15-6J QDR2_BY2_3_SA8
15-9F,15-9N QDR2_BY2_3_D1
15-9F,15-9N QDR2_BY2_3_D2

CP1 100NF
CP2 100NF
CP3 100NF
CP4 100NF
CP5 100NF
CP6 100NF
CP7 100NF
CP8
CP9
CP10
CP11
CP12
CP13
CP14
CP15
CP16
CP17
CP18
CP19

GND
1V5
1V8
5V
VREF_QDR_BY2_3

U17

15-6C,15-11N QDR2_BY2_3_D17 N2 D17
15-7C,15-10N QDR2_BY2_3_D16 M3 D16
15-7C,15-10N QDR2_BY2_3_D15 L3 D15
15-7C,15-10N QDR2_BY2_3_D14 J3 D14
15-8C,15-10N QDR2_BY2_3_D13 G2 D13
15-8C,15-10N QDR2_BY2_3_D12 F3 D12
15-9C,15-10N QDR2_BY2_3_D11 D2 D11
15-8C,15-10N QDR2_BY2_3_D10 C3 D10
15-8C,15-10N QDR2_BY2_3_D9 B3 D9
15-9C,15-10N QDR2_BY2_3_D8 C11 D8
15-9C,15-10N QDR2_BY2_3_D7 D11 D7
15-9C,15-9N QDR2_BY2_3_D6 E10 D6
15-8C,15-9N QDR2_BY2_3_D5 G11 D5
15-8C,15-9N QDR2_BY2_3_D4 J11 D4
15-7C,15-9N QDR2_BY2_3_D3 K10 D3
15-4C,15-9N QDR2_BY2_3_D2 M11 D2
15-4C,15-9N QDR2_BY2_3_D1 N11 D1
15-5C,15-9N QDR2_BY2_3_D0 P10 D0

QDR2P_CTRL_DATA

15-8J,15-10C QDR2_BY2_3_K_P B6 K
15-8J,15-10C QDR2_BY2_3_K_N A6 K#
15-9P QDR2_BY2_3_QVLD P6 QVLD
15-5J QDR2_BY2_3_DLL_OFF H1 DLL_OFF#
15-8C,15-8J QDR2_BY2_3_W A4 W#
15-8J,15-10C QDR2_BY2_3_R A8 R#
15-8J,15-10C QDR2_BY2_BW B7 BW0#
15-8J,15-10C QDR2_BY2_BW_SA A5 BW1#
R55 240R
H11 ZQ

15-7C,15-7J GND
15-7J,15-9C QDR2_BY2_3_SA20 A2 SA20
15-6C,15-7J QDR2_BY2_3_SA19 A10 SA19
15-6C,15-7J QDR2_BY2_3_SA18 R9 SA18
15-6C,15-7J QDR2_BY2_3_SA17 R8 SA17
15-5C,15-7J QDR2_BY2_3_SA16 R7 SA16
15-4C,15-7J QDR2_BY2_3_SA15 R5 SA15
15-5C,15-6J QDR2_BY2_3_SA14 R4 SA14
15-5C,15-6J QDR2_BY2_3_SA13 R3 SA13
15-6C,15-6J QDR2_BY2_3_SA12 P8 SA12
15-5C,15-6J QDR2_BY2_3_SA11 P7 SA11
15-5C,15-6J QDR2_BY2_3_SA10 P5 SA10
15-4C,15-6J QDR2_BY2_3_SA9 P4 SA9
15-4C,15-6J QDR2_BY2_3_SA8 N7 SA8
15-4C,15-6J QDR2_BY2_3_SA7 N6 SA7
15-6C,15-6J QDR2_BY2_3_SA6 N5 SA6
15-6J,15-9C QDR2_BY2_3_SA5 C7 SA5
15-5J,15-9C QDR2_BY2_3_SA4 C5 SA4
15-5J,15-10C QDR2_BY2_3_SA3 B8 SA3
15-5J,15-10C QDR2_BY2_3_SA2 B4 SA2
15-5J,15-10C QDR2_BY2_3_SA1 A9 SA1
15-5J,15-7C QDR2_BY2_3_SA0 A3 SA0

Q17 P3 QDR2_BY2_3_Q17 D26 QDR2_BY2_3_Q[17]
Q16 N3 QDR2_BY2_3_Q16 C25 QDR2_BY2_3_Q[16]
Q15 L2 QDR2_BY2_3_Q15 B25 QDR2_BY2_3_Q[15]
Q14 K3 QDR2_BY2_3_Q14 C23 QDR2_BY2_3_Q[14]
Q13 G3 QDR2_BY2_3_Q13 C22 QDR2_BY2_3_Q[13]
Q12 F2 QDR2_BY2_3_Q12 A23 QDR2_BY2_3_Q[12]
Q11 E3 QDR2_BY2_3_Q11 C20 QDR2_BY2_3_Q[11]
Q10 D3 QDR2_BY2_3_Q10 B20 QDR2_BY2_3_Q[10]
Q9 B2 QDR2_BY2_3_Q9 C19 QDR2_BY2_3_Q[9]
Q8 B11 QDR2_BY2_3_Q8 B18 QDR2_BY2_3_Q[8]
Q7 C10 QDR2_BY2_3_Q7 A19 QDR2_BY2_3_Q[7]
Q6 E11 QDR2_BY2_3_Q6 C18 QDR2_BY2_3_Q[6]
Q5 F11 QDR2_BY2_3_Q5 A20 QDR2_BY2_3_Q[5]
Q4 J10 QDR2_BY2_3_Q4 A21 QDR2_BY2_3_Q[4]
Q3 K11 QDR2_BY2_3_Q3 B21 QDR2_BY2_3_Q[3]
Q2 L11 QDR2_BY2_3_Q2 B22 QDR2_BY2_3_Q[2]
Q1 M10 QDR2_BY2_3_Q1 B23 QDR2_BY2_3_Q[1]
Q0 P11 QDR2_BY2_3_Q0 A24 QDR2_BY2_3_Q[0]

CQ A11 QDR2_BY2_3_CQ_P 15-9J
CQ# A1 QDR2_BY2_3_CQ_N 15-9J

15-8N QDR2_BY2_3_CQ_P C24 QDR2_BY2_3_CQ
15-8N QDR2_BY2_3_CQ_N D25 D25
15-9F,15-10C QDR2_BY2_3_K_P D14 QDR2_BY2_3_K
15-8F,15-10C QDR2_BY2_3_K_N E14 E14
15-8F,15-10C QDR2_BY2_3_R C15 QDR2_BY2_3_R
15-8C,15-8F QDR2_BY2_3_W F15 QDR2_BY2_3_W
15-8F,15-10C QDR2_BY2_BW D15 QDR2_BY2_BW
15-8F,15-10C QDR2_BY3_BW D16 QDR3_BW

15-6C QDR2_BY2_3_SA21 D31 QDR2_BY2_3_SA[21]
15-7C,15-7F QDR2_BY2_3_SA20 F14 QDR2_BY2_3_SA[20]
15-7F,15-9C QDR2_BY2_3_SA19 A14 QDR2_BY2_3_SA[19]
15-6C,15-7F QDR2_BY2_3_SA18 D27 QDR2_BY2_3_SA[18]
15-6C,15-7F QDR2_BY2_3_SA17 A30 QDR2_BY2_3_SA[17]
15-5C,15-7F QDR2_BY2_3_SA16 B30 QDR2_BY2_3_SA[16]
15-4C,15-7F QDR2_BY2_3_SA15 C30 QDR2_BY2_3_SA[15]
15-5C,15-7F QDR2_BY2_3_SA14 B31 QDR2_BY2_3_SA[14]
15-5C,15-7F QDR2_BY2_3_SA13 D30 QDR2_BY2_3_SA[13]
15-6C,15-6F QDR2_BY2_3_SA12 B26 QDR2_BY2_3_SA[12]
15-5C,15-6F QDR2_BY2_3_SA11 A29 QDR2_BY2_3_SA[11]
15-5C,15-6F QDR2_BY2_3_SA10 D29 QDR2_BY2_3_SA[10]
15-4C,15-6F QDR2_BY2_3_SA9 A31 QDR2_BY2_3_SA[9]
15-4C,15-6F QDR2_BY2_3_SA8 G17 QDR2_BY2_3_SA[8]
15-4C,15-6F QDR2_BY2_3_SA7 C27 QDR2_BY2_3_SA[7]
15-6C,15-6F QDR2_BY2_3_SA6 C28 QDR2_BY2_3_SA[6]
15-6F,15-9C QDR2_BY2_3_SA5 E16 QDR2_BY2_3_SA[5]
15-6F,15-9C QDR2_BY2_3_SA4 E17 QDR2_BY2_3_SA[4]
15-6F,15-10C QDR2_BY2_3_SA3 A15 QDR2_BY2_3_SA[3]
15-5F,15-10C QDR2_BY2_3_SA2 B15 QDR2_BY2_3_SA[2]
15-5F,15-10C QDR2_BY2_3_SA1 C14 QDR2_BY2_3_SA[1]
15-5F,15-7C QDR2_BY2_3_SA0 B16 QDR2_BY2_3_SA[0]
15-8F QDR2_BY2_3_DLL_OFF D20 QDR2_BY2_3_DLL_OFF

BANKS=5, 23

U15
R102 10K

QDR2_BY0_1_TDO 14-5H QDR2_BY0_1_TDO R11 TDI
QDR2_TMS 14-5F QDR2_TMS R10 TMS
QDR2_TCK 14-5F QDR2_TCK R2 TCK
TDO R1 QDR2_BY2_3_TDO
QDR2P_JTAG

QDR2_BY2_3_Q[17] F24 QDR2_BY2_3_D17 15-6C,15-11F
QDR2_BY2_3_Q[16] F23 QDR2_BY2_3_D16 15-7C,15-10F
QDR2_BY2_3_Q[15] E23 QDR2_BY2_3_D15 15-7C,15-10F
QDR2_BY2_3_Q[14] E22 QDR2_BY2_3_D14 15-7C,15-10F
QDR2_BY2_3_Q[13] D22 QDR2_BY2_3_D13 15-8C,15-10F
QDR2_BY2_3_Q[12] E21 QDR2_BY2_3_D12 15-8C,15-10F
QDR2_BY2_3_Q[11] D21 QDR2_BY2_3_D11 15-9C,15-10F
QDR2_BY2_3_Q[10] F18 QDR2_BY2_3_D10 15-8C,15-10F
QDR2_BY2_3_Q[9] A16 QDR2_BY2_3_D9 15-8C,15-10F
QDR2_BY2_3_Q[8] B17 QDR2_BY2_3_D8 15-9C,15-10F
QDR2_BY2_3_Q[7] C17 QDR2_BY2_3_D7 15-9C,15-10F
QDR2_BY2_3_Q[6] D17 QDR2_BY2_3_D6 15-9C,15-9F
QDR2_BY2_3_Q[5] F16 QDR2_BY2_3_D5 15-8C,15-9F
QDR2_BY2_3_Q[4] E19 QDR2_BY2_3_D4 15-8C,15-9F
QDR2_BY2_3_Q[3] F20 QDR2_BY2_3_D3 15-7C,15-9F
QDR2_BY2_3_Q[2] G20 QDR2_BY2_3_D2 15-4C,15-9F
QDR2_BY2_3_Q[1] F21 QDR2_BY2_3_D1 15-4C,15-9F
QDR2_BY2_3_Q[0] G21 QDR2_BY2_3_D0 15-5C,15-9F

QDR2_BY2_3_QVLD A25 QDR2_BY2_3_QVLD 15-8F

VREF_QDR_BY2_3
QDR_BY2_3_VREF_3 G18
QDR_BY2_3_VREF_2 F19
QDR_BY2_3_VREF_1 A28
QDR_BY2_3_VREF A18
C56 10NF 25V
C55 10NF 25V
C50 10NF 25V
C46 10NF 25V

VRP_5 D19 RS1 49.9R
VRN_5 E18 RS2 49.9R
VRP_23 B28 R151 49.9R
VRN_23 C29 R152 49.9R

1V5_5_2 F17
1V5_5_1 C16
1V5_5 B19
1V5_23_2 G24
1V5_23_1 F27
1V5_23 C26
C85 220NF 6.3V
C86 220NF 6.3V
C87 220NF 6.3V
C88 470F 6V
C89 470F 6V

U16
VIN 10
VLDOIN 2
VDDQSNS 1
S3 7
S5 9
VTT 3
VTTSNS 5
VTTREF 6
PPAD 11
GND 8
PGND 4
RS3 10K
RS4 10K
C58 4U7F 10V
C59 10UF 16V
C57 100NF 10V
C84 10UF 16V
C69 10UF 10V

GND and PGND (Power GND) should be isolated, with a single point connection between them.

QDR2P_POWER

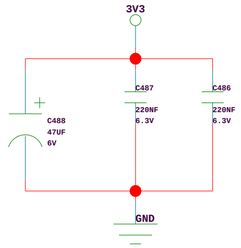
VDDQ15 L8
VDDQ14 L4
VDDQ13 K8
VDDQ12 K4
VDDQ11 J8
VDDQ10 J4
VDDQ9 H9
VDDQ8 H8
VDDQ7 H4
VDDQ6 H3
VDDQ5 G8
VDDQ4 G4
VDDQ3 F9
VDDQ2 F4
VDDQ1 E8
VDDQ0 E4
VDD9 K7
VDD8 J7
VDD7 J5
VDD6 H7
VDD5 H5
VDD4 G7
VDD3 G5
VDD2 F7
VDD1 F5
VDD0 H2
VREF1 H10
VREF0

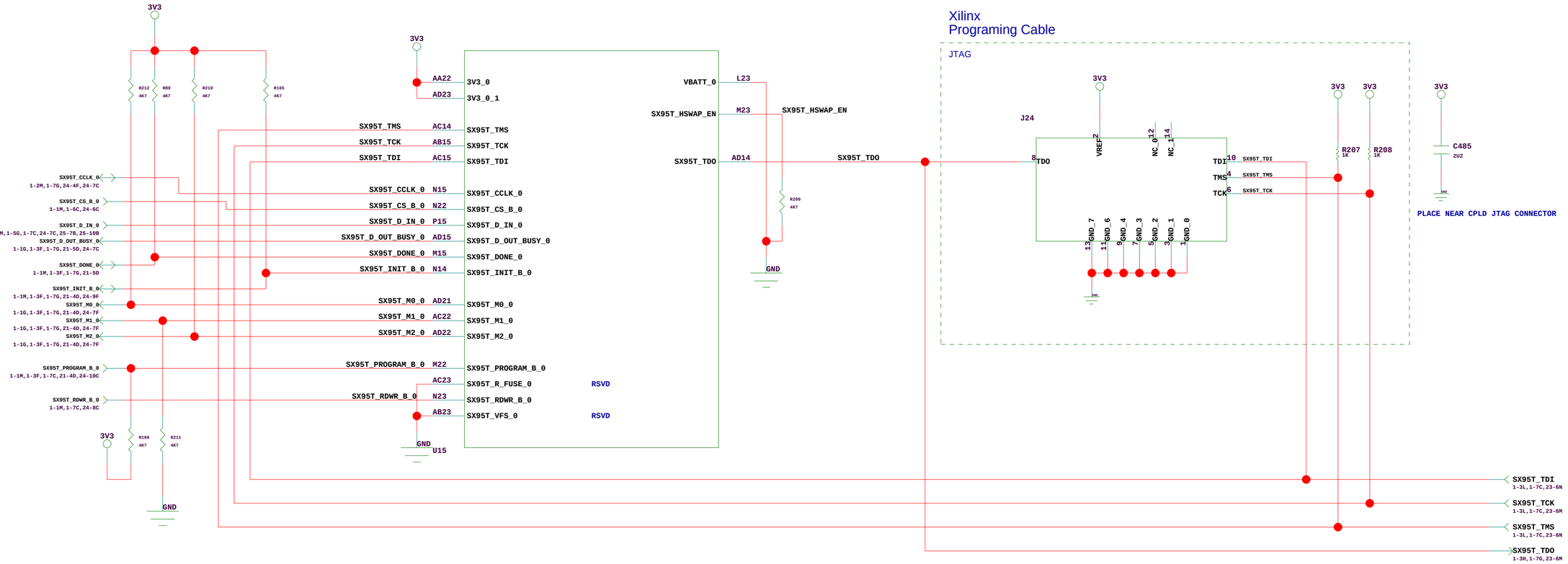
VSS24 N8
VSS23 N4
VSS22 M8
VSS21 M7
VSS20 M6
VSS19 M5
VSS18 M4
VSS17 L7
VSS16 L6
VSS15 L5
VSS14 K6
VSS13 J6
VSS12 H6
VSS11 G6
VSS10 F6
VSS9 E7
VSS8 E6
VSS7 E5
VSS6 D8
VSS5 D7
VSS4 D6
VSS3 D5
VSS2 D4
VSS1 C8
VSS0 C4

TBD

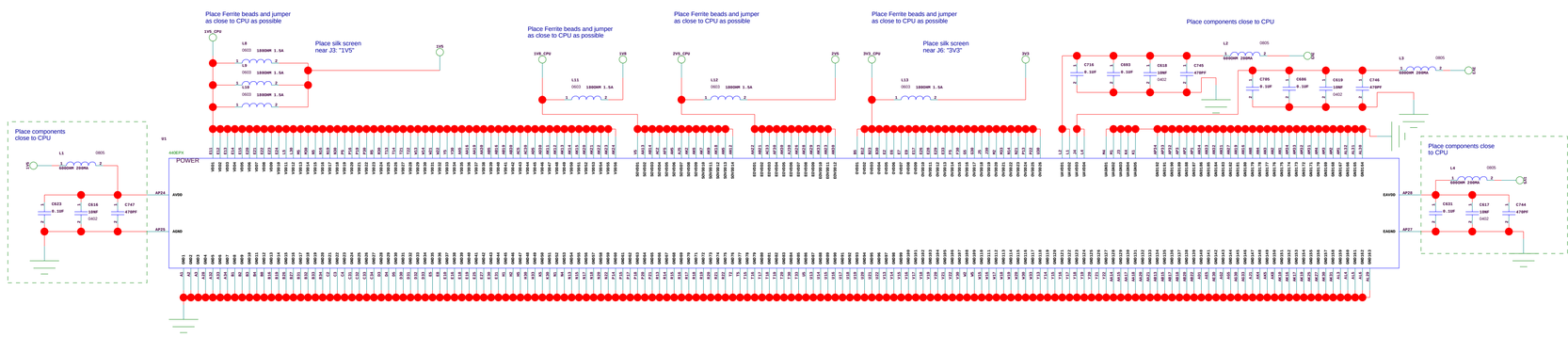
VALID CONFIGURATION MODES

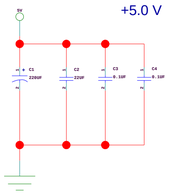
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

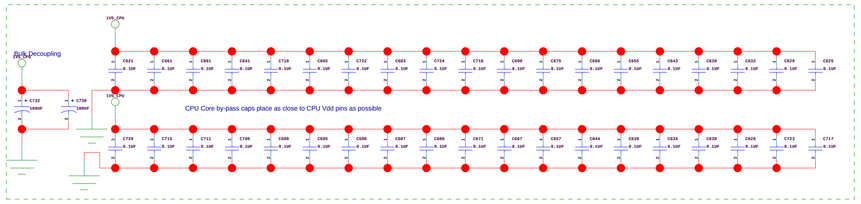


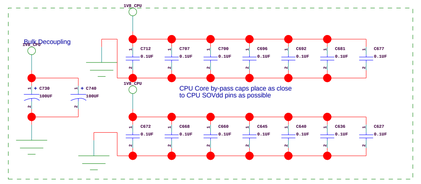


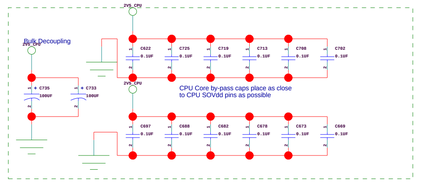
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
6-20-2008_10:20 PATH PATH	





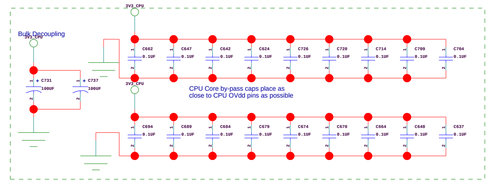


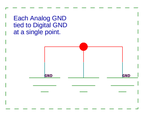




REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

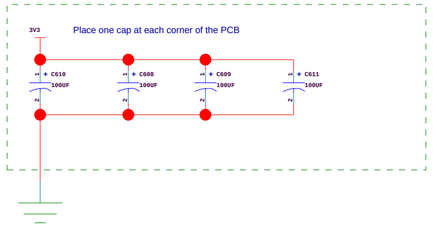
REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2





ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MK
6-20-2008_10:20 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 17 OF 25

REMOVED 3V3 GENERATION



REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET 18 OF 25
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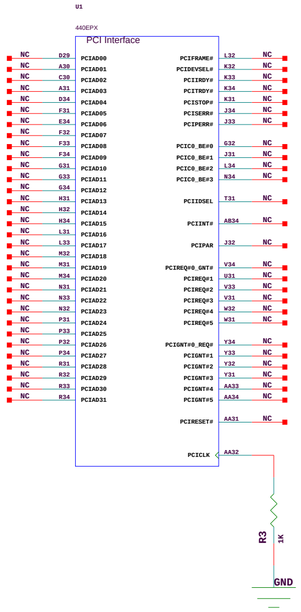

PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-20-2008_10:20 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

Place nearest PHY pin 96

Place nearest PHY pin 101

Place nearest PHY pin 98

Place nearest PHY pin 100

Place as close to PHY CORE VDD power pins as possible

Place as close to PHY IO VDD power pins as possible

UNUSED SECOND ETHERNET MAC

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups. Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place jumers in line with signals

Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5

Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

Bottom LED
Green/Toggle = ACTIVITY

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

NOSTUFF

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

JUMPER DEFAULTS

JP10, JP11	2 - 3	PHY ADD0 = 1
JP12, JP13	1 - 2	Adertised Modes 1000BASE-T, 100BASE-TX, 10BASE-T
JP14, JP15	1 - 2	
JP16, JP17	2 - 3	FULL DUPLEX
JP18, JP19	2 - 3	AUTO NEGOTIATION ENABLED
JP20-23	1 - 2	PHY ADD4:1 = 1111

ROACH/iBOB2	ROACH_PPC_ETH1
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 20 OF 25
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U1
USB 2.0 DEVICE
440EPX

USB2CLK — A5 — NC

SECOND USB INTERFACE NOT IMPLEMENTED

NOTE:
SX95T_D_IN_0 ON SHEET 25, GPIO10

GPIO28/USB2TXVAL	C6	SX95T_D_OUT_BUSY_0	SX95T_D_OUT_BUSY_0 1-1G,1-3F,1-7G,16-4B,24-7C
USB2TXRDY_REFEN	B6	NC	
USB2RXACT_HOLDREQ_RCVINH	D7	NC	
USB2RXVAL_LEAKTEST2	C8	NC	
GPIO27/USB2RXERR_EXTREQ#	A4	SX95T_DONE_0	SX95T_DONE_0 1-1M,1-3F,1-7G
GPIO30/USB2XCVRSEL_EXTACK#	M3	SX95T_INIT_B_0	SX95T_INIT_B_0 1-1M,1-3F,1-7G,24-9F
GPIO31/USB2TERMSEL_BUSREQ	P4		
USB2LS0_DRVINH1	R2	SX95T_M0_0	SX95T_M0_0 1-1G,1-3F,1-7G,16-3B,24-7F
USB2LS1_LEAKTEST_HOLDPRI	P1	NC	
GPIO32/USB2OM0	R3	SX95T_M1_0	SX95T_M1_0 1-1G,1-3F,1-7G,16-3B,24-7F
GPIO33/USB2OM1	R4		
GPIO29/USB2SUSP_HOLDACK	C5	SX95T_M2_0	SX95T_M2_0 1-1G,1-3F,1-7G,16-3B,24-7F
		SX95T_PROGRAM_B_0	SX95T_PROGRAM_B_0 1-1M,1-3F,1-7C,16-3B,24-10C

NOTE:
USB HOST ONLY

USB 2.0 PHY
HOST/DEVICE

USB2XCVR — J2 — USB2_XCVR_D+
USB2XCVR# — J1 — USB2_XCVR_D-
USB2REXT — L3 — R182 3K4 0402 — GND
USB2XTAL — N2
USB2XTAL# — N3

CLK_USB2_48MHZ 1-3B,1-3L,23-4G — CLK_USB2_48MHZ

5V — PTC1 1206L050 500MA — 1 — 2

C614 220UF 10V
C612 100NF 10V
C613 1NF 50V

CRITICAL PLACEMENT
Place SP2 very close to P6

SP2 SOT23 PGB102ST23WR
PGB102ST23WR SP2
GND

VR4 0603 5.5V 20A

NONE P6 1X4 USBA
5 — GND
1 — VCC
2 — D-
3 — D+
4 — GND
6 — GND
292303-1

ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25
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Z_ADDR

DDR_PA[15:0]

DDR_PDQ[63:0]

PPC_ECC[7:0]

DDR SDRAM

U1 — 44GEPX

DDR_PDQ0	AB2	MEMDATA00	MEMADDR00
DDR_PDQ1	AF22	MEMDATA01	MEMADDR01
DDR_PDQ2	AK26	MEMDATA02	MEMADDR02
DDR_PDQ3	AL28	MEMDATA03	MEMADDR03
DDR_PDQ4	AJ22	MEMDATA04	MEMADDR04
DDR_PDQ5	AK22	MEMDATA05	MEMADDR05
DDR_PDQ6	AK21	MEMDATA06	MEMADDR06
DDR_PDQ7	AF21	MEMDATA07	MEMADDR07
DDR_PDQ8	AF28	MEMDATA08	MEMADDR08
DDR_PDQ9	AL18	MEMDATA09	MEMADDR09
DDR_PDQ10	AK17	MEMDATA10	MEMADDR10
DDR_PDQ11	AF17	MEMDATA11	MEMADDR11
DDR_PDQ12	AK25	MEMDATA12	MEMADDR12
DDR_PDQ13	AF18	MEMDATA13	MEMADDR13
DDR_PDQ14	AK18	MEMDATA14	
DDR_PDQ15	AF16	MEMDATA15	
DDR_PDQ16	AK16	MEMDATA16	
DDR_PDQ17	AF15	MEMDATA17	
DDR_PDQ18	AF14	MEMDATA18	
DDR_PDQ19	AL17	MEMDATA19	
DDR_PDQ20	AK27	MEMDATA20	
DDR_PDQ21	AK15	MEMDATA21	
DDR_PDQ22	AK13	MEMDATA22	
DDR_PDQ23	AK24	MEMDATA23	
DDR_PDQ24	AF13	MEMDATA24	
DDR_PDQ25	AK23	MEMDATA25	
DDR_PDQ26	AF12	MEMDATA26	
DDR_PDQ27	AL12	MEMDATA27	
DDR_PDQ28	AK14	MEMDATA28	
DDR_PDQ29	AK12	MEMDATA29	
DDR_PDQ30	AL13	MEMDATA30	
DDR_PDQ31	AF11	MEMDATA31	
DDR_PDQ32	AF3	MEMDATA32	
DDR_PDQ33	AF1	MEMDATA33	
DDR_PDQ34	AD4	MEMDATA34	
DDR_PDQ35	AD3	MEMDATA35	
DDR_PDQ36	AD1	MEMDATA36	
DDR_PDQ37	AF2	MEMDATA37	
DDR_PDQ38	AE2	MEMDATA38	
DDR_PDQ39	AE1	MEMDATA39	
DDR_PDQ40	AC3	MEMDATA40	
DDR_PDQ41	AC1	MEMDATA41	
DDR_PDQ42	AA4	MEMDATA42	
DDR_PDQ43	AA3	MEMDATA43	
DDR_PDQ44	AD2	MEMDATA44	
DDR_PDQ45	AC4	MEMDATA45	
DDR_PDQ46	AB1	MEMDATA46	
DDR_PDQ47	AB2	MEMDATA47	
DDR_PDQ48	Y3	MEMDATA48	
DDR_PDQ49	Y2	MEMDATA49	
DDR_PDQ50	Y4	MEMDATA50	
DDR_PDQ51	Y1	MEMDATA51	
DDR_PDQ52	AA2	MEMDATA52	
DDR_PDQ53	AA1	MEMDATA53	
DDR_PDQ54	W3	MEMDATA54	
DDR_PDQ55	W1	MEMDATA55	
DDR_PDQ56	V1	MEMDATA56	
DDR_PDQ57	U2	MEMDATA57	
DDR_PDQ58	W2	MEMDATA58	
DDR_PDQ59	Y4	MEMDATA59	
DDR_PDQ60	R1	MEMDATA60	
DDR_PDQ61	V3	MEMDATA61	
DDR_PDQ62	T2	MEMDATA62	
DDR_PDQ63	T3	MEMDATA63	

DDR_PA0	AM5	MEMADDR00	
DDR_PA1	AP4	MEMADDR01	
DDR_PA2	AP5	MEMADDR02	
DDR_PA3	AM6	MEMADDR03	
DDR_PA4	AP6	MEMADDR04	
DDR_PA5	AN6	MEMADDR05	
DDR_PA6	AL7	MEMADDR06	
DDR_PA7	AN7	MEMADDR07	
DDR_PA8	AM7	MEMADDR08	
DDR_PA9	AP7	MEMADDR09	
DDR_PA10	AL2	MEMADDR10	
DDR_PA11	AL8	MEMADDR11	
DDR_PA12	AM8	MEMADDR12	
DDR_PA13	AN4	MEMADDR13	
DDR_PBA0	AJ3	BA0	
DDR_PBA1	AK3	BA1	
DDR_PBA2	AP8	BA2	
DDR_PRAS#	AJ4	RAS#	
DDR_PCAS#	AN4	CAS#	
DDR_PWE#	AJ2	WE#	
DDR_PDM0	AL21	DM0	
DDR_PDM1	AP18	DM1	
DDR_PDM2	AP15	DM2	
DDR_PDM3	AL14	DM3	
DDR_PDM4	AD4	DM4	
DDR_PDM5	AN3	DM5	
DDR_PDM6	Y3	DM6	
DDR_PDM7	U3	DM7	
DDR_PDM8	AN18	DM8	
DDR_PDQS0	AM21	DQS0	
DDR_PDQS1	AM19	DQS1	
DDR_PDQS2	AL15	DQS2	
DDR_PDQS3	AM13	DQS3	
DDR_PDQS4	AE3	DQS4	
DDR_PDQS5	AN4	DQS5	
DDR_PDQS6	W4	DQS6	
DDR_PDQS7	Y4	DQS7	
DDR_PDQS8	AP10	DQS8	
DDR_PODT0	AN3	MEMDT0	
DDR_PODT1	AG1	MEMDT1	
DDR_PCS0#	AN2	BANKSEL#0	
DDR_PCS1#	AM1	BANKSEL#1	
DDR_PCKE	AN9	MEMCLKEN	
DDR_PCLKOUT	AL1	MEMCLKOUT	
DDR_PCLKOUT#	AK1	MEMCLKOUT#	

PPC_ECC0	AM11	ECC0	
PPC_ECC1	AL11	ECC1	
PPC_ECC2	AN9	ECC2	
PPC_ECC3	AL9	ECC3	
PPC_ECC4	AM11	ECC4	
PPC_ECC5	AN11	ECC5	
PPC_ECC6	AM10	ECC6	
PPC_ECC7	AP9	ECC7	

VSS1	A2	VSS1	
VSS2	A5	VSS2	
VSS3	A8	VSS3	
VSS4	A15	VSS4	
VSS5	A20	VSS5	
VSS6	A23	VSS6	
VSS7	A26	VSS7	
VSS8	A29	VSS8	
VSS9	AA5	VSS9	
VSS10	AA24	VSS10	
VSS11	AB4	VSS11	
VSS12	AB23	VSS12	
VSS13	AC5	VSS13	
VSS14	AC24	VSS14	
VSS15	AD6	VSS15	
VSS16	AD23	VSS16	
VSS17	AE5	VSS17	
VSS18	AE24	VSS18	
VSS19	AF4	VSS19	
VSS20	AF23	VSS20	
VSS21	AF26	VSS21	
VSS22	AG5	VSS22	
VSS23	AG24	VSS23	
VSS24	AH6	VSS24	
VSS25	AH23	VSS25	
VSS26	AJ5	VSS26	
VSS27	AJ24	VSS27	
VSS28	AK4	VSS28	
VSS29	AK7	VSS29	
VSS30	AK10	VSS30	
VSS31	AK19	VSS31	
VSS32	AL3	VSS32	
VSS33	AL6	VSS33	
VSS34	AL10	VSS34	
VSS35	AL16	VSS35	
VSS36	AL20	VSS36	
VSS37	AL23	VSS37	
VSS38	AL26	VSS38	
VSS39	AM2	VSS39	
VSS40	AM9	VSS40	
VSS41	AM12	VSS41	
VSS42	AM15	VSS42	
VSS43	AM18	VSS43	
VSS44	AM22	VSS44	
VSS45	AM25	VSS45	
VSS46	AN1	VSS46	
VSS47	AN8	VSS47	
VSS48	AN14	VSS48	
VSS49	AN17	VSS49	
VSS50	AN20	VSS50	
VSS51	AN23	VSS51	
VSS52	AN26	VSS52	
VSS53	AN29	VSS53	
VSS54	AP3	VSS54	
VSS55	AP12	VSS55	
VSS56	AP21	VSS56	
VSS57	AP24	VSS57	
VSS58	AP27	VSS58	
VSS59	AR2	VSS59	
VSS60	AR29	VSS60	
VSS61	AT3	VSS61	
VSS62	AT28	VSS62	
VSS63	AU2	VSS63	
VSS64	AU29	VSS64	

Clocks

- DDR_VREF_0V9 — 1V8 — C158 0.10F; C149 0.10F; C151 0.10F 0402; C152 0.10F 0402; C148 100F 0402
- 5V — 1V8 — C459 4U7F 10V; C456 10UF 10V; C460 10UF 10V; C461 10UF 10V; C462 10UF 10V; C463 10UF 10V; C464 10UF 10V; C465 10UF 10V; C466 10UF 10V; C467 10UF 10V; C468 10UF 10V; C469 10UF 10V; C470 10UF 10V; C471 10UF 10V; C472 10UF 10V; C473 10UF 10V; C474 10UF 10V; C475 10UF 10V; C476 10UF 10V; C477 10UF 10V; C478 10UF 10V; C479 10UF 10V; C480 10UF 10V; C481 10UF 10V; C482 10UF 10V; C483 10UF 10V; C484 10UF 10V; C485 10UF 10V; C486 10UF 10V; C487 10UF 10V; C488 10UF 10V; C489 10UF 10V; C490 10UF 10V; C491 10UF 10V; C492 10UF 10V; C493 10UF 10V; C494 10UF 10V; C495 10UF 10V; C496 10UF 10V; C497 10UF 10V; C498 10UF 10V; C499 10UF 10V; C500 10UF 10V; C501 10UF 10V; C502 10UF 10V; C503 10UF 10V; C504 10UF 10V; C505 10UF 10V; C506 10UF 10V; C507 10UF 10V; C508 10UF 10V; C509 10UF 10V; C510 10UF 10V; C511 10UF 10V; C512 10UF 10V; C513 10UF 10V; C514 10UF 10V; C515 10UF 10V; C516 10UF 10V; C517 10UF 10V; C518 10UF 10V; C519 10UF 10V; C520 10UF 10V; C521 10UF 10V; C522 10UF 10V; C523 10UF 10V; C524 10UF 10V; C525 10UF 10V; C526 10UF 10V; C527 10UF 10V; C528 10UF 10V; C529 10UF 10V; C530 10UF 10V; C531 10UF 10V; C532 10UF 10V; C533 10UF 10V; C534 10UF 10V; C535 10UF 10V; C536 10UF 10V; C537 10UF 10V; C538 10UF 10V; C539 10UF 10V; C540 10UF 10V; C541 10UF 10V; C542 10UF 10V; C543 10UF 10V; C544 10UF 10V; C545 10UF 10V; C546 10UF 10V; C547 10UF 10V; C548 10UF 10V; C549 10UF 10V; C550 10UF 10V; C551 10UF 10V; C552 10UF 10V; C553 10UF 10V; C554 10UF 10V; C555 10UF 10V; C556 10UF 10V; C557 10UF 10V; C558 10UF 10V; C559 10UF 10V; C560 10UF 10V; C561 10UF 10V; C562 10UF 10V; C563 10UF 10V; C564 10UF 10V; C565 10UF 10V; C566 10UF 10V; C567 10UF 10V; C568 10UF 10V; C569 10UF 10V; C570 10UF 10V; C571 10UF 10V; C572 10UF 10V; C573 10UF 10V; C574 10UF 10V; C575 10UF 10V; C576 10UF 10V; C577 10UF 10V; C578 10UF 10V; C579 10UF 10V; C580 10UF 10V; C581 10UF 10V; C582 10UF 10V; C583 10UF 10V; C584 10UF 10V; C585 10UF 10V; C586 10UF 10V; C587 10UF 10V; C588 10UF 10V; C589 10UF 10V; C590 10UF 10V; C591 10UF 10V; C592 10UF 10V; C593 10UF 10V; C594 10UF 10V; C595 10UF 10V; C596 10UF 10V; C597 10UF 10V; C598 10UF 10V; C599 10UF 10V; C600 10UF 10V; C601 10UF 10V; C602 10UF 10V; C603 10UF 10V; C604 10UF 10V; C605 10UF 10V; C606 10UF 10V; C607 10UF 10V; C608 10UF 10V; C609 10UF 10V; C610 10UF 10V; C611 10UF 10V; C612 10UF 10V; C613 10UF 10V; C614 10UF 10V; C615 10UF 10V; C616 10UF 10V; C617 10UF 10V; C618 10UF 10V; C619 10UF 10V; C620 10UF 10V; C621 10UF 10V; C622 10UF 10V; C623 10UF 10V; C624 10UF 10V; C625 10UF 10V; C626 10UF 10V; C627 10UF 10V; C628 10UF 10V; C629 10UF 10V; C630 10UF 10V; C631 10UF 10V; C632 10UF 10V; C633 10UF 10V; C634 10UF 10V; C635 10UF 10V; C636 10UF 10V; C637 10UF 10V; C638 10UF 10V; C639 10UF 10V; C640 10UF 10V; C641 10UF 10V; C642 10UF 10V; C643 10UF 10V; C644 10UF 10V; C645 10UF 10V; C646 10UF 10V; C647 10UF 10V; C648 10UF 10V; C649 10UF 10V; C650 10UF 10V; C651 10UF 10V; C652 10UF 10V; C653 100NF 10V; C21 22PF; C457 10UF 10V; C458 10UF 10V; C329 4U7F 10V; C300 100NF 10V; C63 10NF 25V

Place parts as close to CPU as possible

U32 TPS51100DGQ

VIN	10	1V8
VLDOIN	2	1V8
VDDQSNS	1	1V8
S3	7	1V8
S5	8	1V8
VTT	3	DDR_VTT
VTTSNS	5	DDR_VTT
VTTREF	6	DDR_VREF_0V9
PPAD	11	
GND	9	
PGND	4	

R230 10K; R229 10K; R6 120R

Z_IN

L17 0603 1000OHM 1.5A

VDDQ1	1	1V8
VDDQ2	6	1V8
VDDQ3	15	1V8
VDDQ4	25	1V8
VDDQ5	28	1V8
VDDQ6	31	1V8
VDDQ7	36	1V8

U6 — CDCU877ARHAT

AVDD	8	1V8
AGND	7	GND
OE	22	1V8
OS	21	GND
CLK	4	DDR_PCLKOUT
CLK#	5	DDR_PCLKOUT#
Y0	38	NC
Y0#	37	NC
Y1	39	DDR_PCLKOUT1
Y1#	40	DDR_PCLKOUT1#
Y2	3	NC
Y2#	2	NC
Y3	11	NC
Y3#	12	NC
Y4	14	NC
Y4#	13	NC
Y5	34	NC
Y5#	35	NC
Y6	33	NC
Y6#	32	NC
Y7	29	NC
Y7#	30	NC
Y8	19	DDR_PCLKOUT0
Y8#	18	DDR_PCLKOUT0#
Y9	16	DDR_PCLKOUT2
Y9#	17	DDR_PCLKOUT2#
FBIN	27	FBOUT
FBIN#	26	FBOUT#
OAD1	10	GND
OAD2	41	GND

R168 120R; R169 120R

DDR_PCLKOUT# — DDR_PCLKOUT

Z_OUT

Z_FB

FBOUT# — FBOUT

J8

DDR2_DIMM_CB7	168	PPC_ECC7	
DDR2_DIMM_CB6	167	PPC_ECC6	
DDR2_DIMM_CB5	162	PPC_ECC5	
DDR2_DIMM_CB4	161	PPC_ECC4	
DDR2_DIMM_CB3	49	PPC_ECC3	
DDR2_DIMM_CB2	48	PPC_ECC2	
DDR2_DIMM_CB1	43	PPC_ECC1	
DDR2_DIMM_CB0	42	PPC_ECC0	
DDR2_DIMM_DQ[63]	236	DDR_PDQ63	
DDR2_DIMM_DQ[62]	235	DDR_PDQ62	
DDR2_DIMM_DQ[61]	230	DDR_PDQ61	
DDR2_DIMM_DQ[60]	229	DDR_PDQ60	
DDR2_DIMM_DQ[59]	117	DDR_PDQ59	
DDR2_DIMM_DQ[58]	116	DDR_PDQ58	
DDR2_DIMM_DQ[57]	111	DDR_PDQ57	
DDR2_DIMM_DQ[56]	110	DDR_PDQ56	
DDR2_DIMM_DQ[55]	227	DDR_PDQ55	
DDR2_DIMM_DQ[54]	226	DDR_PDQ54	
DDR2_DIMM_DQ[53]	218	DDR_PDQ53	
DDR2_DIMM_DQ[52]	217	DDR_PDQ52	
DDR2_DIMM_DQ[51]	108	DDR_PDQ51	
DDR2_DIMM_DQ[50]	107	DDR_PDQ50	
DDR2_DIMM_DQ[49]	99	DDR_PDQ49	
DDR2_DIMM_DQ[48]	98	DDR_PDQ48	
DDR2_DIMM_DQ[47]	215	DDR_PDQ47	
DDR2_DIMM_DQ[46]	214	DDR_PDQ46	
DDR2_DIMM_DQ[45]	209	DDR_PDQ45	
DDR2_DIMM_DQ[44]	208	DDR_PDQ44	
DDR2_DIMM_DQ[43]	96	DDR_PDQ43	
DDR2_DIMM_DQ[42]	95	DDR_PDQ42	
DDR2_DIMM_DQ[41]	90	DDR_PDQ41	
DDR2_DIMM_DQ[40]	89	DDR_PDQ40	
DDR2_DIMM_DQ[39]	206	DDR_PDQ39	
DDR2_DIMM_DQ[38]	205	DDR_PDQ38	
DDR2_DIMM_DQ[37]	200	DDR_PDQ37	
DDR2_DIMM_DQ[36]	199	DDR_PDQ36	
DDR2_DIMM_DQ[35]	87	DDR_PDQ35	
DDR2_DIMM_DQ[34]	86	DDR_PDQ34	
DDR2_DIMM_DQ[33]	81	DDR_PDQ33	
DDR2_DIMM_DQ[32]	80	DDR_PDQ32	
DDR2_DIMM_DQ[31]	159	DDR_PDQ31	
DDR2_DIMM_DQ[30]	158	DDR_PDQ30	
DDR2_DIMM_DQ[29]	153	DDR_PDQ29	
DDR2_DIMM_DQ[28]	152	DDR_PDQ28	
DDR2_DIMM_DQ[27]	40	DDR_PDQ27	
DDR2_DIMM_DQ[26]	39	DDR_PDQ26	
DDR2_DIMM_DQ[25]	34	DDR_PDQ25	
DDR2_DIMM_DQ[24]	33	DDR_PDQ24	
DDR2_DIMM_DQ[23]	150	DDR_PDQ23	
DDR2_DIMM_DQ[22]	149	DDR_PDQ22	
DDR2_DIMM_DQ[21]	144	DDR_PDQ21	
DDR2_DIMM_DQ[20]	143	DDR_PDQ20	
DDR2_DIMM_DQ[19]	31	DDR_PDQ19	
DDR2_DIMM_DQ[18]	30	DDR_PDQ18	
DDR2_DIMM_DQ[17]	25	DDR_PDQ17	
DDR2_DIMM_DQ[16]	24	DDR_PDQ16	
DDR2_DIMM_DQ[15]	141	DDR_PDQ15	
DDR2_DIMM_DQ[14]	140	DDR_PDQ14	
DDR2_DIMM_DQ[13]	132	DDR_PDQ13	
DDR2_DIMM_DQ[12]	131	DDR_PDQ12	
DDR2_DIMM_DQ[11]	22	DDR_PDQ11	
DDR2_DIMM_DQ[10]	21	DDR_PDQ10	
DDR2_DIMM_DQ[9]	13	DDR_PDQ9	
DDR2_DIMM_DQ[8]	12	DDR_PDQ8	
DDR2_DIMM_DQ[7]	129	DDR_PDQ7	
DDR2_DIMM_DQ[6]	128	DDR_PDQ6	
DDR2_DIMM_DQ[5]	123	DDR_PDQ5	
DDR2_DIMM_DQ[4]	122	DDR_PDQ4	
DDR2_DIMM_DQ[3]	10	DDR_PDQ3	
DDR2_DIMM_DQ[2]	9	DDR_PDQ2	
DDR2_DIMM_DQ[1]	4	DDR_PDQ1	
DDR2_DIMM_DQ[0]	3	DDR_PDQ0	
DDR2_DIMM_SA2	101		
DDR2_DIMM_SA1	240		
DDR2_DIMM_SA0	239		
DDR2_DIMM_SCL	120	I2C0_SCLK	1-2B,1-5L,1-9B,2-2P,2S-5A
DDR2_DIMM_SDA	119	I2C0_SDATA	1-2B,1-5L,1-9E

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DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA2	22-9D,22-10L
DDR2_DIMM_BA[1]	190	DDR_PBA1	22-9L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-7L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	DDR_PCLKOUT2	
DDR2_DIMM_CK_N[2]	221	DDR_PCLKOUT2#	
DDR2_DIMM_CK_P[1]	137	DDR_PCLKOUT1	
DDR2_DIMM_CK_N[1]	138	DDR_PCLKOUT1#	
DDR2_DIMM_CK_P[0]	185	DDR_PCLKOUT0	
DDR2_DIMM_CK_N[0]	186	DDR_PCLKOUT0#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-8D,22-11L
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-8D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	1-2B,1-2M,24-10F
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D
PAR_OUT	55	PPC_DDR2_ERROR	1
PAR_IN	68	PAR_IN	1

R226 4K7; R227 4K7; PPC_DDR2_RESET_N; C313 5PF 50V; C308 5PF 50V; C455 5PF 50V; TP4; TP5

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

DDR_VTT

DDR_PCKE	22-6K,22-8D	RP24
DDR_PA15		
DDR_PA14		
DDR_PBA2	22-8K,22-8D	
DDR_PA12		RP23
DDR_PA11		
DDR_PA9		
NC		
DDR_PA7		RP22
DDR_PA8		
DDR_PA6		
DDR_PA5		
DDR_PA4		RP21
DDR_PA3		
DDR_PA1		
DDR_PA2		
DDR_PA0		RP25
DDR_PBA1	22-8K,22-8D	
DDR_PA10		
DDR_PBA0	22-8K,22-8D	
DDR_PRAS#	22-7K,22-8D	RP26
DDR_PWE#	22-3K,22-8D	
DDR_PCS0#	22-3K,22-8D	
DDR_PCAS#	22-8K,22-8D	
DDR_PCS1#	22-3K,22-8D	RP19
DDR_PODT0	22-8D	
DDR_PA13		
DDR_PODT1	22-8D	

RP24 CP26; RP23 CP28; RP22 CP29; RP21 CP30; RP25 CP32; RP26 CP31; RP19 CP33; GND

J8

VSS_64	237	VDD_9	187
VSS_63	234	VDD_8	184
VSS_62	231	VDD_7	178
VSS_61	228	VDD_6	172
VSS_60	225	VDD_5	69
VSS_59	222	VDD_4	67
VSS_58	219	VDD_3	64
VSS_57	216	VDD_2	59
VSS_56	213	VDD_1	53
VSS_55	210		
VSS_54	207		
VSS_53	204	VDDQ_11	194
VSS_52	201	VDDQ_10	191
VSS_51	198	VDDQ_9	181
VSS_50	169	VDDQ_8	175
VSS_49	166	VDDQ_7	170
VSS_48	163	VDDQ_6	78
VSS_47	160	VDDQ_5	75
VSS_46	157	VDDQ_4	72
VSS_45	154	VDDQ_3	62
VSS_44	151	VDDQ_2	56
VSS_43	148	VDDQ_1	51
VSS_42	145		
VSS_41	142		
VSS_40	139		
VSS_39	136		
VSS_38	133		
VSS_37	130		
VSS_36	127		
VSS_35	124		
VSS_34	121		
VSS_33	118		
VSS_32	115		
VSS_31	112		
VSS_30	109		
VSS_29	106		
VSS_28	103		
VSS_27	100		
VSS_26	97		
VSS_25	94		
VSS_24	91		
VSS_23	88		
VSS_22	85		
VSS_21	82		
VSS_20	79		
VSS_19	66		
VSS_18	65		
VSS_17	50		
VSS_16	47		
VSS_15	44		
VSS_14	41		
VSS_13	38		
VSS_12	35		
VSS_11	32		
VSS_10	29		
VSS_9	26		
VSS_8	23		
VSS_7	20		
VSS_6	17		
VSS_5	14		
VSS_4	11		
VSS_3	8		
VSS_2	5		
VSS_1	2		

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DDR_VREF_0V9 — VREF 1; 3V3 — VDDSPD 238; 1V8

GND

PowerPC DRAM Interface:

- DDR2 240 pin DIMM
- 72 bit ECC
- Unbuffered and Registered DIMMs supported
- Up to 2GB supported
- CAS Latencies: 2, 2.5 or 3
- Clock Frequencies: 133MHz to 166MHz
- Single Ended Strobes

PPC DDR2 LAYOUT NOTES

ROUTE ALL DDR CLOCKS AS LENGTH MATCHED ONLY - DIFFERENTIAL ROUTING NOT REQUIRED

CLOCK DELAYS MUST ADHERE TO THE FOLLOWING:
Z_IN + Z_OUT - Z_FB = Z_ADDR + 500 ps (+-25 ps)
WHERE:
Z_IN = PROPAGATION DELAY ON DDR_PCLKOUT/DDR_PCLKOUT#
Z_OUT = PROPAGATION DELAY ON DDR_PCLKOUTn/DDR_PCLKOUTn#
Z_FB = PROPAGATION DELAY ON FBOUT/FBOUT#
Z_ADDR = PROPAGATION DELAY ON DDR_PADD[13:0]

DDR_PCLKOUTn/DDR_PCLKOUTn# NETS CAN BE SWAPPED ON CLOCK BUFFER TO EASE ROUTING

ALL DQ, DQS, DM, ADDR, CMD AND CTRL LINES LENGTH MATCHED TO 400 ps
MATCHING WITHIN BYTE LANE: 50 ps
209 ps < TRACE LENGTH < 800 ps

U6 THERMAL TAB TO BE CONNECTED TO GND PLANE WITH THERMAL VIAS

DDR_VREF_0V9 / 1V8 / 1V8 / 1V8

C432 100NF 10V; C433 10NF 25V; C454 100NF 10V; C434 10NF 25V; C439 100NF 10V; C443 10NF 25V; C431 100NF 10V; C444 10NF 25V; C436 100NF 10V; C445 10NF 25V; C435 100NF 10V; C446 10NF 25V

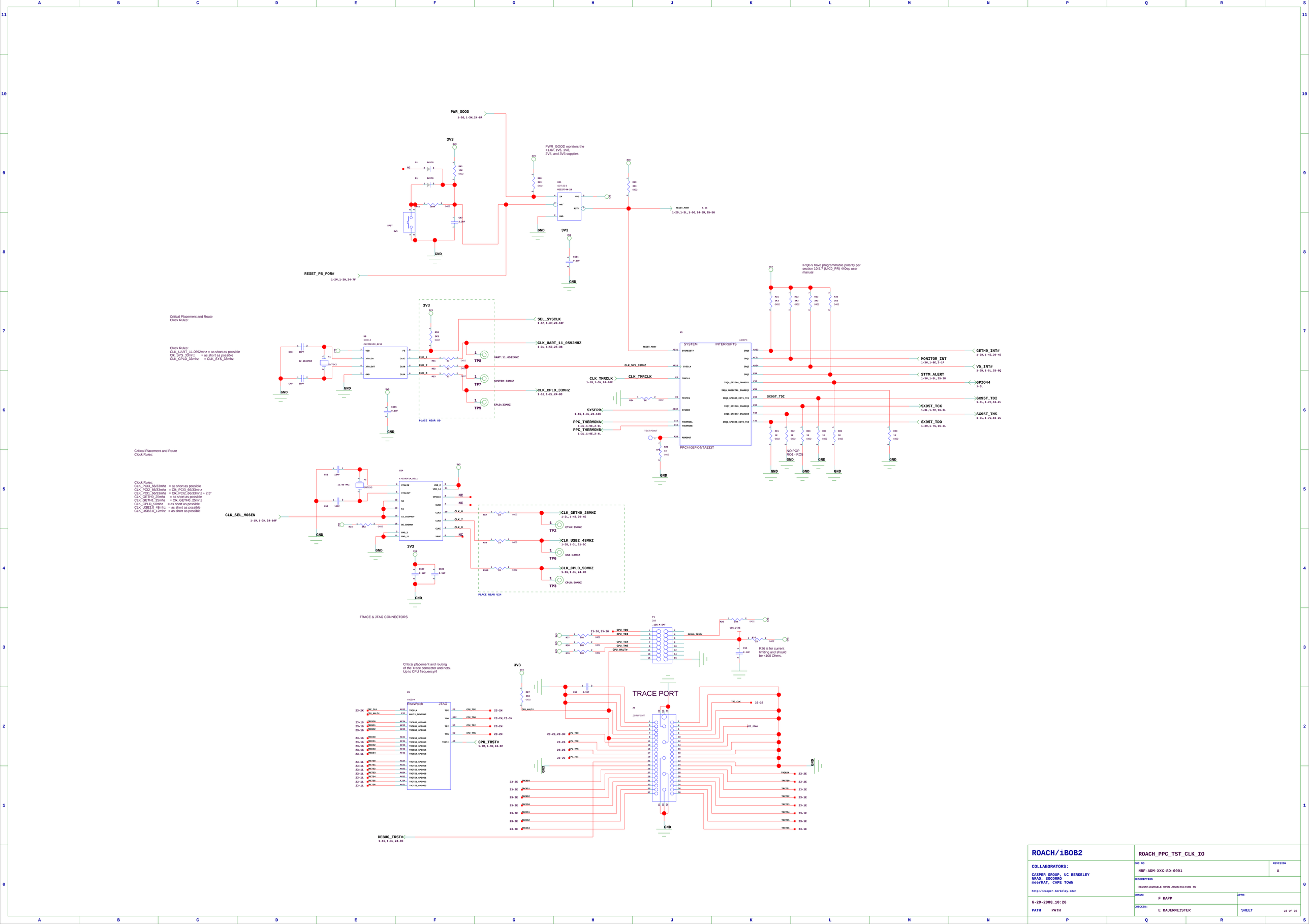
1V8 / 1V8 / 1V8

C438 100NF 10V; C451 10NF 25V; C437 100NF 10V; C452 10NF 25V; C439 100NF 10V; C449 10NF 25V; C440 100NF 10V; C450 10NF 25V; C441 100NF 10V; C448 10NF 25V; C442 100NF 10V; C447 10NF 25V

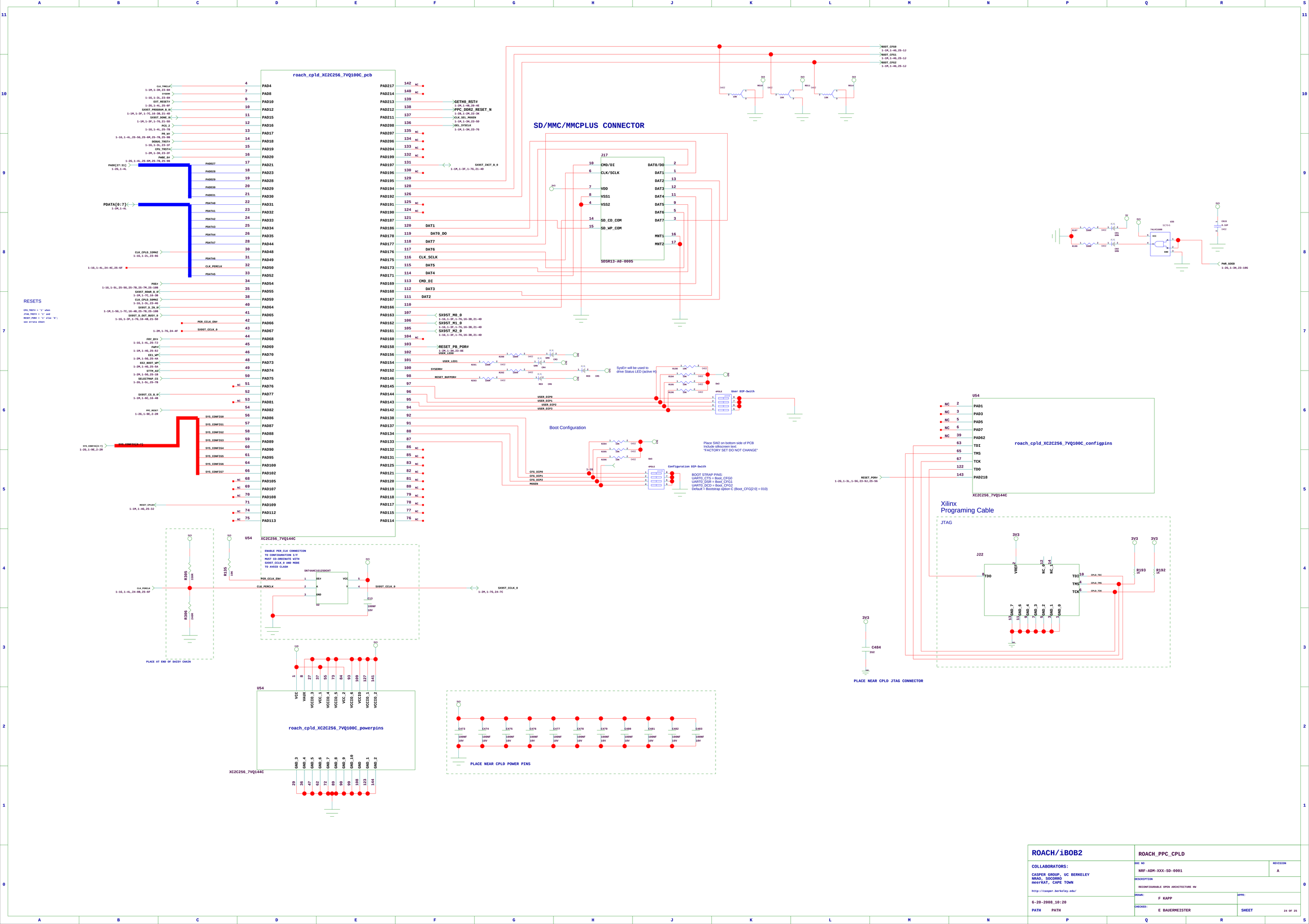
GND

PLACE NEAREST DDR2 MODULE PINS

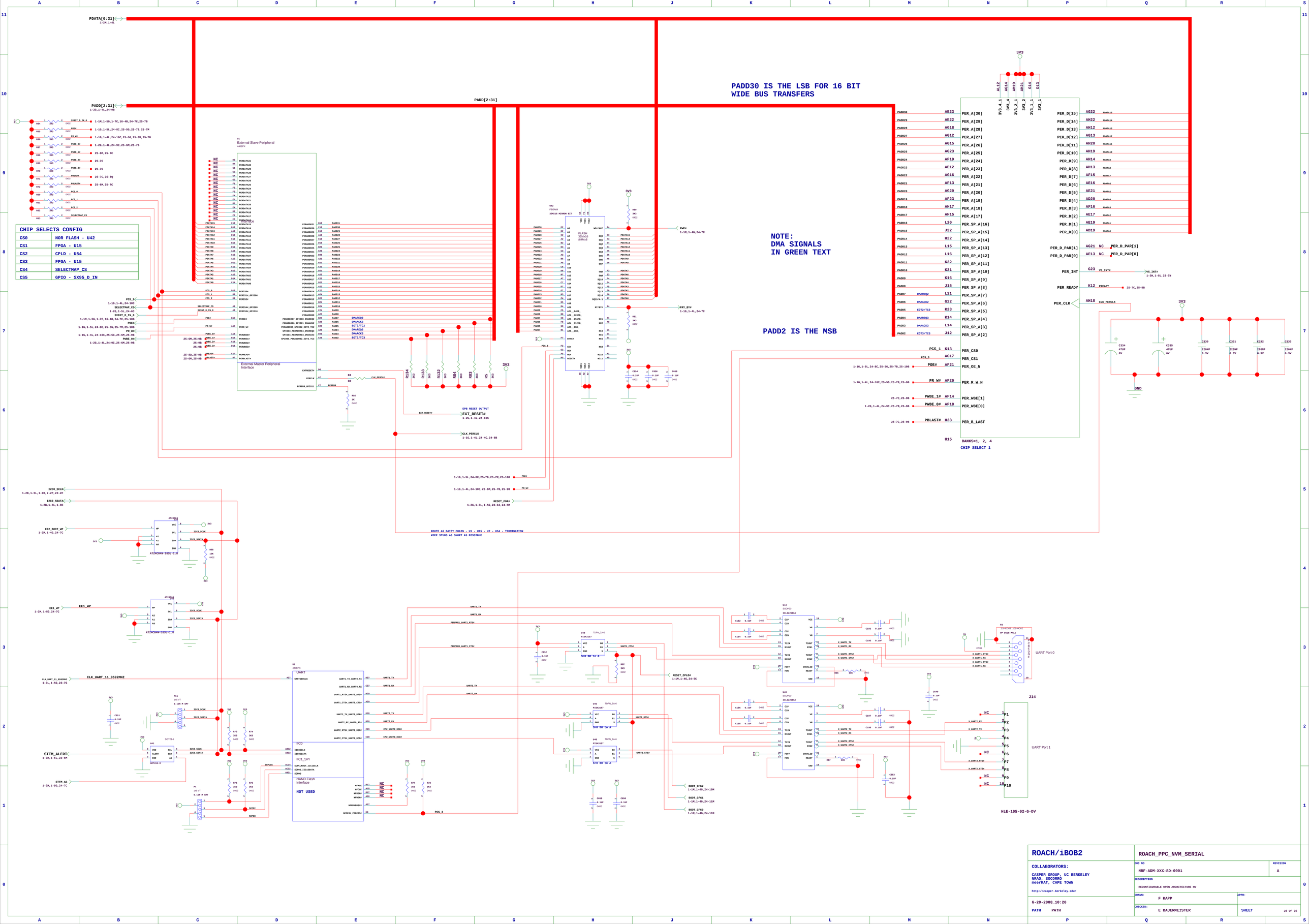
ROACH/iBOB2	ROACH_PPC_DDR2
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A; DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
6-20-2008_10:20	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 22 OF 25



ROACH/iBOB2	**ROACH_PPC_TST_CLK_IO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-20-2008_10:20	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 23 OF 25



ROACH/iBOB2	**ROACH_PPC_CPLD**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-20-2008_10:20	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 24 OF 25



ROACH/iBOB2	ROACH_PPC_NVM_SERIAL
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-20-2008_10:20	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 25 OF 25