VIRTEX5

POWER SUPPLY AND MONITORING

ROACH_MONITOR

1-5I,2-2P,25-5A	I2C0_SCLK	I2C0_SCLK	
1-8E,2-2M,3-10B	FAN2_SENSE	FAN2_SENSE	
1-8E,2-2M,3-10B	FAN1_SENSE	FAN1_SENSE	
1-8E,2-1M,3-9B	FAN3_SENSE	FAN3_SENSE	
1-8E,2-3A,3-6C	3V3_ATX	3V3_ATX	
1-8E,2-2B,3-2H	I2V5	I2V5	
1-8E,2-2B,3-2R	I1V8	I1V8	
1-8E,2-2B,3-5R	I1V5	I1V5	
1-8E,2-1B,3-10R	I1V0	I1V0	
1-8E,2-4A,3-7C	5V_ATX	5V_ATX	
1-9Q,2-B0,19-7P	MGT_AVCC_PG	MGT_AVCC_PG	
1-9Q,2-B0,19-4G	MGT_AVTTX_PG	MGT_AVTTX_PG	
1-9Q,2-B0,19-7G	MGT_AVCCPLL_PG	MGT_AVCCPLL_PG	
1-8E,2-5B,3-7C	PWR_OK	PWR_OK	
1-8E,2-6B,3-6C	12V_ATX	12V_ATX	
	1V0_INHIBIT	1V0_INHIBIT	
		5V9_INHIBIT	1-8B,2-0B,3-9J

2

ROACH_PSU

1-9E,2-6B,3-5B	LOAD_RES_OFF	LOAD_RES_OFF	
1-9E,2-3M,3-10B	FAN1_CONTROL	FAN1_CONTROL	
1-9E,2-5B,3-6G	PS_ONB	PS_ONB	
1-9E,2-2M,3-10B	FAN2_CONTROL	FAN2_CONTROL	
1-9A,2-2M,3-9B	FAN3_CONTROL	FAN3_CONTROL	
1-8E,2-0B,3-9J	1V0_INHIBIT	1V0_INHIBIT	
1-8E,2-1B,3-4J	1V5_INHIBIT	1V5_INHIBIT	
1-8E,2-1B,3-1J	1V8_INHIBIT	1V8_INHIBIT	
1-8E,2-2B,3-3H	2V5_TRACK	2V5_TRACK	
1-8E,2-2B,3-2N	2V5_INHIBIT	2V5_INHIBIT	
		12V_ATX	1-8B,2-6B,3-6C
		3V3_ATX	1-9B,2-3A,3-6C
		5V_ATX	1-8B,2-4A,3-7C
		PWR_OK	1-8B,2-8B,3-7C
		FAN1_SENSE	1-9B,2-2M,3-10B
		FAN2_SENSE	1-9B,2-2M,3-10B
		FAN3_SENSE	1-9B,2-1M,3-9B
		I1V0	1-9B,2-1B,3-10R
		I1V5	1-9B,2-2B,3-5R
		I1V8	1-9B,2-2B,3-2R
		I2V5	1-9B,2-2B,3-2H

3

VIRTEX5 CLOCKS

ROACH_V5_CLK

SX95T_DXN	ATRTN0	
SX95T_DXP	TD0	

7

ZDOK/ADC INTERFACE

ROACH_ADC_0

5

ROACH_ADC_1

6

V5 DDR2 MEMORY

ROACH_DDR2_DIMM

11

V5 DIFFERENTIAL GPIO

ROACH_DIFF_GPIO

12

V5 SE GPIO & MISCELLANEOUS

ROACH_GPIO_MISC

13

GIGABIT TRANSCEIVERS

ROACH_TRANSCEIVERS0_1

8

ROACH_TRANSCEIVERS2_3

9

ROACH_TRANSCEIVERS_PSU

1-9E,2-1M,10-8K	MGT_AVCC_EN	MGT_AVCC_EN	
1-9E,2-1M,10-8B	MGT_AVCCPLL_EN	MGT_AVCCPLL_EN	
1-9E,2-1M,10-5B	MGT_AVTTX_EN	MGT_AVTTX_EN	
		MGT_AVCC_PG	MGT_AVCC_PG
		MGT_AVTTX_PG	MGT_AVTTX_PG
		MGT_AVCCPLL_PG	MGT_AVCCPLL_PG

10

QDRII+ MEMORY

14-5F

ROACH_QDR2P_BY0_1

QDR2_TDI	QDR2_TDI	
QDR2_TCK	QDR2_TCK	
QDR2_THS	QDR2_TMS	
	QDR2_BY0_1_TDO	QDR2_BY0_1_TDO

14

ROACH_QDR2P_BY2_3

QDR2_BY0_1_TDO	QDR2_BY0_1_TDO		
QDR2_THS	QDR2_TMS		
QDR2_TCK	QDR2_TCK		
		QDR2_BY2_3_TDO	QDR2_BY2_3_TDO

15-5H

15

V5 POWER

ROACH_5V_POWER

4

VIRTEX5 CONFIGURATION

ROACH_CONFIG

1-1M,16-4B,24-8C	SX95T_D_IN_0	SX95T_D_IN_0	
1-3L,16-2L,23-6M	SX95T_TCK	SX95T_TCK	
1-3L,16-2L,23-6N	SX95T_TMS	SX95T_TMS	
1-3L,16-2L,23-6R	SX95T_TDI	SX95T_TDI	
1-1M,16-3B,24-8C	SX95T_RDWR_B_0	SX95T_RDWR_B_0	
1-1M,1-3F,16-3B,21-4D,24-10C	SX95T_PROGRAM_B_0	SX95T_PROGRAM_B_0	
1-1M,16-4B,24-6C	SX95T_CS_B_0	SX95T_CS_B_0	
		SX95T_M2_0	1-1G,1-3F,16-3B,21-4D,24-7F
		SX95T_M1_0	1-1G,1-3F,16-3B,21-4D,24-7F
		SX95T_M0_0	1-1G,1-3F,16-3B,21-4D,24-7F
		SX95T_DONE_0	1-1M,1-3F,21-5D
		SX95T_CCLK_0	1-2M,24-4F,24-7C
		SX95T_D_OUT_BUSY_0	1-1G,1-3F,16-4B,21-5D,24-7C
		SX95T_INIT_B_0	1-1M,1-3F,21-4D,24-9F
		SX95T_TDO	1-3H,16-2L,23-6M

16

PPC

MECHANICAL

GND

U3

U49

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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2-27-2008_11:28

PATH PATH

ROACH_TOP

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 1 OF 25

PLACEHOLDER FOR PCB
MEERKAT LOGO

PLACEHOLDER FOR PCB
CASPER LOGO

PLACEHOLDER FOR PCB
NRAO LOGO

BOARD SERIAL NUMBER

CONTRIBUTORS

ETIENNE BAUERMEISTER
HENRY CHEN
STEVE DURAND
FRANCOIS KAPP
ALAN LANDMAN
GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH_PPC_POWER_1

17

ROACH_PPC_POWER_2

18

ROACH_PPC_PCI

19

ROACH_PPC_ETH1

1-2M,20-4E,24-10F	GETH0_RST#	GETH0_RST#	
1-3L,20-4E,23-5G	CLK_GETH0_25MHZ	CLK_GETH0_25MHZ	
		GMCMDIO	GMCMDIO
		GMCMDCLK	GMCMDCLK
		GETH0_INT#	GETH0_INT#
			20-3C,20-4D
			20-3C,20-4D
			1-3M,20-4E,23-7N

20

ROACH_PPC_USB

CONTAINS GPIO TO CONFIG INTERFACE

SX95T_D_OUT_BUSY_0	SX95T_D_OUT_BUSY_0		
SX95T_DONE_0	SX95T_DONE_0		
SX95T_INIT_B_0	SX95T_INIT_B_0		
SX95T_M0_0	SX95T_M0_0		
SX95T_M1_0	SX95T_M1_0		
SX95T_M2_0	SX95T_M2_0		
SX95T_PROGRAM_B_0	SX95T_PROGRAM_B_0		
			1-1G,1-7G,16-4B,21-5D,24-7C
			1-1M,1-7G,21-5D
			1-1M,1-7G,21-4D,24-9F
			1-1G,1-7G,16-3B,21-4D,24-7F
			1-1G,1-7G,16-3B,21-4D,24-7F
			1-1G,1-7G,16-3B,21-4D,24-7F
			1-1M,1-7G,16-3B,21-4D,24-10C
1-3L,21-2C,23-4G	CLK_USB2_48MHZ	CLK_USB2_48MHZ	

21

ROACH_PPC_DDR2

1-2M,22-3K,24-10F	PPC_DDR2_RESET_N	PPC_DDR2_RESET_N

22

ROACH_PPC_TST_CLK_IO

1-4E,20-4E,23-7N	GETH0_INT#	GETH0_INT#	
1-9E,2-1F,23-7M	MONITOR_INT	MONITOR_INT	
1-5L,23-7N,25-8Q	VS_INT#	VS_INT#	
1-5L,23-6M,25-2B	STTM_ALERT	STTM_ALERT	
1-7L,16-2L,23-6M	SX95T_TDO	SX95T_TDO	
1-2M,23-8E,24-7F	RESET_PB_POR#	RESET_PB_POR#	
1-2G,23-1BG,24-8R	PWR_GOOD	PWR_GOOD	
1-2M,23-2F,24-9C	CPU_TRST#	CPU_TRST#	
1-1M,23-5D,24-10F	CLK_SEL_M66EN	CLK_SEL_M66EN	
1-1M,23-7G,24-10F	SEL_SYSCLK	SEL_SYSCLK	
1-1M,23-6B,24-10C	CLK_TMRCLK	CLK_TMRCLK	
		PPC_THERMONA	PPC_THERMONA
		PPC_THERMONB	PPC_THERMONB
		GPIO44	23-6N
		SX95T_TDI	1-7C,16-2L,23-6N
		SX95T_TCK	1-7C,16-2L,23-6M
		SX95T_TMS	1-7C,16-2L,23-6N
		RESET_PORB	1-2G,1-5G,23-5J,24-5M,25-5G
		DEBUG_TRST#	1-1G,23-1F,24-9C
		CLK_GETH0_25MHZ	
		CLK_USB2_48MHZ	1-4B,20-4E,23-5G
		CLK_CPLD_50MHZ	1-3B,21-2C,23-4G
			1-1G,23-4G,24-7C
		SYSERR	1-1G,23-6M,24-10C
		CLK_UART_11_0592MHZ	1-5G,23-7G,25-3D
		CLK_CPLD_33MHZ	1-1G,23-6G,24-8C

23

ROACH_PPC_CPLD

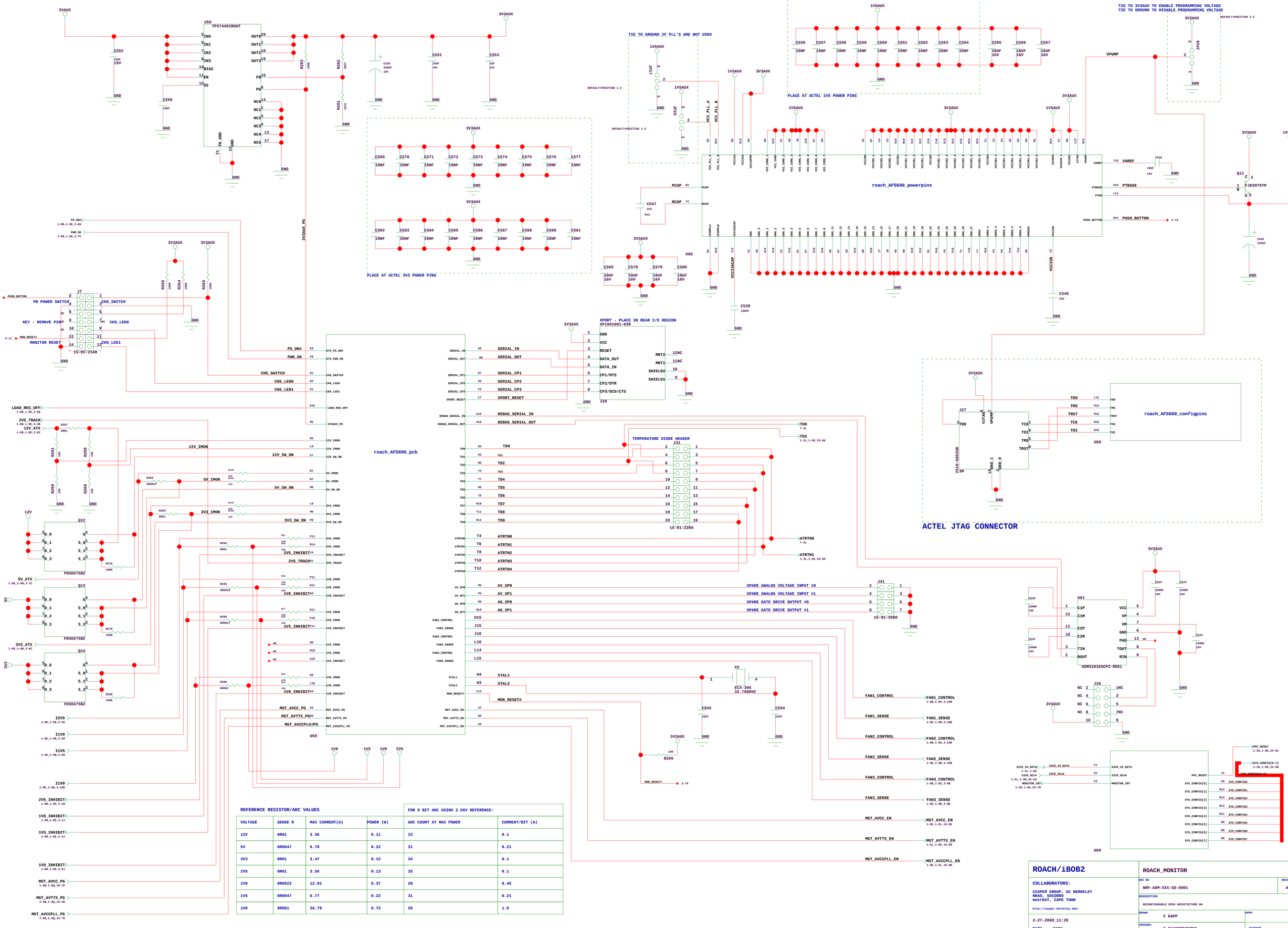
1-9E,2-2B,24-6B	SYS_CONFIG[0:7]	SYS_CONFIG[0:7]	
1-9E,2-2B,24-6C	PPC_RESET	PPC_RESET	
1-3H,23-10G,24-8R	PWR_GOOD	PWR_GOOD	
1-4L,24-10C,25-9F	EXT_RESET#	EXT_RESET#	
1-3L,1-5G,23-9J,24-5M,25-5G	RESET_PORB	RESET_PORB#	
1-4L,24-9C,25-6M,25-7B,25-9B	PWRB_B#	PWRB_B#	
1-4L,24-9B,25-10B	PADD[27:31]	PADD[27:31]	
1-5L,24-8C,25-7B	SELECTMAP_CS	SELECTMAP_CS	
1-4L,24-7C,25-7J	FRY_BY#	FRY_BY#	
1-3L,23-6N,24-10C	SYSERR	SYSERR	
1-2L,23-6L,24-7C	CLK_CPLD_33MHZ	CLK_CPLD_33MHZ	
1-3L,23-1F,24-9C	DEBUG_TRST#	DEBUG_TRST#	
1-4L,24-4C,24-7C,25-6F	CLK_PERCLK	CLK_PERCLK	
1-3L,23-4G,24-7C	CLK_CPLD_50MHZ	CLK_CPLD_50MHZ	
1-4L,24-10C,25-5G,25-6M,25-7B,25-9B	PB_WP	PB_WP	
1-5L,24-8C,25-5G,25-7B,25-7M,25-10B	POE#	POE#	
1-4L,24-10C,25-7B	PCS_2	PCS_2	
1-3F,1-7G,16-4B,21-5D,24-7C	SX95T_D_OUT_BUSY_0	SX95T_D_OUT_BUSY_0	
1-5G,24-5B,25-3B	M66EN	M66EN	
1-3F,1-7G,16-3B,21-4D,24-7F	SX95T_M2_0	SX95T_M0_0	
1-3F,1-7G,16-3B,21-4D,24-7F	SX95T_M1_0	SX95T_M1_0	
1-3F,1-7G,16-3B,21-4D,24-7F	SX95T_M0_0	SX95T_M2_0	
		GETH0_RST#	1-4B,20-4E,24-10F
		PPC_DDR2_RESET_N	1-2B,22-3K,24-10F
		PDATA[0:7]	1-4L
		RESET_PB_POR#	1-3H,23-8E,24-7F
		SX95T_CCLK_0	1-7G,24-4F,24-7C
		STTM_AS	1-5G,24-7C,25-1B
		EE2_BOOT_WP	1-4G,24-7C,25-5A
		EE1_WP	1-5G,24-7C,25-3A
		CPU_TRST#	1-3H,23-2F,24-9C
		SEL_SYSCLK	1-3H,23-7G,24-10F
		CLK_SEL_M66EN	1-3H,23-5D,24-10F
		CLK_TMRCLK	1-3H,23-6M,24-10C
		SX95T_RDWR_B_0	1-7C,16-3B,24-8C
		FWP#	1-4G,24-7C,25-8J
		RESET_CPLD#	1-4G,24-5C,25-3J
		SX95T_INIT_B_0	1-3F,1-7G,21-4D,24-9F
		SX95T_DONE_0	1-3F,1-7G,21-5D
		SX95T_PROGRAM_B_0	1-3F,1-7C,16-3B,21-4D,24-10C
		SX95T_D_IN_0	1-7C,16-4B,24-8C
		SX95T_CS_B_0	1-6C,16-4B,24-6C
		BOOT_CFG0	1-4G,24-11M,25-1J
		BOOT_CFG1	1-4G,24-11M,25-1J
		BOOT_CFG2	1-4G,24-10M,25-1J

24

ROACH_PPC_NVM_SERIAL

1-3L,23-7G,25-3D	CLK_UART_11_0592MHZ	CLK_UART_11_0592MHZ	
1-1G,24-5N,25-3B	M66EN	M66EN	
1-3M,24-7C,25-3A	EE1_WP	EE1_WP	
1-2M,24-7C,25-1B	STTM_AS	STTM_AS	
1-2G,1-3L,23-5J,24-5M,25-5G	RESET_PORB	RESET_PORB#	
1-1M,24-7C,25-8J	FWP#	FWP#	
1-2M,24-7C,25-5A	EE2_BOOT_WP	EE2_BOOT_WP	
1-1M,24-11M,25-1J	BOOT_CFG0	BOOT_CFG0	
1-1M,24-11M,25-1J	BOOT_CFG1	BOOT_CFG1	
1-1M,24-10M,25-1J	BOOT_CFG2	BOOT_CFG2	
1-1M,24-5C,25-3J	RESET_CPLD#	RESET_CPLD#	
		VS_INT#	1-3H,23-7N,25-8Q
		SELECTMAP_CS	1-2G,24-6C,25-7B
		I2C0_SCLK	1-9B,2-2P,25-5A
		I2C0_33_DATA	1-9E
		SCPDI	
		SCPCLK	25-1B
		STTM_ALERT	1-3H,23-6M,25-2B
		SCPDO	25-6B
		POE#	1-1G,24-8C,25-5G,25-7B,25-7M,25-10B
		FRY_BY#	1-1G,24-7C,25-7J
		CLK_PERCLK	1-1G,24-4C,24-7C,25-6F
		PWRE_B#	1-2G,24-9C,25-6M,25-7B,25-9B
		PB_WP	1-1G,24-10C,25-5G,25-6M,25-7B,25-9B
		PCS_2	1-1G,24-10C,25-7B
		PDATA[0:31]	1-2M
		PADD[27:31]	1-2G,24-9B,25-10B
		EXT_RESET#	1-2G,24-10C,25-6F

25



REFERENCE RESISTOR/ADC VALUES				FOR 8 BIT ADC USING 2.56V REFERENCE:	
VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)	ADC COUNT AT MAX POWER	CURRENT/BIT (A)
12V	0R01	3.36	0.11	33	0.1
5V	0R0047	6.78	0.22	31	0.21
3V3	0R01	3.47	0.12	34	0.1
2V5	0R01	3.56	0.13	35	0.1
1V8	0R0022	12.91	0.37	28	0.45
1V5	0R0047	6.77	0.22	31	0.21
1V0	0R001	26.79	0.72	26	1.0

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

2-27-2008, 11:28

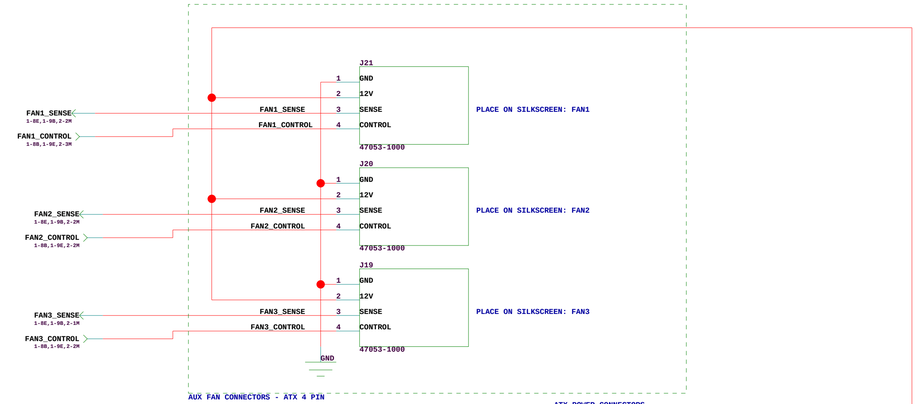
PATH PATH

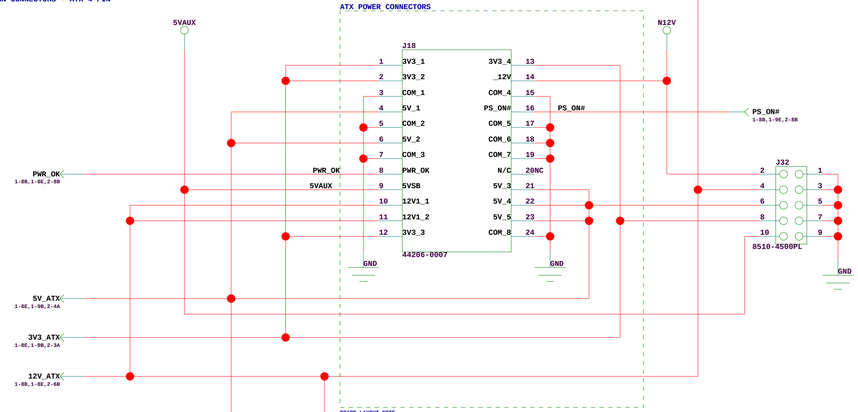
ROACH_MONITOR

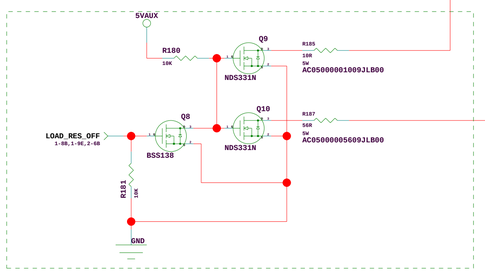
DOC NO	REVISION
NRF-ADM-XXX-SD-0001	A

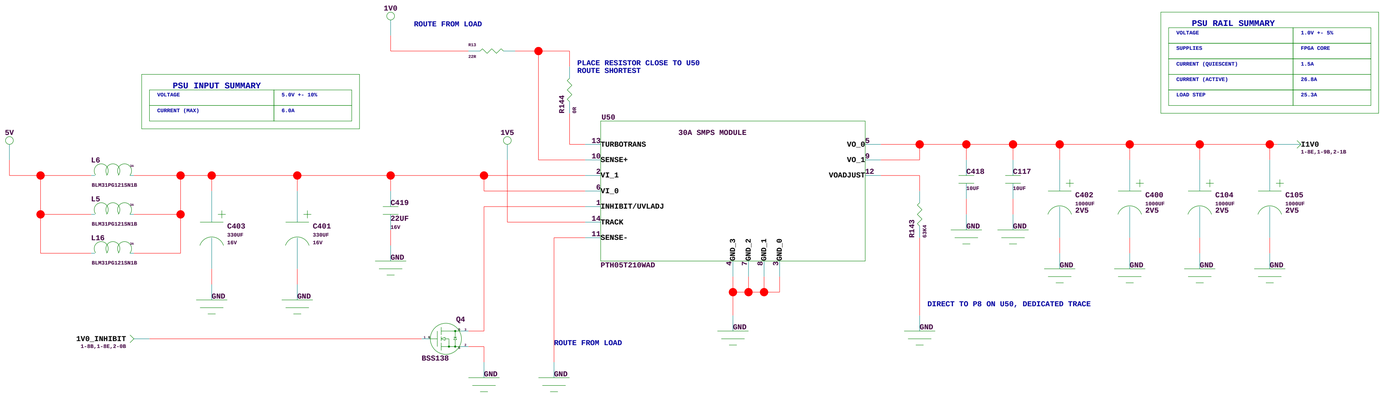
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN:	APPR:
F KAPP	
CHECKED:	SHEET
E BAUERMEISTER	2 OF 25

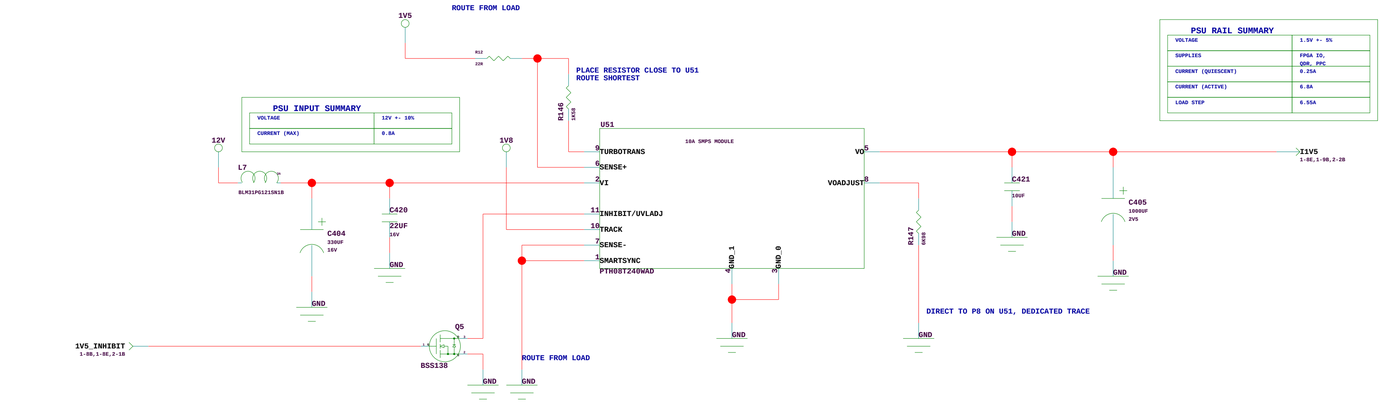


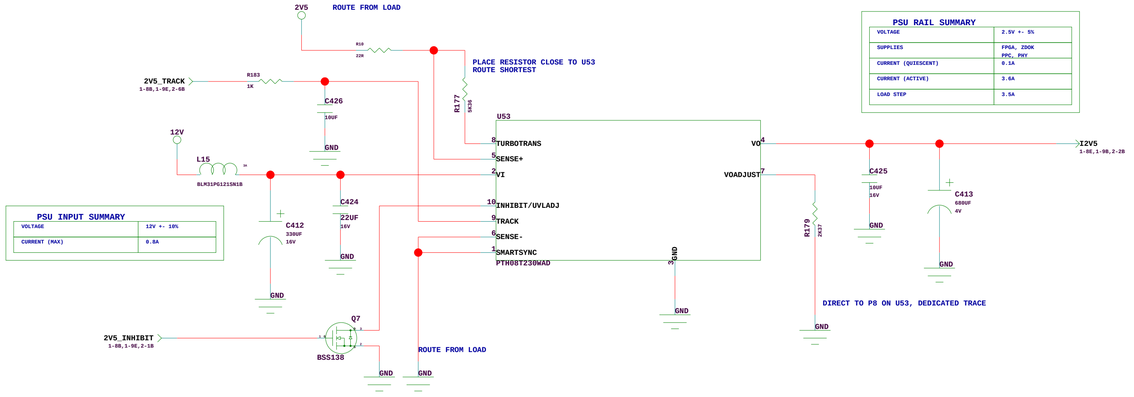


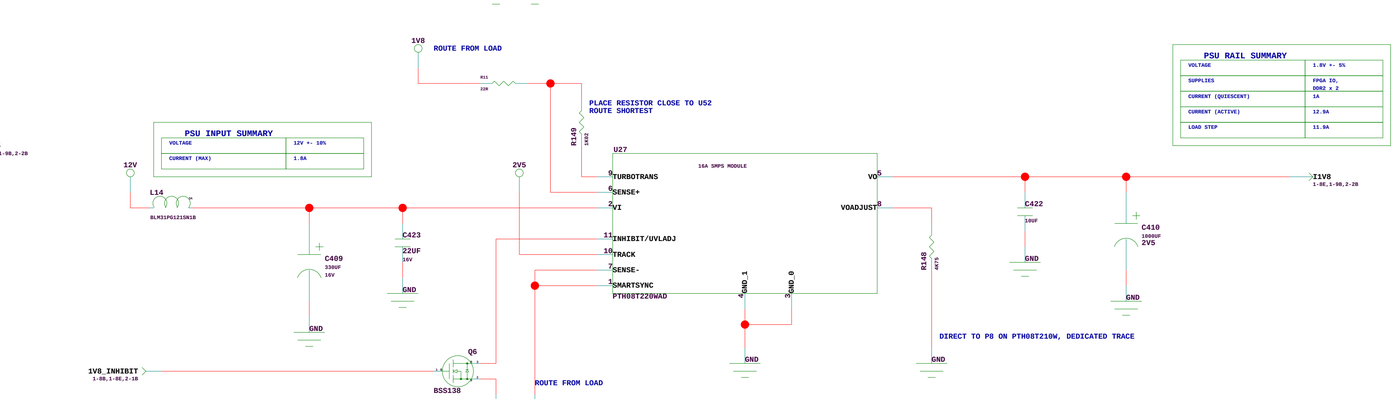




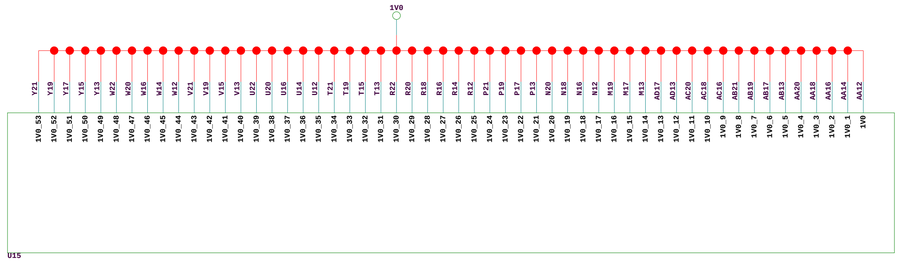
1.2V SUPPLY DELETED - NOT REQUIRED

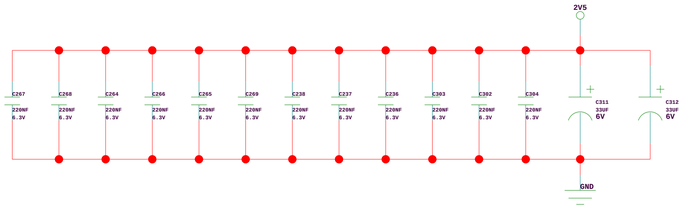


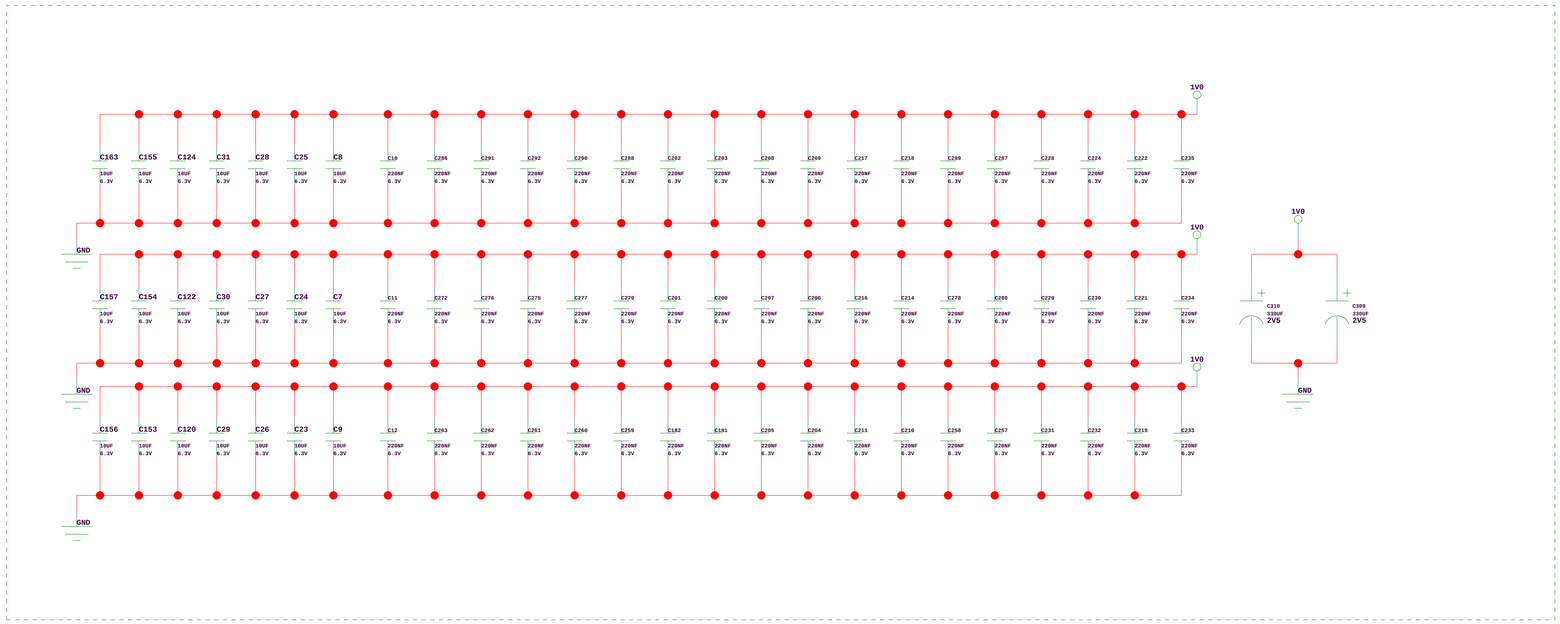


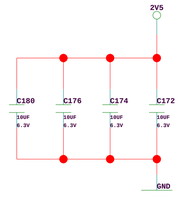


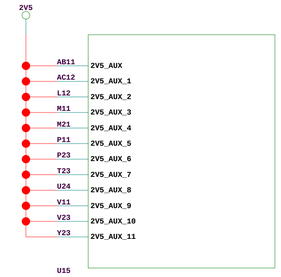
ROACH/iBOB2	**ROACH_PSU**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-27-2008_11:28 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 3 OF 25

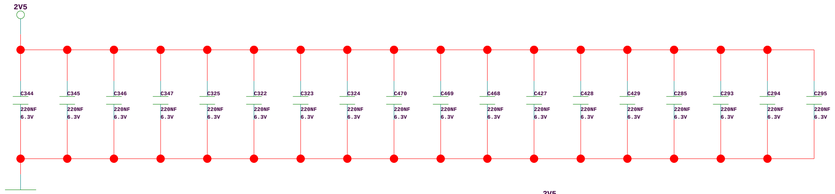


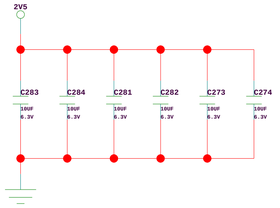


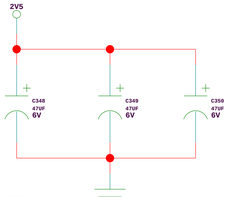


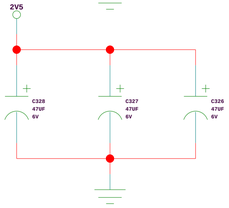


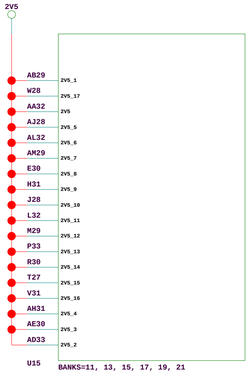


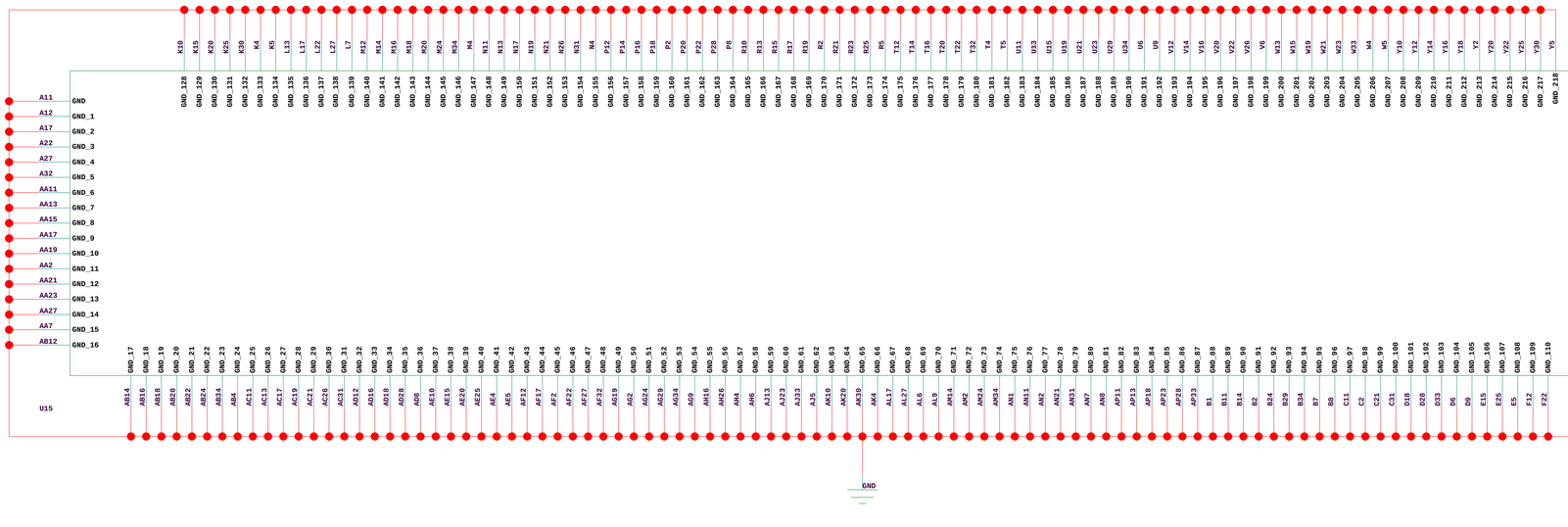












ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE RW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
2-27-2008_11:28 PATH PATH	

| | | |

A	B	C	D	E	F	G	H	J	K	L	M

7													7
6													6
5													5
4													4
3													3
2													2
1													1
0													0

6-5L ZDOK1_CLK0_P H17 → ZDOK1_CLK0_P
6-5L ZDOK1_CLK0_N H18 → ZDOK1_CLK0_N
6-3L ZDOK1_CLK1_P K17 → ZDOK1_CLK1_P
6-3L ZDOK1_CLK1_N L18 → ZDOK1_CLK1_N

ZDOK1_DP_P[37]	AD31	ZDOK1_DP_P37	6-3L
ZDOK1_DP_N[37]	AE31	ZDOK1_DP_N37	6-3L
ZDOK1_DP_P[36]	AF33	ZDOK1_DP_P36	6-3L
ZDOK1_DP_N[36]	AE33	ZDOK1_DP_N36	6-3L
ZDOK1_DP_P[35]	AF31	ZDOK1_DP_P35	6-4L
ZDOK1_DP_N[35]	AG31	ZDOK1_DP_N35	6-4L
ZDOK1_DP_P[34]	AG32	ZDOK1_DP_P34	6-4L
ZDOK1_DP_N[34]	AH32	ZDOK1_DP_N34	6-4L
ZDOK1_DP_P[33]	AG28	ZDOK1_DP_P33	6-4L
ZDOK1_DP_N[33]	AH28	ZDOK1_DP_N33	6-4L
ZDOK1_DP_P[32]	AF24	ZDOK1_DP_P32	6-4L
ZDOK1_DP_N[32]	AG25	ZDOK1_DP_N32	6-4L
ZDOK1_DP_P[31]	AJ30	ZDOK1_DP_P31	6-4L
ZDOK1_DP_N[31]	AH30	ZDOK1_DP_N31	6-4L
ZDOK1_DP_P[30]	AK28	ZDOK1_DP_P30	6-5L
ZDOK1_DP_N[30]	AK27	ZDOK1_DP_N30	6-5L
ZDOK1_DP_P[29]	AK26	ZDOK1_DP_P29	6-5L
ZDOK1_DP_N[29]	AJ27	ZDOK1_DP_N29	6-5L
ZDOK1_DP_P[28]	AB27	ZDOK1_DP_P28	6-5L
ZDOK1_DP_N[28]	AC27	ZDOK1_DP_N28	6-5L
ZDOK1_DP_P[27]	AD30	ZDOK1_DP_P27	6-5L
ZDOK1_DP_N[27]	AC29	ZDOK1_DP_N27	6-5L
ZDOK1_DP_P[26]	AE29	ZDOK1_DP_P26	6-6L
ZDOK1_DP_N[26]	AD29	ZDOK1_DP_N26	6-6L
ZDOK1_DP_P[25]	AG33	ZDOK1_DP_P25	6-6L
ZDOK1_DP_N[25]	AH33	ZDOK1_DP_N25	6-6L
ZDOK1_DP_P[24]	AF29	ZDOK1_DP_P24	6-6L
ZDOK1_DP_N[24]	AF30	ZDOK1_DP_N24	6-6L
ZDOK1_DP_P[23]	AG27	ZDOK1_DP_P23	6-6L
ZDOK1_DP_N[23]	AG26	ZDOK1_DP_N23	6-6L
ZDOK1_DP_P[22]	AK34	ZDOK1_DP_P22	6-6L
ZDOK1_DP_N[22]	AK33	ZDOK1_DP_N22	6-6L
ZDOK1_DP_P[21]	AL34	ZDOK1_DP_P21	6-7L
ZDOK1_DP_N[21]	AL33	ZDOK1_DP_N21	6-7L
ZDOK1_DP_P[20]	AJ25	ZDOK1_DP_P20	6-7L
ZDOK1_DP_N[20]	AH25	ZDOK1_DP_N20	6-7L
ZDOK1_DP_P[19]	AB30	ZDOK1_DP_P19	6-3J
ZDOK1_DP_N[19]	AC30	ZDOK1_DP_N19	6-3J
ZDOK1_DP_P[18]	AC28	ZDOK1_DP_P18	6-3J
ZDOK1_DP_N[18]	AD27	ZDOK1_DP_N18	6-3J
ZDOK1_DP_P[17]	AC25	ZDOK1_DP_P17	6-3J
ZDOK1_DP_N[17]	AC24	ZDOK1_DP_N17	6-3J
ZDOK1_DP_P[16]	AE28	ZDOK1_DP_P16	6-4J
ZDOK1_DP_N[16]	AF28	ZDOK1_DP_N16	6-4J
ZDOK1_DP_P[15]	AD24	ZDOK1_DP_P15	6-4J
ZDOK1_DP_N[15]	AE24	ZDOK1_DP_N15	6-4J
ZDOK1_DP_P[14]	AF25	ZDOK1_DP_P14	6-4J
ZDOK1_DP_N[14]	AF26	ZDOK1_DP_N14	6-4J
ZDOK1_DP_P[13]	AH29	ZDOK1_DP_P13	6-4J
ZDOK1_DP_N[13]	AG30	ZDOK1_DP_N13	6-4J
ZDOK1_DP_P[12]	AH27	ZDOK1_DP_P12	6-4J
ZDOK1_DP_N[12]	AJ26	ZDOK1_DP_N12	6-4J
ZDOK1_DP_P[11]	AM33	ZDOK1_DP_P11	6-5J
ZDOK1_DP_N[11]	AM32	ZDOK1_DP_N11	6-5J
ZDOK1_DP_P[10]	AN32	ZDOK1_DP_P10	6-5J
ZDOK1_DP_N[10]	AP32	ZDOK1_DP_N10	6-5J
ZDOK1_DP_P[9]	AC34	ZDOK1_DP_P9	6-5J
ZDOK1_DP_N[9]	AD34	ZDOK1_DP_N9	6-5J
ZDOK1_DP_P[8]	AD32	ZDOK1_DP_P8	6-5J
ZDOK1_DP_N[8]	AE32	ZDOK1_DP_N8	6-5J
ZDOK1_DP_P[7]	AF34	ZDOK1_DP_P7	6-5J
ZDOK1_DP_N[7]	AE34	ZDOK1_DP_N7	6-5J
ZDOK1_DP_P[6]	AD26	ZDOK1_DP_P6	6-6J
ZDOK1_DP_N[6]	AD25	ZDOK1_DP_N6	6-6J
ZDOK1_DP_P[5]	AE27	ZDOK1_DP_P5	6-6J
ZDOK1_DP_N[5]	AE26	ZDOK1_DP_N5	6-6J
ZDOK1_DP_P[4]	AH34	ZDOK1_DP_P4	6-6J
ZDOK1_DP_N[4]	AJ34	ZDOK1_DP_N4	6-6J
ZDOK1_DP_P[3]	AJ32	ZDOK1_DP_P3	6-6J
ZDOK1_DP_N[3]	AK32	ZDOK1_DP_N3	6-6J
ZDOK1_DP_P[2]	AJ31	ZDOK1_DP_P2	6-6J
ZDOK1_DP_N[2]	AK31	ZDOK1_DP_N2	6-6J
ZDOK1_DP_P[1]	AK29	ZDOK1_DP_P1	6-7J
ZDOK1_DP_N[1]	AJ29	ZDOK1_DP_N1	6-7J
ZDOK1_DP_P[0]	AN34	ZDOK1_DP_P0	6-7J
ZDOK1_DP_N[0]	AN33	ZDOK1_DP_N0	6-7J

U15
BANKS=11, 13, 15, 17, 19, 21

5V
3V3
2V5
1V8

C337 1UF 16V — C336 100NF 10V
C339 1UF 16V — C338 100NF 10V
C340 1UF 16V — C341 100NF 10V
C343 1UF 16V — C342 100NF 10V

P7

W1	W1	B1	B1
X1	X1	B2	B2
Y1	Y1	B3	B3
Z1	Z1	B4	B4
W2	W2	B5	B5
X2	X2	B6	B6
Y2	Y2	B7	B7
Z2	Z2	B8	B8
W3	W3	B9	B9
X3	X3	B10	B10
Y3	Y3	B11	B11
Z3	Z3	B12	B12
W4	W4	B13	B13
X4	X4	B14	B14
Y4	Y4	B15	B15
Z4	Z4	B16	B16
W5	W5	B17	B17
X5	X5	B18	B18
Y5	Y5	B19	B19
Z5	Z5	B20	B20
W6	W6	E1	E1
X6	X6	E2	E2
Y6	Y6	E3	E3
Z6	Z6	E4	E4
		E5	E5
		E6	E6
		E7	E7
		E8	E8
		E9	E9
		E10	E10
		E11	E11
		E12	E12
		E13	E13
		E14	E14
		E15	E15
		E16	E16
		E17	E17
		E18	E18
		E19	E19
		E20	E20

6367550-5
ZDOK40

P7

6-0E	ZDOK1_DP_P0	A1	A1	C1	ZDOK1_DP_P20 6-4E
6-0E	ZDOK1_DP_N0	A2	A2	C2	ZDOK1_DP_N20 6-4E
6-0E	ZDOK1_DP_P1	A3	A3	C3	ZDOK1_DP_P21 6-4E
6-0E	ZDOK1_DP_N1	A4	A4	C4	ZDOK1_DP_N21 6-4E
6-0E	ZDOK1_DP_P2	A5	A5	C5	ZDOK1_DP_P22 6-4E
6-0E	ZDOK1_DP_N2	A6	A6	C6	ZDOK1_DP_N22 6-4E
6-1E	ZDOK1_DP_P3	A7	A7	C7	ZDOK1_DP_P23 6-5E
6-1E	ZDOK1_DP_N3	A8	A8	C8	ZDOK1_DP_N23 6-5E
6-1E	ZDOK1_DP_P4	A9	A9	C9	ZDOK1_DP_P24 6-5E
6-1E	ZDOK1_DP_N4	A10	A10	C10	ZDOK1_DP_N24 6-5E
6-1E	ZDOK1_DP_P5	A11	A11	C11	ZDOK1_DP_P25 6-5E
6-1E	ZDOK1_DP_N5	A12	A12	C12	ZDOK1_DP_N25 6-5E
6-1E	ZDOK1_DP_P6	A13	A13	C13	ZDOK1_DP_P26 6-5E
6-1E	ZDOK1_DP_N6	A14	A14	C14	ZDOK1_DP_N26 6-5E
6-1E	ZDOK1_DP_P7	A15	A15	C15	ZDOK1_DP_P27 6-5E
6-1E	ZDOK1_DP_N7	A16	A16	C16	ZDOK1_DP_N27 6-5E
6-2E	ZDOK1_DP_P8	A17	A17	C17	ZDOK1_DP_P28 6-6E
6-2E	ZDOK1_DP_N8	A18	A18	C18	ZDOK1_DP_N28 6-6E
6-2E	ZDOK1_DP_P9	A19	A19	C19	ZDOK1_CLK0_P 6-7B
6-2E	ZDOK1_DP_N9	A20	A20	C20	ZDOK1_CLK0_N 6-7B
6-2E	ZDOK1_DP_P10	D1	D1	F1	ZDOK1_DP_P29 6-6E
6-2E	ZDOK1_DP_N10	D2	D2	F2	ZDOK1_DP_N29 6-6E
6-2E	ZDOK1_DP_P11	D3	D3	F3	ZDOK1_DP_P30 6-6E
6-2E	ZDOK1_DP_N11	D4	D4	F4	ZDOK1_DP_N30 6-6E
6-2E	ZDOK1_DP_P12	D5	D5	F5	ZDOK1_DP_P31 6-6E
6-2E	ZDOK1_DP_N12	D6	D6	F6	ZDOK1_DP_N31 6-6E
6-3E	ZDOK1_DP_P13	D7	D7	F7	ZDOK1_DP_P32 6-6E
6-3E	ZDOK1_DP_N13	D8	D8	F8	ZDOK1_DP_N32 6-6E
6-3E	ZDOK1_DP_P14	D9	D9	F9	ZDOK1_DP_P33 6-7E
6-3E	ZDOK1_DP_N14	D10	D10	F10	ZDOK1_DP_N33 6-7E
6-3E	ZDOK1_DP_P15	D11	D11	F11	ZDOK1_DP_P34 6-7E
6-3E	ZDOK1_DP_N15	D12	D12	F12	ZDOK1_DP_N34 6-7E
6-3E	ZDOK1_DP_P16	D13	D13	F13	ZDOK1_DP_P35 6-7E
6-3E	ZDOK1_DP_N16	D14	D14	F14	ZDOK1_DP_N35 6-7E
6-3E	ZDOK1_DP_P17	D15	D15	F15	ZDOK1_DP_P36 6-7E
6-3E	ZDOK1_DP_N17	D16	D16	F16	ZDOK1_DP_N36 6-7E
6-4E	ZDOK1_DP_P18	D17	D17	F17	ZDOK1_DP_P37 6-7E
6-4E	ZDOK1_DP_N18	D18	D18	F18	ZDOK1_DP_N37 6-7E
6-4E	ZDOK1_DP_P19	D19	D19	F19	ZDOK1_CLK1_P 6-7B
6-4E	ZDOK1_DP_N19	D20	D20	F20	ZDOK1_CLK1_N 6-7B

6367550-5

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

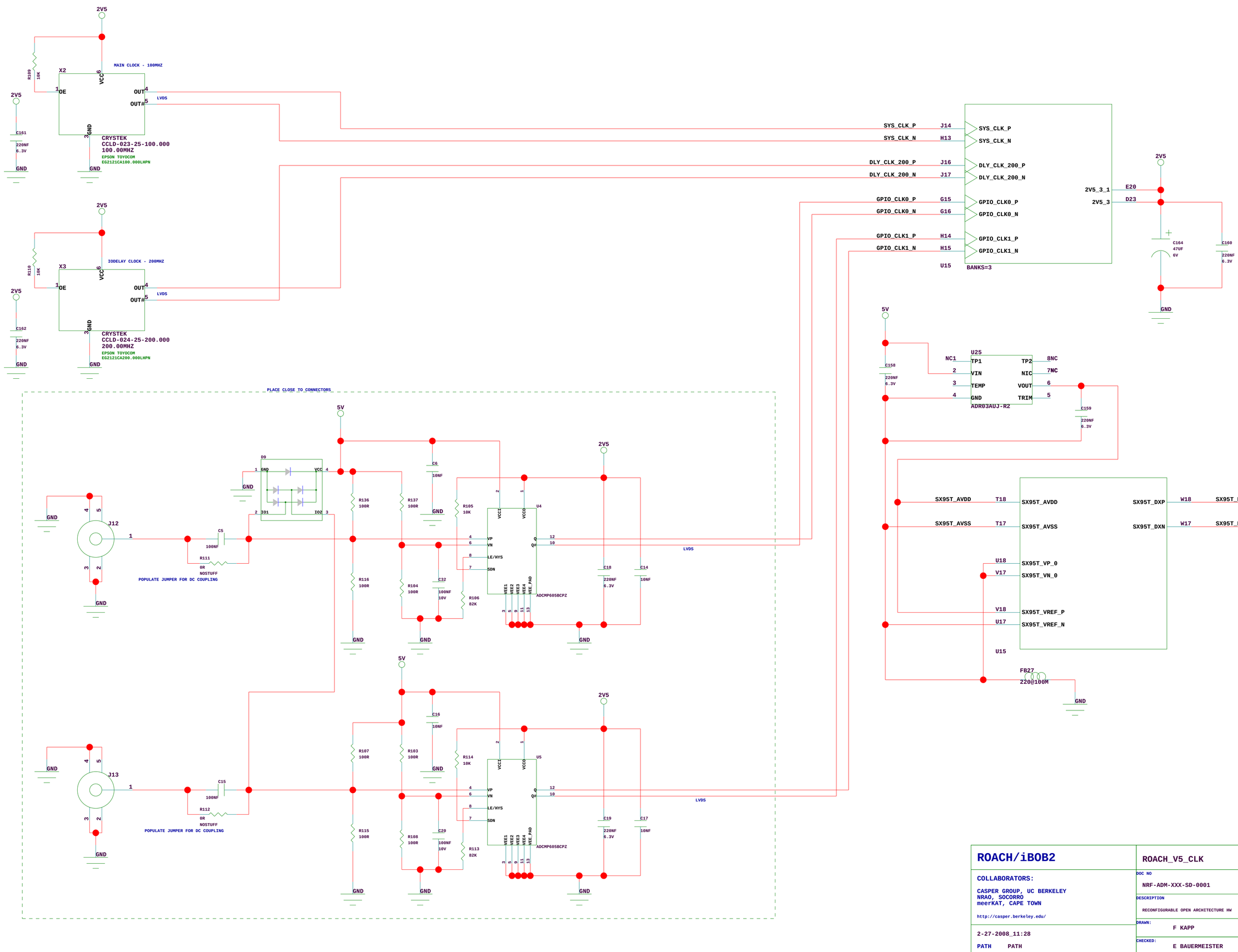
http://casper.berkeley.edu/

2-27-2008_11:28

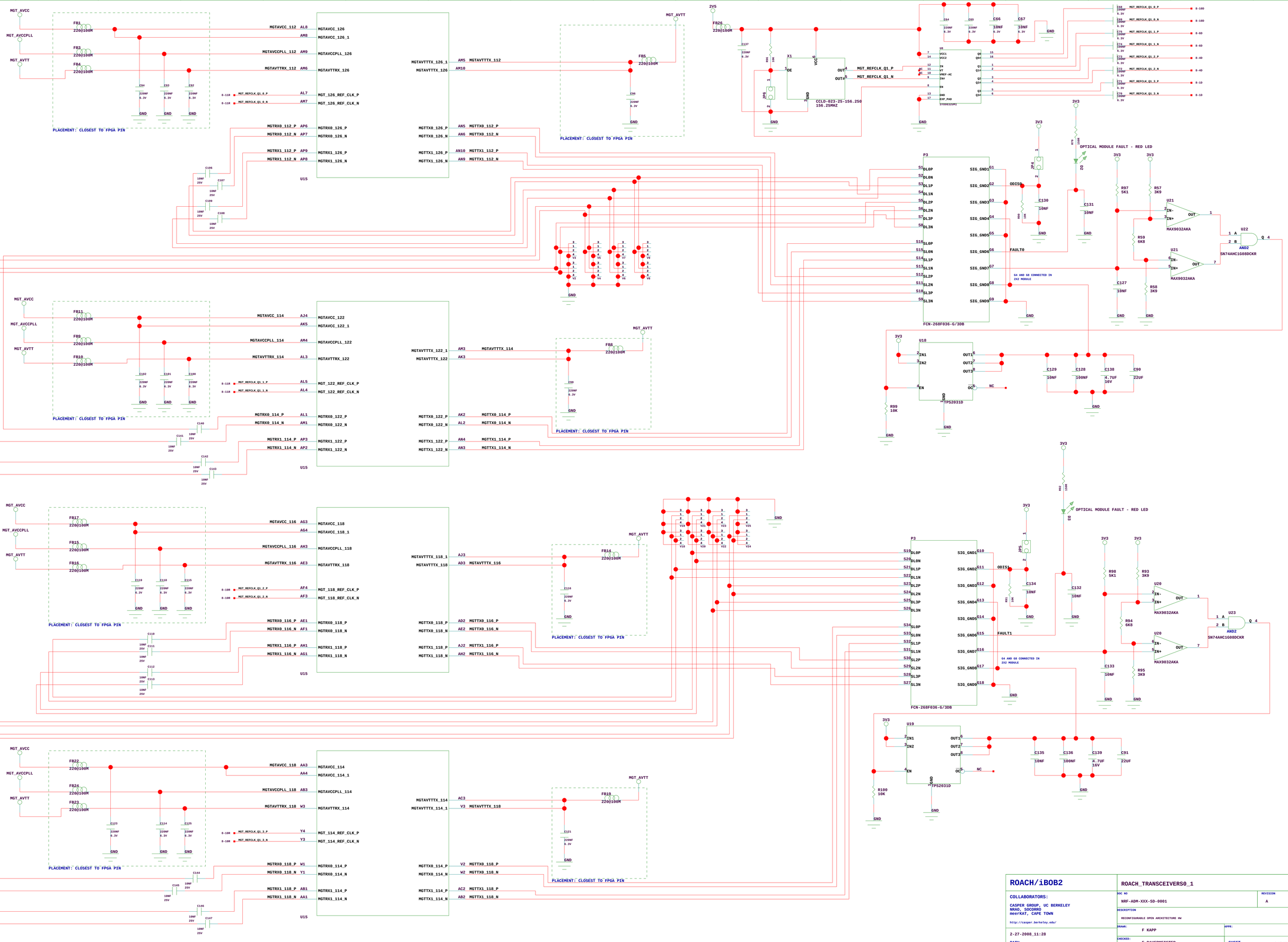
PATH PATH

ROACH_ADC_1

DOC NO: NRF-ADM-XXX-SD-0001
REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 6 OF 25



ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
2-27-2008_11:28 PATH PATH	



ROACH/iBOB2	**ROACH_TRANSCEIVERS0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-27-2008_11:28	DRAWN: F KAPP
PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET: 8 OF 25

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

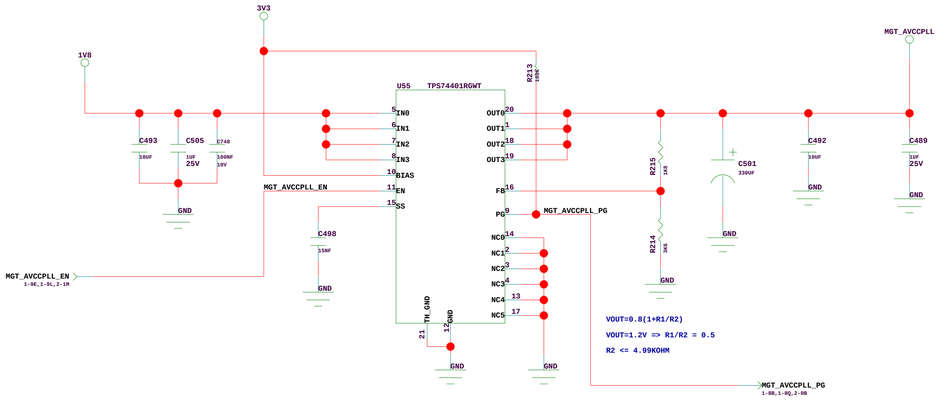
G4 AND G8 CONNECTED IN
2X2 MODULE

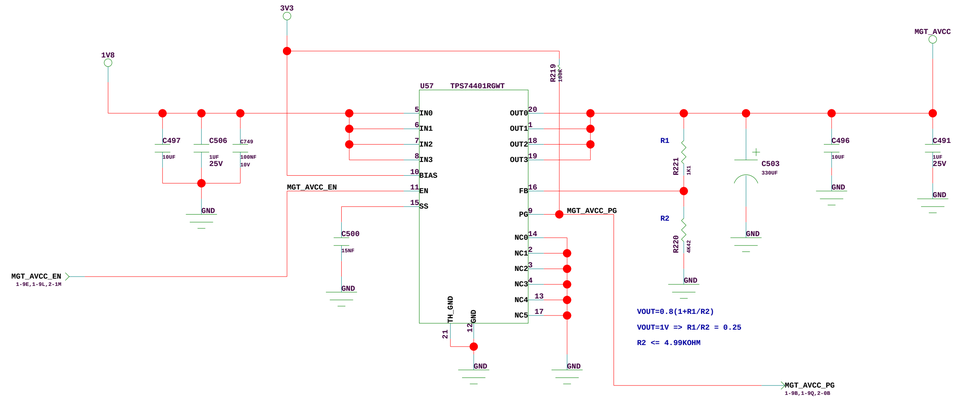
OPTICAL MODULE FAULT - RED LED

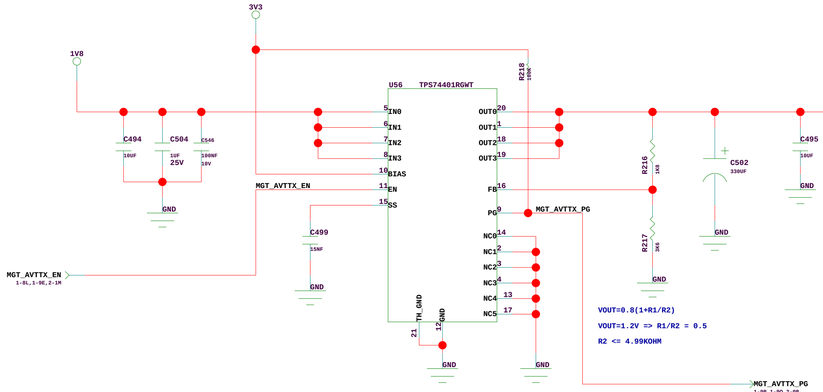
CCLD-023-25-156.250
156.25MHZ

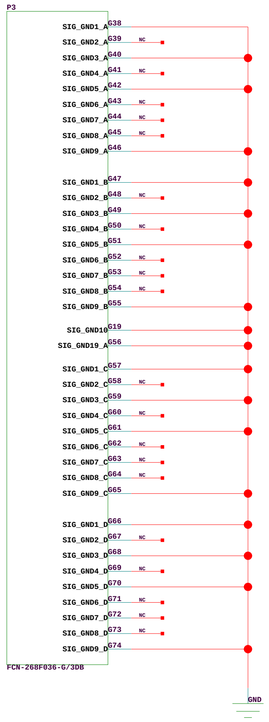
FCN-268F036-G/3DB

ROACH/iBOB2	ROACH_TRANSCEIVERS2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-27-2008_11:28	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 9 OF 25

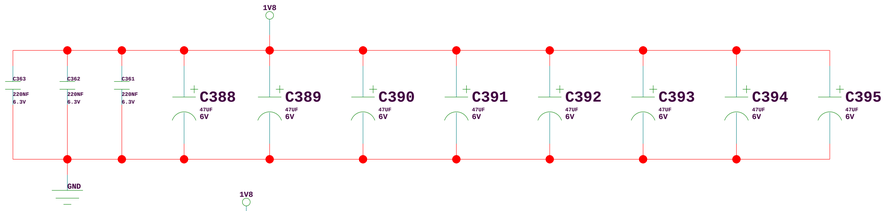


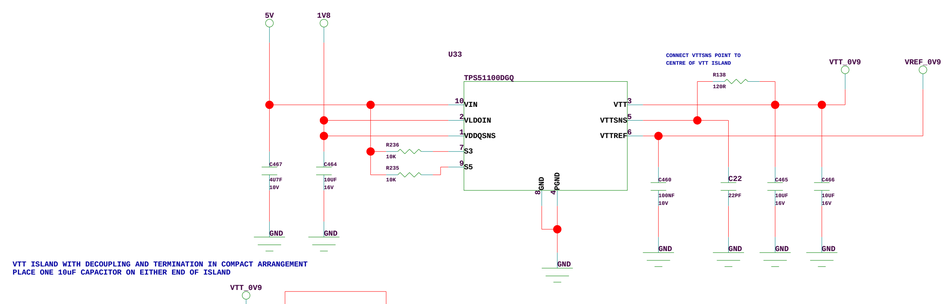


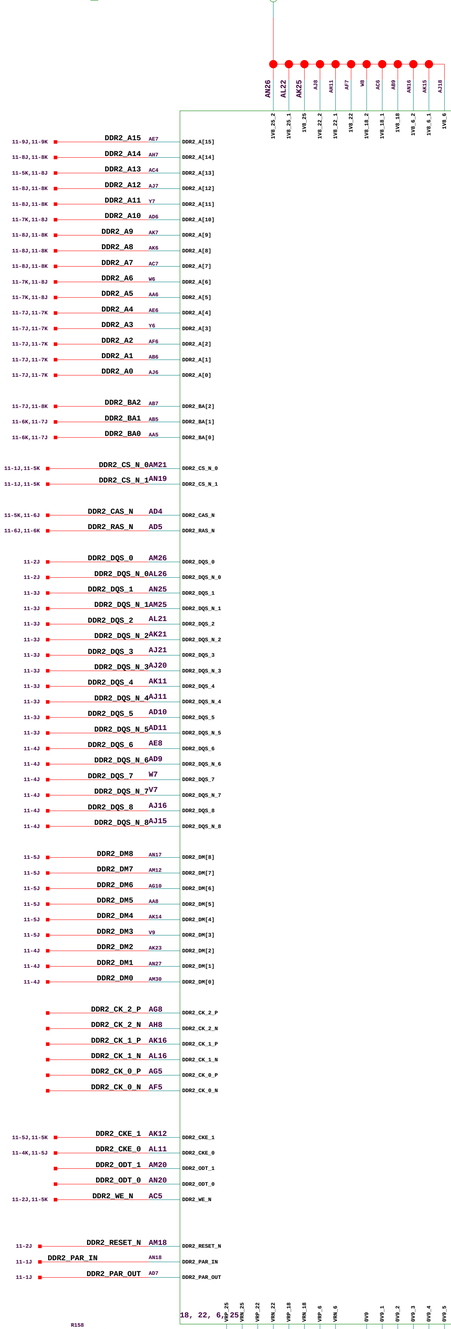


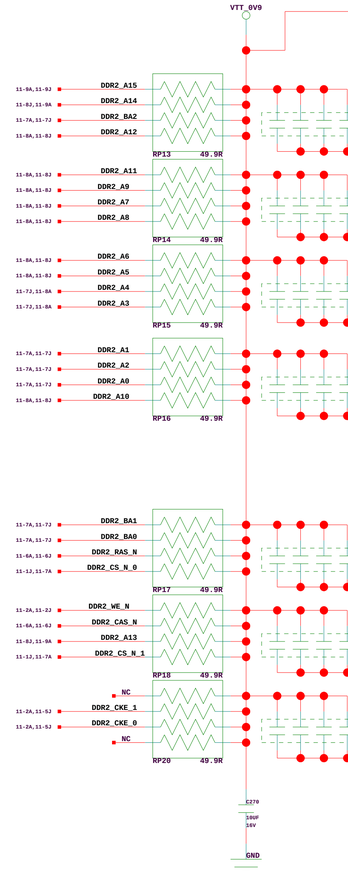


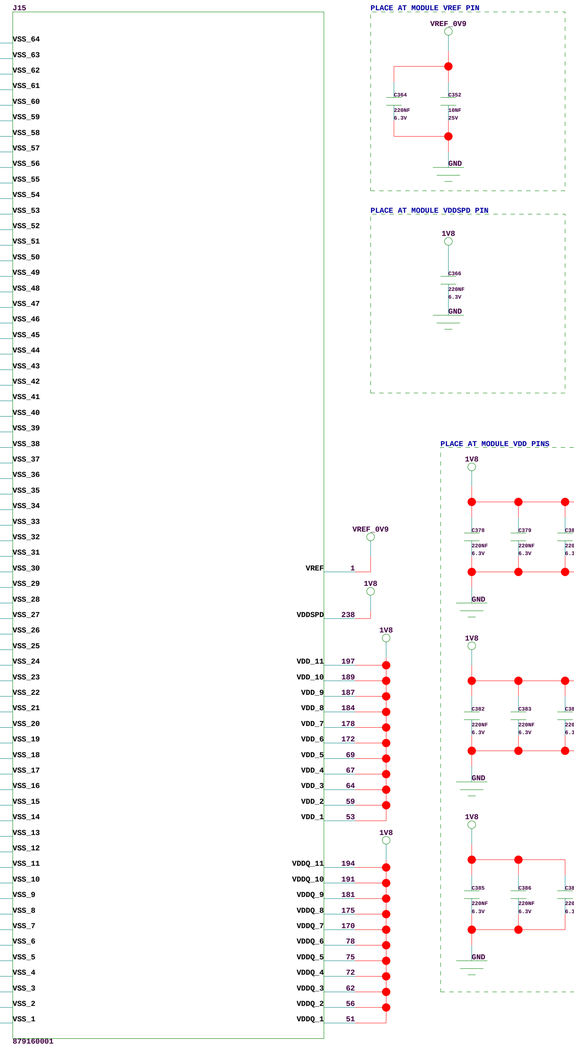
ROACH/iBOB2	ROACH_TRANSCEIVERS_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-27-2008_11:28	DRAWN: F KAPP · APPR:
PATH PATH	CHECKED: E BAUERMEISTER · SHEET 10 OF 25

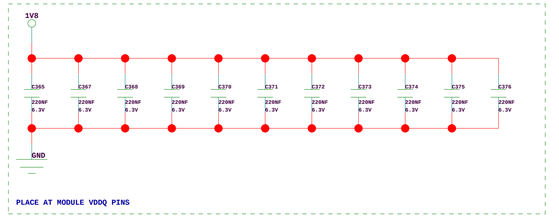












ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

2-27-2008_11:28

PATH PATH

ROACH_DDR2_DIMM

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

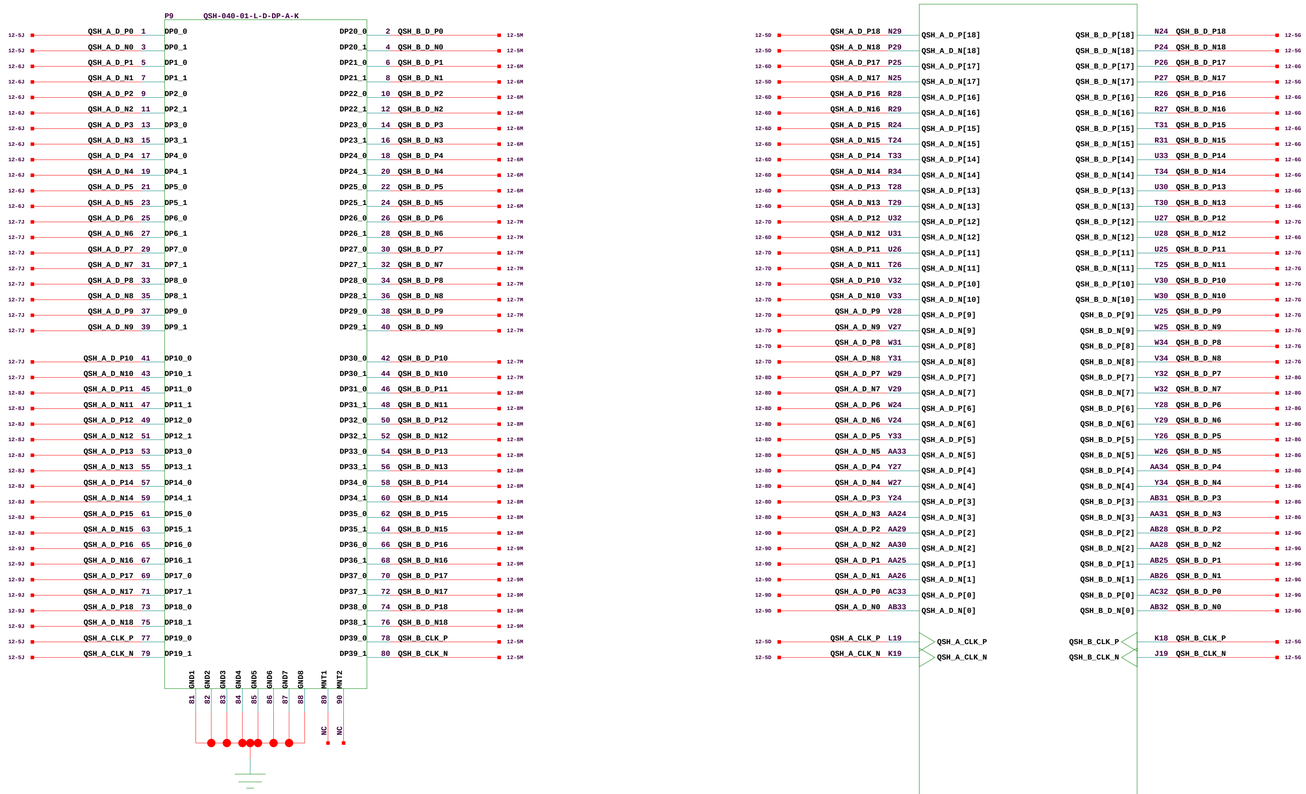
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE NW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 11 OF 25



ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

2-27-2008_11:28

PATH PATH

ROACH_DIFF_GPIO

DOC NO: NRF-ADM-XXX-SD-0001
REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 12 OF 25

GPIOLVC18[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

GPIOLVC25[0] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

IO VOLTAGE LEVEL SELECT	
1-2: 3.3V	DEFAULT
2-3: 2.5V	

IF CR58 IS ON, CLOCK CAPABLE GPIO'S ARE OUTPUTS

ROACH/iBOB2	ROACH_GPIO_MISC
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
2-27-2008_11:28 PATH PATH	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MM
	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 13 OF 25

VTT_QDR_BY0_1

RP28 51R
RP29 51R
RP30 51R
RP31 51R
RP32 51R
RP27 51R
RP33 51R
RP34 51R
RP35 51R
RP36 51R
RP37 51R
RP38 51R

CP41 CP42 CP43 CP44 CP45 CP46 CP47 CP48 CP49 CP50 CP51 CP52

GND

14-8J,14-9F QDR2_BY0_1_K_P
14-8F,14-8J QDR2_BY0_1_K_N
14-8F,14-8J QDR2_BY1_BW
14-5F,14-5J QDR2_BY0_1_SA2
14-5F,14-5J QDR2_BY0_1_SA1
14-5J,14-6F QDR2_BY0_1_SA3
14-8F,14-8J QDR2_BY0_1_R
14-8F,14-8J QDR2_BY0_BW
14-5J,14-6F QDR2_BY0_1_SA4
14-10F,14-10N QDR2_BY0_1_D10
14-10F,14-10N QDR2_BY0_1_D8
14-7F,14-7J QDR2_BY0_1_SA19
14-9F,14-9N QDR2_BY0_1_D6
14-10F,14-10N QDR2_BY0_1_D11
14-6F,14-6J QDR2_BY0_1_SA5
14-10F,14-10N QDR2_BY0_1_D7
14-9F,14-9N QDR2_BY0_1_D4
14-10F,14-10N QDR2_BY0_1_D13
14-9F,14-9N QDR2_BY0_1_D5
14-10F,14-10N QDR2_BY0_1_D12
14-8F,14-8J QDR2_BY0_1_W
14-10F,14-10N QDR2_BY0_1_D9
14-5F,14-5J QDR2_BY0_1_SA0
14-7F,14-7J QDR2_BY0_1_SA20
14-9F,14-9N QDR2_BY0_1_D2
14-10F,14-10N QDR2_BY0_1_D15
14-9F,14-9N QDR2_BY0_1_D3
14-10F,14-10N QDR2_BY0_1_D14
14-6F,14-6J QDR2_BY0_1_SA7
14-6F,14-6J QDR2_BY0_1_SA8
14-9F,14-9N QDR2_BY0_1_D1
14-10F,14-10N QDR2_BY0_1_D16
14-6J,14-7F QDR2_BY0_1_SA13
14-6J,14-7F QDR2_BY0_1_SA14
14-6F,14-6J QDR2_BY0_1_SA9
14-7F,14-7J QDR2_BY0_1_SA15
14-6F,14-6J QDR2_BY0_1_SA10
NC
14-7F,14-7J QDR2_BY0_1_SA16
14-6F,14-6J QDR2_BY0_1_SA11
14-7F,14-7J QDR2_BY0_1_SA17
14-6F,14-6J QDR2_BY0_1_SA12
14-7F,14-7J QDR2_BY0_1_SA18
14-9F,14-9N QDR2_BY0_1_D0
14-7J QDR2_BY0_1_SA21
NC
14-11F,14-11N QDR2_BY0_1_D17
14-6F,14-6J QDR2_BY0_1_SA6

U63

14-4C,14-11N	QDR2_BY0_1_D17	N2	D17
14-6C,14-10N	QDR2_BY0_1_D16	M3	D16
14-7C,14-10N	QDR2_BY0_1_D15	L3	D15
14-7C,14-10N	QDR2_BY0_1_D14	J3	D14
14-8C,14-10N	QDR2_BY0_1_D13	G2	D13
14-8C,14-10N	QDR2_BY0_1_D12	F3	D12
14-9C,14-10N	QDR2_BY0_1_D11	D2	D11
14-9C,14-10N	QDR2_BY0_1_D10	C3	D10
14-8C,14-10N	QDR2_BY0_1_D9	B3	D9
14-9C,14-10N	QDR2_BY0_1_D8	C11	D8
14-8C,14-10N	QDR2_BY0_1_D7	D11	D7
14-9C,14-9N	QDR2_BY0_1_D6	E10	D6
14-8C,14-9N	QDR2_BY0_1_D5	G11	D5
14-8C,14-9N	QDR2_BY0_1_D4	J11	D4
14-7C,14-9N	QDR2_BY0_1_D3	K10	D3
14-7C,14-9N	QDR2_BY0_1_D2	M11	D2
14-6C,14-9N	QDR2_BY0_1_D1	N11	D1
14-4C,14-9N	QDR2_BY0_1_D0	P10	D0

QDR2P_CTRL_DATA

14-8J,14-10C	QDR2_BY0_1_K_P	B6	K
14-8J,14-10C	QDR2_BY0_1_K_N	A6	K#
14-9F	QDR2_BY0_1_QVLD	P6	QVLD
14-5J	QDR2_BY0_1_DLL_OFF	H1	DLL_OFF#
14-8C,14-8J	QDR2_BY0_1_W	A4	W#
14-8J,14-10C	QDR2_BY0_1_R	A8	R#
14-8J,14-10C	QDR2_BY0_BW	B7	BW0#
14-8J,14-10C	QDR2_BY1_BW	A5	BW1#
	R304 240R	H11	ZQ
14-7C,14-7J	QDR2_BY0_1_SA20	A2	SA20
14-7J,14-9C	QDR2_BY0_1_SA19	A10	SA19
14-4C,14-7J	QDR2_BY0_1_SA18	R9	SA18
14-5C,14-7J	QDR2_BY0_1_SA17	R8	SA17
14-5C,14-7J	QDR2_BY0_1_SA16	R7	SA16
14-5C,14-7J	QDR2_BY0_1_SA15	R5	SA15
14-6C,14-8J	QDR2_BY0_1_SA14	R4	SA14
14-6C,14-8J	QDR2_BY0_1_SA13	R3	SA13
14-5C,14-8J	QDR2_BY0_1_SA12	P8	SA12
14-5C,14-8J	QDR2_BY0_1_SA11	P7	SA11
14-5C,14-8J	QDR2_BY0_1_SA10	P5	SA10
14-6C,14-8J	QDR2_BY0_1_SA9	P4	SA9
14-6C,14-8J	QDR2_BY0_1_SA8	N7	SA8
14-6C,14-8J	QDR2_BY0_1_SA7	N6	SA7
14-4C,14-8J	QDR2_BY0_1_SA6	N5	SA6
14-6J,14-9C	QDR2_BY0_1_SA5	C7	SA5
14-5J,14-9C	QDR2_BY0_1_SA4	C5	SA4
14-5J,14-10C	QDR2_BY0_1_SA3	B8	SA3
14-5J,14-10C	QDR2_BY0_1_SA2	B4	SA2
14-5J,14-10C	QDR2_BY0_1_SA1	A9	SA1
14-5J,14-7C	QDR2_BY0_1_SA0	A3	SA0

TP9

QDR2_TDI 1-BL → R11 QDR2_TDI
QDR2_TMS 15-5F → R10 QDR2_TMS
QDR2_TCK 15-5F → R2 QDR2_TCK
R134 10K

U63

TDI	R1	QDR2_BY0_1_TDO 15-5F
TMS		
TCK		

QDR2P_JTAG

Q17	P3	QDR2_BY0_1_Q17	14-11J
Q16	N3	QDR2_BY0_1_Q16	14-10J
Q15	L2	QDR2_BY0_1_Q15	14-10J
Q14	K3	QDR2_BY0_1_Q14	14-10J
Q13	G3	QDR2_BY0_1_Q13	14-10J
Q12	F2	QDR2_BY0_1_Q12	14-10J
Q11	E3	QDR2_BY0_1_Q11	14-10J
Q10	D3	QDR2_BY0_1_Q10	14-10J
Q9	B2	QDR2_BY0_1_Q9	14-10J
Q8	B11	QDR2_BY0_1_Q8	14-10J
Q7	C10	QDR2_BY0_1_Q7	14-10J
Q6	E11	QDR2_BY0_1_Q6	14-9J
Q5	F11	QDR2_BY0_1_Q5	14-9J
Q4	J10	QDR2_BY0_1_Q4	14-9J
Q3	K11	QDR2_BY0_1_Q3	14-9J
Q2	L11	QDR2_BY0_1_Q2	14-9J
Q1	M10	QDR2_BY0_1_Q1	14-9J
Q0	P11	QDR2_BY0_1_Q0	14-9J

CQ	A11	QDR2_BY0_1_CQ_P	14-9J
CQ#	A1	QDR2_BY0_1_CQ_N	14-9J

14-11J	QDR2_BY0_1_Q17 J11	QDR2_BY0_1_Q[17]
14-10J	QDR2_BY0_1_Q16 K11	QDR2_BY0_1_Q[16]
14-10J	QDR2_BY0_1_Q15 F9	QDR2_BY0_1_Q[15]
14-10J	QDR2_BY0_1_Q14 E8	QDR2_BY0_1_Q[14]
14-10J	QDR2_BY0_1_Q13 G8	QDR2_BY0_1_Q[13]
14-10J	QDR2_BY0_1_Q12 N10	QDR2_BY0_1_Q[12]
14-10J	QDR2_BY0_1_Q11 L9	QDR2_BY0_1_Q[11]
14-10J	QDR2_BY0_1_Q10 N9	QDR2_BY0_1_Q[10]
14-10J	QDR2_BY0_1_Q9 M8	QDR2_BY0_1_Q[9]
14-10J	QDR2_BY0_1_Q8 H8	QDR2_BY0_1_Q[8]
14-10J	QDR2_BY0_1_Q7 M10	QDR2_BY0_1_Q[7]
14-9J	QDR2_BY0_1_Q6 F8	QDR2_BY0_1_Q[6]
14-9J	QDR2_BY0_1_Q5 H9	QDR2_BY0_1_Q[5]
14-9J	QDR2_BY0_1_Q4 H10	QDR2_BY0_1_Q[4]
14-9J	QDR2_BY0_1_Q3 G10	QDR2_BY0_1_Q[3]
14-9J	QDR2_BY0_1_Q2 F10	QDR2_BY0_1_Q[2]
14-9J	QDR2_BY0_1_Q1 G11	QDR2_BY0_1_Q[1]
14-9J	QDR2_BY0_1_Q0 E11	QDR2_BY0_1_Q[0]
14-8H	QDR2_BY0_1_CQ_P K8	QDR2_BY0_1_CQ_P
14-8H	QDR2_BY0_1_CQ_N K9	QDR2_BY0_1_CQ_N
14-9F,14-10C	QDR2_BY0_1_K_P H5	QDR2_BY0_1_K_P
14-8F,14-10C	QDR2_BY0_1_K_N G5	QDR2_BY0_1_K_N
14-8F,14-10C	QDR2_BY0_1_R J5	QDR2_BY0_1_R
14-8C,14-8F	QDR2_BY0_1_W M5	QDR2_BY0_1_W
14-8F,14-10C	QDR2_BY0_BW F5	QDR2_BY0_BW
14-8F,14-10C	QDR2_BY1_BW L6	QDR2_BY1_BW
14-4C	QDR2_BY0_1_SA21 G12	QDR2_BY0_1_SA[21]
14-7C,14-7F	QDR2_BY0_1_SA20 P5	QDR2_BY0_1_SA[20]
14-7F,14-9C	QDR2_BY0_1_SA19 M6	QDR2_BY0_1_SA[19]
14-4C,14-7F	QDR2_BY0_1_SA18 A13	QDR2_BY0_1_SA[18]
14-5C,14-7F	QDR2_BY0_1_SA17 C13	QDR2_BY0_1_SA[17]
14-5C,14-7F	QDR2_BY0_1_SA16 B12	QDR2_BY0_1_SA[16]
14-5C,14-7F	QDR2_BY0_1_SA15 F13	QDR2_BY0_1_SA[15]
14-6C,14-7F	QDR2_BY0_1_SA14 G13	QDR2_BY0_1_SA[14]
14-6C,14-7F	QDR2_BY0_1_SA13 E12	QDR2_BY0_1_SA[13]
14-5C,14-8F	QDR2_BY0_1_SA12 B13	QDR2_BY0_1_SA[12]
14-5C,14-8F	QDR2_BY0_1_SA11 E13	QDR2_BY0_1_SA[11]
14-5C,14-8F	QDR2_BY0_1_SA10 C12	QDR2_BY0_1_SA[10]
14-6C,14-8F	QDR2_BY0_1_SA9 D12	QDR2_BY0_1_SA[9]
14-6C,14-8F	QDR2_BY0_1_SA8 F6	QDR2_BY0_1_SA[8]
14-6C,14-8F	QDR2_BY0_1_SA7 G6	QDR2_BY0_1_SA[7]
14-4C,14-8F	QDR2_BY0_1_SA6 D11	QDR2_BY0_1_SA[6]
14-6F,14-9C	QDR2_BY0_1_SA5 U10	QDR2_BY0_1_SA[5]
14-6F,14-9C	QDR2_BY0_1_SA4 R6	QDR2_BY0_1_SA[4]
14-6F,14-10C	QDR2_BY0_1_SA3 K6	QDR2_BY0_1_SA[3]
14-5F,14-10C	QDR2_BY0_1_SA2 L4	QDR2_BY0_1_SA[2]
14-5F,14-10C	QDR2_BY0_1_SA1 N5	QDR2_BY0_1_SA[1]
14-5F,14-7C	QDR2_BY0_1_SA0 T6	QDR2_BY0_1_SA[0]
14-8F	QDR2_BY0_1_DLL_OFFE9	QDR2_BY0_1_DLL_OFF

U15 BANKS=12, 20

R101 10K

QDR2_BY0_1_D[17]	E7	QDR2_BY0_1_D17	14-4C,14-11F
QDR2_BY0_1_D[16]	K7	QDR2_BY0_1_D16	14-6C,14-10F
QDR2_BY0_1_D[15]	N8	QDR2_BY0_1_D15	14-7C,14-10F
QDR2_BY0_1_D[14]	J6	QDR2_BY0_1_D14	14-7C,14-10F
QDR2_BY0_1_D[13]	N7	QDR2_BY0_1_D13	14-8C,14-10F
QDR2_BY0_1_D[12]	P7	QDR2_BY0_1_D12	14-8C,14-10F
QDR2_BY0_1_D[11]	R7	QDR2_BY0_1_D11	14-9C,14-10F
QDR2_BY0_1_D[10]	P6	QDR2_BY0_1_D10	14-9C,14-10F
QDR2_BY0_1_D[9]	U7	QDR2_BY0_1_D9	14-8C,14-10F
QDR2_BY0_1_D[8]	T8	QDR2_BY0_1_D8	14-9C,14-10F
QDR2_BY0_1_D[7]	R8	QDR2_BY0_1_D7	14-8C,14-10F
QDR2_BY0_1_D[6]	M7	QDR2_BY0_1_D6	14-9C,14-9F
QDR2_BY0_1_D[5]	T9	QDR2_BY0_1_D5	14-8C,14-9F
QDR2_BY0_1_D[4]	T10	QDR2_BY0_1_D4	14-8C,14-9F
QDR2_BY0_1_D[3]	E6	QDR2_BY0_1_D3	14-7C,14-9F
QDR2_BY0_1_D[2]	G7	QDR2_BY0_1_D2	14-7C,14-9F
QDR2_BY0_1_D[1]	T11	QDR2_BY0_1_D1	14-6C,14-9F
QDR2_BY0_1_D[0]	R11	QDR2_BY0_1_D0	14-4C,14-9F
QDR2_BY0_1_QVLD	F11	QDR2_BY0_1_QVLD	14-8F

VREF_QDR_BY0_1

QDR_BY0_1_VREF_3 P10 C593 10NF 25V
QDR_BY0_1_VREF_2 L8 C592 10NF 25V
QDR_BY0_1_VREF_1 L5 C591 10NF 25V
QDR_BY0_1_VREF D10 C590 10NF 25V

1V5

VRP_20 L11 R22 49.9R
VRN_20 L10 R40 49.9R
VRP_12 P9 R301 49.9R
VRN_12 R9 R300 49.9R

GND

1V5_20_2 J8
1V5_20_1 H11
1V5_20 E10 C591 220NF 6.3V
1V5_12_2 T7 C600 220NF 6.3V
1V5_12_1 N6 C599 220NF 6.3V
1V5_12 M9 C602 470F 6V
C603 470F 6V

GND

5V 1V5

U62

TPS51100DGQ

10	VIN	
2	VLDOIN	
1	VDDQSNS	
7	S3	
9	S5	
3	VTT	VTT_QDR_BY0_1
5	VTTSNS	
6	VTTREF	
8	PGND	
4	GND	

R302 10K
R303 10K

C595 4U7F 10V
C596 10UF 16V
C594 100NF 10V
C598 10UF 16V
C597 10UF 16V

GND and PGND (Power GND) should be isolated, with a single point connection between them.

1V5 1V8 VREF_QDR_BY0_1

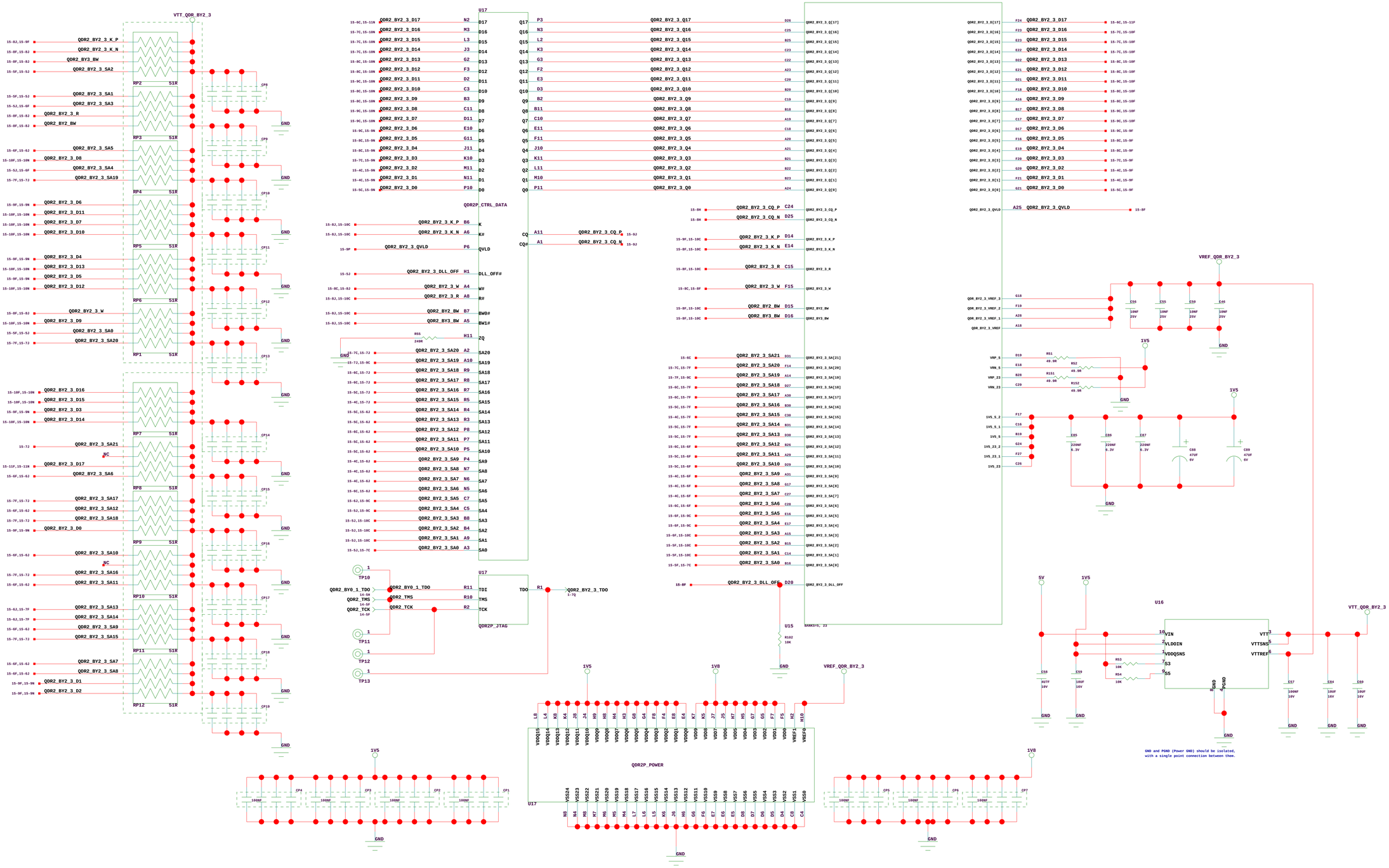
QDR2P_POWER

VDDQ15	VDDQ14	VDDQ13	VDDQ12	VDDQ11	VDDQ10	VDDQ9	VDDQ8	VDDQ7	VDDQ6	VDDQ5	VDDQ4	VDDQ3	VDDQ2	VDDQ1	VDDQ0	VDD9	VDD8	VDD7	VDD6	VDD5	VDD4	VDD3	VDD2	VDD1	VDD0	VREF1	VREF0
L8	L4	K8	K4	J8	J4	H9	H8	H4	H3	G8	G4	F9	F4	E8	E4	K7	K5	J7	J5	H7	H5	G7	G5	F7	F5	H2	H10

VSS24	VSS23	VSS22	VSS21	VSS20	VSS19	VSS18	VSS17	VSS16	VSS15	VSS14	VSS13	VSS12	VSS11	VSS10	VSS9	VSS8	VSS7	VSS6	VSS5	VSS4	VSS3	VSS2	VSS1	VSS0
N8	N4	M8	M7	M6	M5	M4	L7	L6	L5	K6	J6	H6	G6	F6	E7	E6	E5	D8	D7	D6	D5	D4	C8	C4

CP37 CP36 CP35 CP34 CP38 CP39 CP40 100NF

GND

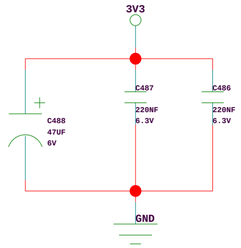


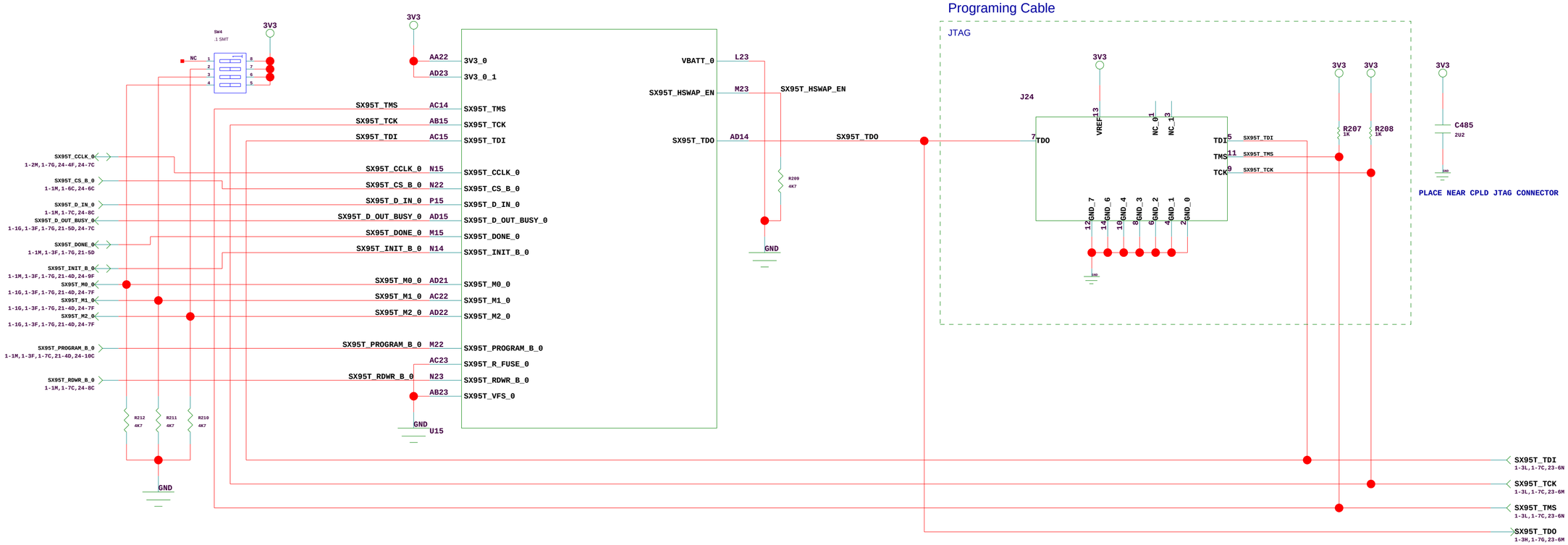
ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-27-2008_11:28 PATH PATH	DRAWN: F KAPP · APPR:
	CHECKED: E BAUERMEISTER · SHEET 15 OF 25

TBD

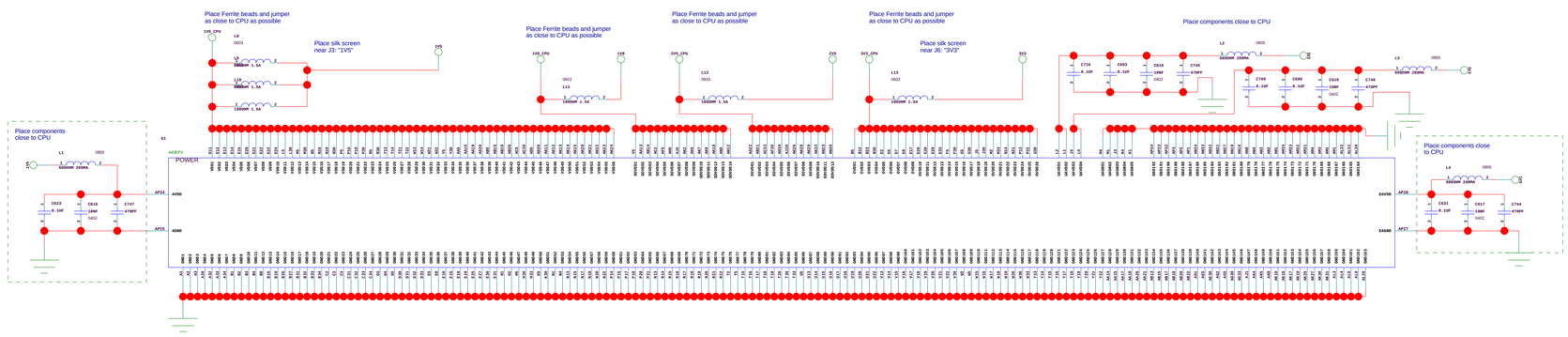
VALID CONFIGURATION MODES

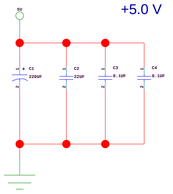
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

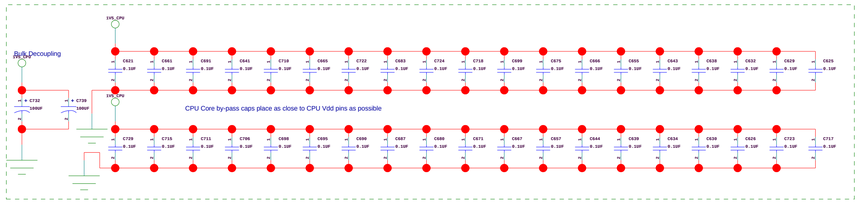


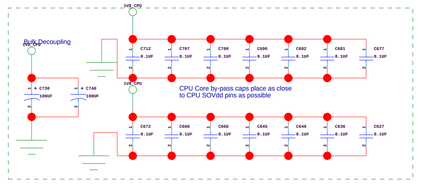


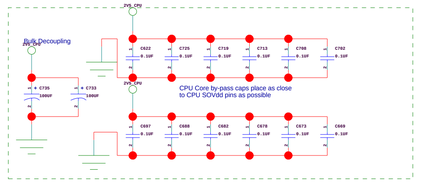
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
2-27-2008_11:28 PATH PATH	

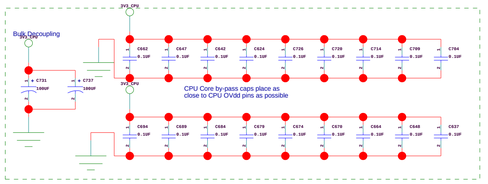


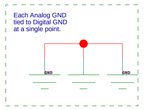










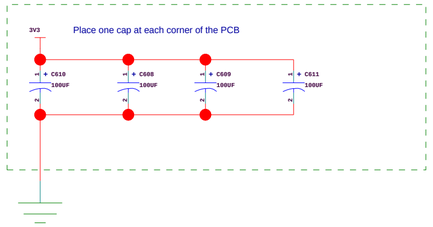


REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: **CASPER GROUP, UC BERKELEY** **NRAO, SOCORRO** **meerKAT, CAPE TOWN** http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 17 OF 25
2-27-2008_11:28 PATH PATH	

REMOVED 3V3 GENERATION



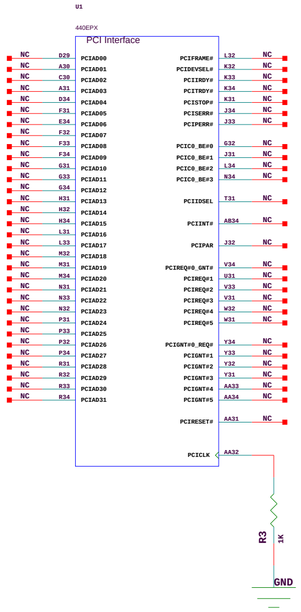
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET 18 OF 25
2-27-2008_11:28 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-27-2008_11:28 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

Place nearest PHY pin 96

Place nearest PHY pin 101

Place nearest PHY pin 98

Place nearest PHY pin 100

Place as close to PHY CORE VDD power pins as possible

Place as close to PHY IO VDD power pins as possible

UNUSED SECOND ETHERNET MAC

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups. Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place jumers in line with signals

Place decoupling C close to termination R All traces 50Ohm WRT GND or 2V5

Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

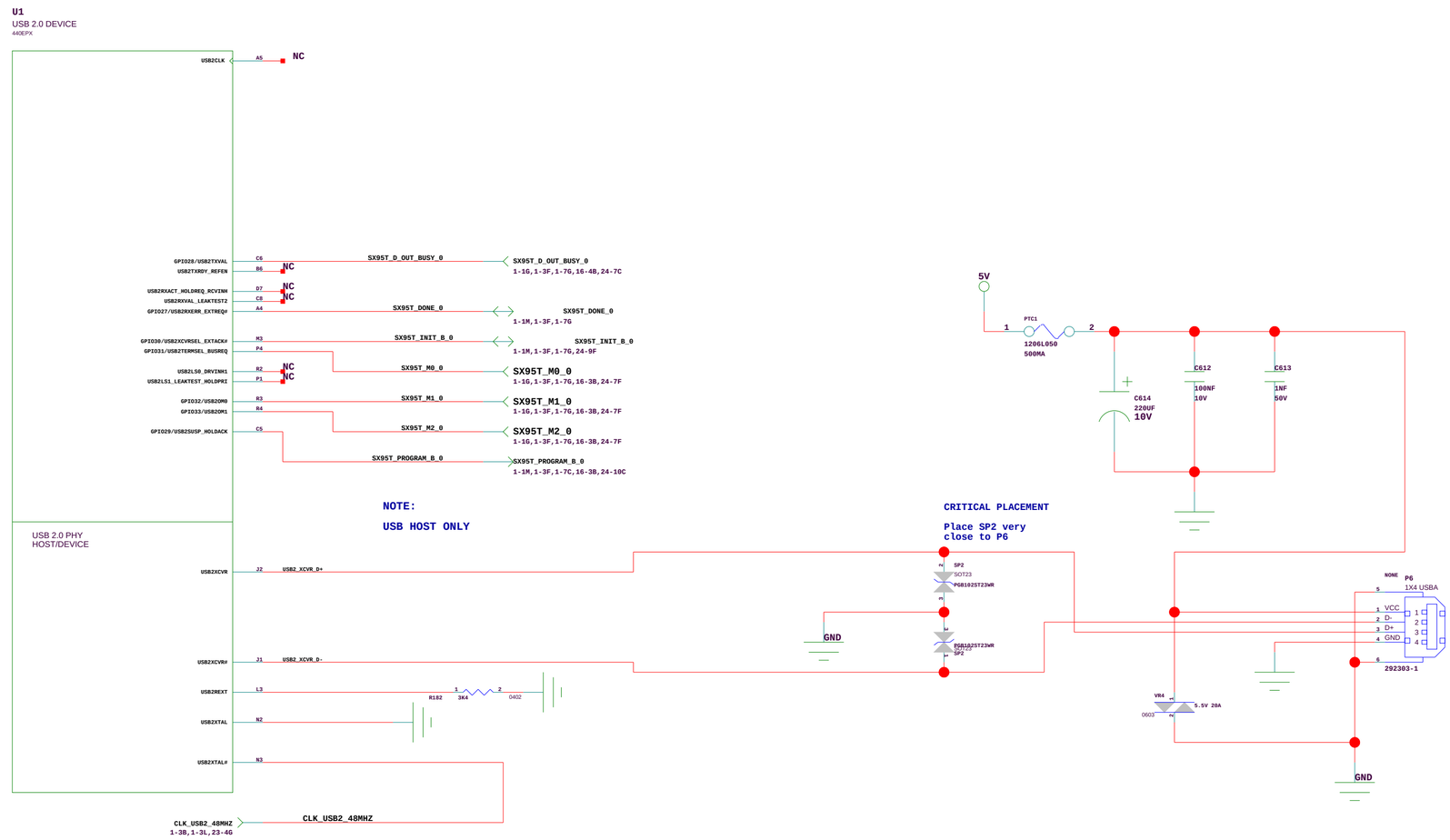
Bottom LED
Green/Toggle = ACTIVITY

HFJ11-1G02E-L12

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

ROACH/iBOB2	ROACH_PPC_ETH1
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-27-2008_11:28	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 20 OF 25



ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-27-2008_11:28 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25

DDR_PA[15:0]

DDR_PD[63:0]

U1

DDR SDRAM

44OEPX

DDR_PD0	AB2	MEMDATA00	MEMADDR00
DDR_PD1	AF2	MEMDATA01	MEMADDR01
DDR_PD2	AK5	MEMDATA02	MEMADDR02
DDR_PD3	AL28	MEMDATA03	MEMADDR03
DDR_PD4	AL22	MEMDATA04	MEMADDR04
DDR_PD5	AK22	MEMDATA05	MEMADDR05
DDR_PD6	AK21	MEMDATA06	MEMADDR06
DDR_PD7	AF21	MEMDATA07	MEMADDR07
DDR_PD8	AF28	MEMDATA08	MEMADDR08
DDR_PD9	AL18	MEMDATA09	MEMADDR09
DDR_PD10	AK17	MEMDATA10	MEMADDR10
DDR_PD11	AF17	MEMDATA11	MEMADDR11
DDR_PD12	AK26	MEMDATA12	MEMADDR12
DDR_PD13	AF16	MEMDATA13	MEMADDR13
DDR_PD14	AK16	MEMDATA14	
DDR_PD15	AF15	MEMDATA15	
DDR_PD16	AK15	MEMDATA16	
DDR_PD17	AF14	MEMDATA17	
DDR_PD18	AL15	MEMDATA18	
DDR_PD19	AF13	MEMDATA19	
DDR_PD20	AL17	MEMDATA20	
DDR_PD21	AK17	MEMDATA21	
DDR_PD22	AK13	MEMDATA22	
DDR_PD23	AK15	MEMDATA23	
DDR_PD24	AF13	MEMDATA24	
DDR_PD25	AK13	MEMDATA25	
DDR_PD26	AF12	MEMDATA26	
DDR_PD27	AL12	MEMDATA27	
DDR_PD28	AK14	MEMDATA28	
DDR_PD29	AK14	MEMDATA29	
DDR_PD30	AL13	MEMDATA30	
DDR_PD31	AK12	MEMDATA31	
DDR_PD32	AF3	MEMDATA32	
DDR_PD33	AF1	MEMDATA33	
DDR_PD34	AD4	MEMDATA34	
DDR_PD35	AD3	MEMDATA35	
DDR_PD36	AB3	MEMDATA36	
DDR_PD37	AF2	MEMDATA37	
DDR_PD38	AE2	MEMDATA38	
DDR_PD39	AE1	MEMDATA39	
DDR_PD40	AC3	MEMDATA40	
DDR_PD41	AC1	MEMDATA41	
DDR_PD42	AA4	MEMDATA42	
DDR_PD43	AA3	MEMDATA43	
DDR_PD44	AD2	MEMDATA44	
DDR_PD45	AC4	MEMDATA45	
DDR_PD46	AB1	MEMDATA46	
DDR_PD47	AB2	MEMDATA47	
DDR_PD48	Y3	MEMDATA48	
DDR_PD49	Y2	MEMDATA49	
DDR_PD50	Y4	MEMDATA50	
DDR_PD51	V3	MEMDATA51	
DDR_PD52	AA2	MEMDATA52	
DDR_PD53	AA1	MEMDATA53	
DDR_PD54	W3	MEMDATA54	
DDR_PD55	W1	MEMDATA55	
DDR_PD56	V1	MEMDATA56	
DDR_PD57	U2	MEMDATA57	
DDR_PD58	T4	MEMDATA58	
DDR_PD59	R1	MEMDATA59	
DDR_PD60	V2	MEMDATA60	
DDR_PD61	T1	MEMDATA61	
DDR_PD62	T3	MEMDATA62	
DDR_PD63	T2	MEMDATA63	

DDR_PA0	AM5	MEMADDR00	
DDR_PA1	AP4	MEMADDR01	
DDR_PA2	AP5	MEMADDR02	
DDR_PA3	AM6	MEMADDR03	
DDR_PA4	AP6	MEMADDR04	
DDR_PA5	AN6	MEMADDR05	
DDR_PA6	AL7	MEMADDR06	
DDR_PA7	AN7	MEMADDR07	
DDR_PA8	AM7	MEMADDR08	
DDR_PA9	AP7	MEMADDR09	
DDR_PA10	AL2	MEMADDR10	
DDR_PA11	AL8	MEMADDR11	
DDR_PA12	AM8	MEMADDR12	
DDR_PA13	AN4	MEMADDR13	
DDR_PBA0	AJ3	BA0	22-7L,22-8K
DDR_PBA1	AN3	BA1	22-8K,22-10L
DDR_PBA2	AP8	BA2	22-8K,22-8L
DDR_PRAS#	AJ4	RAS#	22-7K,22-7L
DDR_PCAS#	AN4	CAS#	22-7L,22-8K
DDR_PWE#	AJ2	WE#	22-3K,22-7L
DDR_PDM0	AL21	DM0	22-5K
DDR_PDM1	AP18	DM1	22-6K
DDR_PDM2	AP15	DM2	22-6K
DDR_PDM3	AL14	DM3	22-6K
DDR_PDM4	AD4	DM4	22-6K
DDR_PDM5	AB3	DM5	22-6K
DDR_PDM6	Y3	DM6	22-6K
DDR_PDM7	V3	DM7	22-6K
DDR_PDM8	AP10	DM8	22-6K
DDR_PODT0	AN3	MEMDT0	22-7L
DDR_PODT1	AG1	MEMDT1	22-6L
DDR_PCS0#	AN2	BANKSELA0	22-3K,22-7L
DDR_PCS1#	AM1	BANKSELA1	22-3K,22-7L
DDR_PCKE	AN9	MEMCLKEN	22-6K,22-11L
DDR_CLKOUT	AL1	MEMCLKOUT	
DDR_CLKOUT#	AM1	MEMCLKOUT#	

PPC_ECC0	AM11	ECC0	22-9F
PPC_ECC1	AL11	ECC1	22-9F
PPC_ECC2	AN9	ECC2	22-9F
PPC_ECC3	AL9	ECC3	22-10F
PPC_ECC4	AM11	ECC4	22-10F
PPC_ECC5	AN11	ECC5	22-10F
PPC_ECC6	AM10	ECC6	22-10F
PPC_ECC7	AP9	ECC7	22-10F

SVREF1A	Y4		
SVREF2A	AL19		
SVREF1B	AF4		
SVREF2B	AL19		

DDR2 Clock line must be 500ps longer than Address/Command lines
To compensate for additional loading when using unbuffered DIMM's
See P84 of PPC440EPx for more information

Place parts as close to CPU as possible

5V

1V8

DDR_VREF_0V9

C158 0.1UF

C149 0.1UF

C151 0.1UF 0402

C152 0.1UF 0402

C148 100F 0402

U32

TPS51100DGQ

VIN	10		
VLDOIN	2		
VDDQSNS	1	VTT	3
S3	7	VTTSNS	5
S5	9	VTTREF	6
GND	8	PGND	4

R230 10K

R229 10K

R6 120R

DDR_VTT

C459 4U7F 10V

C456 10UF 16V

C453 100NF 10V

C21 22PF

C457 10UF 16V

C458 10UF 16V

GND

J8

PPC_ECC7	22-6D	168	DDR2_DIMM_CB7
PPC_ECC6	22-6D	167	DDR2_DIMM_CB6
PPC_ECC5	22-7D	162	DDR2_DIMM_CB5
PPC_ECC4	22-7D	161	DDR2_DIMM_CB4
PPC_ECC3	22-7D	49	DDR2_DIMM_CB3
PPC_ECC2	22-7D	48	DDR2_DIMM_CB2
PPC_ECC1	22-7D	43	DDR2_DIMM_CB1
PPC_ECC0	22-7D	42	DDR2_DIMM_CB0
DDR_PDQ63		236	DDR2_DIMM_DQ[63]
DDR_PDQ62		235	DDR2_DIMM_DQ[62]
DDR_PDQ61		230	DDR2_DIMM_DQ[61]
DDR_PDQ60		229	DDR2_DIMM_DQ[60]
DDR_PDQ59		117	DDR2_DIMM_DQ[59]
DDR_PDQ58		116	DDR2_DIMM_DQ[58]
DDR_PDQ57		111	DDR2_DIMM_DQ[57]
DDR_PDQ56		110	DDR2_DIMM_DQ[56]
DDR_PDQ55		227	DDR2_DIMM_DQ[55]
DDR_PDQ54		226	DDR2_DIMM_DQ[54]
DDR_PDQ53		218	DDR2_DIMM_DQ[53]
DDR_PDQ52		217	DDR2_DIMM_DQ[52]
DDR_PDQ51		108	DDR2_DIMM_DQ[51]
DDR_PDQ50		107	DDR2_DIMM_DQ[50]
DDR_PDQ49		99	DDR2_DIMM_DQ[49]
DDR_PDQ48		98	DDR2_DIMM_DQ[48]
DDR_PDQ47		215	DDR2_DIMM_DQ[47]
DDR_PDQ46		214	DDR2_DIMM_DQ[46]
DDR_PDQ45		209	DDR2_DIMM_DQ[45]
DDR_PDQ44		208	DDR2_DIMM_DQ[44]
DDR_PDQ43		96	DDR2_DIMM_DQ[43]
DDR_PDQ42		95	DDR2_DIMM_DQ[42]
DDR_PDQ41		90	DDR2_DIMM_DQ[41]
DDR_PDQ40		89	DDR2_DIMM_DQ[40]
DDR_PDQ39		206	DDR2_DIMM_DQ[39]
DDR_PDQ38		205	DDR2_DIMM_DQ[38]
DDR_PDQ37		200	DDR2_DIMM_DQ[37]
DDR_PDQ36		199	DDR2_DIMM_DQ[36]
DDR_PDQ35		87	DDR2_DIMM_DQ[35]
DDR_PDQ34		86	DDR2_DIMM_DQ[34]
DDR_PDQ33		81	DDR2_DIMM_DQ[33]
DDR_PDQ32		80	DDR2_DIMM_DQ[32]
DDR_PDQ31		159	DDR2_DIMM_DQ[31]
DDR_PDQ30		158	DDR2_DIMM_DQ[30]
DDR_PDQ29		153	DDR2_DIMM_DQ[29]
DDR_PDQ28		152	DDR2_DIMM_DQ[28]
DDR_PDQ27		40	DDR2_DIMM_DQ[27]
DDR_PDQ26		39	DDR2_DIMM_DQ[26]
DDR_PDQ25		34	DDR2_DIMM_DQ[25]
DDR_PDQ24		33	DDR2_DIMM_DQ[24]
DDR_PDQ23		150	DDR2_DIMM_DQ[23]
DDR_PDQ22		149	DDR2_DIMM_DQ[22]
DDR_PDQ21		144	DDR2_DIMM_DQ[21]
DDR_PDQ20		143	DDR2_DIMM_DQ[20]
DDR_PDQ19		31	DDR2_DIMM_DQ[19]
DDR_PDQ18		30	DDR2_DIMM_DQ[18]
DDR_PDQ17		25	DDR2_DIMM_DQ[17]
DDR_PDQ16		24	DDR2_DIMM_DQ[16]
DDR_PDQ15		141	DDR2_DIMM_DQ[15]
DDR_PDQ14		140	DDR2_DIMM_DQ[14]
DDR_PDQ13		132	DDR2_DIMM_DQ[13]
DDR_PDQ12		131	DDR2_DIMM_DQ[12]
DDR_PDQ11		22	DDR2_DIMM_DQ[11]
DDR_PDQ10		21	DDR2_DIMM_DQ[10]
DDR_PDQ9		13	DDR2_DIMM_DQ[9]
DDR_PDQ8		12	DDR2_DIMM_DQ[8]
DDR_PDQ7		129	DDR2_DIMM_DQ[7]
DDR_PDQ6		128	DDR2_DIMM_DQ[6]
DDR_PDQ5		123	DDR2_DIMM_DQ[5]
DDR_PDQ4		122	DDR2_DIMM_DQ[4]
DDR_PDQ3		10	DDR2_DIMM_DQ[3]
DDR_PDQ2		9	DDR2_DIMM_DQ[2]
DDR_PDQ1		4	DDR2_DIMM_DQ[1]
DDR_PDQ0		3	DDR2_DIMM_DQ[0]
		101	DDR2_DIMM_SA2
		240	DDR2_DIMM_SA1
		239	DDR2_DIMM_SA0
		120	DDR2_DIMM_SCL
		119	DDR2_DIMM_SDA
		879160001	

1V8

R228 4K7

R227 4K7

PPC_DDR2_DIMM_SCL

PPC_DDR2_DIMM_SDA

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA1	22-9D,22-10L
DDR2_DIMM_BA[1]	190	DDR_PBA2	22-8L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-7L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	NC	
DDR2_DIMM_CK_N[2]	221	NC	
DDR2_DIMM_CK_P[1]	137	NC	
DDR2_DIMM_CK_N[1]	138	NC	
DDR2_DIMM_CK_P[0]	185	DDR_CLKOUT	
DDR2_DIMM_CK_N[0]	186	DDR_CLKOUT#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-8D,22-11L
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-8D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-71,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-71,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-71,22-8D
PAR_OUT	55	PPC_DDR2_ERROR	1 TP4
PAR_IN	68	PAR_IN	1 TP5

R226 4K7

PPC_DDR2_RESET_N

1-2B,1-2M,24-10F

C455 5PF 50V

879160001

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

DDR_VTT

22-6K,22-8D	DDR_PCKE	RP24	CP26
	DDR_PA15		
	DDR_PA14		
22-8K,22-8D	DDR_PBA1		
	DDR_PA12	RP23	CP28
	DDR_PA11		
	DDR_PA9		
	NC		
	DDR_PA7	RP22	CP29
	DDR_PA8		
	DDR_PA6		
	DDR_PA5		
	DDR_PA4	RP21	CP30
	DDR_PA3		
	DDR_PA1		
	DDR_PA2		
	DDR_PA0	RP25	CP32
22-8K,22-8D	DDR_PBA2		
	DDR_PA10		
22-8K,22-8D	DDR_PBA0		
22-7K,22-8D	DDR_PRAS#	RP26	CP31
22-3K,22-8D	DDR_PWE#		
22-3K,22-8D	DDR_PCS0#		
22-8K,22-8D	DDR_PCAS#		
22-3K,22-8D	DDR_PCS1#	RP19	CP33
22-8D	DDR_PODT0		
	DDR_PA13		
22-8D	DDR_PODT1		

GND

J8

VSS_64	237	69	VSS_63
VSS_62	234	67	VSS_61
VSS_60	231	64	VSS_59
VSS_58	228	62	VSS_57
VSS_56	225	59	VSS_55
VSS_54	222	53	VSS_53
VSS_52	219	194	VSS_51
VSS_50	216	191	VSS_49
VSS_48	213	181	VSS_47
VSS_46	210	175	VSS_45
VSS_44	207	170	VSS_43
VSS_42	204	78	VSS_41
VSS_40	201	75	VSS_39
VSS_38	198	72	VSS_37
VSS_36	169	62	VSS_35
VSS_34	166	56	VSS_33
VSS_32	163	51	VSS_31
VSS_30	160		VSS_29
VSS_28	157		VSS_27
VSS_26	154		VSS_25
VSS_24	151		VSS_23
VSS_22	148		VSS_21
VSS_20	145		VSS_19
VSS_18	142		VSS_17
VSS_16	139		VSS_15
VSS_14	136		VSS_13
VSS_12	133		VSS_11
VSS_10	130		VSS_9
VSS_8	127		VSS_7
VSS_6	124		VSS_5
VSS_4	121		VSS_3
VSS_2	118		VSS_1
	115		
	112		
	109		
	106		
	103		
	100		
	97		
	94		
	91		
	88		
	85		
	82		
	79		
	66		
	65		
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	47		
	44		
	41		
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	35		
	32		
	29		
	26		
	23		
	20		
	17		
	14		
	11		
	8		
	5		
	2		

879160001

DDR_VREF_0V9

VREF 1

1V8

VDDSPD 238

1V8

VDD_11	197	194	VDDQ_11
VDD_10	189	191	VDDQ_10
VDD_9	187	181	VDDQ_9
VDD_8	184	175	VDDQ_8
VDD_7	178	170	VDDQ_7
VDD_6	172	78	VDDQ_6
VDD_5	69	75	VDDQ_5
VDD_4	67	72	VDDQ_4
VDD_3	64	62	VDDQ_3
VDD_2	59	56	VDDQ_2
VDD_1	53	51	VDDQ_1

1V8

GND

DDR_VREF_0V9

1V8

1V8

1V8

C432 100NF 10V

C433 10NF 25V

C454 100NF 10V

C434 10NF 25V

C430 100NF 10V

C443 10NF 25V

C431 100NF 10V

C444 10NF 25V

C436 100NF 10V

C445 10NF 25V

C435 100NF 10V

C446 10NF 25V

GND

1V8

1V8

1V8

C438 100NF 10V

C451 10NF 25V

C437 100NF 10V

C452 10NF 25V

C439 100NF 10V

C449 10NF 25V

C440 100NF 10V

C450 10NF 25V

C441 100NF 10V

C448 10NF 25V

C442 100NF 10V

C447 10NF 25V

GND

PLACE NEAREST DDR2 MODULE PINS

ROACH/iBOB2

ROACH_PPC_DDR2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

2-27-2008_11:28

PATH PATH

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

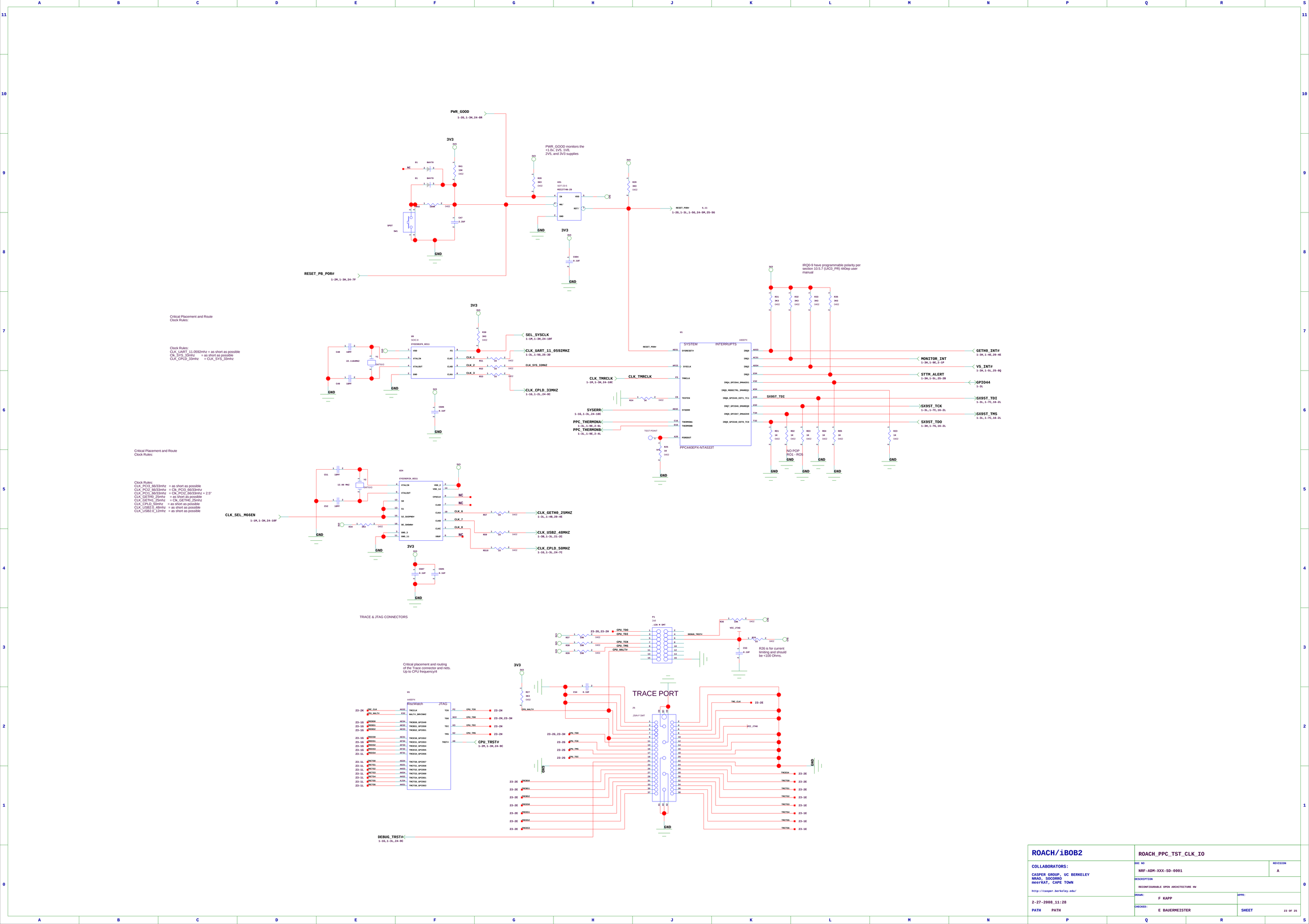
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 22 OF 25



ROACH/iBOB2	**ROACH_PPC_TST_CLK_IO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
2-27-2008_11:28	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 23 OF 25

RESETS

CPU_TRST# = '1' when
JTAG_TRST# = '1' and
RESET_POR# = '1' else '0';
see errata sheet

roach_cpld_XC2C256_7VQ100C_pcb

CLK_TMCLK	4	PAD4	
SYSRR	7	PAD8	
EXT_RESET#	9	PAD10	
SX95T_PROGRAM_B_0	10	PAD12	
SX95T_DONE_0	11	PAD15	
PCS_2	12	PAD16	
PB_WE	13	PAD17	
DEBUG_TRST#	14	PAD18	
CPU_TRST#	15	PAD19	
FWBE_0#	16	PAD20	
PADATA[27:31]	17	PADA27	
	18	PADA28	
	19	PADA29	
	20	PADA30	
PDATA[0:7]	21	PADA31	
	22	PDATA0	
	23	PDATA1	
	24	PDATA2	
	25	PDATA3	
	26	PDATA4	
	28	PDATA7	
CLK_CPLD_33MHZ	30	PAD48	
	31	PDATA6	
	32	PDATA5	
PDE#	33	PAD52	
SX95T_BOOT_B_0	34	PAD54	
SX95T_D_IN_0	35	PAD55	
CLK_CPLD_50MHZ	38	PAD59	
SX95T_D_OUT_BUSY_0	40	PAD64	
	41	PER_CCLK_EN#	
	42	CLK_PERCLK	
	43	SX95T_CCLK_0	
FRY_BY#	44	PAD68	
FWP#	45	PAD69	
EE1_WP#	46	PAD70	
EE2_BOOT_WP#	48	PAD73	
STTM_AS#	49	PAD74	
SELECTMAP_CS	50	PAD75	
	51	NC	PAD76
SX95T_CS_B_0	52	PAD77	
	53	NC	PAD81
PPC_RESET	54	PAD82	
SYS_CONFIG0	56	PAD86	
SYS_CONFIG1	57	PAD87	
SYS_CONFIG2	58	PAD88	
SYS_CONFIG3	59	PAD89	
SYS_CONFIG4	60	PAD90	
SYS_CONFIG5	61	PAD95	
SYS_CONFIG6	64	PAD100	
SYS_CONFIG7	66	PAD102	
	68	NC	PAD105
	69	NC	PAD107
	70	NC	PAD108
RESET_CPLD#	71	PAD109	
	74	NC	PAD112
	75	NC	PAD113
	142	NC	PAD217
	140	NC	PAD214
GETH0_RST#	139	PAD213	
PPC_DDR2_RESET_N	138	PAD212	
CLK_SEL_MGGEN	137	PAD211	
SEL_SYSCLK	136	PAD208	
	135	NC	PAD207
	134	NC	PAD206
	133	NC	PAD204
	132	NC	PAD199
SX95T_INIT_B_0	131	PAD197	
	130	NC	PAD196
	129		PAD195
	128		PAD194
	126		PAD192
	125	NC	PAD191
	124	NC	PAD190
	121		PAD187
DAT1	120		PAD186
DAT0_DO	119		PAD178
DAT7	118		PAD177
DAT6	117		PAD176
CLK_SCLK	116		PAD175
DAT5	115		PAD173
DAT4	114		PAD171
CMD_DI	113		PAD169
DAT3	112		PAD168
DAT2	111		PAD167
	110		PAD166
	107		PAD163
SX95T_M0_0	106		PAD162
SX95T_M1_0	105		PAD161
SX95T_M2_0	104		PAD160
	103		PAD158
RESET_PB_POR#	102		PAD156
USER_LED0	101		PAD154
USER_LED1	100		PAD152
SYSERR#	98		PAD146
RESET_BUFPOR#	97		PAD145
	96		PAD144
	95		PAD143
	94		PAD142
	92		PAD138
	91		PAD137
	88		PAD134
	87		PAD133
	86	NC	PAD132
	85	NC	PAD131
	83	NC	PAD125
	82	NC	PAD121
	81	NC	PAD120
	80	NC	PAD119
	79	NC	PAD118
	78	NC	PAD117
	77	NC	PAD115
	76	NC	PAD114

U54 XC2C256_7VQ144C

SYS_CONFIG[0:7] 1-2G,1-9E,2-2R

RESET_CPLD# 1-1M,1-4G,25-3J

BOOT_CFG0 1-1M,1-4G,25-1J
BOOT_CFG1 1-1M,1-4G,25-1J
BOOT_CFG2 1-1M,1-4G,25-1J

SD/MMC/MMCPLUS CONNECTOR

J17 SDSR13-A0-0005

CMD/DI	10	DAT0/DO	2
CLK/SCLK	6	DAT1	1
		DAT2	13
VDD	7	DAT3	12
VSS1	8	DAT4	11
VSS2	4	DAT5	9
		DAT6	5
SD_CD_COM	14	DAT7	3
SD_WP_COM	15		
		MNT1	16
		MNT2	17

SX95T_INIT_B_0 1-1M,1-3F,1-7G,21-4D

SX95T_M0_0 1-1G,1-3F,1-7G,16-3D,21-4D
SX95T_M1_0 1-1G,1-3F,1-7G,16-3D,21-4D
SX95T_M2_0 1-1G,1-3F,1-7G,16-3D,21-4D

RESET_PB_POR# 1-2M,1-3G,23-8E

SysErr will be used to drive Status LED (active H)

SW2 User DIP-Switch

USER_DIP0
USER_DIP1
USER_DIP2
USER_DIP3

Boot Configuration

CFG_DIP0
CFG_DIP1
CFG_DIP2
MGGEN

SW3 Configuration DIP-Swith

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

U54 roach_cpld_XC2C256_7VQ100C_configpins

XC2C256_7VQ144C

RESET_POR# 1-2G,1-3L,1-5G,23-9J,25-5G

Xilinx Programing Cable

JTAG J22

PLACE NEAR CPLD JTAG CONNECTOR

C484 20Z

U54 roach_cpld_XC2C256_7VQ100C_powerpins

XC2C256_7VQ144C

VCC	1	GND_3	29
VAUX	8	GND_4	36
VCCIO_3	27	GND_5	47
VCC_1	37	GND_6	62
VCCIO_4	55	GND_7	72
VCCIO_5	73	GND_8	89
VCC_2	84	GND_9	90
VCCIO_6	93	GND_10	99
VCCIO	109	GND	108
VCCIO_1	127	GND_1	123
VCCIO_2	141	GND_2	144

PLACE AT END OF DAISY CHAIN

ENABLE PER_CLK CONNECTION
TO CONFIGURATION I/F
MUST CO-ORDINATE WITH
SX95T_CCLK_0 AND MODE
TO AVOID CLASH

SN74AHC1G125DCKT

PER_CCLK_EN# 1 OE# VCC 5
CLK_PERCLK 2 A Y 4
3 GND
U2

R135 10K
R305 330R
R306 240R
C13 100NF 10V

CLK_PERCLK 1-1G,1-4L,24-7C,25-6F
SX95T_CCLK_0 1-2M,1-7G,24-4F

PLACE NEAR CPLD POWER PINS

C473 C474 C475 C476 C477 C478 C479 C480 C481 C482 C483
100NF 10V

Xilinx Programing Cable

J22

VREF	13	NC_0	3
TDO	7	NC_1	5
		TDI	9
		TMS	11
		TCK	13
GND_7	12	GND_6	10
GND_4	8	GND_3	6
GND_2	4	GND_1	2
GND_0	1		

R193 1K
R192 1K

PLACE NEAR CPLD JTAG CONNECTOR

C484 20Z

U35 74LVC1G08 SC70-5

R197 100R
R199 100R
C61 100N
C62 100N
C615 0.01F

PWR_GOOD 1-2G,1-3H,23-10G

ROACH/iBOB2	ROACH_PPC_CPLD	
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
2-27-2008_11:28 PATH PATH	DRAWN: F KAPP	APPR:
	CHECKED: E BAUERMEISTER	SHEET 24 OF 25

PDATA[0:31]
1-2M,1-4L

PADD[20:31]
1-2G,1-4L,24-9B,25-10B

PADD[2:31]

PADD30 IS THE LSB FOR 16 BIT WIDE BUS TRANSFERS

**NOTE:
DMA SIGNALS
IN GREEN TEXT**

PADD2 IS THE MSB

3V3

PCS_3_GPIO910 — 25-7C
PDEV — 1-1G,1-5L,24-8C,25-5G,25-7B,25-7M
PB_WP — 1-1G,1-4L,24-10C,25-5G,25-6M,25-7B
PWBE_0# — 1-2G,1-4L,24-9C,25-6M,25-7B
PWBE_1# — 25-6M,25-7C
PWBE_2# — 25-7C
PWBE_3# — 25-7C
PREADY — 25-7C,25-9Q
PBLAST# — 25-6M,25-7C
PCS_0
PCS_1
PCS_2
SELECTMAP_CS

External Slave Peripheral
AXEEPH

PERDATA[31:0]
PERADDR[31:2]
PERADDR[0]
PERADDR[1]
PERCS0
PERCS1#_GPIO06
PERCS2#
PERCS4#_GPIO09
PERCS5#_GPIO10
PERDEV
PERWE_WP
PERBE_0#
PERBE_1#
PERBE_2#
PERBE_3#
PERREADY
PERBLAST#

External Master Peripheral
Interface

EXTRESET#
PERCLK
PERERR_GPIO11

R134 R133 R132 R84 R83 R5 — 3K3

R6 — 0R — CLK_PERCLK

R85 — 1K

EXT_RESET# — EPB RESET OUTPUT
1-2G,1-4L,24-10C

CLK_PERCLK
1-1G,1-4L,24-4C,24-7C

U42
FBGA64
32Mx16 MIRROR BIT
FLASH
32Mx16
4Mx8B

WP#/ACC
RY/BY#
PCS_0
PADD[30:2]
PDATA[15:0]

R86 — 3K3 — RY/BY#
1-1M,1-4G,24-7C

R81 — 3K3

R5 — 3K3

C654 C656 C659 — 0.1UF 0402

RESET_CPLD#
1-1M,1-4G,24-5C

BOOT_CFG2
1-1M,1-4G,24-10M

BOOT_CFG1
1-1M,1-4G,24-11M

BOOT_CFG0
1-1M,1-4G,24-11M

PADD30 AE23 PER_A[30]
PADD29 AE22 PER_A[29]
PADD28 AG18 PER_A[28]
PADD27 AG12 PER_A[27]
PADD26 AG15 PER_A[26]
PADD25 AG23 PER_A[25]
PADD24 AF19 PER_A[24]
PADD23 AE12 PER_A[23]
PADD22 AG16 PER_A[22]
PADD21 AF13 PER_A[21]
PADD20 AG20 PER_A[20]
PADD19 AF23 PER_A[19]
PADD18 AH17 PER_A[18]
PADD17 AH15 PER_A[17]
PADD16 L20 PER_SP_A[16]
PADD15 J22 PER_SP_A[15]
PADD14 H22 PER_SP_A[14]
PADD13 L15 PER_SP_A[13]
PADD12 L16 PER_SP_A[12]
PADD11 K22 PER_SP_A[11]
PADD10 K21 PER_SP_A[10]
PADD9 K16 PER_SP_A[9]
PADD8 J15 PER_SP_A[8]
PADD7 DMAREQ2 L21 PER_SP_A[7]
PADD6 DMAACK2 G22 PER_SP_A[6]
PADD5 EOT2/TC2 K23 PER_SP_A[5]
PADD4 DMAREQ3 K14 PER_SP_A[4]
PADD3 DMAACK3 L14 PER_SP_A[3]
PADD2 EOT3/TC3 J12 PER_SP_A[2]

PCS_1 K13 PER_CS0
POE# AF21 PER_OE_N
PR_W# AF20 PER_R_W_N
PWBE_1# AF14 PER_WBE[1]
PWBE_0# AF18 PER_WBE[0]
PBLAST# H23 PER_B_LAST

U15
BANKS=1, 2, 4
CHIP SELECT 1

3V3_4_1 AL12
3V3_4_2 AG14
3V3_3_2 AM19
3V3_2 AM21
3V3_1_1 G14
3V3_1 D13

PER_D[15] AH14 PDATA15
PER_D[14] AH22 PDATA14
PER_D[13] AH13 PDATA13
PER_D[12] AG22 PDATA12
PER_D[11] AE21 PDATA11
PER_D[10] AG13 PDATA10
PER_D[9] AH20 PDATA9
PER_D[8] AH12 PDATA8
PER_D[7] AE17 PDATA7
PER_D[6] AD20 PDATA6
PER_D[5] AF16 PDATA5
PER_D[4] AH19 PDATA4
PER_D[3] AE16 PDATA3
PER_D[2] AE19 PDATA2
PER_D[1] AF15 PDATA1
PER_D[0] AD19 PDATA0

PER_D_PAR[1] AG21 NC
PER_D_PAR[0] AE13 NC

PER_INT G23 — VS_INT#
1-3H,1-5L,23-7N

PER_READY K12 — PREADY
25-7C,25-9B

PER_CLK H12 — CLK_PERCLK

C334 470F 6V
C335 470F 6V
C330 220NF 0.3V
C331 220NF 0.3V
C332 220NF 0.3V
C333 220NF 0.3V

GND

I2C0_SCLK
1-5L,1-9B,2-2P

I2C0_33_DATA
1-5L,1-8E

EE2_BOOT_WP
1-2M,1-4G,24-7C

ATMEL 256
ATMEL_256_SOIC_8
ATMEL_256_SOIC_8_NARROW
ATMEL_256_SOIC_8_WIDE
ATMEL_256_SOIC_8_WIDE_SWAP
ATMEL_256_SOIC_8_WIDE_SWAP_NOSILK
ATMEL_256_SOIC_8_WIDE_NOSILK
ATMEL_256_SOIC_8_NARROW_NOSILK
ATMEL_256_SOIC_8_NARROW_SWAP
ATMEL_256_SOIC_8_NARROW_SWAP_NOSILK
AT24C04N-10SU-1.8

R88 — 15K

NO POP
R89 — 0R

I2C0_33_DATA
I2C0_66_DATA
I2C0_SDATA

BUFFL_2A-6
PI5A3157
S=B BO TO A

M66EN
1-1G,1-5G,24-5M

EE1_WP
1-2M,1-5G,24-7C

R90 — 15K

R91 VT 0.12k H SMT

C651 — 0.1UF

SOT23-6

STTM_ALERT
1-3M,1-5L,23-6M

STTM_AS
1-2M,1-5G,24-7C

R73 R74 — 3K3

R75 R76 R77 R78 — 3K3

R40 VT 0.12k H SMT

SCPCLK
1-5L

SCPDI
1-5L

SCPDO
1-5L

SCPCLK
SCPDI
SCPDO

U1
AXEEPH
UART
UARTSERCLK
CLK_UART_11.0592MHZ
1-3L,1-5G,23-7G

UART1_TX_UART0_TX
UART1_RX_UART0_RX
UART1_RTS#_UART0_RTS#
UART1_CTS#_UART0_CTS#
UART2_TX_UART0_DTR#
UART2_RX_UART0_RI#
UART2_RTS#_UART0_DSR#
UART2_CTS#_UART0_DCD#

IIC0
IIC1_SPI
NAND Flash
Interface
NOT USED

SCPCLKOUT_IIC1SCLK
SCPDI_IIC1SDATA
SCPDO

NFALE
NFCLE
NFREN#
NFWEN#
NFRDYBUSY#
NFCE3#_PERCS3#

UART1_TX
UART1_RX
UART2_TX
UART2_RX
UART2_RTS#
UART2_CTS#

PERPARB_UART1_RTS#
PERPARB_UART1_CTS#

U48 TDFN_ZA-6 PI5A3157 S=B BO TO A
U45 TDFN_ZA-6 PI5A3157 S=B BO TO A
U46 TDFN_ZA-6 PI5A3157 S=B BO TO A

C652 — 0.1UF

R82 — 3K3

U44 SSOP20 ICL3225ECA
U43 SSOP20 ICL3225ECA

C192 C194 C196 C198 — 0.1UF
C193 C195 C197 C199 — 0.1UF

X_UART1_TX
X_UART1_RX
X_UART1_RTS#
X_UART1_CTS#
X_UART2_TX
X_UART2_RX
X_UART2_RTS#
X_UART2_CTS#

R85 R87 — 10K

C649 C653 — 0.1UF

P2
DSUB9_FEMALE_90DEGREE
RF BOOB MALE
UART Port 0

J14
HLE-105-02-G-DV
UART Port 1

NC P1
X_UART2_RX P2
X_UART2_TX P3
P4
P5
NC P6
X_UART2_RTS# P7
NC P8
NC P9
P10

ROUTE AS DAISY CHAIN - U1 - U15 - U2 - U54 - TERMINATION
KEEP STUBS AS SHORT AS POSSIBLE

1-1G,1-5L,24-8C,25-7B,25-7M,25-10B — PDEV
1-1G,1-4L,24-10C,25-6M,25-7B,25-9B — PB_WP
RESET_PORb
1-2G,1-3L,1-5G,23-8J,24-5M

ROACH/iBOB2	**ROACH_PPC_NVM_SERIAL**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 25 OF 25
2-27-2008_11:28 PATH PATH	