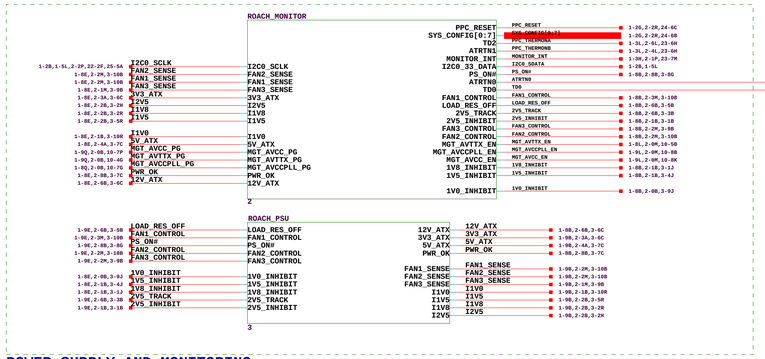
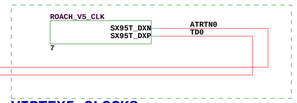
VIRTEX5

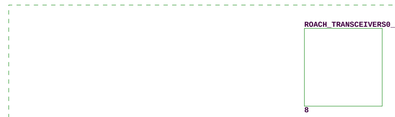


POWER SUPPLY AND MONITORING

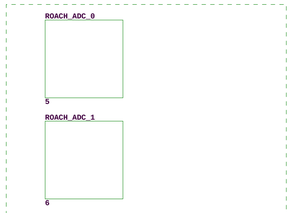


VIRTEX5 CLOCKS

V5 DDR2 MEMORY

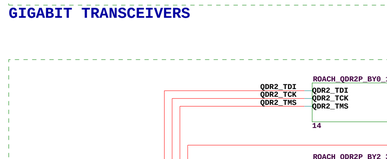


GIGABIT TRANSCEIVERS

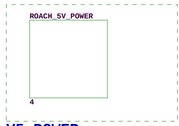


ZDOK/ADC INTERFACE

V5 DIFFERENTIAL GPIO



QDRII+ MEMORY

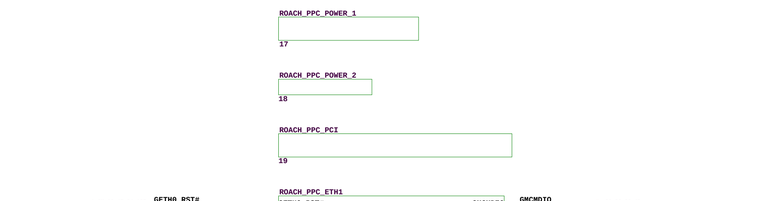


V5 POWER

VIRTEX5 CONFIGURATION

V5 SE GPIO & MISCELLANEOUS

PPC



MECHANICAL

BOARD FIDUCIALS

LOGO'S

PLACEHOLDER FOR PCB
MEERKAT LOGO

PLACEHOLDER FOR PCB
CASPER LOGO

PLACEHOLDER FOR PCB
ROACH LOGO

PLACEHOLDER FOR PCB
NRAO LOGO

BOARD SERIAL NUMBER

CONTRIBUTORS

ETIENNE BAUERMEISTER
HENRY CHEN
STEVE DURAND
FRANCOIS KAPP
ALAN LANGMAN
GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2	ROACH_TOP
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-3-2008_11:20	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 1 OF 25

roach_AFS600_pcb

PLACE AT ACTEL 3V3 POWER PINS

PLACE AT ACTEL 1V5 POWER PINS

roach_AFS600_powerpins

roach_AFS600_configpins

ACTEL JTAG CONNECTOR

TIE TO GROUND IF PLL'S ARE NOT USED

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

XPORT - PLACE IN REAR I/O REGION
XP1001001-03R

PB POWER SWITCH

KEY - REMOVE PIN

MONITOR RESET

TEMPERATURE DIODE HEADER

SPARE ANALOG VOLTAGE INPUT #0

SPARE ANALOG VOLTAGE INPUT #1

SPARE GATE DRIVE OUTPUT #0

SPARE GATE DRIVE OUTPUT #1

REFERENCE RESISTOR/ADC VALUES

VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)
12V	0R01	3.36	0.11
5V	0R0047	6.78	0.22
3V3	0R01	3.47	0.12
2V5	0R01	3.56	0.13
1V8	0R0022	12.91	0.37
1V5	0R0047	6.77	0.22
1V0	0R001	26.79	0.72

FOR 8 BIT ADC USING 2.56V REFERENCE:

ADC COUNT AT MAX POWER	CURRENT/BIT (A)
33	0.1
31	0.21
34	0.1
35	0.1
28	0.45
31	0.21
26	1.0

ROACH/iBOB2	ROACH_MONITOR
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
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7-3-2008_11:20	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 2 OF 25

AUX FAN CONNECTORS - ATX 4 PIN

J21
1 GND
2 12V
3 SENSE
4 CONTROL
47053-1000

FAN1_SENSE 3 — 1-8B,1-9B,2-2M
FAN1_CONTROL 4 — 1-8B,1-9E,2-2M
PLACE ON SILKSCREEN: FAN1

J20
1 GND
2 12V
3 SENSE
4 CONTROL
47053-1000

FAN2_SENSE 3 — 1-8E,1-9B,2-2M
FAN2_CONTROL 4 — 1-8B,1-9E,2-2M
PLACE ON SILKSCREEN: FAN2

J19
1 GND
2 12V
3 SENSE
4 CONTROL
47053-1000

FAN3_SENSE 3 — 1-8E,1-9B,2-1M
FAN3_CONTROL 4 — 1-8B,1-9E,2-2M
PLACE ON SILKSCREEN: FAN3

GND

ATX POWER CONNECTORS

5VAUX
N12V

J18
1 3V3_1
2 3V3_2
3 COM_1
4 5V_1
5 COM_2
6 5V_2
7 COM_3
8 PWR_OK
9 5VSB
10 12V1_1
11 12V1_2
12 3V3_3
13 3V3_4
14 _12V
15 COM_4
16 PS_ON#
17 COM_5
18 COM_6
19 COM_7
20 NC
21 5V_3
22 5V_4
23 5V_5
24 COM_8
44206-0007

PS_ON# — 1-8B,1-9E,2-8B
PWR_OK — 1-8B,1-8E,2-8B
5VAUX
J32
8510-4500PL

5V_ATX — 1-8E,1-9B,2-4A
3V3_ATX — 1-8E,1-9B,2-3A
12V_ATX — 1-8B,1-8E,2-6B

GND

BOARD LAYOUT NOTE
SEPARATE GROUND RETURN CURRENTS FROM MAIN BOARD GROUND PLANES
BETWEEN POWER INPUT CONNECTORS AND REGULATOR AREA ON BOARD.

LOAD RESISTORS FOR ATX PSU MIN LOAD
SWITCH OFF ONCE LOAD EXCEEDS MINIMUM SPEC
ADJUST RESISTOR VALUES FOR ACTUAL SUPPLY

5VAUX
R180 10K
Q9 NDS331N
R185 10R 5W AC05000001009JL800
Q8 BSS138
Q10 NDS331N
R187 56R 5W AC05000005609JL800
LOAD_RES_OFF — 1-8B,1-9E,2-6B
R181 10K
GND

PSU INPUT SUMMARY

VOLTAGE	5.0V +- 10%
CURRENT (MAX)	6.0A

5V
L6 BLM31PG121SN1B
L5 BLM31PG121SN1B
L16 BLM31PG121SN1B
C403 330UF 16V
C401 330UF 16V
C419 22UF 16V
GND

1V0
ROUTE FROM LOAD
R13 22R
PLACE RESISTOR CLOSE TO U50
ROUTE SHORTEST
R144 6R

U50 30A SMPS MODULE
13 TURBOTRANS
10 SENSE+
2 VI_1
6 VI_0
1 INHIBIT/UVLADJ
14 TRACK
11 SENSE-
PTH05T210WAD

1V5
1V0_INHIBIT — 1-8B,1-8E,2-6B
Q4 BSS138
ROUTE FROM LOAD

4 GND_3
7 GND_2
8 GND_1
3 GND_0

VO_0 5
VO_1 9
VOADJUST 12
R143 634R
DIRECT TO P8 ON U50, DEDICATED TRACE

C418 10UF
C117 10UF
C402 1000UF 2V5
C400 1000UF 2V5
C104 1000UF 2V5
C105 1000UF 2V5
I1V0 — 1-8E,1-9D,2-1B

PSU RAIL SUMMARY

VOLTAGE	1.0V +- 5%
SUPPLIES	FPGA CORE
CURRENT (QUIESCENT)	1.5A
CURRENT (ACTIVE)	26.8A
LOAD STEP	25.3A

1.2V SUPPLY DELETED - NOT REQUIRED

LOAD RESISTORS FOR ATX PSU MIN LOAD
SWITCH OFF ONCE LOAD EXCEEDS MINIMUM SPEC
ADJUST RESISTOR VALUES FOR ACTUAL SUPPLY

5VAUX
R180 10K
Q9 NDS331N
R185 10R 5W AC05000001009JL800
Q8 BSS138
Q10 NDS331N
R187 56R 5W AC05000005609JL800
LOAD_RES_OFF — 1-8B,1-9E,2-6B
R181 10K
GND

1V5
ROUTE FROM LOAD
R12 22R
PLACE RESISTOR CLOSE TO U51
ROUTE SHORTEST
R146 1K82

U51 16A SMPS MODULE
9 TURBOTRANS
6 SENSE+
2 VI
11 INHIBIT/UVLADJ
10 TRACK
7 SENSE-
1 SMARTSYNC
PTH08T240WAD

12V
L7 BLM31PG121SN1B
C404 330UF 16V
C420 22UF 16V
GND

1V8
1V5_INHIBIT — 1-8B,1-8E,2-1B
Q5 BSS138
ROUTE FROM LOAD

4 GND_1
3 GND_0

VO 5
VOADJUST 8
R147 649R
DIRECT TO P8 ON U51, DEDICATED TRACE

C421 10UF
C405 1000UF 2V5
I1V5 — 1-8E,1-9D,2-2B

PSU RAIL SUMMARY

VOLTAGE	1.5V +- 5%
SUPPLIES	FPGA IO, QDR, PPC
CURRENT (QUIESCENT)	0.25A
CURRENT (ACTIVE)	6.8A
LOAD STEP	6.55A

2V5
ROUTE FROM LOAD
R10 22R
PLACE RESISTOR CLOSE TO U53
ROUTE SHORTEST
R177 649R

2V5_TRACK — 1-8B,1-9E,2-6B
R183 1K
C426 10UF
U53
8 TURBOTRANS
5 SENSE+
2 VI
10 INHIBIT/UVLADJ
9 TRACK
6 SENSE-
1 SMARTSYNC
PTH08T230WAD

12V
L15 BLM31PG121SN1B
C412 330UF 16V
C424 22UF 16V
GND

2V5_INHIBIT — 1-8B,1-9E,2-1B
Q7 BSS138
ROUTE FROM LOAD

VO 4
VOADJUST 7
R179 2K87
DIRECT TO P8 ON U53, DEDICATED TRACE
C425 10UF 16V
C413 680UF 4V
I2V5 — 1-8E,1-9B,2-2B

PSU INPUT SUMMARY

VOLTAGE	12V +- 10%
CURRENT (MAX)	0.8A

PSU RAIL SUMMARY

VOLTAGE	2.5V +- 5%
SUPPLIES	FPGA, ZDOK PPC, PHY
CURRENT (QUIESCENT)	0.1A
CURRENT (ACTIVE)	3.6A
LOAD STEP	3.5A

1V8
ROUTE FROM LOAD
R11 22R
PLACE RESISTOR CLOSE TO U52
ROUTE SHORTEST
R149 1K82

U27 16A SMPS MODULE
9 TURBOTRANS
6 SENSE+
2 VI
11 INHIBIT/UVLADJ
10 TRACK
7 SENSE-
1 SMARTSYNC
PTH08T220WAD

12V
L14 BLM31PG121SN1B
C409 330UF 16V
C423 22UF 16V
GND

2V5
1V8_INHIBIT — 1-8B,1-8E,2-1B
Q6 BSS138
ROUTE FROM LOAD

4 GND_1
3 GND_0

VO 5
VOADJUST 8
R148 487R
DIRECT TO P8 ON PTH08T210W, DEDICATED TRACE
C422 10UF
C410 1000UF 2V5
I1V8 — 1-8E,1-9D,2-2B

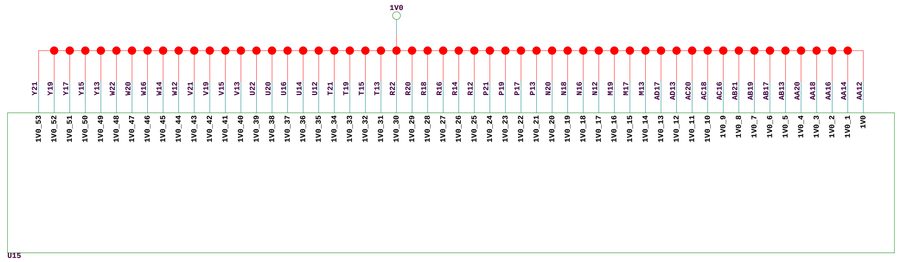
PSU RAIL SUMMARY

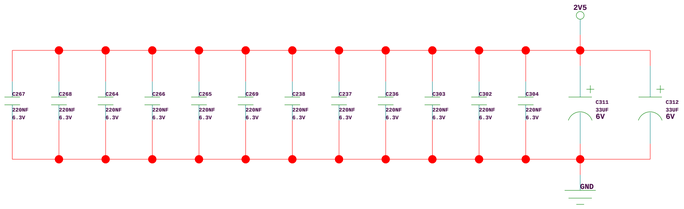
VOLTAGE	1.8V +- 5%
SUPPLIES	FPGA IO, DDR2 x 2
CURRENT (QUIESCENT)	1A
CURRENT (ACTIVE)	12.9A
LOAD STEP	11.9A

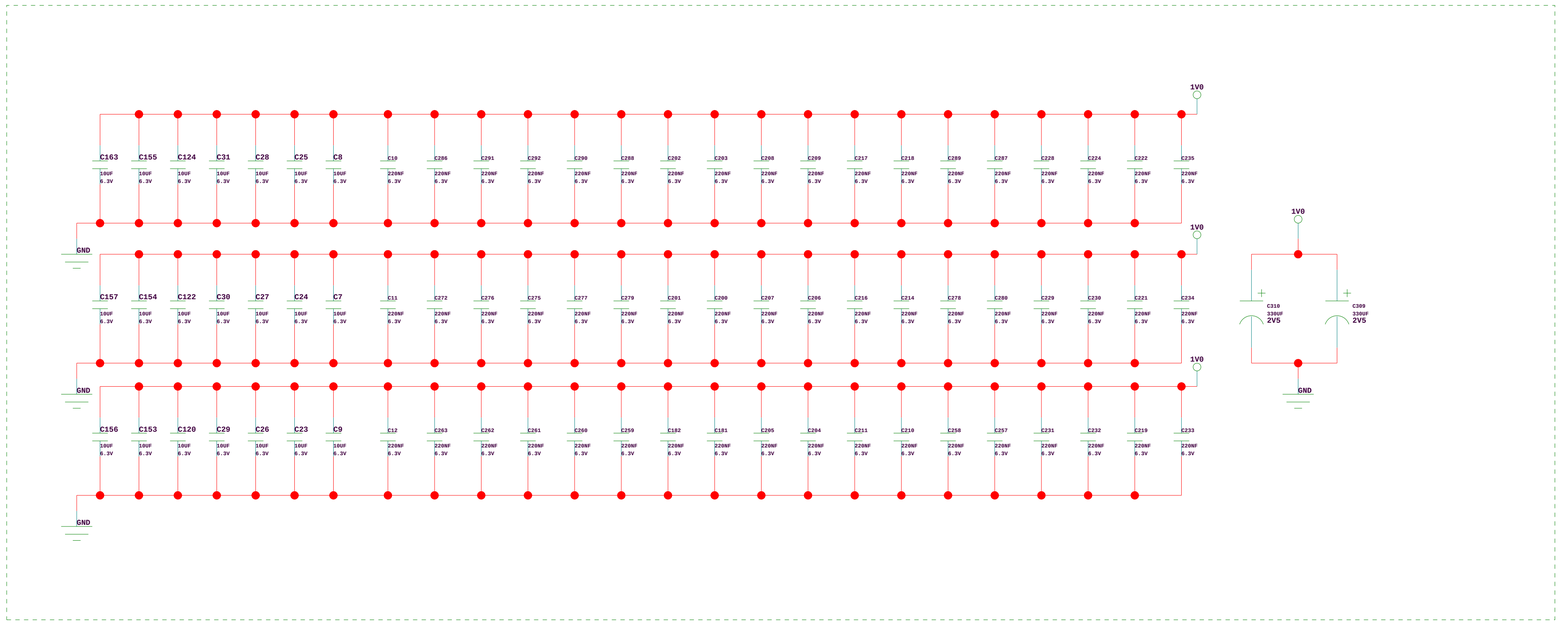
PSU INPUT SUMMARY

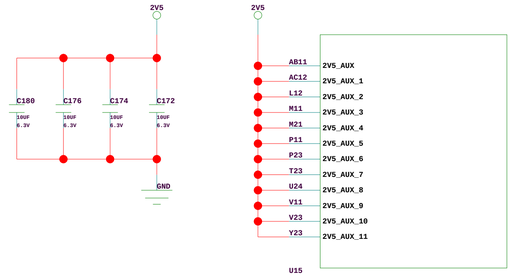
VOLTAGE	12V +- 10%
CURRENT (MAX)	1.8A

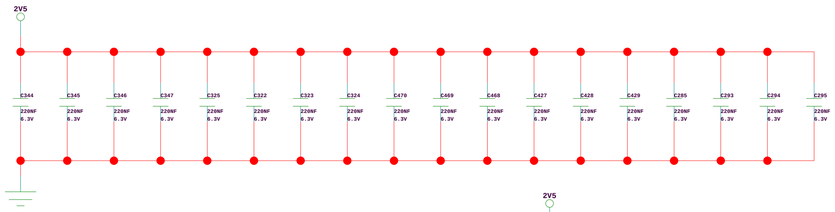
ROACH/iBOB2	ROACH_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-3-2008_11:20	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 3 OF 25

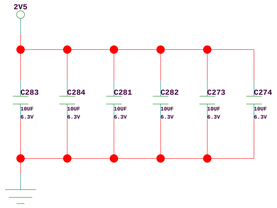


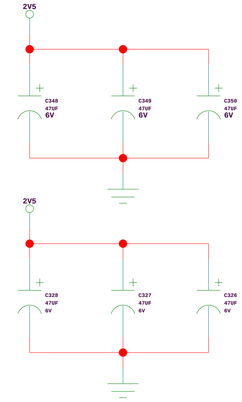


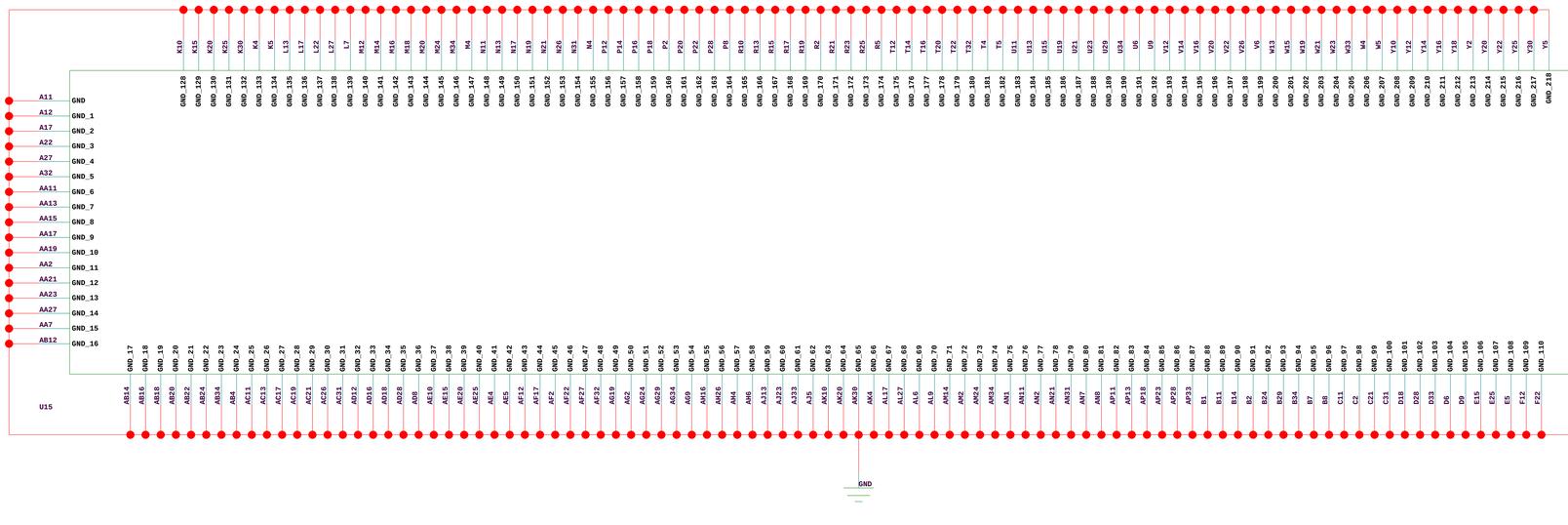












ROACH/iBOB2	ROACH_5V_POWER
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-3-2008_11:20 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 4 OF 25

5-5L	ZDOK0_CLK0_P	J20	ZDOK0_CLK0_P
5-5L	ZDOK0_CLK0_N	J21	ZDOK0_CLK0_N
5-3L	ZDOK0_CLK1_P	H19	ZDOK0_CLK1_P
5-3L	ZDOK0_CLK1_N	H20	ZDOK0_CLK1_N

ZDOK0_DP_P[37]	B33	ZDOK0_DP_P37	5-3L
ZDOK0_DP_N[37]	C33	ZDOK0_DP_N37	5-3L
ZDOK0_DP_P[36]	F25	ZDOK0_DP_P36	5-3L
ZDOK0_DP_N[36]	F26	ZDOK0_DP_N36	5-3L
ZDOK0_DP_P[35]	E32	ZDOK0_DP_P35	5-4L
ZDOK0_DP_N[35]	E33	ZDOK0_DP_N35	5-4L
ZDOK0_DP_P[34]	F33	ZDOK0_DP_P34	5-4L
ZDOK0_DP_N[34]	E34	ZDOK0_DP_N34	5-4L
ZDOK0_DP_P[33]	G32	ZDOK0_DP_P33	5-4L
ZDOK0_DP_N[33]	H32	ZDOK0_DP_N33	5-4L
ZDOK0_DP_P[32]	J27	ZDOK0_DP_P32	5-4L
ZDOK0_DP_N[32]	J26	ZDOK0_DP_N32	5-4L
ZDOK0_DP_P[31]	H34	ZDOK0_DP_P31	5-4L
ZDOK0_DP_N[31]	J34	ZDOK0_DP_N31	5-4L
ZDOK0_DP_P[30]	K31	ZDOK0_DP_P30	5-5L
ZDOK0_DP_N[30]	L31	ZDOK0_DP_N30	5-5L
ZDOK0_DP_P[29]	L30	ZDOK0_DP_P29	5-5L
ZDOK0_DP_N[29]	M30	ZDOK0_DP_N29	5-5L
ZDOK0_DP_P[28]	C34	ZDOK0_DP_P28	5-5L
ZDOK0_DP_N[28]	D34	ZDOK0_DP_N28	5-5L
ZDOK0_DP_P[27]	E29	ZDOK0_DP_P27	5-5L
ZDOK0_DP_N[27]	F29	ZDOK0_DP_N27	5-5L
ZDOK0_DP_P[26]	H25	ZDOK0_DP_P26	5-6L
ZDOK0_DP_N[26]	H24	ZDOK0_DP_N26	5-6L
ZDOK0_DP_P[25]	G30	ZDOK0_DP_P25	5-6L
ZDOK0_DP_N[25]	F30	ZDOK0_DP_N25	5-6L
ZDOK0_DP_P[24]	G33	ZDOK0_DP_P24	5-6L
ZDOK0_DP_N[24]	F34	ZDOK0_DP_N24	5-6L
ZDOK0_DP_P[23]	J30	ZDOK0_DP_P23	5-6L
ZDOK0_DP_N[23]	J31	ZDOK0_DP_N23	5-6L
ZDOK0_DP_P[22]	L25	ZDOK0_DP_P22	5-6L
ZDOK0_DP_N[22]	L26	ZDOK0_DP_N22	5-6L
ZDOK0_DP_P[21]	L29	ZDOK0_DP_P21	5-7L
ZDOK0_DP_N[21]	K29	ZDOK0_DP_N21	5-7L
ZDOK0_DP_P[20]	N27	ZDOK0_DP_P20	5-7L
ZDOK0_DP_N[20]	M27	ZDOK0_DP_N20	5-7L
ZDOK0_DP_P[19]	B32	ZDOK0_DP_P19	5-3J
ZDOK0_DP_N[19]	A33	ZDOK0_DP_N19	5-3J
ZDOK0_DP_P[18]	E26	ZDOK0_DP_P18	5-3J
ZDOK0_DP_N[18]	E27	ZDOK0_DP_N18	5-3J
ZDOK0_DP_P[17]	G25	ZDOK0_DP_P17	5-3J
ZDOK0_DP_N[17]	G26	ZDOK0_DP_N17	5-3J
ZDOK0_DP_P[16]	G27	ZDOK0_DP_P16	5-4J
ZDOK0_DP_N[16]	H27	ZDOK0_DP_N16	5-4J
ZDOK0_DP_P[15]	J24	ZDOK0_DP_P15	5-4J
ZDOK0_DP_N[15]	J25	ZDOK0_DP_N15	5-4J
ZDOK0_DP_P[14]	H30	ZDOK0_DP_P14	5-4J
ZDOK0_DP_N[14]	G31	ZDOK0_DP_N14	5-4J
ZDOK0_DP_P[13]	K27	ZDOK0_DP_P13	5-4J
ZDOK0_DP_N[13]	K26	ZDOK0_DP_N13	5-4J
ZDOK0_DP_P[12]	J32	ZDOK0_DP_P12	5-4J
ZDOK0_DP_N[12]	H33	ZDOK0_DP_N12	5-4J
ZDOK0_DP_P[11]	K33	ZDOK0_DP_P11	5-5J
ZDOK0_DP_N[11]	K32	ZDOK0_DP_N11	5-5J
ZDOK0_DP_P[10]	L34	ZDOK0_DP_P10	5-5J
ZDOK0_DP_N[10]	K34	ZDOK0_DP_N10	5-5J
ZDOK0_DP_P[9]	C32	ZDOK0_DP_P9	5-5J
ZDOK0_DP_N[9]	D32	ZDOK0_DP_N9	5-5J
ZDOK0_DP_P[8]	E28	ZDOK0_DP_P8	5-5J
ZDOK0_DP_N[8]	F28	ZDOK0_DP_N8	5-5J
ZDOK0_DP_P[7]	F31	ZDOK0_DP_P7	5-5J
ZDOK0_DP_N[7]	E31	ZDOK0_DP_N7	5-5J
ZDOK0_DP_P[6]	H28	ZDOK0_DP_P6	5-6J
ZDOK0_DP_N[6]	G28	ZDOK0_DP_N6	5-6J
ZDOK0_DP_P[5]	H29	ZDOK0_DP_P5	5-6J
ZDOK0_DP_N[5]	J29	ZDOK0_DP_N5	5-6J
ZDOK0_DP_P[4]	K24	ZDOK0_DP_P4	5-6J
ZDOK0_DP_N[4]	L24	ZDOK0_DP_N4	5-6J
ZDOK0_DP_P[3]	K28	ZDOK0_DP_P3	5-6J
ZDOK0_DP_N[3]	L28	ZDOK0_DP_N3	5-6J
ZDOK0_DP_P[2]	M25	ZDOK0_DP_P2	5-6J
ZDOK0_DP_N[2]	M26	ZDOK0_DP_N2	5-6J
ZDOK0_DP_P[1]	M28	ZDOK0_DP_P1	5-7J
ZDOK0_DP_N[1]	N28	ZDOK0_DP_N1	5-7J
ZDOK0_DP_P[0]	M31	ZDOK0_DP_P0	5-7J
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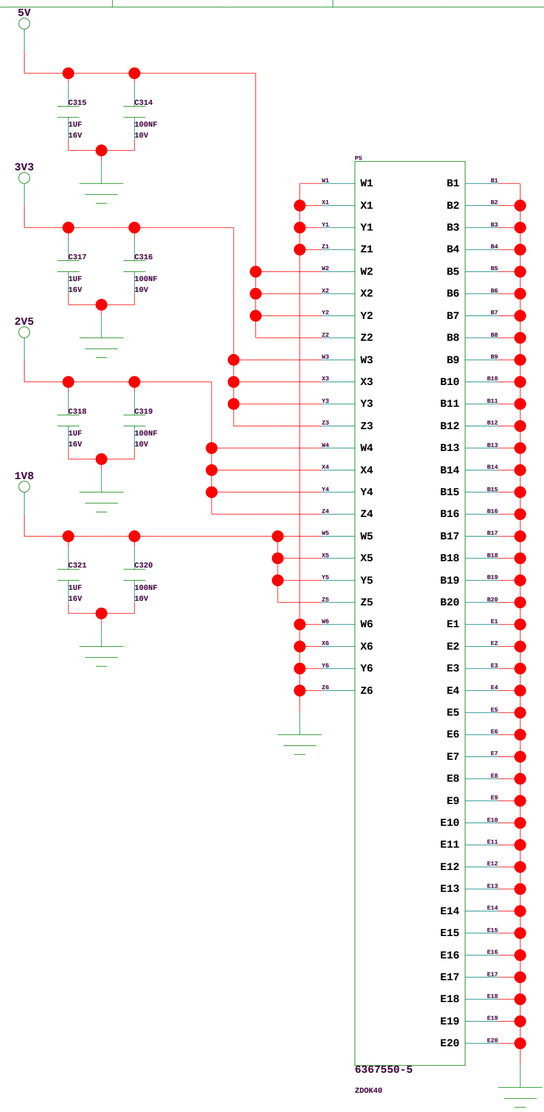
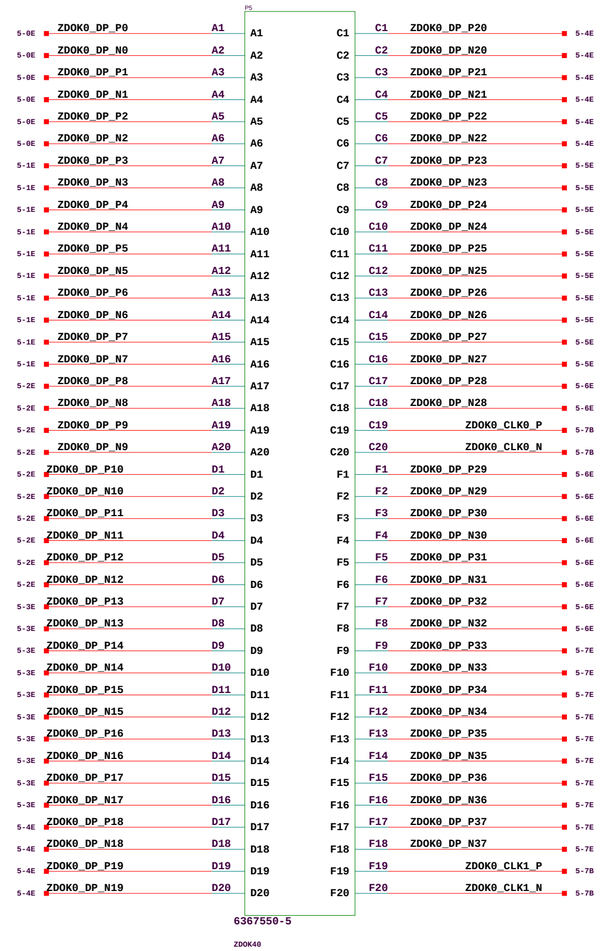
U15

BANKS=11, 13, 15, 17, 19, 21





ROACH/iBOB2	**ROACH_ADC_0**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-3-2008_11:20 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 5 OF 25

ZDOK1_CLK0_P H17
ZDOK1_CLK0_N H18
ZDOK1_CLK1_P K17
ZDOK1_CLK1_N L18
ZDOK1_CLK0_P
ZDOK1_CLK0_N
ZDOK1_CLK1_P
ZDOK1_CLK1_N
ZDOK1_DP_P[37] AD31 ZDOK1_DP_P37
ZDOK1_DP_N[37] AE31 ZDOK1_DP_N37
ZDOK1_DP_P[36] AF33 ZDOK1_DP_P36
ZDOK1_DP_N[36] AE33 ZDOK1_DP_N36
ZDOK1_DP_P[35] AF31 ZDOK1_DP_P35
ZDOK1_DP_N[35] AG31 ZDOK1_DP_N35
ZDOK1_DP_P[34] AG32 ZDOK1_DP_P34
ZDOK1_DP_N[34] AH32 ZDOK1_DP_N34
ZDOK1_DP_P[33] AG28 ZDOK1_DP_P33
ZDOK1_DP_N[33] AH28 ZDOK1_DP_N33
ZDOK1_DP_P[32] AF24 ZDOK1_DP_P32
ZDOK1_DP_N[32] AG25 ZDOK1_DP_N32
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ZDOK1_DP_N[28] AC27 ZDOK1_DP_N28
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ZDOK1_DP_P[19] AB30 ZDOK1_DP_P19
ZDOK1_DP_N[19] AC30 ZDOK1_DP_N19
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ZDOK1_DP_P[17] AC25 ZDOK1_DP_P17
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ZDOK1_DP_P[16] AE28 ZDOK1_DP_P16
ZDOK1_DP_N[16] AF28 ZDOK1_DP_N16
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ZDOK1_DP_P[14] AF25 ZDOK1_DP_P14
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ZDOK1_DP_N[1] AJ29 ZDOK1_DP_N1
ZDOK1_DP_P[0] AN34 ZDOK1_DP_P0
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U15
BANKS=11, 13, 15, 17, 19, 21
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3V3
2V5
1V8
C337 1UF 16V
C336 100NF 10V
C339 1UF 16V
C338 100NF 10V
C340 1UF 16V
C341 100NF 10V
C343 1UF 16V
C342 100NF 10V
P7
6367550-5
ZDOK40
ZDOK1_DP_P0 A1
ZDOK1_DP_N0 A2
ZDOK1_DP_P1 A3
ZDOK1_DP_N1 A4
ZDOK1_DP_P2 A5
ZDOK1_DP_N2 A6
ZDOK1_DP_P3 A7
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ZDOK1_DP_P5 A11
ZDOK1_DP_N5 A12
ZDOK1_DP_P6 A13
ZDOK1_DP_N6 A14
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ZDOK1_DP_P18 D17
ZDOK1_DP_N18 D18
ZDOK1_DP_P19 D19
ZDOK1_DP_N19 D20
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C15 ZDOK1_DP_P27
C16 ZDOK1_DP_N27
C17 ZDOK1_DP_P28
C18 ZDOK1_DP_N28
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C20 ZDOK1_CLK0_N
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F3 ZDOK1_DP_P30
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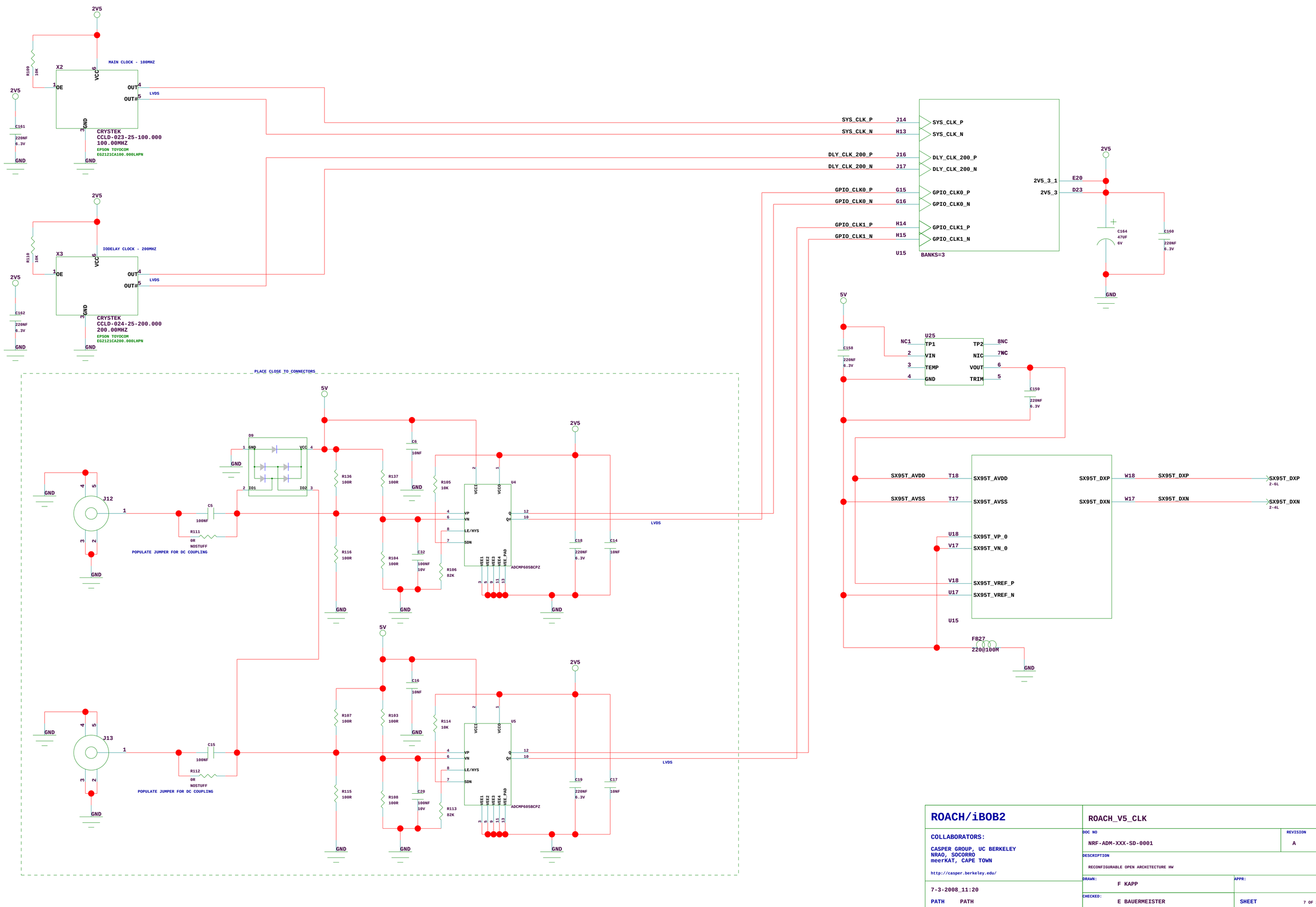
F18 ZDOK1_DP_N37
F19 ZDOK1_CLK1_P
F20 ZDOK1_CLK1_N
6367550-5
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
7-3-2008_11:20
PATH PATH
ROACH_ADC_1
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 6 OF 25



ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

7-3-2008_11:20

PATH PATH

ROACH_V5_CLK

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 7 OF 25

ROACH/iBOB2	**ROACH_TRANSCEIVERS0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 8 OF 25
7-3-2008_11:20 PATH	

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

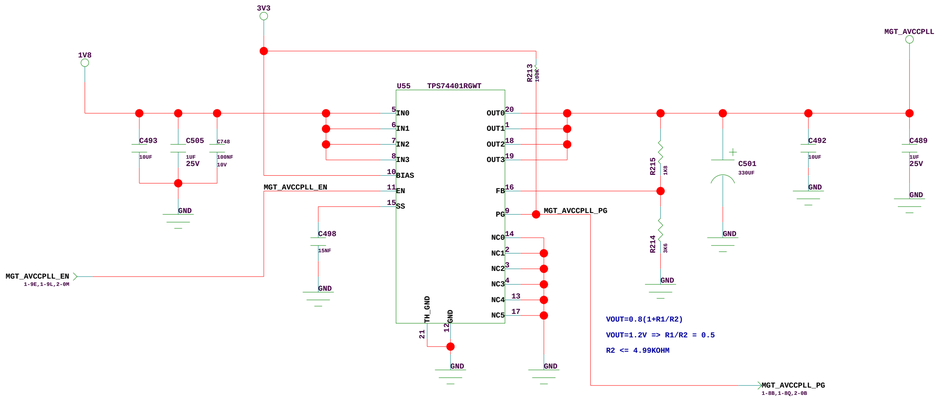
G4 AND G8 CONNECTED IN 2X2 MODULE

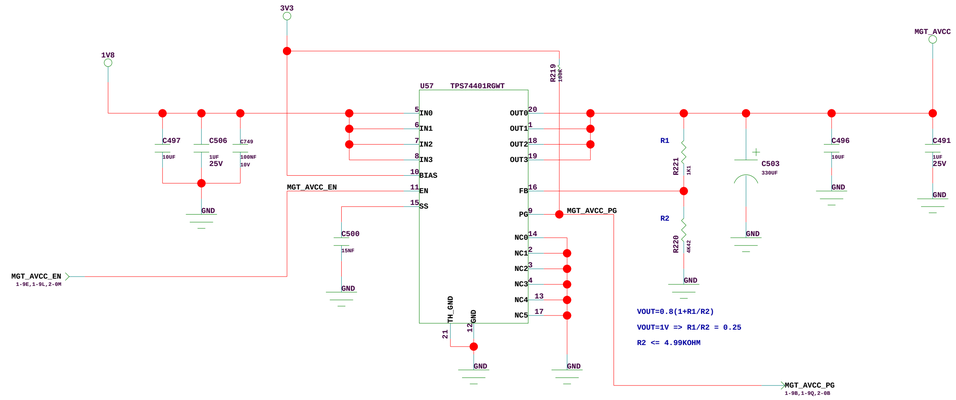
OPTICAL MODULE FAULT - RED LED

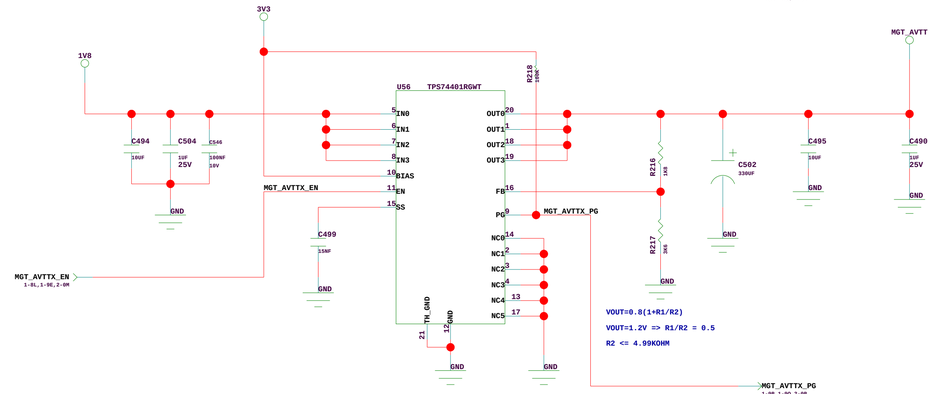
CCLD-023-25-156.250 156.25MHZ

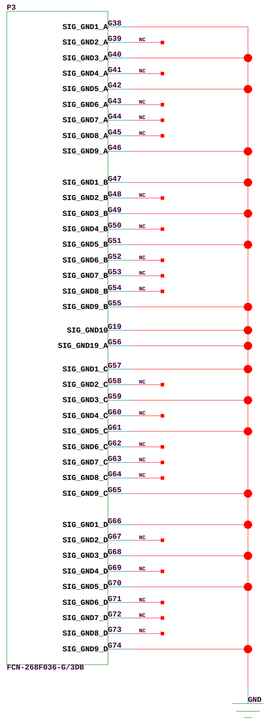
FCN-268F036-G/3DB

ROACH/iBOB2	ROACH_TRANSCEIVERS2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-3-2008_11:20	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 9 OF 25

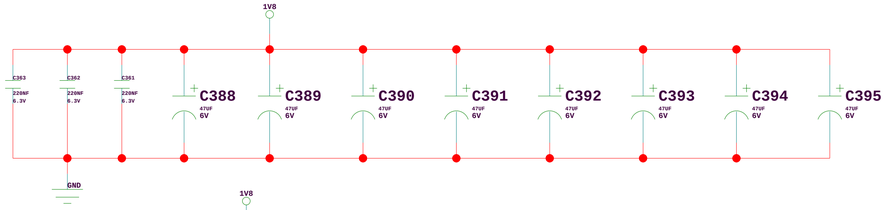


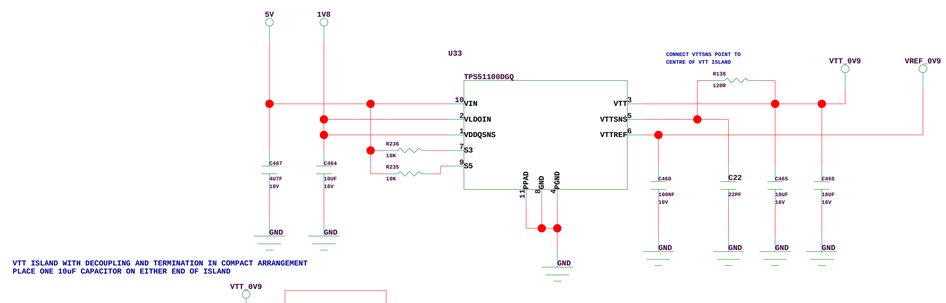


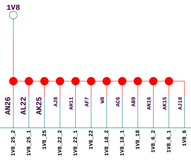


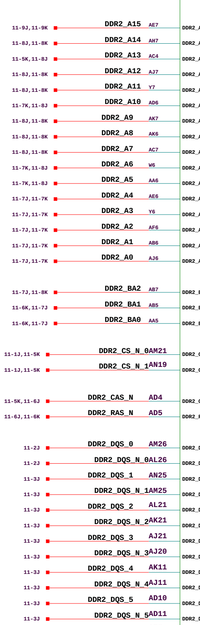


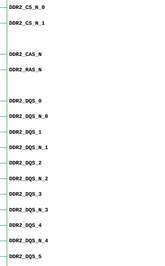
ROACH/iBOB2	**ROACH_TRANSCEIVERS_PSU**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 10 OF 25
7-3-2008_11:20 PATH PATH	



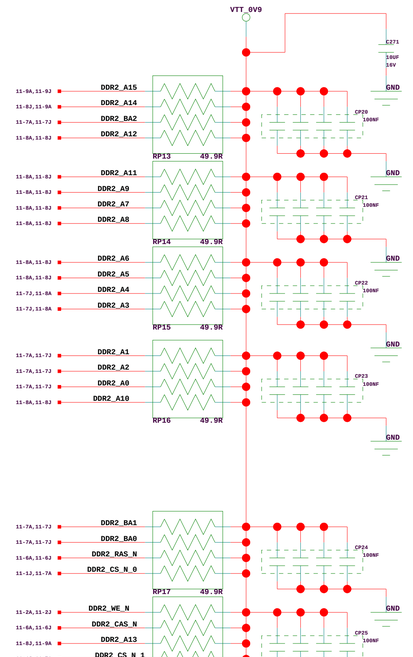


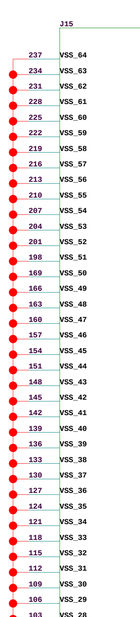


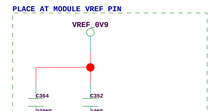


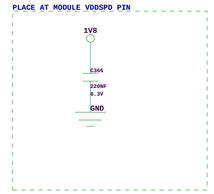


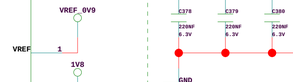
VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
PLACE ONE 10uF CAPACITOR ON EITHER END OF ISLAND

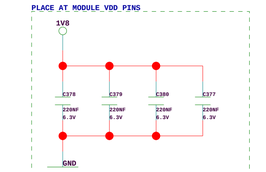


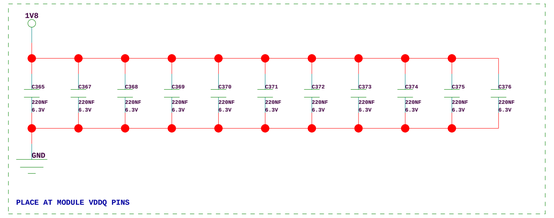




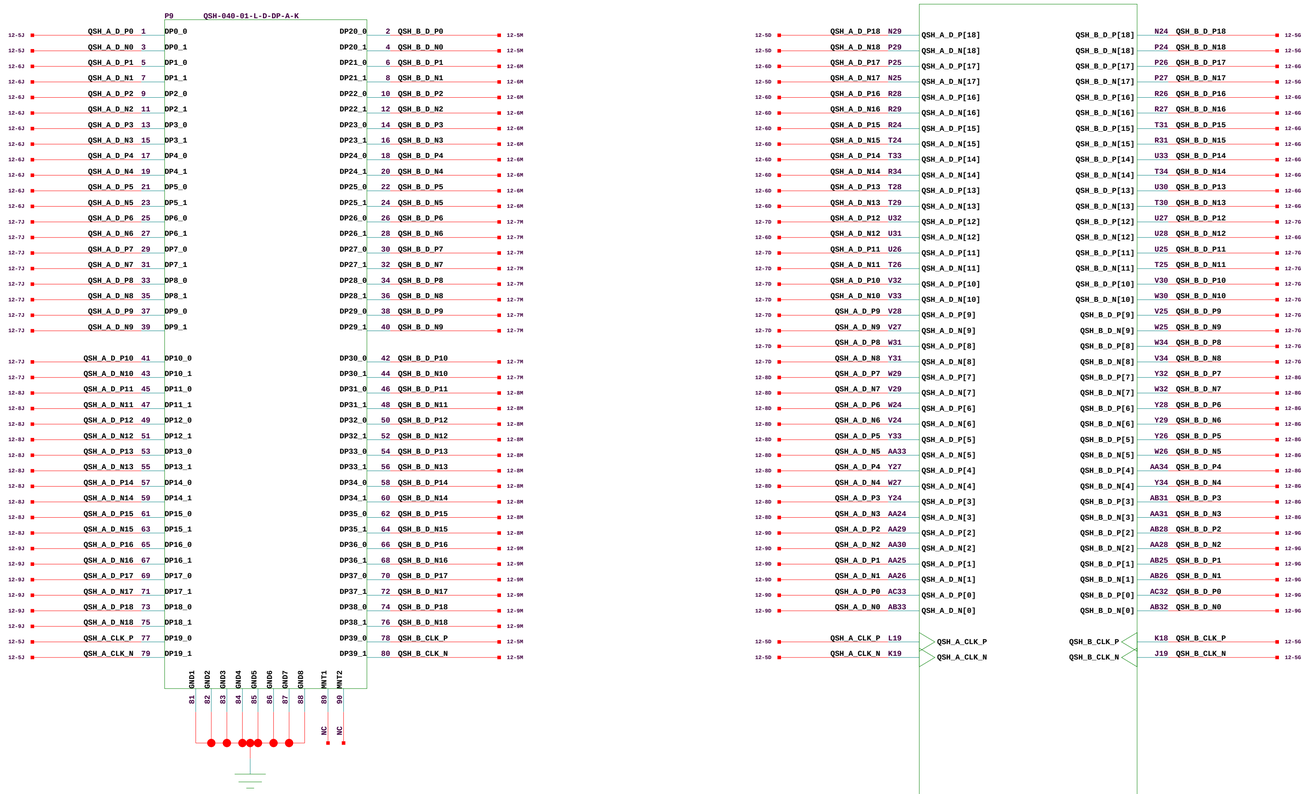




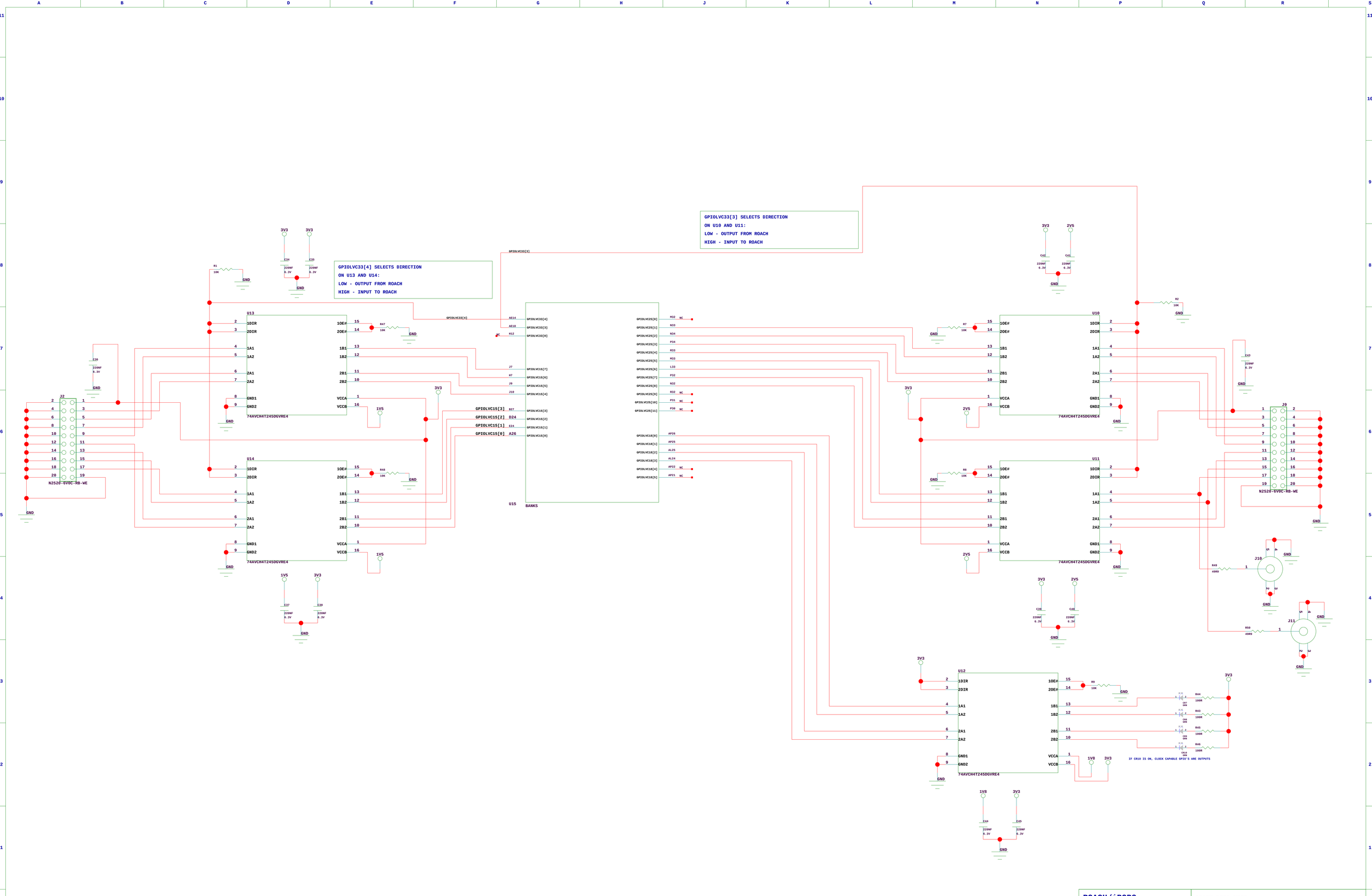




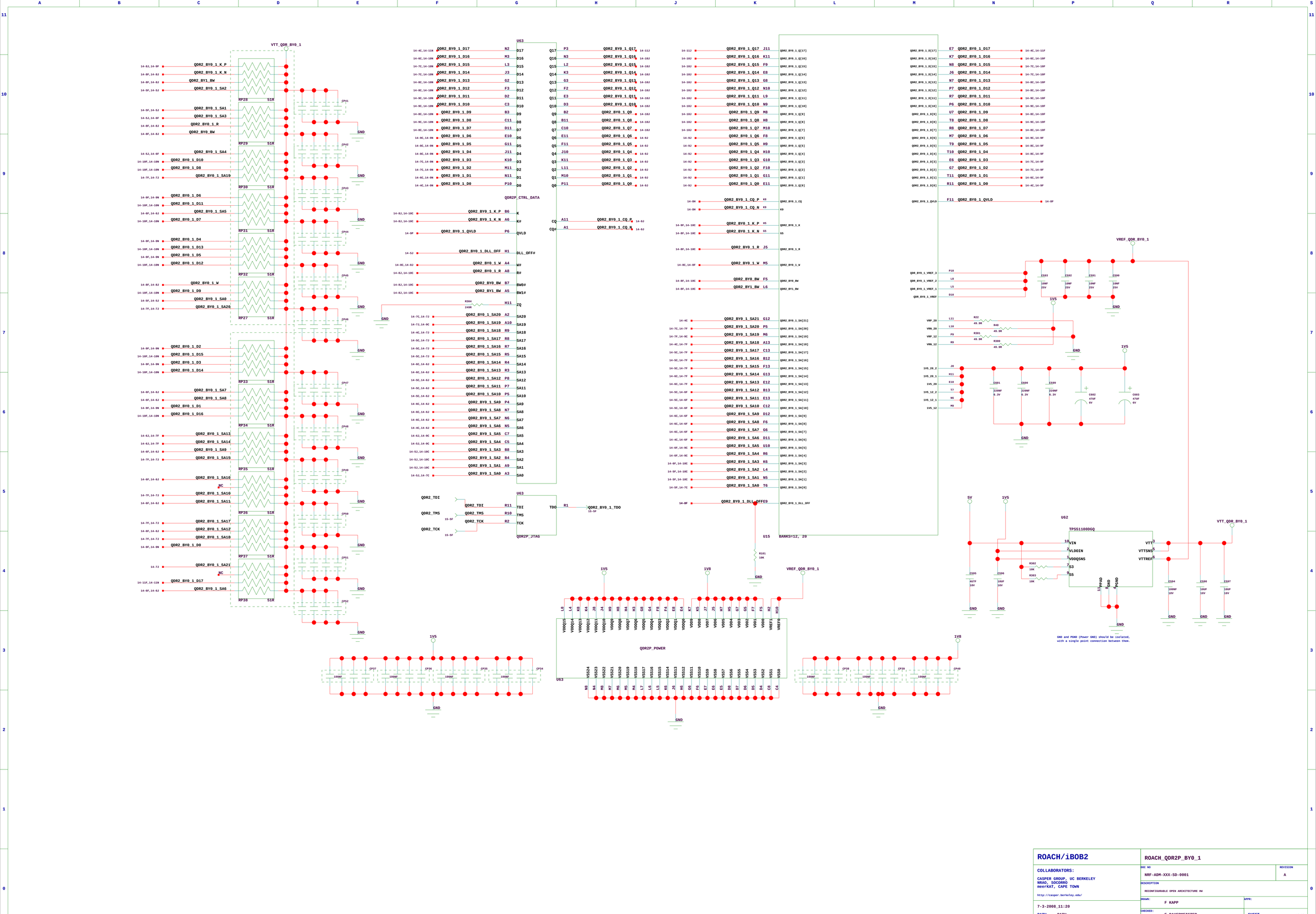
ROACH/iBOB2	**ROACH_DDR2_DIMM**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-3-2008_11:20 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 11 OF 25



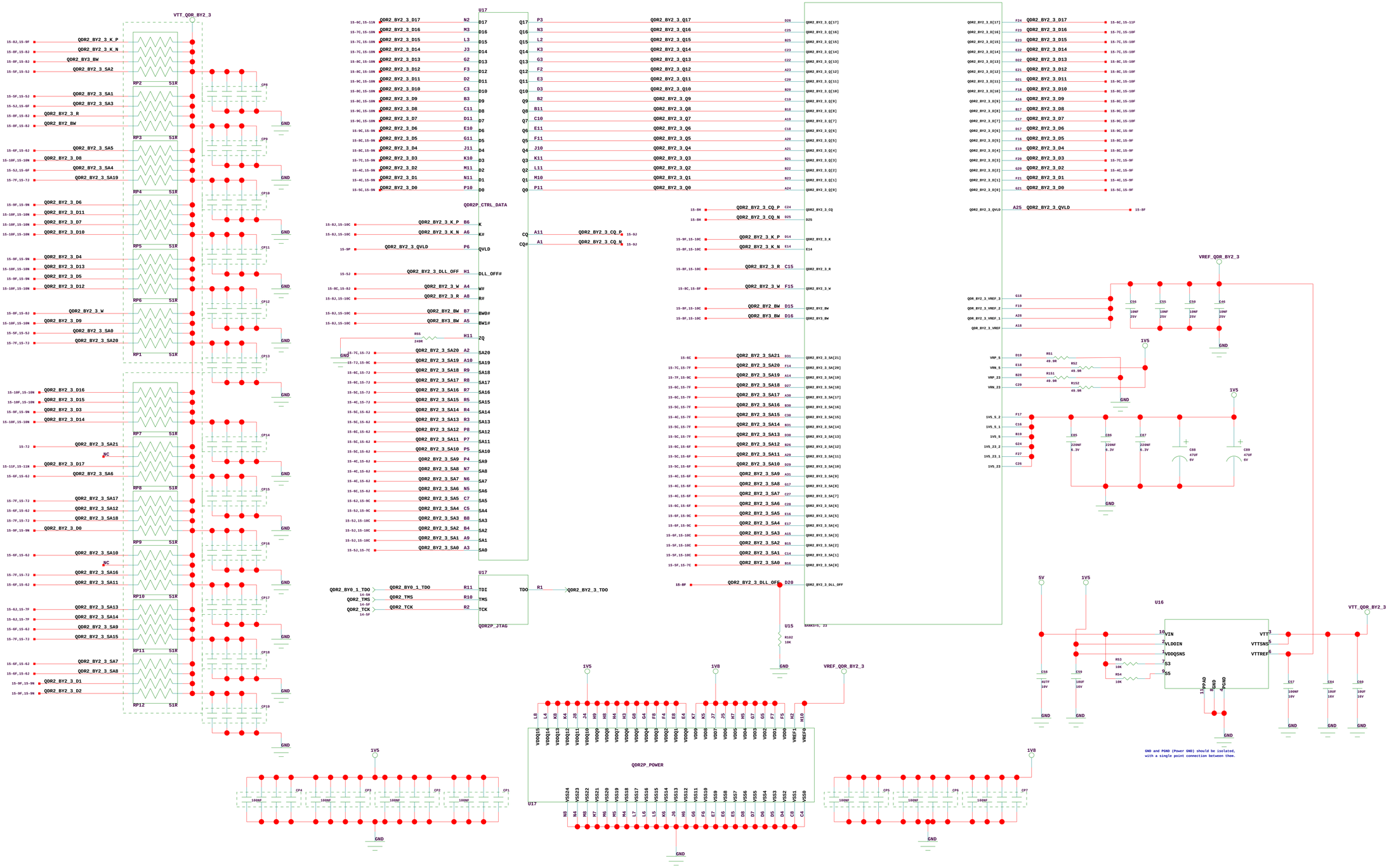
ROACH/iBOB2		ROACH_DIFF_GPIO	
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/		DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
		DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW	
7-3-2008_11:20 PATH PATH		DRAWN: F KAPP	APPR:
		CHECKED: E BAUERMEISTER	SHEET 12 OF 25



ROACH/iBOB2	**ROACH_GPIO_MISC**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-3-2008_11:20 PATH PATH	DRAWN: F KAPP — APPR:
	CHECKED: E BAUERMEISTER — SHEET 13 OF 25



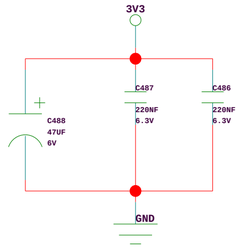
ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS:	DOC NO: NRF-ADM-XXX-SD-0001
CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN	REVISION: A
http://casper.berkeley.edu/	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-3-2008_11:20	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 14 OF 25

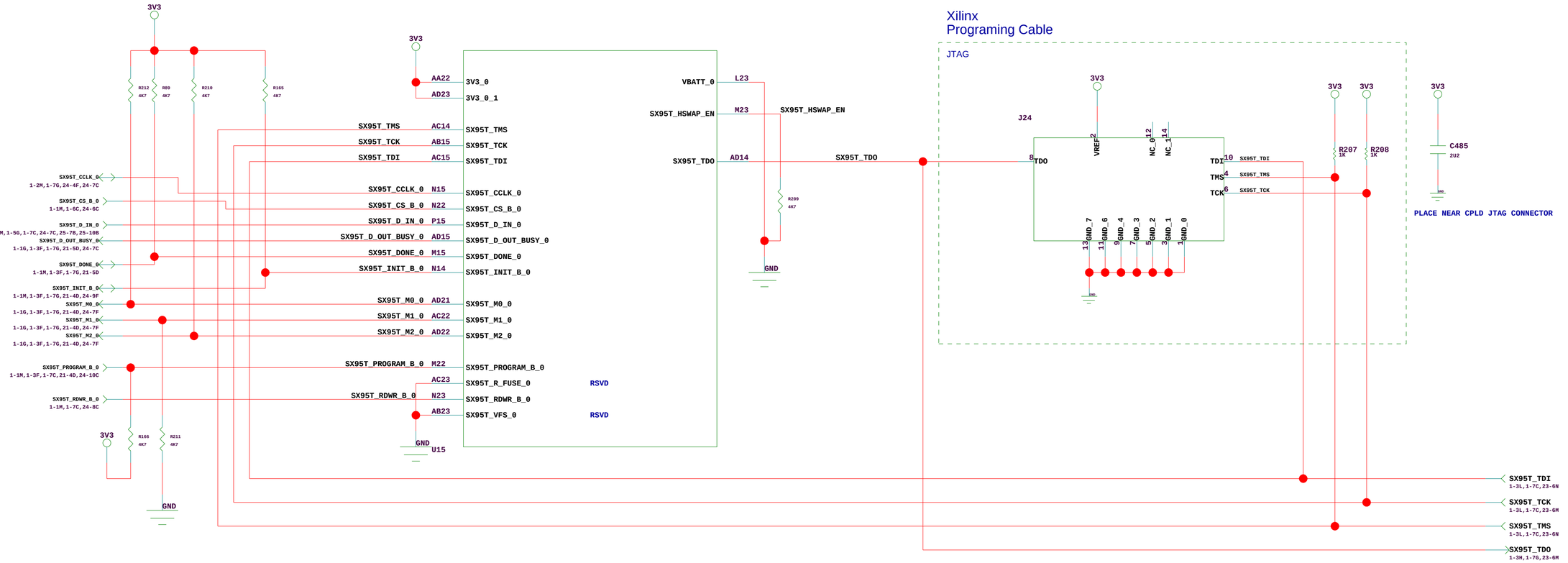


ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-3-2008_11:20 PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 15 OF 25

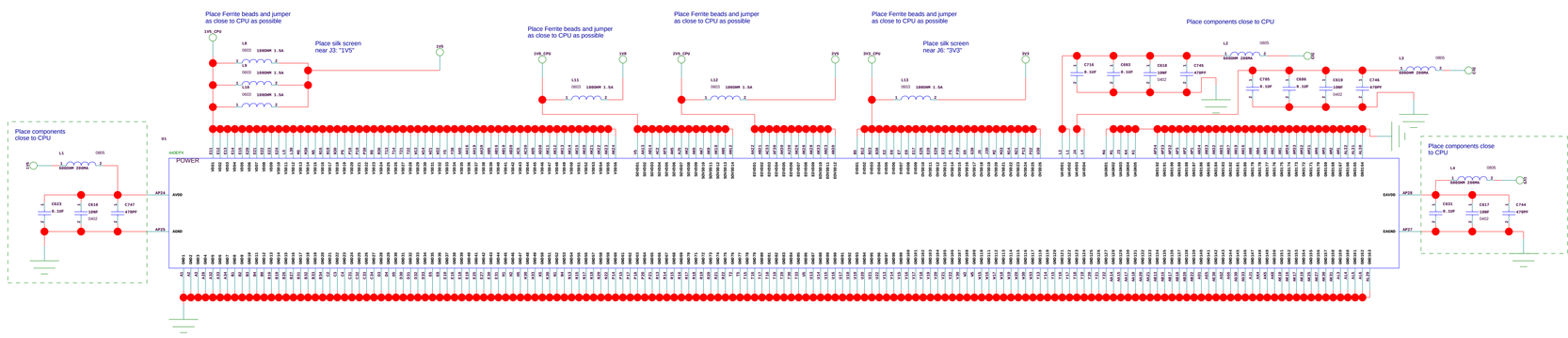
TBD

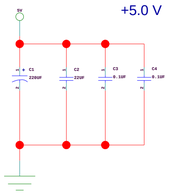
VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

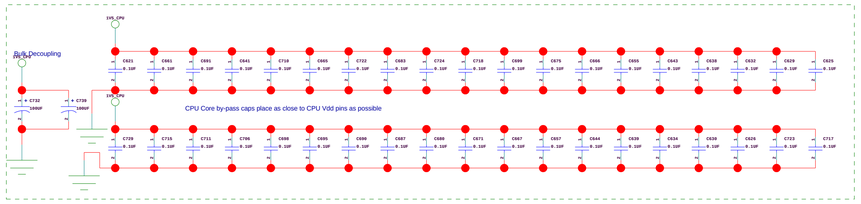


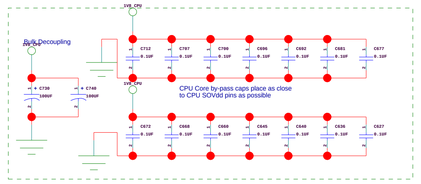


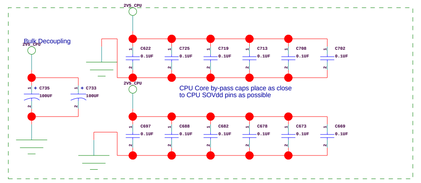
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
7-3-2008_11:20 PATH PATH	





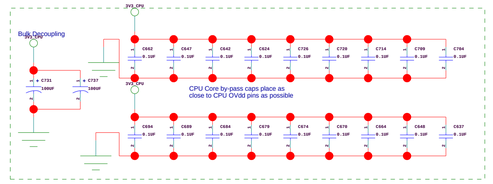


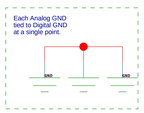




REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

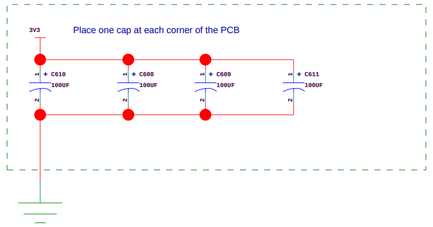
REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2





ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: **CASPER GROUP, UC BERKELEY** **NRAO, SOCORRO** **meerKAT, CAPE TOWN** http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET: 17 OF 25
7-3-2008_11:20 PATH PATH	

REMOVED 3V3 GENERATION



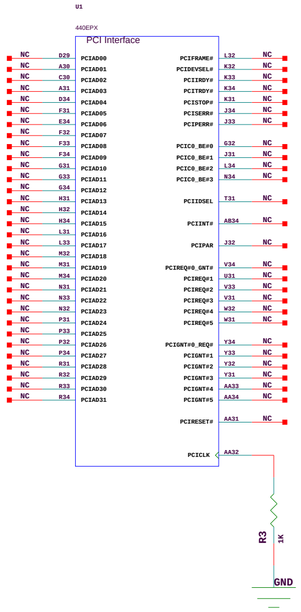
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

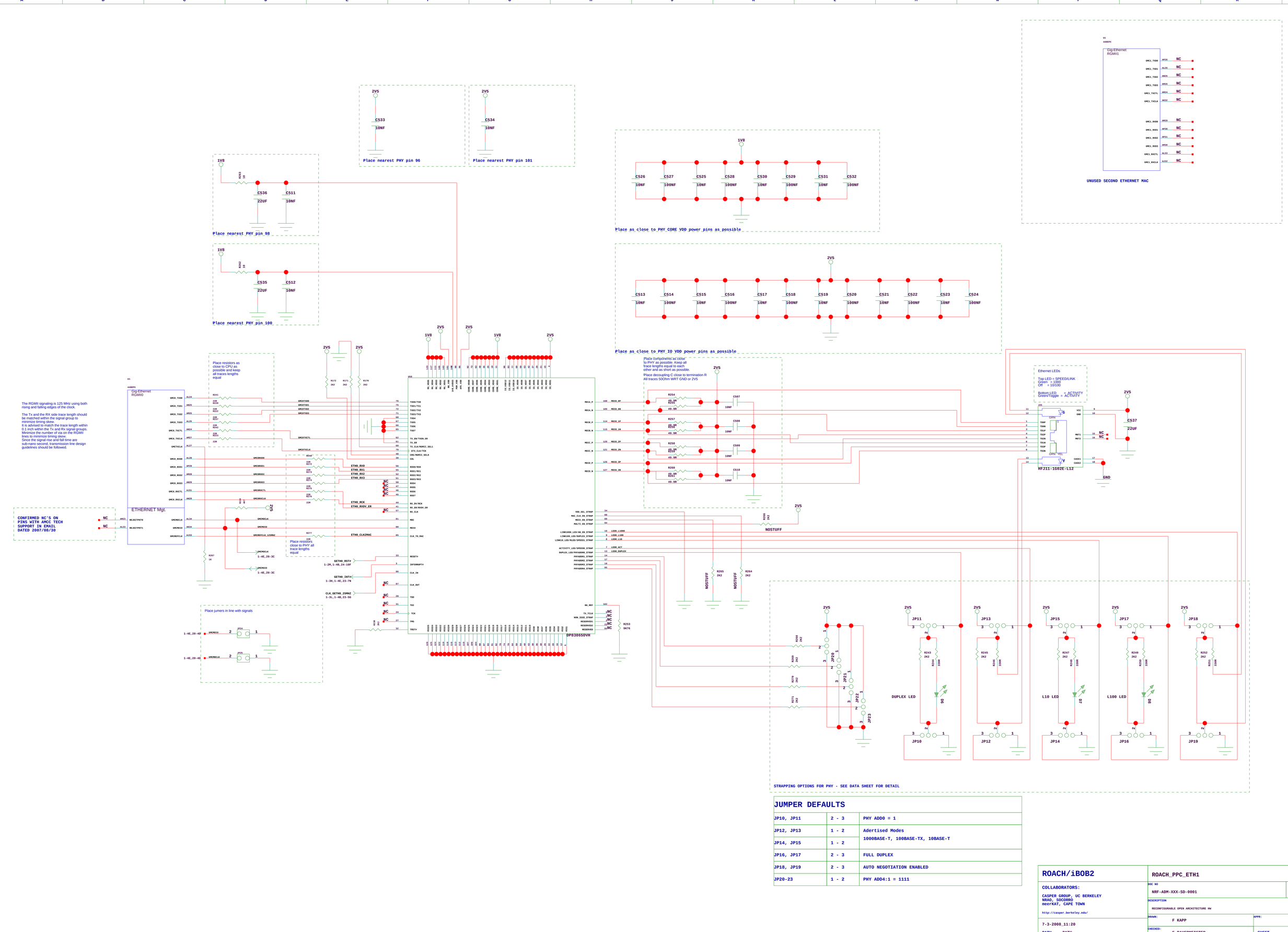
REMOVED +2V5 GENERATION

ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET 18 OF 25
7-3-2008_11:20 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-3-2008_11:20 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25



JUMPER DEFAULTS

JP10, JP11	2 - 3	PHY ADD0 = 1
JP12, JP13	1 - 2	Adertised Modes 1000BASE-T, 100BASE-TX, 10BASE-T
JP14, JP15	1 - 2	
JP16, JP17	2 - 3	FULL DUPLEX
JP18, JP19	2 - 3	AUTO NEGOTIATION ENABLED
JP20-23	1 - 2	PHY ADD4:1 = 1111

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

7-3-2008_11:20

PATH PATH

ROACH_PPC_ETH1

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 20 OF 25

U1
USB 2.0 DEVICE
440EPX

USB2CLK — A5 — NC

SECOND USB INTERFACE NOT IMPLEMENTED

NOTE:
SX95T_D_IN_0 ON SHEET 25, GPIO10

GPIO28/USB2TXVAL	C6	SX95T_D_OUT_BUSY_0	SX95T_D_OUT_BUSY_0 1-1G,1-3F,1-7G,16-4B,24-7C
USB2TXRDY_REFEN	B6	NC	
USB2RXACT_HOLDREQ_RCVINH	D7	NC	
USB2RXVAL_LEAKTEST2	C8	NC	
GPIO27/USB2RXERR_EXTREQ#	A4	SX95T_DONE_0	SX95T_DONE_0 1-1M,1-3F,1-7G
GPIO30/USB2XCVRSEL_EXTACK#	M3	SX95T_INIT_B_0	SX95T_INIT_B_0 1-1M,1-3F,1-7G,24-9F
GPIO31/USB2TERMSEL_BUSREQ	P4		
USB2LS0_DRVINH1	R2	SX95T_M0_0	SX95T_M0_0 1-1G,1-3F,1-7G,16-3B,24-7F
USB2LS1_LEAKTEST_HOLDPRI	P1	NC	
GPIO32/USB2OM0	R3	SX95T_M1_0	SX95T_M1_0 1-1G,1-3F,1-7G,16-3B,24-7F
GPIO33/USB2OM1	R4		
GPIO29/USB2SUSP_HOLDACK	C5	SX95T_M2_0	SX95T_M2_0 1-1G,1-3F,1-7G,16-3B,24-7F
		SX95T_PROGRAM_B_0	SX95T_PROGRAM_B_0 1-1M,1-3F,1-7C,16-3B,24-10C

NOTE:
USB HOST ONLY

USB 2.0 PHY
HOST/DEVICE

USB2XCVR — J2 — USB2_XCVR_D+
USB2XCVR# — J1 — USB2_XCVR_D-
USB2REXT — L3 — R182 3K4 0402 — GND
USB2XTAL — N2
USB2XTAL# — N3

CLK_USB2_48MHZ 1-3B,1-3L,23-4G — CLK_USB2_48MHZ

CRITICAL PLACEMENT
Place SP2 very close to P6

SP2 SOT23 PGB102ST23WR
PGB102ST23WR SP2
GND

5V — PTC1 1206L050 500MA — 1 — 2
C614 220UF 10V
C612 100NF 10V
C613 1NF 50V

VR4 0603 5.5V 20A

P6 NONE 1X4 USBA
1 VCC
2 D-
3 D+
4 GND
5
6
292303-1

GND

ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25
7-3-2008_11:20 PATH PATH	

Z_ADDR

DDR_PA[15:0]

DDR_PDQ[63:0]

PPC_ECC[7:0]

DDR SDRAM

U1 — 44GEPX

DDR_PDQ0	AB2	MEMDATA00	MEMADDR00
DDR_PDQ1	AF22	MEMDATA01	MEMADDR01
DDR_PDQ2	AK26	MEMDATA02	MEMADDR02
DDR_PDQ3	AL28	MEMDATA03	MEMADDR03
DDR_PDQ4	AJ22	MEMDATA04	MEMADDR04
DDR_PDQ5	AK22	MEMDATA05	MEMADDR05
DDR_PDQ6	AB21	MEMDATA06	MEMADDR06
DDR_PDQ7	AF21	MEMDATA07	MEMADDR07
DDR_PDQ8	AF28	MEMDATA08	MEMADDR08
DDR_PDQ9	AL18	MEMDATA09	MEMADDR09
DDR_PDQ10	AB17	MEMDATA10	MEMADDR10
DDR_PDQ11	AF17	MEMDATA11	MEMADDR11
DDR_PDQ12	AB26	MEMDATA12	MEMADDR12
DDR_PDQ13	AF18	MEMDATA13	MEMADDR13
DDR_PDQ14	AB18	MEMDATA14	
DDR_PDQ15	AF16	MEMDATA15	
DDR_PDQ16	AB16	MEMDATA16	
DDR_PDQ17	AF15	MEMDATA17	
DDR_PDQ18	AF14	MEMDATA18	
DDR_PDQ19	AL17	MEMDATA19	
DDR_PDQ20	AB17	MEMDATA20	
DDR_PDQ21	AB13	MEMDATA21	
DDR_PDQ22	AB15	MEMDATA22	
DDR_PDQ23	AF13	MEMDATA23	
DDR_PDQ24	AB13	MEMDATA24	
DDR_PDQ25	AB12	MEMDATA25	
DDR_PDQ26	AF12	MEMDATA26	
DDR_PDQ27	AL12	MEMDATA27	
DDR_PDQ28	AB14	MEMDATA28	
DDR_PDQ29	AB14	MEMDATA29	
DDR_PDQ30	AL13	MEMDATA30	
DDR_PDQ31	AB12	MEMDATA31	
DDR_PDQ32	AF3	MEMDATA32	
DDR_PDQ33	AF1	MEMDATA33	
DDR_PDQ34	AB4	MEMDATA34	
DDR_PDQ35	AB3	MEMDATA35	
DDR_PDQ36	AB1	MEMDATA36	
DDR_PDQ37	AF2	MEMDATA37	
DDR_PDQ38	AE2	MEMDATA38	
DDR_PDQ39	AE1	MEMDATA39	
DDR_PDQ40	AC2	MEMDATA40	
DDR_PDQ41	AC1	MEMDATA41	
DDR_PDQ42	AA4	MEMDATA42	
DDR_PDQ43	AA3	MEMDATA43	
DDR_PDQ44	AA2	MEMDATA44	
DDR_PDQ45	AC4	MEMDATA45	
DDR_PDQ46	AB1	MEMDATA46	
DDR_PDQ47	AB2	MEMDATA47	
DDR_PDQ48	Y3	MEMDATA48	
DDR_PDQ49	Y2	MEMDATA49	
DDR_PDQ50	Y4	MEMDATA50	
DDR_PDQ51	Y1	MEMDATA51	
DDR_PDQ52	AA2	MEMDATA52	
DDR_PDQ53	AA1	MEMDATA53	
DDR_PDQ54	W3	MEMDATA54	
DDR_PDQ55	W1	MEMDATA55	
DDR_PDQ56	V1	MEMDATA56	
DDR_PDQ57	U2	MEMDATA57	
DDR_PDQ58	W3	MEMDATA58	
DDR_PDQ59	W1	MEMDATA59	
DDR_PDQ60	Y4	MEMDATA60	
DDR_PDQ61	V1	MEMDATA61	
DDR_PDQ62	T3	MEMDATA62	
DDR_PDQ63	T3	MEMDATA63	

DDR_PA0	AM5	MEMADDR00	
DDR_PA1	AP4	MEMADDR01	
DDR_PA2	AM5	MEMADDR02	
DDR_PA3	AM6	MEMADDR03	
DDR_PA4	AP6	MEMADDR04	
DDR_PA5	AN6	MEMADDR05	
DDR_PA6	AL7	MEMADDR06	
DDR_PA7	AN7	MEMADDR07	
DDR_PA8	AM7	MEMADDR08	
DDR_PA9	AP7	MEMADDR09	
DDR_PA10	AL2	MEMADDR10	
DDR_PA11	AL8	MEMADDR11	
DDR_PA12	AN8	MEMADDR12	
DDR_PA13	AN4	MEMADDR13	
DDR_PBA0	AJ3	BA0	
DDR_PBA1	AK3	BA1	
DDR_PBA2	AP8	BA2	
DDR_PRAS#	AJ4	RAS#	
DDR_PCAS#	AN4	CAS#	
DDR_PWE#	AJ2	WE#	

DDR_PDM0	AL21	DM0	
DDR_PDM1	AP18	DM1	
DDR_PDM2	AP15	DM2	
DDR_PDM3	AL14	DM3	
DDR_PDM4	AD4	DM4	
DDR_PDM5	AB3	DM5	
DDR_PDM6	Y3	DM6	
DDR_PDM7	V3	DM7	
DDR_PDM8	AN18	DM8	

DDR_PDQS0	AM21	DQS0	
DDR_PDQS1	AM19	DQS1	
DDR_PDQS2	AL15	DQS2	
DDR_PDQS3	AM13	DQS3	
DDR_PDQS4	AB3	DQS4	
DDR_PDQS5	AB4	DQS5	
DDR_PDQS6	W4	DQS6	
DDR_PDQS7	T4	DQS7	
DDR_PDQS8	AP10	DQS8	

DDR_PODT0	AN3	MEMDT0	
DDR_PODT1	AG1	MEMDT1	
DDR_PCS0#	AN2	BANKSEL#0	
DDR_PCS1#	AM1	BANKSEL#1	
DDR_PCKE	AN9	MEMCKE0	
DDR_PCLKOUT	AL1	MEMCLKOUT	
DDR_PCLKOUT#	AK1	MEMCLKOUT#	

PPC_ECC0	AM11	ECC0	
PPC_ECC1	AL11	ECC1	
PPC_ECC2	AN9	ECC2	
PPC_ECC3	AL9	ECC3	
PPC_ECC4	AM11	ECC4	
PPC_ECC5	AN11	ECC5	
PPC_ECC6	AM10	ECC6	
PPC_ECC7	AP9	ECC7	

SVREF1A	Y4	SVREF1A	
SVREF1B	AL19	SVREF1B	
SVREF2A	AF4	SVREF2A	
SVREF2B	AL19	SVREF2B	

J8

DDR2_DIMM_CB7	168	PPC_ECC7	
DDR2_DIMM_CB6	167	PPC_ECC6	
DDR2_DIMM_CB5	162	PPC_ECC5	
DDR2_DIMM_CB4	161	PPC_ECC4	
DDR2_DIMM_CB3	49	PPC_ECC3	
DDR2_DIMM_CB2	48	PPC_ECC2	
DDR2_DIMM_CB1	43	PPC_ECC1	
DDR2_DIMM_CB0	42	PPC_ECC0	
DDR2_DIMM_DQ[63]	236	DDR_PDQ63	
DDR2_DIMM_DQ[62]	235	DDR_PDQ62	
DDR2_DIMM_DQ[61]	230	DDR_PDQ61	
DDR2_DIMM_DQ[60]	229	DDR_PDQ60	
DDR2_DIMM_DQ[59]	117	DDR_PDQ59	
DDR2_DIMM_DQ[58]	116	DDR_PDQ58	
DDR2_DIMM_DQ[57]	111	DDR_PDQ57	
DDR2_DIMM_DQ[56]	110	DDR_PDQ56	
DDR2_DIMM_DQ[55]	227	DDR_PDQ55	
DDR2_DIMM_DQ[54]	226	DDR_PDQ54	
DDR2_DIMM_DQ[53]	218	DDR_PDQ53	
DDR2_DIMM_DQ[52]	217	DDR_PDQ52	
DDR2_DIMM_DQ[51]	108	DDR_PDQ51	
DDR2_DIMM_DQ[50]	107	DDR_PDQ50	
DDR2_DIMM_DQ[49]	99	DDR_PDQ49	
DDR2_DIMM_DQ[48]	98	DDR_PDQ48	
DDR2_DIMM_DQ[47]	215	DDR_PDQ47	
DDR2_DIMM_DQ[46]	214	DDR_PDQ46	
DDR2_DIMM_DQ[45]	209	DDR_PDQ45	
DDR2_DIMM_DQ[44]	208	DDR_PDQ44	
DDR2_DIMM_DQ[43]	96	DDR_PDQ43	
DDR2_DIMM_DQ[42]	95	DDR_PDQ42	
DDR2_DIMM_DQ[41]	90	DDR_PDQ41	
DDR2_DIMM_DQ[40]	89	DDR_PDQ40	
DDR2_DIMM_DQ[39]	206	DDR_PDQ39	
DDR2_DIMM_DQ[38]	205	DDR_PDQ38	
DDR2_DIMM_DQ[37]	200	DDR_PDQ37	
DDR2_DIMM_DQ[36]	199	DDR_PDQ36	
DDR2_DIMM_DQ[35]	87	DDR_PDQ35	
DDR2_DIMM_DQ[34]	86	DDR_PDQ34	
DDR2_DIMM_DQ[33]	81	DDR_PDQ33	
DDR2_DIMM_DQ[32]	80	DDR_PDQ32	
DDR2_DIMM_DQ[31]	159	DDR_PDQ31	
DDR2_DIMM_DQ[30]	158	DDR_PDQ30	
DDR2_DIMM_DQ[29]	153	DDR_PDQ29	
DDR2_DIMM_DQ[28]	152	DDR_PDQ28	
DDR2_DIMM_DQ[27]	40	DDR_PDQ27	
DDR2_DIMM_DQ[26]	39	DDR_PDQ26	
DDR2_DIMM_DQ[25]	34	DDR_PDQ25	
DDR2_DIMM_DQ[24]	33	DDR_PDQ24	
DDR2_DIMM_DQ[23]	150	DDR_PDQ23	
DDR2_DIMM_DQ[22]	149	DDR_PDQ22	
DDR2_DIMM_DQ[21]	144	DDR_PDQ21	
DDR2_DIMM_DQ[20]	143	DDR_PDQ20	
DDR2_DIMM_DQ[19]	31	DDR_PDQ19	
DDR2_DIMM_DQ[18]	30	DDR_PDQ18	
DDR2_DIMM_DQ[17]	25	DDR_PDQ17	
DDR2_DIMM_DQ[16]	24	DDR_PDQ16	
DDR2_DIMM_DQ[15]	141	DDR_PDQ15	
DDR2_DIMM_DQ[14]	140	DDR_PDQ14	
DDR2_DIMM_DQ[13]	132	DDR_PDQ13	
DDR2_DIMM_DQ[12]	131	DDR_PDQ12	
DDR2_DIMM_DQ[11]	22	DDR_PDQ11	
DDR2_DIMM_DQ[10]	21	DDR_PDQ10	
DDR2_DIMM_DQ[9]	13	DDR_PDQ9	
DDR2_DIMM_DQ[8]	12	DDR_PDQ8	
DDR2_DIMM_DQ[7]	129	DDR_PDQ7	
DDR2_DIMM_DQ[6]	128	DDR_PDQ6	
DDR2_DIMM_DQ[5]	123	DDR_PDQ5	
DDR2_DIMM_DQ[4]	122	DDR_PDQ4	
DDR2_DIMM_DQ[3]	10	DDR_PDQ3	
DDR2_DIMM_DQ[2]	9	DDR_PDQ2	
DDR2_DIMM_DQ[1]	4	DDR_PDQ1	
DDR2_DIMM_DQ[0]	3	DDR_PDQ0	
DDR2_DIMM_SA2	101		
DDR2_DIMM_SA1	240		
DDR2_DIMM_SA0	239		
DDR2_DIMM_SCL	120	I2C0_SCLK	1-2B,1-5L,1-9B,2-2P,2S-5A
DDR2_DIMM_SDA	119	I2C0_SDATA	1-2B,1-5L,1-9E

879160001

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA2	22-9D,22-10L
DDR2_DIMM_BA[1]	190	DDR_PBA1	22-9L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-7L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	DDR_PCLKOUT2	
DDR2_DIMM_CK_N[2]	221	DDR_PCLKOUT2#	
DDR2_DIMM_CK_P[1]	137	DDR_PCLKOUT1	
DDR2_DIMM_CK_N[1]	138	DDR_PCLKOUT1#	
DDR2_DIMM_CK_P[0]	185	DDR_PCLKOUT0	
DDR2_DIMM_CK_N[0]	186	DDR_PCLKOUT0#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-8D,22-11L
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-8D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	1-2B,1-2M,24-10F
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D
PAR_OUT	55	PPC_DDR2_ERROR	1
PAR_IN	68	PAR_IN	1

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J8

VSS_64	237	187	VDD_9
VSS_63	234	184	VDD_8
VSS_62	231	178	VDD_7
VSS_61	228	172	VDD_6
VSS_60	225	69	VDD_5
VSS_59	222	67	VDD_4
VSS_58	219	64	VDD_3
VSS_57	216	59	VDD_2
VSS_56	213	53	VDD_1
VSS_55	210		
VSS_54	207	194	VDDQ_11
VSS_53	204	191	VDDQ_10
VSS_52	201	181	VDDQ_9
VSS_51	198	175	VDDQ_8
VSS_50	169	170	VDDQ_7
VSS_49	166	78	VDDQ_6
VSS_48	163	75	VDDQ_5
VSS_47	160	72	VDDQ_4
VSS_46	157	62	VDDQ_3
VSS_45	154	56	VDDQ_2
VSS_44	151	51	VDDQ_1
VSS_43	148		
VSS_42	145		
VSS_41	142		
VSS_40	139		
VSS_39	136		
VSS_38	133		
VSS_37	130		
VSS_36	127		
VSS_35	124		
VSS_34	121		
VSS_33	118		
VSS_32	115		
VSS_31	112		
VSS_30	109		
VSS_29	106		
VSS_28	103		
VSS_27	100		
VSS_26	97		
VSS_25	94		
VSS_24	91		
VSS_23	88		
VSS_22	85		
VSS_21	82		
VSS_20	79		
VSS_19	66		
VSS_18	65		
VSS_17	50		
VSS_16	47		
VSS_15	44		
VSS_14	41		
VSS_13	38		
VSS_12	35		
VSS_11	32		
VSS_10	29		
VSS_9	26		
VSS_8	23		
VSS_7	20		
VSS_6	17		
VSS_5	14		
VSS_4	11		
VSS_3	8		
VSS_2	5		
VSS_1	2		

879160001

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

DDR_VTT

22-8K,22-8D	DDR_PCKE	RP24	CP26
	DDR_PA15		
	DDR_PA14		
22-8K,22-8D	DDR_PBA2		
	DDR_PA12	RP23	CP28
	DDR_PA11		
	DDR_PA9		
	NC		
	DDR_PA7	RP22	CP29
	DDR_PA8		
	DDR_PA6		
	DDR_PA5		
	DDR_PA4	RP21	CP30
	DDR_PA3		
	DDR_PA1		
	DDR_PA2		
22-8K,22-8D	DDR_PA0	RP25	CP32
	DDR_PBA1		
	DDR_PA10		
22-8K,22-8D	DDR_PBA0		
22-7K,22-8D	DDR_PRAS#	RP26	CP31
22-3K,22-8D	DDR_PWE#		
22-3K,22-8D	DDR_PCS0#		
22-8K,22-8D	DDR_PCAS#		
22-3K,22-8D	DDR_PCS1#	RP19	CP33
22-8D	DDR_PODT0		
	DDR_PA13		
22-8D	DDR_PODT1		

GND

PowerPC DRAM Interface:

- DDR2 240 pin DIMM
- 72 bit ECC
- Unbuffered and Registered DIMMs supported
- Up to 2GB supported
- CAS Latencies: 2, 2.5 or 3
- Clock Frequencies: 133MHz to 166MHz
- Single Ended Strobes

DDR_VREF_0V9 / 3V3 / 1V8

VREF 1 — VDDSPD 238

VDD_11 197, VDD_10 189, VDD_9 187, VDD_8 184, VDD_7 178, VDD_6 172, VDD_5 69, VDD_4 67, VDD_3 64, VDD_2 59, VDD_1 53

VDDQ_11 194, VDDQ_10 191, VDDQ_9 181, VDDQ_8 175, VDDQ_7 170, VDDQ_6 78, VDDQ_5 75, VDDQ_4 72, VDDQ_3 62, VDDQ_2 56, VDDQ_1 51

GND

5V / 1V8 / DDR_VREF_0V9 / DDR_VTT

U32 TPS51100DGQ

VIN	10	5V
VLDOIN	2	5V
VDDQSNS	1	1V8
S3	7	1V8
S5	8	1V8
VTT	3	DDR_VTT
VTTSNS	5	DDR_VTT
VTTREF	6	DDR_VREF_0V9
PPAD	11	
GND	9	
PGND	4	

R230 10K, R229 10K, R6 120R

C459 4U7F 10V, C456 10UF 10V, C453 100NF 10V, C21 22PF, C457 10UF 10V, C458 10UF 10V

GND

1V8 / Z_IN / Z_OUT / Z_FB

L17 0603 1000OHM 1.5A

C329 4U7F 10V, C300 100NF 10V, C63 10NF 25V

R167 10K

R168 120R

R169 120R

U6 CDCU877ARHAT

AVDD	8	1V8
AGND	7	GND
OE	22	1V8
OS	21	GND
CLK	4	DDR_PCLKOUT
CLK#	5	DDR_PCLKOUT#
FBIN	27	FBOUT
FBIN#	26	FBOUT#
GND1	18	GND
GND2	41	GND
Y0	38	NC
Y0#	37	NC
Y1	39	DDR_PCLKOUT1
Y1#	40	DDR_PCLKOUT1#
Y2	3	NC
Y2#	2	NC
Y3	11	NC
Y3#	12	NC
Y4	14	NC
Y4#	13	NC
Y5	34	NC
Y5#	35	NC
Y6	33	NC
Y6#	32	NC
Y7	29	NC
Y7#	30	NC
Y8	19	DDR_PCLKOUT0
Y8#	18	DDR_PCLKOUT0#
Y9	16	DDR_PCLKOUT2
Y9#	17	DDR_PCLKOUT2#
FBOUT	24	FBOUT
FBOUT#	25	FBOUT#

FBOUT#, FBOUT

DDR_VREF_0V9 / 1V8 decoupling

C432 100NF 10V, C433 10NF 25V

C454 100NF 10V, C434 10NF 25V

C439 100NF 10V, C443 10NF 25V, C431 100NF 10V, C444 10NF 25V

C436 100NF 10V, C445 10NF 25V, C435 100NF 10V, C446 10NF 25V

C438 100NF 10V, C451 10NF 25V, C437 100NF 10V, C452 10NF 25V

C439 100NF 10V, C449 10NF 25V, C440 100NF 10V, C450 10NF 25V

C441 100NF 10V, C448 10NF 25V, C442 100NF 10V, C447 10NF 25V

PLACE NEAREST DDR2 MODULE PINS

PPC DDR2 LAYOUT NOTES

- ROUTE ALL DDR CLOCKS AS LENGTH MATCHED ONLY - DIFFERENTIAL ROUTING NOT REQUIRED
- CLOCK DELAYS MUST ADHERE TO THE FOLLOWING:
  Z_IN + Z_OUT - Z_FB = Z_ADDR + 500 ps (+-25 ps)
  WHERE:
  Z_IN = PROPAGATION DELAY ON DDR_PCLKOUT/DDR_PCLKOUT#
  Z_OUT = PROPAGATION DELAY ON DDR_PCLKOUTn/DDR_PCLKOUTn#
  Z_FB = PROPAGATION DELAY ON FBOUT/FBOUT#
  Z_ADDR = PROPAGATION DELAY ON DDR_PADD[13:0]
- DDR_PCLKOUTn/DDR_PCLKOUTn# NETS CAN BE SWAPPED ON CLOCK BUFFER TO EASE ROUTING
- ALL DQ, DQS, DM, ADDR, CMD AND CTRL LINES LENGTH MATCHED TO 400 ps
  MATCHING WITHIN BYTE LANE: 50 ps
  209 ps < TRACE LENGTH < 800 ps
- U6 THERMAL TAB TO BE CONNECTED TO GND PLANE WITH THERMAL VIAS

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

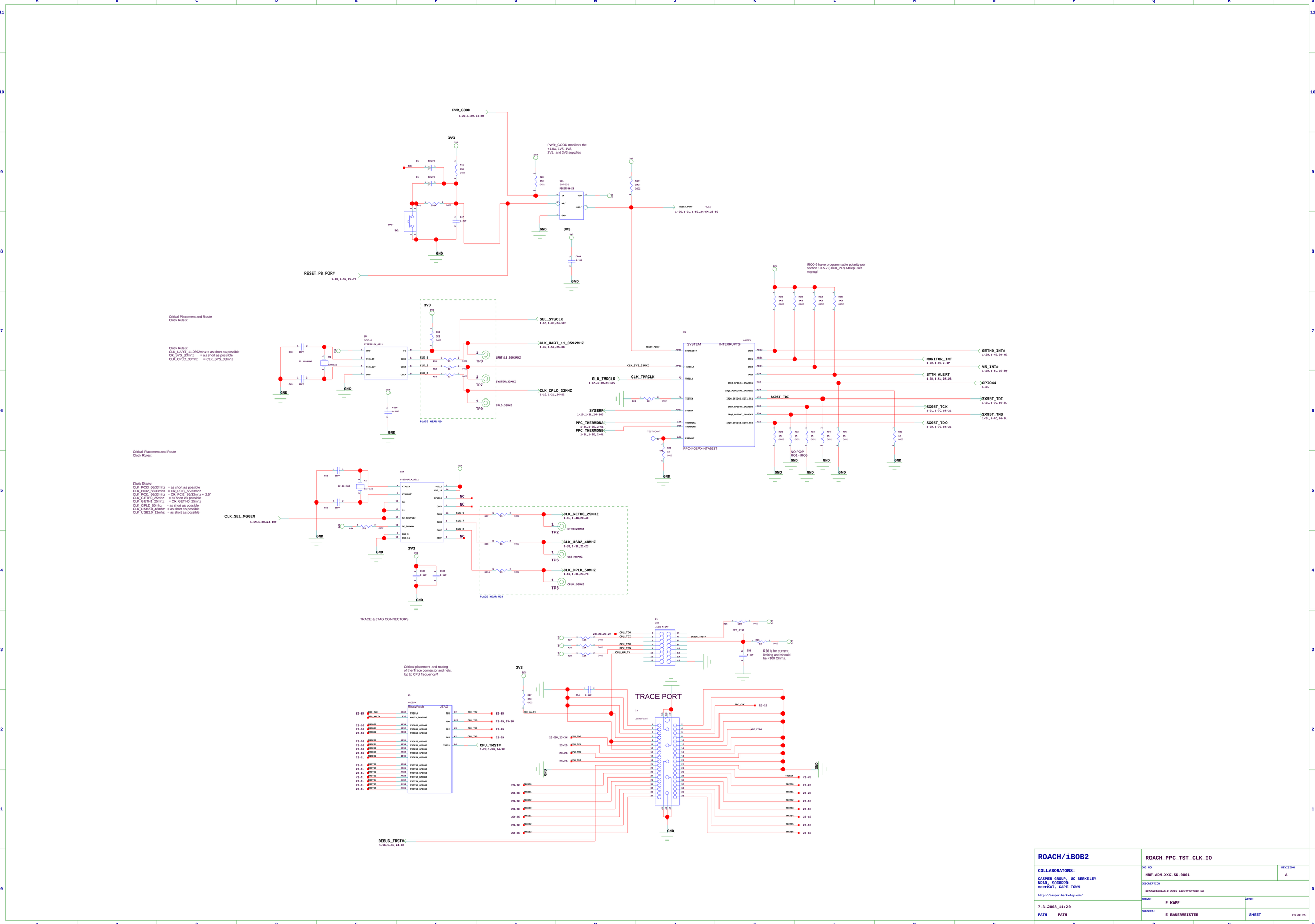
http://casper.berkeley.edu/

7-3-2008_11:20

PATH PATH

ROACH_PPC_DDR2

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	22 OF 25



ROACH/iBOB2	**ROACH_PPC_TST_CLK_IO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
7-3-2008_11:20	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 23 OF 25

roach_cpld_XC2C256_7VQ100C_pcb

CLK_TMCLK	4	PAD4	
SYSRR	7	PAD8	
EXT_RESETf	9	PAD10	
SX95T_PROGRAM_B_0	10	PAD12	
SX95T_DONE_0	11	PAD15	
PCS_2	12	PAD16	
PB_WI	13	PAD17	
DEBUG_TRSTf	14	PAD18	
CPU_TRSTn	15	PAD19	
FWBE_0#	16	PAD20	
PADO[27:31]	17	PADO27	
	18	PADO28	
	19	PADO29	
	20	PADO30	
	21	PADO31	
PDATA[0:7]	22	PDATA0	
	23	PDATA1	
	24	PDATA2	
	25	PDATA3	
	26	PDATA4	
	28	PDATA7	
CLK_CPLD_33MHZ	30	PAD48	
	31	PDATA6	
CLK_PERCLK	32	PAD50	
	33	PDATA5	
PDEX	34	PAD54	
SX95T_RDWR_B_0	35	PAD55	
CLK_CPLD_50MHZ	38	PAD59	
SX95T_D_IN_0	40	PAD64	
SX95T_D_OUT_BUSY_0	41	PAD65	
PER_CCLK_ENf	42	PAD66	
SX95T_CCLK_0	43	PAD67	
FRY_BYf	44	PAD68	
FWPC	45	PAD69	
EE1_WPC	46	PAD70	
EE2_BOOT_WPC	48	PAD73	
STTM_ASC	49	PAD74	
SELECTMAP_CS	50	PAD75	
	51	PAD76	NC
SX95T_CS_B_0	52	PAD77	
	53	PAD81	NC
PPC_RESET	54	PAD82	
SYS_CONFIG0	56	PAD86	
SYS_CONFIG1	57	PAD87	
SYS_CONFIG2	58	PAD88	
SYS_CONFIG3	59	PAD89	
SYS_CONFIG4	60	PAD90	
SYS_CONFIG5	61	PAD95	
SYS_CONFIG6	64	PAD100	
SYS_CONFIG7	66	PAD102	
	68	PAD105	NC
	69	PAD107	NC
	70	PAD108	NC
RESET_CPLD#	71	PAD109	
	74	PAD112	NC
	75	PAD113	NC

SYS_CONFIG[0:7] ← SYS_CONFIG[0:7] 1-2G,1-9E,2-2R

	142	PAD217	NC
	140	PAD214	NC
GETH0_RST#	139	PAD213	
PPC_DDR2_RESET_N	138	PAD212	
CLK_SEL_MGGEN	137	PAD211	
SEL_SYSCLK	136	PAD208	
	135	PAD207	NC
	134	PAD206	NC
	133	PAD204	NC
	132	PAD199	NC
SX95T_INIT_B_0	131	PAD197	
	130	PAD196	NC
	129	PAD195	
	128	PAD194	
	126	PAD192	
	125	PAD191	NC
	124	PAD190	NC
	121	PAD187	
DAT1	120	PAD186	
DAT0_DO	119	PAD178	
DAT7	118	PAD177	
DAT6	117	PAD176	
CLK_SCLK	116	PAD175	
DAT5	115	PAD173	
DAT4	114	PAD171	
CMD_DI	113	PAD169	
DAT3	112	PAD168	
DAT2	111	PAD167	
	110	PAD166	
	107	PAD163	
SX95T_M0_0	106	PAD162	
SX95T_M1_0	105	PAD161	
SX95T_M2_0	104	PAD160	
	103	PAD158	
RESET_PB_POR#	102	PAD156	
USER_LED0	101	PAD154	
USER_LED1	100	PAD152	
SYSERR#	98	PAD146	
RESET_BUFPOR#	97	PAD145	
	96	PAD144	
USER_DIP0	95	PAD143	
USER_DIP1	94	PAD142	
USER_DIP2	92	PAD138	
USER_DIP3	91	PAD137	
	88	PAD134	
	87	PAD133	
	86	PAD132	NC
	85	PAD131	NC
	83	PAD125	NC
	82	PAD121	NC
	81	PAD120	NC
	80	PAD119	NC
	79	PAD118	NC
	78	PAD117	NC
	77	PAD115	NC
	76	PAD114	NC

U54 XC2C256_7VQ144C

SD/MMC/MMCPLUS CONNECTOR

J17 SDSR13-A0-0005

CMD/DI	10	DAT0/DO	2
CLK/SCLK	6	DAT1	1
		DAT2	13
VDD	7	DAT3	12
VSS1	8	DAT4	11
VSS2	4	DAT5	9
		DAT6	5
SD_CD_COM	14	DAT7	3
SD_WP_COM	15		
		MNT1	16
		MNT2	17

BOOT_CFG0 1-1M,1-4G,25-1J
BOOT_CFG1 1-1M,1-4G,25-1J
BOOT_CFG2 1-1M,1-4G,25-1J

RESETS

CPU_TRSTn = '1' when JTAG_TRSTn = '1' and RESET_PORn = '1' else '0'; see errata sheet

Boot Configuration

SysErr will be used to drive Status LED (active H)

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

roach_cpld_XC2C256_7VQ100C_configpins

U54 XC2C256_7VQ144C

NC	2	PAD1
NC	3	PAD3
NC	5	PAD5
NC	6	PAD7
NC	39	PAD62
TDI	63	
TMS	65	
TCK	67	
TDO	122	
RESET_PORn	143	PAD218

1-2G,1-9L,23-9J,25-5G

Xilinx Programing Cable

JTAG

J22

TDO	8	
VREF	2	3V3
NC_0	12	
NC_1	14	
TDI	10	CPLD_TDI
TMS	4	CPLD_TMS
TCK	6	CPLD_TCK
GND_7	11	
GND_6	13	
GND_4	9	
GND_3	7	
GND_2	5	
GND_1	3	
GND_0	1	

R193 1K, R192 1K

PLACE NEAR CPLD JTAG CONNECTOR

roach_cpld_XC2C256_7VQ100C_powerpins

U54 XC2C256_7VQ144C

VCC	1	
VAUX	8	
VCCIO_3	27	
VCC_1	37	
VCCIO_4	55	
VCCIO_5	73	
VCC_2	84	
VCCIO_6	93	
VCCIO	109	
VCCIO_1	127	
VCCIO_2	141	
GND_3	29	
GND_4	36	
GND_5	47	
GND_6	62	
GND_7	72	
GND_8	89	
GND_9	99	
GND_10	108	
GND	123	
GND_1	144	
GND_2		

PLACE NEAR CPLD POWER PINS

R305 220R, R306 240R, R135 10K

PLACE AT END OF DAISY CHAIN

ENABLE PER_CLK CONNECTION TO CONFIGURATION I/F MUST CO-ORDINATE WITH SX95T_CCLK_0 AND MODE TO AVOID CLASH

SN74AHC1G125DCKT: PER_CCLK_ENf → DE#; CLK_PERCLK → A; SX95T_CCLK_0 ← Y; GND; VCC; C13 100NF 10V

CLK_PERCLK 1-1G,1-4L,24-8B,25-6F → SX95T_CCLK_0 1-2M,1-7G,24-7C

C473	100NF 10V	
C474	100NF 10V	
C475	100NF 10V	
C476	100NF 10V	
C477	100NF 10V	
C478	100NF 10V	
C479	100NF 10V	
C480	100NF 10V	
C481	100NF 10V	
C482	100NF 10V	
C483	100NF 10V	

C484 20Z

PLACE NEAR CPLD JTAG CONNECTOR

C615 0.1UF

PWR_GOOD 1-2G,1-3M,23-1DG

R197	330R	0402
R199	330R	0402
C61	68N	0402
C62	68N	0402

U35 SC70-5 74LVC1G08 VCC GND

R196	10K	0402
R195	10K	0402
R194	10K	0402
R198	10K	0402

R204	10K	0402
R205	10K	0402
R206	10K	0402

R200	1500	0402
R201	1500	0402
R202	1500	0402
R203	1500	0402

LED0	0805	CR3
LED1	0805	CR4
SYSERR	0805	CR5
RESET_BUFPOR	0805	CR6

SW2 4POLE User DIP-Switch

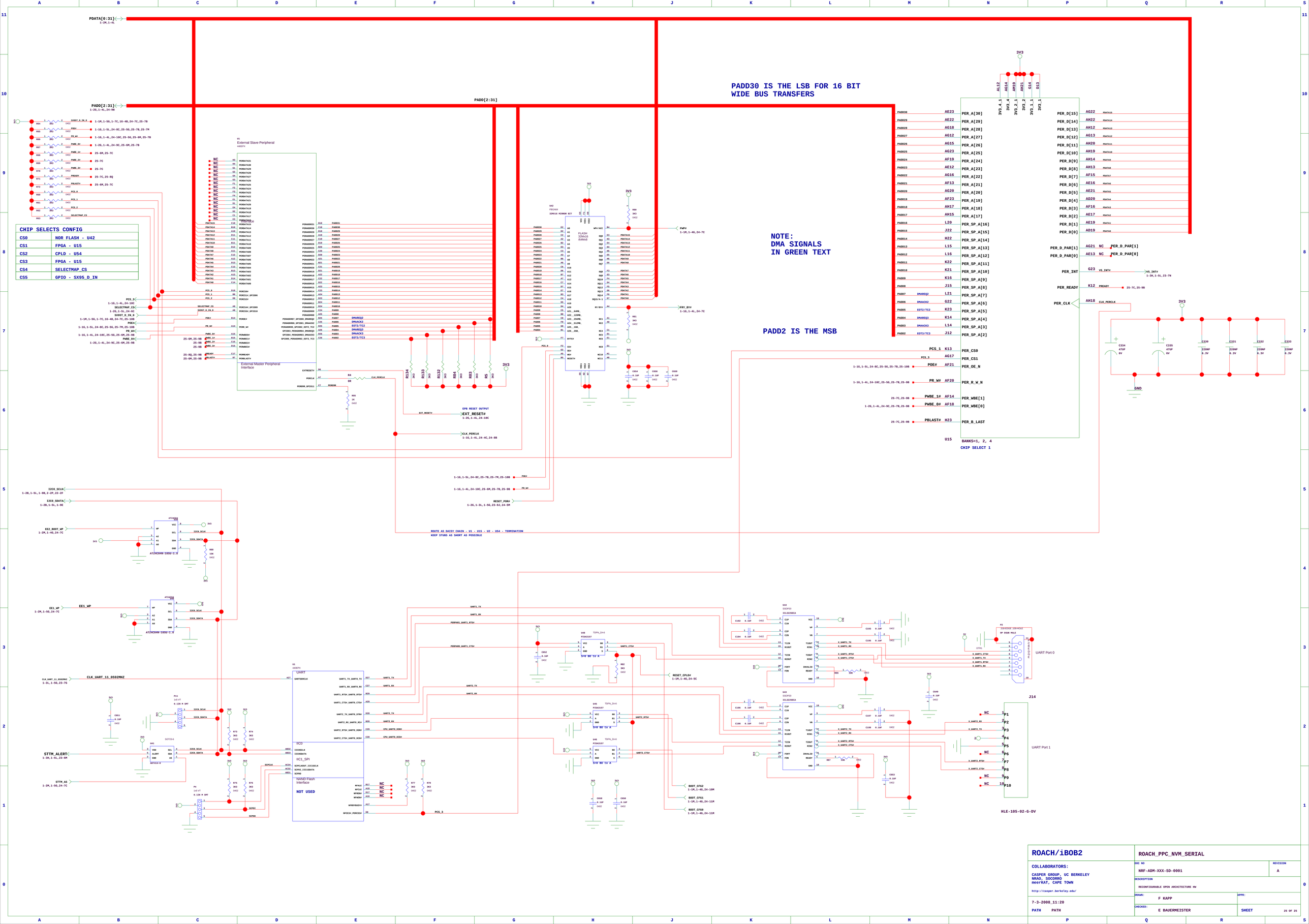
SW3 4POLE Configuration DIP-Switch

CFG_DIP0
CFG_DIP1
CFG_DIP2
MGGEN

R10	10K	0402
R11	10K	0402
R14	10K	0402

BOOT_CFG0 1-1M,1-4G,25-1J
BOOT_CFG1 1-1M,1-4G,25-1J
BOOT_CFG2 1-1M,1-4G,25-1J

	ROACH/iBOB2	ROACH_PPC_CPLD
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN	DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
http://casper.berkeley.edu/	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
7-3-2008_11:20 PATH PATH	DRAWN: F KAPP	APPR:
	CHECKED: E BAUERMEISTER	SHEET 24 OF 25


PADD30 IS THE LSB FOR 16 BIT
WIDE BUS TRANSFERS
NOTE:
DMA SIGNALS
IN GREEN TEXT
PADD2 IS THE MSB
CHIP SELECTS CONFIG
CS0 NOR FLASH - U42
CS1 FPGA - U15
CS2 CPLD - U54
CS3 FPGA - U15
CS4 SELECTMAP_CS
CS5 GPIO - SX95_D_IN
External Slave Peripheral
External Master Peripheral Interface
EPB RESET OUTPUT
EXT_RESET#
CLK_PERCLK
ROUTE AS DAISY CHAIN - U1 - U15 - U2 - U54 - TERMINATION
KEEP STUBS AS SHORT AS POSSIBLE
BANKS=1, 2, 4
CHIP SELECT 1
UART Port 0
UART Port 1
HLE-105-02-G-DV
NOT USED
ROACH/iBOB2
ROACH_PPC_NVM_SERIAL
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
7-3-2008_11:20
PATH PATH
DOC NO
NRF-ADM-XXX-SD-0001
REVISION
A
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:
F KAPP
APPR:
CHECKED:
E BAUERMEISTER
SHEET
25 OF 25