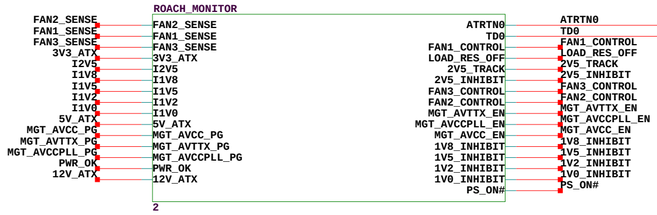
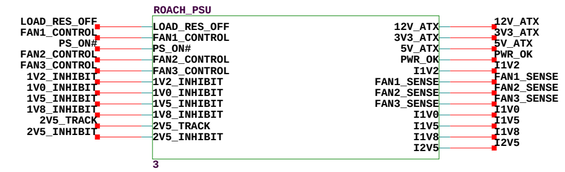
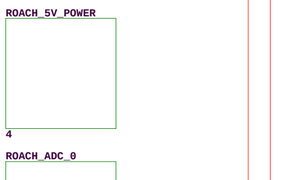

ROACH_MONITOR
FAN2_SENSE
FAN1_SENSE
FAN3_SENSE
3V3_ATX
I2V5
I1V8
I1V5
I1V2
I1V0
5V_ATX
MGT_AVCC_PG
MGT_AVTTX_PG
MGT_AVCCPLL_PG
PWR_OK
12V_ATX
ATRTN0
TD0
FAN1_CONTROL
LOAD_RES_OFF
2V5_TRACK
2V5_INHIBIT
FAN3_CONTROL
FAN2_CONTROL
MGT_AVTTX_EN
MGT_AVCCPLL_EN
MGT_AVCC_EN
1V8_INHIBIT
1V5_INHIBIT
1V2_INHIBIT
1V0_INHIBIT
PS_ON#
2

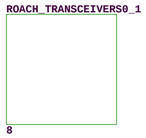

ROACH_PSU
LOAD_RES_OFF
FAN1_CONTROL
PS_ON#
FAN2_CONTROL
FAN3_CONTROL
1V2_INHIBIT
1V0_INHIBIT
1V5_INHIBIT
1V8_INHIBIT
2V5_TRACK
2V5_INHIBIT
12V_ATX
3V3_ATX
5V_ATX
PWR_OK
I1V2
FAN1_SENSE
FAN2_SENSE
FAN3_SENSE
I1V0
I1V5
I1V8
I2V5
3


ROACH_5V_POWER
4


ROACH_ADC_0
5


ROACH_ADC_1
6

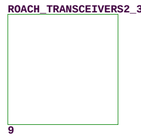

ROACH_V5_CLK
SX95T_DXN
SX95T_DXP
ATRTN0
TD0
7


ROACH_TRANSCEIVERS0_1
8

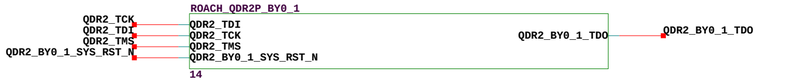

ROACH_DDR2_DIMM
11


ROACH_DIFF_GPIO
12


ROACH_GPIO_MISC
13


ROACH_TRANSCEIVERS2_3
9

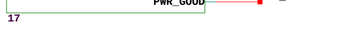

ROACH_TRANSCEIVERS_PSU
MGT_AVCC_EN
MGT_AVCCPLL_EN
MGT_AVTTX_EN
MGT_AVCC_PG
MGT_AVTTX_PG
MGT_AVCCPLL_PG
10


ROACH_QDR2P_BY0_1
QDR2_TCK
QDR2_TDI
QDR2_TMS
QDR2_BY0_1_SYS_RST_N
QDR2_BY0_1_TDO
14


ROACH_QDR2P_BY2_3
QDR2_BY0_1_TDO
QDR2_TMS
QDR2_TCK
QDR2_BY2_3_SYS_RST_N
QDR2_BY2_3_TDO
15


ROACH_CONFIG
SX95T_D_IN_0
SX95T_TCK
SX95T_TMS
SX95T_TDI
SX95T_RDWR_B_0
SX95T_PROGRAM_B_0
SX95T_CS_B_0
SX95T_DONE_0
SX95T_CCLK_0
SX95T_D_OUT_BUSY_0
SX95T_INIT_B_0
SX95T_TDO
16


ROACH_PPC_POWER_1
DDR_VREF_+0.9V
PWR_GOOD
17

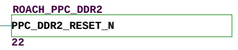

DDR_VREF_+0.9V
PWR_GOOD


ROACH_PPC_POWER_2
PWR_GOOD
18

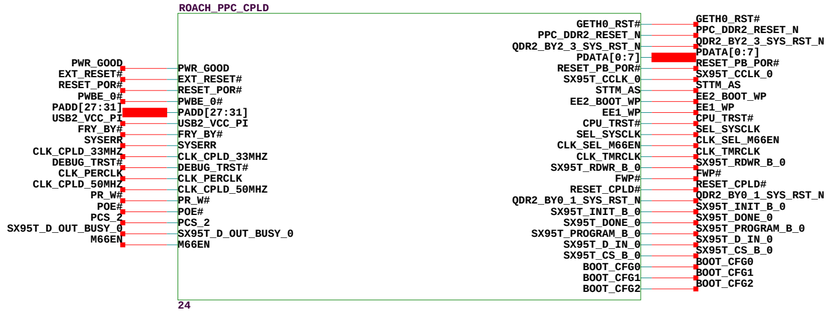

ROACH_PPC_PCI
CLK_PCI1_66/33MHZ
CLK_PCI2_66/33MHZ
M66EN
PCI_INTA#
19

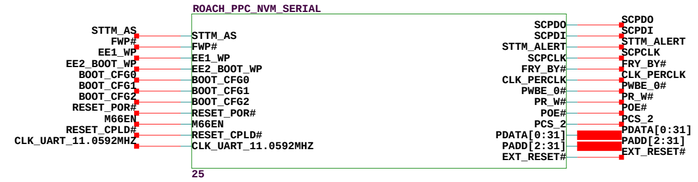

ROACH_PPC_ETH1
GETH0_RST#
CLK_GETH0_25MHZ
GMCMDIO
GMCMDCLK
GETH0_INT#
20

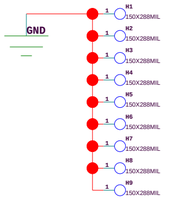

ROACH_PPC_USB
CLK_USB2.0_48MHZ
USB2_VCC_PI
21

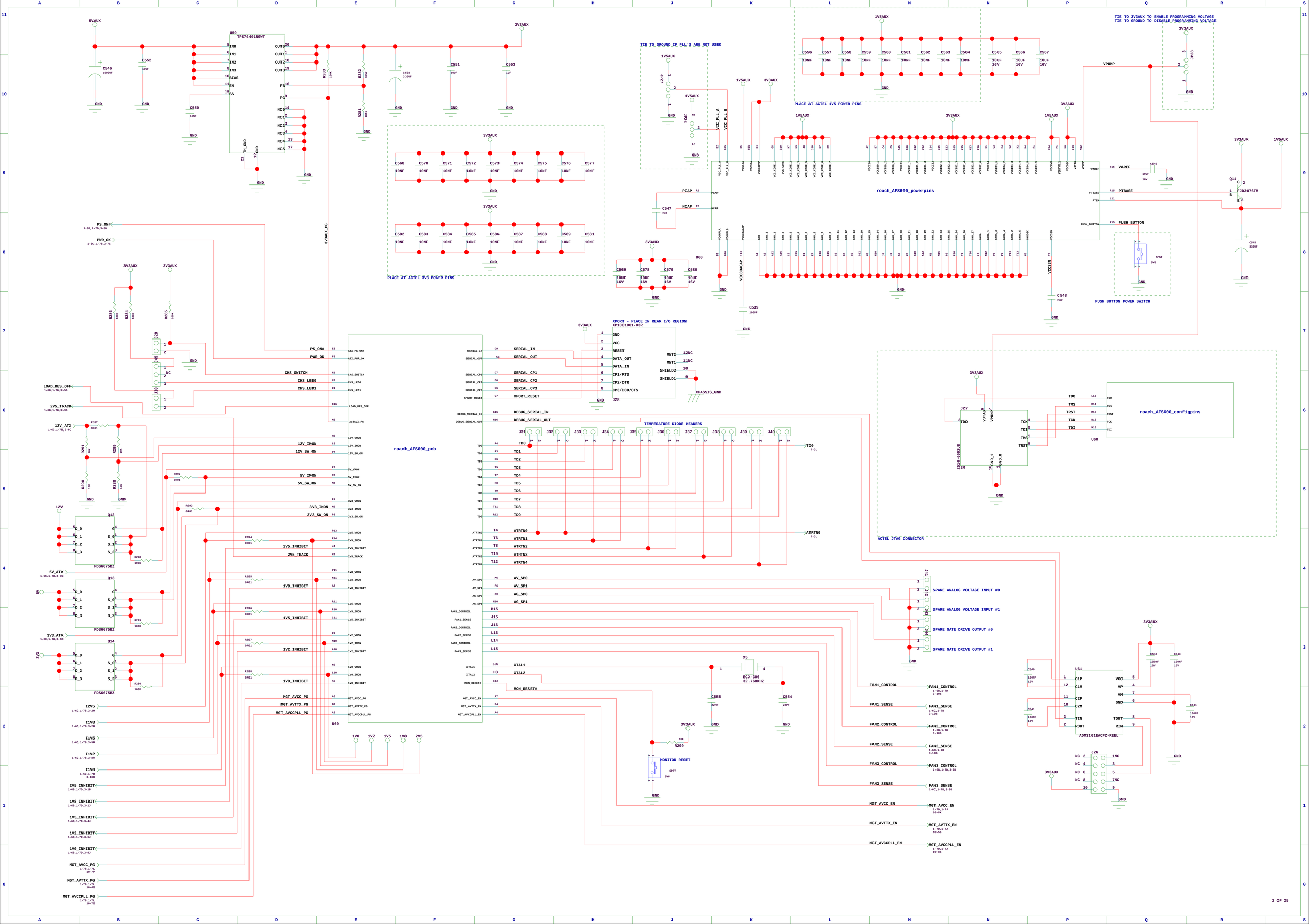

ROACH_PPC_DDR2
PPC_DDR2_RESET_N
22

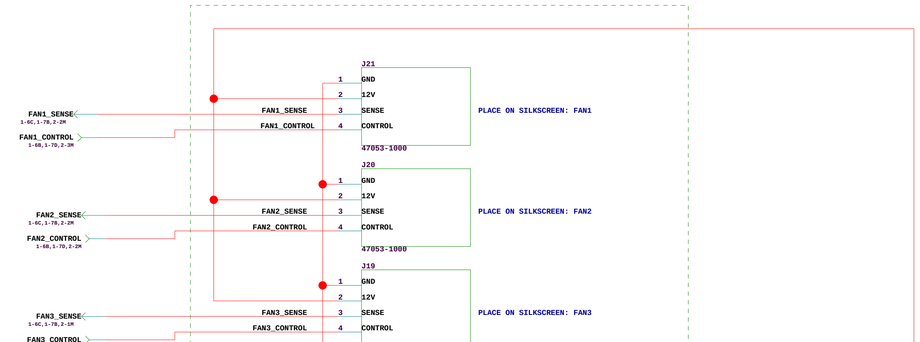
ROACH_PPC_TST_CLK_IO
RESET_PB_POR#
PWR_GOOD
CPU_TRST#
SEL_SYSCLK
GETH0_INT#
GETH1_INT#
PCI_INTA#
STTM_ALERT
SX95T_TDO
CLK_TMRCLK
CLK_SEL_M66EN
GETH0_INT#
GETH1_INT#
PCI_INTA#
STTM_ALERT
SX95T_TDO
RESET_PB_POR#
PWR_GOOD
CPU_TRST#
CLK_SEL_M66EN
SEL_SYSCLK
CLK_TMRCLK
CLK_PCI1_66/33MHZ
GPIO44
SX95T_TDI
SX95T_TCK
SX95T_TMS
RESET_POR#
DEBUG_TRST#
CLK_PCI2_66/33MHZ
CLK_PCI3_66/33MHZ
CLK_GETH0_25MHZ
CLK_USB2.0_48MHZ
CLK_USB2.0_12MHZ
SYSERR
CLK_UART_11.0592MHZ
CLK_CPLD_33MHZ
CLK_GETH1_25MHZ
CLK_UART_11.0592MHZ
CLK_CPLD_33MHZ
GPIO44
CLK_CPLD_50MHZ
CLK_USB2.0_12MHZ
CLK_USB2.0_48MHZ
CLK_GETH1_25MHZ
CLK_GETH0_25MHZ
CLK_PCI3_66/33MHZ
CLK_PCI2_66/33MHZ
CLK_PCI1_66/33MHZ
DEBUG_TRST#
SYSERR
RESET_POR#
SX95T_TDI
SX95T_TCK
SX95T_TMS
23

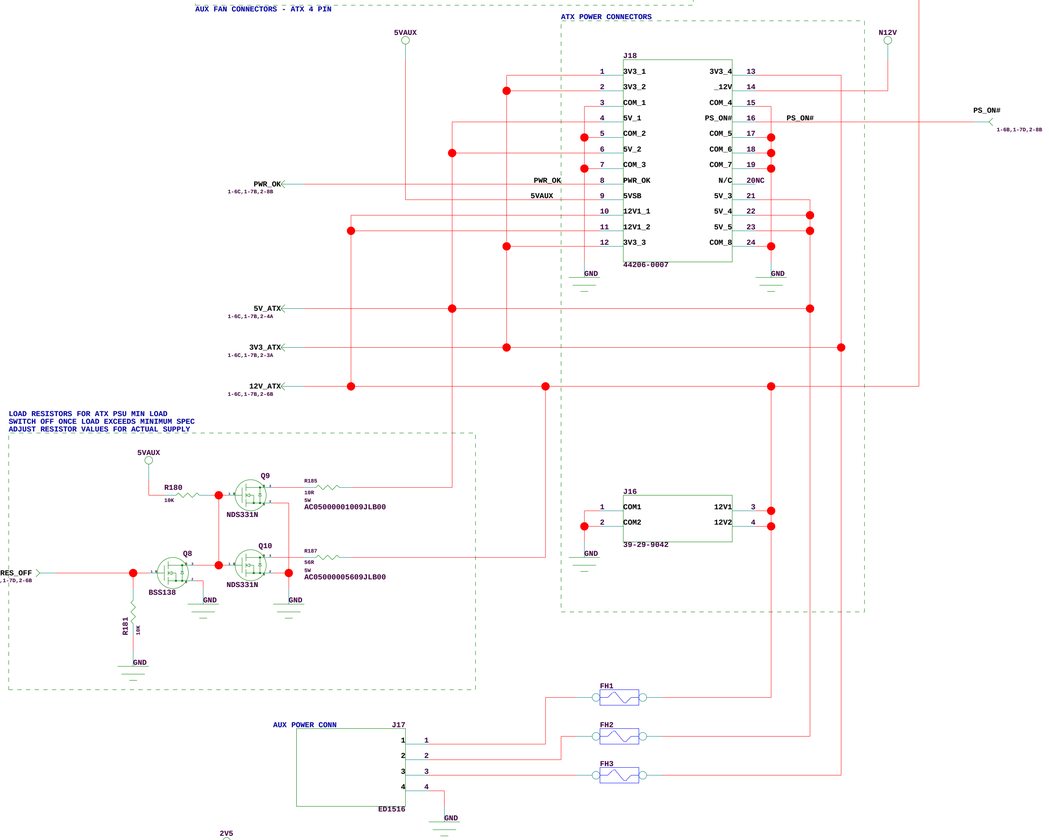

ROACH_PPC_CPLD
PWR_GOOD
EXT_RESET#
RESET_POR#
PWBE_0#
PADD[27:31]
USB2_VCC_PI
FRY_BY#
SYSERR
CLK_CPLD_33MHZ
DEBUG_TRST#
CLK_PERCLK
CLK_CPLD_50MHZ
PR_W#
POE#
PCS_2
SX95T_D_OUT_BUSY_0
M66EN
GETH0_RST#
PPC_DDR2_RESET_N
QDR2_BY2_3_SYS_RST_N
PDATA[0:7]
RESET_PB_POR#
SX95T_CCLK_0
STTM_AS
EE2_BOOT_WP
EE1_WP
CPU_TRST#
SEL_SYSCLK
CLK_SEL_M66EN
CLK_TMRCLK
SX95T_RDWR_B_0
FWP#
RESET_CPLD#
QDR2_BY0_1_SYS_RST_N
SX95T_INIT_B_0
SX95T_DONE_0
SX95T_PROGRAM_B_0
SX95T_D_IN_0
SX95T_CS_B_0
BOOT_CFG0
BOOT_CFG1
BOOT_CFG2
24

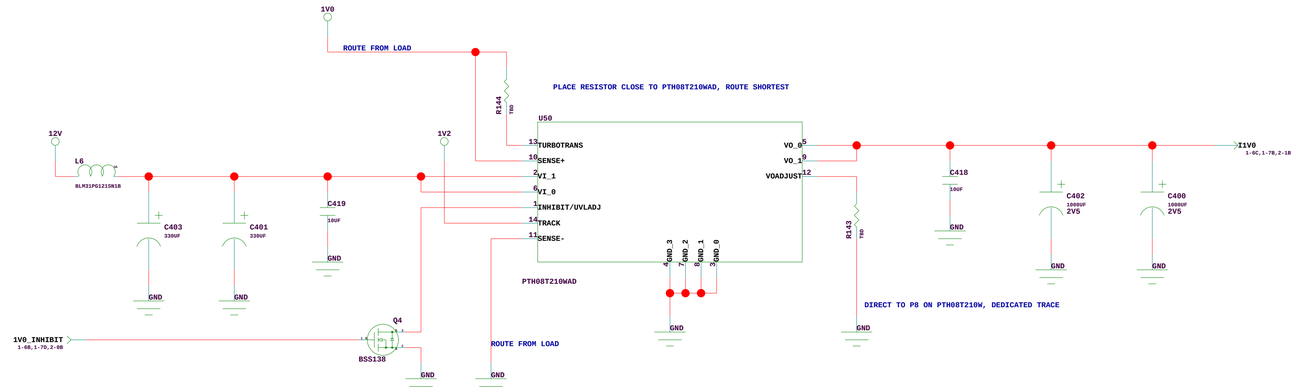

ROACH_PPC_NVM_SERIAL
STTM_AS
FWP#
EE1_WP
EE2_BOOT_WP
BOOT_CFG0
BOOT_CFG1
BOOT_CFG2
RESET_POR#
M66EN
RESET_CPLD#
CLK_UART_11.0592MHZ
SCPDO
SCPDI
STTM_ALERT
SCPCLK
FRY_BY#
CLK_PERCLK
PWBE_0#
PR_W#
POE#
PCS_2
PDATA[0:31]
PADD[2:31]
EXT_RESET#
25

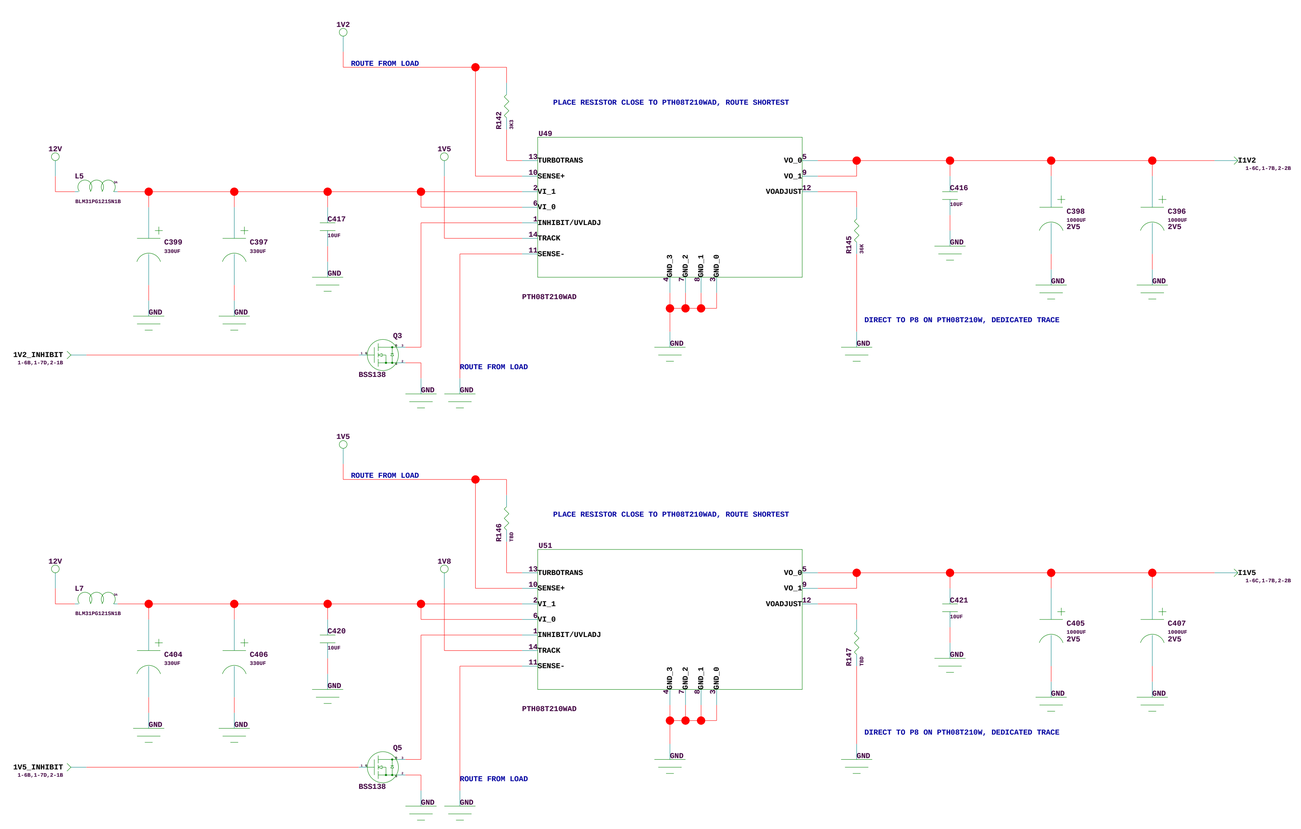

GND
H1
H2
H3
H4
H5
H6
H7
H8
H9
150X288MIL


U59
TPS74401RGWT
5VAUX
3V3AUX
C546 1000UF
C552 10NF
C550 15NF
C538 330UF
C551 10UF
C553 1UF
R283 100K
R282 2K37
R281 1K15
TH_GND
3V3AUX_PG
TIE TO GROUND IF PLL'S ARE NOT USED
JP27
JP26
PLACE AT ACTEL 3V3 POWER PINS
C568 C570 C571 C572 C573 C574 C575 C576 C577 C582 C583 C584 C585 C586 C587 C588 C589 C581 10NF
PLACE AT ACTEL 1V5 POWER PINS
C556 C557 C558 C559 C560 C561 C562 C563 C564 10NF
C565 C566 C567 10UF 16V
TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE
JP28
VPUMP
roach_AFS600_powerpins
VCC_PLL_A
VCC_PLL_B
PCAP
NCAP
C547 2U2
U60
C569 C578 C579 C580 10UF 16V
C539 100PF
VCC33AUXP
VCC33N
C548 2U2
VAREF
C549 10UF 16V
PTBASE
PTEM
Q11 FJD3076TM
C545 330UF
PUSH_BUTTON
SW5 SPST
PUSH BUTTON POWER SWITCH
PS_ON# 1-6B,1-7D,3-8G
PWR_OK 1-6C,1-7B,3-7C
R286 100R
R284 100R
R285 100K
J29
J45
J30
LOAD_RES_OFF 1-6B,1-7D,3-5B
2V5_TRACK 1-6B,1-7D,3-3B
CHS_SWITCH
CHS_LED0
CHS_LED1
LOAD_RES_OFF
3V3AUX_PG
12V_ATX 1-6C,1-7B,3-6C
R287 0R01
R291 10K
R289 10K
R290 10K
R288 10K
12V_IMON
12V_SW_ON
12V_VMON
12V_IMON
12V_SW_ON
R292 0R01
5V_IMON
5V_SW_ON
5V_VMON
5V_IMON
5V_SW_ON
R293 0R01
3V3_IMON
3V3_SW_ON
3V3_VMON
3V3_IMON
3V3_SW_ON
R294 0R01
2V5_INHIBIT
2V5_TRACK
2V5_VMON
2V5_IMON
2V5_INHIBIT
2V5_TRACK
R295 0R01
1V8_INHIBIT
1V8_VMON
1V8_IMON
1V8_INHIBIT
R296 0R01
1V5_INHIBIT
1V5_VMON
1V5_IMON
1V5_INHIBIT
R297 0R01
1V2_INHIBIT
1V2_VMON
1V2_IMON
1V2_INHIBIT
R298 0R01
1V0_INHIBIT
1V0_VMON
1V0_IMON
1V0_INHIBIT
MGT_AVCC_PG
MGT_AVTTX_PG
MGT_AVCCPLL_PG
Q12 FDS6675BZ
Q13 FDS6675BZ
Q14 FDS6675BZ
R278 100K
R279 100K
R280 100K
I2V5 1-6C,1-7B,3-2H
I1V8 1-6C,1-7B,3-2B
I1V5 1-6C,1-7B,3-5B
I1V2 1-6C,1-7B,3-6B
I1V0 1-6C,1-7B 3-10B
2V5_INHIBIT 1-6B,1-7D,3-1B
1V8_INHIBIT 1-6B,1-7D,3-1J
1V5_INHIBIT 1-6B,1-7D,3-4J
1V2_INHIBIT 1-6B,1-7D,3-6J
1V0_INHIBIT 1-6B,1-7D,3-9J
MGT_AVCC_PG 1-7B,1-7L 10-7P
MGT_AVTTX_PG 1-7B,1-7L 10-4G
MGT_AVCCPLL_PG 1-7B,1-7L 10-7G
roach_AFS600_pcb
XPORT - PLACE IN REAR I/O REGION
XP1001001-03R
J28
SERIAL_IN
SERIAL_OUT
SERIAL_CP1
SERIAL_CP2
SERIAL_CP3
XPORT_RESET
MNT2
MNT1
SHIELD2
SHIELD1
CHASSIS_GND
DEBUG_SERIAL_IN
DEBUG_SERIAL_OUT
TEMPERATURE DIODE HEADERS
J31 J32 J33 J34 J35 J36 J37 J38 J39 J40
TD0 TD1 TD2 TD3 TD4 TD5 TD6 TD7 TD8 TD9
ATRTN0 ATRTN1 ATRTN2 ATRTN3 ATRTN4
AV_SP0 AV_SP1 AG_SP0 AG_SP1
FAN1_CONTROL
FAN1_SENSE
FAN2_CONTROL
FAN2_SENSE
FAN3_CONTROL
FAN3_SENSE
XTAL1
XTAL2
MON_RESET#
X5 ECX-306 32.768KHZ
C555 C554 22PF
R299 10K
MONITOR RESET SW6 SPST
MGT_AVCC_EN
MGT_AVTTX_EN
MGT_AVCCPLL_EN
J41
SPARE ANALOG VOLTAGE INPUT #0
SPARE ANALOG VOLTAGE INPUT #1
SPARE GATE DRIVE OUTPUT #0
SPARE GATE DRIVE OUTPUT #1
ACTEL JTAG CONNECTOR
J27
TDO TMS TRST TCK TDI
Z510-6002UB
roach_AFS600_configpins
U61 ADM3101EACPZ-REEL
C540 C541 C542 C543 C544 100NF 10V
J26
2 OF 25

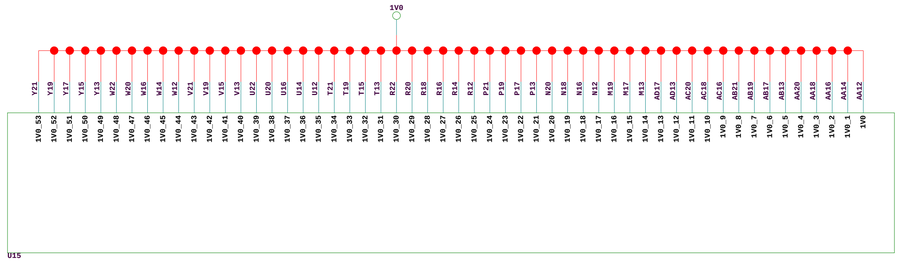


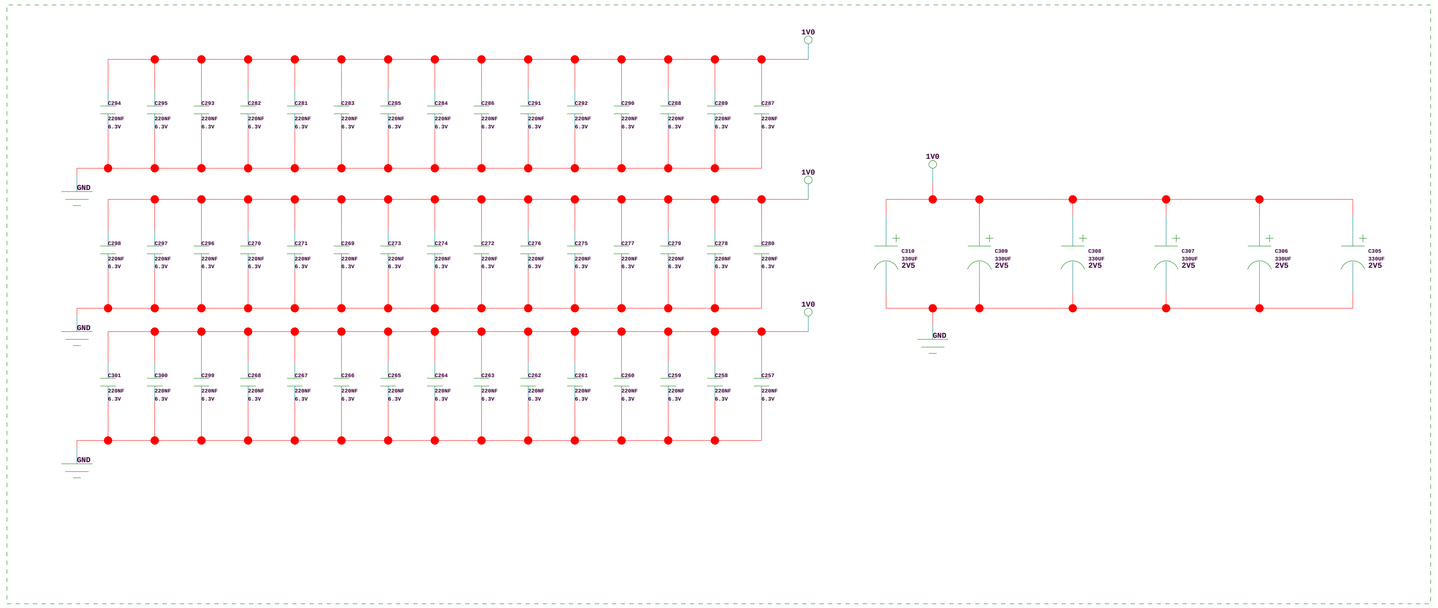




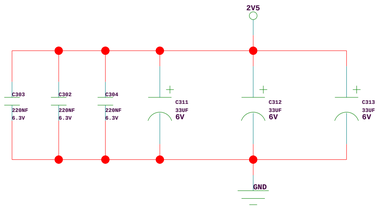


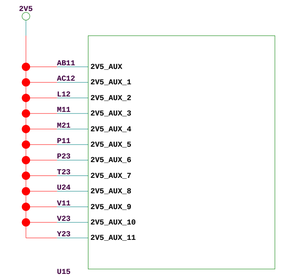
SOURCE VOLTAGES TO BE SELECTED

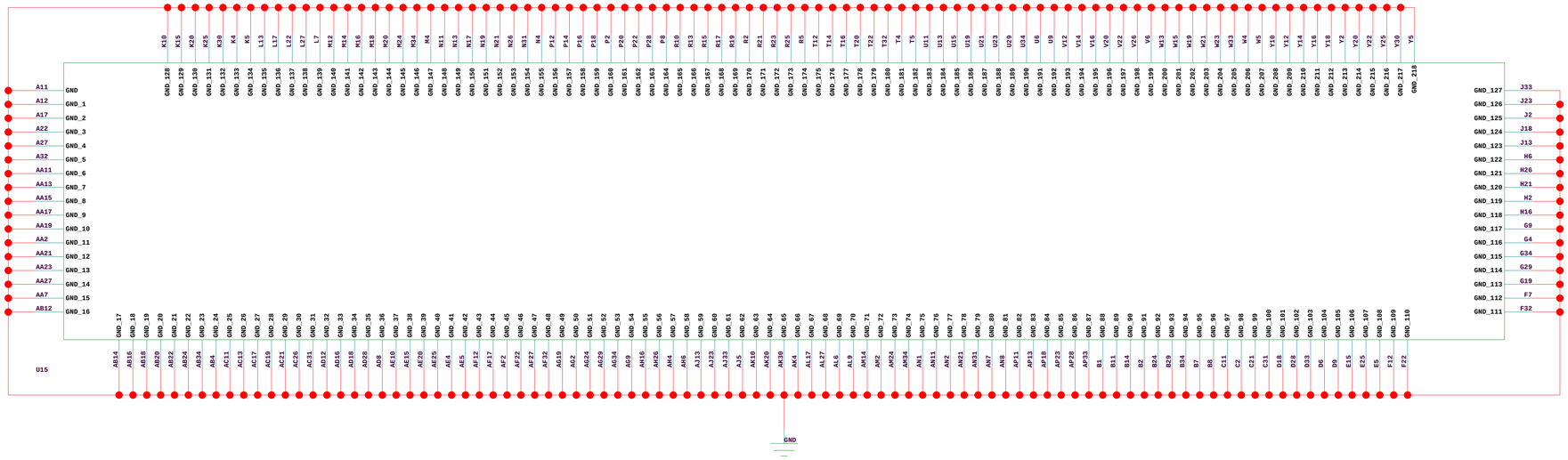

1V0
V21 Y19 Y17 Y15 Y13 W22 W20 W16 W14 W12 V21 V19 V15 V13 U22 U20 U16 U14 U12 T21 T19 T15 T13 R22 R20 R18 R16 R14 R12 P21 P19 P17 P13 N20 N18 N16 N12 M19 M17 M13 AD17 AD13 AC20 AC18 AC16 AB21 AB19 AB17 AB13 AA20 AA18 AA16 AA14 AA12
1V0_53 1V0_52 1V0_51 1V0_50 1V0_49 1V0_48 1V0_47 1V0_46 1V0_45 1V0_44 1V0_43 1V0_42 1V0_41 1V0_40 1V0_39 1V0_38 1V0_37 1V0_36 1V0_35 1V0_34 1V0_33 1V0_32 1V0_31 1V0_30 1V0_29 1V0_28 1V0_27 1V0_26 1V0_25 1V0_24 1V0_23 1V0_22 1V0_21 1V0_20 1V0_19 1V0_18 1V0_17 1V0_16 1V0_15 1V0_14 1V0_13 1V0_12 1V0_11 1V0_10 1V0_9 1V0_8 1V0_7 1V0_6 1V0_5 1V0_4 1V0_3 1V0_2 1V0_1 1V0
U15


1V0
C294 C295 C293 C282 C281 C283 C285 C284 C286 C291 C292 C290 C288 C289 C287
C298 C297 C296 C270 C271 C269 C273 C274 C272 C276 C275 C277 C279 C278 C280
C301 C300 C299 C260 C267 C266 C265 C264 C263 C262 C261 C268 C259 C258 C257
220NF 6.3V
GND

1V0
C310 C309 C308 C307 C306 C305
330UF 2V5
GND


2V5
C303 C302 C304 C311 C312 C313
220NF 6.3V
33UF 6V
GND


2V5
AB11 AC12 L12 M11 M21 P11 P23 T23 U24 V11 V23 Y23
2V5_AUX 2V5_AUX_1 2V5_AUX_2 2V5_AUX_3 2V5_AUX_4 2V5_AUX_5 2V5_AUX_6 2V5_AUX_7 2V5_AUX_8 2V5_AUX_9 2V5_AUX_10 2V5_AUX_11
U15


K10 K15 K20 K25 K30 K4 K5 L13 L17 L22 L27 L7 M12 M14 M16 M18 M20 M24 M24 M4 N11 N13 N17 N19 N21 N26 N31 N4 P12 P14 P16 P18 P2 P20 P22 P28 P8 R10 R13 R15 R17 R19 R2 R21 R23 R25 R5 T12 T14 T16 T20 T22 T32 T4 T5 U11 U13 U15 U19 U21 U23 U29 U34 U6 U9 V12 V14 V16 V20 V22 V26 V6 W13 W15 W19 W21 W23 W3 W4 W5 Y10 Y12 Y14 Y16 Y18 Y2 Y20 Y22 Y25 Y30 Y5
GND_128 GND_129 GND_130 GND_131 GND_132 GND_133 GND_134 GND_135 GND_136 GND_137 GND_138 GND_139 GND_140 GND_141 GND_142 GND_143 GND_144 GND_145 GND_146 GND_147 GND_148 GND_149 GND_150 GND_151 GND_152 GND_153 GND_154 GND_155 GND_156 GND_157 GND_158 GND_159 GND_160 GND_161 GND_162 GND_163 GND_164 GND_165 GND_166 GND_167 GND_168 GND_169 GND_170 GND_171 GND_172 GND_173 GND_174 GND_175 GND_176 GND_177 GND_178 GND_179 GND_180 GND_181 GND_182 GND_183 GND_184 GND_185 GND_186 GND_187 GND_188 GND_189 GND_190 GND_191 GND_192 GND_193 GND_194 GND_195 GND_196 GND_197 GND_198 GND_199 GND_200 GND_201 GND_202 GND_203 GND_204 GND_205 GND_206 GND_207 GND_208 GND_209 GND_210 GND_211 GND_212 GND_213 GND_214 GND_215 GND_216 GND_217 GND_218
A11 A12 A17 A22 A27 A32 AA11 AA13 AA15 AA17 AA19 AA2 AA21 AA23 AA27 AA7 AB12
GND GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16
GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_25 GND_26 GND_27 GND_28 GND_29 GND_30 GND_31 GND_32 GND_33 GND_34 GND_35 GND_36 GND_37 GND_38 GND_39 GND_40 GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67 GND_68 GND_69 GND_70 GND_71 GND_72 GND_73 GND_74 GND_75 GND_76 GND_77 GND_78 GND_79 GND_80 GND_81 GND_82 GND_83 GND_84 GND_85 GND_86 GND_87 GND_88 GND_89 GND_90 GND_91 GND_92 GND_93 GND_94 GND_95 GND_96 GND_97 GND_98 GND_99 GND_100 GND_101 GND_102 GND_103 GND_104 GND_105 GND_106 GND_107 GND_108 GND_109 GND_110
AB14 AB16 AB18 AB20 AB22 AB24 AB34 AB4 AC11 AC13 AC17 AC19 AC21 AC26 AC31 AD12 AD16 AD18 AD28 AD8 AE10 AE15 AE20 AE25 AE4 AE5 AF12 AF17 AF2 AF22 AF27 AF32 AG19 AG2 AG24 AG29 AG34 AG9 AH16 AH26 AH4 AH6 AJ13 AJ23 AJ33 AJ5 AK10 AK20 AK30 AK4 AL17 AL27 AL6 AL9 AM14 AM2 AM24 AM34 AN1 AN11 AN2 AN21 AN7 AN8 AP11 AP13 AP18 AP23 AP28 AP33 B1 B11 B14 B2 B24 B29 B34 B7 B8 C11 C2 C21 C31 D18 D28 D3 D6 D9 E15 E25 E5 F12 F22
U15
GND
GND_127 GND_126 GND_125 GND_124 GND_123 GND_122 GND_121 GND_120 GND_119 GND_118 GND_117 GND_116 GND_115 GND_114 GND_113 GND_112 GND_111
J33 J23 J2 J18 J13 H6 H26 H21 H2 H16 G9 G4 G34 G29 G19 F7 F32


ZDOK0_CLK0_P K18
ZDOK0_CLK0_N J19
ZDOK0_CLK1_P J16
ZDOK0_CLK1_N J17
2V5
R133 100R
R132 100R
VRP_20 L11
VRN_20 L10
R134 100R
R135 100R
VRP_12_GPIOLVC25 P9
VRN_12_GPIOLVC25 R9
M9 2V5_12
N6 2V5_12_1
T7 2V5_12_2
E10 2V5_20
H11 2V5_20_1
J8 2V5_20_2
C328 47UF 6V
C327 47UF 6V
C326 47UF 6V
C329 47UF 6V
C325 220NF 6.3V
C322 220NF 6.3V
C323 220NF 6.3V
C324 220NF 6.3V
U15
BANKS=20, 12
5V0
3V3
1V8
C315 1UF 16V
C314 100NF 10V
C317 1UF 16V
C316 100NF 10V
C318 1UF 16V
C319 100NF 10V
C321 1UF 16V
C320 100NF 10V
P5
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ZDOK40
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ZDOK1_CLK0_P L19
ZDOK1_CLK0_N K19
ZDOK1_CLK1_P H14
ZDOK1_CLK1_N H15
2V5
R137 100R
R136 100R
VRP_18 AG6
VRN_18 AH5
R138 100R
R139 100R
VRP_22_GPIOLVC25 AE9
VRN_22_GPIOLVC25 AF8
AB9 2V5_18
AC6 2V5_18_1
W8 2V5_18_2
AF7 2V5_22
AH11 2V5_22_1
AJ8 2V5_22_2
C348 47UF 6V
C349 47UF 6V
C350 47UF 6V
C351 47UF 6V
C344 220NF 6.3V
C345 220NF 6.3V
C346 220NF 6.3V
C347 220NF 6.3V
ZDOK1_DP_P[37] AG10
ZDOK1_DP_N[37] AG11
ZDOK1_DP_P[36] AG8
ZDOK1_DP_N[36] AH8
ZDOK1_DP_P[35] AH9
ZDOK1_DP_N[35] AH10
ZDOK1_DP_P[34] AF11
ZDOK1_DP_N[34] AE11
ZDOK1_DP_P[33] AJ9
ZDOK1_DP_N[33] AJ10
ZDOK1_DP_P[32] AF9
ZDOK1_DP_N[32] AF10
ZDOK1_DP_P[31] AK8
ZDOK1_DP_N[31] AK9
ZDOK1_DP_P[30] AK11
ZDOK1_DP_N[30] AJ11
ZDOK1_DP_P[29] AD10
ZDOK1_DP_N[29] AD11
ZDOK1_DP_P[28] AE8
ZDOK1_DP_N[28] AD9
ZDOK1_DP_P[27] AL11
ZDOK1_DP_N[27] AL10
ZDOK1_DP_P[26] AC10
ZDOK1_DP_N[26] AC9
ZDOK1_DP_P[25] AM12
ZDOK1_DP_N[25] AM11
ZDOK1_DP_P[24] AC8
ZDOK1_DP_N[24] AB8
ZDOK1_DP_P[23] AP12
ZDOK1_DP_N[23] AN12
ZDOK1_DP_P[22] AA8
ZDOK1_DP_N[22] AA9
ZDOK1_DP_P[21] AN13
ZDOK1_DP_N[21] AM13
ZDOK1_DP_P[20] AB10
ZDOK1_DP_N[20] AA10
ZDOK1_DP_P[19] AN14
ZDOK1_DP_N[19] AP14
ZDOK1_DP_P[18] V10
ZDOK1_DP_N[18] V9
ZDOK1_DP_P[17] AK7
ZDOK1_DP_N[17] AK6
ZDOK1_DP_P[16] V8
ZDOK1_DP_N[16] U8
ZDOK1_DP_P[15] AJ7
ZDOK1_DP_N[15] AJ6
ZDOK1_DP_P[14] W10
ZDOK1_DP_N[14] W9
ZDOK1_DP_P[13] AH7
ZDOK1_DP_N[13] AG7
ZDOK1_DP_P[12] Y11
ZDOK1_DP_N[12] W11
ZDOK1_DP_P[11] W7
ZDOK1_DP_N[11] V7
ZDOK1_DP_P[10] AG5
ZDOK1_DP_N[10] AF5
ZDOK1_DP_P[9] AE7
ZDOK1_DP_N[9] AF6
ZDOK1_DP_P[8] W6
ZDOK1_DP_N[8] Y6
ZDOK1_DP_P[7] AD6
ZDOK1_DP_N[7] AE6
ZDOK1_DP_P[6] AA6
ZDOK1_DP_N[6] Y7
ZDOK1_DP_P[5] AD4
ZDOK1_DP_N[5] AD5
ZDOK1_DP_P[4] Y8
ZDOK1_DP_N[4] Y9
ZDOK1_DP_P[3] AC7
ZDOK1_DP_N[3] AD7
ZDOK1_DP_P[2] AA5
ZDOK1_DP_N[2] AB5
ZDOK1_DP_P[1] AB6
ZDOK1_DP_N[1] AB7
ZDOK1_DP_P[0] AC4
ZDOK1_DP_N[0] AC5
U15
BANKS=18, 22
5V0
3V3
2V5
1V8
C337 1UF 16V
C336 100NF 10V
C339 1UF 16V
C338 100NF 10V
C340 1UF 16V
C341 100NF 10V
C343 1UF 16V
C342 100NF 10V
P7
W1 X1 Y1 Z1 W2 X2 Y2 Z2 W3 X3 Y3 Z3 W4 X4 Y4 Z4 W5 X5 Y5 Z5 W6 X6 Y6 Z6
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20
6367550-5
ZDOK49
ZDOK1_DP_P[0] ZDOK1_DP_N[0] ZDOK1_DP_P[1] ZDOK1_DP_N[1] ZDOK1_DP_P[2] ZDOK1_DP_N[2] ZDOK1_DP_P[3] ZDOK1_DP_N[3] ZDOK1_DP_P[4] ZDOK1_DP_N[4] ZDOK1_DP_P[5] ZDOK1_DP_N[5] ZDOK1_DP_P[6] ZDOK1_DP_N[6] ZDOK1_DP_P[7] ZDOK1_DP_N[7] ZDOK1_DP_P[8] ZDOK1_DP_N[8] ZDOK1_DP_P[9] ZDOK1_DP_N[9] ZDOK1_DP_P[10] ZDOK1_DP_N[10] ZDOK1_DP_P[11] ZDOK1_DP_N[11] ZDOK1_DP_P[12] ZDOK1_DP_N[12] ZDOK1_DP_P[13] ZDOK1_DP_N[13] ZDOK1_DP_P[14] ZDOK1_DP_N[14] ZDOK1_DP_P[15] ZDOK1_DP_N[15] ZDOK1_DP_P[16] ZDOK1_DP_N[16] ZDOK1_DP_P[17] ZDOK1_DP_N[17] ZDOK1_DP_P[18] ZDOK1_DP_N[18] ZDOK1_DP_P[19] ZDOK1_DP_N[19]
P7
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15 F16 F17 F18 F19 F20
ZDOK1_DP_P[20] ZDOK1_DP_N[20] ZDOK1_DP_P[21] ZDOK1_DP_N[21] ZDOK1_DP_P[22] ZDOK1_DP_N[22] ZDOK1_DP_P[23] ZDOK1_DP_N[23] ZDOK1_DP_P[24] ZDOK1_DP_N[24] ZDOK1_DP_P[25] ZDOK1_DP_N[25] ZDOK1_DP_P[26] ZDOK1_DP_N[26] ZDOK1_DP_P[27] ZDOK1_DP_N[27] ZDOK1_DP_P[28] ZDOK1_DP_N[28] ZDOK1_CLK0_P ZDOK1_CLK0_N ZDOK1_DP_P[29] ZDOK1_DP_N[29] ZDOK1_DP_P[30] ZDOK1_DP_N[30] ZDOK1_DP_P[31] ZDOK1_DP_N[31] ZDOK1_DP_P[32] ZDOK1_DP_N[32] ZDOK1_DP_P[33] ZDOK1_DP_N[33] ZDOK1_DP_P[34] ZDOK1_DP_N[34] ZDOK1_DP_P[35] ZDOK1_DP_N[35] ZDOK1_DP_P[36] ZDOK1_DP_N[36] ZDOK1_DP_P[37] ZDOK1_DP_N[37] ZDOK1_CLK1_P ZDOK1_CLK1_N
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2V5
R109 10K
X2
OE
VCC
OUT
OUT#
GND
CCLD-023-25-100.000
100.00MHZ
C161 220NF 6.3V
PLACE AT FPGA
R112 100R
SYS_CLK_P H17
SYS_CLK_N H18
DLY_CLK_200_P K17
DLY_CLK_200_N L18
GPIO_CLK0_P H19
GPIO_CLK0_N H20
GPIO_CLK1_P G15
GPIO_CLK1_N G16
U15
BANKS=3
2V5_3_1 E20
2V5_3 D23
C164 47UF 6V
C160 220NF 6.3V
R110 10K
X3
CCLD-024-25-200.000
200.00MHZ
C162 220NF 6.3V
R111 100R
5V
U25
ADR03AUJ-R2
NC1
TP1
VIN
TEMP
GND
TP2
NIC
VOUT
TRIM
8NC
7NC
6
5
C158 220NF 6.3V
C159 220NF 6.3V
PLACE CLOSE TO CONNECTOR
PLACE CLOSE TO FPGA PINS
J12
TBD
C155 10PF
C153 10NF
U27
IN
IN#
VT
VREF_AC
SY58604U
Q
Q#
VCC
R101 49R9 NOSTUFF
R102 49R9 NOSTUFF
C163 220NF 6.3V
R116 249R
R113 249R
R115 62R5
R114 62R5
GPIO_CLK0_P
GPIO_CLK0_N
J13
C156 10PF
C154 10NF
U26
R104 49R9 NOSTUFF
R103 49R9 NOSTUFF
C157 220NF 6.3V
R108 249R
R107 249R
R105 62R5
R106 62R5
GPIO_CLK1_P
GPIO_CLK1_N
SX95T_AVDD T18
SX95T_AVSS T17
U18 SX95T_VP_0
V17 SX95T_VN_0
V18 SX95T_VREF_P
U17 SX95T_VREF_N
U15
FB27 220@100M
SX95T_DXP W18
SX95T_DXN W17
SX95T_DXP 2-6L
SX95T_DXN 2-4L

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB2 220@100M
FB3 220@100M
FB4 220@100M
C95 C94 C93 C92 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_112 R3 MGTAVCC_112
MGTAVCC_112_1 R4 MGTAVCC_112_1
MGTAVCCPLL_112 T3 MGTAVCCPLL_112
MGTAVTTRX_112 N3 MGTAVTTRX_112
MGT_112_REF_CLK_P P4 MGT_112_REF_CLK_P
MGT_112_REF_CLK_N P3 MGT_112_REF_CLK_N
MGTRX0_112_P N1 MGTRX0_112_P
MGTRX0_112_N P1 MGTRX0_112_N
MGTRX1_112_P T1 MGTRX1_112_P
MGTRX1_112_N R1 MGTRX1_112_N
U15
MGTRREF V4 MGTRREF
MGT_VTRXC V5 MGTAVTTRXC
MGTAVTTTX_112 M3 MGTAVTTTX_112
MGTAVTTTX_112_1 U3 MGTAVTTTX_112_1
MGTTX0_112_P M2 MGTTX0_112_P
MGTTX0_112_N N2 MGTTX0_112_N
MGTTX1_112_P U2 MGTTX1_112_P
MGTTX1_112_N T2 MGTTX1_112_N
R56 49.9R
MGT_AVTT
FB25 220@100M
FB5 220@100M
FB6 220@100M
C126 C97 C96 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
2V5
FB26 220@100M
C137 220NF 6.3V
R64 10K
X1
CCLD-023-25-156.250
156.25MHZ
JP6
OE
VCC
OUT
GND
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
C104 C105 C106 C107 C108 C109 10NF 25V
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB11 220@100M
FB12 220@100M
FB9 220@100M
FB10 220@100M
C103 C102 C101 C100 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_114 AA3 MGTAVCC_114
MGTAVCC_114_1 AA4 MGTAVCC_114_1
MGTAVCCPLL_114 AB3 MGTAVCCPLL_114
MGTAVTTRX_114 W3 MGTAVTTRX_114
MGT_114_REF_CLK_P NC Y4 MGT_114_REF_CLK_P
MGT_114_REF_CLK_N NC Y3 MGT_114_REF_CLK_N
MGTRX0_114_P W1 MGTRX0_114_P
MGTRX0_114_N Y1 MGTRX0_114_N
MGTRX1_114_P AB1 MGTRX1_114_P
MGTRX1_114_N AA1 MGTRX1_114_N
U15
C140 C141 C142 C143 10NF 25V
MGTAVTTTX_114 AC3 MGTAVTTTX_114
MGTAVTTTX_114_1 V3 MGTAVTTTX_114_1
MGTTX0_114_P V2 MGTTX0_114_P
MGTTX0_114_N W2 MGTTX0_114_N
MGTTX1_114_P AC2 MGTTX1_114_P
MGTTX1_114_N AB2 MGTTX1_114_N
MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT
MGT_AVTT
FB8 220@100M
FB7 220@100M
C98 C99 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB17 220@100M
FB18 220@100M
FB15 220@100M
FB16 220@100M
C120 C119 C118 C115 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_116 J3 MGTAVCC_116
MGTAVCC_116_1 J4 MGTAVCC_116_1
MGTAVCCPLL_116 K3 MGTAVCCPLL_116
MGTAVTTRX_116 G3 MGTAVTTRX_116
MGT_116_REF_CLK_P NC H4 MGT_116_REF_CLK_P
MGT_116_REF_CLK_N NC H3 MGT_116_REF_CLK_N
MGTRX0_116_P G1 MGTRX0_116_P
MGTRX0_116_N H1 MGTRX0_116_N
MGTRX1_116_P K1 MGTRX1_116_P
MGTRX1_116_N J1 MGTRX1_116_N
U15
C110 C111 C112 C113 10NF 25V
MGTAVTTTX_116_1 L3 MGTAVTTTX_116_1
MGTAVTTTX_116 F3 MGTAVTTTX_116
MGTTX0_116_P F2 MGTTX0_116_P
MGTTX0_116_N G2 MGTTX0_116_N
MGTTX1_116_P L2 MGTTX1_116_P
MGTTX1_116_N K2 MGTTX1_116_N
MGT_AVTT
FB14 220@100M
FB13 220@100M
C116 C117 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB22 220@100M
FB21 220@100M
FB24 220@100M
FB23 220@100M
C123 C124 C114 C125 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_118 AG3 MGTAVCC_118
MGTAVCC_118_1 AG4 MGTAVCC_118_1
MGTAVCCPLL_118 AH3 MGTAVCCPLL_118
MGTAVTTRX_118 AE3 MGTAVTTRX_118
MGT_118_REF_CLK_P NC AF4 MGT_118_REF_CLK_P
MGT_118_REF_CLK_N NC AF3 MGT_118_REF_CLK_N
MGTRX0_118_P AE1 MGTRX0_118_P
MGTRX0_118_N AF1 MGTRX0_118_N
MGTRX1_118_P AH1 MGTRX1_118_P
MGTRX1_118_N AG1 MGTRX1_118_N
U15
C144 C145 C146 C147 10NF 25V
MGTAVTTTX_118_1 AJ3 MGTAVTTTX_118_1
MGTAVTTTX_118 AD3 MGTAVTTTX_118
MGTTX0_118_P AD2 MGTTX0_118_P
MGTTX0_118_N AE2 MGTTX0_118_N
MGTTX1_118_P AJ2 MGTTX1_118_P
MGTTX1_118_N AH2 MGTTX1_118_N
MGT_AVTT
FB19 220@100M
FB20 220@100M
C122 C121 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
P3
S1 DL0P
S2 DL0N
S3 DL1P
S4 DL1N
S5 DL2P
S6 DL2N
S7 DL3P
S8 DL3N
S16 SL0P
S15 SL0N
S14 SL1P
S13 SL1N
S12 SL2P
S11 SL2N
S10 SL3P
S9 SL3N
MGTRX0_114_P
MGTRX0_114_N
MGTRX1_114_P
MGTRX1_114_N
SIG_GND1 G1
SIG_GND2 G2
SIG_GND3 G3
SIG_GND4 G4
SIG_GND5 G5
SIG_GND6 G6
SIG_GND7 G7
SIG_GND8 G8
SIG_GND9 G9
SIG_GND10 G19
FCN-268F036-G/3DB
3V3
JP4
ODIS
R58 10K
C130 10NF
GND
FAULT
R79 150R
D2
OPTICAL MODULE FAULT - RED LED
C131 10NF
R97 5K1
RS7 3K9
U21
MAX9032AKA
RS9 6K8
U20
MAX9032AKA
C127 10NF
RS8 3K9
U22
AND2
SN74AHC1G08DCKR
U18
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
TPS2031D
R99 10K
C129 10NF
C128 100NF
C138 4.7UF 16V
C90 22UF
P3
S19 DL0P
S20 DL0N
S21 DL1P
S22 DL1N
S23 DL2P
S24 DL2N
S25 DL3P
S26 DL3N
S34 SL0P
S33 SL0N
S32 SL1P
S31 SL1N
S30 SL2P
S29 SL2N
S28 SL3P
S27 SL3N
FCN-268F036-G/3DB
JP5
R51 10K
C134 10NF
R52 150R
D1
OPTICAL MODULE FAULT - RED LED
C132 10NF
R98 5K1
R93 3K9
U23
AND2
SN74AHC1G08DCKR
R94 6K8
C133 10NF
R95 3K9
U19
TPS2031D
R100 10K
C135 10NF
C136 100NF
C139 4.7UF 16V
C91 22UF
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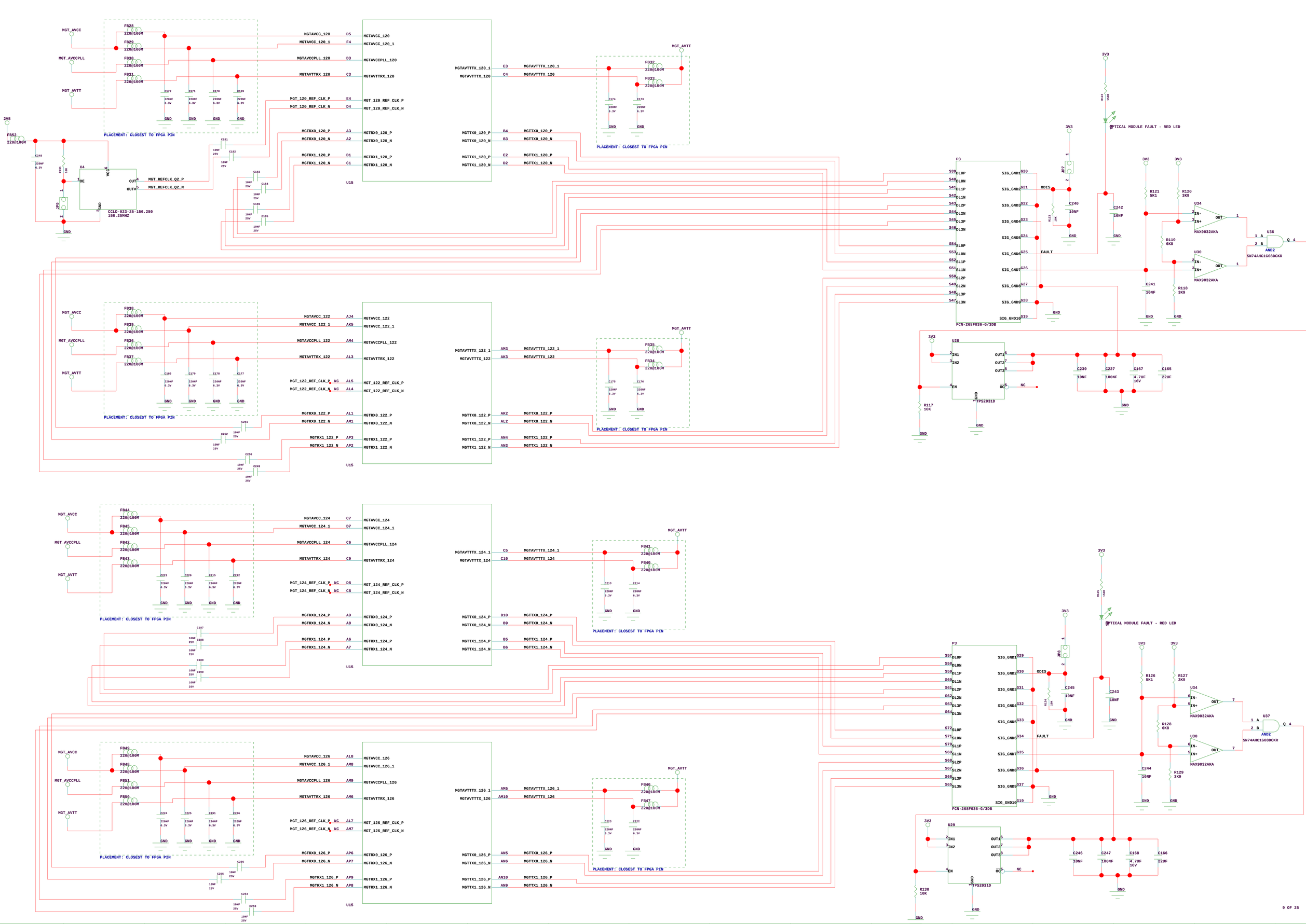
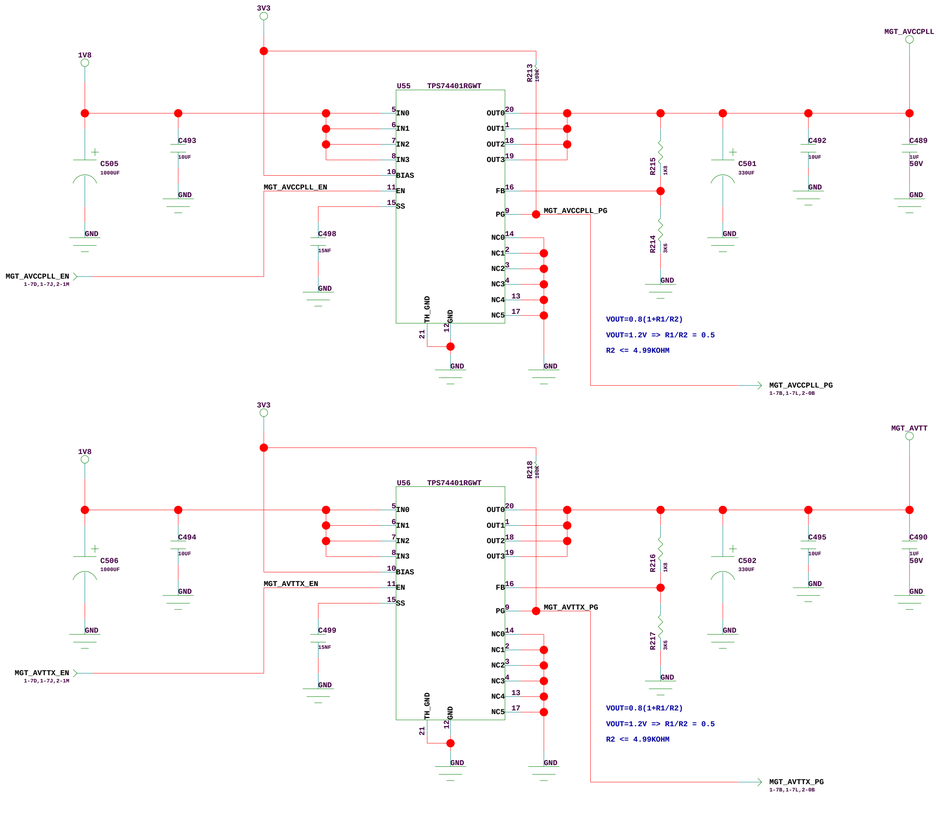
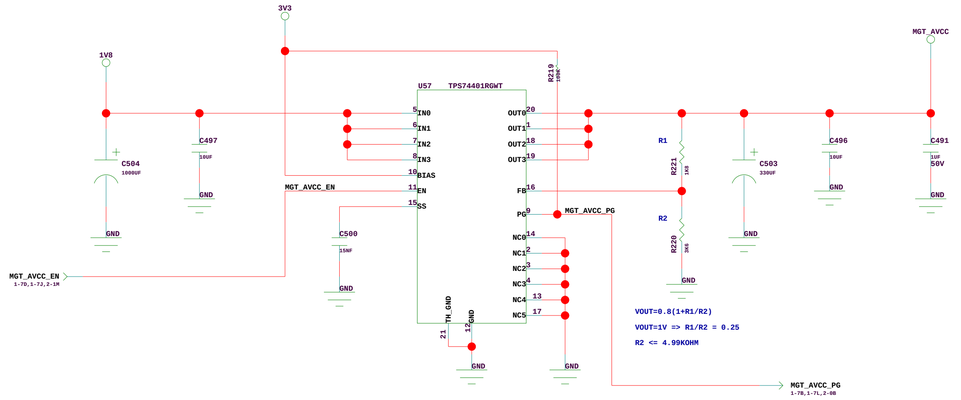
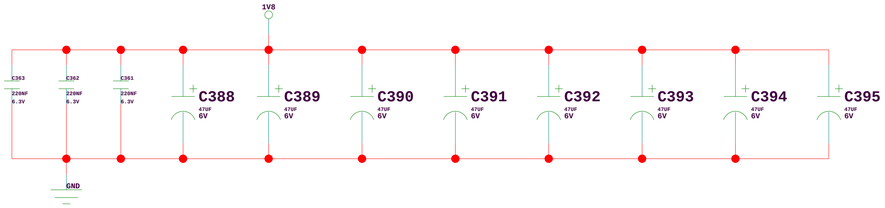
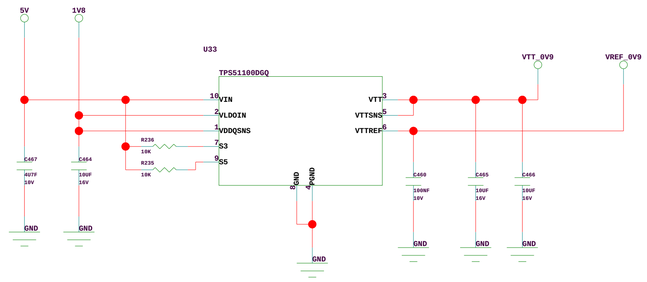

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB28 220@100M
FB29 220@100M
FB30 220@100M
FB31 220@100M
C172 220NF 6.3V
C171 220NF 6.3V
C170 220NF 6.3V
C169 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_120 D5 MGTAVCC_120
MGTAVCC_120_1 F4 MGTAVCC_120_1
MGTAVCCPLL_120 D3 MGTAVCCPLL_120
MGTAVTTRX_120 C3 MGTAVTTRX_120
MGT_120_REF_CLK_P E4 MGT_120_REF_CLK_P
MGT_120_REF_CLK_N D4 MGT_120_REF_CLK_N
MGTRX0_120_P A3 MGTRX0_120_P
MGTRX0_120_N A2 MGTRX0_120_N
MGTRX1_120_P D1 MGTRX1_120_P
MGTRX1_120_N C1 MGTRX1_120_N
U15
MGTAVTTTX_120_1 E3 MGTAVTTTX_120_1
MGTAVTTTX_120 C4 MGTAVTTTX_120
MGTTX0_120_P B4 MGTTX0_120_P
MGTTX0_120_N B3 MGTTX0_120_N
MGTTX1_120_P E2 MGTTX1_120_P
MGTTX1_120_N D2 MGTTX1_120_N
FB32 220@100M
FB33 220@100M
C174 220NF 6.3V
C173 220NF 6.3V
2V5
FB52 220@100M
C248 220NF 6.3V
R131 10K
X4
OE
VCC
OUT
GND
JP9
CCLD-023-25-156.250
156.25MHZ
MGT_REFCLK_Q2_P
MGT_REFCLK_Q2_N
C181 10NF 25V
C182 10NF 25V
C183 10NF 25V
C184 10NF 25V
C186 10NF 25V
C185 10NF 25V
P3
DL0P S39
DL0N S40
DL1P S41
DL1N S42
DL2P S43
DL2N S44
DL3P S45
DL3N S46
SL0P S54
SL0N S53
SL1P S52
SL1N S51
SL2P S50
SL2N S49
SL3P S48
SL3N S47
FCN-268F036-G/3DB
SIG_GND1 G20
SIG_GND2 G21
SIG_GND3 G22
SIG_GND4 G23
SIG_GND5 G24
SIG_GND6 G25
SIG_GND7 G26
SIG_GND8 G27
SIG_GND9 G28
SIG_GND10 G19
ODIS
FAULT
JP7
R123 10K
C240 10NF
C242 10NF
3V3
R132 150R
OPTICAL MODULE FAULT - RED LED
R121 5K1
R120 3K9
R119 6K8
R118 3K9
U34 MAX9032AKA
U30 MAX9032AKA
U36 AND2 SN74AHC1G08DCKR
C241 10NF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB38 220@100M
FB39 220@100M
FB36 220@100M
FB37 220@100M
C180 220NF 6.3V
C179 220NF 6.3V
C178 220NF 6.3V
C177 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_122 AJ4 MGTAVCC_122
MGTAVCC_122_1 AK5 MGTAVCC_122_1
MGTAVCCPLL_122 AM4 MGTAVCCPLL_122
MGTAVTTRX_122 AL3 MGTAVTTRX_122
MGT_122_REF_CLK_P NC AL5 MGT_122_REF_CLK_P
MGT_122_REF_CLK_N NC AL4 MGT_122_REF_CLK_N
MGTRX0_122_P AL1 MGTRX0_122_P
MGTRX0_122_N AM1 MGTRX0_122_N
MGTRX1_122_P AP3 MGTRX1_122_P
MGTRX1_122_N AP2 MGTRX1_122_N
U15
MGTAVTTTX_122_1 AM3 MGTAVTTTX_122_1
MGTAVTTTX_122 AK3 MGTAVTTTX_122
MGTTX0_122_P AK2 MGTTX0_122_P
MGTTX0_122_N AL2 MGTTX0_122_N
MGTTX1_122_P AN4 MGTTX1_122_P
MGTTX1_122_N AN3 MGTTX1_122_N
FB35 220@100M
FB34 220@100M
C175 220NF 6.3V
C176 220NF 6.3V
C251 10NF 25V
C252 10NF 25V
C250 10NF 25V
C249 10NF 25V
C256 10NF 25V
C255 10NF 25V
C254 10NF 25V
C253 10NF 25V
U28
U29
IN1
IN2
EN
GND
OUT1
OUT2
OUT3
OC
NC
TPS2031D
R117 10K
R130 10K
C239 10NF
C227 100NF
C167 4.7UF 16V
C165 22UF
C246 10NF
C247 100NF
C168 4.7UF 16V
C166 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB49 220@100M
FB48 220@100M
FB51 220@100M
FB50 220@100M
C224 220NF 6.3V
C225 220NF 6.3V
C191 220NF 6.3V
C226 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_126 AL8 MGTAVCC_126
MGTAVCC_126_1 AM8 MGTAVCC_126_1
MGTAVCCPLL_126 AM9 MGTAVCCPLL_126
MGTAVTTRX_126 AM6 MGTAVTTRX_126
MGT_126_REF_CLK_P NC AL7 MGT_126_REF_CLK_P
MGT_126_REF_CLK_N NC AM7 MGT_126_REF_CLK_N
MGTRX0_126_P AP6 MGTRX0_126_P
MGTRX0_126_N AP7 MGTRX0_126_N
MGTRX1_126_P AP9 MGTRX1_126_P
MGTRX1_126_N AP8 MGTRX1_126_N
U15
MGTAVTTTX_126_1 AM5 MGTAVTTTX_126_1
MGTAVTTTX_126 AM10 MGTAVTTTX_126
MGTTX0_126_P AN5 MGTTX0_126_P
MGTTX0_126_N AN6 MGTTX0_126_N
MGTTX1_126_P AN10 MGTTX1_126_P
MGTTX1_126_N AN9 MGTTX1_126_N
FB46 220@100M
FB47 220@100M
C223 220NF 6.3V
C222 220NF 6.3V
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB44 220@100M
FB45 220@100M
FB42 220@100M
FB43 220@100M
C221 220NF 6.3V
C220 220NF 6.3V
C215 220NF 6.3V
C212 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_124 C7 MGTAVCC_124
MGTAVCC_124_1 D7 MGTAVCC_124_1
MGTAVCCPLL_124 C6 MGTAVCCPLL_124
MGTAVTTRX_124 C9 MGTAVTTRX_124
MGT_124_REF_CLK_P NC D8 MGT_124_REF_CLK_P
MGT_124_REF_CLK_N NC C8 MGT_124_REF_CLK_N
MGTRX0_124_P A9 MGTRX0_124_P
MGTRX0_124_N A8 MGTRX0_124_N
MGTRX1_124_P A6 MGTRX1_124_P
MGTRX1_124_N A7 MGTRX1_124_N
U15
MGTAVTTTX_124_1 C5 MGTAVTTTX_124_1
MGTAVTTTX_124 C10 MGTAVTTTX_124
MGTTX0_124_P B10 MGTTX0_124_P
MGTTX0_124_N B9 MGTTX0_124_N
MGTTX1_124_P B5 MGTTX1_124_P
MGTTX1_124_N B6 MGTTX1_124_N
FB41 220@100M
FB40 220@100M
C213 220NF 6.3V
C214 220NF 6.3V
C187 10NF 25V
C188 10NF 25V
C189 10NF 25V
C190 10NF 25V
P3
DL0P S57
DL0N S58
DL1P S59
DL1N S60
DL2P S61
DL2N S62
DL3P S63
DL3N S64
SL0P S72
SL0N S71
SL1P S70
SL1N S69
SL2P S68
SL2N S67
SL3P S66
SL3N S65
FCN-268F036-G/3DB
SIG_GND1 G29
SIG_GND2 G30
SIG_GND3 G31
SIG_GND4 G32
SIG_GND5 G33
SIG_GND6 G34
SIG_GND7 G35
SIG_GND8 G36
SIG_GND9 G37
SIG_GND10 G19
ODIS
FAULT
JP8
R124 10K
C245 10NF
C243 10NF
3V3
R125 150R
OPTICAL MODULE FAULT - RED LED
R126 5K1
R127 3K9
R128 6K8
R129 3K9
U34 MAX9032AKA
U30 MAX9032AKA
U37 AND2 SN74AHC1G08DCKR
C244 10NF
9 OF 25

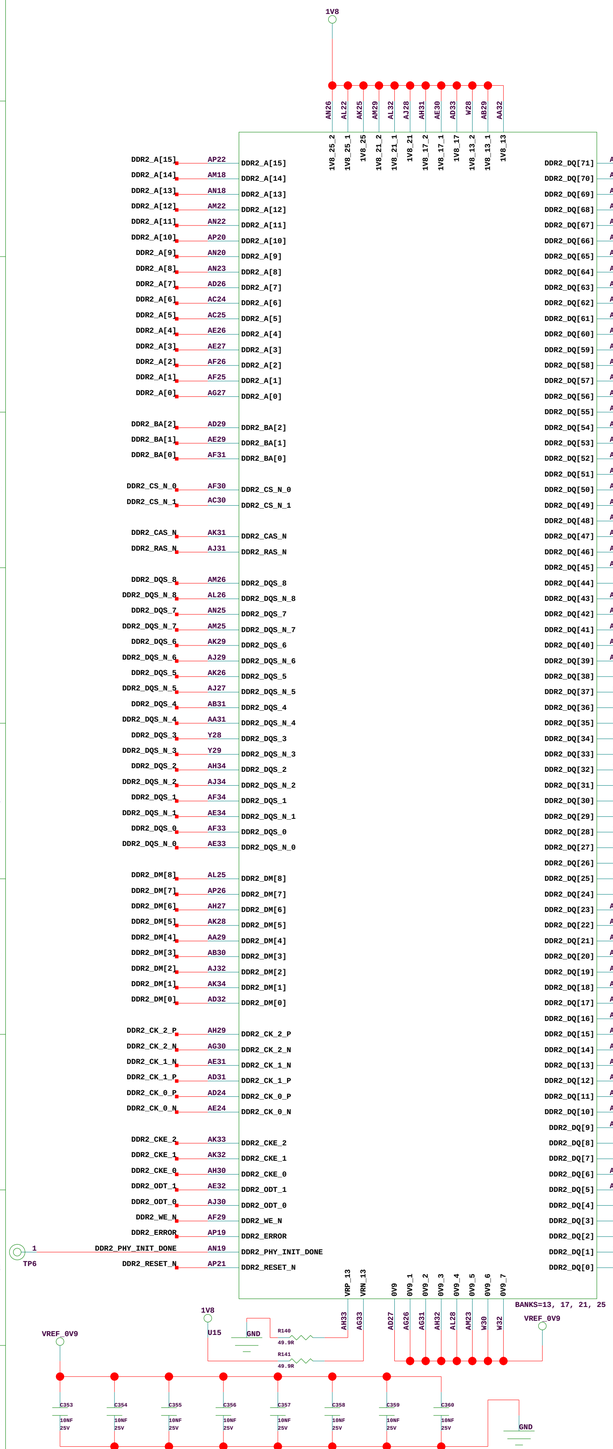

3V3
1V8
MGT_AVCCPLL
U55 TPS74401RGWT
C505 1000UF
C493 10UF
C498 15NF
C501 330UF
C492 10UF
C489 1UF 50V
R213 100K
R215 1K
R214 3K3
MGT_AVCCPLL_EN
MGT_AVCCPLL_PG
IN0 IN1 IN2 IN3 BIAS EN SS
OUT0 OUT1 OUT2 OUT3 FB PG
NC0 NC1 NC2 NC3 NC4 NC5
TH_GND GND
VOUT=0.8(1+R1/R2)
VOUT=1.2V => R1/R2 = 0.5
R2 <= 4.99KOHM
MGT_AVCCPLL_EN 1-7D,1-7J,2-1M
MGT_AVCCPLL_PG 1-7D,1-7L,2-0B


3V3
1V8
MGT_AVCC
U57 TPS74401RGWT
C504 1000UF
C497 10UF
C500 15NF
C503 330UF
C496 10UF
C491 1UF 50V
R219 100K
R1
R221 1K
R2
R220 3K
MGT_AVCC_EN
MGT_AVCC_PG
IN0 IN1 IN2 IN3 BIAS EN SS
OUT0 OUT1 OUT2 OUT3 FB PG
NC0 NC1 NC2 NC3 NC4 NC5
TH_GND GND
VOUT=0.8(1+R1/R2)
VOUT=1V => R1/R2 = 0.25
R2 <= 4.99KOHM
MGT_AVCC_EN 1-7D,1-7J,2-1M
MGT_AVCC_PG 1-7D,1-7L,2-0B

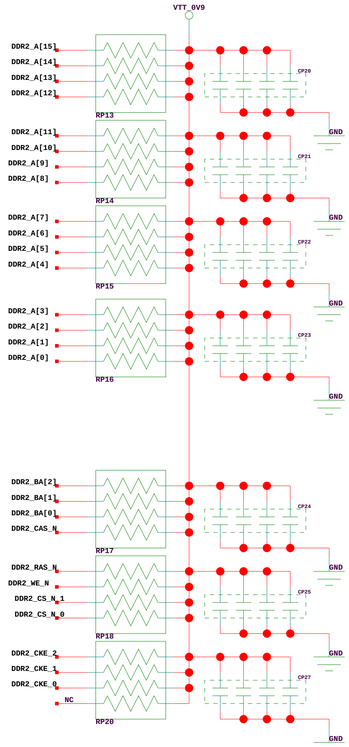
3V3
1V8
MGT_AVTT
U56 TPS74401RGWT
C506 1000UF
C494 10UF
C499 15NF
C502 330UF
C495 10UF
C490 1UF 50V
R218 100K
R216 1K
R217 3K
MGT_AVTTX_EN
MGT_AVTTX_PG
IN0 IN1 IN2 IN3 BIAS EN SS
OUT0 OUT1 OUT2 OUT3 FB PG
NC0 NC1 NC2 NC3 NC4 NC5
TH_GND GND
VOUT=0.8(1+R1/R2)
VOUT=1.2V => R1/R2 = 0.5
R2 <= 4.99KOHM
MGT_AVTTX_EN 1-7D,1-7J,2-1M
MGT_AVTTX_PG 1-7D,1-7L,2-0B

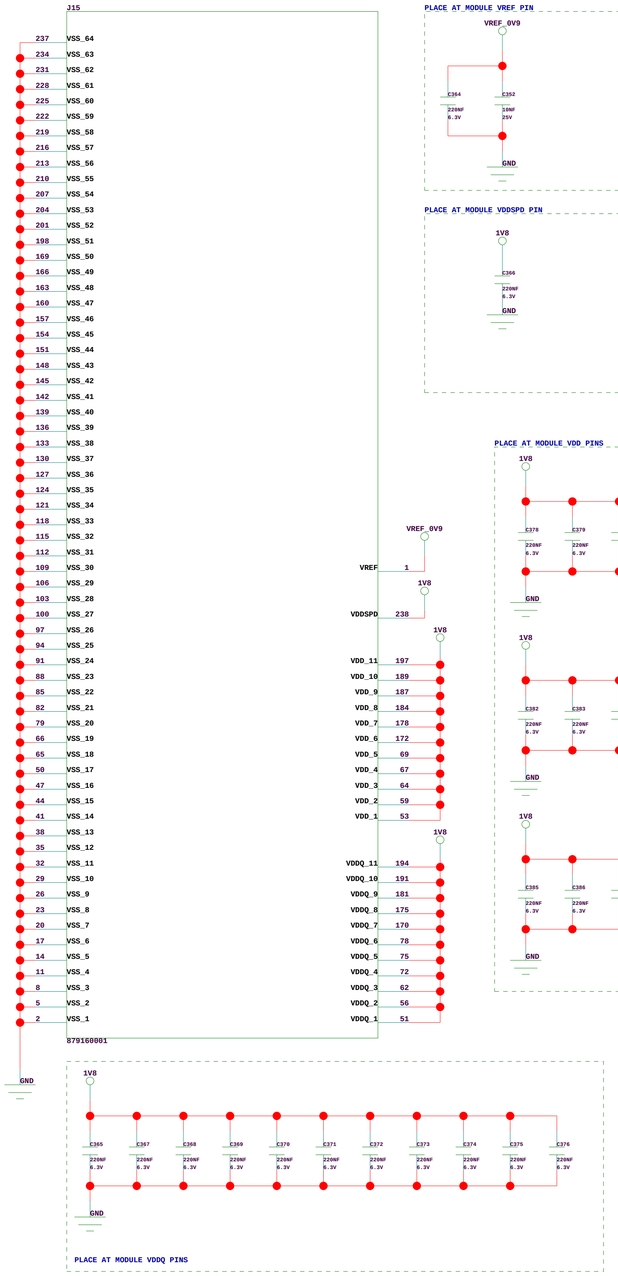


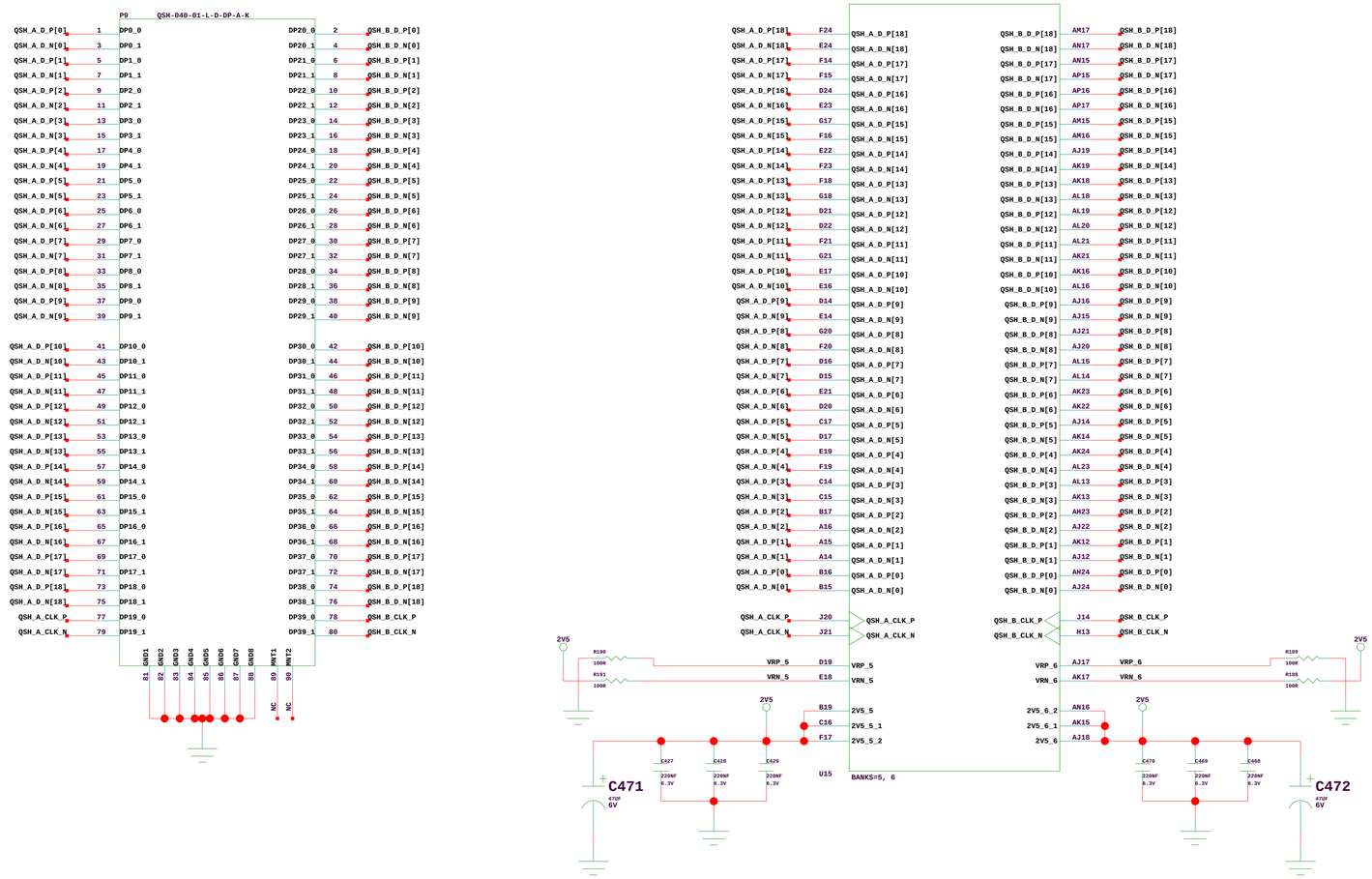


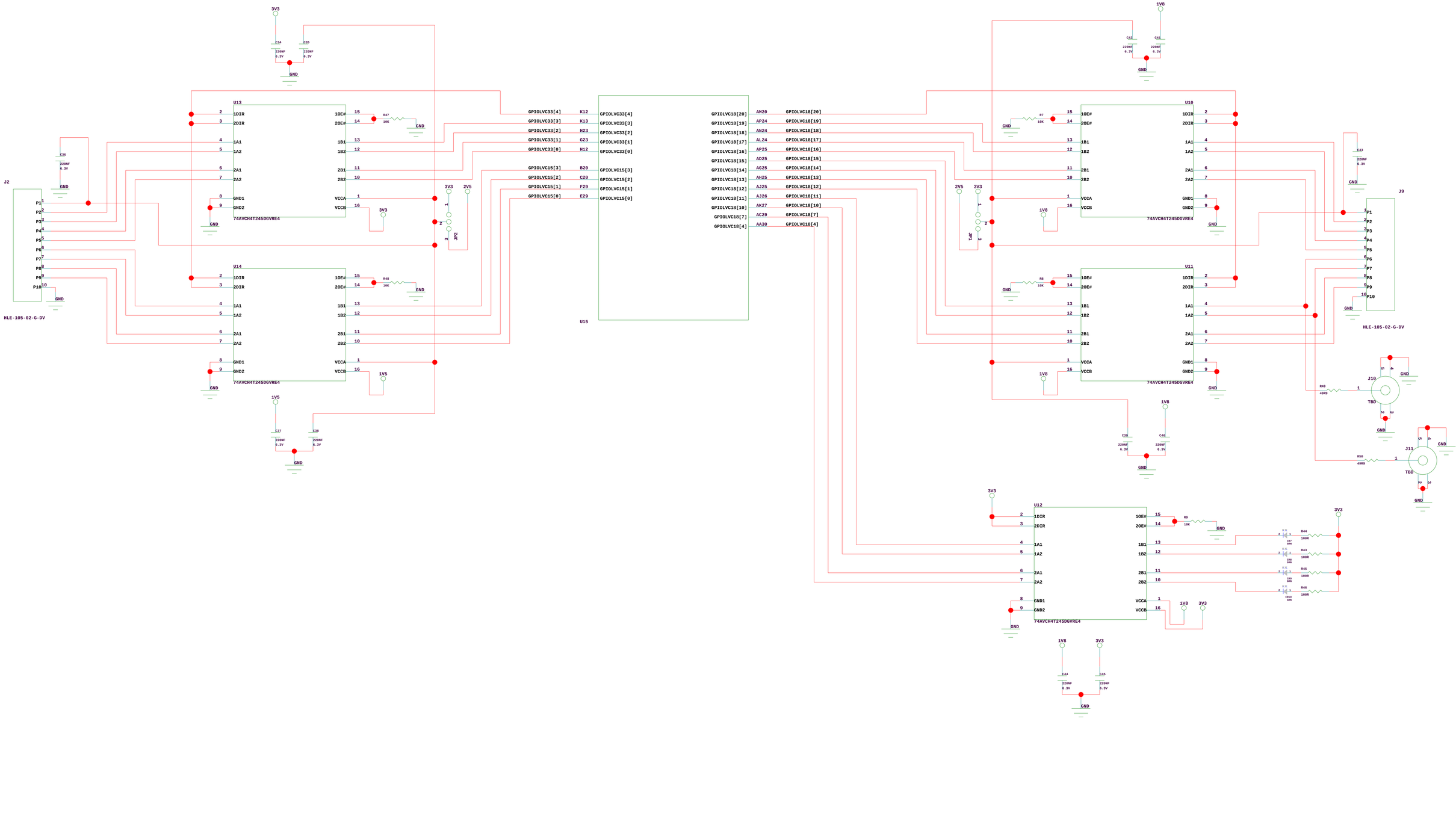


VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

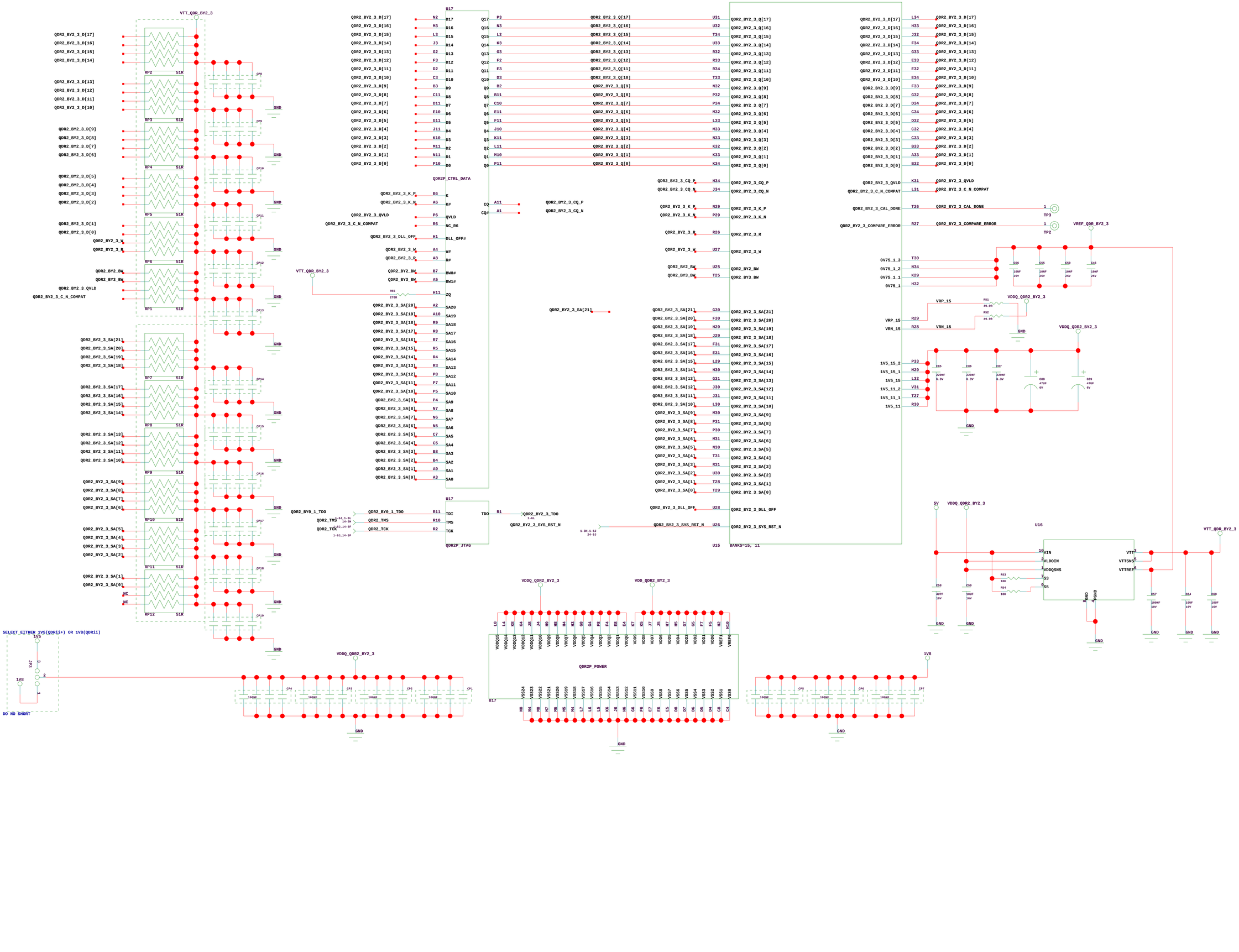





P9 QSH-040-01-L-D-DP-A-K
QSH_A_D_P[0] 1 DP0_0 DP20_0 2 QSH_B_D_P[0]
QSH_A_D_N[0] 3 DP0_1 DP20_1 4 QSH_B_D_N[0]
QSH_A_D_P[1] 5 DP1_0 DP21_0 6 QSH_B_D_P[1]
QSH_A_D_N[1] 7 DP1_1 DP21_1 8 QSH_B_D_N[1]
QSH_A_D_P[2] 9 DP2_0 DP22_0 10 QSH_B_D_P[2]
QSH_A_D_N[2] 11 DP2_1 DP22_1 12 QSH_B_D_N[2]
QSH_A_D_P[3] 13 DP3_0 DP23_0 14 QSH_B_D_P[3]
QSH_A_D_N[3] 15 DP3_1 DP23_1 16 QSH_B_D_N[3]
QSH_A_D_P[4] 17 DP4_0 DP24_0 18 QSH_B_D_P[4]
QSH_A_D_N[4] 19 DP4_1 DP24_1 20 QSH_B_D_N[4]
QSH_A_D_P[5] 21 DP5_0 DP25_0 22 QSH_B_D_P[5]
QSH_A_D_N[5] 23 DP5_1 DP25_1 24 QSH_B_D_N[5]
QSH_A_D_P[6] 25 DP6_0 DP26_0 26 QSH_B_D_P[6]
QSH_A_D_N[6] 27 DP6_1 DP26_1 28 QSH_B_D_N[6]
QSH_A_D_P[7] 29 DP7_0 DP27_0 30 QSH_B_D_P[7]
QSH_A_D_N[7] 31 DP7_1 DP27_1 32 QSH_B_D_N[7]
QSH_A_D_P[8] 33 DP8_0 DP28_0 34 QSH_B_D_P[8]
QSH_A_D_N[8] 35 DP8_1 DP28_1 36 QSH_B_D_N[8]
QSH_A_D_P[9] 37 DP9_0 DP29_0 38 QSH_B_D_P[9]
QSH_A_D_N[9] 39 DP9_1 DP29_1 40 QSH_B_D_N[9]
QSH_A_D_P[10] 41 DP10_0 DP30_0 42 QSH_B_D_P[10]
QSH_A_D_N[10] 43 DP10_1 DP30_1 44 QSH_B_D_N[10]
QSH_A_D_P[11] 45 DP11_0 DP31_0 46 QSH_B_D_P[11]
QSH_A_D_N[11] 47 DP11_1 DP31_1 48 QSH_B_D_N[11]
QSH_A_D_P[12] 49 DP12_0 DP32_0 50 QSH_B_D_P[12]
QSH_A_D_N[12] 51 DP12_1 DP32_1 52 QSH_B_D_N[12]
QSH_A_D_P[13] 53 DP13_0 DP33_0 54 QSH_B_D_P[13]
QSH_A_D_N[13] 55 DP13_1 DP33_1 56 QSH_B_D_N[13]
QSH_A_D_P[14] 57 DP14_0 DP34_0 58 QSH_B_D_P[14]
QSH_A_D_N[14] 59 DP14_1 DP34_1 60 QSH_B_D_N[14]
QSH_A_D_P[15] 61 DP15_0 DP35_0 62 QSH_B_D_P[15]
QSH_A_D_N[15] 63 DP15_1 DP35_1 64 QSH_B_D_N[15]
QSH_A_D_P[16] 65 DP16_0 DP36_0 66 QSH_B_D_P[16]
QSH_A_D_N[16] 67 DP16_1 DP36_1 68 QSH_B_D_N[16]
QSH_A_D_P[17] 69 DP17_0 DP37_0 70 QSH_B_D_P[17]
QSH_A_D_N[17] 71 DP17_1 DP37_1 72 QSH_B_D_N[17]
QSH_A_D_P[18] 73 DP18_0 DP38_0 74 QSH_B_D_P[18]
QSH_A_D_N[18] 75 DP18_1 DP38_1 76 QSH_B_D_N[18]
QSH_A_CLK_P 77 DP19_0 DP39_0 78 QSH_B_CLK_P
QSH_A_CLK_N 79 DP19_1 DP39_1 80 QSH_B_CLK_N
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 MNT1 MNT2
81 82 83 84 85 86 87 88 89 90
NC NC
QSH_A_D_P[18] F24 QSH_A_D_P[18]
QSH_A_D_N[18] E24 QSH_A_D_N[18]
QSH_A_D_P[17] F14 QSH_A_D_P[17]
QSH_A_D_N[17] F15 QSH_A_D_N[17]
QSH_A_D_P[16] D24 QSH_A_D_P[16]
QSH_A_D_N[16] E23 QSH_A_D_N[16]
QSH_A_D_P[15] G17 QSH_A_D_P[15]
QSH_A_D_N[15] F16 QSH_A_D_N[15]
QSH_A_D_P[14] E22 QSH_A_D_P[14]
QSH_A_D_N[14] F23 QSH_A_D_N[14]
QSH_A_D_P[13] F18 QSH_A_D_P[13]
QSH_A_D_N[13] G18 QSH_A_D_N[13]
QSH_A_D_P[12] D21 QSH_A_D_P[12]
QSH_A_D_N[12] D22 QSH_A_D_N[12]
QSH_A_D_P[11] F21 QSH_A_D_P[11]
QSH_A_D_N[11] G21 QSH_A_D_N[11]
QSH_A_D_P[10] E17 QSH_A_D_P[10]
QSH_A_D_N[10] E16 QSH_A_D_N[10]
QSH_A_D_P[9] D14 QSH_A_D_P[9]
QSH_A_D_N[9] E14 QSH_A_D_N[9]
QSH_A_D_P[8] G20 QSH_A_D_P[8]
QSH_A_D_N[8] F20 QSH_A_D_N[8]
QSH_A_D_P[7] D16 QSH_A_D_P[7]
QSH_A_D_N[7] D15 QSH_A_D_N[7]
QSH_A_D_P[6] E21 QSH_A_D_P[6]
QSH_A_D_N[6] D20 QSH_A_D_N[6]
QSH_A_D_P[5] C17 QSH_A_D_P[5]
QSH_A_D_N[5] D17 QSH_A_D_N[5]
QSH_A_D_P[4] E19 QSH_A_D_P[4]
QSH_A_D_N[4] F19 QSH_A_D_N[4]
QSH_A_D_P[3] C14 QSH_A_D_P[3]
QSH_A_D_N[3] C15 QSH_A_D_N[3]
QSH_A_D_P[2] B17 QSH_A_D_P[2]
QSH_A_D_N[2] A16 QSH_A_D_N[2]
QSH_A_D_P[1] A15 QSH_A_D_P[1]
QSH_A_D_N[1] A14 QSH_A_D_N[1]
QSH_A_D_P[0] B16 QSH_A_D_P[0]
QSH_A_D_N[0] B15 QSH_A_D_N[0]
QSH_A_CLK_P J20 QSH_A_CLK_P
QSH_A_CLK_N J21 QSH_A_CLK_N
VRP_5 D19 VRP_5
VRN_5 E18 VRN_5
B19 2V5_5
C16 2V5_5_1
F17 2V5_5_2
U15
BANKS=5, 6
QSH_B_D_P[18] AM17 QSH_B_D_P[18]
QSH_B_D_N[18] AN17 QSH_B_D_N[18]
QSH_B_D_P[17] AN15 QSH_B_D_P[17]
QSH_B_D_N[17] AP15 QSH_B_D_N[17]
QSH_B_D_P[16] AP16 QSH_B_D_P[16]
QSH_B_D_N[16] AP17 QSH_B_D_N[16]
QSH_B_D_P[15] AM15 QSH_B_D_P[15]
QSH_B_D_N[15] AM16 QSH_B_D_N[15]
QSH_B_D_P[14] AJ19 QSH_B_D_P[14]
QSH_B_D_N[14] AK19 QSH_B_D_N[14]
QSH_B_D_P[13] AK18 QSH_B_D_P[13]
QSH_B_D_N[13] AL18 QSH_B_D_N[13]
QSH_B_D_P[12] AL19 QSH_B_D_P[12]
QSH_B_D_N[12] AL20 QSH_B_D_N[12]
QSH_B_D_P[11] AL21 QSH_B_D_P[11]
QSH_B_D_N[11] AK21 QSH_B_D_N[11]
QSH_B_D_P[10] AK16 QSH_B_D_P[10]
QSH_B_D_N[10] AL16 QSH_B_D_N[10]
QSH_B_D_P[9] AJ16 QSH_B_D_P[9]
QSH_B_D_N[9] AJ15 QSH_B_D_N[9]
QSH_B_D_P[8] AJ21 QSH_B_D_P[8]
QSH_B_D_N[8] AJ20 QSH_B_D_N[8]
QSH_B_D_P[7] AL15 QSH_B_D_P[7]
QSH_B_D_N[7] AL14 QSH_B_D_N[7]
QSH_B_D_P[6] AK23 QSH_B_D_P[6]
QSH_B_D_N[6] AK22 QSH_B_D_N[6]
QSH_B_D_P[5] AJ14 QSH_B_D_P[5]
QSH_B_D_N[5] AK14 QSH_B_D_N[5]
QSH_B_D_P[4] AK24 QSH_B_D_P[4]
QSH_B_D_N[4] AL23 QSH_B_D_N[4]
QSH_B_D_P[3] AL13 QSH_B_D_P[3]
QSH_B_D_N[3] AK13 QSH_B_D_N[3]
QSH_B_D_P[2] AH23 QSH_B_D_P[2]
QSH_B_D_N[2] AJ22 QSH_B_D_N[2]
QSH_B_D_P[1] AK12 QSH_B_D_P[1]
QSH_B_D_N[1] AJ12 QSH_B_D_N[1]
QSH_B_D_P[0] AH24 QSH_B_D_P[0]
QSH_B_D_N[0] AJ24 QSH_B_D_N[0]
QSH_B_CLK_P J14 QSH_B_CLK_P
QSH_B_CLK_N H13 QSH_B_CLK_N
VRP_6 AJ17 VRP_6
VRN_6 AK17 VRN_6
2V5_6_2 AN16
2V5_6_1 AK15
2V5_6 AJ18
2V5
R190 100R
R191 100R
C427 220NF 6.3V
C428 220NF 6.3V
C429 220NF 6.3V
C471 470F 6V
R189 100R
R188 100R
C470 220NF 6.3V
C469 220NF 6.3V
C468 220NF 6.3V
C472 470F 6V

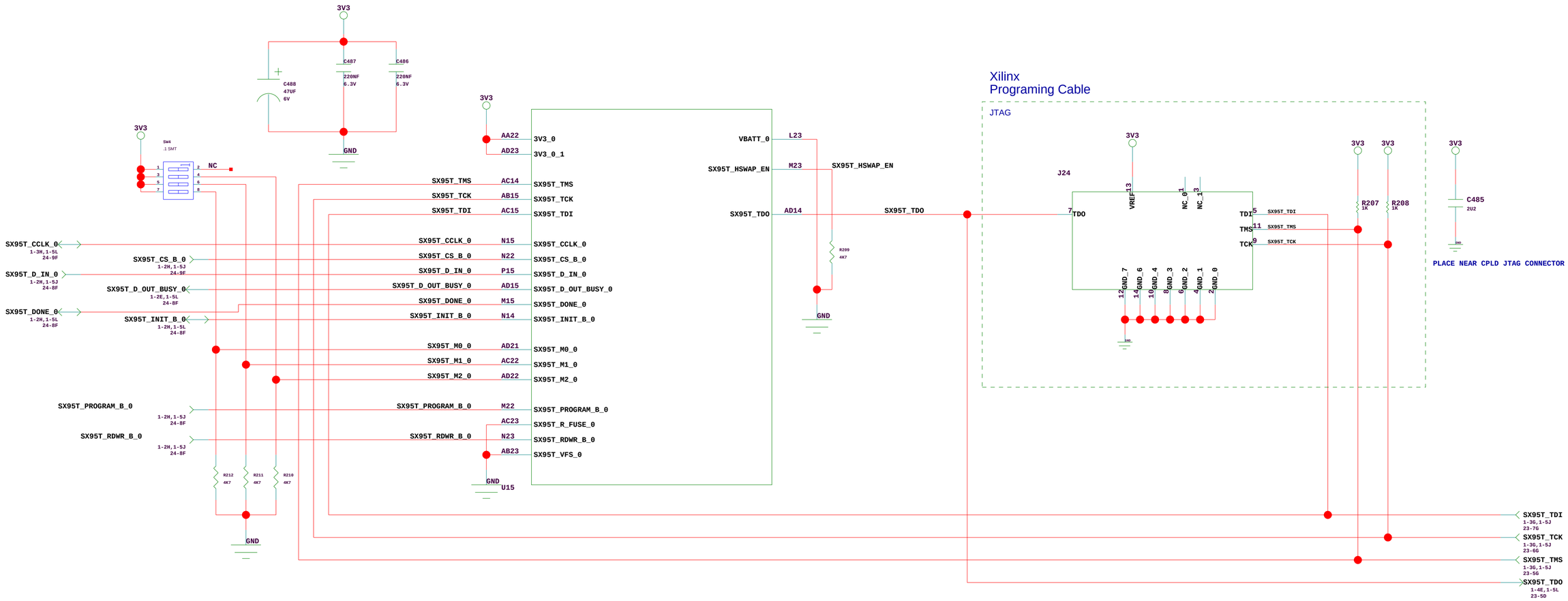

3V3
C34
220NF
6.3V
C35
220NF
6.3V
GND
U13
1DIR
2DIR
1A1
1A2
2A1
2A2
GND1
GND2
1OE#
2OE#
1B1
1B2
2B1
2B2
VCCA
VCCB
R47
10K
74AVCH4T245DGVRE4
C36
J2
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
HLE-105-02-G-DV
JP2
2V5
U14
R48
1V5
C37
C38
U15
GPIOLVC33[4]
GPIOLVC33[3]
GPIOLVC33[2]
GPIOLVC33[1]
GPIOLVC33[0]
GPIOLVC15[3]
GPIOLVC15[2]
GPIOLVC15[1]
GPIOLVC15[0]
K12
K13
H23
G23
H12
B20
C20
F29
E29
GPIOLVC18[20]
GPIOLVC18[19]
GPIOLVC18[18]
GPIOLVC18[17]
GPIOLVC18[16]
GPIOLVC18[15]
GPIOLVC18[14]
GPIOLVC18[13]
GPIOLVC18[12]
GPIOLVC18[11]
GPIOLVC18[10]
GPIOLVC18[7]
GPIOLVC18[4]
AM20
AP24
AN24
AL24
AP25
AD25
AG25
AH25
AJ25
AJ26
AK27
AC29
AA30
1V8
C42
C41
U10
U11
R7
R8
JP1
C43
J9
J10
J11
R49
R50
TBD
U12
R9
R44
R43
R45
R46
C44
C45
13 OF 25

VTT_QDR_BY0_1
VDDQ_QDR2_BY0_1
VDD_QDR2_BY0_1
VREF_QDR_BY0_1
U63
QDR2P_CTRL_DATA
QDR2P_JTAG
QDR2P_POWER
U15
BANKS=23, 19
U62
TPS51100DGQ
VIN
VLDOIN
VDDQSNS
S3
S5
VTT
VTTSNS
VTTREF
GND
PGND
RP27 51R
RP28 51R
RP29 51R
RP30 51R
RP31 51R
RP32 51R
RP33 51R
RP34 51R
RP35 51R
RP36 51R
RP37 51R
RP38 51R
R304 270R
R300 49.9R
R301 49.9R
R302 10K
R303 10K
TP7
TP8
JP29
QDR2_BY0_1_D[17]
QDR2_BY0_1_D[0]
QDR2_BY0_1_Q[17]
QDR2_BY0_1_Q[0]
QDR2_BY0_1_SA[21]
QDR2_BY0_1_SA[0]
QDR2_BY0_1_K_P
QDR2_BY0_1_K_N
QDR2_BY0_1_CQ_P
QDR2_BY0_1_CQ_N
QDR2_BY0_1_QVLD
QDR2_BY0_1_C_N_COMPAT
QDR2_BY0_1_DLL_OFF
QDR2_BY0_1_W
QDR2_BY0_1_R
QDR2_BY0_BW
QDR2_BY1_BW
QDR2_BY0_1_CAL_DONE
QDR2_BY0_1_COMPARE_ERROR
QDR2_BY0_1_TDO
QDR2_BY0_1_SYS_RST_N
QDR2_TDI
QDR2_TMS
QDR2_TCK
0V75_0_3
0V75_0_2
0V75_0_1
0V75_0
VRP_23
VRN_23
1V5_23_2
1V5_23_1
1V5_23
1V5_19_2
1V5_19_1
1V5_19
5V
1V5
1V8
SELECT EITHER 1V5(QDRii+) OR 1V8(QDRii)
DO NO SHORT


VTT_QDR_BY2_3
RP1 51R
RP2 51R
RP3 51R
RP4 51R
RP5 51R
RP6 51R
RP7 51R
RP8 51R
RP9 51R
RP10 51R
RP11 51R
RP12 51R
CP1
CP2
CP3
CP4
CP5
CP6
CP7
CP8
CP9
CP10
CP11
CP12
CP13
CP14
CP15
CP16
CP17
CP18
CP19
GND
QDR2_BY2_3_D[17]
QDR2_BY2_3_D[16]
QDR2_BY2_3_D[15]
QDR2_BY2_3_D[14]
QDR2_BY2_3_D[13]
QDR2_BY2_3_D[12]
QDR2_BY2_3_D[11]
QDR2_BY2_3_D[10]
QDR2_BY2_3_D[9]
QDR2_BY2_3_D[8]
QDR2_BY2_3_D[7]
QDR2_BY2_3_D[6]
QDR2_BY2_3_D[5]
QDR2_BY2_3_D[4]
QDR2_BY2_3_D[3]
QDR2_BY2_3_D[2]
QDR2_BY2_3_D[1]
QDR2_BY2_3_D[0]
QDR2_BY2_3_W
QDR2_BY2_3_R
QDR2_BY2_BW
QDR2_BY3_BW
QDR2_BY2_3_QVLD
QDR2_BY2_3_C_N_COMPAT
QDR2_BY2_3_SA[21]
QDR2_BY2_3_SA[20]
QDR2_BY2_3_SA[19]
QDR2_BY2_3_SA[18]
QDR2_BY2_3_SA[17]
QDR2_BY2_3_SA[16]
QDR2_BY2_3_SA[15]
QDR2_BY2_3_SA[14]
QDR2_BY2_3_SA[13]
QDR2_BY2_3_SA[12]
QDR2_BY2_3_SA[11]
QDR2_BY2_3_SA[10]
QDR2_BY2_3_SA[9]
QDR2_BY2_3_SA[8]
QDR2_BY2_3_SA[7]
QDR2_BY2_3_SA[6]
QDR2_BY2_3_SA[5]
QDR2_BY2_3_SA[4]
QDR2_BY2_3_SA[3]
QDR2_BY2_3_SA[2]
QDR2_BY2_3_SA[1]
QDR2_BY2_3_SA[0]
NC
NC
U17
QDR2P_CTRL_DATA
QDR2_BY2_3_K_P
QDR2_BY2_3_K_N
QDR2_BY2_3_QVLD
QDR2_BY2_3_C_N_COMPAT
QDR2_BY2_3_DLL_OFF
QDR2_BY2_3_W
QDR2_BY2_3_R
QDR2_BY2_BW
QDR2_BY3_BW
R55 270R
QDR2_BY2_3_SA[20]
QDR2_BY2_3_SA[19]
QDR2_BY2_3_SA[18]
QDR2_BY2_3_SA[17]
QDR2_BY2_3_SA[16]
QDR2_BY2_3_SA[15]
QDR2_BY2_3_SA[14]
QDR2_BY2_3_SA[13]
QDR2_BY2_3_SA[12]
QDR2_BY2_3_SA[11]
QDR2_BY2_3_SA[10]
QDR2_BY2_3_SA[9]
QDR2_BY2_3_SA[8]
QDR2_BY2_3_SA[7]
QDR2_BY2_3_SA[6]
QDR2_BY2_3_SA[5]
QDR2_BY2_3_SA[4]
QDR2_BY2_3_SA[3]
QDR2_BY2_3_SA[2]
QDR2_BY2_3_SA[1]
QDR2_BY2_3_SA[0]
QDR2_BY2_3_CQ_P
QDR2_BY2_3_CQ_N
QDR2_BY0_1_TDO
QDR2_TMS
QDR2_TCK
QDR2P_JTAG
QDR2_BY2_3_TDO
QDR2_BY2_3_SYS_RST_N
U15
BANKS=15, 11
QDR2P_POWER
VDDQ_QDR2_BY2_3
VDD_QDR2_BY2_3
1V8
5V
SELECT_EITHER_1V5(QDRii+) OR 1V8(QDRii)
JP3
1V5
DO NOT SHORT
100NF
U16
VIN
VLDOIN
VDDQSNS
S3
S5
VTT
VTTSNS
VTTREF
PGND
GND
TP2
TP3
VREF_QDR_BY2_3
0V75_1_3
0V75_1_2
0V75_1_1
0V75_1
VRP_15
VRN_15
1V5_15_2
1V5_15_1
1V5_15
1V5_11_2
1V5_11_1
1V5_11
5V_VDDQ_QDR2_BY2_3

TBD

VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input



Place components close to CPU

L1
600Ohm 200mA
C1P-1 0.1UF
C1P-2 .01UF
C1P-3 470PF
AP24
AP25

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J3: "1V5"

1V5_CPU
L8 1600Ohm 1.5A
L9 1600Ohm 1.5A
J3 10N M SMT
R046 0
R047 0
NO POP
1V5

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J4: "1V8"

1V8_CPU
L11 1600Ohm 1.5A
J4 0.11N M SMT
R042 0
NO POP
1V8

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J5: "2V5"

2V5_CPU
L12 1600Ohm 1.5A
J5 0.11N M SMT
R043 0
NO POP
2V5

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J6: "3V3"

3V3_CPU
L13 1600Ohm 1.5A
J6 0.11N M SMT
R044 0
NO POP
3V3

Place components close to CPU

L2 600Ohm 200mA
L3 600Ohm 200mA
C1P-7 0.1UF
C1P-8 0.1UF
C1P-9 .01UF
C1P-10 470PF
C1P-11 0.1UF
C1P-12 0.1UF
C1P-13 .01UF
C1P-14 470PF

Place components close to CPU

L4 600Ohm 200mA
C1P-4 0.1UF
C1P-5 .01UF
C1P-6 470PF

U1 440EPX
POWER
AVDD
ADDD
EAVDD
EADDD
AP26
AP27

Alternate power input terminal
Two 10A fuses result in 16A rating

+5.0 V

5V
C1 220UF
C2 220UF
C3 0.1UF
C4 0.1UF

Bulk Decoupling
5V_CPU
C0-1 1000UF
C0-2 1000UF

1V5_CPU
CPU Core by-pass caps place as close to CPU Vdd pins as possible
C1-1 0.1UF
C1-2 0.1UF
C1-3 0.1UF
C1-4 0.1UF
C1-5 0.1UF
C1-6 0.1UF
C1-7 0.1UF
C1-8 0.1UF
C1-9 0.1UF
C1-10 0.1UF
C1-11 0.1UF
C1-12 0.1UF
C1-13 0.1UF
C1-14 0.1UF
C1-15 0.1UF
C1-16 0.1UF
C1-17 0.1UF
C1-18 0.1UF
C1-19 0.1UF
C1-20 0.1UF
C1-21 0.1UF
C1-22 0.1UF
C1-23 0.1UF
C1-24 0.1UF
C1-25 0.1UF
C1-26 0.1UF
C1-27 0.1UF
C1-28 0.1UF
C1-29 0.1UF
C1-30 0.1UF
C1-31 0.1UF
C1-32 0.1UF
C1-33 0.1UF
C1-34 0.1UF
C1-35 0.1UF
C1-36 0.1UF
C1-37 0.1UF
C1-38 0.1UF

Bulk Decoupling
3V3_CPU
C0-7 1000UF
C0-8 1000UF

3V3_CPU
CPU Core by-pass caps place as close to CPU SOVdd pins as possible
C1-39 0.1UF
C1-40 0.1UF
C1-41 0.1UF
C1-42 0.1UF
C1-43 0.1UF
C1-44 0.1UF
C1-45 0.1UF
C1-46 0.1UF
C1-47 0.1UF
C1-48 0.1UF
C1-49 0.1UF
C1-50 0.1UF
C1-51 0.1UF
C1-52 0.1UF

Bulk Decoupling
2V5_CPU
C0-9 1000UF
C0-10 1000UF

2V5_CPU
CPU Core by-pass caps place as close to CPU SOVdd pins as possible
C1-53 0.1UF
C1-54 0.1UF
C1-55 0.1UF
C1-56 0.1UF
C1-57 0.1UF
C1-58 0.1UF
C1-59 0.1UF
C1-60 0.1UF
C1-61 0.1UF
C1-62 0.1UF
C1-63 0.1UF
C1-64 0.1UF

Bulk Decoupling
1V8_CPU
C0-11 1000UF
C0-12 1000UF

1V8_CPU
CPU Core by-pass caps place as close to CPU OVdd pins as possible
C1-65 0.1UF
C1-66 0.1UF
C1-67 0.1UF
C1-68 0.1UF
C1-69 0.1UF
C1-70 0.1UF
C1-71 0.1UF
C1-72 0.1UF
C1-73 0.1UF
C1-74 0.1UF
C1-75 0.1UF
C1-76 0.1UF
C1-77 0.1UF
C1-78 0.1UF
C1-79 0.1UF
C1-80 0.1UF
C1-81 0.1UF
C1-82 0.1UF

Each Analog GND tied to Digital GND at a single point.

+1.8 V

Place all components within this block close together

~2.9Amp

J15
C5 0.1UF
C6 330UF
C7 330UF
C10 0.1UF

Place these 4 caps close to DDR parts
J16
C0-3 1000UF
C0-4 1000UF
C0-5 1000UF
C0-6 1000UF

5V
C6 22UF
C5 0.1UF
GND
U2 LTC3736EUF
VIN_LTC3736_1
R1 10
C7 2.2UF
C8 0.1UF
C32 22UF
SI7540DP SO-8
Q1
Q2
L20 1.5UH
Axle_OUT1
C18 220PF
RSET1 84.2K, 1%
VOUT= 0.6v(1+R1/R2)
R4 33.2K, 1%
RSET2 22.1K, 1%
R2 22.1K, 1%
R3 10K
C19 220PF
100PF
CE-1
R045 0
C23B 0.1UF
SENSE1+
TG1
SW1
BG1
PGND_B
VFB1
ITH1
IPRG1
RUN/SS
TRACK
PGOOD
SENSE2+
TG2
SW2
BG2
PGND
VFB2
ITH2
IPRG2
PLLLPF
SYNC/FCB
PWR_GOOD
1-3E,1-4C,1-4E
18-2F,23-7H
24-B3
L21 1.5UH
C11 0.1UF
C17 330UF
C12 330UF
C13 0.1UF
RSET3 33.2K, 1%
C14 220PF
RSET4 22.1K, 1%
C24 100PF
C25 100PF
VOUT= 0.6v(1+R1/R2)
PLLLPF = VIN = 750khz
~3.6Amp

+1.5 V

Place all components within this block close together

+0.9 V

5V
U3 TPS51100
VIN
S3
S5
GND
PAD
VDDQSNS
VIN_S3
VTTREF
VTTSNS
VTT
PGND
C23 2.2UF
C24 100UF
C25 100UF
C31 220PF
C21 0.1UF
C22 0.1UF
Use 25mil trace
VOUT_VREF_+0.9V
1-4C
C26 100UF
C27 100UF
C28 100UF
C29 0.1UF
C30 0.1UF

VTT_+0.9V
VTT island by-pass caps place evenly across VTT island
(1 cap for every 2 signals terminated)
(1 Tantalum Cap on each end of island)
VTT regulator placed at center of VTT island
CVT-1 330UF
CVT-2 330UF
CVT-3 0.1UF
CVT-4 0.1UF
CVT-5 0.1UF
CVT-6 0.1UF
CVT-7 0.1UF
CVT-8 0.1UF
CVT-9 0.1UF
CVT-10 0.1UF
CVT-11 0.1UF
CVT-12 0.1UF
CVT-13 0.1UF
CVT-14 0.1UF

Place all components within
this block close together

+3.3 V

U4
AXM016A0X3

5V
3V3
16Amp

C210 0.1UF
C211 1UF
C200 220UF
C201 220UF
C202 22UF
C203 22UF
C204 0.1UF
C205 0.1UF
C206 1UF
C207 10UF
C208 330UF
C209 330UF

VIN1
VIN2
ON/OFF
GND1
GND2
VOUT1
VOUT2
VOUT3
SENSE
TRIM

RSET5
3.16K, 1%

Place RSET5 between pins 1 & 3

Place one cap at each corner of the PCB

3V3

CB-13 100UF
CB-14 100UF
CB-15 100UF
CB-16 100UF

Place all components within
this block close together

+12 V

U5
PTN04050CAZ

5V
12V
1.0Amp

C216 22UF
C217 100UF
C218 100UF
C219 22UF

VIN
VOUT
GND
ADJ

RSET6
1.33K, 1%

Place RSET6 between pins 1 & 3

Place all components within
this block close together

-12 V

U6
PTN04050AAZ

5V
-12V
500mAmp

C228 4.7UF
C229 100UF
C230 100UF
C231 4.7UF

VIN
VOUT
INH
GND
ADJ

RSET7
1.96K, 1%

Place RSET7 between pins 1 & 4

Place all components within
this block close together

+1.0 V

U7
MCP1726

3V3
+1.0V
1.0 Amp

C232 4.7UF
C233 2.2UF
C234 .01UF

VIN1
VIN2
VOUT1
ADJ
SHDN#
PGD
GND
PAD
CDLY

RSET8
33.2K, 1%
RSET9
22.1K, 1%

VOUT= 0.41v(R1/R2)+0.41V

NO POP

Place all components within
this block close together

+2.5 V

U8
MCP1726

3V3
2V5
1.0 Amp

C235 4.7UF
C236 2.2UF
C237 .01UF

VIN1
VIN2
VOUT1
ADJ
SHDN#
PGD
GND
PAD
CDLY

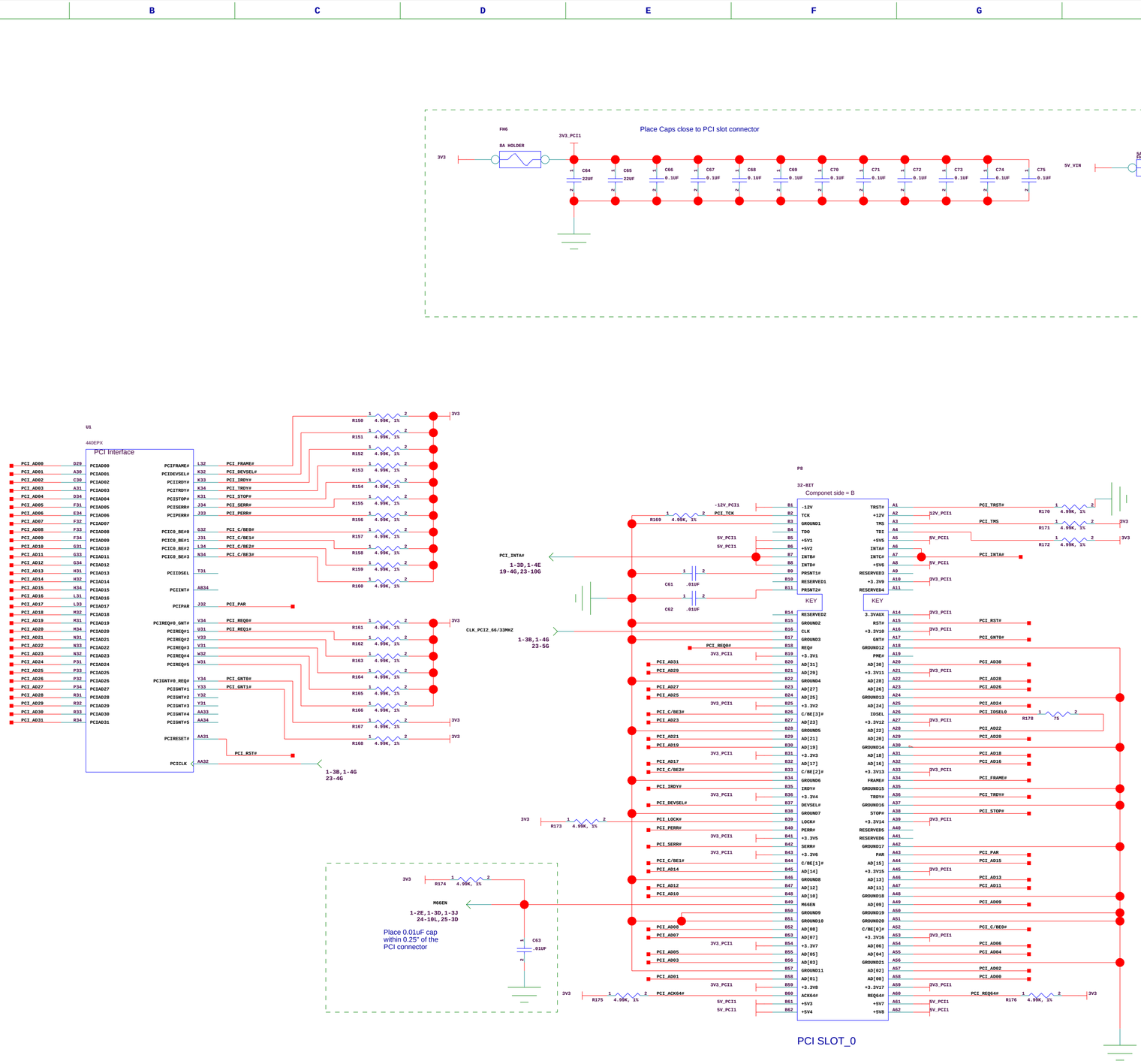
RSET10
110K, 1%
RSET11
22.1K, 1%

VOUT= 0.41v(R1/R2)+0.41V

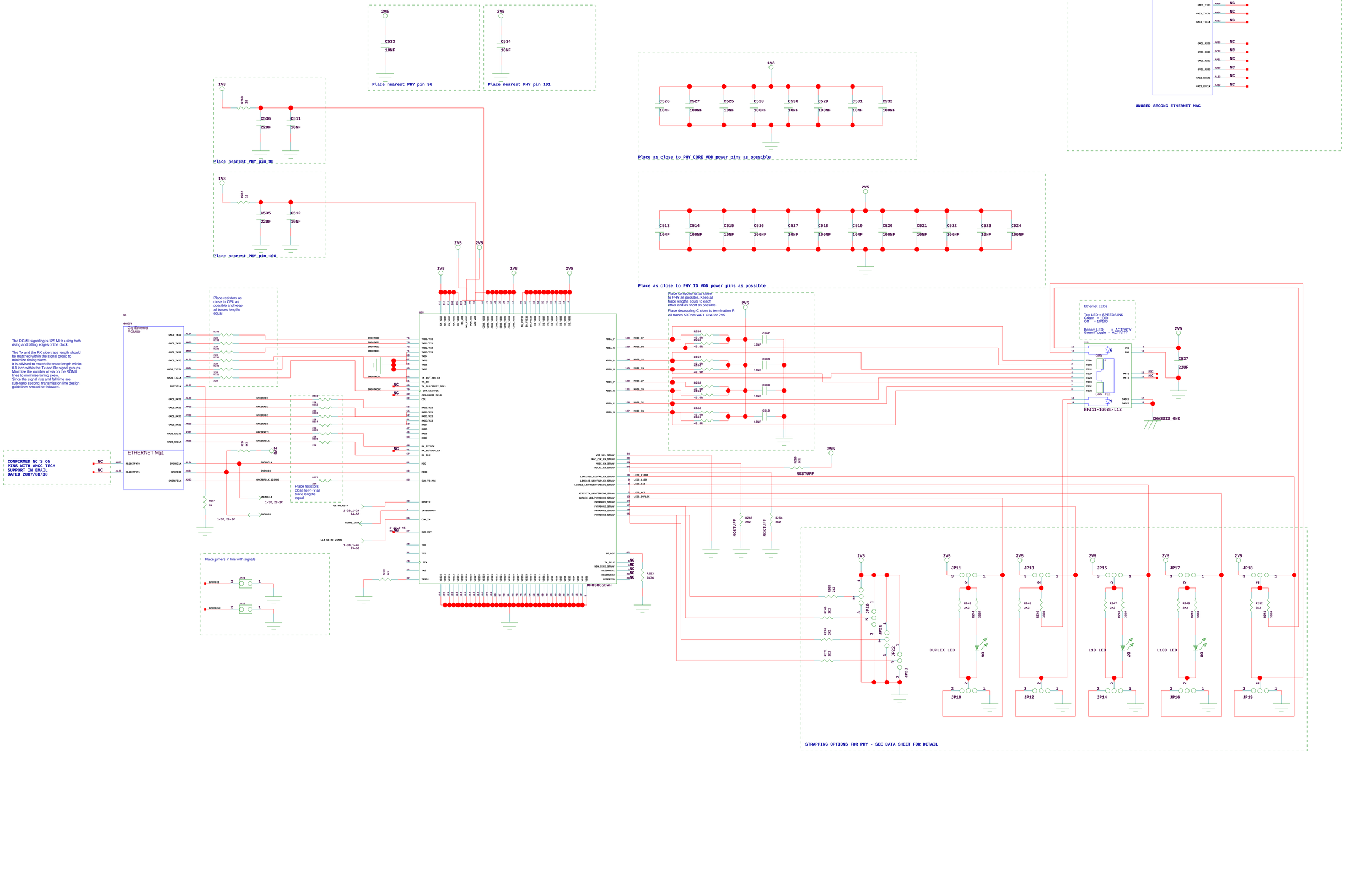
NO POP

PWR_GOOD

1-3E,1-4C,1-4E
17-3F,23-7M
24-8J



Optional PRSNT signals are not used, max 25W is available		
PRSNT1#	PRSNT2#	Expansion Configuration
Open	Open	No expansion board present
Ground	Open	Expansion board present, 25 W maximum
Open	Ground	Expansion board present, 15 W maximum
Ground	Ground	Expansion board present, 7.5 W maximum


Gig-Ethernet RGMII
ETHERNET Mgt.
DP83865DVH
Place nearest PHY pin 96
Place nearest PHY pin 101
Place nearest PHY pin 98
Place nearest PHY pin 100
Place as close to PHY CORE VDD power pins as possible
Place as close to PHY IO VDD power pins as possible
Place resistors as close to CPU as possible and keep all traces lengths equal
Place resistors close to PHY all trace lengths equal
Place jumpers in line with signals
The RGMII signaling is 125 MHz using both rising and falling edges of the clock.
The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.
Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.
CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30
UNUSED SECOND ETHERNET MAC
Ethernet LEDs
Top LED = SPEED/LINK
Green = 1000
Off = 10/100
Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY
HFJ11-1G02E-L12
CHASSIS_GND
STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL
DUPLEX LED
L10 LED
L100 LED
NOSTUFF

U1

USB 2.0 DEVICE

440EPX

USB2CLK	A5	NC
USB2TXVAL	C6	NC
USB2TXRDY_REFEN	B6	NC
USB2RXACT_HOLDREQ_RCVINH	D7	NC
USB2RXVAL_LEAKTEST2	C8	NC
USB2RXERR_EXTREQ#	A4	NC
USB2XCVRSEL_EXTACK#	M3	NC
USB2TERMSEL_BUSREQ	P4	NC
USB2LS0_DRVINH1	R2	NC
USB2LS1_LEAKTEST_HOLDPRI	P1	NC
USB2OM0	R3	NC
USB2OM1	R4	NC
USB2SUSP_HOLDACK	C5	NC

USB 2.0 PHY
HOST/DEVICE

USB2XCVR J2 USB2_XCVR_D+

USB2XCVR# J1 USB2_XCVR_D-

USB2REXT L3 — R182 3.40K, 1% — (GND)

USB2XTAL N2 — (GND)

USB2XTAL# N3 — 0 — RO30 — RO30: [1:2] for 440EPx [3:2] for 440GRx — (GND)

CLK_USB2.0_48MHZ

1-2B,1-4G
23-9J

CRITICAL PLACEMENT

Place SP2 very close to P6

SP2 PGB102ST23WR

SP2 PGB102ST23WR

CHASSIS_GND

CHASSIS_GND

VR3 5.5V 20A

VR4 5.5V 20A

CHASSIS_GND

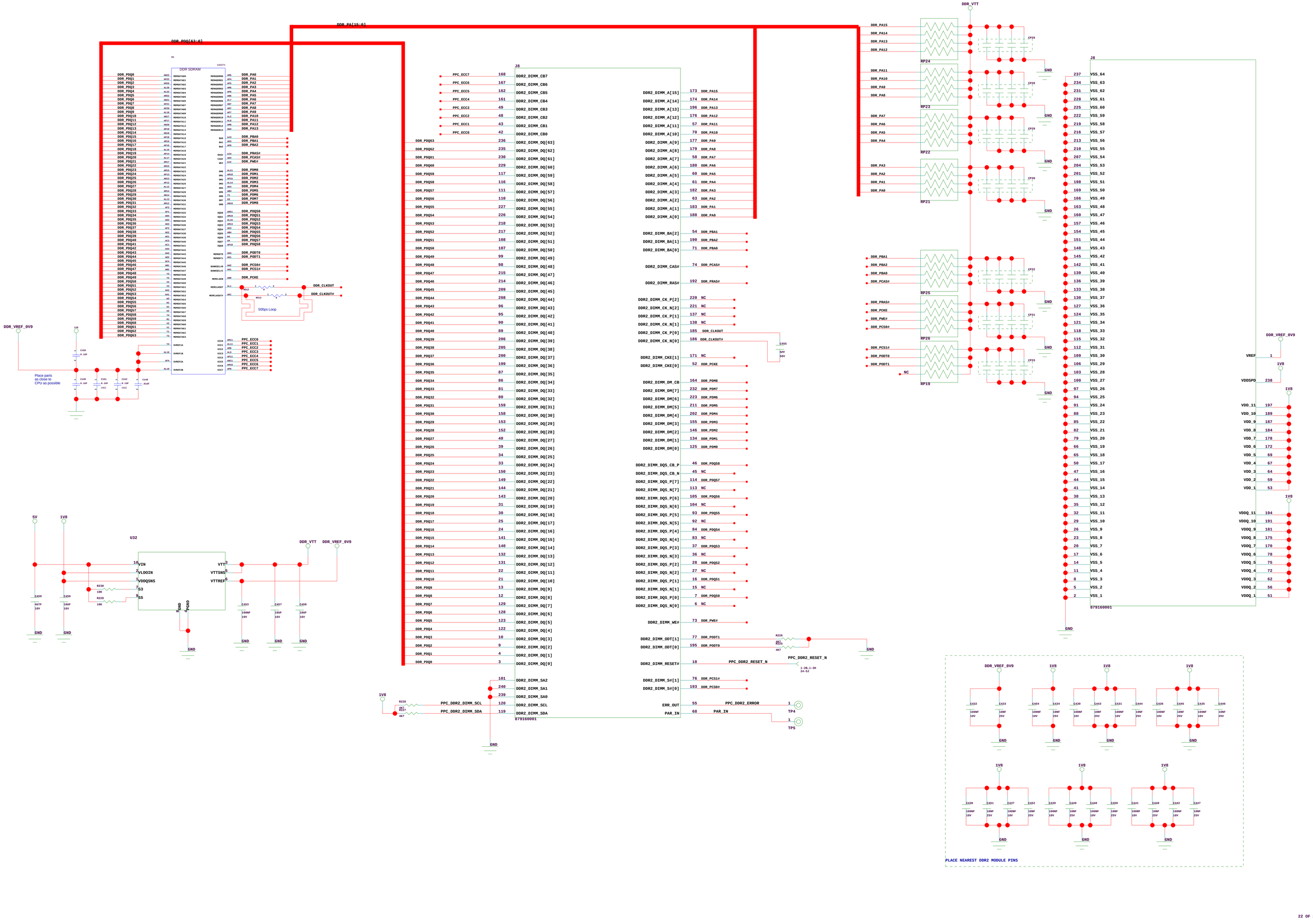
CHASSIS_GND

P6

F TH

GND
D+
D-
VCC

USB2_VCC_PI — R194 1-2D,1-3E 15K — R195 24-6C 15K — (GND)


DDR_PD0[63:0]
DDR_PA[15:0]
DDR SDRAM
U1
44DEPX
DDR_PD0
DDR_PD1
DDR_PD2
DDR_PD3
DDR_PD4
DDR_PD5
DDR_PD6
DDR_PD7
DDR_PD8
DDR_PD9
DDR_PD10
DDR_PD11
DDR_PD12
DDR_PD13
DDR_PD14
DDR_PD15
DDR_PD16
DDR_PD17
DDR_PD18
DDR_PD19
DDR_PD20
DDR_PD21
DDR_PD22
DDR_PD23
DDR_PD24
DDR_PD25
DDR_PD26
DDR_PD27
DDR_PD28
DDR_PD29
DDR_PD30
DDR_PD31
DDR_PD32
DDR_PD33
DDR_PD34
DDR_PD35
DDR_PD36
DDR_PD37
DDR_PD38
DDR_PD39
DDR_PD40
DDR_PD41
DDR_PD42
DDR_PD43
DDR_PD44
DDR_PD45
DDR_PD46
DDR_PD47
DDR_PD48
DDR_PD49
DDR_PD50
DDR_PD51
DDR_PD52
DDR_PD53
DDR_PD54
DDR_PD55
DDR_PD56
DDR_PD57
DDR_PD58
DDR_PD59
DDR_PD60
DDR_PD61
DDR_PD62
DDR_PD63
DDR_PA0
DDR_PA1
DDR_PA2
DDR_PA3
DDR_PA4
DDR_PA5
DDR_PA6
DDR_PA7
DDR_PA8
DDR_PA9
DDR_PA10
DDR_PA11
DDR_PA12
DDR_PA13
DDR_PA14
DDR_PA15
DDR_PBA0
DDR_PBA1
DDR_PBA2
DDR_PRAS#
DDR_PCAS#
DDR_PWE#
DDR_PDM0
DDR_PDM1
DDR_PDM2
DDR_PDM3
DDR_PDM4
DDR_PDM5
DDR_PDM6
DDR_PDM7
DDR_PDM8
DDR_PDQS0
DDR_PDQS1
DDR_PDQS2
DDR_PDQS3
DDR_PDQS4
DDR_PDQS5
DDR_PDQS6
DDR_PDQS7
DDR_PDQS8
DDR_PODT0
DDR_PODT1
DDR_PCS0#
DDR_PCS1#
DDR_PCKE
DDR_CLKOUT
DDR_CLKOUT#
PPC_ECC0
PPC_ECC1
PPC_ECC2
PPC_ECC3
PPC_ECC4
PPC_ECC5
PPC_ECC6
PPC_ECC7
R012
R013
500ps Loop
DDR_VREF_0V9
5V
1V8
C158
0.1UF
C148
0.1UF
C151
0.1UF
0402
C152
0.1UF
0402
C148
0.01UF
Place parts
as close to
CPU as possible
U32
VIN
VLDOIN
VDDQSNS
S3
S5
VTT
VTTSNS
VTTREF
GND
PGND
R230
10K
R229
10K
C459
.027F
10V
C456
.10UF
16V
C453
.100NF
10V
C457
.10UF
16V
C458
.10UF
16V
DDR_VTT
DDR_VREF_0V9
J8
DDR2_DIMM_CB7
DDR2_DIMM_CB6
DDR2_DIMM_CB5
DDR2_DIMM_CB4
DDR2_DIMM_CB3
DDR2_DIMM_CB2
DDR2_DIMM_CB1
DDR2_DIMM_CB0
DDR2_DIMM_DQ[63]
DDR2_DIMM_DQ[62]
DDR2_DIMM_DQ[61]
DDR2_DIMM_DQ[60]
DDR2_DIMM_DQ[59]
DDR2_DIMM_DQ[58]
DDR2_DIMM_DQ[57]
DDR2_DIMM_DQ[56]
DDR2_DIMM_DQ[55]
DDR2_DIMM_DQ[54]
DDR2_DIMM_DQ[53]
DDR2_DIMM_DQ[52]
DDR2_DIMM_DQ[51]
DDR2_DIMM_DQ[50]
DDR2_DIMM_DQ[49]
DDR2_DIMM_DQ[48]
DDR2_DIMM_DQ[47]
DDR2_DIMM_DQ[46]
DDR2_DIMM_DQ[45]
DDR2_DIMM_DQ[44]
DDR2_DIMM_DQ[43]
DDR2_DIMM_DQ[42]
DDR2_DIMM_DQ[41]
DDR2_DIMM_DQ[40]
DDR2_DIMM_DQ[39]
DDR2_DIMM_DQ[38]
DDR2_DIMM_DQ[37]
DDR2_DIMM_DQ[36]
DDR2_DIMM_DQ[35]
DDR2_DIMM_DQ[34]
DDR2_DIMM_DQ[33]
DDR2_DIMM_DQ[32]
DDR2_DIMM_DQ[31]
DDR2_DIMM_DQ[30]
DDR2_DIMM_DQ[29]
DDR2_DIMM_DQ[28]
DDR2_DIMM_DQ[27]
DDR2_DIMM_DQ[26]
DDR2_DIMM_DQ[25]
DDR2_DIMM_DQ[24]
DDR2_DIMM_DQ[23]
DDR2_DIMM_DQ[22]
DDR2_DIMM_DQ[21]
DDR2_DIMM_DQ[20]
DDR2_DIMM_DQ[19]
DDR2_DIMM_DQ[18]
DDR2_DIMM_DQ[17]
DDR2_DIMM_DQ[16]
DDR2_DIMM_DQ[15]
DDR2_DIMM_DQ[14]
DDR2_DIMM_DQ[13]
DDR2_DIMM_DQ[12]
DDR2_DIMM_DQ[11]
DDR2_DIMM_DQ[10]
DDR2_DIMM_DQ[9]
DDR2_DIMM_DQ[8]
DDR2_DIMM_DQ[7]
DDR2_DIMM_DQ[6]
DDR2_DIMM_DQ[5]
DDR2_DIMM_DQ[4]
DDR2_DIMM_DQ[3]
DDR2_DIMM_DQ[2]
DDR2_DIMM_DQ[1]
DDR2_DIMM_DQ[0]
DDR2_DIMM_SA2
DDR2_DIMM_SA1
DDR2_DIMM_SA0
DDR2_DIMM_SCL
DDR2_DIMM_SDA
879160001
DDR2_DIMM_A[15]
DDR2_DIMM_A[14]
DDR2_DIMM_A[13]
DDR2_DIMM_A[12]
DDR2_DIMM_A[11]
DDR2_DIMM_A[10]
DDR2_DIMM_A[9]
DDR2_DIMM_A[8]
DDR2_DIMM_A[7]
DDR2_DIMM_A[6]
DDR2_DIMM_A[5]
DDR2_DIMM_A[4]
DDR2_DIMM_A[3]
DDR2_DIMM_A[2]
DDR2_DIMM_A[1]
DDR2_DIMM_A[0]
DDR2_DIMM_BA[2]
DDR2_DIMM_BA[1]
DDR2_DIMM_BA[0]
DDR2_DIMM_CAS#
DDR2_DIMM_RAS#
DDR2_DIMM_CK_P[2]
DDR2_DIMM_CK_N[2]
DDR2_DIMM_CK_P[1]
DDR2_DIMM_CK_N[1]
DDR2_DIMM_CK_P[0]
DDR2_DIMM_CK_N[0]
DDR2_DIMM_CKE[1]
DDR2_DIMM_CKE[0]
DDR2_DIMM_DM_CB
DDR2_DIMM_DM[7]
DDR2_DIMM_DM[6]
DDR2_DIMM_DM[5]
DDR2_DIMM_DM[4]
DDR2_DIMM_DM[3]
DDR2_DIMM_DM[2]
DDR2_DIMM_DM[1]
DDR2_DIMM_DM[0]
DDR2_DIMM_DQS_CB_P
DDR2_DIMM_DQS_CB_N
DDR2_DIMM_DQS_P[7]
DDR2_DIMM_DQS_N[7]
DDR2_DIMM_DQS_P[6]
DDR2_DIMM_DQS_N[6]
DDR2_DIMM_DQS_P[5]
DDR2_DIMM_DQS_N[5]
DDR2_DIMM_DQS_P[4]
DDR2_DIMM_DQS_N[4]
DDR2_DIMM_DQS_P[3]
DDR2_DIMM_DQS_N[3]
DDR2_DIMM_DQS_P[2]
DDR2_DIMM_DQS_N[2]
DDR2_DIMM_DQS_P[1]
DDR2_DIMM_DQS_N[1]
DDR2_DIMM_DQS_P[0]
DDR2_DIMM_DQS_N[0]
DDR2_DIMM_WE#
DDR2_DIMM_ODT[1]
DDR2_DIMM_ODT[0]
DDR2_DIMM_RESET#
DDR2_DIMM_S#[1]
DDR2_DIMM_S#[0]
ERR_OUT
PAR_IN
DDR_CLKOUT
DDR_CLKOUT#
C455
.5PF
50V
PPC_DDR2_RESET_N
1-2R,1-3R
2A-5J
PPC_DDR2_ERROR
PAR_IN
TP4
TP5
R226
4K7
R228
4K7
R227
4K7
PPC_DDR2_DIMM_SCL
PPC_DDR2_DIMM_SDA
VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
DDR_VTT
RP24
RP23
RP22
RP21
RP25
RP26
RP19
CP26
CP28
CP29
CP30
CP32
CP31
CP33
GND
J8
VSS_64
VSS_63
VSS_62
VSS_61
VSS_60
VSS_59
VSS_58
VSS_57
VSS_56
VSS_55
VSS_54
VSS_53
VSS_52
VSS_51
VSS_50
VSS_49
VSS_48
VSS_47
VSS_46
VSS_45
VSS_44
VSS_43
VSS_42
VSS_41
VSS_40
VSS_39
VSS_38
VSS_37
VSS_36
VSS_35
VSS_34
VSS_33
VSS_32
VSS_31
VSS_30
VSS_29
VSS_28
VSS_27
VSS_26
VSS_25
VSS_24
VSS_23
VSS_22
VSS_21
VSS_20
VSS_19
VSS_18
VSS_17
VSS_16
VSS_15
VSS_14
VSS_13
VSS_12
VSS_11
VSS_10
VSS_9
VSS_8
VSS_7
VSS_6
VSS_5
VSS_4
VSS_3
VSS_2
VSS_1
879160001
DDR_VREF_0V9
VREF
1V8
VDDSPD
VDD_11
VDD_10
VDD_9
VDD_8
VDD_7
VDD_6
VDD_5
VDD_4
VDD_3
VDD_2
VDD_1
VDDQ_11
VDDQ_10
VDDQ_9
VDDQ_8
VDDQ_7
VDDQ_6
VDDQ_5
VDDQ_4
VDDQ_3
VDDQ_2
VDDQ_1
C432
C433
C454
C434
C430
C443
C431
C444
C436
C445
C435
C446
C438
C451
C437
C452
C439
C449
C440
C450
C441
C448
C442
C447
.100NF
10V
.10NF
25V
PLACE NEAREST DDR2 MODULE PINS

PWR_GOOD
1-30,1-4E
19-4E,19-4G

3V3

PWR_GOOD monitors the
+1.0v, 1V5, 1V8,
2V5, and 3V3 supplies

D1 BAV70
R41 10K
R42 100
C47 2.2UF
SPST SW1
U31 MIC2779M-29
IN VDD OUT RST/ MR/ GND
R28 2.2K
R29 3.3K
C31-1 0.1UF
GND

RESET_PBR#
1-4E

RESET_PORR
1-2B,1-4G
21-1B
0,11

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_3V3_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz

U9 CY22381FX_8211
C48 18PF
C49 18PF
22.1184MHZ
Y1
VDD XTALIN XTALOUT GND FS CLKC CLKB CLKA
R30 2.2K
R31 33
R32 33
R33 33
CLK_1
CLK_2
CLK_3
SEL_SYSCLK
1-2B,1-4E
24-7C
CLK_UART_11.0592MHZ
1-3G,1-5J
16-2L
CLK_SYS_33MHZ
CLK_CPLD_33MHZ
1-3G,1-5J
16-2L
C9-1 0.1UF

U1 440EPX
SYSTEM
SYSRESET# SYSCLK YMCLK TESTEN SYSERR THERMONA THERMONB PERROUT
INTERRUPTS
IRQ0 IRQ1 IRQ2 IRQ3 IRQ4_GPIO44_DMAACK1 IRQ5_MDDCTRL_DMAREQ1 IRQ6_GPIO45_EXT1_TC1 IRQ7_GPIO46_DMAREQ0 IRQ8_GPIO47_DMAACK0 IRQ9_GPIO48_EOT0_TC0
PPC440EPX-NTA533T

CLK_TMRCLK
1-2K,1-3E
24-7C
SYSERR
1-3E,1-3G,1-3J
24-8C,25-8H
R24 1K
TEST POINT TP1

IRQ0-9 have programmable polarity per
section 10.5.7 (UIC0_PR) 440ep user
manual

R31 3.3K
R32 2.2K
R33 3.3K
R35 3.3K
GETH0_INT#
1-3M,1-4E
24-8C
GETH1_INT#
1-3E,1-4G,1-4E
17-3F,18-2F
24-8J
PCI_INTA#
1-3M,1-4E
24-7C
STTM_ALERT
1-2N,1-4E
24-7C
GPIO44
1-2E,1-4G
24-7C
SX95T_TDI
1-4G
SX95T_TCK
1-4G
SX95T_TMS
1-3E,1-4G
24-7C
SX95T_TDO
1-3D,1-4E
20-4E
R01 1K
R02 1K
R03 1K
R04 1K
R05 1K
R23 1K
NO POP
RO1 - RO5

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible

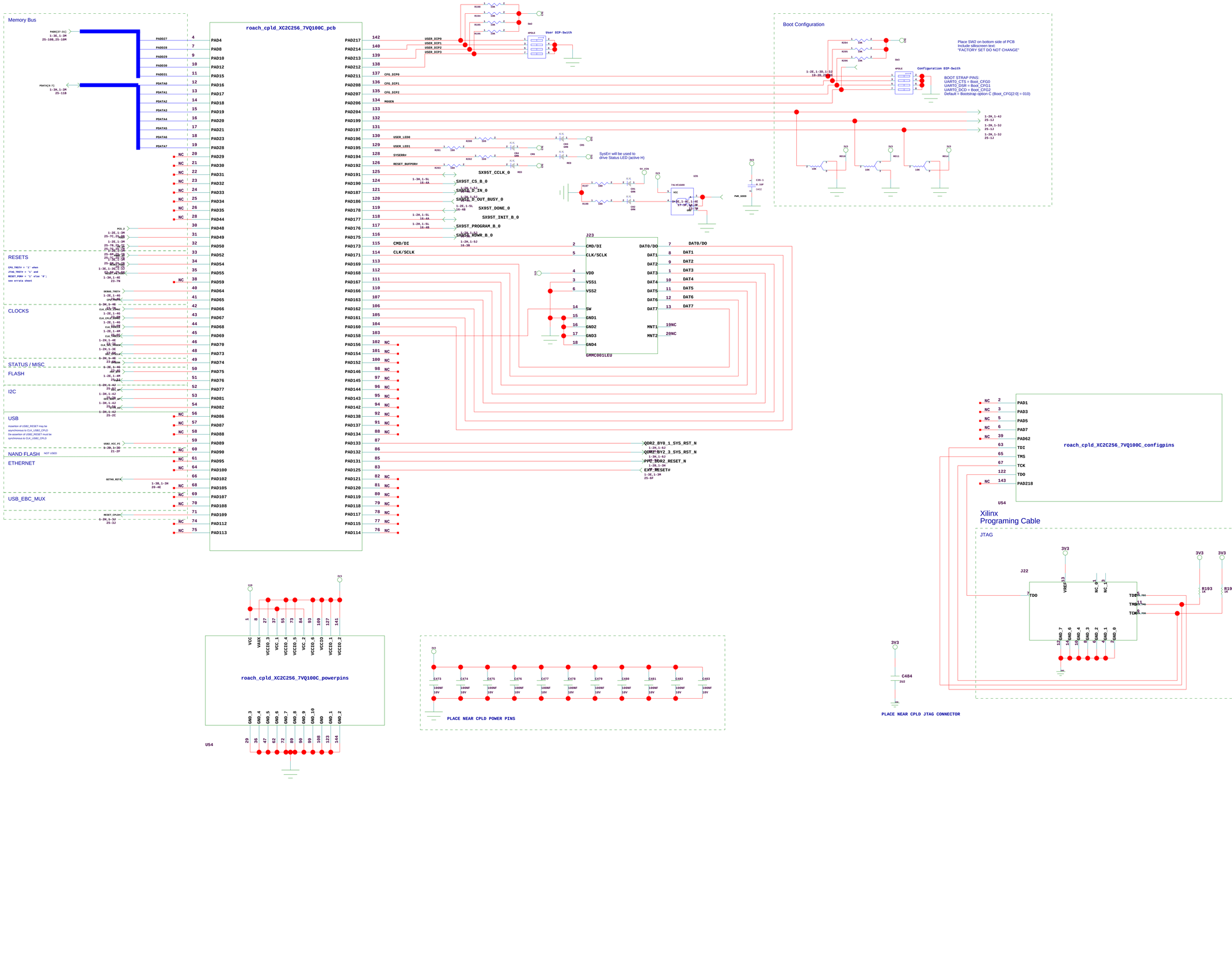
U24 CY27033FXA_8211
C51 18PF
C52 18PF
12.00 MHZ
Y2
XTALIN XTALOUT S0 S1 S2_SUSPMODE OE_SHDWN# GND_3 GND_11 VDD_2 VDD_14 CPUCLK CLKD CLKA CLKB CLKC XBUF
CLK_SEL_M66EN
1-4E,1-5L
16-2L
R34 2.2K
R54 33
R55 33
R56 33
R57 33
R58 33
R59 33
R510 33
R511 33
CLK_PCI1_66/33MHZ
1-3J,1-4G
25-3D
CLK_PCI2_66/33MHZ
1-3B,1-4G
20-4E
CLK_PCI3_66/33MHZ
1-4G
CLK_GETH0_25MHZ
1-3B,1-4G
19-4E
CLK_GETH1_25MHZ
1-3G,1-5J
16-2L
CLK_USB2.0_48MHZ
1-3B,1-4G
19-3C
CLK_CPLD_50MHZ
1-2E,1-4G
24-7C
CLK_USB2.0_12MHZ
1-2D,1-4G
24-7C
C16-1 0.1UF
C18-1 0.1UF

TRACE & JTAG CONNECTORS

P1 .12X H SMT
CPU_TDO
CPU_TDI
CPU_TCK
CPU_TMS
CPU_HALT#
DEBUG_TRST#
R36 10K
VCC_JTAG
R26 33
C53 0.1UF
R26 is for current
limiting and should
be <100 Ohms.
R37 10K
R38 10K
R39 10K
R49 10K

Critical placement and routing
of the Trace connector and nets.
Up to CPU frequency/4

U1 440EPX
PROBEWatch JTAG
TRC_CLK CPU_HALT
TRCES0 TRCES1 TRCES2 TRCES3 TRCES4
TRCTL0 TRCTL1 TRCTL2 TRCTL3 TRCTL4 TRCTL5 TRCTL6
TRCCLK HALT_DRVINH2
TRCBS0_GPIO49 TRCBS1_GPIO50 TRCBS2_GPIO51
TRCES0_GPIO52 TRCES1_GPIO53 TRCES2_GPIO54 TRCES3_GPIO55 TRCES4_GPIO56
TRCTL0_GPIO57 TRCTL1_GPIO58 TRCTL2_GPIO59 TRCTL3_GPIO60 TRCTL4_GPIO61 TRCTL5_GPIO62 TRCTL6_GPIO63
TCK TDO TDI TMS TRST#
CPU_TCK CPU_TDO CPU_TDI CPU_TMS
CPU_TRST#
1-4E,1-4M
25-2B
DEBUG_TRST#
1-4G
3V3
C54 0.1UF
R27 2.2K
R12 R14 R15 R22
CPU_HALT#
CPU_TDO
CPU_TCK
CPU_TMS
CPU_TDI
MCH10 MCH51 MCH52 MCH50 MCH31 MCH32 MCH33
TRACE PORT
J1 25JN F SMT
R18 R11 R13 R16 R17 R18 R19 R20 R21
TRC_CLK
VCC_JTAG
TRCES4
TRCTL0 TRCTL1 TRCTL2 TRCTL3 TRCTL4 TRCTL5 TRCTL6


Memory Bus
roach_cpld_XC2C256_7VQ100C_pcb
RESETS
CLOCKS
STATUS / MISC
FLASH
I2C
USB
NAND FLASH
NOT USED
ETHERNET
USB_EBC_MUX
Boot Configuration
User DIP-Swith
Configuration DIP-Swith
Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"
BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)
SysErr will be used to
drive Status LED (active H)
GMMC001LEU
roach_cpld_XC2C256_7VQ100C_configpins
Xilinx
Programing Cable
JTAG
roach_cpld_XC2C256_7VQ100C_powerpins
PLACE NEAR CPLD POWER PINS
PLACE NEAR CPLD JTAG CONNECTOR
U54

PDATA[0:31]
PADD[2:31]
External Slave Peripheral
External Master Peripheral Interface
FLASH
FWP#
FRY_BY#
EXT_RESET#
CLK_PERCLK
NO POP
PCS_2
POE#
PR_W#
PWBE_0#
3V3
GND
PCS_1
PWBE_1#
PBLAST#
PER_CS0
PER_OE_N
PER_R_W_N
PER_WBE[1]
PER_WBE[0]
PER_B_LAST
PER_D_PAR[1]
PER_D_PAR[0]
PER_ERR
PER_READY
PERERR
PREADY
U15
BANKS=1, 2, 4
CHIP SELECT 1
UART
I2C0
I2C1_SPI
NAND Flash Interface
NOT USED
UART Port 0
UART Port 1
J14
HLE-105-02-G-DV