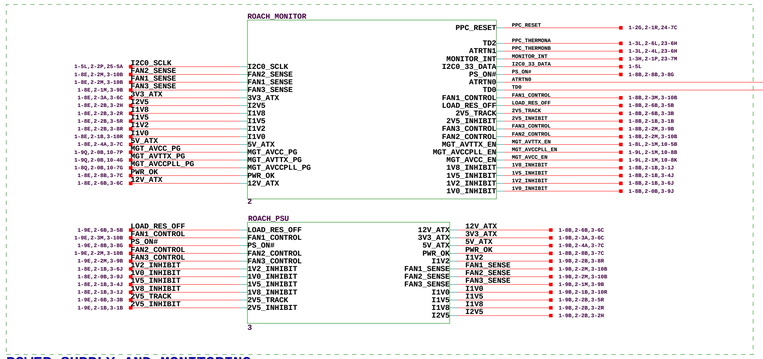
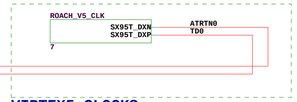
VIRTEX5

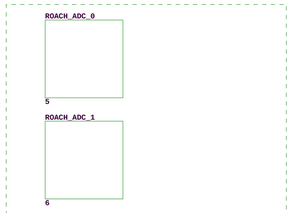
POWER SUPPLY AND MONITORING



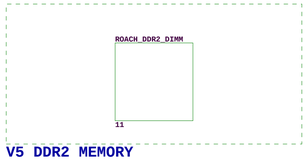
VIRTEX5 CLOCKS



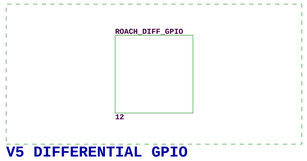
ZDOK/ADC INTERFACE



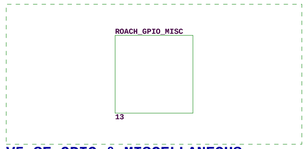
V5 DDR2 MEMORY



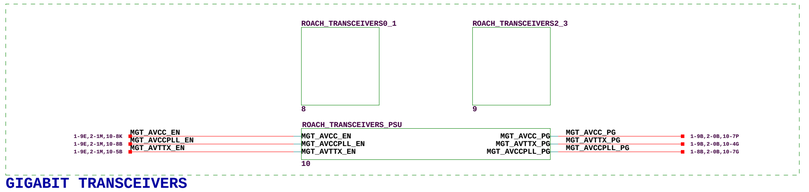
V5 DIFFERENTIAL GPIO



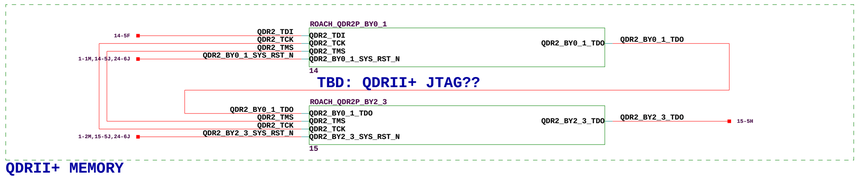
V5 SE GPIO & MISCELLANEOUS



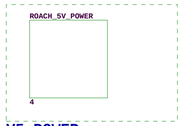
GIGABIT TRANSCEIVERS



QDRII+ MEMORY



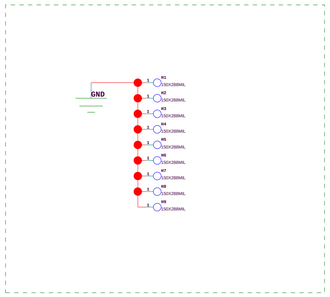
V5 POWER



VIRTEX5 CONFIGURATION

PPC

MECHANICAL



CONTRIBUTORS

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MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2	**ROACH_TOP**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-15-2007_14:28 PATH PATH	DRAWN: F KAPP APPR:
	CHECKED: E BAUERMEISTER SHEET 1 OF 25

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

TIE TO GROUND IF PLL'S ARE NOT USED

PLACE AT ACTEL 3V3 POWER PINS

PLACE AT ACTEL 1V5 POWER PINS

roach_AFS600_powerpins

roach_AFS600_pcb

roach_AFS600_configpins

PB POWER SWITCH

KEY - REMOVE PIN

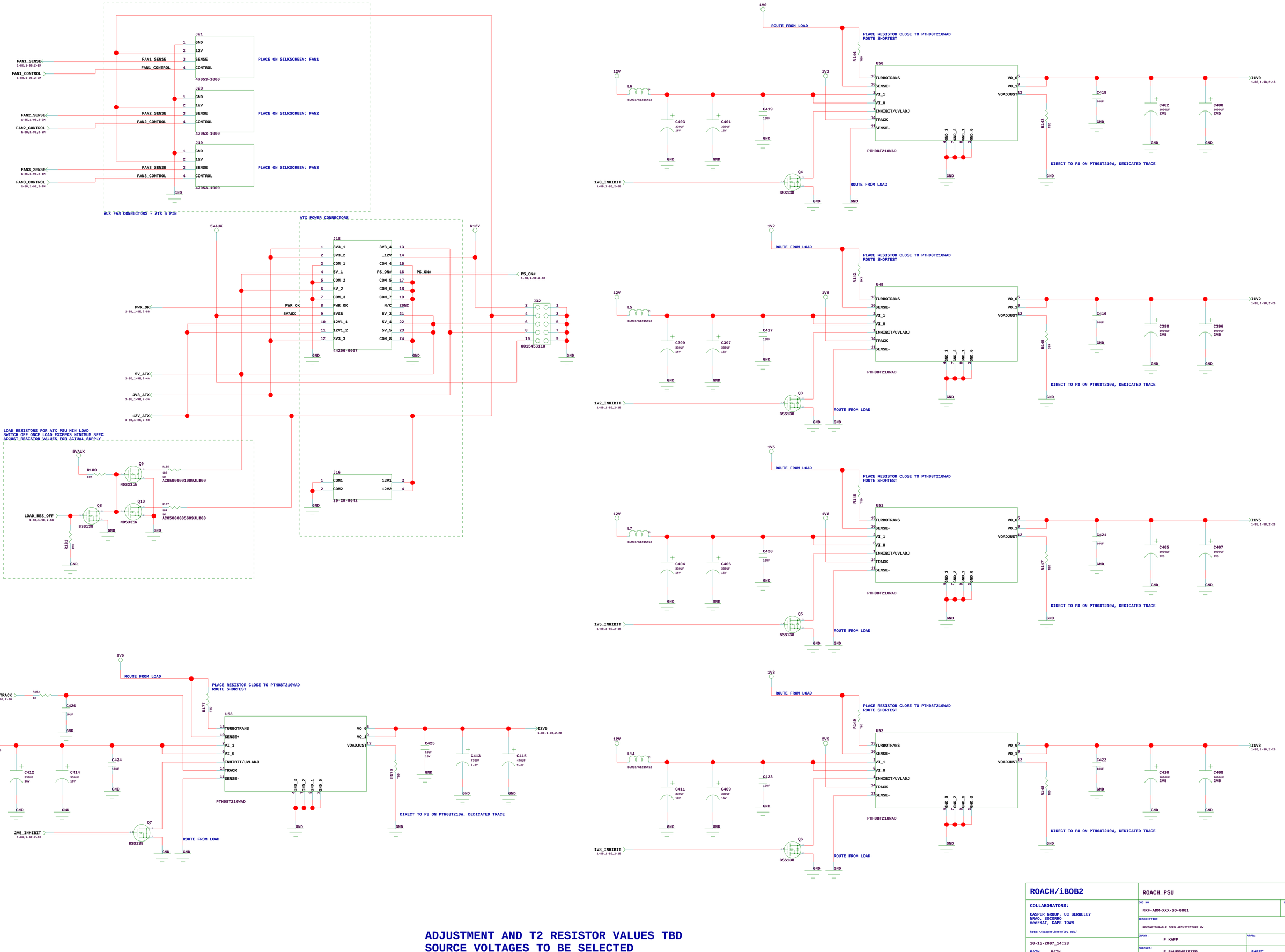
MONITOR RESET

XPORT - PLACE IN REAR I/O REGION

TEMPERATURE DIODE HEADER

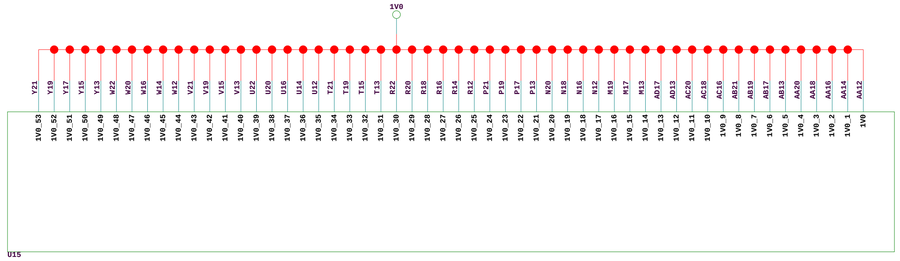
ACTEL JTAG CONNECTOR

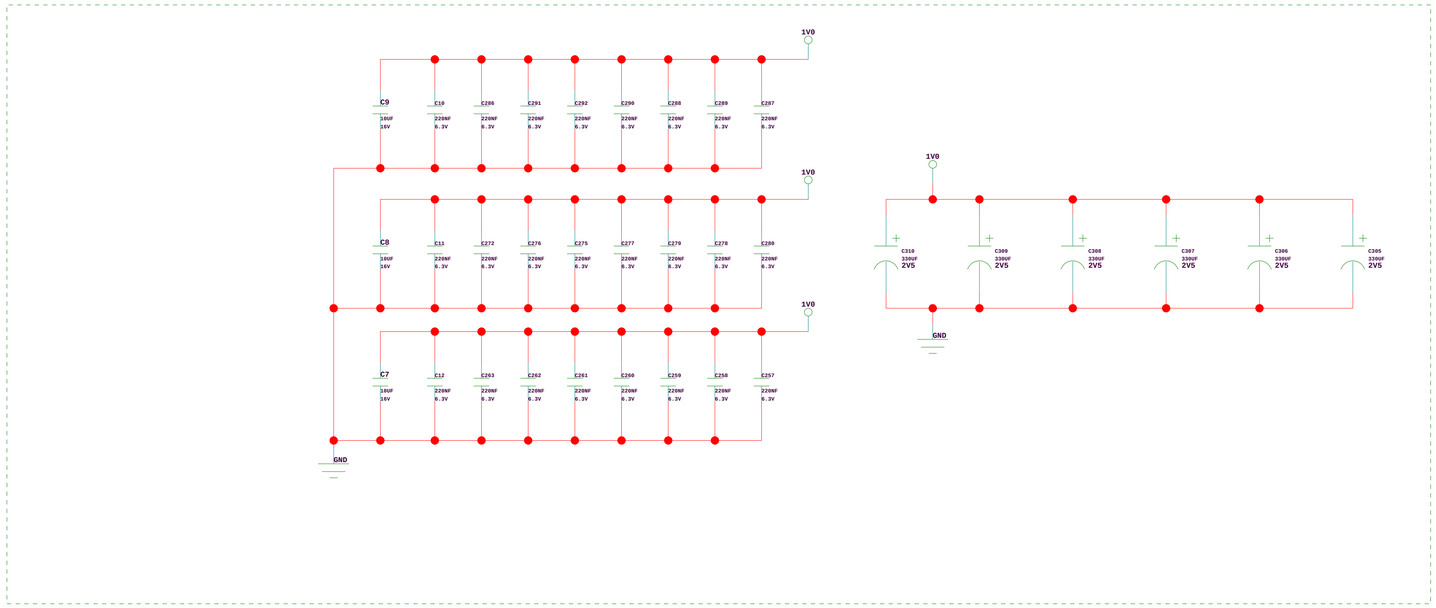
ROACH/iBOB2	ROACH_MONITOR
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-15-2007_14:28	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 2 OF 25

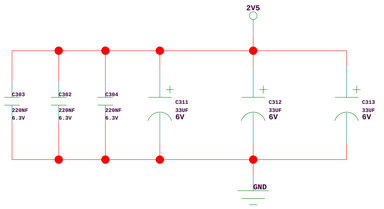


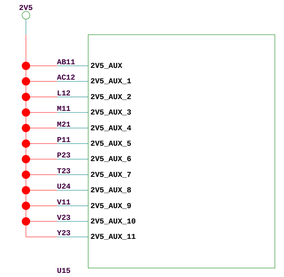
ADJUSTMENT AND T2 RESISTOR VALUES TBD
SOURCE VOLTAGES TO BE SELECTED

ROACH/iBOB2	**ROACH_PSU**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE RW
10-15-2007_14:28	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 3 OF 25









ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
10-15-2007_14:28 PATH PATH	

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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10-15-2007_14:28

PATH PATH

ROACH_ADC_0

DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 5 OF 25

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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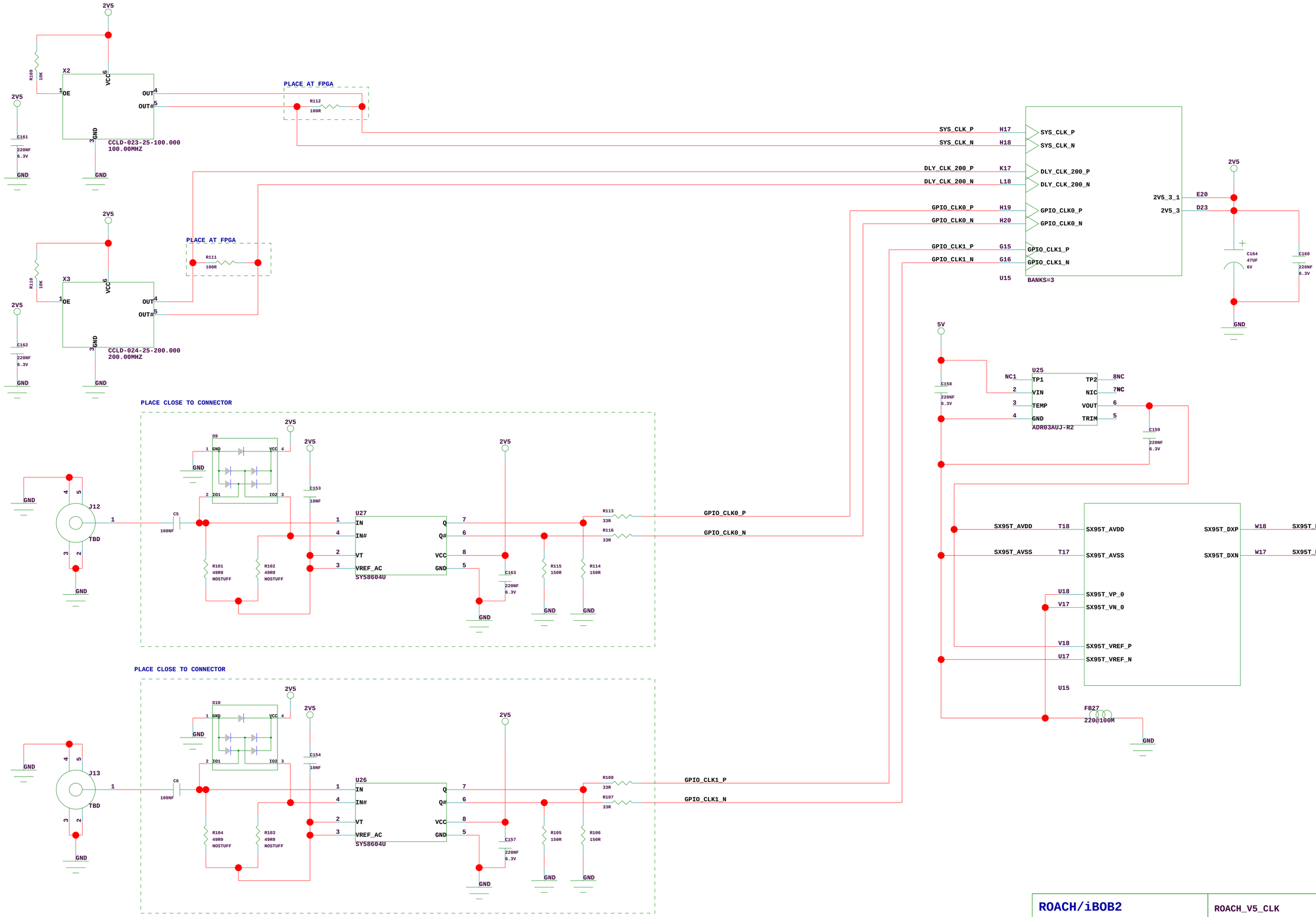
10-15-2007_14:28

PATH PATH

ROACH_ADC_1

DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 6 OF 25



ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

10-15-2007_14:28

PATH PATH

ROACH_V5_CLK

DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 7 OF 25

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB3 220@100M
FB4 220@100M
C94 220NF 6.3V
C93 220NF 6.3V
C92 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_112 R3 MGTAVCC_112
R4 MGTAVCC_112_1
MGTAVCCPLL_112 T3 MGTAVCCPLL_112
MGTAVTTRX_112 N3 MGTAVTTRX_112
MGT_112_REF_CLK_P P4 MGT_112_REF_CLK_P
MGT_112_REF_CLK_N P3 MGT_112_REF_CLK_N
MGTRX0_112_P N1 MGTRX0_112_P
MGTRX0_112_N P1 MGTRX0_112_N
MGTRX1_112_P T1 MGTRX1_112_P
MGTRX1_112_N R1 MGTRX1_112_N
U15
MGTRREF V4 MGTRREF
MGT_VTRXC V5 MGTAVTTRXC
R56 49.9R
MGTAVTTTX_112 M3 MGTAVTTTX_112
MGTAVTTTX_112_1 U3
MGTTX0_112_P M2 MGTTX0_112_P
MGTTX0_112_N N2 MGTTX0_112_N
MGTTX1_112_P U2 MGTTX1_112_P
MGTTX1_112_N T2 MGTTX1_112_N
MGT_AVTT
FB25 220@100M
FB5 220@100M
C126 220NF 6.3V
C96 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
2V5
FB26 220@100M
C137 220NF 6.3V
R84 10K
X1
CCLD-023-25-156.250
156.25MHZ
JP6
OE
VCC
OUT
GND
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
C104 10NF 25V
C105 10NF 25V
C106 10NF 25V
C107 10NF 25V
C109 10NF 25V
C108 10NF 25V
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB11 220@100M
FB9 220@100M
FB10 220@100M
C102 220NF 6.3V
C101 220NF 6.3V
C100 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_114 AA3 MGTAVCC_114
AA4 MGTAVCC_114_1
MGTAVCCPLL_114 AB3 MGTAVCCPLL_114
MGTAVTTRX_114 W3 MGTAVTTRX_114
MGT_114_REF_CLK_P NC Y4 MGT_114_REF_CLK_P
MGT_114_REF_CLK_N NC Y3 MGT_114_REF_CLK_N
MGTRX0_114_P W1 MGTRX0_114_P
MGTRX0_114_N Y1 MGTRX0_114_N
MGTRX1_114_P AB1 MGTRX1_114_P
MGTRX1_114_N AA1 MGTRX1_114_N
U15
C140 10NF 25V
C141 10NF 25V
C142 10NF 25V
C143 10NF 25V
MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT
MGTAVTTTX_114 AC3 MGTAVTTTX_114
MGTAVTTTX_114_1 V3
MGTTX0_114_P V2 MGTTX0_114_P
MGTTX0_114_N W2 MGTTX0_114_N
MGTTX1_114_P AC2 MGTTX1_114_P
MGTTX1_114_N AB2 MGTTX1_114_N
MGT_AVTT
FB8 220@100M
C99 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB17 220@100M
FB15 220@100M
FB16 220@100M
C119 220NF 6.3V
C118 220NF 6.3V
C115 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_116 J3 MGTAVCC_116
J4 MGTAVCC_116_1
MGTAVCCPLL_116 K3 MGTAVCCPLL_116
MGTAVTTRX_116 G3 MGTAVTTRX_116
MGT_116_REF_CLK_P NC H4 MGT_116_REF_CLK_P
MGT_116_REF_CLK_N NC H3 MGT_116_REF_CLK_N
MGTRX0_116_P G1 MGTRX0_116_P
MGTRX0_116_N H1 MGTRX0_116_N
MGTRX1_116_P K1 MGTRX1_116_P
MGTRX1_116_N J1 MGTRX1_116_N
U15
C110 10NF 25V
C111 10NF 25V
C112 10NF 25V
C113 10NF 25V
MGTAVTTTX_116_1 L3
MGTAVTTTX_116 F3 MGTAVTTTX_116
MGTTX0_116_P F2 MGTTX0_116_P
MGTTX0_116_N G2 MGTTX0_116_N
MGTTX1_116_P L2 MGTTX1_116_P
MGTTX1_116_N K2 MGTTX1_116_N
MGT_AVTT
FB14 220@100M
C116 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB22 220@100M
FB24 220@100M
FB23 220@100M
C123 220NF 6.3V
C114 220NF 6.3V
C125 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_118 AG3 MGTAVCC_118
AG4 MGTAVCC_118_1
MGTAVCCPLL_118 AH3 MGTAVCCPLL_118
MGTAVTTRX_118 AE3 MGTAVTTRX_118
MGT_118_REF_CLK_P NC AF4 MGT_118_REF_CLK_P
MGT_118_REF_CLK_N NC AF3 MGT_118_REF_CLK_N
MGTRX0_118_P AE1 MGTRX0_118_P
MGTRX0_118_N AF1 MGTRX0_118_N
MGTRX1_118_P AH1 MGTRX1_118_P
MGTRX1_118_N AG1 MGTRX1_118_N
U15
C144 10NF 25V
C145 10NF 25V
C146 10NF 25V
C147 10NF 25V
MGTAVTTTX_118_1 AJ3
MGTAVTTTX_118 AD3 MGTAVTTTX_118
MGTTX0_118_P AD2 MGTTX0_118_P
MGTTX0_118_N AE2 MGTTX0_118_N
MGTTX1_118_P AJ2 MGTTX1_118_P
MGTTX1_118_N AH2 MGTTX1_118_N
MGT_AVTT
FB19 220@100M
C121 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
P3
FCN-268F036-G/3DB
S1 DL0P
S2 DL0N
S3 DL1P
S4 DL1N
S5 DL2P
S6 DL2N
S7 DL3P
S8 DL3N
S16 SL0P
S15 SL0N
S14 SL1P
S13 SL1N
S12 SL2P
S11 SL2N
S10 SL3P
S9 SL3N
SIG_GND1 G1
SIG_GND2 G2
SIG_GND3 G3
SIG_GND4 G4
SIG_GND5 G5
SIG_GND6 G6
SIG_GND7 G7
SIG_GND8 G8
SIG_GND9 G9
SIG_GND10 G19
G4 AND G8 CONNECTED IN 2X2 MODULE
ODIS0
FAULT0
JP4
R88 10K
C130 10NF
C131 10NF
3V3
R79 150R
D2
OPTICAL MODULE FAULT - RED LED
R97 5K1
RS7 3K9
R59 6K8
RS8 3K9
U21 MAX9032AKA
U20 MAX9032AKA
C127 10NF
U22 AND2 SN74AHC1G08DCKR
U18 TPS2031D
R99 10K
C129 10NF
C128 100NF
C138 4.7UF 16V
C90 22UF
P3
FCN-268F036-G/3DB
S19 DL0P
S20 DL0N
S21 DL1P
S22 DL1N
S23 DL2P
S24 DL2N
S25 DL3P
S26 DL3N
S34 SL0P
S33 SL0N
S32 SL1P
S31 SL1N
S30 SL2P
S29 SL2N
S28 SL3P
S27 SL3N
SIG_GND1 G10
SIG_GND2 G11
SIG_GND3 G12
SIG_GND4 G13
SIG_GND5 G14
SIG_GND6 G15
SIG_GND7 G16
SIG_GND8 G17
SIG_GND9 G18
SIG_GND10 G19
G4 AND G8 CONNECTED IN 2X2 MODULE
ODIS1
FAULT1
JP5
R89 10K
C134 10NF
C132 10NF
3V3
R79 150R
D3
OPTICAL MODULE FAULT - RED LED
R98 5K1
R93 3K9
R94 6K8
R95 3K9
U23 AND2 SN74AHC1G08DCKR
U19 TPS2031D
R100 10K
C135 10NF
C136 100NF
C139 4.7UF 16V
C91 22UF
C133 10NF
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
10-15-2007_14:28
PATH PATH
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DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 8 OF 25

ROACH/iBOB2

ROACH_TRANSCEIVERS2_3

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

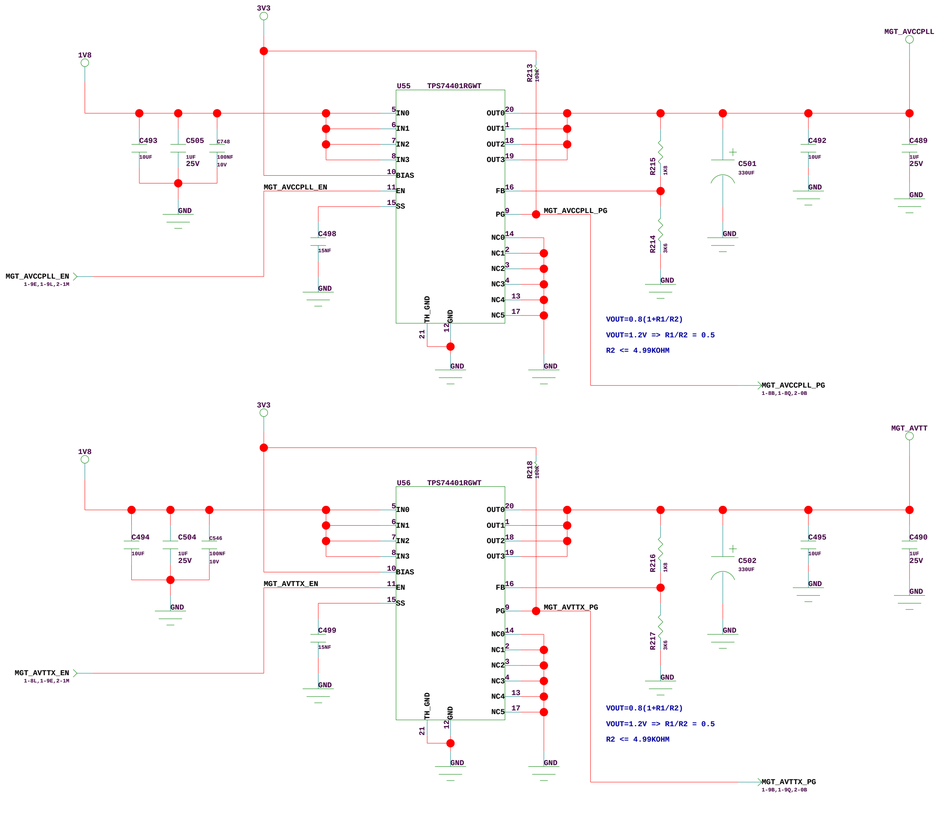
APPR:

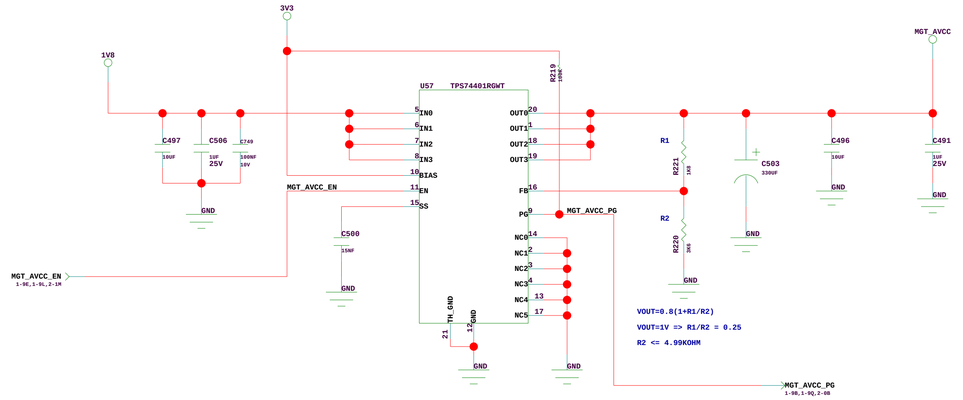
CHECKED: E BAUERMEISTER

10-15-2007_14:28

PATH PATH

SHEET 9 OF 25





ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

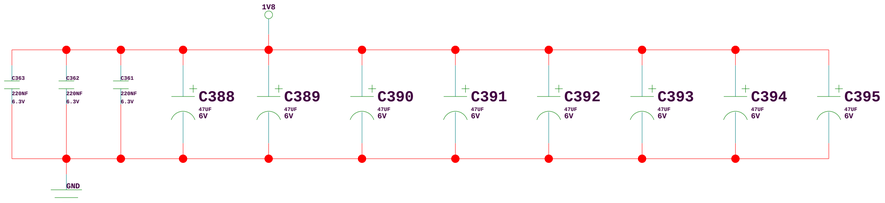
http://casper.berkeley.edu/

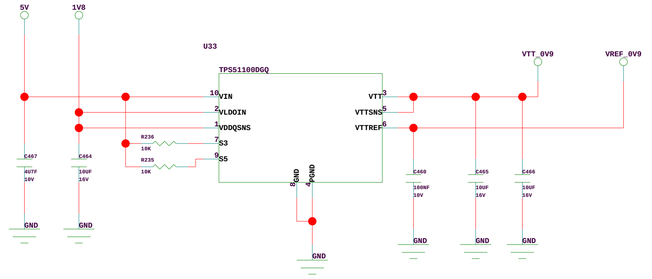
10-15-2007_14:28

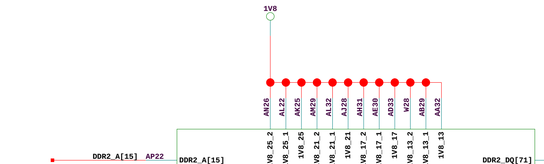
PATH PATH

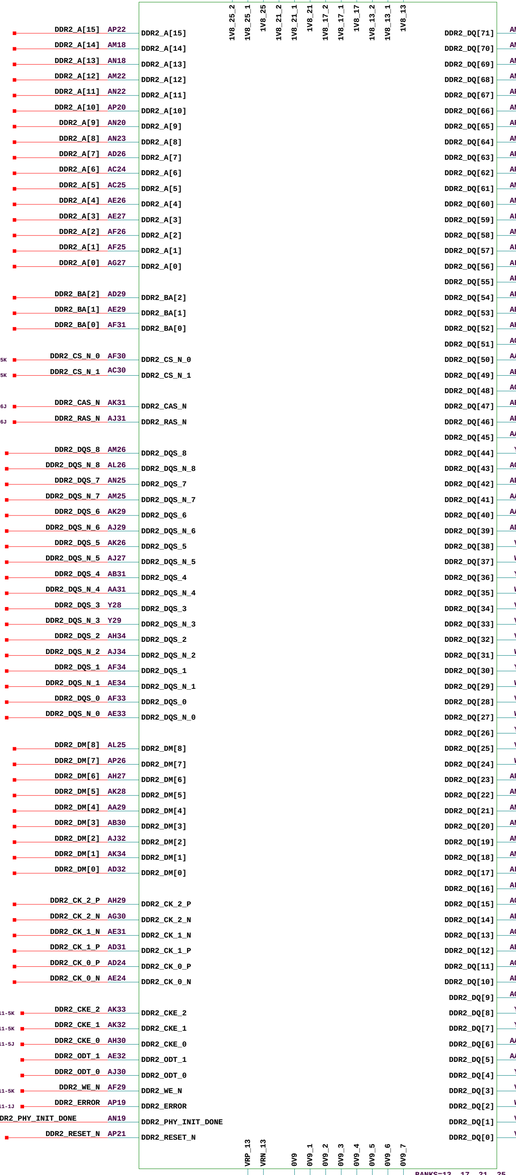
ROACH_TRANSCEIVERS_PSU

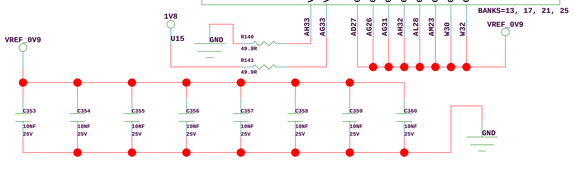
DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 10 OF 25

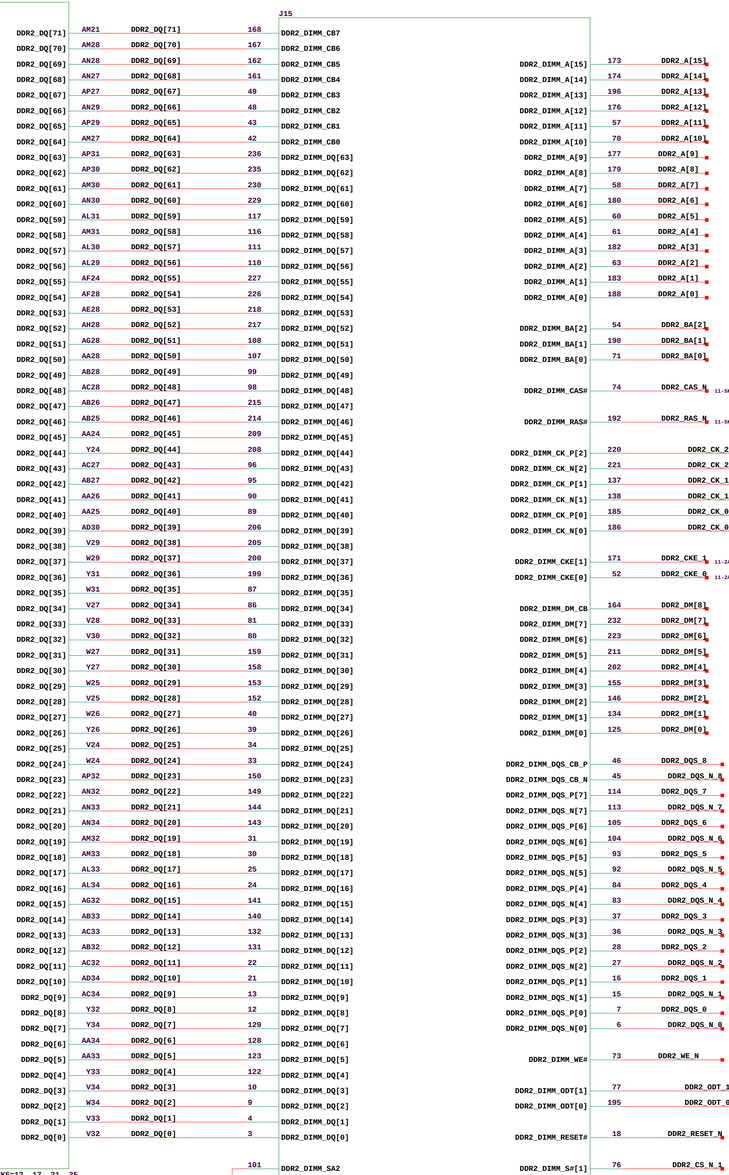


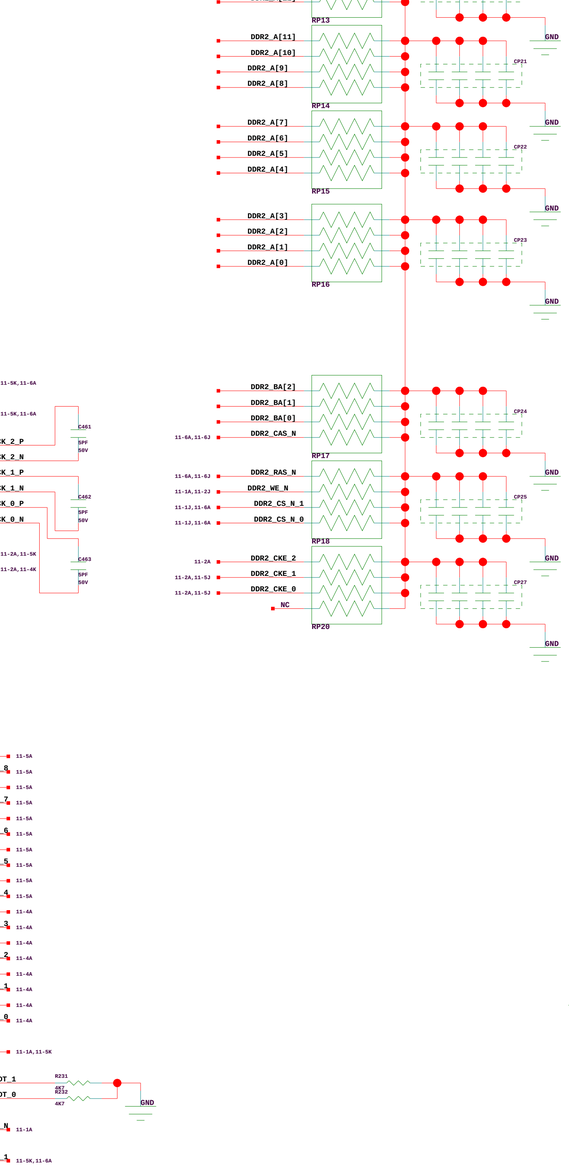




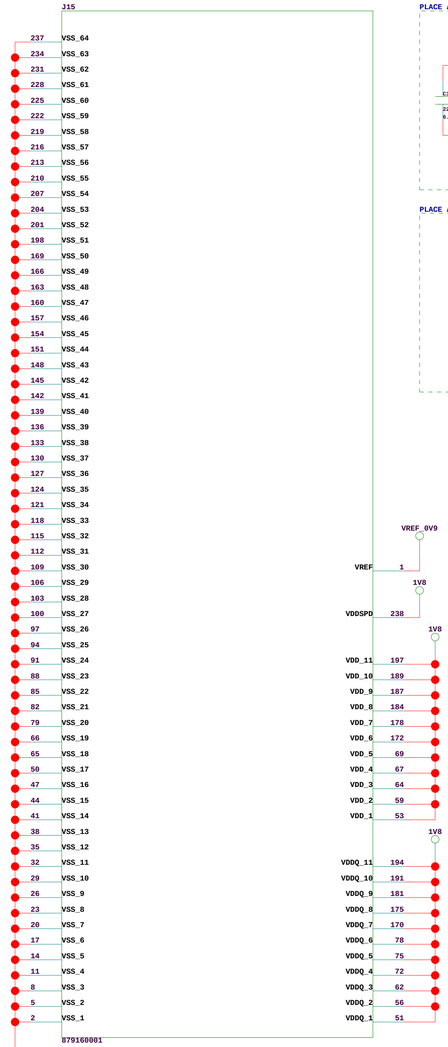


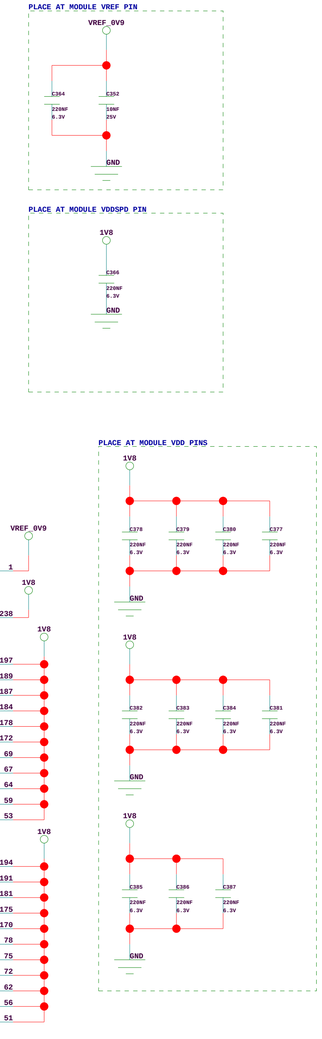


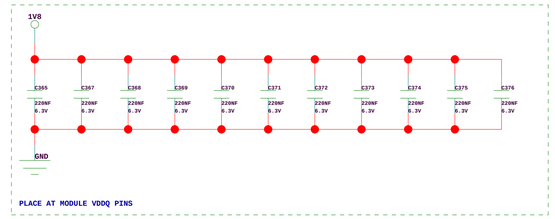




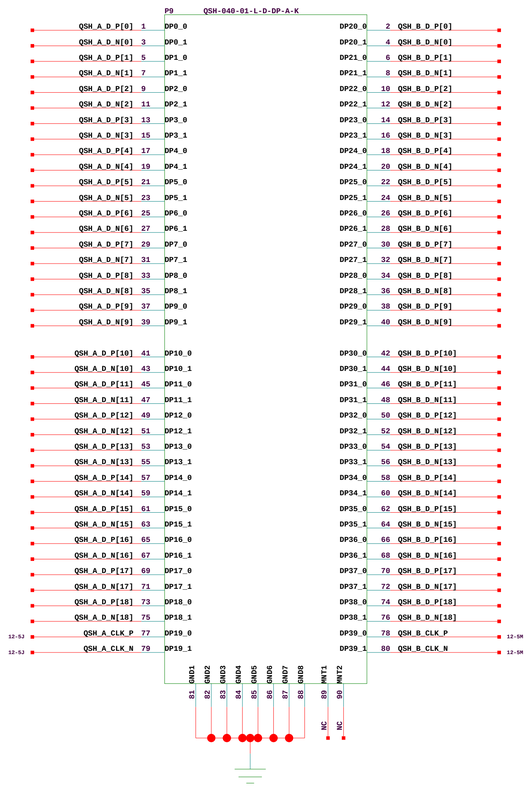
VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

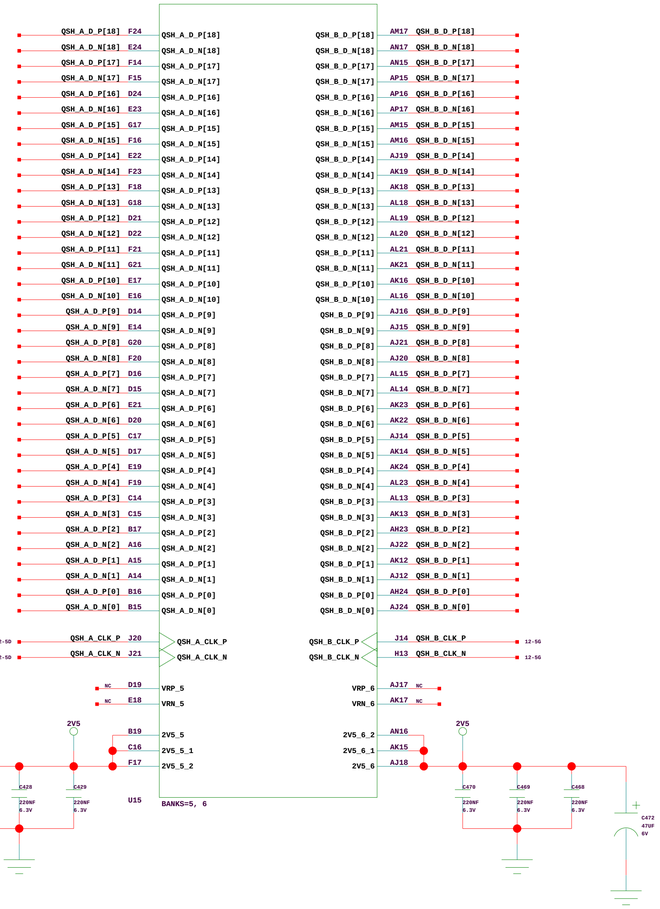






ROACH/iBOB2	ROACH_DDR2_DIMM
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-15-2007_14:28 PATH PATH	DRAWN: F KAPP APPR:
	CHECKED: E BAUERMEISTER SHEET 11 OF 25





ROACH/iBOB2	**ROACH_DIFF_GPIO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-15-2007_14:28 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 12 OF 25

GPIOLVC18[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

GPIOLVC18[20] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

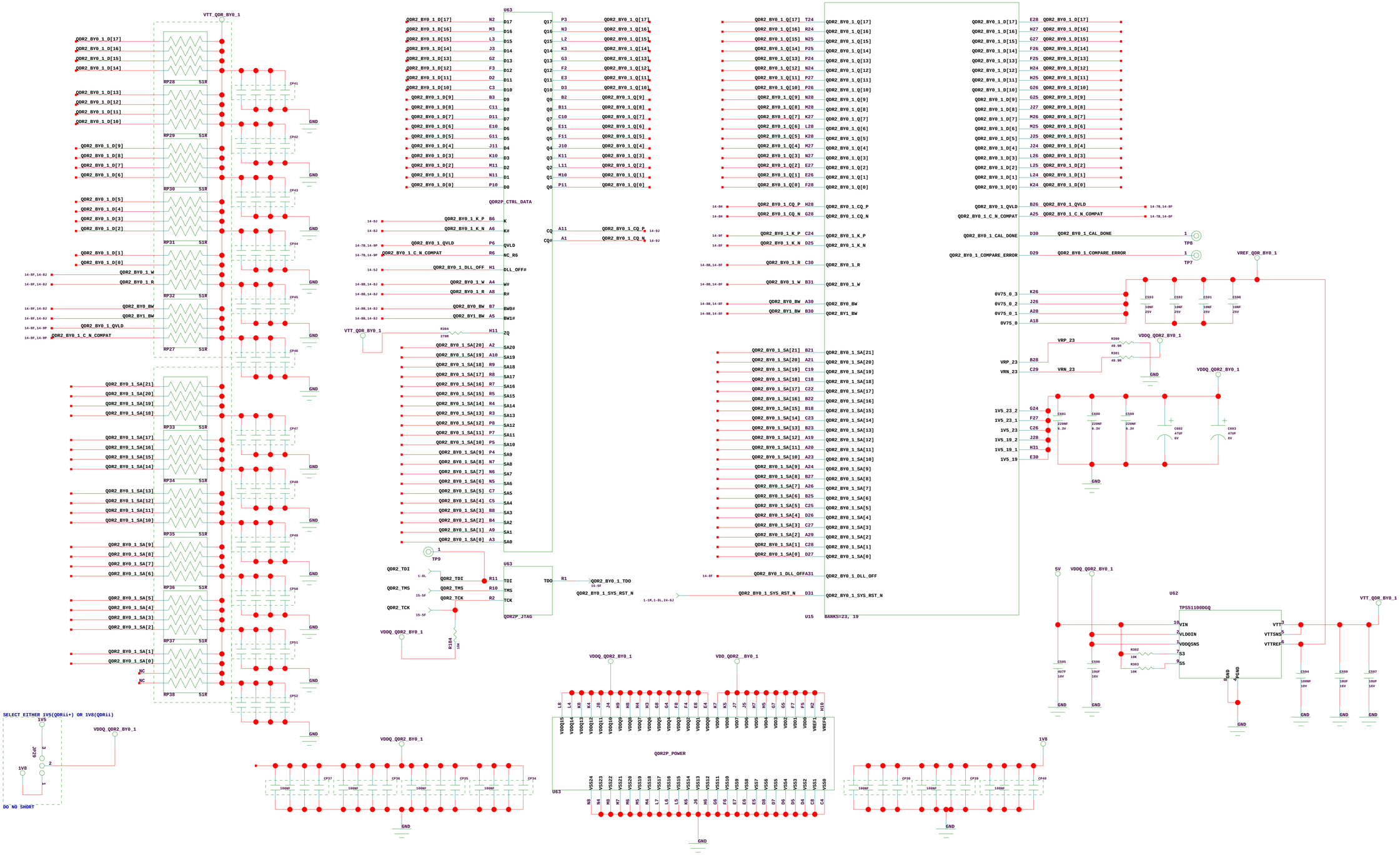
IO VOLTAGE LEVEL SELECT

1-2: 3.3V
2-3: 2.5V

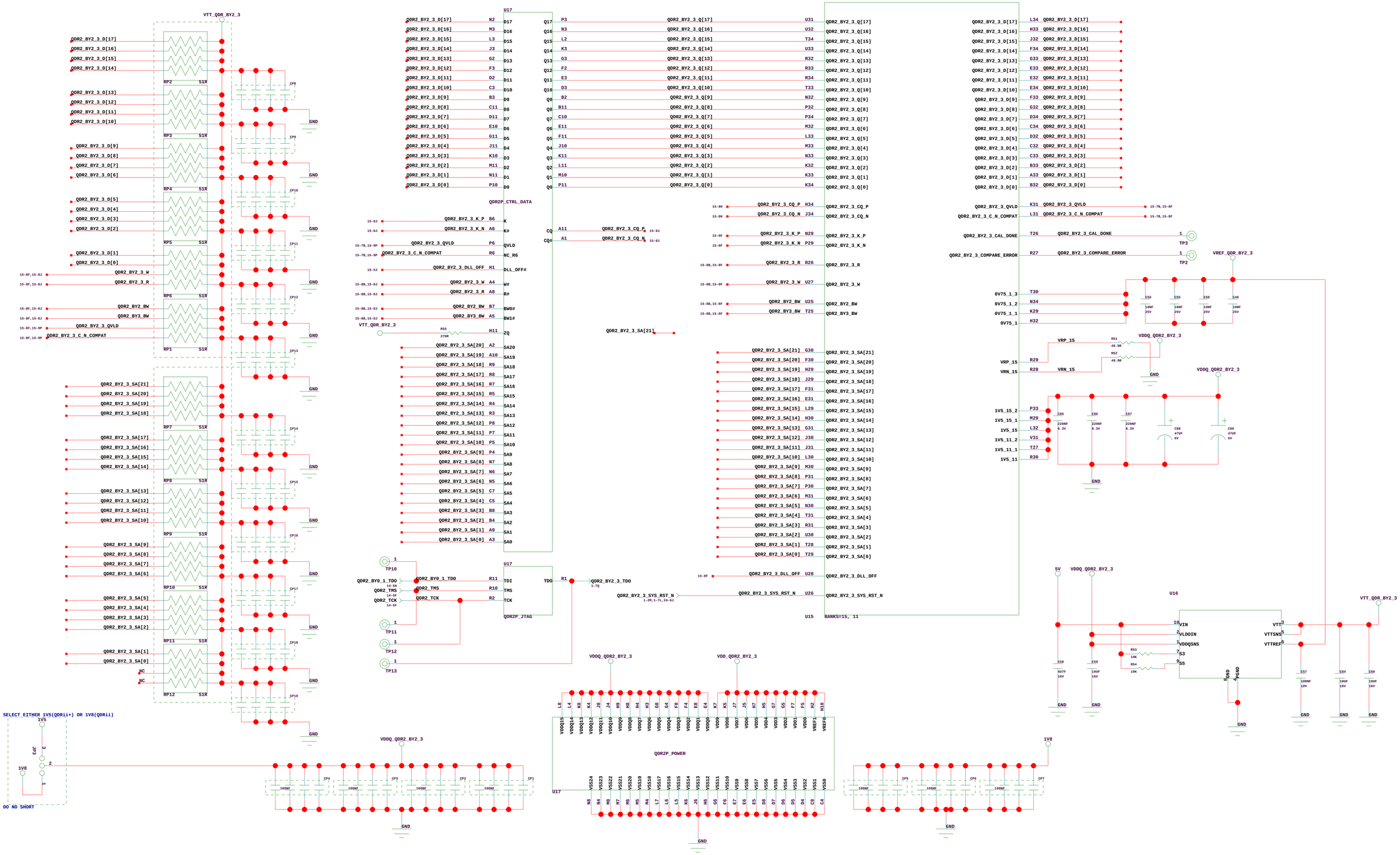
GPIOLVC18[4] IS DUAL FUNCTION:
1. DRIVES LED
2. CONTROLS DIRECTION ON GPIOLVC33[1-4]

IF CR10 IS ON, CLOCK CAPABLE GPIO'S ARE OUTPUTS

ROACH/iBOB2	ROACH_GPIO_MISC	
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW	
10-15-2007_14:28 PATH PATH	DRAWN: F KAPP	APPR:
	CHECKED: E BAUERMEISTER	SHEET 13 OF 25



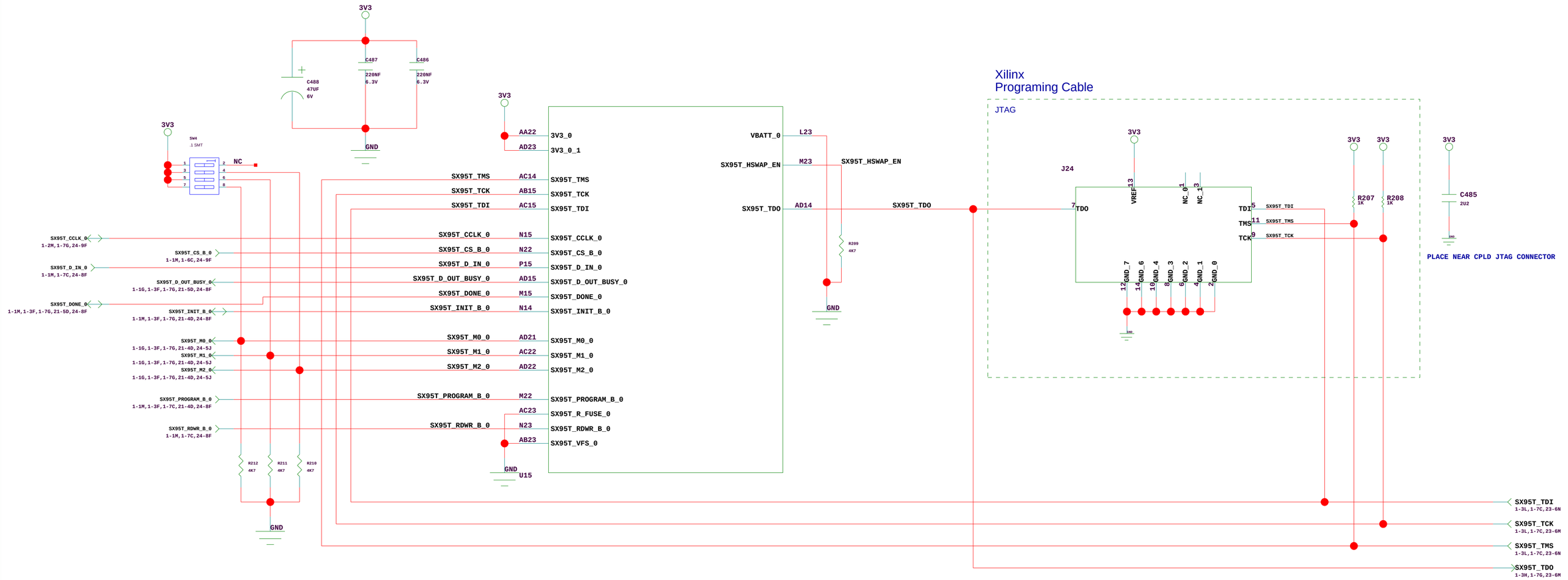
ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 14 OF 25
10-15-2007_14:28 PATH PATH	



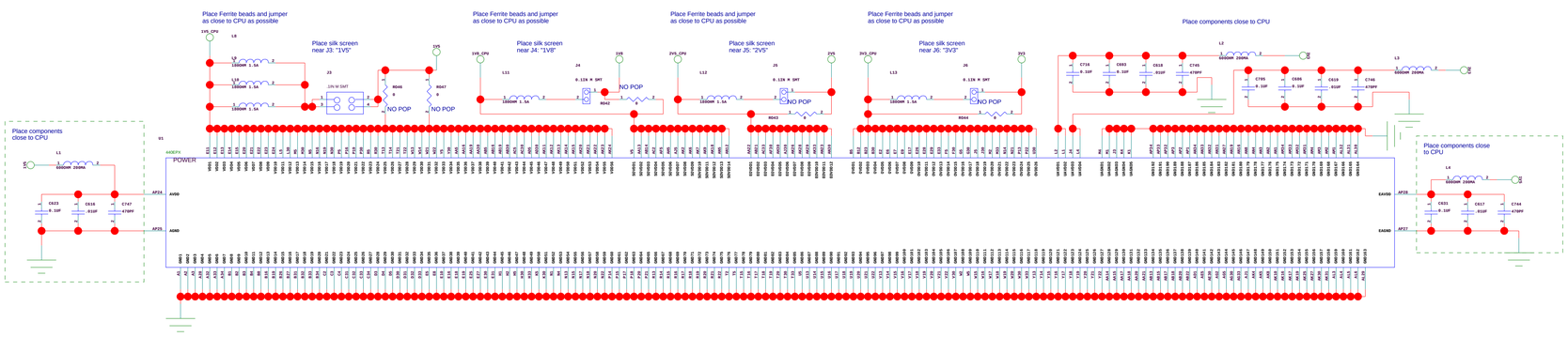
ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET: 15 OF 25
10-15-2007_14:28 PATH PATH	

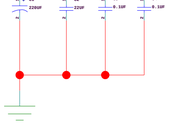
TBD

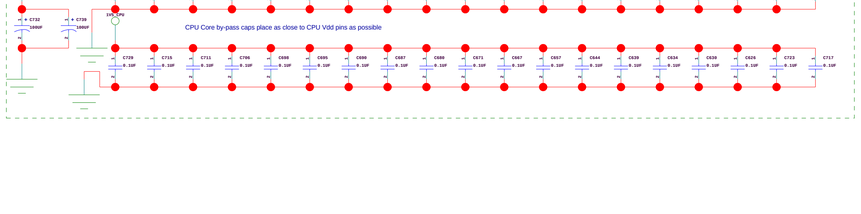
VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

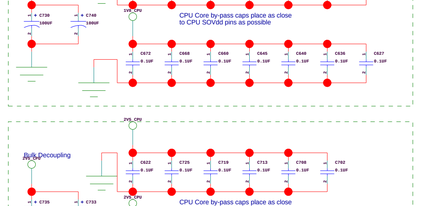


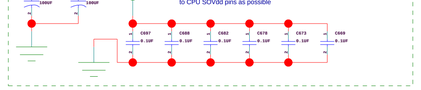
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
10-15-2007_14:28 PATH PATH	

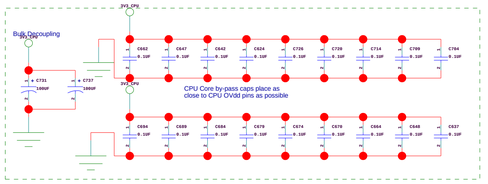




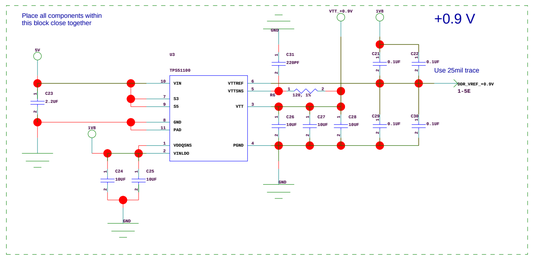


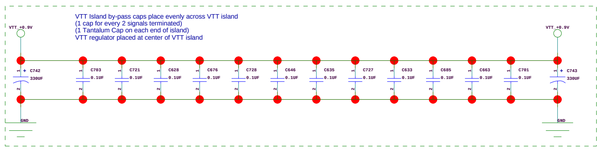


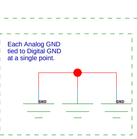




REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

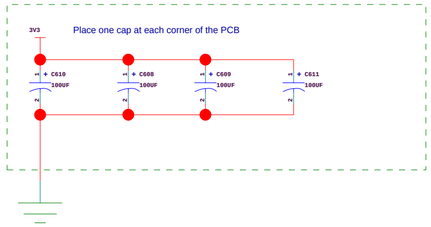






ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 17 OF 25
10-15-2007_14:28 PATH PATH	

REMOVED 3V3 GENERATION



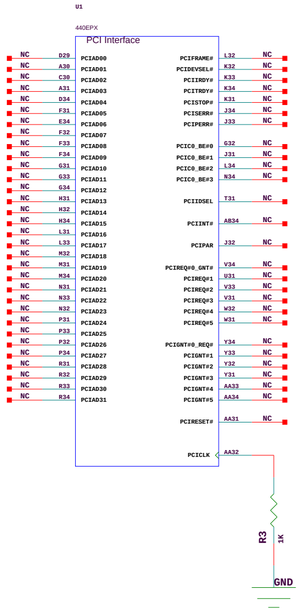
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET: 18 OF 25
10-15-2007_14:28 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-15-2007_14:28 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

Place nearest PHY pin 96
Place nearest PHY pin 101
Place nearest PHY pin 98
Place nearest PHY pin 100
Place as close to PHY CORE VDD power pins as possible
Place as close to PHY IO VDD power pins as possible
UNUSED SECOND ETHERNET MAC
Gig-Ethernet RGMII1
Gig-Ethernet RGMII0
ETHERNET Mgt.
Place resistors as close to CPU as possible and keep all traces lengths equal
Place resistors close to PHY all trace lengths equal
Place components as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible.
Place decoupling C close to termination R
All traces 50Ohm ref GND or 2V5
Ethernet LEDs
Top LED = SPEED/LINK
Green = 1000
Yellow = 10/100
Off = 10/100
Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY
HFJ11-1G02E-L12
CHASSIS_GND
The RGMII signaling is 125 MHz using both rising and falling edges of the clock.
The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.
Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.
CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30
Place jumers in line with signals
DP83865DVH
NOSTUFF
DUPLEX LED
L10 LED
L100 LED
STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL
ROACH/iBOB2
ROACH_PPC_ETH1
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
CHECKED: E BAUERMEISTER
10-15-2007_14:28
PATH PATH
SHEET 20 OF 25

U1

USB 2.0 DEVICE

440EPX

USB2CLK — A5 — NC

GPIO28/USB2TXVAL — C6 — NC
USB2TXRDY_REFEN — B6 — NC
USB2RXACT_HOLDREQ_RCVINH — D7 — NC
USB2RXVAL_LEAKTEST2 — C8 — NC
GPIO27/USB2RXERR_EXTREQ# — A4 — SX95T_DONE_0 <> SX95T_DONE_0
1-1M,1-3F,1-7G,24-8F

GPIO30/USB2XCVRSEL_EXTACK# — M3 — SX95T_INIT_B_0 <> SX95T_INIT_B_0
GPIO31/USB2TERMSEL_BUSREQ — P4
1-1M,1-3F,1-7G,24-8F

USB2LS0_DRVINH1 — R2 — NC — SX95T_M0_0 — SX95T_M0_0
USB2LS1_LEAKTEST_HOLDPRI — P1 — NC
1-1G,1-3F,1-7G,16-3B,24-5J

GPIO32/USB2OM0 — R3 — SX95T_M1_0 — SX95T_M1_0
GPIO33/USB2OM1 — R4
1-1G,1-3F,1-7G,16-3B,24-5J

GPIO29/USB2SUSP_HOLDACK — C5 — SX95T_M2_0 — SX95T_M2_0
1-1G,1-3F,1-7G,16-3B,24-5J

SX95T_PROGRAM_B_0 — SX95T_PROGRAM_B_0
1-1M,1-3F,1-7C,16-3B,24-8F

NOTE:

USB HOST ONLY

USB 2.0 PHY
HOST/DEVICE

USB2XCVR — J2 — USB2_XCVR_D+
USB2XCVR# — J1 — USB2_XCVR_D-
USB2REXT — L3 — R182 3.40K, 1% — CHASSIS_GND
USB2XTAL — N2
USB2XTAL# — N3
CLK_USB2.0_48MHZ
1-3B,1-3L,23-4G

CRITICAL PLACEMENT

Place SP2 very close to P6

SP2 — PGB102ST23WR — SP2

5V — PTC1 1206L050 500MA — C614 220UF 10V — C612 100NF 10V — C613 1NF 50V

VR4 5.5V 20A — VR3 5.5V 20A

P6
1X4 USBA
1 VCC
2 D-
3 D+
4 GND
5
6
292303-1

CHASSIS_GND

ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25
10-15-2007_14:28 PATH PATH	

DDR_PA[15:0]

DDR_PD0[63:0]

U1

DDR SDRAM

64DEPX

DDR_PD0	MEMDATA00	MEMADDR00	DDR_PA0
DDR_PD1	MEMDATA01	MEMADDR01	DDR_PA1
DDR_PD2	MEMDATA02	MEMADDR02	DDR_PA2
DDR_PD3	MEMDATA03	MEMADDR03	DDR_PA3
DDR_PD4	MEMDATA04	MEMADDR04	DDR_PA4
DDR_PD5	MEMDATA05	MEMADDR05	DDR_PA5
DDR_PD6	MEMDATA06	MEMADDR06	DDR_PA6
DDR_PD7	MEMDATA07	MEMADDR07	DDR_PA7
DDR_PD8	MEMDATA08	MEMADDR08	DDR_PA8
DDR_PD9	MEMDATA09	MEMADDR09	DDR_PA9
DDR_PD10	MEMDATA10	MEMADDR10	DDR_PA10
DDR_PD11	MEMDATA11	MEMADDR11	DDR_PA11
DDR_PD12	MEMDATA12	MEMADDR12	DDR_PA12
DDR_PD13	MEMDATA13	MEMADDR13	DDR_PA13
DDR_PD14	MEMDATA14		
DDR_PD15	MEMDATA15	BA0	DDR_PBA0
DDR_PD16	MEMDATA16	BA1	DDR_PBA1
DDR_PD17	MEMDATA17	BA2	DDR_PBA2
DDR_PD18	MEMDATA18		
DDR_PD19	MEMDATA19	RAS#	DDR_PRAS#
DDR_PD20	MEMDATA20	CAS#	DDR_PCAS#
DDR_PD21	MEMDATA21	WE#	DDR_PWE#
DDR_PD22	MEMDATA22		
DDR_PD23	MEMDATA23	DM0	DDR_PDM0
DDR_PD24	MEMDATA24	DM1	DDR_PDM1
DDR_PD25	MEMDATA25	DM2	DDR_PDM2
DDR_PD26	MEMDATA26	DM3	DDR_PDM3
DDR_PD27	MEMDATA27	DM4	DDR_PDM4
DDR_PD28	MEMDATA28	DM5	DDR_PDM5
DDR_PD29	MEMDATA29	DM6	DDR_PDM6
DDR_PD30	MEMDATA30	DM7	DDR_PDM7
DDR_PD31	MEMDATA31	DM8	DDR_PDM8
DDR_PD32	MEMDATA32		
DDR_PD33	MEMDATA33	DQS0	DDR_PDQS0
DDR_PD34	MEMDATA34	DQS1	DDR_PDQS1
DDR_PD35	MEMDATA35	DQS2	DDR_PDQS2
DDR_PD36	MEMDATA36	DQS3	DDR_PDQS3
DDR_PD37	MEMDATA37	DQS4	DDR_PDQS4
DDR_PD38	MEMDATA38	DQS5	DDR_PDQS5
DDR_PD39	MEMDATA39	DQS6	DDR_PDQS6
DDR_PD40	MEMDATA40	DQS7	DDR_PDQS7
DDR_PD41	MEMDATA41	DQS8	DDR_PDQS8
DDR_PD42	MEMDATA42		
DDR_PD43	MEMDATA43	MEMDT0	DDR_PODT0
DDR_PD44	MEMDATA44	MEMDT1	DDR_PODT1
DDR_PD45	MEMDATA45		
DDR_PD46	MEMDATA46	BANKSEL#0	DDR_PCS0#
DDR_PD47	MEMDATA47	BANKSEL#1	DDR_PCS1#
DDR_PD48	MEMDATA48		
DDR_PD49	MEMDATA49	MEMCLKEN	DDR_PCKE
DDR_PD50	MEMDATA50		
DDR_PD51	MEMDATA51	MEMCLKOUT	DDR_CLKOUT
DDR_PD52	MEMDATA52		
DDR_PD53	MEMDATA53	MEMCLKOUT#	DDR_CLKOUT#
DDR_PD54	MEMDATA54		
DDR_PD55	MEMDATA55		
DDR_PD56	MEMDATA56		
DDR_PD57	MEMDATA57		
DDR_PD58	MEMDATA58		
DDR_PD59	MEMDATA59		
DDR_PD60	MEMDATA60		
DDR_PD61	MEMDATA61		
DDR_PD62	MEMDATA62		
DDR_PD63	MEMDATA63		
		ECC0	PPC_ECC0
		ECC1	PPC_ECC1
		ECC2	PPC_ECC2
		ECC3	PPC_ECC3
		ECC4	PPC_ECC4
		ECC5	PPC_ECC5
		ECC6	PPC_ECC6
		ECC7	PPC_ECC7

DDR_CLKOUT

DDR_CLKOUT#

R813 1 2 500ps Loop

DDR_VREF_0V9

5V

1V8

C158 0.1UF

C148 0.1UF

C151 0.1UF 0402

C152 0.1UF 0402

C148 0.01UF

Place parts as close to CPU as possible

U32

VIN 10

VLDOIN 2

VDDQSNS 1

S3 7

S5 9

VTT 3

VTTSNS 5

VTTREF 6

GND 8

PGND 4

R230 10K

R229 10K

C459 4U7F 10V

C456 10UF 16V

C453 100NF 10V

C457 10UF 16V

C458 10UF 16V

DDR_VTT

DDR_VREF_0V9

GND

J8

DDR_PDQ63	236	DDR2_DIMM_DQ[63]	PPC_ECC7 168 22-6D
DDR_PDQ62	235	DDR2_DIMM_DQ[62]	PPC_ECC6 167 22-6D
DDR_PDQ61	230	DDR2_DIMM_DQ[61]	PPC_ECC5 162 22-7D
DDR_PDQ60	229	DDR2_DIMM_DQ[60]	PPC_ECC4 161 22-7D
DDR_PDQ59	117	DDR2_DIMM_DQ[59]	PPC_ECC3 49 22-7D
DDR_PDQ58	116	DDR2_DIMM_DQ[58]	PPC_ECC2 48 22-7D
DDR_PDQ57	111	DDR2_DIMM_DQ[57]	PPC_ECC1 43 22-7D
DDR_PDQ56	110	DDR2_DIMM_DQ[56]	PPC_ECC0 42 22-7D
DDR_PDQ55	227	DDR2_DIMM_DQ[55]	
DDR_PDQ54	226	DDR2_DIMM_DQ[54]	
DDR_PDQ53	218	DDR2_DIMM_DQ[53]	
DDR_PDQ52	217	DDR2_DIMM_DQ[52]	
DDR_PDQ51	108	DDR2_DIMM_DQ[51]	
DDR_PDQ50	107	DDR2_DIMM_DQ[50]	
DDR_PDQ49	99	DDR2_DIMM_DQ[49]	
DDR_PDQ48	98	DDR2_DIMM_DQ[48]	
DDR_PDQ47	215	DDR2_DIMM_DQ[47]	
DDR_PDQ46	214	DDR2_DIMM_DQ[46]	
DDR_PDQ45	209	DDR2_DIMM_DQ[45]	
DDR_PDQ44	208	DDR2_DIMM_DQ[44]	
DDR_PDQ43	96	DDR2_DIMM_DQ[43]	
DDR_PDQ42	95	DDR2_DIMM_DQ[42]	
DDR_PDQ41	90	DDR2_DIMM_DQ[41]	
DDR_PDQ40	89	DDR2_DIMM_DQ[40]	
DDR_PDQ39	206	DDR2_DIMM_DQ[39]	
DDR_PDQ38	205	DDR2_DIMM_DQ[38]	
DDR_PDQ37	200	DDR2_DIMM_DQ[37]	
DDR_PDQ36	199	DDR2_DIMM_DQ[36]	
DDR_PDQ35	87	DDR2_DIMM_DQ[35]	
DDR_PDQ34	86	DDR2_DIMM_DQ[34]	
DDR_PDQ33	81	DDR2_DIMM_DQ[33]	
DDR_PDQ32	80	DDR2_DIMM_DQ[32]	
DDR_PDQ31	159	DDR2_DIMM_DQ[31]	
DDR_PDQ30	158	DDR2_DIMM_DQ[30]	
DDR_PDQ29	153	DDR2_DIMM_DQ[29]	
DDR_PDQ28	152	DDR2_DIMM_DQ[28]	
DDR_PDQ27	40	DDR2_DIMM_DQ[27]	
DDR_PDQ26	39	DDR2_DIMM_DQ[26]	
DDR_PDQ25	34	DDR2_DIMM_DQ[25]	
DDR_PDQ24	33	DDR2_DIMM_DQ[24]	
DDR_PDQ23	150	DDR2_DIMM_DQ[23]	
DDR_PDQ22	149	DDR2_DIMM_DQ[22]	
DDR_PDQ21	144	DDR2_DIMM_DQ[21]	
DDR_PDQ20	143	DDR2_DIMM_DQ[20]	
DDR_PDQ19	31	DDR2_DIMM_DQ[19]	
DDR_PDQ18	30	DDR2_DIMM_DQ[18]	
DDR_PDQ17	25	DDR2_DIMM_DQ[17]	
DDR_PDQ16	24	DDR2_DIMM_DQ[16]	
DDR_PDQ15	141	DDR2_DIMM_DQ[15]	
DDR_PDQ14	140	DDR2_DIMM_DQ[14]	
DDR_PDQ13	132	DDR2_DIMM_DQ[13]	
DDR_PDQ12	131	DDR2_DIMM_DQ[12]	
DDR_PDQ11	22	DDR2_DIMM_DQ[11]	
DDR_PDQ10	21	DDR2_DIMM_DQ[10]	
DDR_PDQ9	13	DDR2_DIMM_DQ[9]	
DDR_PDQ8	12	DDR2_DIMM_DQ[8]	
DDR_PDQ7	129	DDR2_DIMM_DQ[7]	
DDR_PDQ6	128	DDR2_DIMM_DQ[6]	
DDR_PDQ5	123	DDR2_DIMM_DQ[5]	
DDR_PDQ4	122	DDR2_DIMM_DQ[4]	
DDR_PDQ3	10	DDR2_DIMM_DQ[3]	
DDR_PDQ2	9	DDR2_DIMM_DQ[2]	
DDR_PDQ1	4	DDR2_DIMM_DQ[1]	
DDR_PDQ0	3	DDR2_DIMM_DQ[0]	
	101	DDR2_DIMM_SA2	
	240	DDR2_DIMM_SA1	
	239	DDR2_DIMM_SA0	
	120	DDR2_DIMM_SCL	PPC_DDR2_DIMM_SCL
	119	DDR2_DIMM_SDA	PPC_DDR2_DIMM_SDA

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1V8

R228 4K7

R227 4K7

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA1	22-8L,22-9D
DDR2_DIMM_BA[1]	190	DDR_PBA2	22-8L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-8L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	NC	
DDR2_DIMM_CK_N[2]	221	NC	
DDR2_DIMM_CK_P[1]	137	NC	
DDR2_DIMM_CK_N[1]	138	NC	
DDR2_DIMM_CK_P[0]	185	DDR_CLKOUT	
DDR2_DIMM_CK_N[0]	186	DDR_CLKOUT#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-7L,22-8D
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-9D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D
ERR_OUT	55	PPC_DDR2_ERROR	1 TP4
PAR_IN	68	PAR_IN	1 TP5

R226 4K7

PPC_DDR2_RESET_N

1-2B,1-2M,24-5J

C455 5PF 50V

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

DDR_VTT

RP24 DDR_PA15 DDR_PA14 DDR_PA13 DDR_PA12

RP23 DDR_PA11 DDR_PA10 DDR_PA9 DDR_PA8

RP22 DDR_PA7 DDR_PA6 DDR_PA5 DDR_PA4

RP21 DDR_PA3 DDR_PA2 DDR_PA1 DDR_PA0

RP25 22-8K,22-9D DDR_PBA1 22-8K,22-9D DDR_PBA2 22-8K,22-9D DDR_PBA0 22-8K,22-9D DDR_PCAS#

RP26 22-7K,22-9D DDR_PRAS# 22-6K,22-8D DDR_PCKE 22-3K,22-9D DDR_PWE# 22-3K,22-8D DDR_PCS0#

RP19 22-3K,22-8D DDR_PCS1# 22-8D DDR_PODT0 22-8D DDR_PODT1 NC

CP26 CP28 CP29 CP30 CP32 CP31 CP33

GND

J8

	237	VSS_64	
	234	VSS_63	
	231	VSS_62	
	228	VSS_61	
	225	VSS_60	
	222	VSS_59	
	219	VSS_58	
	216	VSS_57	
	213	VSS_56	
	210	VSS_55	
	207	VSS_54	
	204	VSS_53	
	201	VSS_52	
	198	VSS_51	
	169	VSS_50	
	166	VSS_49	
	163	VSS_48	
	160	VSS_47	
	157	VSS_46	
	154	VSS_45	
	151	VSS_44	
	148	VSS_43	
	145	VSS_42	
	142	VSS_41	
	139	VSS_40	
	136	VSS_39	
	133	VSS_38	
	130	VSS_37	
	127	VSS_36	
	124	VSS_35	
	121	VSS_34	
	118	VSS_33	
	115	VSS_32	
	112	VSS_31	
	109	VSS_30	
	106	VSS_29	
	103	VSS_28	
	100	VSS_27	
	97	VSS_26	
	94	VSS_25	
	91	VSS_24	
	88	VSS_23	
	85	VSS_22	
	82	VSS_21	
	79	VSS_20	
	66	VSS_19	
	65	VSS_18	
	50	VSS_17	
	47	VSS_16	
	44	VSS_15	
	41	VSS_14	
	38	VSS_13	
	35	VSS_12	
	32	VSS_11	
	29	VSS_10	
	26	VSS_9	
	23	VSS_8	
	20	VSS_7	
	17	VSS_6	
	14	VSS_5	
	11	VSS_4	
	8	VSS_3	
	5	VSS_2	
	2	VSS_1	

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DDR_VREF_0V9

VREF 1

1V8

VDDSPD 238

1V8

VDD_11	197	
VDD_10	189	
VDD_9	187	
VDD_8	184	
VDD_7	178	
VDD_6	172	
VDD_5	69	
VDD_4	67	
VDD_3	64	
VDD_2	59	
VDD_1	53	

1V8

VDDQ_11	194	
VDDQ_10	191	
VDDQ_9	181	
VDDQ_8	175	
VDDQ_7	170	
VDDQ_6	78	
VDDQ_5	75	
VDDQ_4	72	
VDDQ_3	62	
VDDQ_2	56	
VDDQ_1	51	

879160001

GND

DDR_VREF_0V9 1V8 1V8 1V8

C432 100NF 10V C433 10NF 25V

C454 100NF 10V C434 10NF 25V

C430 100NF 10V C443 10NF 25V C431 100NF 10V C444 10NF 25V

C436 100NF 10V C445 10NF 25V C435 100NF 10V C446 10NF 25V

GND

1V8 1V8 1V8

C438 100NF 10V C451 10NF 25V C437 100NF 10V C452 10NF 25V

C439 100NF 10V C449 10NF 25V C440 100NF 10V C450 10NF 25V

C441 100NF 10V C448 10NF 25V C442 100NF 10V C447 10NF 25V

GND

PLACE NEAREST DDR2 MODULE PINS

ROACH/iBOB2		ROACH_PPC_DDR2			
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN		DOC NO: NRF-ADM-XXX-SD-0001		REVISION: A	
http://casper.berkeley.edu/		DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW			
10-15-2007_14:28		DRAWN: F KAPP		APPR:	
PATH PATH		CHECKED: E BAUERMEISTER		SHEET 22 OF 25	

PWR_GOOD
1-2G,1-3H,24-8K

3V3

PWR_GOOD monitors the
+1.0v, 1V5, 1V8,
2V5, and 3V3 supplies

D1 BAV70

R41 10K

R40 100

C47 2.2UF

SPST SW1

U31 MIC2775YM-29

R28 2.2K

R29 3.3K

RESET_PORW 6,11
1-2D,1-3L,1-5G,24-8C,25-5G

GND

C484 0.1UF

RESET_PB_POR#
1-2M,1-3H,24-8C

IRQ0-9 have programmable polarity per section 10.5.7 (UIC0_PPC 440ep user manual

R31 2.3K
R32 2.3K
R33 3.3K
R35 3.3K

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_3V3_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz

U9 CY22381FX_8211

C48 18PF
C49 18PF
22.1184MHZ
Y1

R30 2.3K

SEL_SYSCLK
1-1M,1-3H,24-7C

CLK_UART_11.0592MHZ
1-3L,1-5G,25-3D

CLK_SYS_33MHZ

CLK_CPLD_33MHZ
1-1G,1-2L,24-7C

R51 33
R52 33
R53 33

C606 0.1UF

U1 440EPX

SYSTEM INTERRUPTS

RESET_PORW
SYSRESET#
SYSCLK
YMRCLK
TESTEN
SYSERR
THERMONA
THERMONB
PGROUT

CLK_TMRCLK
1-1M,1-3H,24-7C

R24 1K

SYSERR
1-1G,1-3L,24-7C

PPC_THERMONA
1-3L,1-9E,2-6L
PPC_THERMONB
1-3L,1-9E,2-4L

TEST POINT TP1

R25 1K

PPC440EPX-NTA533T

IRQ0
IRQ1
IRQ2
IRQ3
IRQ4_GPIO44_DMAACK1
IRQ5_MDDCTRL_DMAREQ1
IRQ6_GPIO45_EXT1_TC1
IRQ7_GPIO46_DMAREQ0
IRQ8_GPIO47_DMAACK0
IRQ9_GPIO48_EOT0_TC0

GETH0_INT#
1-3M,1-4E,20-4E
MONITOR_INT
1-3M,1-9E,2-1P
VS_INT#
1-3M,1-5L,25-8Q
STTM_ALERT
1-3M,1-5L,25-2B
GPIO44
1-3L
SX95T_TDI
1-3L,1-7C,18-2L
SX95T_TCK
1-3L,1-7C,18-2L
SX95T_TMS
1-3L,1-7C,18-2L
SX95T_TDO
1-3M,1-7G,18-2L

R01 1K
R02 1K
R03 1K
R04 1K
R05 1K
R23 1K

NO POP
RO1 - RO5

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible

U24 CY2292FZX_8211

C51 18PF
C52 18PF
12.00 MHZ
Y2

CLK_SEL_M66EN
1-1M,1-3H,24-7C

R34 2.3K

R54 33
R55 33

CLK_PCI1_66/33MHZ
1-3L
CLK_PCI2_66/33MHZ
1-3L

CLK_4
NC
CLK_6
CLK_7
CLK_8
NC

R57 33
R59 33
R510 33

CLK_GETH0_25MHZ
1-3L,1-4D,20-4E
CLK_USB2.0_48MHZ
1-3G,1-3L,21-2C
CLK_CPLD_50MHZ
1-1G,1-3L,24-7C

C607 0.1UF
C605 0.1UF

TRACE & JTAG CONNECTORS

P1 .12X H SMT

23-2G
CPU_TDO
CPU_TDI
CPU_TCK
CPU_TMS
CPU_HALT#
DEBUG_TRST#

R37 10K
R38 10K
R39 10K
R49 10K

R36 10K
VCC_JTAG
R26 33
C53 0.1UF

R26 is for current limiting and should be <100 Ohms.

Critical placement and routing
of the Trace connector and nets.
Up to CPU frequency/4

TRACE PORT

V1 440EPX

PROVision JTAG

NC_CLK
CPU_HALT#
MCB58
MCB51
MCB52
MCE58
MCE51
MCE52
MCE53
MCE54
MCT58
MCT51
MCT52
MCT53
MCT54
MCT55
MCT56

TCK
TDO
TDI
TMS
TRST#

CPU_TCK
CPU_TDO
CPU_TDI
CPU_TMS

CPU_TRST#
1-2M,1-3H,24-7C

R27 2.3K
C54 0.1UF

R12 0
R14 0
R15 0
R22 0

J1 JSCN F SMT

R18 0
R11 0
TRC-CLK
R13 0
R16 0
R17 0
R19 0
R20 0
R21 0

23-2E
VCC_JTAG

TRCE54
TRCT58
TRCT51
TRCT52
TRCT53
TRCT54
TRCT55
TRCT56

DEBUG_TRST#
1-1G,1-3L,24-7C

GND

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

10-15-2007_14:28

PATH PATH

ROACH_PPC_TST_CLK_IO

DOC NO: NRF-ADM-XXX-SD-0001
REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER

SHEET 23 OF 25

Memory Bus

PAR#[27:31]
1-2G,1-4L,25-10B

PADATA[0:7]
3-2M,3-4L

PADATA0
PADATA1
PADATA2
PADATA3
PADATA4
PADATA5
PADATA6
PADATA7

PAD#027
PAD#028
PAD#029
PAD#030
PAD#031

RESETS

CPU_TRST# = '1' when JTAG_TRST# = '1' and RESET_PORB = '1' else '0';
see errata sheet

SELECTMAP_CS
1-2G,1-5L,25-7B
PCS_2
1-1G,1-4L,25-7B
PORB
1-1G,1-5L,25-5G,25-7B,25-7M,25-10B
PR_WE
3-1G,3-4L;29-5G,28-6M,d5-7B,25-9B
PWRE_B#
1-2G,1-4L,25-6M,25-7B,25-9B
RESET_PORB
1-2G,1-3L,1-5G,23-9J,25-5G
RESET_PR_PROG
1-2M,1-3M,23-8E
PPC_RESET
1-2G,1-9E,2-1B
DEBUG_TRST#
1-1G,1-3L,23-1F
CPU_TRST#
1-2M,1-2M;23-2F

CLOCKS

CLK_CPLD_33MHZ
1-1G,1-2L,23-6G
CLK_CPLD_50MHZ
1-1G,1-3L,23-4G
CLK_PXICLK
1-1G,1-4L,25-6F
CLK_TMCLK#
1-1M,1-3M,23-6H
CLK_SEL_PXIEN#
1-1M,1-3M,23-5D
SEL_SYSCLK
1-1M,1-3M;23-7D
SYSEN0
3-1G,3-3L;23-8H

STATUS / MISC

FPGA_BSY
1-1G,1-4L,25-7J
PAPG#
3-1M,3-4G;25-8J

FLASH

EE1_WP
1-2M,1-5L,25-1A
EE2_BOOT_WP
1-2M,1-4G,25-5A
ETTH_AS#
1-2M,1-5G,25-1B

I2C

USB

Assertion of USB2_RESET may be asynchronous to CLK_USB2_CPLD
De-assertion of USB2_RESET must be synchronous to CLK_USB2_CPLD

NAND FLASH NOT USED

ETHERNET

GETH0_RST#
1-2M,1-4B,20-4E

USB_EBC_MUX

RESET_CPLD#
1-1M,1-4G,25-3J

PER_CCLK_EN#

U54

roach_cpld_XC2C256_7VQ100C_pcb

PAD4 PAD8 PAD10 PAD12 PAD15 PAD16 PAD17 PAD18 PAD19 PAD20 PAD21 PAD23 PAD28 PAD29 PAD30 PAD31 PAD32 PAD33 PAD34 PAD35 PAD44 PAD48 PAD49 PAD50 PAD52 PAD54 PAD55 PAD59 PAD64 PAD65 PAD66 PAD67 PAD68 PAD69 PAD70 PAD73 PAD74 PAD75 PAD76 PAD77 PAD81 PAD82 PAD86 PAD87 PAD88 PAD89 PAD90 PAD95 PAD100 PAD102 PAD105 PAD107 PAD108 PAD109 PAD112 PAD113

PAD217 PAD214 PAD213 PAD212 PAD211 PAD208 PAD207 PAD206 PAD204 PAD199 PAD197 PAD196 PAD195 PAD194 PAD192 PAD191 PAD190 PAD187 PAD186 PAD178 PAD177 PAD176 PAD175 PAD173 PAD171 PAD169 PAD168 PAD167 PAD166 PAD163 PAD162 PAD161 PAD160 PAD158 PAD156 PAD154 PAD152 PAD146 PAD145 PAD144 PAD143 PAD142 PAD138 PAD137 PAD134 PAD133 PAD132 PAD131 PAD125 PAD121 PAD120 PAD119 PAD118 PAD117 PAD115 PAD114

XC2C256_7VQ100C

ENABLE PER_CLK CONNECTION TO CONFIGURATION I/F MUST CO-ORDINATE WITH SX95T_CCLK_0 AND MODE TO AVOID CLASH

SN74AHC1G125DCKT
U2

C13 100NF 10V

U54

roach_cpld_XC2C256_7VQ100C_powerpins

VCC VAUX VCCIO_3 VCC_1 VCCIO_4 VCCIO_5 VCC_2 VCCIO_6 VCCIO VCCIO_1 VCCIO_2

GND_3 GND_4 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND GND_1 GND_2

XC2C256_7VQ100C

PLACE NEAR CPLD POWER PINS

C473 C474 C475 C476 C477 C478 C479 C480 C481 C482 C483 100NF 10V

USER_DIP0
USER_DIP1
USER_DIP2
USER_DIP3

User DIP-Swith

USER_LED0
USER_LED1
SYSERR#
RESET_BUFPOR#

SX95T_CCLK_0
SX95T_CLK_B_0
SX95T_D_IN_0
SX95T_D_OUT_BUSY_0
SX95T_DONE_0
SX95T_INIT_B_0
SX95T_PROGRAM_B_0
SX95T_ROWB_B_0

CMD/DI
CLK/SCLK

SD/MMC/MMCPLUS CONNECTOR

J17

CMD/DI
CLK/SCLK
VDD
VSS1
VSS2
SD_CD_COM
SD_WP_COM

DAT0/DO DAT1 DAT2 DAT3 DAT4 DAT5 DAT6 DAT7 MNT1 MNT2

GMC050064SEU

QDR2_BY0_1_SYS_RST_N
1-1M,1-4L,34-5J
QDR2_BY2_3_SYS_RST_N
1-2M,1-7L,15-5J
PPC_DDR2_RESET_N
1-2G,1-2M,22-2B
EXT_RESET#
1-2G,1-4L,25-6F

SX95T_M0_0
1-1G,1-3F,1-7G,16-3B,21-4D
SX95T_M1_0
SX95T_M2_0

SysErr will be used to drive Status LED (active H)

74LVC1G08

Boot Configuration

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

Configuration DIP-Swith

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

BOOT_CFG0
BOOT_CFG1
BOOT_CFG2

PWR_GOOD
1-2G,1-3H,23-10G

U54

roach_cpld_XC2C256_7VQ100C_configpins

PAD1 PAD3 PAD5 PAD7 PAD62 TDI TMS TCK TDO PAD218

XC2C256_7VQ100C

Xilinx
Programing Cable

JTAG

J22

TDO VREF NC_0 NC_1 TDI TMS TCK GND_7 GND_6 GND_4 GND_3 GND_2 GND_1 GND_0

R193 1K R192 1K

PLACE NEAR CPLD JTAG CONNECTOR

ROACH/iBOB2	ROACH_PPC_CPLD
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-15-2007_14:28 PATH PATH	DRAWN: F KAPP APPR:
	CHECKED: E BAUERMEISTER SHEET 24 OF 25

PDATA[0:31]
PADD[2:31]
PADD30 IS THE LSB FOR 16 BIT
WIDE BUS TRANSFERS
NOTE:
DMA SIGNALS
IN GREEN TEXT
PADD2 IS THE MSB
External Slave Peripheral
External Master Peripheral Interface
FLASH
EPB RESET OUTPUT
EXT_RESET#
CLK_PERCLK
U15
BANKS=1, 2, 4
CHIP SELECT 1
NO POP
UART
IIC0
IIC1_SPI
NAND Flash Interface
NOT USED
UART Port 0
UART Port 1
J14
HLE-105-02-G-DV
GND
ROACH/iBOB2
ROACH_PPC_NVM_SERIAL
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
DOC NO
NRF-ADM-XXX-SD-0001
REVISION
A
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:
F KAPP
CHECKED:
E BAUERMEISTER
10-15-2007_14:28
PATH
SHEET
25 OF 25