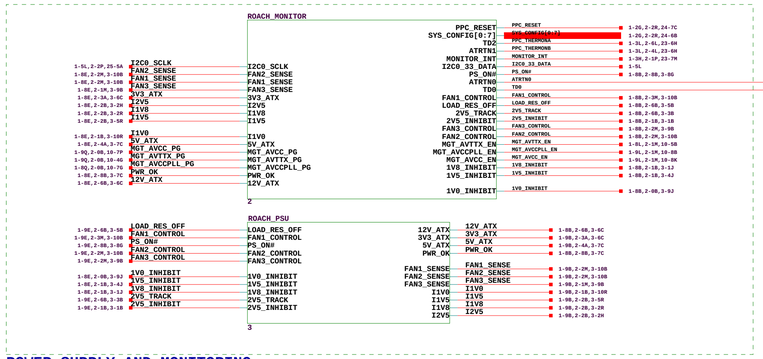
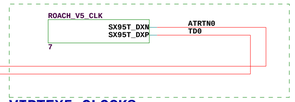
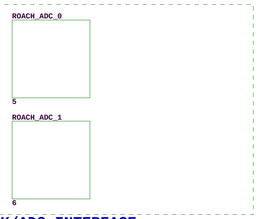
VIRTEX5

POWER SUPPLY AND MONITORING



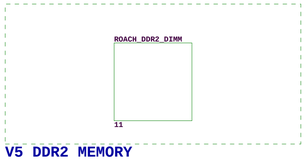
VIRTEX5 CLOCKS



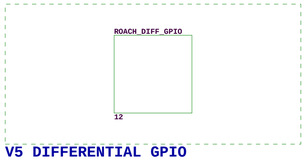


ZDOK/ADC INTERFACE

V5 DDR2 MEMORY

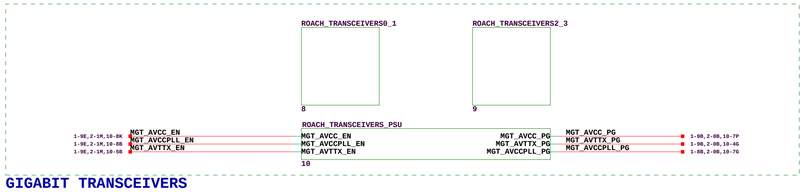


V5 DIFFERENTIAL GPIO

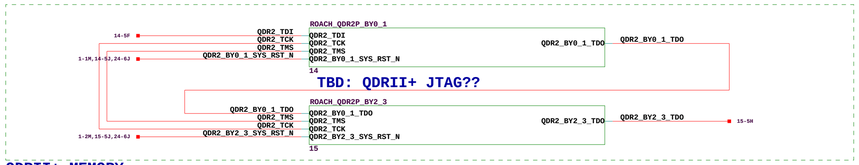


V5 SE GPIO & MISCELLANEOUS

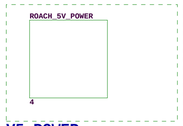
GIGABIT TRANSCEIVERS



QDRII+ MEMORY

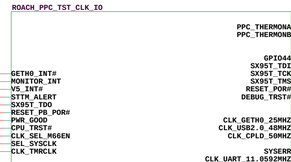


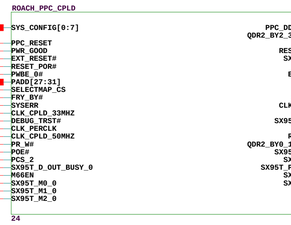
V5 POWER



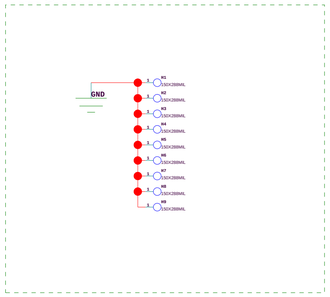
VIRTEX5 CONFIGURATION

PPC





MECHANICAL



CONTRIBUTORS

ETIENNE BAUERMEISTER
HENRY CHEN
STEVE DURAND
FRANCOIS KAPP
ALAN LANDMAN
GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHEIMER

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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11-14-2007_14:55

PATH PATH

ROACH_TOP

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 1 OF 25

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

TIE TO GROUND IF PLL'S ARE NOT USED

PLACE AT ACTEL 3V3 POWER PINS

PLACE AT ACTEL 1V5 POWER PINS

roach_AFS600_powerpins

roach_AFS600_configpins

roach_AFS600_pcb

PB POWER SWITCH

KEY - REMOVE PIN

MONITOR RESET

XPORT - PLACE IN REAR I/O REGION

TEMPERATURE DIODE HEADER

ACTEL JTAG CONNECTOR

REFERENCE RESISTOR/ADC VALUES

FOR 8 BIT ADC USING 2.56V REFERENCE:

VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)	ADC COUNT AT MAX POWER	CURRENT/BIT (A)
12V	0R01	3.36	0.11	33	0.1
5V	0R0047	6.78	0.22	31	0.21
3V3	0R01	3.47	0.12	34	0.1
2V5	0R01	3.56	0.13	35	0.1
1V8	0R0022	12.91	0.37	28	0.45
1V5	0R0047	6.77	0.22	31	0.21
1V0	0R001	26.79	0.72	26	1.0

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
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11-14-2007_14:55

PATH PATH

ROACH_MONITOR

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	2 OF 25

PSU INPUT SUMMARY

VOLTAGE	5.0V +- 10%
CURRENT (MAX)	6.0A

PSU RAIL SUMMARY

VOLTAGE	1.0V +- 5%
SUPPLIES	FPGA CORE
CURRENT (QUIESCENT)	1.5A
CURRENT (ACTIVE)	26.8A
LOAD STEP	25.3A

PSU INPUT SUMMARY

VOLTAGE	12V +- 10%
CURRENT (MAX)	0.8A

PSU RAIL SUMMARY

VOLTAGE	1.5V +- 5%
SUPPLIES	FPGA IO, QDR, PPC
CURRENT (QUIESCENT)	0.25A
CURRENT (ACTIVE)	6.8A
LOAD STEP	6.55A

PSU RAIL SUMMARY

VOLTAGE	2.5V +- 5%
SUPPLIES	FPGA, ZDOK PPC, PHY
CURRENT (QUIESCENT)	0.1A
CURRENT (ACTIVE)	3.6A
LOAD STEP	3.5A

PSU INPUT SUMMARY

VOLTAGE	12V +- 10%
CURRENT (MAX)	1.8A

PSU RAIL SUMMARY

VOLTAGE	1.8V +- 5%
SUPPLIES	FPGA IO, DDR2 x 2
CURRENT (QUIESCENT)	1A
CURRENT (ACTIVE)	12.9A
LOAD STEP	11.9A

PSU INPUT SUMMARY

VOLTAGE	12V +- 10%
CURRENT (MAX)	0.8A

ROACH/iBOB2

COLLABORATORS:

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PATH PATH

ROACH_PSU

DOC NO: NRF-ADM-XXX-SD-0001

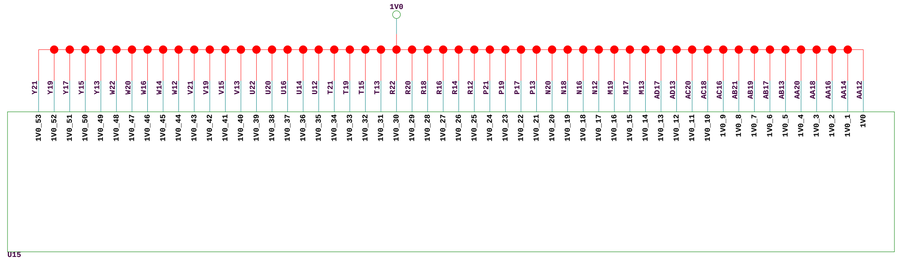
REVISION: A

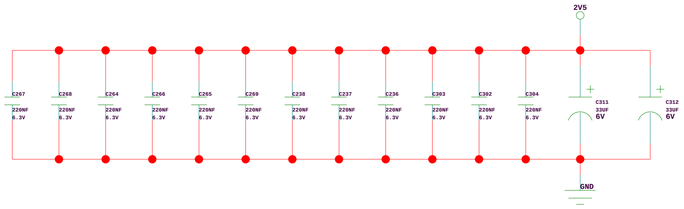
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

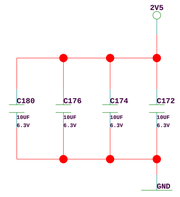
DRAWN: F KAPP

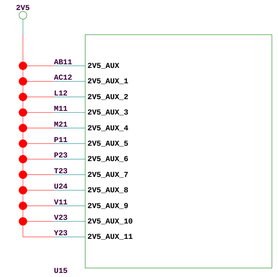
APPR:

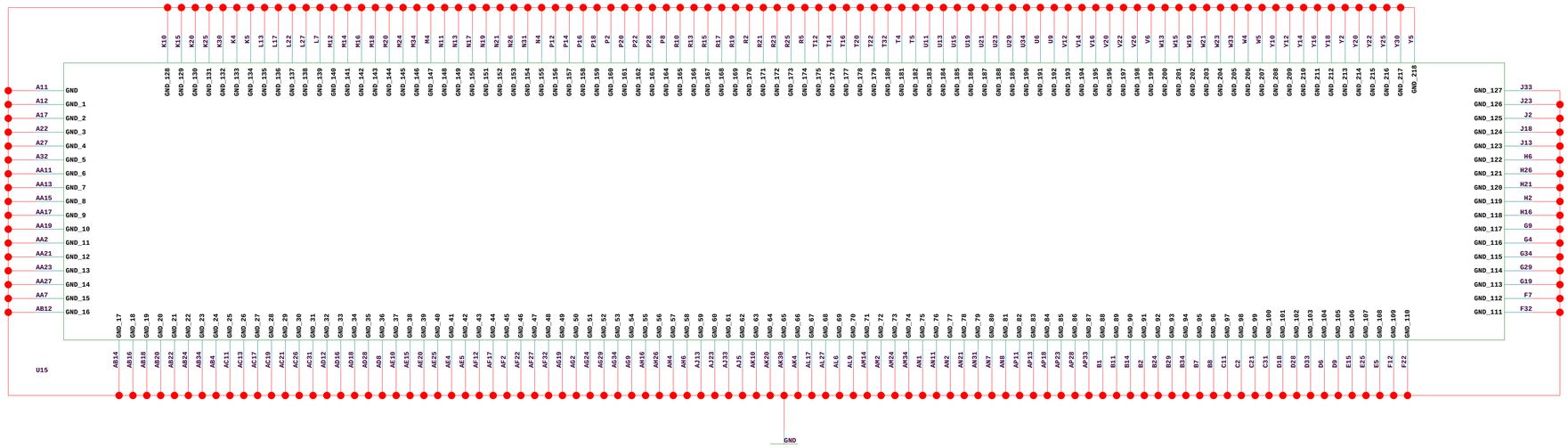
CHECKED: E BAUERMEISTER











ROACH/iBOB2	ROACH_5V_POWER
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
11-14-2007_14:55 PATH PATH	


ZDOK0_CLK0_P K18
ZDOK0_CLK0_N J19
ZDOK0_CLK1_P J16
ZDOK0_CLK1_N J17
VRP_20 L11
VRN_20 L10
VRP_12_GPIOLVC25 P9
VRN_12_GPIOLVC25 R9
2V5_12 M9
2V5_12_1 N6
2V5_12_2 T7
2V5_20 E10
2V5_20_1 H11
2V5_20_2 J8
ZDOK0_DP_P[37] E6
ZDOK0_DP_N[37] E7
ZDOK0_DP_P[36] T9
ZDOK0_DP_N[36] U10
ZDOK0_DP_P[35] G6
ZDOK0_DP_N[35] G7
ZDOK0_DP_P[34] T10
ZDOK0_DP_N[34] T11
ZDOK0_DP_P[33] F5
ZDOK0_DP_N[33] F6
ZDOK0_DP_P[32] R11
ZDOK0_DP_N[32] P10
ZDOK0_DP_P[31] H5
ZDOK0_DP_N[31] G5
ZDOK0_DP_P[30] H7
ZDOK0_DP_N[30] J7
ZDOK0_DP_P[29] T8
ZDOK0_DP_N[29] U7
ZDOK0_DP_P[28] R7
ZDOK0_DP_N[28] R8
ZDOK0_DP_P[27] J6
ZDOK0_DP_N[27] J5
ZDOK0_DP_P[26] R6
ZDOK0_DP_N[26] T6
ZDOK0_DP_P[25] K7
ZDOK0_DP_N[25] K6
ZDOK0_DP_P[24] P7
ZDOK0_DP_N[24] P6
ZDOK0_DP_P[23] L4
ZDOK0_DP_N[23] L5
ZDOK0_DP_P[22] N5
ZDOK0_DP_N[22] P5
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ZDOK0_DP_N[20] N7
ZDOK0_DP_P[19] M6
ZDOK0_DP_N[19] M5
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ZDOK0_DP_N[18] G13
ZDOK0_DP_P[17] N10
ZDOK0_DP_N[17] N9
ZDOK0_DP_P[16] E12
ZDOK0_DP_N[16] E13
ZDOK0_DP_P[15] M10
ZDOK0_DP_N[15] L9
ZDOK0_DP_P[14] F11
ZDOK0_DP_N[14] E11
ZDOK0_DP_P[13] M8
ZDOK0_DP_N[13] L8
ZDOK0_DP_P[12] G11
ZDOK0_DP_N[12] G12
ZDOK0_DP_P[11] B13
ZDOK0_DP_N[11] C13
ZDOK0_DP_P[10] K8
ZDOK0_DP_N[10] K9
ZDOK0_DP_P[9] J10
ZDOK0_DP_N[9] J9
ZDOK0_DP_P[8] A13
ZDOK0_DP_N[8] B12
ZDOK0_DP_P[7] H10
ZDOK0_DP_N[7] H9
ZDOK0_DP_P[6] D12
ZDOK0_DP_N[6] C12
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ZDOK0_DP_N[5] J11
ZDOK0_DP_P[4] D11
ZDOK0_DP_N[4] D10
ZDOK0_DP_P[3] G8
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ZDOK0_DP_N[1] F8
ZDOK0_DP_P[0] E9
ZDOK0_DP_N[0] E8
5-5L
5-3L
NC
2V5
C328 47UF 6V
C327 47UF 6V
C326 47UF 6V
C329 47UF 6V
C325 220NF 6.3V
C322 220NF 6.3V
C323 220NF 6.3V
C324 220NF 6.3V
U15
BANKS=20, 12
5V
3V3
2V5
1V8
C315 1UF 16V
C314 100NF 10V
C317 1UF 16V
C316 100NF 10V
C318 1UF 16V
C319 100NF 10V
C321 1UF 16V
C320 100NF 10V
P5
6367550-5
ZDOK40
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ZDOK0_DP_N[0] A2
ZDOK0_DP_P[1] A3
ZDOK0_DP_N[1] A4
ZDOK0_DP_P[2] A5
ZDOK0_DP_N[2] A6
ZDOK0_DP_P[3] A7
ZDOK0_DP_N[3] A8
ZDOK0_DP_P[4] A9
ZDOK0_DP_N[4] A10
ZDOK0_DP_P[5] A11
ZDOK0_DP_N[5] A12
ZDOK0_DP_P[6] A13
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ZDOK0_DP_N[9] A20
ZDOK0_DP_P[10] D1
ZDOK0_DP_N[10] D2
ZDOK0_DP_P[11] D3
ZDOK0_DP_N[11] D4
ZDOK0_DP_P[12] D5
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ZDOK0_DP_P[19] D19
ZDOK0_DP_N[19] D20
C1 ZDOK0_DP_P[20]
C2 ZDOK0_DP_N[20]
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C4 ZDOK0_DP_N[21]
C5 ZDOK0_DP_P[22]
C6 ZDOK0_DP_N[22]
C7 ZDOK0_DP_P[23]
C8 ZDOK0_DP_N[23]
C9 ZDOK0_DP_P[24]
C10 ZDOK0_DP_N[24]
C11 ZDOK0_DP_P[25]
C12 ZDOK0_DP_N[25]
C13 ZDOK0_DP_P[26]
C14 ZDOK0_DP_N[26]
C15 ZDOK0_DP_P[27]
C16 ZDOK0_DP_N[27]
C17 ZDOK0_DP_P[28]
C18 ZDOK0_DP_N[28]
C19 ZDOK0_CLK0_P 5-7B
C20 ZDOK0_CLK0_N 5-7B
F1 ZDOK0_DP_P[29]
F2 ZDOK0_DP_N[29]
F3 ZDOK0_DP_P[30]
F4 ZDOK0_DP_N[30]
F5 ZDOK0_DP_P[31]
F6 ZDOK0_DP_N[31]
F7 ZDOK0_DP_P[32]
F8 ZDOK0_DP_N[32]
F9 ZDOK0_DP_P[33]
F10 ZDOK0_DP_N[33]
F11 ZDOK0_DP_P[34]
F12 ZDOK0_DP_N[34]
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F16 ZDOK0_DP_N[36]
F17 ZDOK0_DP_P[37]
F18 ZDOK0_DP_N[37]
F19 ZDOK0_CLK1_P 5-7B
F20 ZDOK0_CLK1_N 5-7B
6367550-5
ZDOK40
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
11-14-2007_14:55
PATH PATH
ROACH_ADC_0
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 5 OF 25

ROACH/iBOB2

COLLABORATORS:

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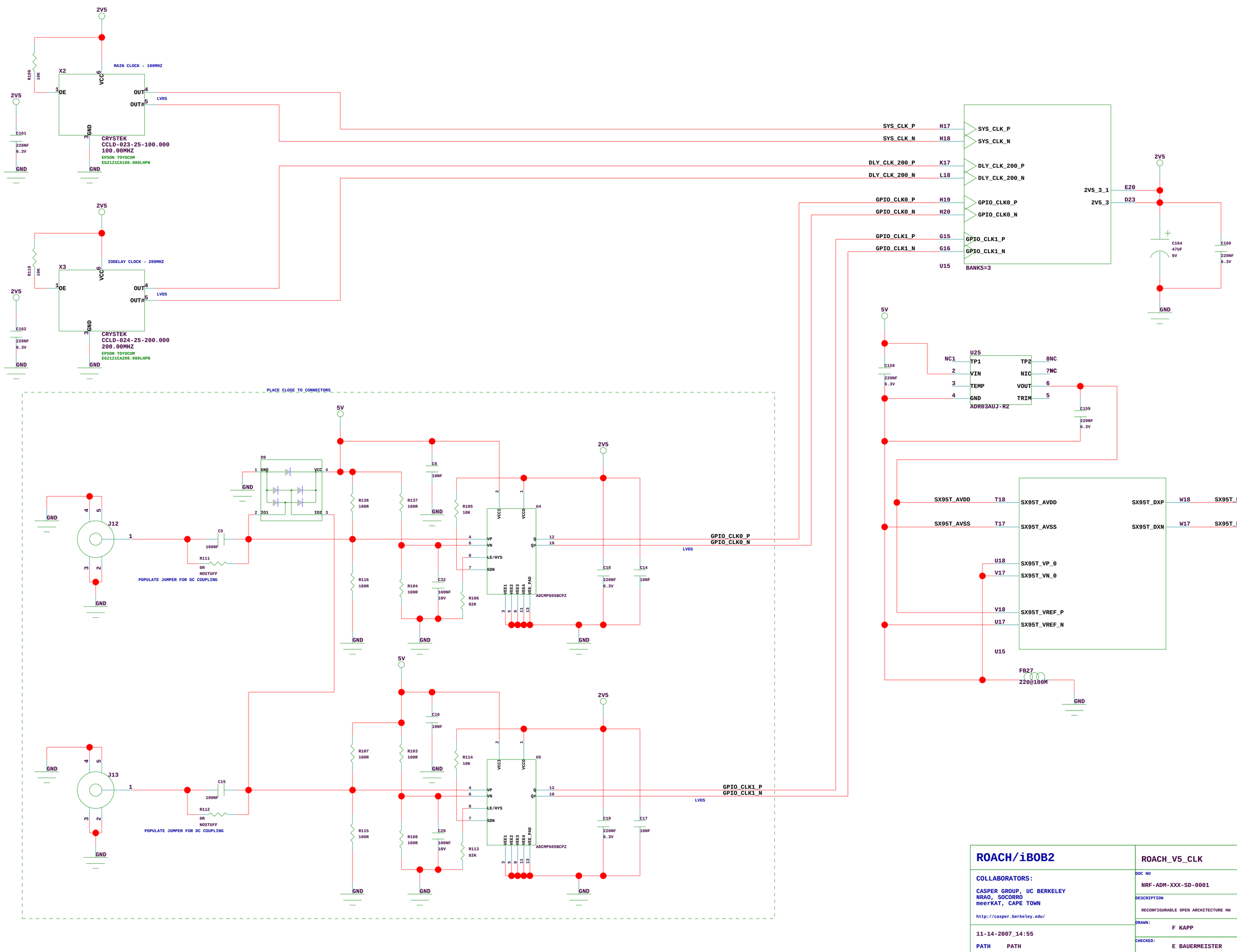
11-14-2007_14:55

PATH PATH

ROACH_ADC_1

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	6 OF 25



ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
11-14-2007_14:55 PATH PATH	

ROACH/iBOB2

ROACH_TRANSCEIVERS0_1

COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

DOC NO: NRF-ADM-XXX-SD-0001
REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER

11-14-2007_14:55
PATH PATH

SHEET 8 OF 25

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

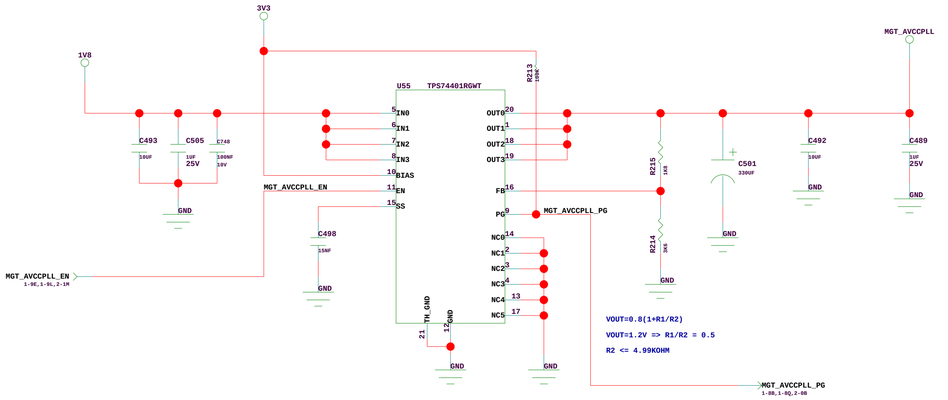
G4 AND G8 CONNECTED IN
2X2 MODULE

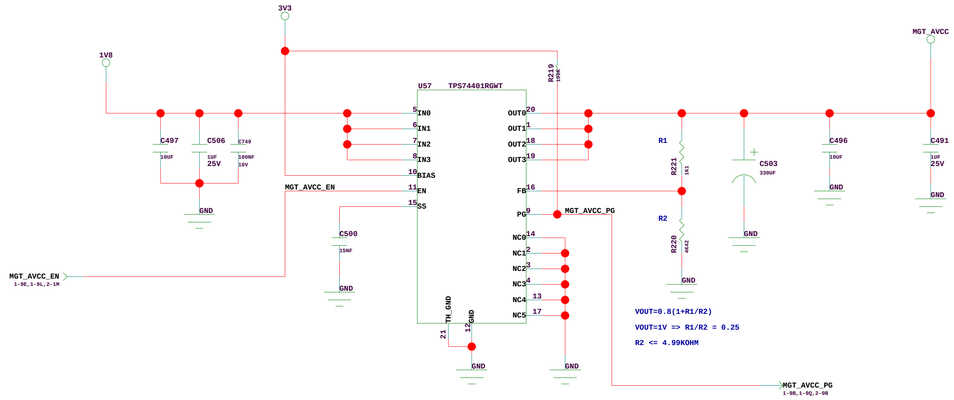
OPTICAL MODULE FAULT - RED LED

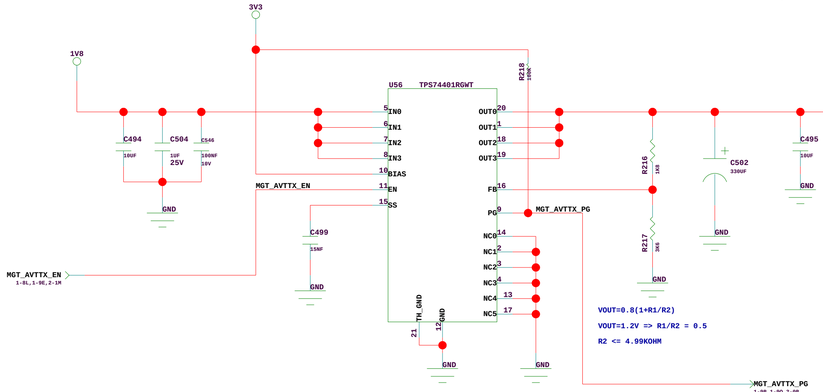
CCLD-023-25-156.250
156.25MHZ

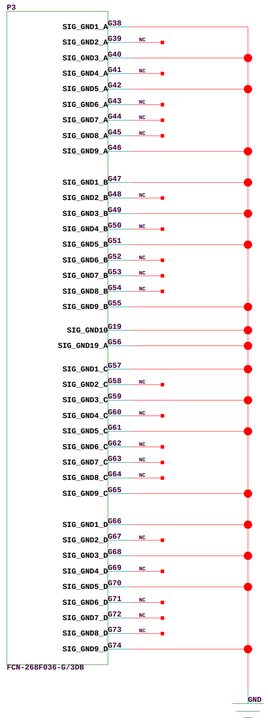
FCN-268F036-G/3DB

ROACH/iBOB2	ROACH_TRANSCEIVERS2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
11-14-2007_14:55	DRAWN: F KAPP APPR:
PATH PATH	CHECKED: E BAUERMEISTER SHEET 9 OF 25

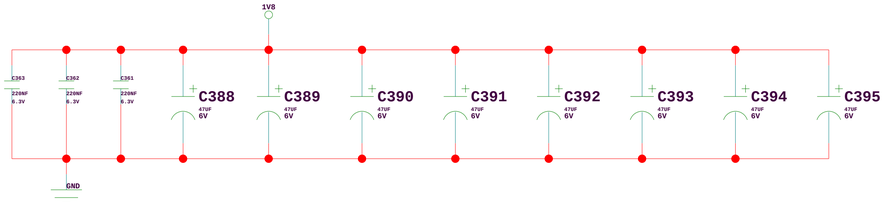


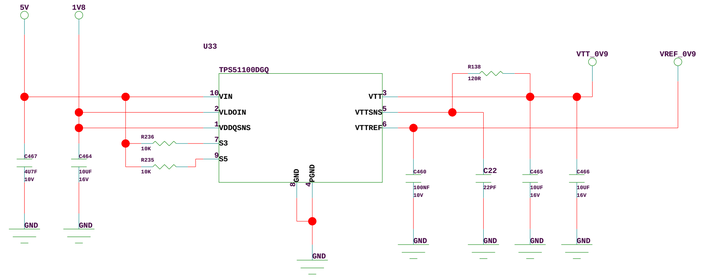


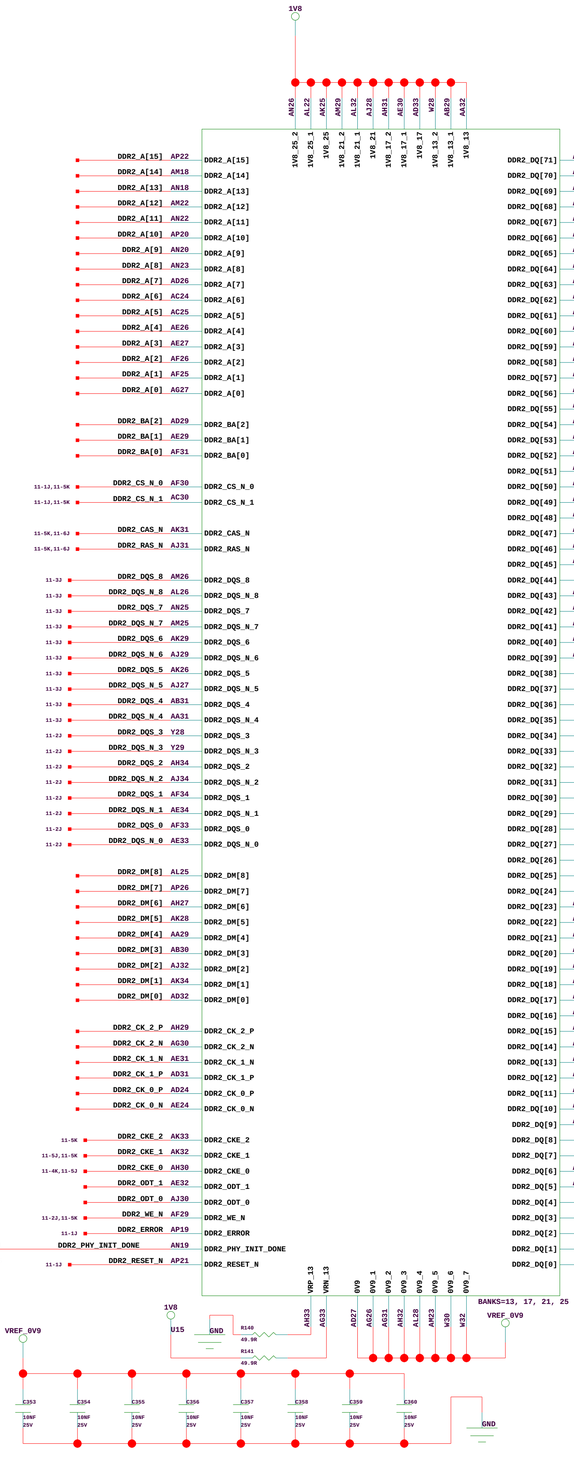


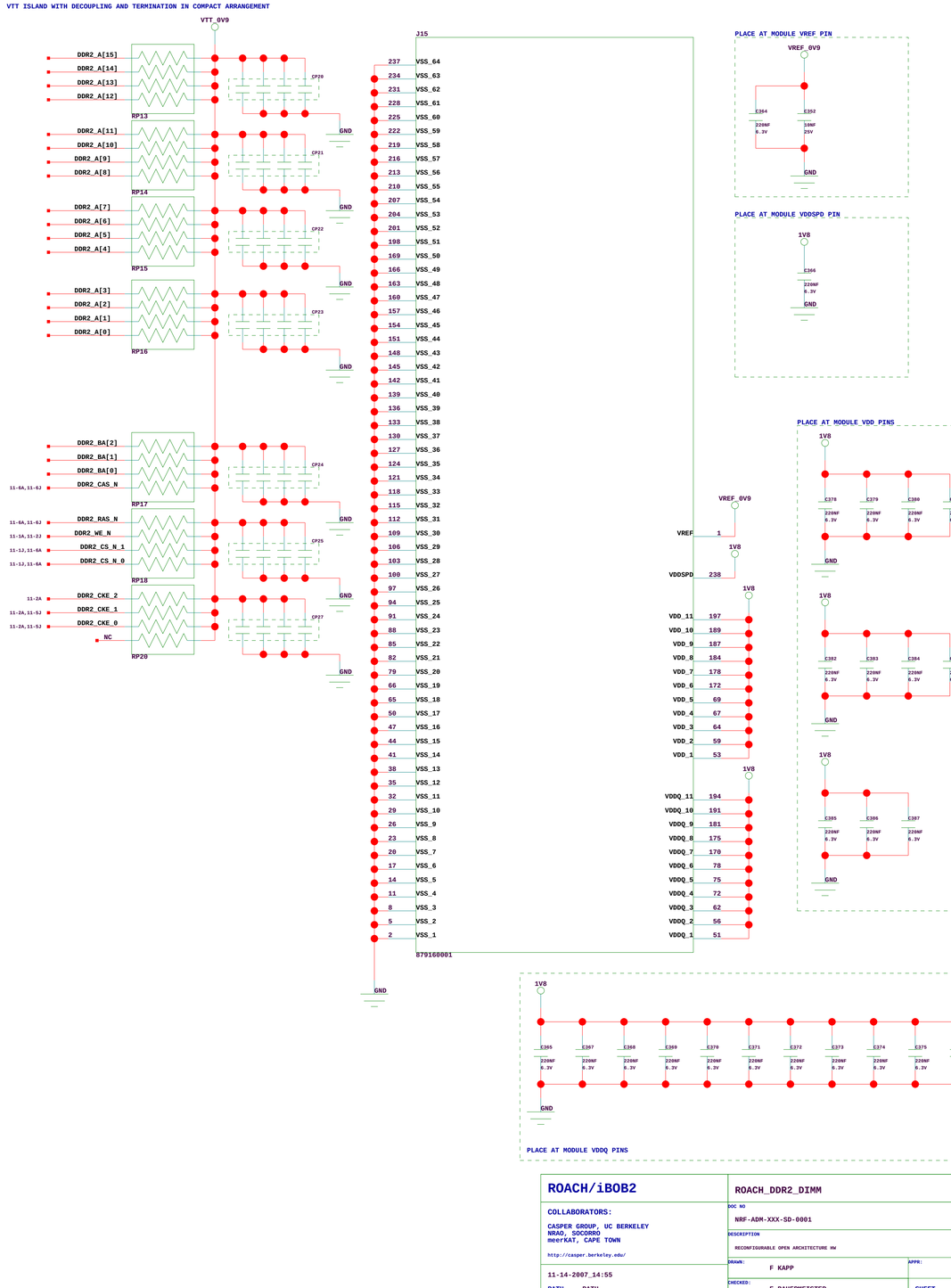


ROACH/iBOB2	**ROACH_TRANSCEIVERS_PSU**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-14-2007_14:55	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 10 OF 25

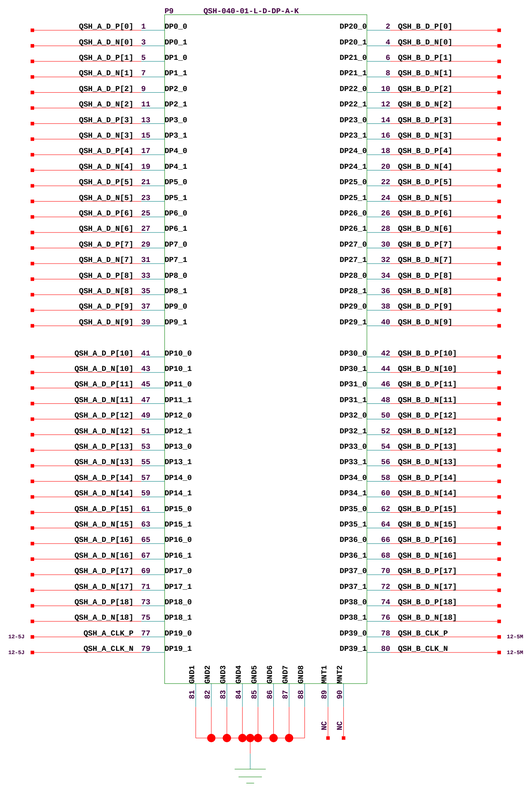


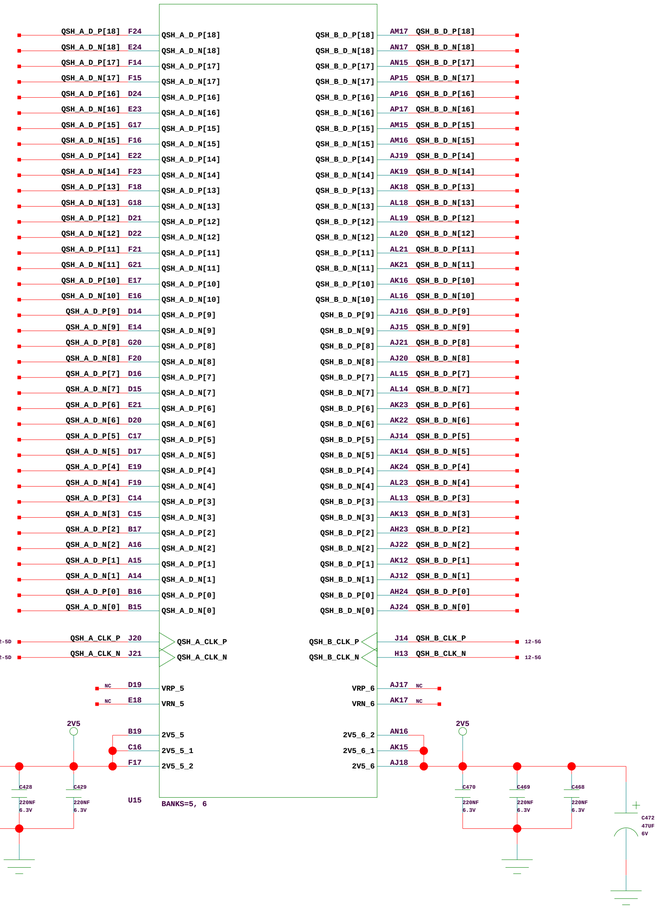






ROACH/iBOB2	**ROACH_DDR2_DIMM**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A; DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW; DRAWN: F KAPP; APPR:
11-14-2007_14:55; PATH PATH	CHECKED: E BAUERMEISTER; SHEET 11 OF 25





ROACH/iBOB2	**ROACH_DIFF_GPIO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-14-2007_14:55 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 12 OF 25

GPIOLVC18[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

GPIOLVC18[20] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

IO VOLTAGE LEVEL SELECT	
1-2: 3.3V	DEFAULT
2-3: 2.5V	

GPIOLVC18[4] IS DUAL FUNCTION:
1. DRIVES LED
2. CONTROLS DIRECTION ON GPIOLVC33[1-4]

IF CR18 IS ON, CLOCK CAPABLE GPIO'S ARE OUTPUTS

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

11-14-2007_14:55

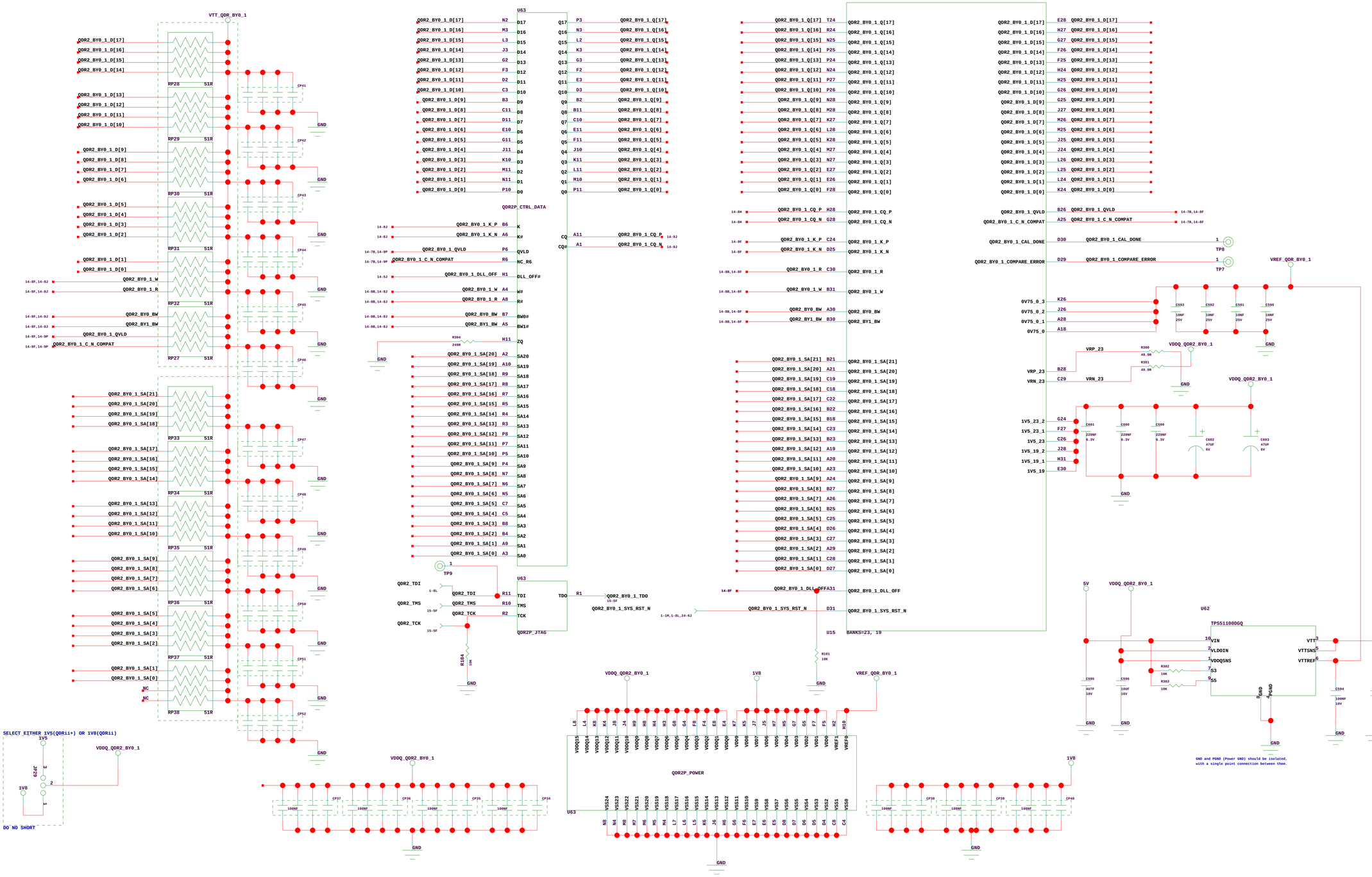
PATH PATH

ROACH_GPIO_MISC

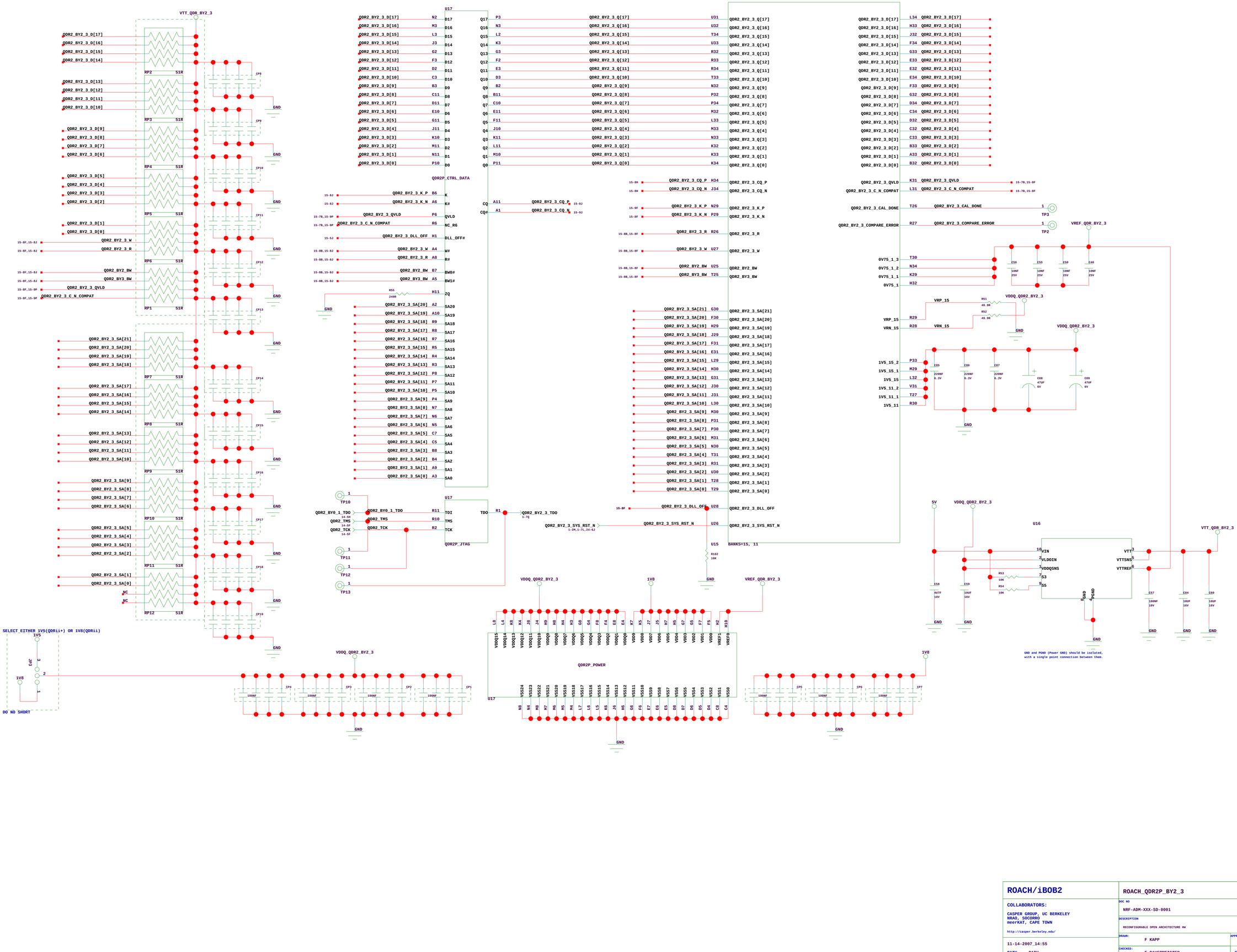
DOC NO	REVISION
NRF-ADM-XXX-SD-0001	A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MM

DRAWN:	APPR:
F KAPP	
CHECKED:	SHEET
E BAUERMEISTER	13 OF 25



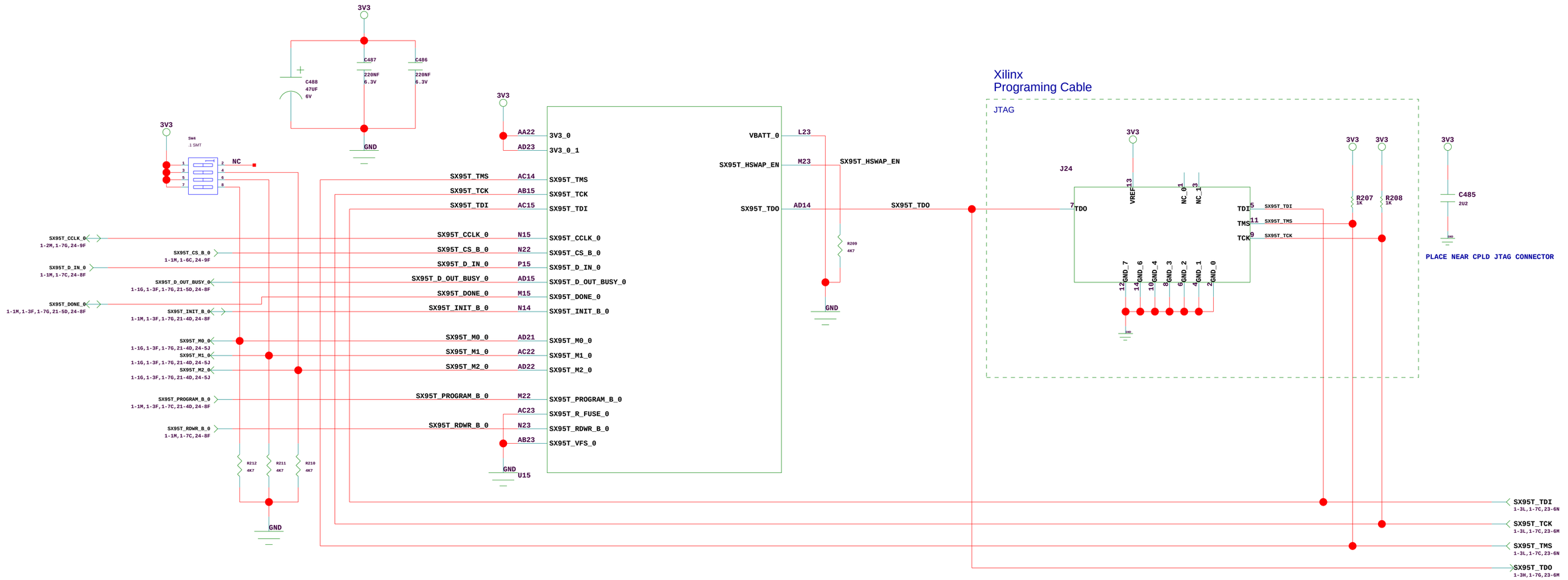
ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-14-2007_14:55 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 14 OF 25



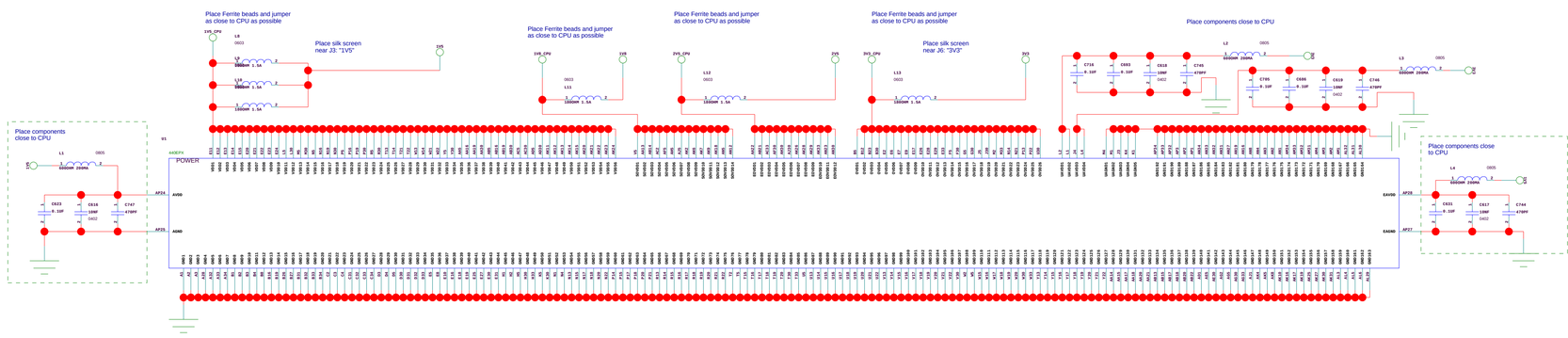
ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS:	DOC NO: NRF-ADM-XXX-SD-0001
CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN	REVISION: A
http://casper.berkeley.edu/	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-14-2007_14:55	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 15 OF 25

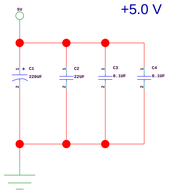
TBD

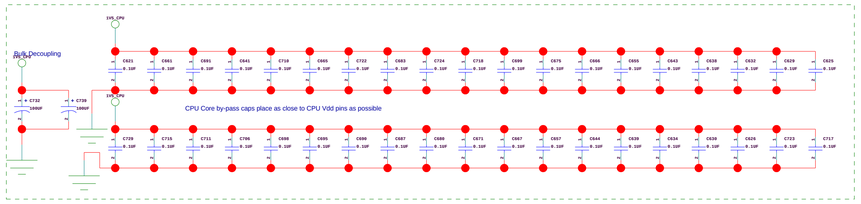
VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

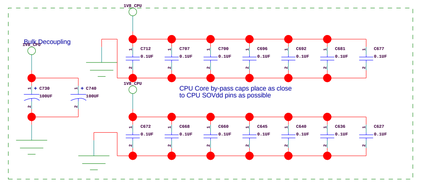


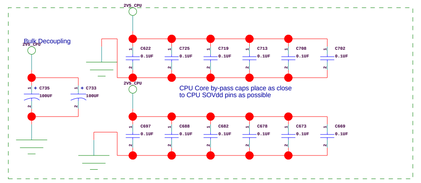
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
11-14-2007_14:55 PATH PATH	

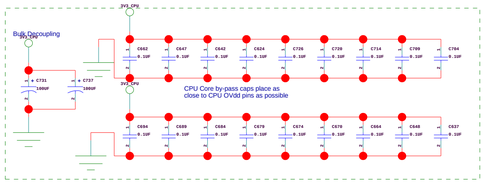


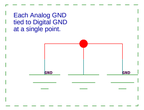










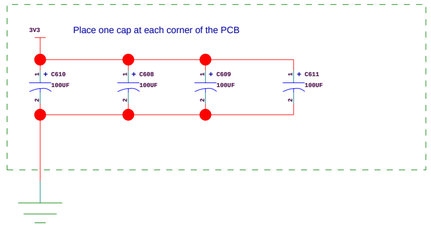


REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 17 OF 25
11-14-2007_14:55 PATH PATH	

REMOVED 3V3 GENERATION



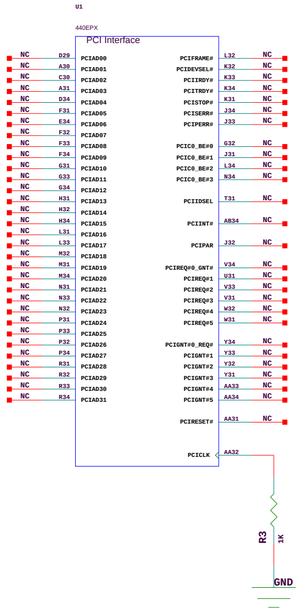
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET: 18 OF 25
11-14-2007_14:55 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-14-2007_14:55 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

Place nearest PHY pin 96

Place nearest PHY pin 101

Place nearest PHY pin 98

Place nearest PHY pin 100

Place as close to PHY CORE VDD power pins as possible

Place as close to PHY IO VDD power pins as possible

UNUSED SECOND ETHERNET MAC

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups. Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place jumers in line with signals

Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5

Place decoupling C as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible.

Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

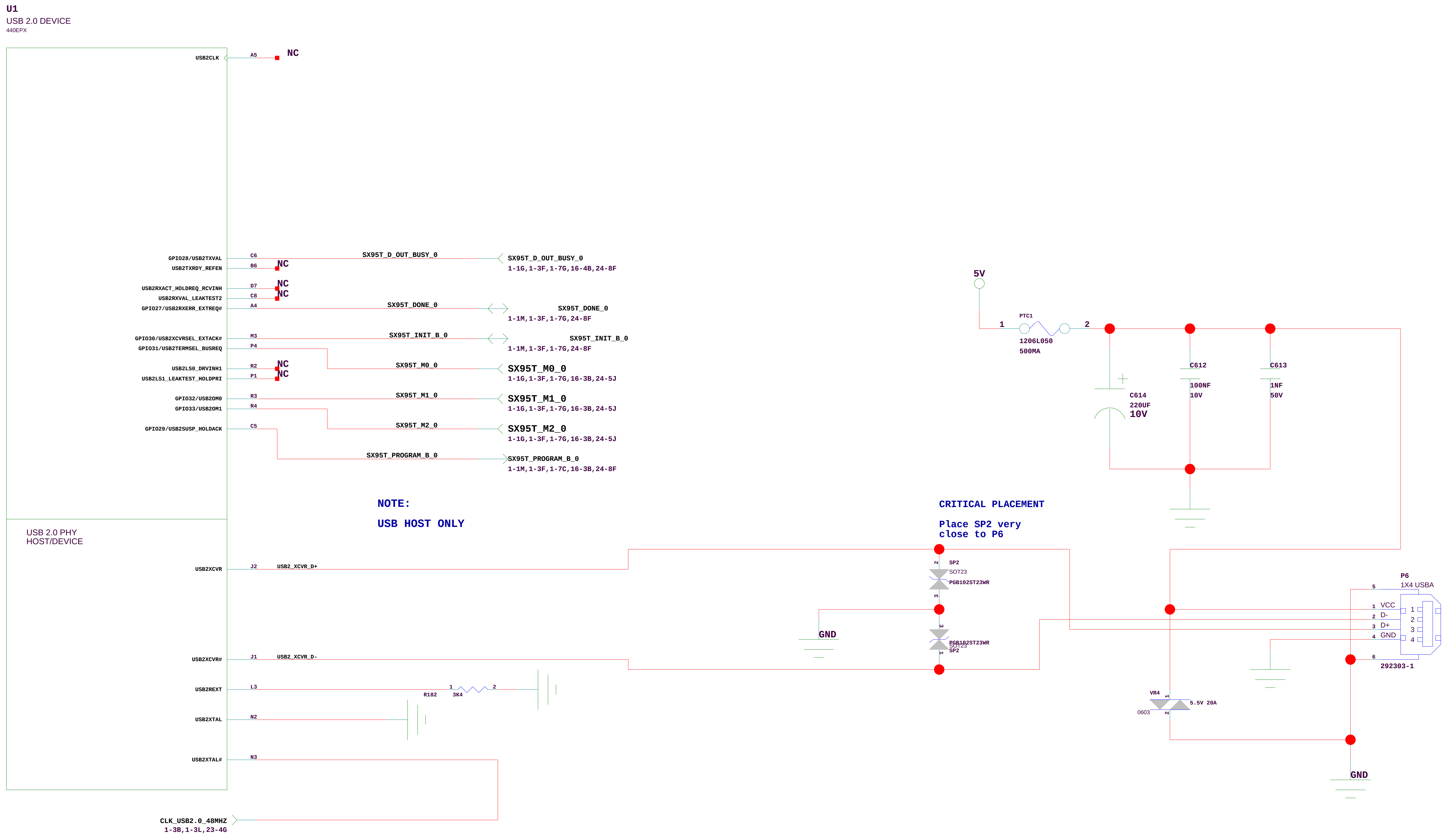
Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

ETHERNET Mgt.

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

ROACH/iBOB2	ROACH_PPC_ETH1
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
11-14-2007_14:55	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 20 OF 25



ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

11-14-2007_14:55

PATH PATH

ROACH_PPC_USB

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 21 OF 25

ROACH/iBOB2

ROACH_PPC_DDR2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

CHECKED: E BAUERMEISTER

APPR:

11-14-2007_14:55

PATH PATH

SHEET 22 OF 25

PWR_GOOD
1-2G,1-3H,24-8K

3V3

PWR_GOOD monitors the
+1.0V, 1V5, 1V8,
2V5, and 3V3 supplies

RESET_PB_POR#
1-2M,1-3H,24-8C

RESET_PORH
6,11
1-2G,1-3L,1-5G,24-8C,25-5G

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_3V3_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz

SEL_SYSCLK
1-1M,1-3H,24-7C

CLK_UART_11.0592MHZ
1-1L,1-5G,25-3D

CLK_SYS_33MHZ

CLK_CPLD_33MHZ
1-1G,1-2L,24-7C

CLK_TMRCLK
1-1M,1-3H,24-7C

SYSERR
1-1G,1-3L,24-7C

PPC_THERMONA
1-3L,1-9E,2-6L

PPC_THERMONB
1-3L,1-9E,2-4L

PPC440EPX-NTA533T

IRQ0-9 have programmable polarity per
section 10.5.7 (UIC0_PR) 440ep user
manual

MONITOR_INT
1-3H,1-9E,2-1P

VS_INT#
1-3H,1-5L,25-8Q

STTM_ALERT
1-3H,1-5L,25-2B

GPIO44
1-3L

SX95T_TDI
1-3L,1-7C,18-2L

SX95T_TCK
1-3L,1-7C,18-2L

SX95T_TMS
1-3L,1-7C,18-2L

SX95T_TDO
1-3H,1-7G,18-2L

NO POP
RO1 - RO5

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible

CLK_SEL_M66EN
1-1M,1-3H,24-7C

CLK_GETH0_25MHZ
1-3L,1-4B,20-4E

CLK_USB2.0_48MHZ
1-3B,1-3L,21-8C

CLK_CPLD_50MHZ
1-1G,1-3L,24-7C

TRACE & JTAG CONNECTORS

Critical placement and routing
of the Trace connector and nets.
Up to CPU frequency/4

TRACE PORT

CPU_TDO
CPU_TDI
CPU_TCK
CPU_TMS
CPU_HALT#

DEBUG_TRST#
1-1G,1-3L,24-7C

R26 is for current
limiting and should
be <100 Ohms.

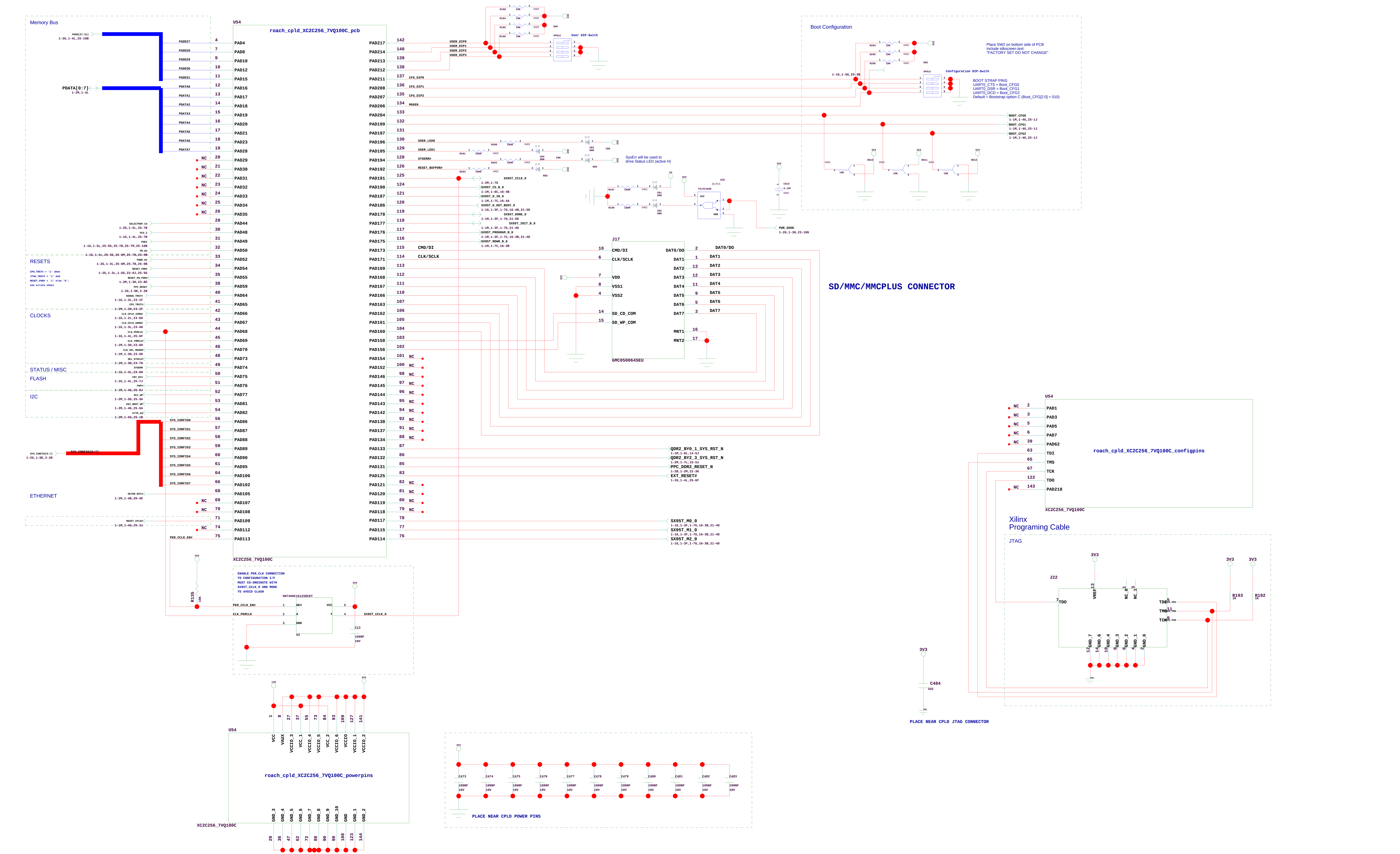
CPU_TRST#
1-2M,1-3H,24-7C

VCC_JTAG

TMC54
TMC56
TMC51
TMC52
TMC53
TMC54
TMC55
TMC56

23-2E
23-2E
23-2E
23-1E
23-1E
23-1E
23-1E
23-1E

ROACH/iBOB2	ROACH_PPC_TST_CLK_IO
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 23 OF 25
11-14-2007_14:55 PATH PATH	



ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

11-14-2007_14:55

PATH PATH

ROACH_PPC_CPLD

DOC NO	REVISION
NRF-ADM-XXX-SD-0001	A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 24 OF 25

ROACH/iBOB2	ROACH_PPC_NVM_SERIAL	
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
11-14-2007_14:55	DRAWN: F KAPP	APPR:
PATH PATH	CHECKED: E BAUERMEISTER	SHEET 25 OF 25