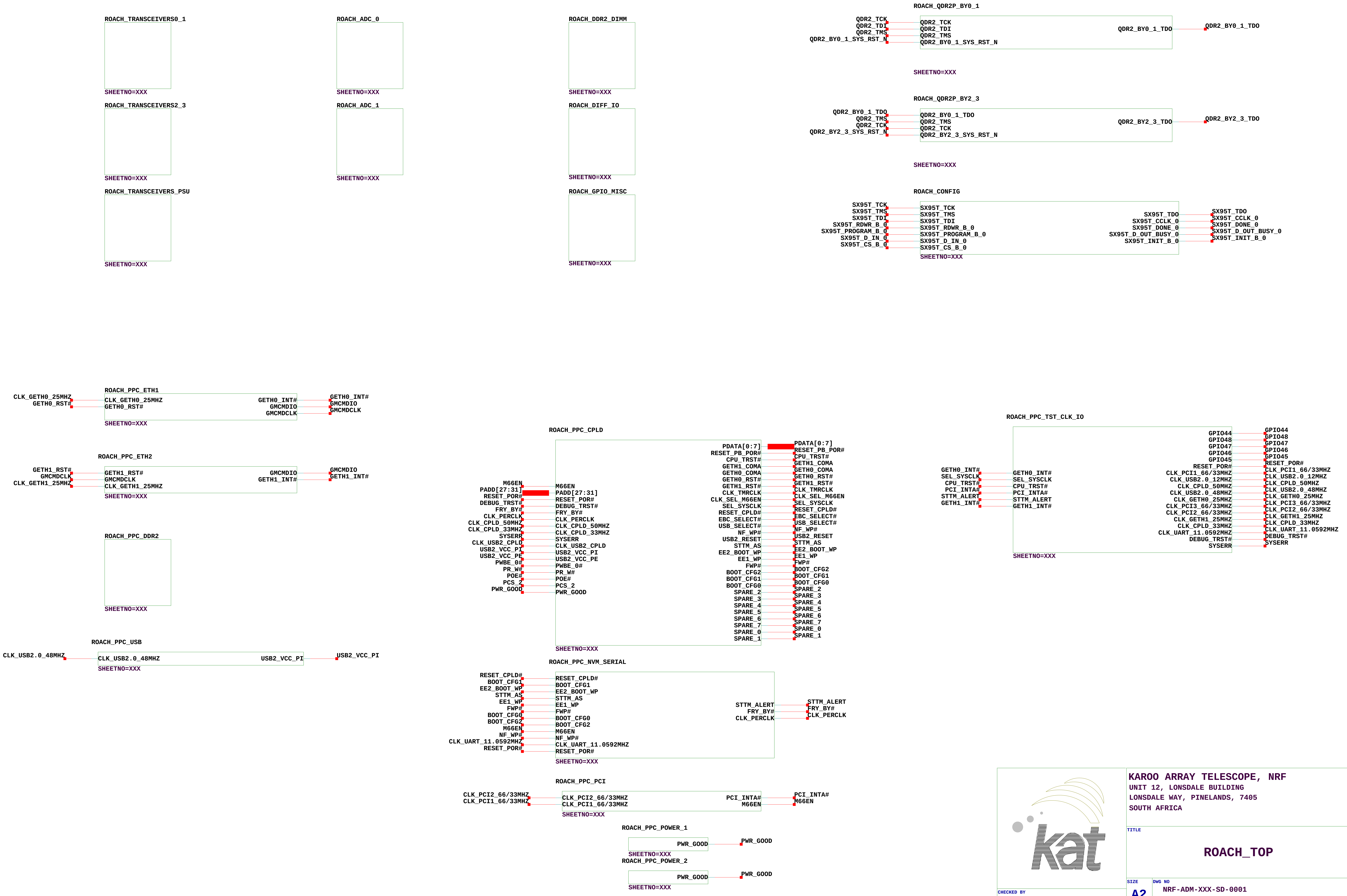

ROACH_TRANSCEIVERS0_1
SHEETNO=XXX
ROACH_TRANSCEIVERS2_3
SHEETNO=XXX
ROACH_TRANSCEIVERS_PSU
SHEETNO=XXX
ROACH_ADC_0
SHEETNO=XXX
ROACH_ADC_1
SHEETNO=XXX
ROACH_DDR2_DIMM
SHEETNO=XXX
ROACH_DIFF_IO
SHEETNO=XXX
ROACH_GPIO_MISC
SHEETNO=XXX
ROACH_QDR2P_BY0_1
QDR2_TCK
QDR2_TDI
QDR2_TMS
QDR2_BY0_1_SYS_RST_N
QDR2_TCK
QDR2_TDI
QDR2_TMS
QDR2_BY0_1_SYS_RST_N
QDR2_BY0_1_TDO
QDR2_BY0_1_TDO
SHEETNO=XXX
ROACH_QDR2P_BY2_3
QDR2_BY0_1_TDO
QDR2_TMS
QDR2_TCK
QDR2_BY2_3_SYS_RST_N
QDR2_BY0_1_TDO
QDR2_TMS
QDR2_TCK
QDR2_BY2_3_SYS_RST_N
QDR2_BY2_3_TDO
QDR2_BY2_3_TDO
SHEETNO=XXX
ROACH_CONFIG
SX95T_TCK
SX95T_TMS
SX95T_TDI
SX95T_RDWR_B_0
SX95T_PROGRAM_B_0
SX95T_D_IN_0
SX95T_CS_B_0
SX95T_TCK
SX95T_TMS
SX95T_TDI
SX95T_RDWR_B_0
SX95T_PROGRAM_B_0
SX95T_D_IN_0
SX95T_CS_B_0
SX95T_TDO
SX95T_CCLK_0
SX95T_DONE_0
SX95T_D_OUT_BUSY_0
SX95T_INIT_B_0
SX95T_TDO
SX95T_CCLK_0
SX95T_DONE_0
SX95T_D_OUT_BUSY_0
SX95T_INIT_B_0
SHEETNO=XXX
ROACH_PPC_ETH1
CLK_GETH0_25MHZ
GETH0_RST#
CLK_GETH0_25MHZ
GETH0_RST#
GETH0_INT#
GMCMDIO
GMCMDCLK
GETH0_INT#
GMCMDIO
GMCMDCLK
SHEETNO=XXX
ROACH_PPC_ETH2
GETH1_RST#
GMCMDCLK
CLK_GETH1_25MHZ
GETH1_RST#
GMCMDCLK
CLK_GETH1_25MHZ
GMCMDIO
GETH1_INT#
GMCMDIO
GETH1_INT#
SHEETNO=XXX
ROACH_PPC_DDR2
SHEETNO=XXX
ROACH_PPC_USB
CLK_USB2.0_48MHZ
CLK_USB2.0_48MHZ
USB2_VCC_PI
USB2_VCC_PI
SHEETNO=XXX
ROACH_PPC_CPLD
M66EN
PADD[27:31]
RESET_POR#
DEBUG_TRST#
FRY_BY#
CLK_PERCLK
CLK_CPLD_50MHZ
CLK_CPLD_33MHZ
SYSERR
CLK_USB2_CPLD
USB2_VCC_PI
USB2_VCC_PE
PWBE_0#
PR_W#
POE#
PCS_2
PWR_GOOD
M66EN
PADD[27:31]
RESET_POR#
DEBUG_TRST#
FRY_BY#
CLK_PERCLK
CLK_CPLD_50MHZ
CLK_CPLD_33MHZ
SYSERR
CLK_USB2_CPLD
USB2_VCC_PI
USB2_VCC_PE
PWBE_0#
PR_W#
POE#
PCS_2
PWR_GOOD
PDATA[0:7]
RESET_PB_POR#
CPU_TRST#
GETH1_COMA
GETH0_COMA
GETH0_RST#
GETH1_RST#
CLK_TMRCLK
CLK_SEL_M66EN
SEL_SYSCLK
RESET_CPLD#
EBC_SELECT#
USB_SELECT#
NF_WP#
USB2_RESET
STTM_AS
EE2_BOOT_WP
EE1_WP
FWP#
BOOT_CFG2
BOOT_CFG1
BOOT_CFG0
SPARE_2
SPARE_3
SPARE_4
SPARE_5
SPARE_6
SPARE_7
SPARE_0
SPARE_1
PDATA[0:7]
RESET_PB_POR#
CPU_TRST#
GETH1_COMA
GETH0_COMA
GETH0_RST#
GETH1_RST#
CLK_TMRCLK
CLK_SEL_M66EN
SEL_SYSCLK
RESET_CPLD#
EBC_SELECT#
USB_SELECT#
NF_WP#
USB2_RESET
STTM_AS
EE2_BOOT_WP
EE1_WP
FWP#
BOOT_CFG2
BOOT_CFG1
BOOT_CFG0
SPARE_2
SPARE_3
SPARE_4
SPARE_5
SPARE_6
SPARE_7
SPARE_0
SPARE_1
SHEETNO=XXX
ROACH_PPC_NVM_SERIAL
RESET_CPLD#
BOOT_CFG1
EE2_BOOT_WP
STTM_AS
EE1_WP
FWP#
BOOT_CFG0
BOOT_CFG2
M66EN
NF_WP#
CLK_UART_11.0592MHZ
RESET_POR#
RESET_CPLD#
BOOT_CFG1
EE2_BOOT_WP
STTM_AS
EE1_WP
FWP#
BOOT_CFG0
BOOT_CFG2
M66EN
NF_WP#
CLK_UART_11.0592MHZ
RESET_POR#
STTM_ALERT
FRY_BY#
CLK_PERCLK
STTM_ALERT
FRY_BY#
CLK_PERCLK
SHEETNO=XXX
ROACH_PPC_PCI
CLK_PCI2_66/33MHZ
CLK_PCI1_66/33MHZ
CLK_PCI2_66/33MHZ
CLK_PCI1_66/33MHZ
PCI_INTA#
M66EN
PCI_INTA#
M66EN
SHEETNO=XXX
ROACH_PPC_POWER_1
PWR_GOOD
PWR_GOOD
SHEETNO=XXX
ROACH_PPC_POWER_2
PWR_GOOD
PWR_GOOD
SHEETNO=XXX
ROACH_PPC_TST_CLK_IO
GETH0_INT#
SEL_SYSCLK
CPU_TRST#
PCI_INTA#
STTM_ALERT
GETH1_INT#
GETH0_INT#
SEL_SYSCLK
CPU_TRST#
PCI_INTA#
STTM_ALERT
GETH1_INT#
GPIO44
GPIO48
GPIO47
GPIO46
GPIO45
RESET_POR#
CLK_PCI1_66/33MHZ
CLK_USB2.0_12MHZ
CLK_CPLD_50MHZ
CLK_USB2.0_48MHZ
CLK_GETH0_25MHZ
CLK_PCI3_66/33MHZ
CLK_PCI2_66/33MHZ
CLK_GETH1_25MHZ
CLK_CPLD_33MHZ
CLK_UART_11.0592MHZ
DEBUG_TRST#
SYSERR
GPIO44
GPIO48
GPIO47
GPIO46
GPIO45
RESET_POR#
CLK_PCI1_66/33MHZ
CLK_USB2.0_12MHZ
CLK_CPLD_50MHZ
CLK_USB2.0_48MHZ
CLK_GETH0_25MHZ
CLK_PCI3_66/33MHZ
CLK_PCI2_66/33MHZ
CLK_GETH1_25MHZ
CLK_CPLD_33MHZ
CLK_UART_11.0592MHZ
DEBUG_TRST#
SYSERR
SHEETNO=XXX

KAROO ARRAY TELESCOPE, NRF
UNIT 12, LONSDALE BUILDING
LONSDALE WAY, PINELANDS, 7405
SOUTH AFRICA

TITLE
ROACH_TOP

SIZE	DWG NO	REV
A2	NRF-ADM-XXX-SD-0001	A

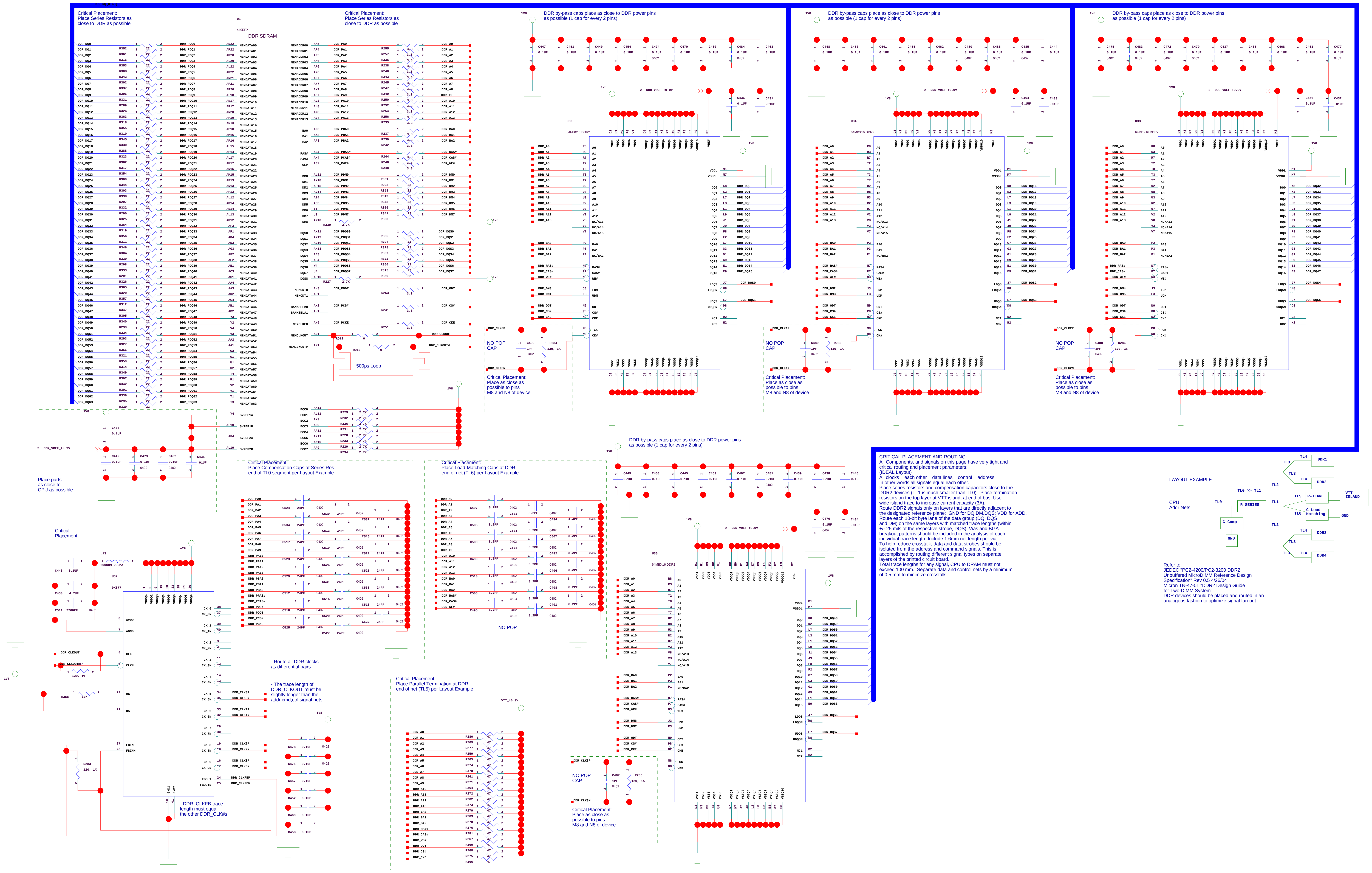
CHECKED BY
<PUT NAME HERE>

DRAWN BY
FRANCOIS KAPP

SCALE
NTS

SHEET 1 of 1

9-7-2007_16:22



Critical Placement:
Place Series Resistors as close to DDR as possible

DDR by-pass caps place as close to DDR power pins as possible (1 cap for every 2 pins)

Critical Placement:
Place as close as possible to pins M8 and N8 of device

Place parts as close to CPU as possible

Critical Placement

Critical Placement:
Place Compensation Caps at Series Res. end of TL0 segment per Layout Example

Critical Placement:
Place Load-Matching Caps at DDR end of net (TL6) per Layout Example

- Route all DDR clocks as differential pairs

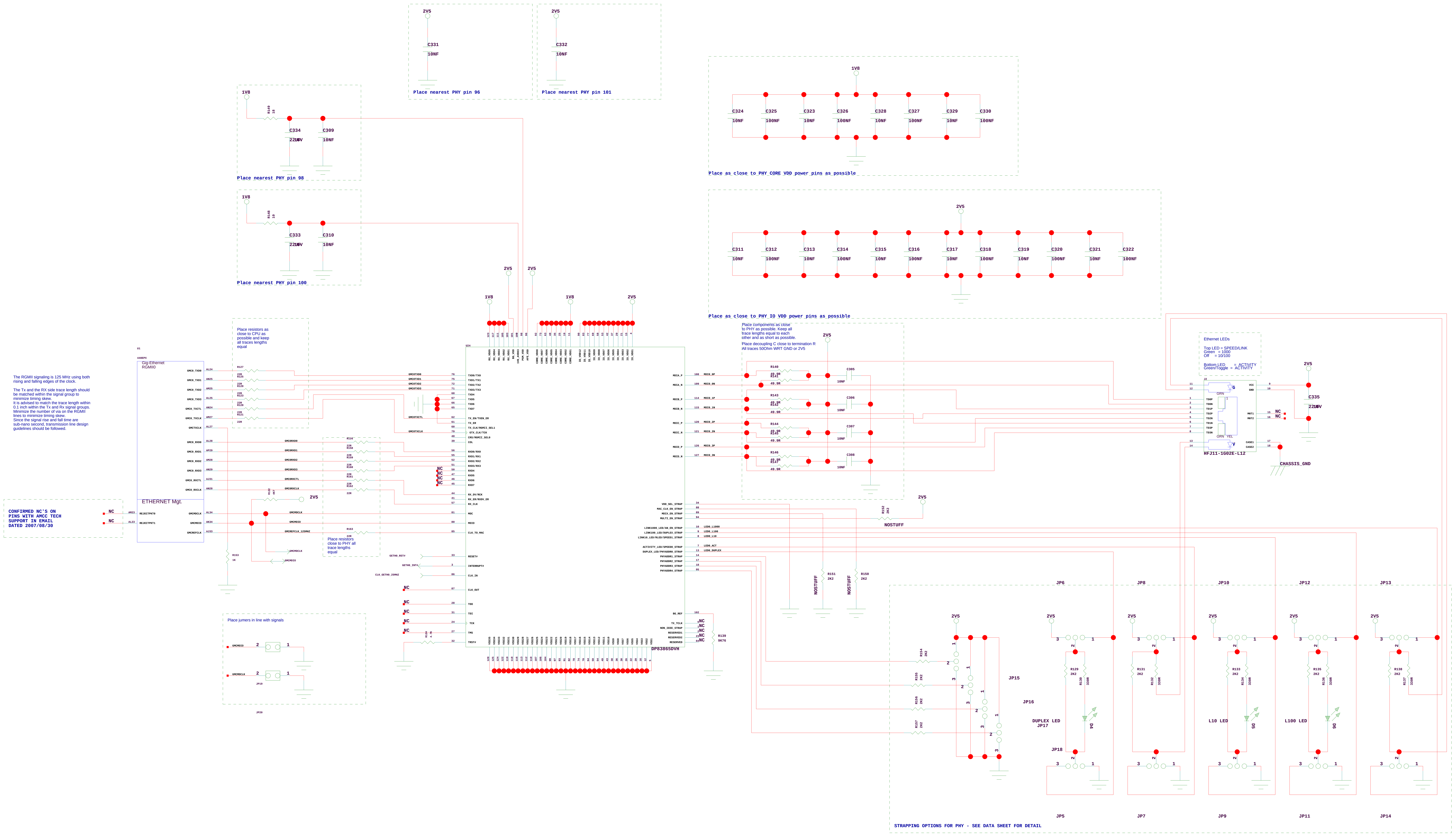
- The trace length of DDR_CLKOUT must be slightly longer than the addr,cmd,ctrl signal nets

- DDR_CLKFB trace length must equal the other DDR_CLKn's

Critical Placement:
Place Parallel Termination at DDR end of net (TL5) per Layout Example

CRITICAL PLACEMENT AND ROUTING:
All Components, and signals on this page have very tight and critical routing and placement parameters:
(IDEAL Layout)
All clocks = each other = data lines = control = address
In other words all signals equal each other.
Place series resistors and compensation capacitors close to the DDR2 devices (TL1 is much smaller than TL0). Place termination resistors on the top layer at VTT island, at end of bus. Use wide island trace to increase current capacity (3A).
Route DDR2 signals only on layers that are directly adjacent to the designated reference plane: GND for DQ,DM,DQS; VDD for ADD.
Route each 10-bit byte lane of the data group (DQ, DQS, and DM) on the same layers with matched trace lengths (within +/- 25 mils of the respective strobe, DQS). Vias and BGA breakout patterns should be included in the analysis of each individual trace length. Include 1.6mm net length per via.
To help reduce crosstalk, data and data strobes should be isolated from the address and command signals. This is accomplished by routing different signal types on separate layers of the printed circuit board.
Total trace lengths for any signal, CPU to DRAM must not exceed 100 mm. Separate data and control nets by a minimum of 0.5 mm to minimize crosstalk.

Refer to:
JEDEC "PC2-4200/PC2-3200 DDR2 Unbuffered MicroDIMM Reference Design Specification" Rev 0.5 4/26/04
Micron TN-47-01 "DDR2 Design Guide for Two-DIMM System"
DDR devices should be placed and routed in an analogous fashion to optimize signal fan-out.



U1
440EPX
Gig-Ethernet RGMII0
ETHERNET Mgt.
GMC0_TXD0
GMC0_TXD1
GMC0_TXD2
GMC0_TXD3
GMC0_TXCTL
GMC0_TXCLK
GMCTXCLK
GMC0_RXD0
GMC0_RXD1
GMC0_RXD2
GMC0_RXD3
GMC0_RXCTL
GMC0_RXCLK
REJECTPKT0
REJECTPKT1
GMCMDCLK
GMCMDIO
GMCREFCLK
NC
R153
1K
U24
DP83865DVH
2V5
1V8
C331
10NF
C332
10NF
Place nearest PHY pin 96
Place nearest PHY pin 101
C334
22UF
C309
10NF
Place nearest PHY pin 98
C333
22UF
C310
10NF
Place nearest PHY pin 100
C324
C325
C323
C326
C328
C327
C329
C330
10NF
100NF
Place as close to PHY CORE VDD power pins as possible
C311
C312
C313
C314
C315
C316
C317
C318
C319
C320
C321
C322
Place as close to PHY IO VDD power pins as possible
R140
R141
R143
R142
R144
R145
R146
R147
49.9R
C305
C306
C307
C308
MDI0_0P
MDI0_0N
MDI0_1P
MDI0_1N
MDI0_2P
MDI0_2N
MDI0_3P
MDI0_3N
J2
HFJ11-1G02E-L12
VCC
GND
MNT1
MNT2
CASE1
CASE2
TD0P
TD0N
TD1P
TD2P
TD2N
TD1N
TD3P
TD3N
GRN
YEL
C335
22UF
CHASSIS_GND
R152
2K2
NOSTUFF
R151
2K2
R150
2K2
R139
5K76
JP5
JP6
JP7
JP8
JP9
JP10
JP11
JP12
JP13
JP14
JP15
JP16
JP17
JP18
JP19
JP20
DUPLEX LED
L10 LED
L100 LED
STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.
Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place jumers in line with signals

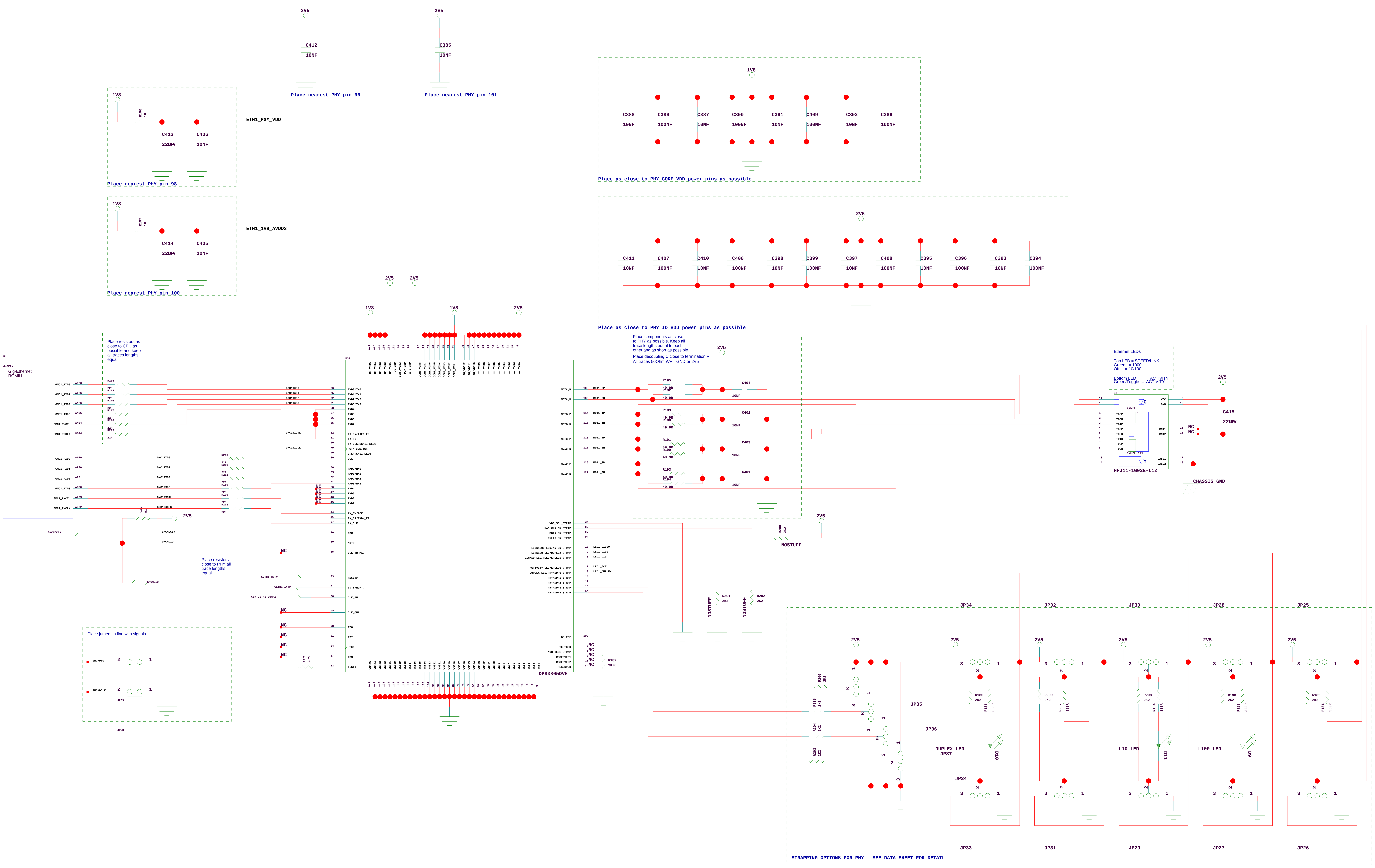
Place components as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible.

Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5

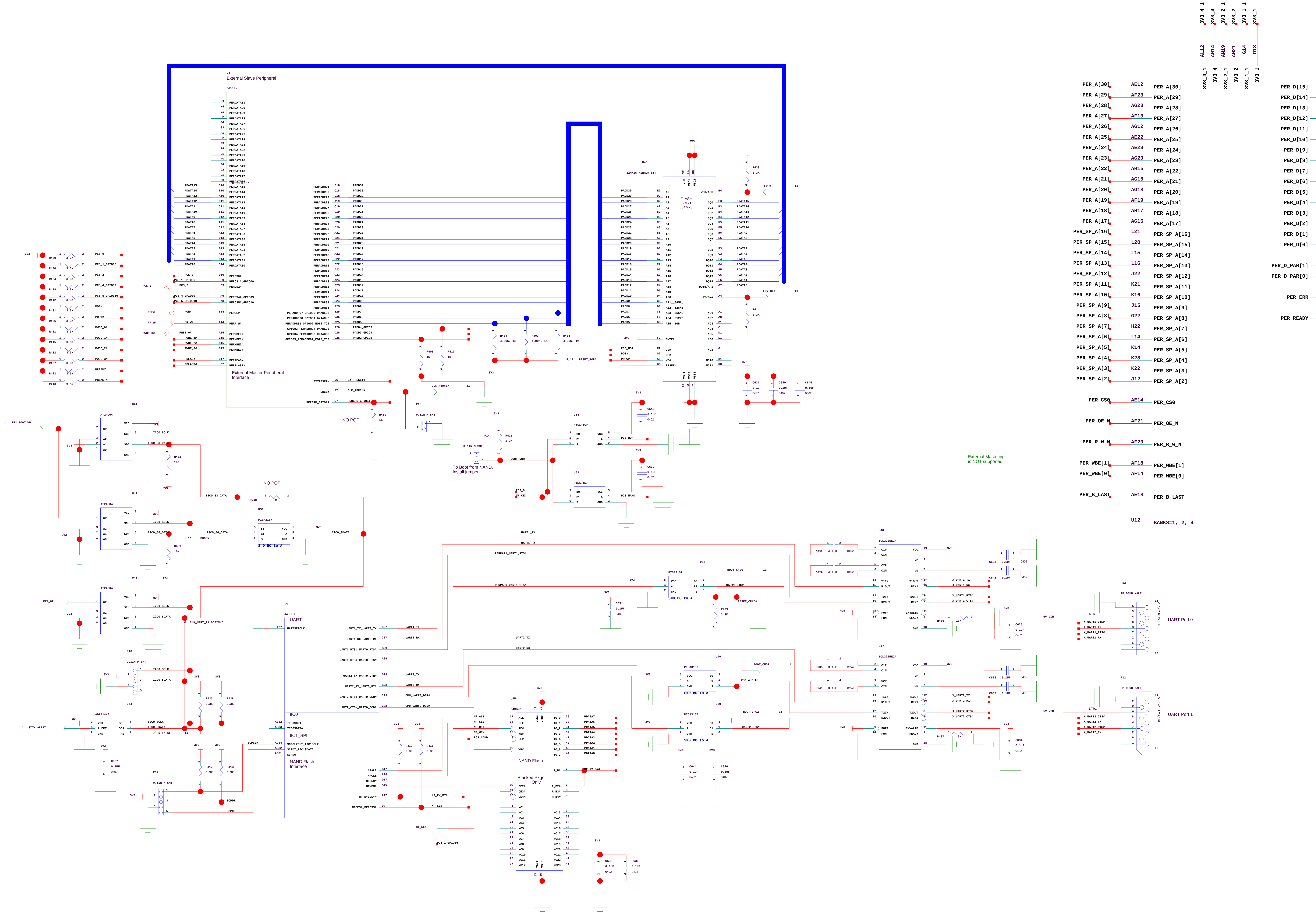
Ethernet LEDs

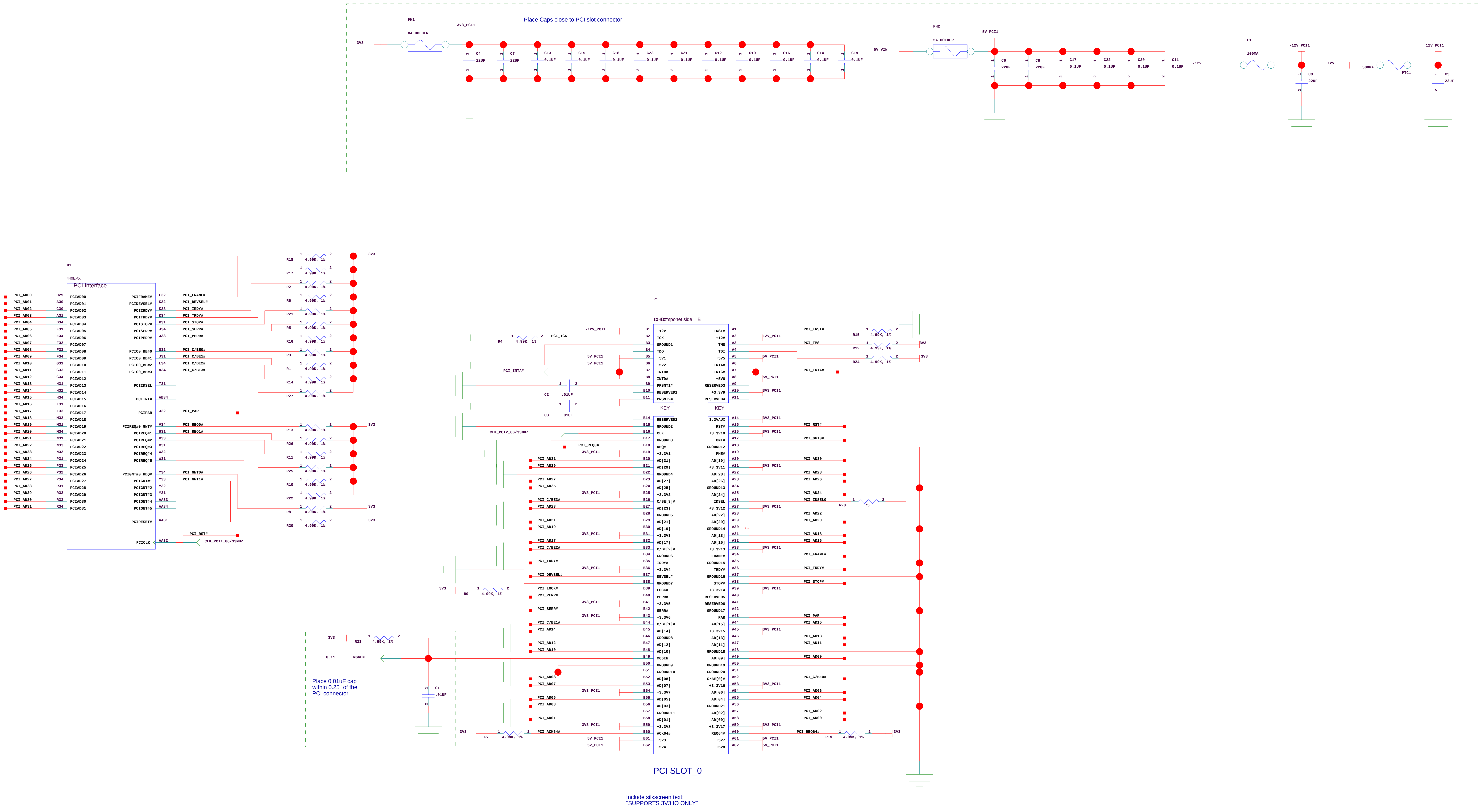
Top LED = SPEED/LINK
Green = 1000
Off = 10/100

Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY



2V5
C412
10NF
Place nearest PHY pin 96
C385
Place nearest PHY pin 101
1V8
R196
C413
22UF
C406
10NF
ETH1_PGM_VDD
Place nearest PHY pin 98
R197
C414
C405
ETH1_1V8_AVDD3
Place nearest PHY pin 100
C388
C389
C387
C390
C391
C409
C392
C386
100NF
Place as close to PHY CORE VDD power pins as possible
C411
C407
C410
C400
C398
C399
C397
C408
C395
C396
C393
C394
Place as close to PHY IO VDD power pins as possible
Place resistors as close to CPU as possible and keep all traces lengths equal
Gig-Ethernet RGMII1
GMC1_TXD0
GMC1_TXD1
GMC1_TXD2
GMC1_TXD3
GMC1_TXCTL
GMC1_TXCLK
GMC1_RXD0
GMC1_RXD1
GMC1_RXD2
GMC1_RXD3
GMC1_RXCTL
GMC1_RXCLK
GMCMDCLK
GMCMDIO
Place resistors close to PHY all trace lengths equal
ETH1_RSTn
ETH1_INTn
CLK_GETH1_25MHZ
Place jumers in line with signals
JP38
JP39
U21
DP83865DVH
TXD0/TX0
TXD1/TX1
TXD2/TX2
TXD3/TX3
TX_EN/TXEN_ER
GTX_CLK/TCK
RXD0/RX0
RXD1/RX1
RXD2/RX2
RXD3/RX3
RX_DV/RCK
RX_CLK
MDC
MDIO
CLK_TO_MAC
RESETn
INTERRUPTn
CLK_IN
CLK_OUT
TDO
TDI
TCK
TMS
TRSTn
NC
MDIA_P
MDIA_N
MDIB_P
MDIB_N
MDIC_P
MDIC_N
MDID_P
MDID_N
VDD_SEL_STRAP
MAC_CLK_EN_STRAP
MDIX_EN_STRAP
MULTI_EN_STRAP
LINK1000_LED/AN_EN_STRAP
LINK100_LED/DUPLEX_STRAP
LINK10_LED/RLED/SPEED1_STRAP
ACTIVITY_LED/SPEED0_STRAP
DUPLEX_LED/PHYADDR0_STRAP
PHYADDR1_STRAP
PHYADDR2_STRAP
PHYADDR3_STRAP
PHYADDR4_STRAP
BG_REF
R187
9K76
Place components as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible
Place decoupling C close to termination R All traces 50Ohm WRT GND or 2V5
R195
R190
R189
R188
R191
R192
R193
R194
49.9R
C404
C402
C403
C401
R200
2K2
NOSTUFF
R201
R202
Ethernet LEDs
Top LED = SPEED/LINK
Green = 1000
Off = 10/100
Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY
GRN
YEL
HFJ11-1G02E-L12
C415
CHASSIS_GND
JP34
JP32
JP30
JP28
JP25
JP35
JP36
DUPLEX LED
JP37
JP24
L10 LED
L100 LED
D10
D11
D9
R186
R185
R209
R207
R208
R184
R199
R183
R182
R181
330R
JP33
JP31
JP29
JP27
JP26
STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL


External Slave Peripheral
External Master Peripheral Interface
NO POP
FLASH 32Mx16 /64Mx8
To Boot from NAND, Install jumper
S=0 B0 to A
UART
IIC0
IIC1_SPI
NAND Flash Interface
NAND Flash
Stacked Pkgs Only
UART Port 0
UART Port 1
External Mastering is NOT supported
3V3_4_1
3V3_4
3V3_2_1
3V3_2
3V3_1_1
3V3_1
AL12
AG14
AM19
AH21
G14
D13
PER_A[30] AE12
PER_A[29] AF23
PER_A[28] AG23
PER_A[27] AF13
PER_A[26] AG12
PER_A[25] AE22
PER_A[24] AE23
PER_A[23] AG20
PER_A[22] AH15
PER_A[21] AG15
PER_A[20] AG18
PER_A[19] AF19
PER_A[18] AH17
PER_A[17] AG16
PER_SP_A[16] L21
PER_SP_A[15] L20
PER_SP_A[14] L15
PER_SP_A[13] L16
PER_SP_A[12] J22
PER_SP_A[11] K21
PER_SP_A[10] K16
PER_SP_A[9] J15
PER_SP_A[8] G22
PER_SP_A[7] H22
PER_SP_A[6] L14
PER_SP_A[5] K14
PER_SP_A[4] K23
PER_SP_A[3] K22
PER_SP_A[2] J12
PER_CS0 AE14
PER_OE_N AF21
PER_R_W_N AF20
PER_WBE[1] AF18
PER_WBE[0] AF14
PER_B_LAST AE18
PER_D[15] AF15
PER_D[14] AE16
PER_D[13] AE21
PER_D[12] AD20
PER_D[11] AF16
PER_D[10] AE17
PER_D[9] AE19
PER_D[8] AD19
PER_D[7] AG22
PER_D[6] AH22
PER_D[5] AH12
PER_D[4] AG13
PER_D[3] AH20
PER_D[2] AH19
PER_D[1] AH14
PER_D[0] AH13
PER_D_PAR[1] AG21
PER_D_PAR[0] AE13
PER_ERR AG17
PER_READY AH18
U12
BANKS=1, 2, 4


Place Caps close to PCI slot connector
FH1
5A HOLDER
3V3
3V3_PCI1
C4 22UF
C7 22UF
C13 0.1UF
C15 0.1UF
C18 0.1UF
C23 0.1UF
C21 0.1UF
C12 0.1UF
C10 0.1UF
C16 0.1UF
C14 0.1UF
C19 0.1UF
FH2
5A HOLDER
5V_VIN
5V_PCI1
C6 22UF
C8 22UF
C17 0.1UF
C22 0.1UF
C20 0.1UF
C11 0.1UF
F1
100MA
-12V
-12V_PCI1
C9 22UF
12V
500MA
PTC1
12V_PCI1
C5 22UF
U1
440EPX
PCI Interface
R18 4.99K, 1%
R17 4.99K, 1%
PCI_FRAME#
PCI_DEVSEL#
PCI_IRDY#
PCI_TRDY#
PCI_STOP#
PCI_SERR#
PCI_PERR#
PCI_C/BE0#
PCI_C/BE1#
PCI_C/BE2#
PCI_C/BE3#
PCI_PAR
PCI_REQ0#
PCI_REQ1#
PCI_GNT0#
PCI_GNT1#
PCI_RST#
CLK_PCI1_66/33MHZ
P1
32-Bit Component side = B
-12V_PCI1
PCI_TCK
PCI_INTA#
C2 .01UF
C3 .01UF
KEY
CLK_PCI2_66/33MHZ
PCI_TRST#
PCI_TMS
R15 4.99K, 1%
R12 4.99K, 1%
R24 4.99K, 1%
R28 75
R19 4.99K, 1%
R7 4.99K, 1%
R9 4.99K, 1%
PCI_ACK64#
PCI_REQ64#
PCI_IDSEL0
3V3
R23 4.99K, 1%
6,11
M66EN
C1 .01UF
Place 0.01uF cap within 0.25" of the PCI connector
PCI SLOT_0
Include silkscreen text: "SUPPORTS 3V3 IO ONLY"

Optional PRSNT signals are not used, max 25W is available

PRSNT1#	PRSNT2#	Expansion Configuration
Open	Open	No expansion board present
Ground	Open	Expansion board present, 25 W maximum
Open	Ground	Expansion board present, 15 W maximum
Ground	Ground	Expansion board present, 7.5 W maximum

KAROO ARRAY TELESCOPE, NRF
UNIT 12, LONSDALE BUILDING
LONSDALE WAY, PINELANDS, 7405
SOUTH AFRICA

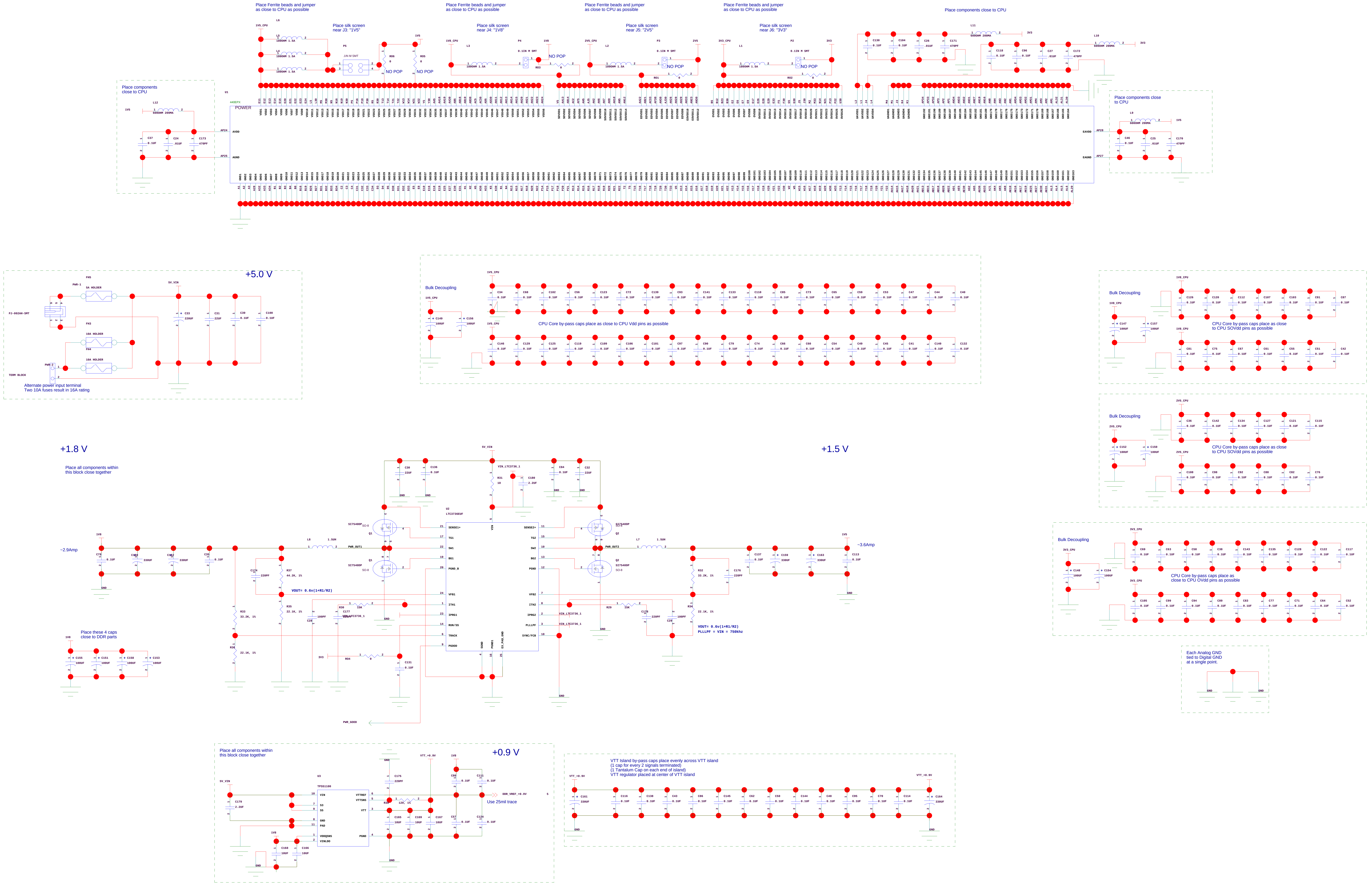
TITLE
ROACH_PPC_PCI

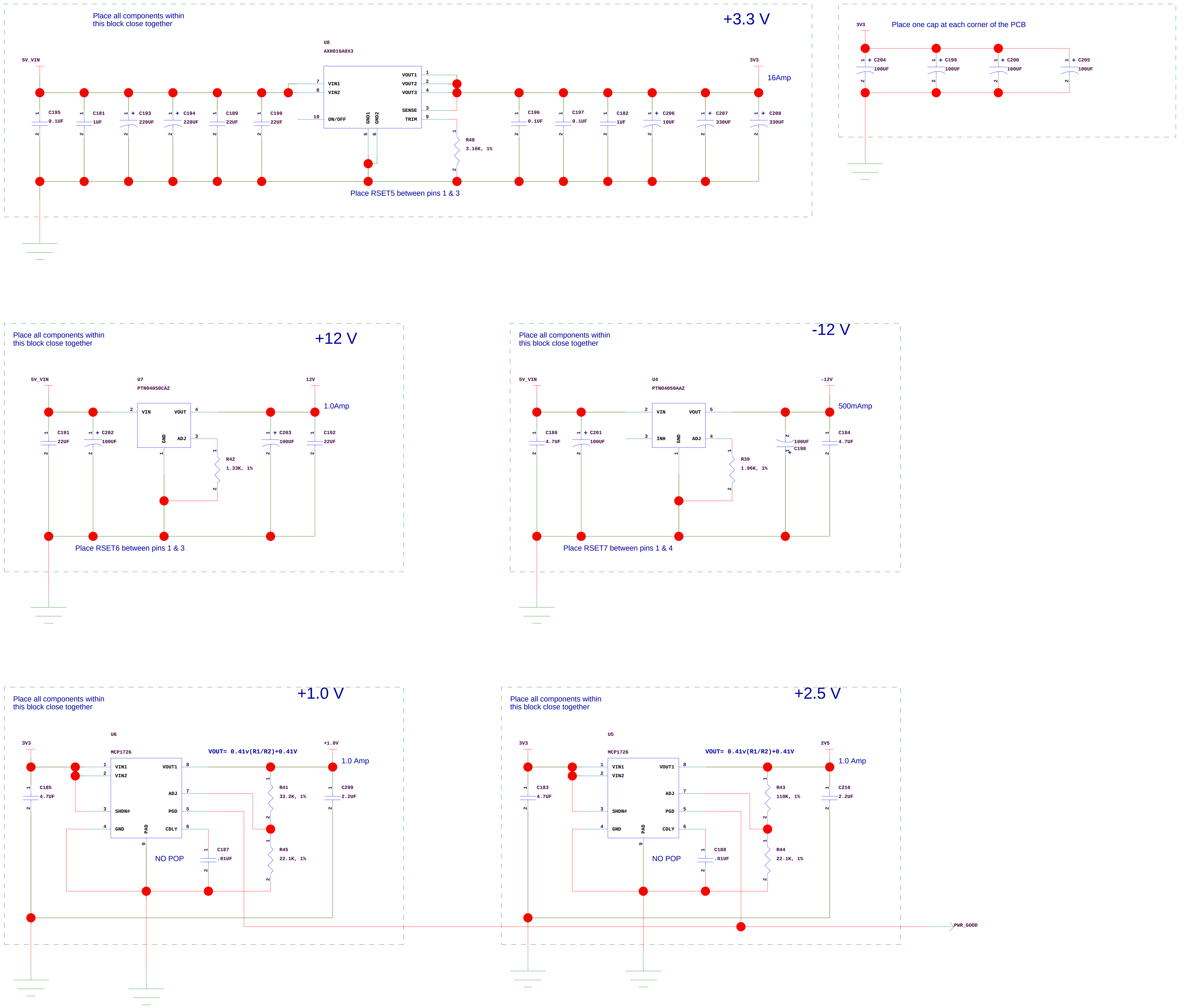
CHECKED BY
<PUT NAME HERE>

DRAWN BY
<PUT NAME HERE>

SIZE A2
DWG NO <PUT DRAWING NUMBER HERE>
REV 0

SCALE NTS
SHEET 1 of 1
9-7-2007_16:22


Place Ferrite beads and jumper as close to CPU as possible
Place silk screen near J3: "1V5"
Place silk screen near J4: "1V8"
Place silk screen near J5: "2V5"
Place silk screen near J6: "3V3"
Place components close to CPU
NO POP
1800HM 1.5A
6000HM 200MA
0.1IN M SMT
U1
440EPX
POWER
AVDD
AGND
EAVDD
EAGND
Place components close to CPU
+5.0 V
5A HOLDER
10A HOLDER
5V_VIN
C33 220UF
C31 22UF
C39 0.1UF
C100 0.1UF
Alternate power input terminal
Two 10A fuses result in 16A rating
Bulk Decoupling
1V5_CPU
C149 100UF
C156 100UF
CPU Core by-pass caps place as close to CPU Vdd pins as possible
1V8_CPU
C147 100UF
C157 100UF
CPU Core by-pass caps place as close to CPU SOVdd pins as possible
2V5_CPU
C152 100UF
C150 100UF
CPU Core by-pass caps place as close to CPU SOVdd pins as possible
3V3_CPU
C148 100UF
C154 100UF
CPU Core by-pass caps place as close to CPU OVdd pins as possible
Each Analog GND tied to Digital GND at a single point.
+1.8 V
Place all components within this block close together
~2.9Amp
U2
LTC3736EUF
SI7540DP
SO-8
L8 1.5UH
PWR_OUT1
VOUT= 0.6v(1+R1/R2)
R37 44.2K, 1%
R35 22.1K, 1%
R33 33.2K, 1%
R36 22.1K, 1%
Place these 4 caps close to DDR parts
C155 100UF
C151 100UF
C158 100UF
C153 100UF
PWR_GOOD
+1.5 V
~3.6Amp
L7 1.5UH
PWR_OUT2
R32 33.2K, 1%
R34 22.1K, 1%
VOUT= 0.6v(1+R1/R2)
PLLLPF = VIN = 750khz
+0.9 V
Place all components within this block close together
U3
TPS51100
DDR_VREF_+0.9V
Use 25mil trace
VTT_+0.9V
VTT Island by-pass caps place evenly across VTT island
(1 cap for every 2 signals terminated)
(1 Tantalum Cap on each end of island)
VTT regulator placed at center of VTT island
C161 330UF
C164 330UF
GND


+3.3 V
Place all components within this block close together
U8
AXH016A0X3
5V_VIN
VIN1
VIN2
ON/OFF
GND1
GND2
VOUT1
VOUT2
VOUT3
SENSE
TRIM
3V3
16Amp
C195 0.1UF
C181 1UF
C193 220UF
C194 220UF
C189 22UF
C190 22UF
R40 3.16K, 1%
C196 0.1UF
C197 0.1UF
C182 1UF
C206 10UF
C207 330UF
C208 330UF
Place RSET5 between pins 1 & 3
3V3
Place one cap at each corner of the PCB
C204 100UF
C199 100UF
C200 100UF
C205 100UF
+12 V
Place all components within this block close together
5V_VIN
U7
PTN04050CAZ
VIN
VOUT
GND
ADJ
12V
1.0Amp
C191 22UF
C202 100UF
R42 1.33K, 1%
C203 100UF
C192 22UF
Place RSET6 between pins 1 & 3
-12 V
Place all components within this block close together
5V_VIN
U4
PTN04050AAZ
VIN
INH
GND
VOUT
ADJ
-12V
500mAmp
C186 4.7UF
C201 100UF
R39 1.96K, 1%
100UF C198
C184 4.7UF
Place RSET7 between pins 1 & 4
+1.0 V
Place all components within this block close together
3V3
U6
MCP1726
VIN1
VIN2
SHDN#
GND
PAD
VOUT1
ADJ
PGD
CDLY
VOUT= 0.41v(R1/R2)+0.41V
+1.0V
1.0 Amp
C185 4.7UF
R41 33.2K, 1%
C209 2.2UF
NO POP
C187 .01UF
R45 22.1K, 1%
+2.5 V
Place all components within this block close together
3V3
U5
MCP1726
VIN1
VIN2
SHDN#
GND
PAD
VOUT1
ADJ
PGD
CDLY
VOUT= 0.41v(R1/R2)+0.41V
2V5
1.0 Amp
C183 4.7UF
R43 110K, 1%
C210 2.2UF
NO POP
C188 .01UF
R44 22.1K, 1%
PWR_GOOD

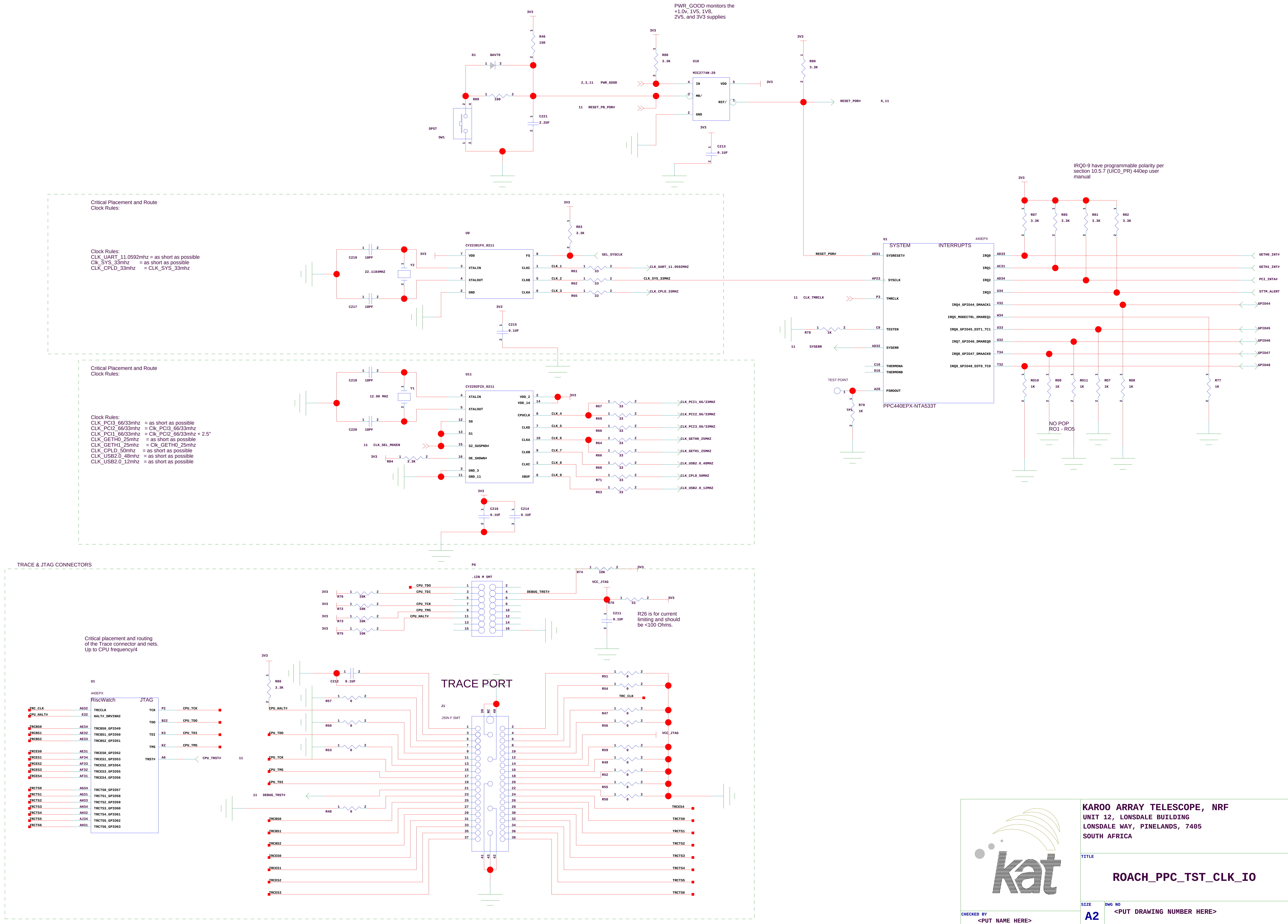
KAROO ARRAY TELESCOPE, NRF
UNIT 12, LONSDALE BUILDING
LONSDALE WAY, PINELANDS, 7405
SOUTH AFRICA

TITLE
ROACH_PPC_POWER_2

SIZE A2	DWG NO <PUT DRAWING NUMBER HERE>	REV 0
SCALE NTS	SHEET 1 of 1	9-7-2007_16:22

CHECKED BY
<PUT NAME HERE>

DRAWN BY
<PUT NAME HERE>


3V3
R46
15K
D1
BAV70
R89
100
SPST
SW1
C221
2.2UF
2,3,11 PWR_GOOD
11 RESET_PB_POR#
R88
3.3K
U10
MIC2774N-29
IN
VDD
MR/
RST/
GND
C213
0.1UF
R80
3.3K
RESET_POR#
6,11
U9
CY22381FX_0211
C219
18PF
C217
18PF
22.1184MHZ
Y2
VDD
XTALIN
XTALOUT
GND
FS
CLKC
CLKB
CLKA
R83
3.3K
SEL_SYSCLK
CLK_1
CLK_2
CLK_3
R61
R62
R65
33
CLK_UART_11.0592MHZ
CLK_SYS_33MHZ
CLK_CPLD_33MHZ
C215
0.1UF
U11
CY2292FZX_0211
C218
18PF
C220
18PF
12.00 MHZ
Y1
XTALIN
XTALOUT
S0
S1
S2_SUSPND#
OE_SHDWN#
GND_3
GND_11
VDD_2
VDD_14
CPUCLK
CLKD
CLKA
CLKB
CLKC
XBUF
11 CLK_SEL_M66EN
R84
3.3K
CLK_4
CLK_5
CLK_6
CLK_7
CLK_8
CLK_9
R67
R69
R60
R64
R66
R68
R71
R63
CLK_PCI1_66/33MHZ
CLK_PCI2_66/33MHZ
CLK_PCI3_66/33MHZ
CLK_GETH0_25MHZ
CLK_GETH1_25MHZ
CLK_USB2.0_48MHZ
CLK_CPLD_50MHZ
CLK_USB2.0_12MHZ
C216
0.1UF
C214
0.1UF
U1
440EPX
SYSTEM
INTERRUPTS
SYSRESET#
SYSCLK
TMRCLK
TESTEN
SYSERR
THERMONA
THERMONB
PSROOUT
IRQ0
IRQ1
IRQ2
IRQ3
IRQ4_GPIO44_DMAACK1
IRQ5_MODECTRL_DMAREQ1
IRQ6_GPIO45_EOT1_TC1
IRQ7_GPIO46_DMAREQ0
IRQ8_GPIO47_DMAACK0
IRQ9_GPIO48_EOT0_TC0
PPC440EPX-NTA533T
11 CLK_TMRCLK
R78
1K
11 SYSERR
TEST POINT
TP1
R79
1K
R87
R85
R81
R82
3.3K
GETH0_INT#
GETH1_INT#
PCI_INTA#
STTM_ALERT
GPIO44
GPIO45
GPIO46
GPIO47
GPIO48
RO10
RO9
RO11
RO7
RO8
R77
1K
P6
.1IN M SMT
CPU_TDO
CPU_TDI
CPU_TCK
CPU_TMS
CPU_HALT#
DEBUG_TRST#
R76
R72
R73
R75
10K
R74
10K
VCC_JTAG
R70
33
C211
0.1UF
U1
440EPX
RiscWatch
JTAG
TRCLK
HALT#_DRVINH2
TRCBS0_GPIO49
TRCBS1_GPIO50
TRCBS2_GPIO51
TRCES0_GPIO52
TRCES1_GPIO53
TRCES2_GPIO54
TRCES3_GPIO55
TRCES4_GPIO56
TRCTS0_GPIO57
TRCTS1_GPIO58
TRCTS2_GPIO59
TRCTS3_GPIO60
TRCTS4_GPIO61
TRCTS5_GPIO62
TRCTS6_GPIO63
TCK
TDO
TDI
TMS
TRST#
CPU_TRST#
R86
3.3K
C212
0.1UF
R57
R50
R53
R48
J1
.25IN F SMT
R51
R54
TRC_CLK
R47
R56
R59
R49
R52
R55
R58
TRCES4
TRCTS0
TRCTS1
TRCTS2
TRCTS3
TRCTS4
TRCTS5
TRCTS6
TRCBS0
TRCBS1
TRCBS2
TRCES0
TRCES1
TRCES2
TRCES3
11 DEBUG_TRST#

PWR_GOOD monitors the
+1.0v, 1V5, 1V8,
2V5, and 3V3 supplies

IRQ0-9 have programmable polarity per
section 10.5.7 (UIC0_PR) 440ep user
manual

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_SYS_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible

NO POP
RO1 - RO5

TRACE & JTAG CONNECTORS

R26 is for current
limiting and should
be <100 Ohms.

Critical placement and routing
of the Trace connector and nets.
Up to CPU frequency/4

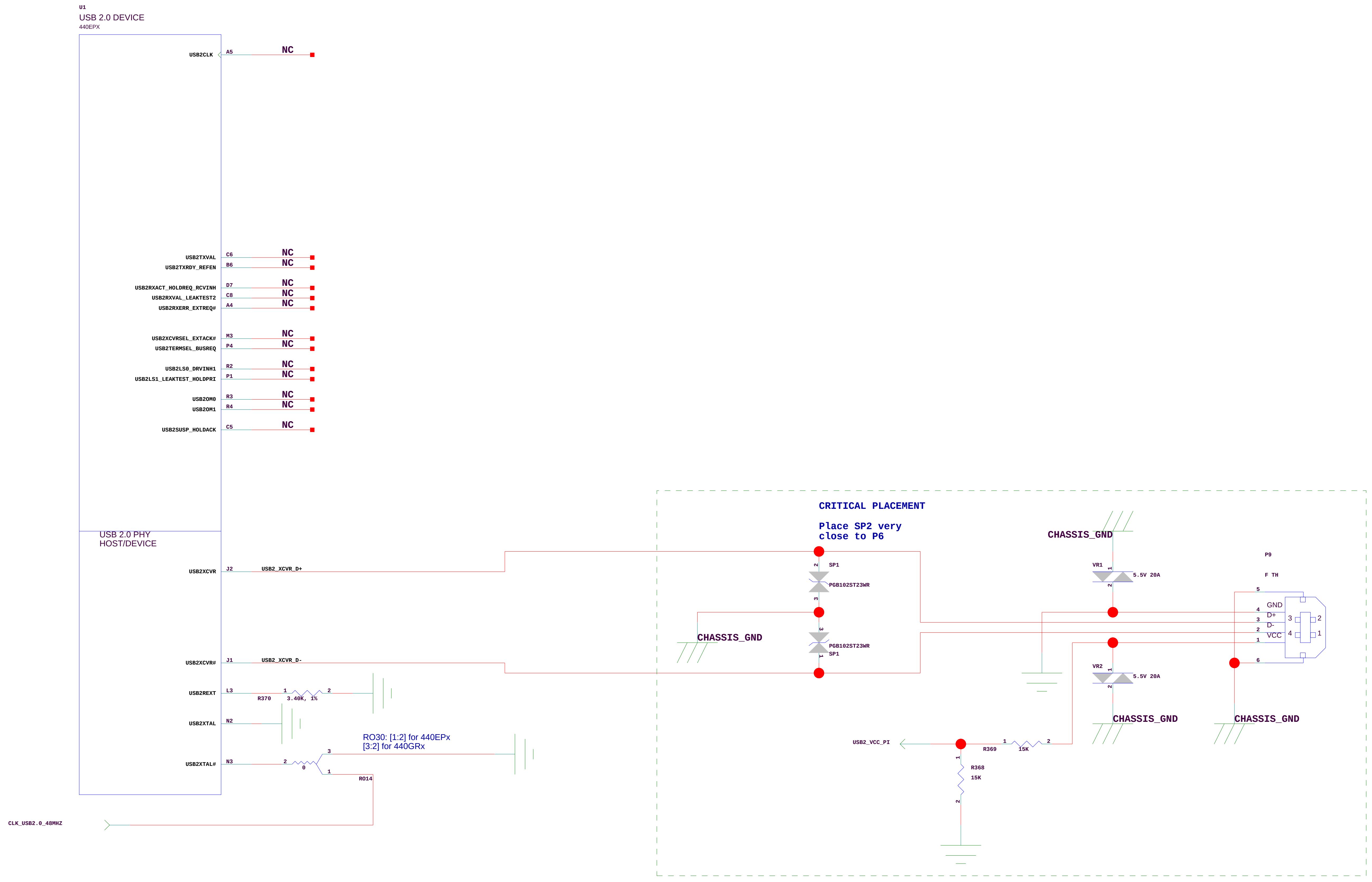
TRACE PORT

KAROO ARRAY TELESCOPE, NRF
UNIT 12, LONSDALE BUILDING
LONSDALE WAY, PINELANDS, 7405
SOUTH AFRICA

TITLE
ROACH_PPC_TST_CLK_IO

SIZE A2
DWG NO <PUT DRAWING NUMBER HERE>
REV 0

CHECKED BY <PUT NAME HERE>
DRAWN BY <PUT NAME HERE>
SCALE NTS
SHEET 1 of 1
9-7-2007_16:22


U1
USB 2.0 DEVICE
440EPX
USB2CLK
A5
NC
USB2TXVAL
C6
NC
USB2TXRDY_REFEN
B6
NC
USB2RXACT_HOLDREQ_RCVINH
D7
NC
USB2RXVAL_LEAKTEST2
C8
NC
USB2RXERR_EXTREQ#
A4
NC
USB2XCVRSEL_EXTACK#
M3
NC
USB2TERMSEL_BUSREQ
P4
NC
USB2LS0_DRVINH1
R2
NC
USB2LS1_LEAKTEST_HOLDPRI
P1
NC
USB2OM0
R3
NC
USB2OM1
R4
NC
USB2SUSP_HOLDACK
C5
NC
USB 2.0 PHY
HOST/DEVICE
USB2XCVR
J2
USB2_XCVR_D+
USB2XCVR#
J1
USB2_XCVR_D-
USB2REXT
L3
1
2
R370
3.40K, 1%
USB2XTAL
N2
USB2XTAL#
N3
2
0
3
1
RO14
CLK_USB2.0_48MHZ
2
SP1
PGB102ST23WR
3
3
PGB102ST23WR
SP1
1
CHASSIS_GND
CHASSIS_GND
VR1
1
2
5.5V 20A
VR2
1
2
5.5V 20A
CHASSIS_GND
CHASSIS_GND
P9
F TH
5
4
3
2
1
6
GND
D+
D-
VCC
3
4
2
1
USB2_VCC_PI
1
2
R369
15K
1
R368
15K
2

RO30: [1:2] for 440EPx
[3:2] for 440GRx

CRITICAL PLACEMENT

Place SP2 very
close to P6

KAROO ARRAY TELESCOPE, NRF
UNIT 12, LONSDALE BUILDING
LONSDALE WAY, PINELANDS, 7405
SOUTH AFRICA

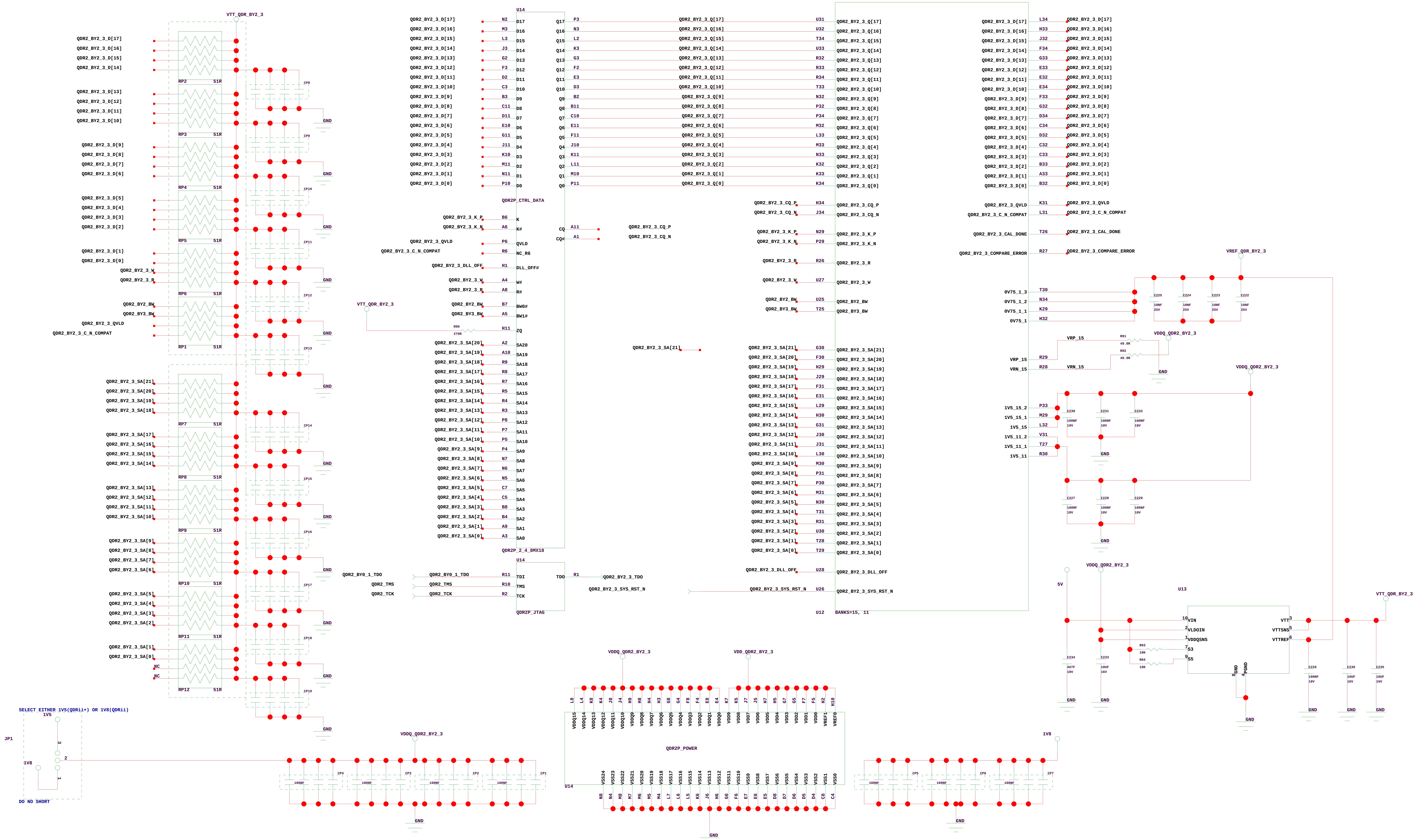
TITLE
ROACH_PPC_USB

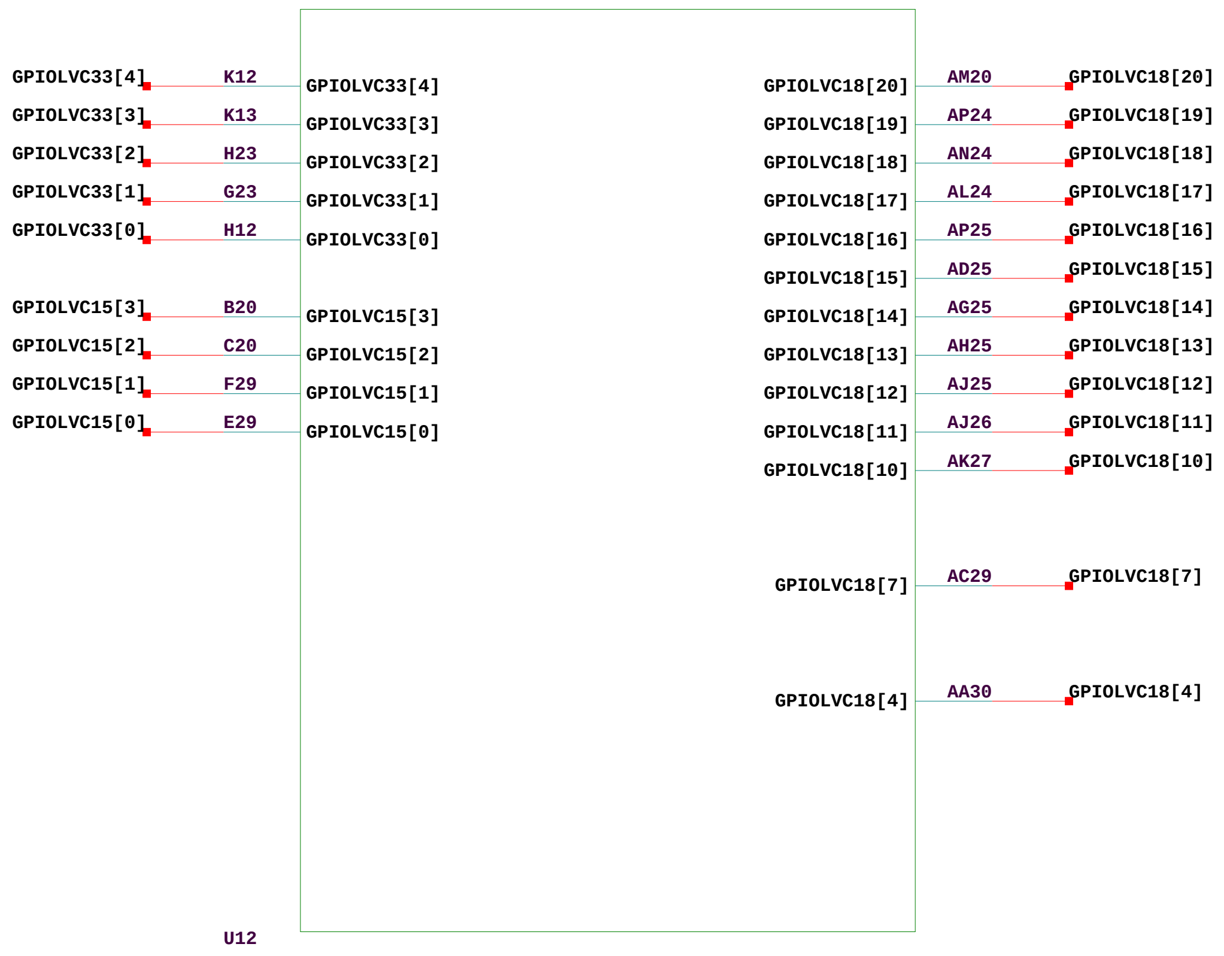
SIZE A2
DWG NO <PUT DRAWING NUMBER HERE>
REV 0

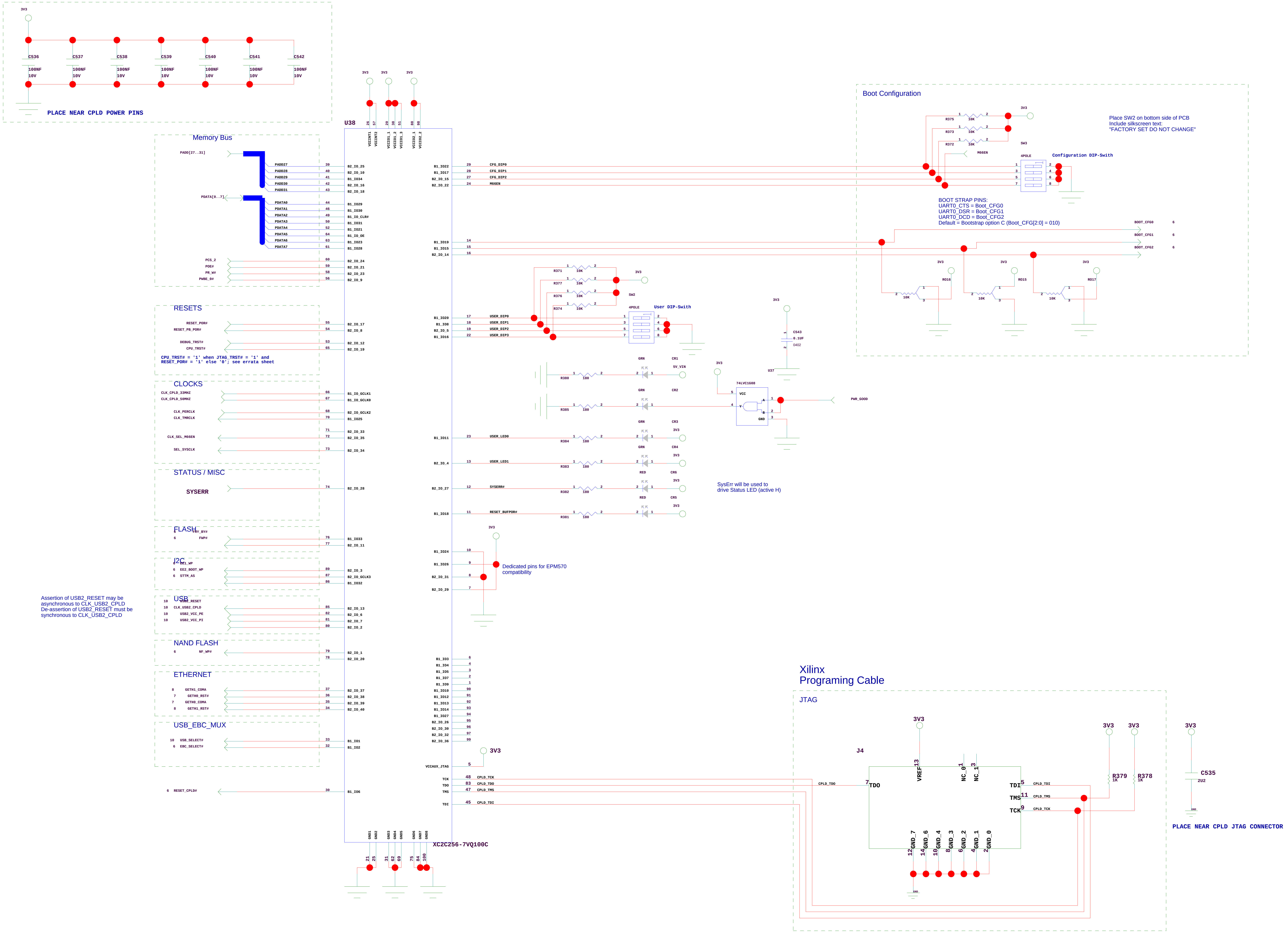
CHECKED BY
<PUT NAME HERE>

DRAWN BY
<PUT NAME HERE>

SCALE NTS
SHEET 1 of 1
9-7-2007_16:22


VTT_QDR_BY2_3
RP1 51R
RP2 51R
RP3 51R
RP4 51R
RP5 51R
RP6 51R
RP7 51R
RP8 51R
RP9 51R
RP10 51R
RP11 51R
RP12 51R
CP8
CP9
CP10
CP11
CP12
CP13
CP14
CP15
CP16
CP17
CP18
CP19
GND
QDR2_BY2_3_D[17]
QDR2_BY2_3_D[16]
QDR2_BY2_3_D[15]
QDR2_BY2_3_D[14]
QDR2_BY2_3_D[13]
QDR2_BY2_3_D[12]
QDR2_BY2_3_D[11]
QDR2_BY2_3_D[10]
QDR2_BY2_3_D[9]
QDR2_BY2_3_D[8]
QDR2_BY2_3_D[7]
QDR2_BY2_3_D[6]
QDR2_BY2_3_D[5]
QDR2_BY2_3_D[4]
QDR2_BY2_3_D[3]
QDR2_BY2_3_D[2]
QDR2_BY2_3_D[1]
QDR2_BY2_3_D[0]
QDR2_BY2_3_W
QDR2_BY2_3_R
QDR2_BY2_BW
QDR2_BY3_BW
QDR2_BY2_3_QVLD
QDR2_BY2_3_C_N_COMPAT
QDR2_BY2_3_SA[21]
QDR2_BY2_3_SA[20]
QDR2_BY2_3_SA[19]
QDR2_BY2_3_SA[18]
QDR2_BY2_3_SA[17]
QDR2_BY2_3_SA[16]
QDR2_BY2_3_SA[15]
QDR2_BY2_3_SA[14]
QDR2_BY2_3_SA[13]
QDR2_BY2_3_SA[12]
QDR2_BY2_3_SA[11]
QDR2_BY2_3_SA[10]
QDR2_BY2_3_SA[9]
QDR2_BY2_3_SA[8]
QDR2_BY2_3_SA[7]
QDR2_BY2_3_SA[6]
QDR2_BY2_3_SA[5]
QDR2_BY2_3_SA[4]
QDR2_BY2_3_SA[3]
QDR2_BY2_3_SA[2]
QDR2_BY2_3_SA[1]
QDR2_BY2_3_SA[0]
NC
NC
U14
QDR2P_CTRL_DATA
QDR2_BY2_3_K_P
QDR2_BY2_3_K_N
QDR2_BY2_3_DLL_OFF
VTT_QDR_BY2_3
R90
270R
ZQ
QDR2P_2_4_SMX18
QDR2_BY2_3_CQ_P
QDR2_BY2_3_CQ_N
QDR2_BY2_3_Q[17]
QDR2_BY2_3_Q[0]
QDR2P_JTAG
QDR2_BY0_1_TDO
QDR2_TMS
QDR2_TCK
TDI
TMS
TCK
TDO
QDR2_BY2_3_TDO
QDR2_BY2_3_SYS_RST_N
U12
BANKS=15, 11
QDR2_BY2_3_CAL_DONE
QDR2_BY2_3_COMPARE_ERROR
VREF_QDR_BY2_3
0V75_1_3
0V75_1_2
0V75_1_1
0V75_1
C225 C224 C223 C222
10NF 25V
VRP_15
VRN_15
R91 49.9R
R92 49.9R
VDDQ_QDR2_BY2_3
1V5_15_2
1V5_15_1
1V5_15
1V5_11_2
1V5_11_1
1V5_11
C230 C231 C232
C227 C228 C229
100NF 16V
U13
5V
VIN
VLDOIN
VDDQSNS
S3
S5
GND
PGND
VTT
VTTSNS
VTTREF
R93 10K
R94 10K
C234 4U7F 16V
C233 10UF 16V
C226 100NF 16V
C236 10UF 16V
C235 10UF 16V
VTT_QDR_BY2_3
VDDQ_QDR2_BY2_3
VDD_QDR2_BY2_3
QDR2P_POWER
VDDQ15 … VDDQ0
VDD9 … VDD0
VREF1
VREF0
VSS24 … VSS0
SELECT EITHER 1V5(QDRii+) OR 1V8(QDRii)
1V5
1V8
JP1
DO NO SHORT
CP1
CP2
CP3
CP4
CP5
CP6
CP7
100NF
1V8


GPIOLVC33[4]
K12
GPIOLVC33[4]
GPIOLVC33[3]
K13
GPIOLVC33[3]
GPIOLVC33[2]
H23
GPIOLVC33[2]
GPIOLVC33[1]
G23
GPIOLVC33[1]
GPIOLVC33[0]
H12
GPIOLVC33[0]
GPIOLVC15[3]
B20
GPIOLVC15[3]
GPIOLVC15[2]
C20
GPIOLVC15[2]
GPIOLVC15[1]
F29
GPIOLVC15[1]
GPIOLVC15[0]
E29
GPIOLVC15[0]
GPIOLVC18[20]
AM20
GPIOLVC18[20]
GPIOLVC18[19]
AP24
GPIOLVC18[19]
GPIOLVC18[18]
AN24
GPIOLVC18[18]
GPIOLVC18[17]
AL24
GPIOLVC18[17]
GPIOLVC18[16]
AP25
GPIOLVC18[16]
GPIOLVC18[15]
AD25
GPIOLVC18[15]
GPIOLVC18[14]
AG25
GPIOLVC18[14]
GPIOLVC18[13]
AH25
GPIOLVC18[13]
GPIOLVC18[12]
AJ25
GPIOLVC18[12]
GPIOLVC18[11]
AJ26
GPIOLVC18[11]
GPIOLVC18[10]
AK27
GPIOLVC18[10]
GPIOLVC18[7]
AC29
GPIOLVC18[7]
GPIOLVC18[4]
AA30
GPIOLVC18[4]
U12


3V3
C536
C537
C538
C539
C540
C541
C542
100NF
10V
PLACE NEAR CPLD POWER PINS
U38
VCCINT1
VCCINT2
VCCIO1_1
VCCIO1_2
VCCIO1_3
VCCIO2_1
VCCIO2_2
Memory Bus
PADD[27..31]
PADD27
PADD28
PADD29
PADD30
PADD31
PDATA[0..7]
PDATA0
PDATA1
PDATA2
PDATA3
PDATA4
PDATA5
PDATA6
PDATA7
PCS_2
POE#
PR_W#
PWBE_0#
RESETS
RESET_POR#
RESET_PB_POR#
DEBUG_TRST#
CPU_TRST#
CLOCKS
CLK_CPLD_33MHZ
CLK_CPLD_50MHZ
CLK_PERCLK
CLK_TMRCLK
CLK_SEL_M66EN
SEL_SYSCLK
STATUS / MISC
SYSERR
FLASH
FRY_BY#
FWP#
I2C
EE1_WP
EE2_BOOT_WP
STTM_AS
USB
USB2_RESET
CLK_USB2_CPLD
USB2_VCC_PE
USB2_VCC_PI
NAND FLASH
NF_WP#
ETHERNET
GETH1_COMA
GETH0_RST#
GETH0_COMA
GETH1_RST#
USB_EBC_MUX
USB_SELECT#
EBC_SELECT#
RESET_CPLD#
B2_IO_25
B1_IO10
B1_IO34
B2_IO_16
B2_IO_18
B1_IO29
B1_IO30
B1_IO_CLR#
B1_IO31
B1_IO21
B1_IO_OE
B1_IO23
B1_IO28
B2_IO_24
B2_IO_21
B2_IO_23
B2_IO_9
B2_IO_17
B2_IO_8
B2_IO_12
B2_IO_19
B1_IO_GCLK1
B1_IO_GCLK0
B2_IO_GCLK2
B1_IO25
B2_IO_33
B2_IO_35
B2_IO_34
B2_IO_28
B1_IO33
B2_IO_11
B2_IO_3
B2_IO_GCLK3
B1_IO32
B2_IO_13
B2_IO_6
B2_IO_7
B2_IO_2
B2_IO_1
B2_IO_20
B2_IO_37
B2_IO_38
B2_IO_39
B2_IO_40
B1_IO1
B1_IO2
B1_IO6
B1_IO22
B1_IO17
B2_IO_15
B2_IO_22
CFG_DIP0
CFG_DIP1
CFG_DIP2
M66EN
B1_IO19
B1_IO15
B2_IO_14
B1_IO20
B1_IO8
B2_IO_5
B1_IO16
USER_DIP0
USER_DIP1
USER_DIP2
USER_DIP3
B1_IO11
USER_LED0
B2_IO_4
USER_LED1
B2_IO_27
SYSERR#
B1_IO18
RESET_BUFPOR#
B1_IO24
B1_IO26
B2_IO_31
B2_IO_29
B1_IO3
B1_IO4
B1_IO5
B1_IO7
B1_IO9
B1_IO10
B1_IO12
B1_IO13
B1_IO14
B1_IO27
B2_IO_26
B2_IO_30
B2_IO_32
B2_IO_36
VCCAUX_JTAG
TCK
TDO
TMS
TDI
CPLD_TCK
CPLD_TDO
CPLD_TMS
CPLD_TDI
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
XC2C256-7VQ100C
Boot Configuration
R375
R373
R372
10K
SW3
4POLE
Configuration DIP-Swith
BOOT_CFG0
BOOT_CFG1
BOOT_CFG2
R016
R015
R017
R371
R377
R376
R374
SW2
User DIP-Swith
C543
0.1UF
0402
U37
74LVC1G08
VCC
GND
PWR_GOOD
GRN
RED
CR1
CR2
CR3
CR4
CR5
CR6
5V_VIN
R380
R385
R384
R383
R382
R381
180
Xilinx
Programing Cable
JTAG
J4
VREF
NC_0
NC_1
TDO
TDI
TMS
TCK
GND_7
GND_6
GND_4
GND_3
GND_2
GND_1
GND_0
R379
R378
1K
C535
2U2
PLACE NEAR CPLD JTAG CONNECTOR

CPU_TRST# = '1' when JTAG_TRST# = '1' and
RESET_POR# = '1' else '0'; see errata sheet

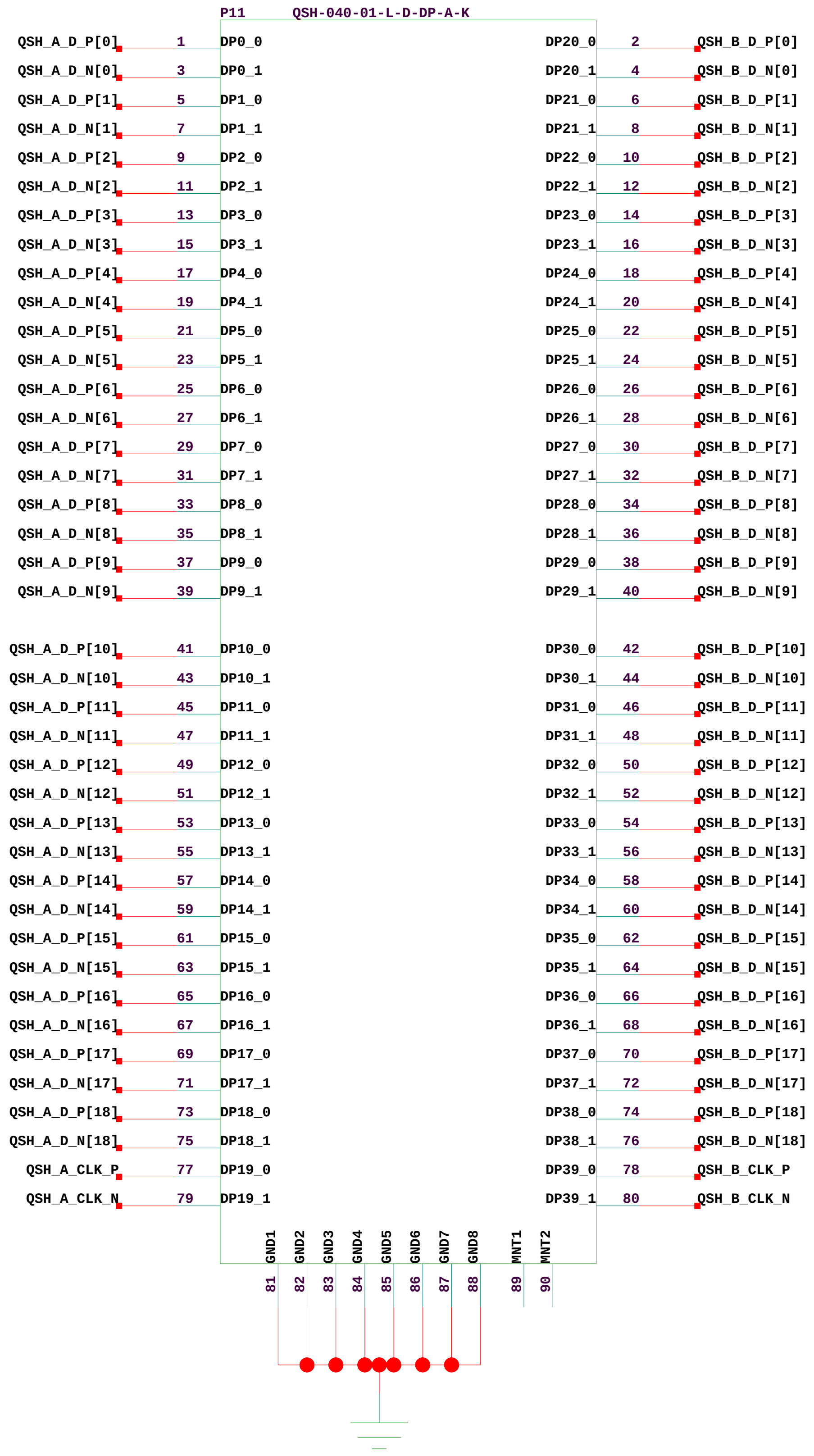
Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

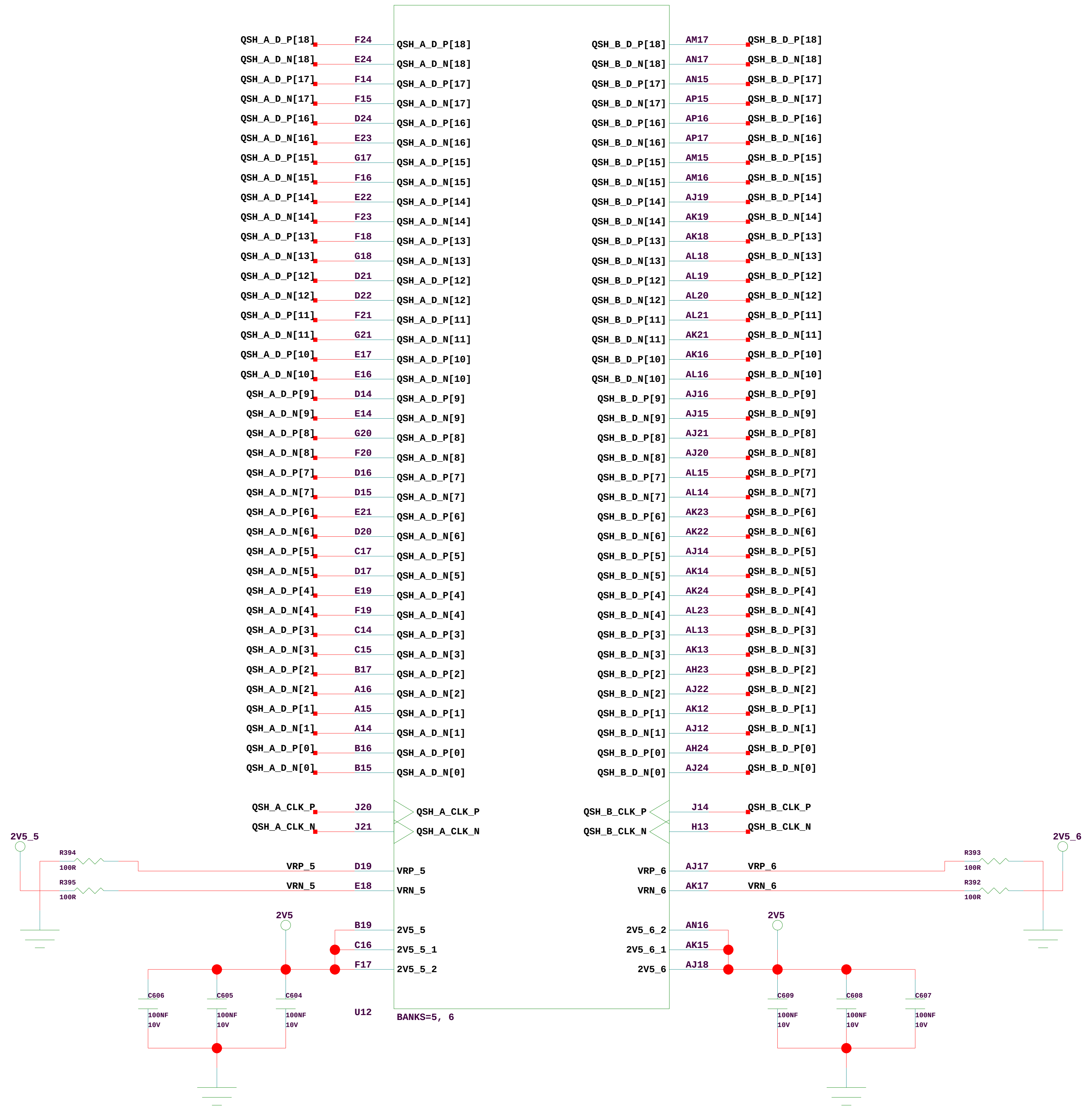
BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

SysErr will be used to
drive Status LED (active H)

Dedicated pins for EPM570
compatibility

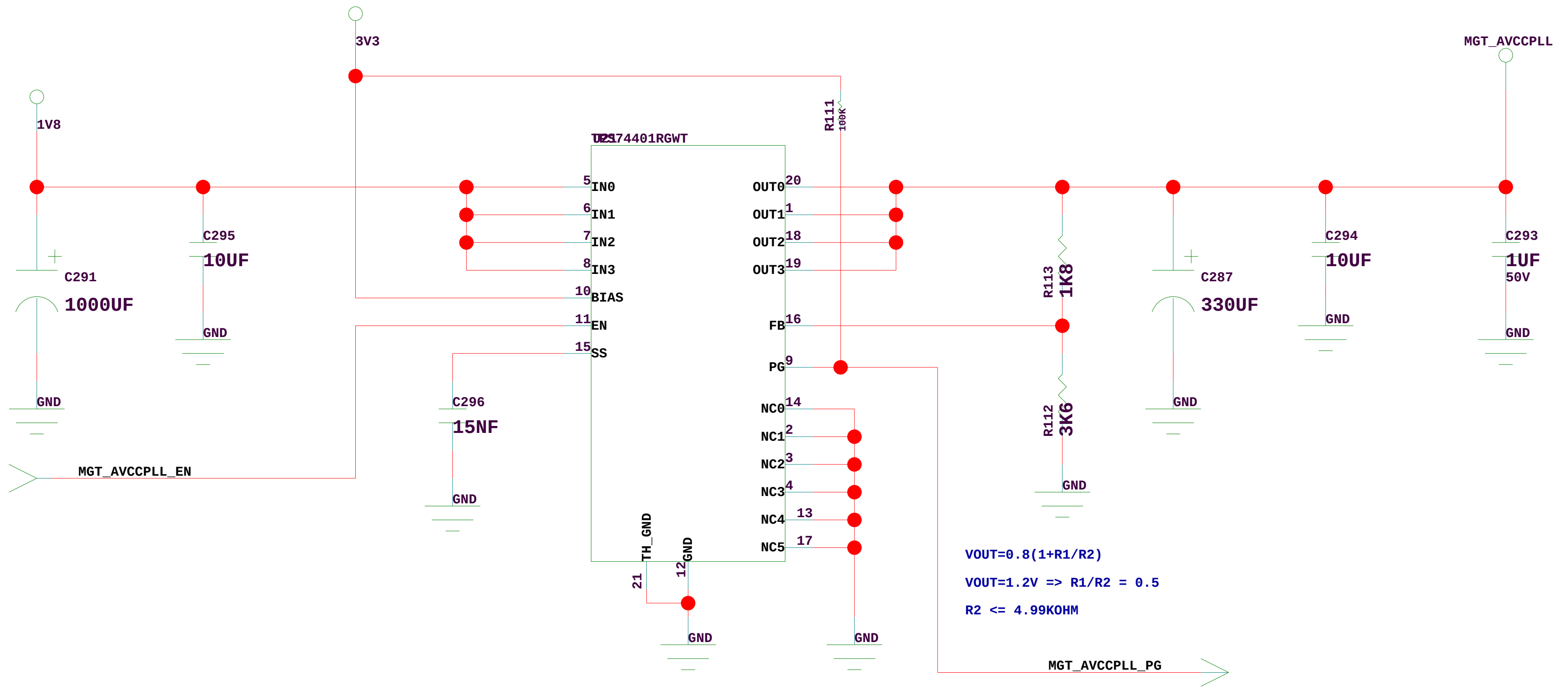
Assertion of USB2_RESET may be
asynchronous to CLK_USB2_CPLD
De-assertion of USB2_RESET must be
synchronous to CLK_USB2_CPLD


P11 QSH-040-01-L-D-DP-A-K
QSH_A_D_P[0] 1 DP0_0 | DP20_0 2 QSH_B_D_P[0]
QSH_A_D_N[0] 3 DP0_1 | DP20_1 4 QSH_B_D_N[0]
QSH_A_D_P[1] 5 DP1_0 | DP21_0 6 QSH_B_D_P[1]
QSH_A_D_N[1] 7 DP1_1 | DP21_1 8 QSH_B_D_N[1]
QSH_A_D_P[2] 9 DP2_0 | DP22_0 10 QSH_B_D_P[2]
QSH_A_D_N[2] 11 DP2_1 | DP22_1 12 QSH_B_D_N[2]
QSH_A_D_P[3] 13 DP3_0 | DP23_0 14 QSH_B_D_P[3]
QSH_A_D_N[3] 15 DP3_1 | DP23_1 16 QSH_B_D_N[3]
QSH_A_D_P[4] 17 DP4_0 | DP24_0 18 QSH_B_D_P[4]
QSH_A_D_N[4] 19 DP4_1 | DP24_1 20 QSH_B_D_N[4]
QSH_A_D_P[5] 21 DP5_0 | DP25_0 22 QSH_B_D_P[5]
QSH_A_D_N[5] 23 DP5_1 | DP25_1 24 QSH_B_D_N[5]
QSH_A_D_P[6] 25 DP6_0 | DP26_0 26 QSH_B_D_P[6]
QSH_A_D_N[6] 27 DP6_1 | DP26_1 28 QSH_B_D_N[6]
QSH_A_D_P[7] 29 DP7_0 | DP27_0 30 QSH_B_D_P[7]
QSH_A_D_N[7] 31 DP7_1 | DP27_1 32 QSH_B_D_N[7]
QSH_A_D_P[8] 33 DP8_0 | DP28_0 34 QSH_B_D_P[8]
QSH_A_D_N[8] 35 DP8_1 | DP28_1 36 QSH_B_D_N[8]
QSH_A_D_P[9] 37 DP9_0 | DP29_0 38 QSH_B_D_P[9]
QSH_A_D_N[9] 39 DP9_1 | DP29_1 40 QSH_B_D_N[9]
QSH_A_D_P[10] 41 DP10_0 | DP30_0 42 QSH_B_D_P[10]
QSH_A_D_N[10] 43 DP10_1 | DP30_1 44 QSH_B_D_N[10]
QSH_A_D_P[11] 45 DP11_0 | DP31_0 46 QSH_B_D_P[11]
QSH_A_D_N[11] 47 DP11_1 | DP31_1 48 QSH_B_D_N[11]
QSH_A_D_P[12] 49 DP12_0 | DP32_0 50 QSH_B_D_P[12]
QSH_A_D_N[12] 51 DP12_1 | DP32_1 52 QSH_B_D_N[12]
QSH_A_D_P[13] 53 DP13_0 | DP33_0 54 QSH_B_D_P[13]
QSH_A_D_N[13] 55 DP13_1 | DP33_1 56 QSH_B_D_N[13]
QSH_A_D_P[14] 57 DP14_0 | DP34_0 58 QSH_B_D_P[14]
QSH_A_D_N[14] 59 DP14_1 | DP34_1 60 QSH_B_D_N[14]
QSH_A_D_P[15] 61 DP15_0 | DP35_0 62 QSH_B_D_P[15]
QSH_A_D_N[15] 63 DP15_1 | DP35_1 64 QSH_B_D_N[15]
QSH_A_D_P[16] 65 DP16_0 | DP36_0 66 QSH_B_D_P[16]
QSH_A_D_N[16] 67 DP16_1 | DP36_1 68 QSH_B_D_N[16]
QSH_A_D_P[17] 69 DP17_0 | DP37_0 70 QSH_B_D_P[17]
QSH_A_D_N[17] 71 DP17_1 | DP37_1 72 QSH_B_D_N[17]
QSH_A_D_P[18] 73 DP18_0 | DP38_0 74 QSH_B_D_P[18]
QSH_A_D_N[18] 75 DP18_1 | DP38_1 76 QSH_B_D_N[18]
QSH_A_CLK_P 77 DP19_0 | DP39_0 78 QSH_B_CLK_P
QSH_A_CLK_N 79 DP19_1 | DP39_1 80 QSH_B_CLK_N
GND1 81
GND2 82
GND3 83
GND4 84
GND5 85
GND6 86
GND7 87
GND8 88
MNT1 89
MNT2 90


QSH_A_D_P[18] F24 QSH_A_D_P[18] | QSH_B_D_P[18] AM17 QSH_B_D_P[18]
QSH_A_D_N[18] E24 QSH_A_D_N[18] | QSH_B_D_N[18] AN17 QSH_B_D_N[18]
QSH_A_D_P[17] F14 QSH_A_D_P[17] | QSH_B_D_P[17] AN15 QSH_B_D_P[17]
QSH_A_D_N[17] F15 QSH_A_D_N[17] | QSH_B_D_N[17] AP15 QSH_B_D_N[17]
QSH_A_D_P[16] D24 QSH_A_D_P[16] | QSH_B_D_P[16] AP16 QSH_B_D_P[16]
QSH_A_D_N[16] E23 QSH_A_D_N[16] | QSH_B_D_N[16] AP17 QSH_B_D_N[16]
QSH_A_D_P[15] G17 QSH_A_D_P[15] | QSH_B_D_P[15] AM15 QSH_B_D_P[15]
QSH_A_D_N[15] F16 QSH_A_D_N[15] | QSH_B_D_N[15] AM16 QSH_B_D_N[15]
QSH_A_D_P[14] E22 QSH_A_D_P[14] | QSH_B_D_P[14] AJ19 QSH_B_D_P[14]
QSH_A_D_N[14] F23 QSH_A_D_N[14] | QSH_B_D_N[14] AK19 QSH_B_D_N[14]
QSH_A_D_P[13] F18 QSH_A_D_P[13] | QSH_B_D_P[13] AK18 QSH_B_D_P[13]
QSH_A_D_N[13] G18 QSH_A_D_N[13] | QSH_B_D_N[13] AL18 QSH_B_D_N[13]
QSH_A_D_P[12] D21 QSH_A_D_P[12] | QSH_B_D_P[12] AL19 QSH_B_D_P[12]
QSH_A_D_N[12] D22 QSH_A_D_N[12] | QSH_B_D_N[12] AL20 QSH_B_D_N[12]
QSH_A_D_P[11] F21 QSH_A_D_P[11] | QSH_B_D_P[11] AL21 QSH_B_D_P[11]
QSH_A_D_N[11] G21 QSH_A_D_N[11] | QSH_B_D_N[11] AK21 QSH_B_D_N[11]
QSH_A_D_P[10] E17 QSH_A_D_P[10] | QSH_B_D_P[10] AK16 QSH_B_D_P[10]
QSH_A_D_N[10] E16 QSH_A_D_N[10] | QSH_B_D_N[10] AL16 QSH_B_D_N[10]
QSH_A_D_P[9] D14 QSH_A_D_P[9] | QSH_B_D_P[9] AJ16 QSH_B_D_P[9]
QSH_A_D_N[9] E14 QSH_A_D_N[9] | QSH_B_D_N[9] AJ15 QSH_B_D_N[9]
QSH_A_D_P[8] G20 QSH_A_D_P[8] | QSH_B_D_P[8] AJ21 QSH_B_D_P[8]
QSH_A_D_N[8] F20 QSH_A_D_N[8] | QSH_B_D_N[8] AJ20 QSH_B_D_N[8]
QSH_A_D_P[7] D16 QSH_A_D_P[7] | QSH_B_D_P[7] AL15 QSH_B_D_P[7]
QSH_A_D_N[7] D15 QSH_A_D_N[7] | QSH_B_D_N[7] AL14 QSH_B_D_N[7]
QSH_A_D_P[6] E21 QSH_A_D_P[6] | QSH_B_D_P[6] AK23 QSH_B_D_P[6]
QSH_A_D_N[6] D20 QSH_A_D_N[6] | QSH_B_D_N[6] AK22 QSH_B_D_N[6]
QSH_A_D_P[5] C17 QSH_A_D_P[5] | QSH_B_D_P[5] AJ14 QSH_B_D_P[5]
QSH_A_D_N[5] D17 QSH_A_D_N[5] | QSH_B_D_N[5] AK14 QSH_B_D_N[5]
QSH_A_D_P[4] E19 QSH_A_D_P[4] | QSH_B_D_P[4] AK24 QSH_B_D_P[4]
QSH_A_D_N[4] F19 QSH_A_D_N[4] | QSH_B_D_N[4] AL23 QSH_B_D_N[4]
QSH_A_D_P[3] C14 QSH_A_D_P[3] | QSH_B_D_P[3] AL13 QSH_B_D_P[3]
QSH_A_D_N[3] C15 QSH_A_D_N[3] | QSH_B_D_N[3] AK13 QSH_B_D_N[3]
QSH_A_D_P[2] B17 QSH_A_D_P[2] | QSH_B_D_P[2] AH23 QSH_B_D_P[2]
QSH_A_D_N[2] A16 QSH_A_D_N[2] | QSH_B_D_N[2] AJ22 QSH_B_D_N[2]
QSH_A_D_P[1] A15 QSH_A_D_P[1] | QSH_B_D_P[1] AK12 QSH_B_D_P[1]
QSH_A_D_N[1] A14 QSH_A_D_N[1] | QSH_B_D_N[1] AJ12 QSH_B_D_N[1]
QSH_A_D_P[0] B16 QSH_A_D_P[0] | QSH_B_D_P[0] AH24 QSH_B_D_P[0]
QSH_A_D_N[0] B15 QSH_A_D_N[0] | QSH_B_D_N[0] AJ24 QSH_B_D_N[0]
QSH_A_CLK_P J20 QSH_A_CLK_P | QSH_B_CLK_P J14 QSH_B_CLK_P
QSH_A_CLK_N J21 QSH_A_CLK_N | QSH_B_CLK_N H13 QSH_B_CLK_N
2V5_5
R394 100R
R395 100R
VRP_5 D19 VRP_5 | VRP_6 AJ17 VRP_6
VRN_5 E18 VRN_5 | VRN_6 AK17 VRN_6
2V5_6
R393 100R
R392 100R
2V5
B19 2V5_5 | 2V5_6_2 AN16
C16 2V5_5_1 | 2V5_6_1 AK15
F17 2V5_5_2 | 2V5_6 AJ18
2V5
C606 100NF 10V
C605 100NF 10V
C604 100NF 10V
U12
BANKS=5, 6
C609 100NF 10V
C608 100NF 10V
C607 100NF 10V

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1
FB2
FB3
FB4
220@100M
C262
C261
C260
C259
220NF
6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_112 R3
MGTAVCC_112_1 R4
MGTAVCCPLL_112 T3
MGTAVTTRX_112 N3
MGT_112_REF_CLK_P P4
MGT_112_REF_CLK_N P3
MGTRX0_112_P N1
MGTRX0_112_N P1
MGTRX1_112_P T1
MGTRX1_112_N R1
U12
MGTRREF V4
MGTAVTTRXC V5
MGTAVTTTX_112 M3
MGTAVTTTX_112_1 U3
MGTTX0_112_P M2
MGTTX0_112_N N2
MGTTX1_112_P U2
MGTTX1_112_N T2
R101
49.9R
FB25
FB5
FB6
C263
C264
C265
2V5
FB26
220@100M
C284
220NF
6.3V
R106
10K
X1
VCC
OE
OUT
OUTB
GND
JP4
CCLD-023-25-156.250
156.25MHZ
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
C237
C238
C239
C240
C242
C241
10NF
25V
FB11
FB12
FB9
FB10
C270
C269
C268
C267
MGTAVCC_114 AA3
MGTAVCC_114_1 AA4
MGTAVCCPLL_114 AB3
MGTAVTTRX_114 W3
MGT_114_REF_CLK_P NC Y4
MGT_114_REF_CLK_N NC Y3
MGTRX0_114_P W1
MGTRX0_114_N Y1
MGTRX1_114_P AB1
MGTRX1_114_N AA1
MGTAVTTTX_114 AC3
MGTAVTTTX_114_1 V3
MGTTX0_114_P V2
MGTTX0_114_N W2
MGTTX1_114_P AC2
MGTTX1_114_N AB2
MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT
FB8
FB7
C265
C266
P7
S1 DL0P
S2 DL0N
S3 DL1P
S4 DL1N
S5 DL2P
S6 DL2N
S7 DL3P
S8 DL3N
S16 SL0P
S15 SL0N
S14 SL1P
S13 SL1N
S12 SL2P
S11 SL2N
S10 SL3P
S9 SL3N
SIG_GND1 G1
SIG_GND2 G2
SIG_GND3 G3
SIG_GND4 G4
SIG_GND5 G5
SIG_GND6 G6
SIG_GND7 G7
SIG_GND8 G8
SIG_GND9 G9
SIG_GND10 G10
FCN-268F036-G/3DB
ODIS
FAULT
3V3
R103
10K
C251
10NF
6.3V
JP2
C252
R102
150R
D2
OPTICAL MODULE FAULT - RED LED
R107
5K1
R95
3K9
R99
6K8
R96
3K9
C249
U18
U17
IN-
IN+
OUT
MAX9032AKA
U19
A
B
Q
AND2
SN74AHC1G08DCKR
U15
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
TPS2031D
R109
10K
C250
10NF
6.3V
C257
100NF
6.3V
C285
4.7UF
16V
C247
22UF
16V
FB17
FB18
FB15
FB16
C277
C276
C275
C272
MGTAVCC_116 J3
MGTAVCC_116_1 J4
MGTAVCCPLL_116 K3
MGTAVTTRX_116 G3
MGT_116_REF_CLK_P NC H4
MGT_116_REF_CLK_N NC H3
MGTRX0_116_P G1
MGTRX0_116_N H1
MGTRX1_116_P K1
MGTRX1_116_N J1
MGTAVTTTX_116_1 L3
MGTAVTTTX_116 F3
MGTTX0_116_P F2
MGTTX0_116_N G2
MGTTX1_116_P L2
MGTTX1_116_N K2
FB14
FB13
C273
C274
C243
C244
C245
C246
FB22
FB21
FB24
FB23
C280
C281
C271
C282
MGTAVCC_118 AG3
MGTAVCC_118_1 AG4
MGTAVCCPLL_118 AH3
MGTAVTTRX_118 AE3
MGT_118_REF_CLK_P NC AF4
MGT_118_REF_CLK_N NC AF3
MGTRX0_118_P AE1
MGTRX0_118_N AF1
MGTRX1_118_P AH1
MGTRX1_118_N AG1
MGTAVTTTX_118_1 AJ3
MGTAVTTTX_118 AD3
MGTTX0_118_P AD2
MGTTX0_118_N AE2
MGTTX1_118_P AJ2
MGTTX1_118_N AH2
FB19
FB20
C279
C278
R105
150R
D3
JP3
R104
10K
C255
C253
R108
5K1
R97
3K9
R100
6K8
R98
3K9
C254
U20
U16
R110
10K
C256
C258
C286
C248

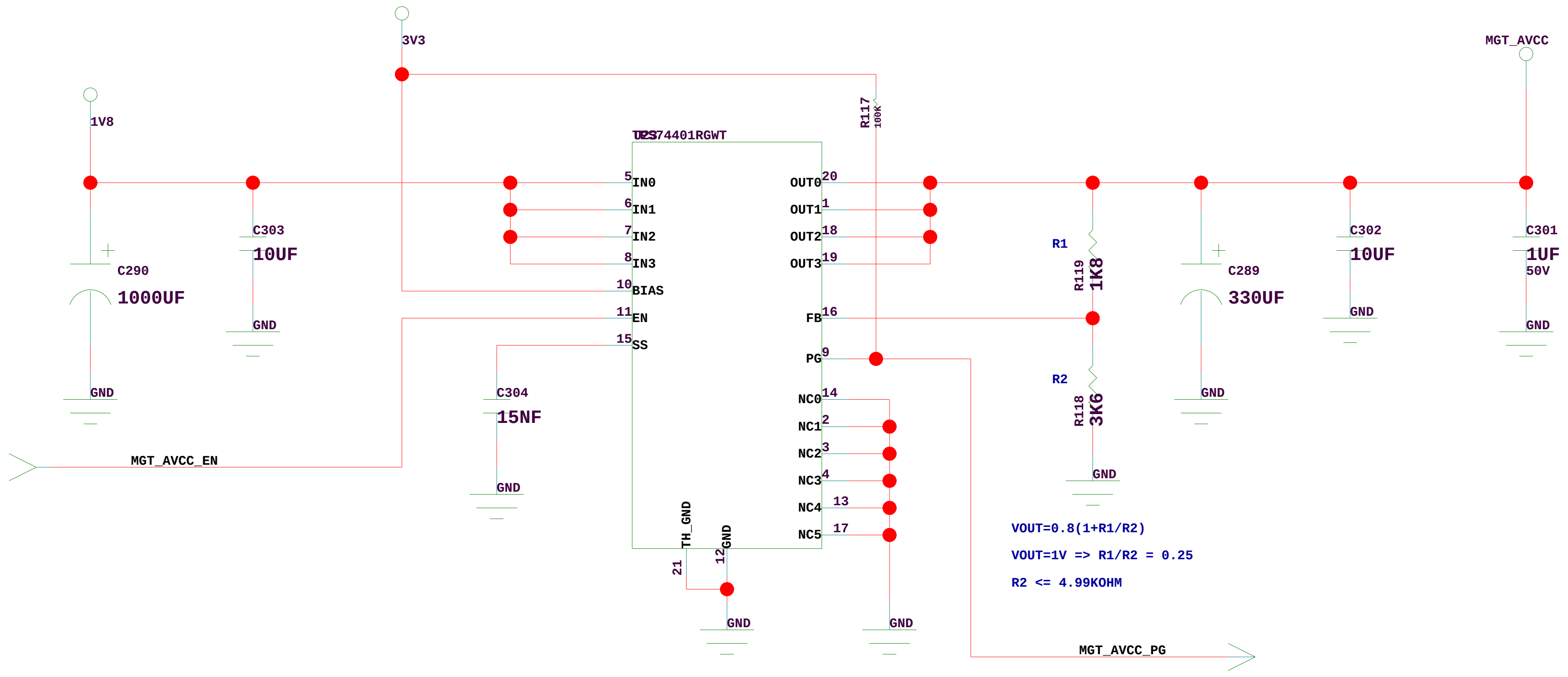
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB27
220@100M
FB28
220@100M
FB29
220@100M
FB30
220@100M
C361
C360
C359
C358
220NF
6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_120
MGTAVCC_120_1
MGTAVCCPLL_120
MGTAVTTRX_120
MGT_120_REF_CLK_P
MGT_120_REF_CLK_N
MGTRX0_120_P
MGTRX0_120_N
MGTRX1_120_P
MGTRX1_120_N
D5
F4
D3
C3
E4
D4
A3
A2
D1
C1
U12
MGTAVTTTX_120_1
MGTAVTTTX_120
E3
C4
MGTTX0_120_P
MGTTX0_120_N
MGTTX1_120_P
MGTTX1_120_N
B4
B3
E2
D2
FB31
220@100M
FB32
220@100M
C363
C362
2V5
FB51
220@100M
C382
220NF
6.3V
R174
10K
X2
VCC
OE
OUT
OUT#
GND
JP23
CCLD-023-25-156.250
156.25MHZ
MGT_REFCLK_Q2_P
MGT_REFCLK_Q2_N
C336
C337
C338
C339
C341
C340
10NF
25V
3V3
R170
100R
OPTICAL MODULE FAULT - RED LED
JP21
P7
S39 DL0P
S40 DL0N
S41 DL1P
S42 DL1N
S43 DL2P
S44 DL2N
S45 DL3P
S46 DL3N
S54 SL0P
S53 SL0N
S52 SL1P
S51 SL1N
S50 SL2P
S49 SL2N
S48 SL3P
S47 SL3N
SIG_GND1 G20
SIG_GND2 G21
SIG_GND3 G22
SIG_GND4 G23
SIG_GND5 G24
SIG_GND6 G25
SIG_GND7 G26
SIG_GND8 G27
SIG_GND9 G28
SIG_GND10 G19
FCN-268F036-G/3DB
ODIS
FAULT
R171
10K
C349
10NF
6.3V
C351
10NF
6.3V
R175
5K1
R165
3K9
R168
6K8
R164
3K9
C350
10NF 6.3V
U28
U27
IN-
IN+
OUT
MAX9032AKA
U29
AND2
SN74AHC1G08DCKR
A
B
Q
U25
IN1
IN2
OUT1
OUT2
OUT3
EN
OC
NC
TPS2031D
R177
10K
C348
10NF
6.3V
C356
100NF
6.3V
C383
4.7UF
16V
C346
22UF
16V
FB37
FB38
FB35
FB36
C369
C368
C367
C366
MGTAVCC_122
MGTAVCC_122_1
MGTAVCCPLL_122
MGTAVTTRX_122
MGT_122_REF_CLK_P
MGT_122_REF_CLK_N
MGTRX0_122_P
MGTRX0_122_N
MGTRX1_122_P
MGTRX1_122_N
AJ4
AK5
AM4
AL3
AL5
AL4
AL1
AM1
AP3
AP2
MGTAVTTTX_122_1
MGTAVTTTX_122
AM3
AK3
MGTTX0_122_P
MGTTX0_122_N
MGTTX1_122_P
MGTTX1_122_N
AK2
AL2
AN4
AN3
FB34
FB33
C364
C365
FB43
FB44
FB41
FB42
C376
C375
C374
C371
MGTAVCC_124
MGTAVCC_124_1
MGTAVCCPLL_124
MGTAVTTRX_124
MGT_124_REF_CLK_P
MGT_124_REF_CLK_N
MGTRX0_124_P
MGTRX0_124_N
MGTRX1_124_P
MGTRX1_124_N
C7
D7
C6
C9
D8
C8
A9
A8
A6
A7
MGTAVTTTX_124_1
MGTAVTTTX_124
C5
C10
MGTTX0_124_P
MGTTX0_124_N
MGTTX1_124_P
MGTTX1_124_N
B10
B9
B5
B6
FB40
FB39
C372
C373
C342
C343
C344
C345
R173
100R
JP22
S57 DL0P
S58 DL0N
S59 DL1P
S60 DL1N
S61 DL2P
S62 DL2N
S63 DL3P
S64 DL3N
S72 SL0P
S71 SL0N
S70 SL1P
S69 SL1N
S68 SL2P
S67 SL2N
S66 SL3P
S65 SL3N
SIG_GND1 G29
SIG_GND2 G30
SIG_GND3 G31
SIG_GND4 G32
SIG_GND5 G33
SIG_GND6 G34
SIG_GND7 G35
SIG_GND8 G36
SIG_GND9 G37
SIG_GND10 G19
R172
10K
C354
10NF
6.3V
C352
10NF
6.3V
R176
5K1
R166
3K9
R169
6K8
R167
3K9
C353
10NF
6.3V
U30
U26
R178
10K
C355
10NF
6.3V
C357
100NF
6.3V
C384
4.7UF
16V
C347
22UF
16V
FB48
FB47
FB50
FB49
C379
C380
C370
C381
MGTAVCC_126
MGTAVCC_126_1
MGTAVCCPLL_126
MGTAVTTRX_126
MGT_126_REF_CLK_P
MGT_126_REF_CLK_N
MGTRX0_126_P
MGTRX0_126_N
MGTRX1_126_P
MGTRX1_126_N
AL8
AM8
AM9
AM6
AL7
AM7
AP6
AP7
AP9
AP8
MGTAVTTTX_126_1
MGTAVTTTX_126
AM5
AM10
MGTTX0_126_P
MGTTX0_126_N
MGTTX1_126_P
MGTTX1_126_N
AN5
AN6
AN10
AN9
FB45
FB46
C378
C377


3V3
1V8
MGT_AVCCPLL
R111
100K
TPS74401RGWT
5 IN0
6 IN1
7 IN2
8 IN3
10 BIAS
11 EN
15 SS
OUT0 20
OUT1 1
OUT2 18
OUT3 19
FB 16
PG 9
NC0 14
NC1 2
NC2 3
NC3 4
NC4 13
NC5 17
TH_GND
21
12 GND
C291
1000UF
C295
10UF
C296
15NF
R113
1K8
R112
3K6
C287
330UF
C294
10UF
C293
1UF
50V
GND
MGT_AVCCPLL_EN
MGT_AVCCPLL_PG

VOUT=0.8(1+R1/R2)

VOUT=1.2V => R1/R2 = 0.5

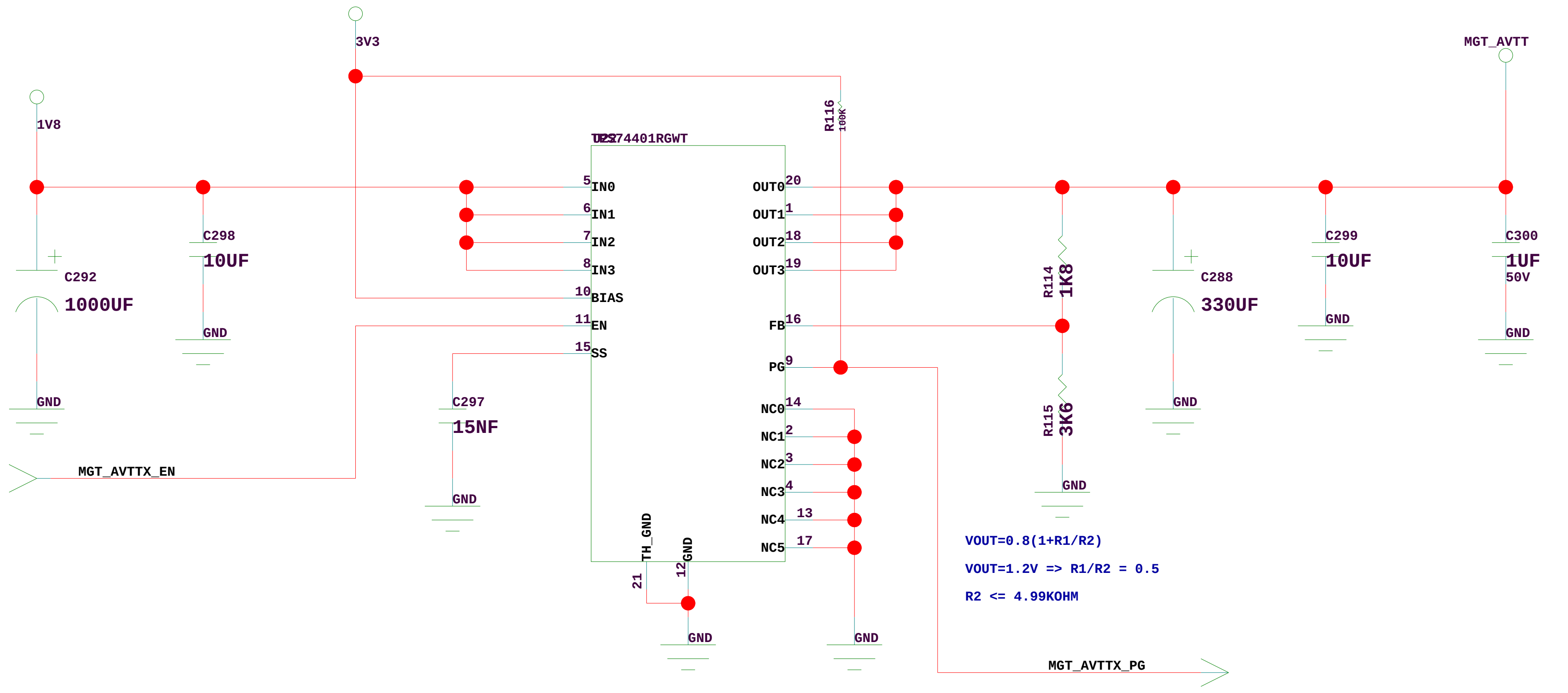
R2 <= 4.99KOHM


3V3
1V8
MGT_AVCC
R117
100K
TPS74401RGWT
5 IN0
6 IN1
7 IN2
8 IN3
10 BIAS
11 EN
15 SS
OUT0 20
OUT1 1
OUT2 18
OUT3 19
FB 16
PG 9
NC0 14
NC1 2
NC2 3
NC3 4
NC4 13
NC5 17
TH_GND
21
12 GND
C290
1000UF
C303
10UF
C304
15NF
R1
R119
1K8
R2
R118
3K6
C289
330UF
C302
10UF
C301
1UF
50V
GND
MGT_AVCC_EN
MGT_AVCC_PG

VOUT=0.8(1+R1/R2)

VOUT=1V => R1/R2 = 0.25

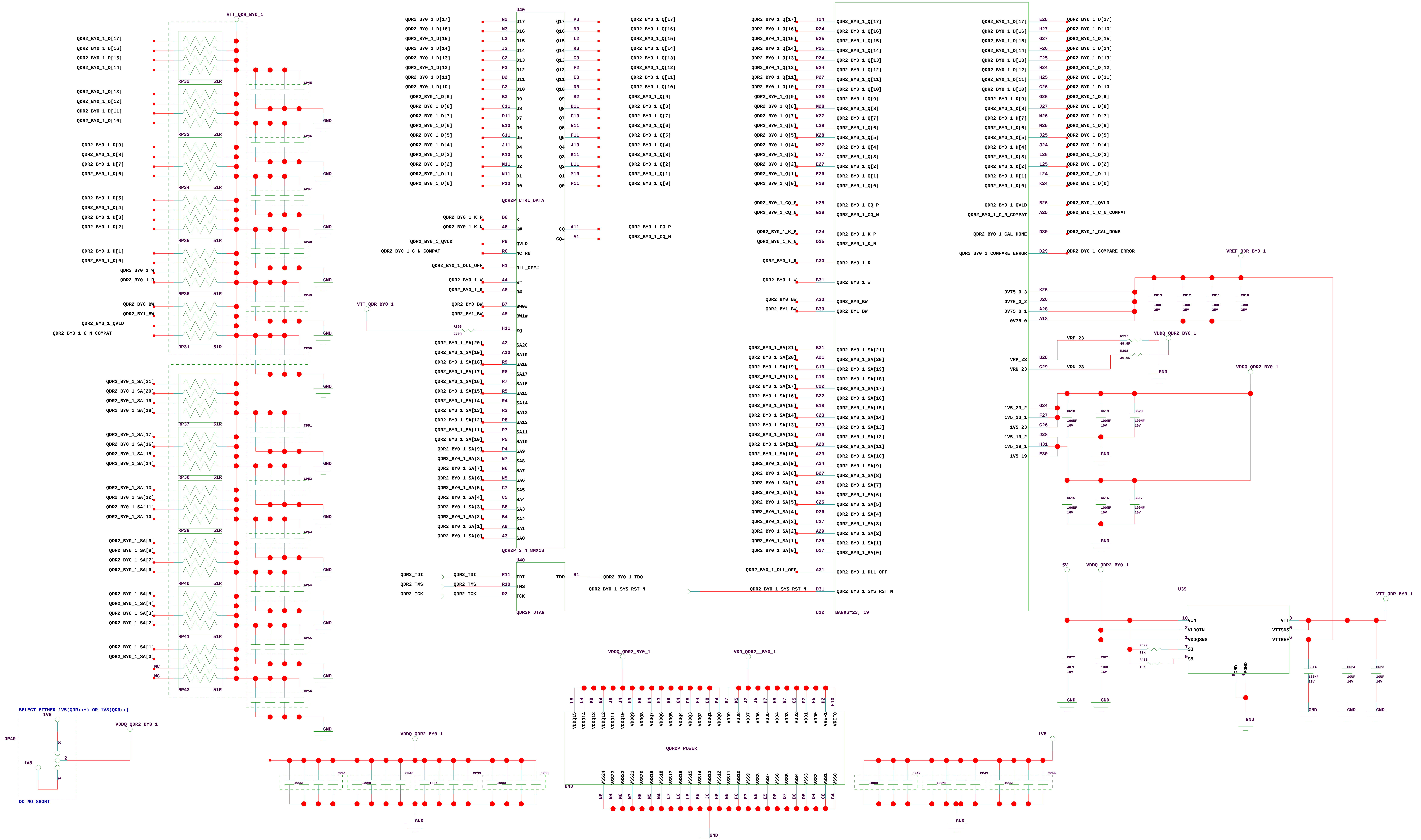
R2 <= 4.99KOHM


3V3
1V8
MGT_AVTT
R116
100K
TPS74401RGWT
5 IN0
6 IN1
7 IN2
8 IN3
10 BIAS
11 EN
15 SS
OUT0 20
OUT1 1
OUT2 18
OUT3 19
FB 16
PG 9
NC0 14
NC1 2
NC2 3
NC3 4
NC4 13
NC5 17
TH_GND
21
12 GND
C292
1000UF
C298
10UF
C297
15NF
R114
1K8
R115
3K6
C288
330UF
C299
10UF
C300
1UF
50V
GND
MGT_AVTTX_EN
MGT_AVTTX_PG

VOUT=0.8(1+R1/R2)

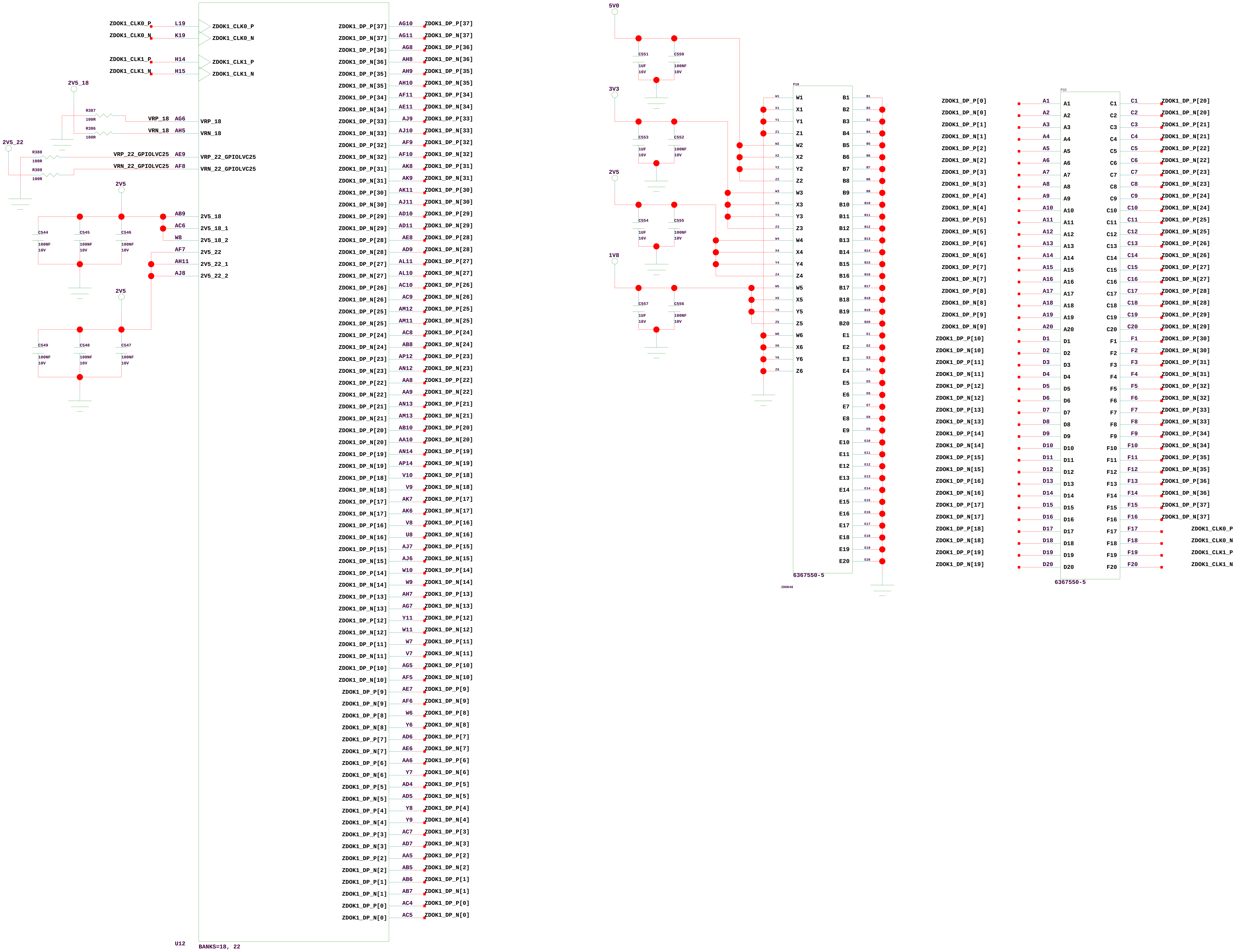
VOUT=1.2V => R1/R2 = 0.5

R2 <= 4.99KOHM

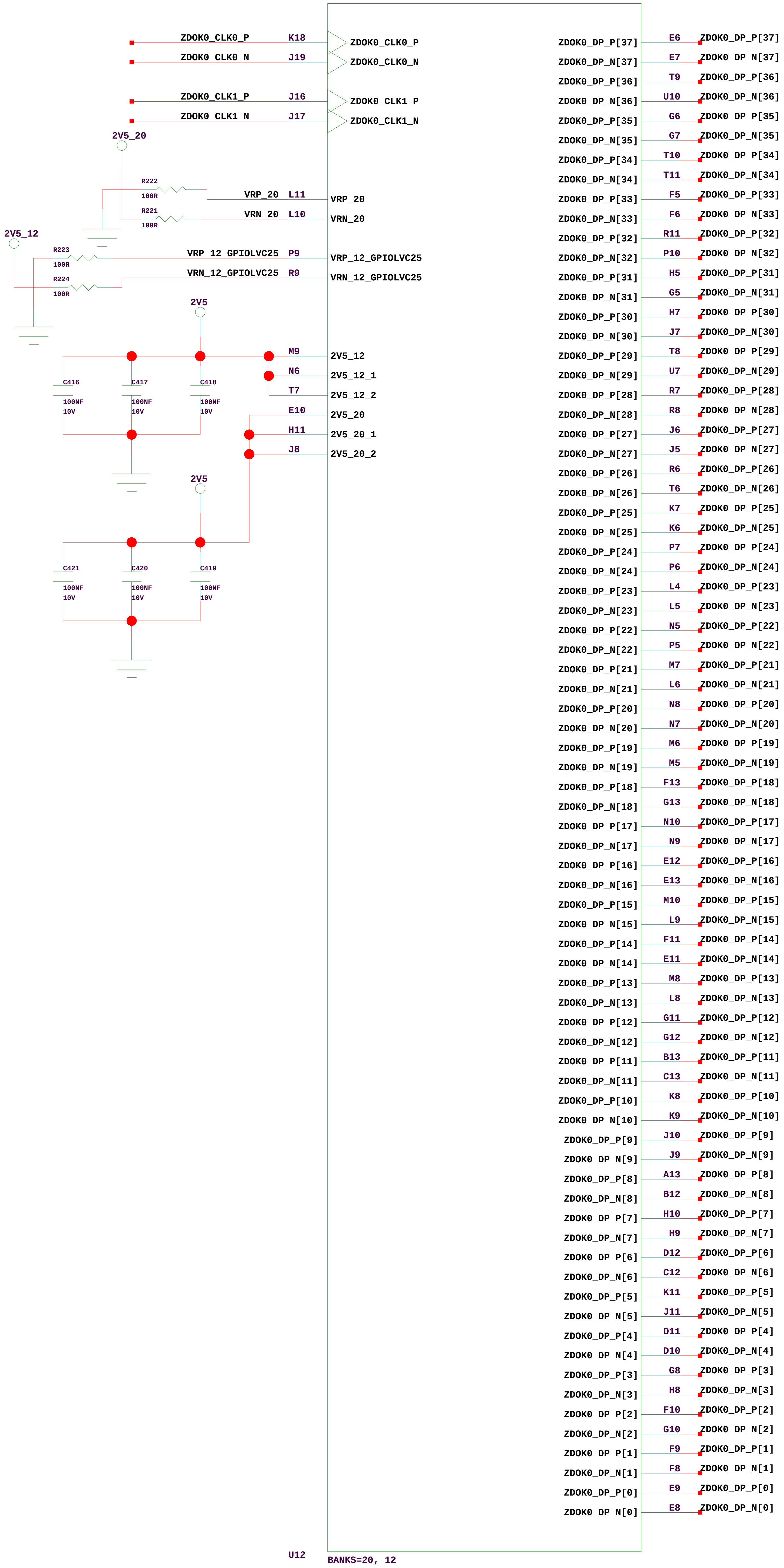

VTT_QDR_BY0_1
RP32 51R
RP33 51R
RP34 51R
RP35 51R
RP36 51R
RP31 51R
RP37 51R
RP38 51R
RP39 51R
RP40 51R
RP41 51R
RP42 51R
CP45
CP46
CP47
CP48
CP49
CP50
CP51
CP52
CP53
CP54
CP55
CP56
GND
QDR2_BY0_1_D[17]
QDR2_BY0_1_D[0]
QDR2_BY0_BW
QDR2_BY1_BW
QDR2_BY0_1_QVLD
QDR2_BY0_1_C_N_COMPAT
QDR2_BY0_1_SA[21]
QDR2_BY0_1_SA[0]
NC
U40
QDR2P_CTRL_DATA
QDR2P_2_4_SMX18
K
K#
QVLD
NC_R6
DLL_OFF#
W#
R#
BW0#
BW1#
ZQ
R396
270R
CQ
CQ#
QDR2_BY0_1_CQ_P
QDR2_BY0_1_CQ_N
QDR2_BY0_1_DLL_OFF
QDR2_BY0_1_K_P
QDR2_BY0_1_K_N
QDR2_BY0_1_W
QDR2_BY0_1_R
QDR2P_JTAG
TDI
TMS
TCK
TDO
QDR2_TDI
QDR2_TMS
QDR2_TCK
QDR2_BY0_1_TDO
QDR2_BY0_1_SYS_RST_N
U12
BANKS=23, 19
QDR2_BY0_1_CAL_DONE
QDR2_BY0_1_COMPARE_ERROR
VREF_QDR_BY0_1
C613
C612
C611
C610
10NF
25V
0V75_0_3
0V75_0_2
0V75_0_1
0V75_0
VRP_23
VRN_23
R397
R398
49.9R
VDDQ_QDR2_BY0_1
1V5_23_2
1V5_23_1
1V5_23
1V5_19_2
1V5_19_1
1V5_19
C618
C619
C620
C615
C616
C617
100NF
10V
5V
U39
VIN
VLDOIN
VDDQSNS
S3
S5
GND
PGND
VTT
VTTSNS
VTTREF
R399
R400
10K
C622
C621
C614
C624
C623
4U7F
10UF
JP40
1V5
1V8
VDD_QDR2__BY0_1
QDR2P_POWER
CP41
CP40
CP39
CP38
CP42
CP43
CP44

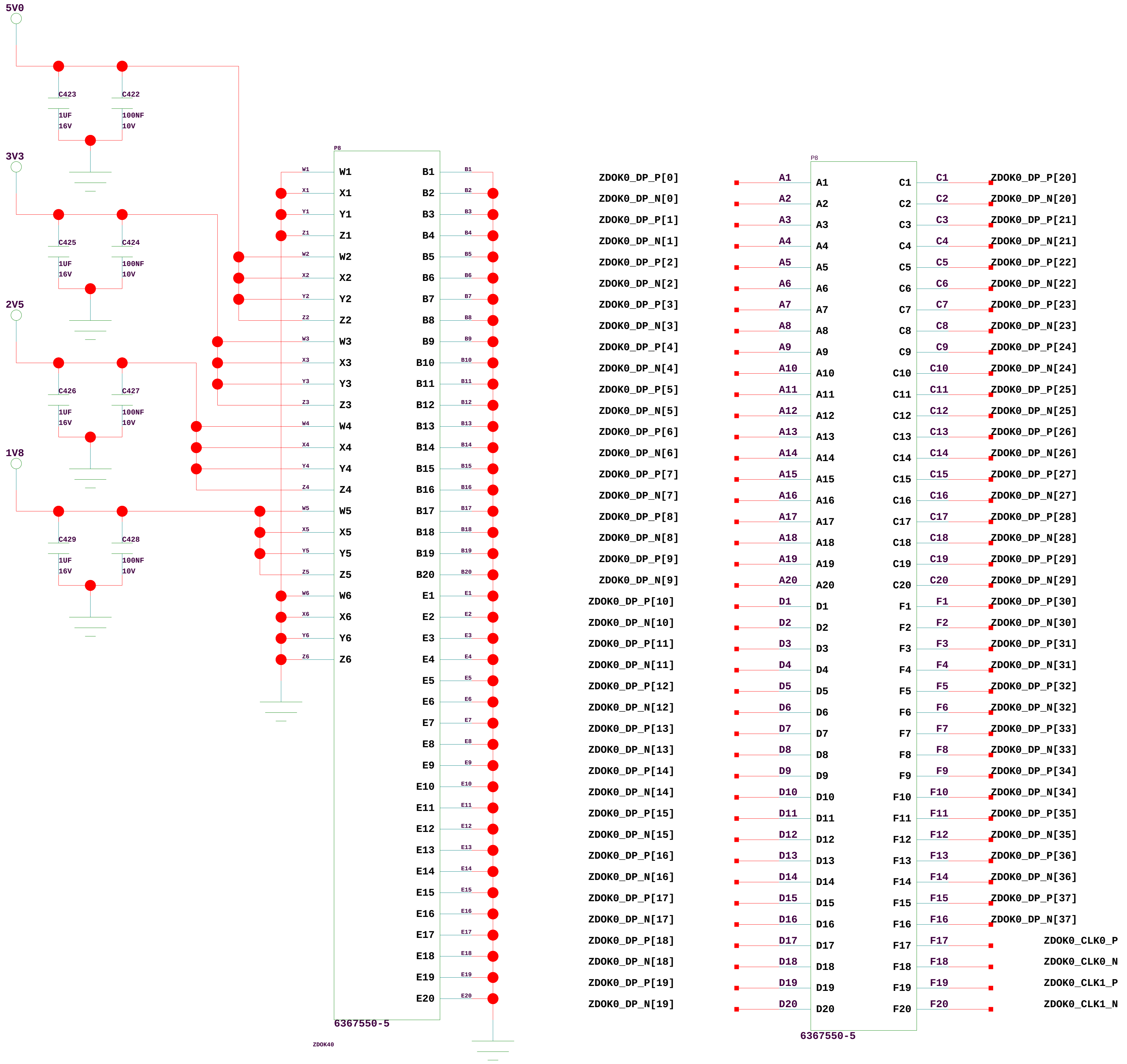
SELECT EITHER 1V5(QDRii+) OR 1V8(QDRii)

DO NO SHORT


ZDOK1_CLK0_P L19 ZDOK1_CLK0_P
ZDOK1_CLK0_N K19 ZDOK1_CLK0_N
ZDOK1_CLK1_P H14 ZDOK1_CLK1_P
ZDOK1_CLK1_N H15 ZDOK1_CLK1_N
2V5_18
R387 100R
R386 100R
VRP_18 AG6 VRP_18
VRN_18 AH5 VRN_18
2V5_22
R388 100R
R389 100R
VRP_22_GPIOLVC25 AE9 VRP_22_GPIOLVC25
VRN_22_GPIOLVC25 AF8 VRN_22_GPIOLVC25
2V5
C544 100NF 10V
C545 100NF 10V
C546 100NF 10V
AB9 2V5_18
AC6 2V5_18_1
W8 2V5_18_2
AF7 2V5_22
AH11 2V5_22_1
AJ8 2V5_22_2
2V5
C549 100NF 10V
C548 100NF 10V
C547 100NF 10V
U12
BANKS=18, 22
ZDOK1_DP_P[37] AG10 ZDOK1_DP_P[37]
ZDOK1_DP_N[37] AG11 ZDOK1_DP_N[37]
ZDOK1_DP_P[36] AG8 ZDOK1_DP_P[36]
ZDOK1_DP_N[36] AH8 ZDOK1_DP_N[36]
ZDOK1_DP_P[35] AH9 ZDOK1_DP_P[35]
ZDOK1_DP_N[35] AH10 ZDOK1_DP_N[35]
ZDOK1_DP_P[34] AF11 ZDOK1_DP_P[34]
ZDOK1_DP_N[34] AE11 ZDOK1_DP_N[34]
ZDOK1_DP_P[33] AJ9 ZDOK1_DP_P[33]
ZDOK1_DP_N[33] AJ10 ZDOK1_DP_N[33]
ZDOK1_DP_P[32] AF9 ZDOK1_DP_P[32]
ZDOK1_DP_N[32] AF10 ZDOK1_DP_N[32]
ZDOK1_DP_P[31] AK8 ZDOK1_DP_P[31]
ZDOK1_DP_N[31] AK9 ZDOK1_DP_N[31]
ZDOK1_DP_P[30] AK11 ZDOK1_DP_P[30]
ZDOK1_DP_N[30] AJ11 ZDOK1_DP_N[30]
ZDOK1_DP_P[29] AD10 ZDOK1_DP_P[29]
ZDOK1_DP_N[29] AD11 ZDOK1_DP_N[29]
ZDOK1_DP_P[28] AE8 ZDOK1_DP_P[28]
ZDOK1_DP_N[28] AD9 ZDOK1_DP_N[28]
ZDOK1_DP_P[27] AL11 ZDOK1_DP_P[27]
ZDOK1_DP_N[27] AL10 ZDOK1_DP_N[27]
ZDOK1_DP_P[26] AC10 ZDOK1_DP_P[26]
ZDOK1_DP_N[26] AC9 ZDOK1_DP_N[26]
ZDOK1_DP_P[25] AM12 ZDOK1_DP_P[25]
ZDOK1_DP_N[25] AM11 ZDOK1_DP_N[25]
ZDOK1_DP_P[24] AC8 ZDOK1_DP_P[24]
ZDOK1_DP_N[24] AB8 ZDOK1_DP_N[24]
ZDOK1_DP_P[23] AP12 ZDOK1_DP_P[23]
ZDOK1_DP_N[23] AN12 ZDOK1_DP_N[23]
ZDOK1_DP_P[22] AA8 ZDOK1_DP_P[22]
ZDOK1_DP_N[22] AA9 ZDOK1_DP_N[22]
ZDOK1_DP_P[21] AN13 ZDOK1_DP_P[21]
ZDOK1_DP_N[21] AM13 ZDOK1_DP_N[21]
ZDOK1_DP_P[20] AB10 ZDOK1_DP_P[20]
ZDOK1_DP_N[20] AA10 ZDOK1_DP_N[20]
ZDOK1_DP_P[19] AN14 ZDOK1_DP_P[19]
ZDOK1_DP_N[19] AP14 ZDOK1_DP_N[19]
ZDOK1_DP_P[18] V10 ZDOK1_DP_P[18]
ZDOK1_DP_N[18] V9 ZDOK1_DP_N[18]
ZDOK1_DP_P[17] AK7 ZDOK1_DP_P[17]
ZDOK1_DP_N[17] AK6 ZDOK1_DP_N[17]
ZDOK1_DP_P[16] V8 ZDOK1_DP_P[16]
ZDOK1_DP_N[16] U8 ZDOK1_DP_N[16]
ZDOK1_DP_P[15] AJ7 ZDOK1_DP_P[15]
ZDOK1_DP_N[15] AJ6 ZDOK1_DP_N[15]
ZDOK1_DP_P[14] W10 ZDOK1_DP_P[14]
ZDOK1_DP_N[14] W9 ZDOK1_DP_N[14]
ZDOK1_DP_P[13] AH7 ZDOK1_DP_P[13]
ZDOK1_DP_N[13] AG7 ZDOK1_DP_N[13]
ZDOK1_DP_P[12] Y11 ZDOK1_DP_P[12]
ZDOK1_DP_N[12] W11 ZDOK1_DP_N[12]
ZDOK1_DP_P[11] W7 ZDOK1_DP_P[11]
ZDOK1_DP_N[11] V7 ZDOK1_DP_N[11]
ZDOK1_DP_P[10] AG5 ZDOK1_DP_P[10]
ZDOK1_DP_N[10] AF5 ZDOK1_DP_N[10]
ZDOK1_DP_P[9] AE7 ZDOK1_DP_P[9]
ZDOK1_DP_N[9] AF6 ZDOK1_DP_N[9]
ZDOK1_DP_P[8] W6 ZDOK1_DP_P[8]
ZDOK1_DP_N[8] Y6 ZDOK1_DP_N[8]
ZDOK1_DP_P[7] AD6 ZDOK1_DP_P[7]
ZDOK1_DP_N[7] AE6 ZDOK1_DP_N[7]
ZDOK1_DP_P[6] AA6 ZDOK1_DP_P[6]
ZDOK1_DP_N[6] Y7 ZDOK1_DP_N[6]
ZDOK1_DP_P[5] AD4 ZDOK1_DP_P[5]
ZDOK1_DP_N[5] AD5 ZDOK1_DP_N[5]
ZDOK1_DP_P[4] Y8 ZDOK1_DP_P[4]
ZDOK1_DP_N[4] Y9 ZDOK1_DP_N[4]
ZDOK1_DP_P[3] AC7 ZDOK1_DP_P[3]
ZDOK1_DP_N[3] AD7 ZDOK1_DP_N[3]
ZDOK1_DP_P[2] AA5 ZDOK1_DP_P[2]
ZDOK1_DP_N[2] AB5 ZDOK1_DP_N[2]
ZDOK1_DP_P[1] AB6 ZDOK1_DP_P[1]
ZDOK1_DP_N[1] AB7 ZDOK1_DP_N[1]
ZDOK1_DP_P[0] AC4 ZDOK1_DP_P[0]
ZDOK1_DP_N[0] AC5 ZDOK1_DP_N[0]
5V0
C551 1UF 16V
C550 100NF 10V
3V3
C553 1UF 16V
C552 100NF 10V
2V5
C554 1UF 16V
C555 100NF 10V
1V8
C557 1UF 16V
C556 100NF 10V
P10
W1 X1 Y1 Z1 W2 X2 Y2 Z2 W3 X3 Y3 Z3 W4 X4 Y4 Z4 W5 X5 Y5 Z5 W6 X6 Y6 Z6
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20
E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20
6367550-5
ZDOK40
P10
ZDOK1_DP_P[0] A1
ZDOK1_DP_N[0] A2
ZDOK1_DP_P[1] A3
ZDOK1_DP_N[1] A4
ZDOK1_DP_P[2] A5
ZDOK1_DP_N[2] A6
ZDOK1_DP_P[3] A7
ZDOK1_DP_N[3] A8
ZDOK1_DP_P[4] A9
ZDOK1_DP_N[4] A10
ZDOK1_DP_P[5] A11
ZDOK1_DP_N[5] A12
ZDOK1_DP_P[6] A13
ZDOK1_DP_N[6] A14
ZDOK1_DP_P[7] A15
ZDOK1_DP_N[7] A16
ZDOK1_DP_P[8] A17
ZDOK1_DP_N[8] A18
ZDOK1_DP_P[9] A19
ZDOK1_DP_N[9] A20
ZDOK1_DP_P[10] D1
ZDOK1_DP_N[10] D2
ZDOK1_DP_P[11] D3
ZDOK1_DP_N[11] D4
ZDOK1_DP_P[12] D5
ZDOK1_DP_N[12] D6
ZDOK1_DP_P[13] D7
ZDOK1_DP_N[13] D8
ZDOK1_DP_P[14] D9
ZDOK1_DP_N[14] D10
ZDOK1_DP_P[15] D11
ZDOK1_DP_N[15] D12
ZDOK1_DP_P[16] D13
ZDOK1_DP_N[16] D14
ZDOK1_DP_P[17] D15
ZDOK1_DP_N[17] D16
ZDOK1_DP_P[18] D17
ZDOK1_DP_N[18] D18
ZDOK1_DP_P[19] D19
ZDOK1_DP_N[19] D20
C1 ZDOK1_DP_P[20]
C2 ZDOK1_DP_N[20]
C3 ZDOK1_DP_P[21]
C4 ZDOK1_DP_N[21]
C5 ZDOK1_DP_P[22]
C6 ZDOK1_DP_N[22]
C7 ZDOK1_DP_P[23]
C8 ZDOK1_DP_N[23]
C9 ZDOK1_DP_P[24]
C10 ZDOK1_DP_N[24]
C11 ZDOK1_DP_P[25]
C12 ZDOK1_DP_N[25]
C13 ZDOK1_DP_P[26]
C14 ZDOK1_DP_N[26]
C15 ZDOK1_DP_P[27]
C16 ZDOK1_DP_N[27]
C17 ZDOK1_DP_P[28]
C18 ZDOK1_DP_N[28]
C19 ZDOK1_DP_P[29]
C20 ZDOK1_DP_N[29]
F1 ZDOK1_DP_P[30]
F2 ZDOK1_DP_N[30]
F3 ZDOK1_DP_P[31]
F4 ZDOK1_DP_N[31]
F5 ZDOK1_DP_P[32]
F6 ZDOK1_DP_N[32]
F7 ZDOK1_DP_P[33]
F8 ZDOK1_DP_N[33]
F9 ZDOK1_DP_P[34]
F10 ZDOK1_DP_N[34]
F11 ZDOK1_DP_P[35]
F12 ZDOK1_DP_N[35]
F13 ZDOK1_DP_P[36]
F14 ZDOK1_DP_N[36]
F15 ZDOK1_DP_P[37]
F16 ZDOK1_DP_N[37]
F17 ZDOK1_CLK0_P
F18 ZDOK1_CLK0_N
F19 ZDOK1_CLK1_P
F20 ZDOK1_CLK1_N
6367550-5

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
VTT_0V9
VREF_0V9
1V8
1V8_13
GND
U12
J5
879160001
BANKS=13, 17, 21, 25
R390
R391
49.9R
C558
C559
C560
C561
C562
C563
C564
C565
C566
C567
C568
C569
100NF
10V
10NF
25V
C570
C571
C572
C573
C574
C575
C576
C577
C578
C579
C580
C581
C582
C583
C584
C585
C586
C587
C588
C589
C590
C591
C592
C593
C594
C595
C596
C597
C598
C599
C600
C601
C602
C603
RP13
RP14
RP15
RP16
RP17
RP18
RP19
RP20
RP21
RP22
RP23
RP24
RP25
RP26
RP27
RP28
RP29
RP30
CP20
CP21
CP22
CP23
CP24
CP25
CP26
CP27
CP28
CP29
CP30
CP31
CP32
CP33
CP34
CP35
CP36
CP37
DDR2_A[15]
DDR2_A[0]
DDR2_BA[2]
DDR2_BA[1]
DDR2_BA[0]
DDR2_CS_N_0
DDR2_CS_N_1
DDR2_CAS_N
DDR2_RAS_N
DDR2_DQS_8
DDR2_DQS_N_8
DDR2_DM[8]
DDR2_CK_2_P
DDR2_CK_2_N
DDR2_CK_1_P
DDR2_CK_1_N
DDR2_CK_0_P
DDR2_CK_0_N
DDR2_CKE_2
DDR2_CKE_1
DDR2_CKE_0
DDR2_ODT_1
DDR2_ODT_0
DDR2_WE_N
DDR2_ERROR
DDR2_PHY_INIT_DONE
DDR2_RESET_N
DDR2_DQ[71]
DDR2_DQ[0]
DDR2_DIMM_CB7
DDR2_DIMM_CB0
DDR2_DIMM_DQ[63]
DDR2_DIMM_DQ[0]
DDR2_DIMM_SA2
DDR2_DIMM_SA1
DDR2_DIMM_SA0
DDR2_DIMM_SCL
DDR2_DIMM_SDA
DDR2_DIMM_A[15]
DDR2_DIMM_A[0]
DDR2_DIMM_WE#
DDR2_DIMM_RESET#
DDR2_DIMM_S#[1]
DDR2_DIMM_S#[0]
ERR_OUT
PAR_IN
NC
VREF
VDDSPD
VDD_11
VDD_1
VDDQ_11
VDDQ_1
VSS_64
VSS_1
VRP_13
VRN_13

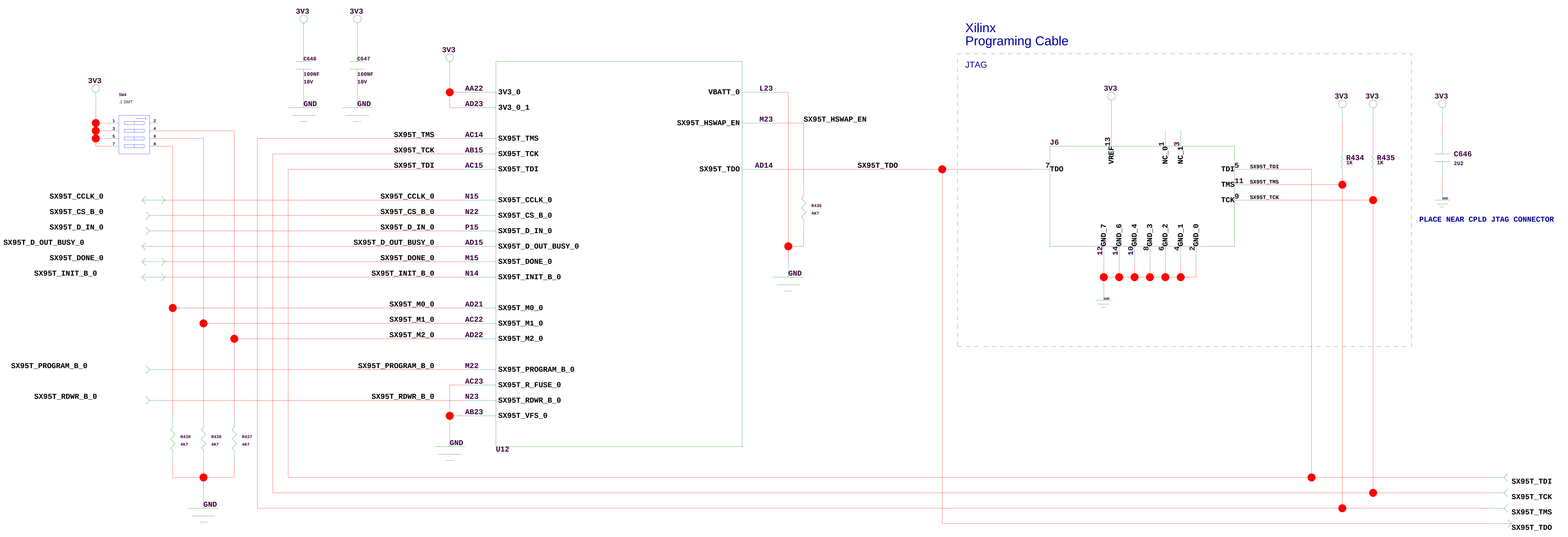

ZDOK0_CLK0_P K18 ZDOK0_CLK0_P
ZDOK0_CLK0_N J19 ZDOK0_CLK0_N
ZDOK0_CLK1_P J16 ZDOK0_CLK1_P
ZDOK0_CLK1_N J17 ZDOK0_CLK1_N
2V5_20
R222
100R
R221
100R
VRP_20 L11 VRP_20
VRN_20 L10 VRN_20
2V5_12
R223
100R
R224
100R
VRP_12_GPIOLVC25 P9 VRP_12_GPIOLVC25
VRN_12_GPIOLVC25 R9 VRN_12_GPIOLVC25
2V5
C416
100NF
10V
C417
100NF
10V
C418
100NF
10V
M9 2V5_12
N6 2V5_12_1
T7 2V5_12_2
E10 2V5_20
H11 2V5_20_1
J8 2V5_20_2
2V5
C421
100NF
10V
C420
100NF
10V
C419
100NF
10V
ZDOK0_DP_P[37] E6 ZDOK0_DP_P[37]
ZDOK0_DP_N[37] E7 ZDOK0_DP_N[37]
ZDOK0_DP_P[36] T9 ZDOK0_DP_P[36]
ZDOK0_DP_N[36] U10 ZDOK0_DP_N[36]
ZDOK0_DP_P[35] G6 ZDOK0_DP_P[35]
ZDOK0_DP_N[35] G7 ZDOK0_DP_N[35]
ZDOK0_DP_P[34] T10 ZDOK0_DP_P[34]
ZDOK0_DP_N[34] T11 ZDOK0_DP_N[34]
ZDOK0_DP_P[33] F5 ZDOK0_DP_P[33]
ZDOK0_DP_N[33] F6 ZDOK0_DP_N[33]
ZDOK0_DP_P[32] R11 ZDOK0_DP_P[32]
ZDOK0_DP_N[32] P10 ZDOK0_DP_N[32]
ZDOK0_DP_P[31] H5 ZDOK0_DP_P[31]
ZDOK0_DP_N[31] G5 ZDOK0_DP_N[31]
ZDOK0_DP_P[30] H7 ZDOK0_DP_P[30]
ZDOK0_DP_N[30] J7 ZDOK0_DP_N[30]
ZDOK0_DP_P[29] T8 ZDOK0_DP_P[29]
ZDOK0_DP_N[29] U7 ZDOK0_DP_N[29]
ZDOK0_DP_P[28] R7 ZDOK0_DP_P[28]
ZDOK0_DP_N[28] R8 ZDOK0_DP_N[28]
ZDOK0_DP_P[27] J6 ZDOK0_DP_P[27]
ZDOK0_DP_N[27] J5 ZDOK0_DP_N[27]
ZDOK0_DP_P[26] R6 ZDOK0_DP_P[26]
ZDOK0_DP_N[26] T6 ZDOK0_DP_N[26]
ZDOK0_DP_P[25] K7 ZDOK0_DP_P[25]
ZDOK0_DP_N[25] K6 ZDOK0_DP_N[25]
ZDOK0_DP_P[24] P7 ZDOK0_DP_P[24]
ZDOK0_DP_N[24] P6 ZDOK0_DP_N[24]
ZDOK0_DP_P[23] L4 ZDOK0_DP_P[23]
ZDOK0_DP_N[23] L5 ZDOK0_DP_N[23]
ZDOK0_DP_P[22] N5 ZDOK0_DP_P[22]
ZDOK0_DP_N[22] P5 ZDOK0_DP_N[22]
ZDOK0_DP_P[21] M7 ZDOK0_DP_P[21]
ZDOK0_DP_N[21] L6 ZDOK0_DP_N[21]
ZDOK0_DP_P[20] N8 ZDOK0_DP_P[20]
ZDOK0_DP_N[20] N7 ZDOK0_DP_N[20]
ZDOK0_DP_P[19] M6 ZDOK0_DP_P[19]
ZDOK0_DP_N[19] M5 ZDOK0_DP_N[19]
ZDOK0_DP_P[18] F13 ZDOK0_DP_P[18]
ZDOK0_DP_N[18] G13 ZDOK0_DP_N[18]
ZDOK0_DP_P[17] N10 ZDOK0_DP_P[17]
ZDOK0_DP_N[17] N9 ZDOK0_DP_N[17]
ZDOK0_DP_P[16] E12 ZDOK0_DP_P[16]
ZDOK0_DP_N[16] E13 ZDOK0_DP_N[16]
ZDOK0_DP_P[15] M10 ZDOK0_DP_P[15]
ZDOK0_DP_N[15] L9 ZDOK0_DP_N[15]
ZDOK0_DP_P[14] F11 ZDOK0_DP_P[14]
ZDOK0_DP_N[14] E11 ZDOK0_DP_N[14]
ZDOK0_DP_P[13] M8 ZDOK0_DP_P[13]
ZDOK0_DP_N[13] L8 ZDOK0_DP_N[13]
ZDOK0_DP_P[12] G11 ZDOK0_DP_P[12]
ZDOK0_DP_N[12] G12 ZDOK0_DP_N[12]
ZDOK0_DP_P[11] B13 ZDOK0_DP_P[11]
ZDOK0_DP_N[11] C13 ZDOK0_DP_N[11]
ZDOK0_DP_P[10] K8 ZDOK0_DP_P[10]
ZDOK0_DP_N[10] K9 ZDOK0_DP_N[10]
ZDOK0_DP_P[9] J10 ZDOK0_DP_P[9]
ZDOK0_DP_N[9] J9 ZDOK0_DP_N[9]
ZDOK0_DP_P[8] A13 ZDOK0_DP_P[8]
ZDOK0_DP_N[8] B12 ZDOK0_DP_N[8]
ZDOK0_DP_P[7] H10 ZDOK0_DP_P[7]
ZDOK0_DP_N[7] H9 ZDOK0_DP_N[7]
ZDOK0_DP_P[6] D12 ZDOK0_DP_P[6]
ZDOK0_DP_N[6] C12 ZDOK0_DP_N[6]
ZDOK0_DP_P[5] K11 ZDOK0_DP_P[5]
ZDOK0_DP_N[5] J11 ZDOK0_DP_N[5]
ZDOK0_DP_P[4] D11 ZDOK0_DP_P[4]
ZDOK0_DP_N[4] D10 ZDOK0_DP_N[4]
ZDOK0_DP_P[3] G8 ZDOK0_DP_P[3]
ZDOK0_DP_N[3] H8 ZDOK0_DP_N[3]
ZDOK0_DP_P[2] F10 ZDOK0_DP_P[2]
ZDOK0_DP_N[2] G10 ZDOK0_DP_N[2]
ZDOK0_DP_P[1] F9 ZDOK0_DP_P[1]
ZDOK0_DP_N[1] F8 ZDOK0_DP_N[1]
ZDOK0_DP_P[0] E9 ZDOK0_DP_P[0]
ZDOK0_DP_N[0] E8 ZDOK0_DP_N[0]
U12
BANKS=20, 12


5V0
C423
1UF
16V
C422
100NF
10V
3V3
C425
1UF
16V
C424
100NF
10V
2V5
C426
1UF
16V
C427
100NF
10V
1V8
C429
1UF
16V
C428
100NF
10V
P8
W1 X1 Y1 Z1 W2 X2 Y2 Z2 W3 X3 Y3 Z3 W4 X4 Y4 Z4 W5 X5 Y5 Z5 W6 X6 Y6 Z6
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20
E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20
6367550-5
ZDOK40
P8
ZDOK0_DP_P[0] A1
ZDOK0_DP_N[0] A2
ZDOK0_DP_P[1] A3
ZDOK0_DP_N[1] A4
ZDOK0_DP_P[2] A5
ZDOK0_DP_N[2] A6
ZDOK0_DP_P[3] A7
ZDOK0_DP_N[3] A8
ZDOK0_DP_P[4] A9
ZDOK0_DP_N[4] A10
ZDOK0_DP_P[5] A11
ZDOK0_DP_N[5] A12
ZDOK0_DP_P[6] A13
ZDOK0_DP_N[6] A14
ZDOK0_DP_P[7] A15
ZDOK0_DP_N[7] A16
ZDOK0_DP_P[8] A17
ZDOK0_DP_N[8] A18
ZDOK0_DP_P[9] A19
ZDOK0_DP_N[9] A20
ZDOK0_DP_P[10] D1
ZDOK0_DP_N[10] D2
ZDOK0_DP_P[11] D3
ZDOK0_DP_N[11] D4
ZDOK0_DP_P[12] D5
ZDOK0_DP_N[12] D6
ZDOK0_DP_P[13] D7
ZDOK0_DP_N[13] D8
ZDOK0_DP_P[14] D9
ZDOK0_DP_N[14] D10
ZDOK0_DP_P[15] D11
ZDOK0_DP_N[15] D12
ZDOK0_DP_P[16] D13
ZDOK0_DP_N[16] D14
ZDOK0_DP_P[17] D15
ZDOK0_DP_N[17] D16
ZDOK0_DP_P[18] D17
ZDOK0_DP_N[18] D18
ZDOK0_DP_P[19] D19
ZDOK0_DP_N[19] D20
C1 ZDOK0_DP_P[20]
C2 ZDOK0_DP_N[20]
C3 ZDOK0_DP_P[21]
C4 ZDOK0_DP_N[21]
C5 ZDOK0_DP_P[22]
C6 ZDOK0_DP_N[22]
C7 ZDOK0_DP_P[23]
C8 ZDOK0_DP_N[23]
C9 ZDOK0_DP_P[24]
C10 ZDOK0_DP_N[24]
C11 ZDOK0_DP_P[25]
C12 ZDOK0_DP_N[25]
C13 ZDOK0_DP_P[26]
C14 ZDOK0_DP_N[26]
C15 ZDOK0_DP_P[27]
C16 ZDOK0_DP_N[27]
C17 ZDOK0_DP_P[28]
C18 ZDOK0_DP_N[28]
C19 ZDOK0_DP_P[29]
C20 ZDOK0_DP_N[29]
F1 ZDOK0_DP_P[30]
F2 ZDOK0_DP_N[30]
F3 ZDOK0_DP_P[31]
F4 ZDOK0_DP_N[31]
F5 ZDOK0_DP_P[32]
F6 ZDOK0_DP_N[32]
F7 ZDOK0_DP_P[33]
F8 ZDOK0_DP_N[33]
F9 ZDOK0_DP_P[34]
F10 ZDOK0_DP_N[34]
F11 ZDOK0_DP_P[35]
F12 ZDOK0_DP_N[35]
F13 ZDOK0_DP_P[36]
F14 ZDOK0_DP_N[36]
F15 ZDOK0_DP_P[37]
F16 ZDOK0_DP_N[37]
F17 ZDOK0_CLK0_P
F18 ZDOK0_CLK0_N
F19 ZDOK0_CLK1_P
F20 ZDOK0_CLK1_N
6367550-5

TBD

VALID CONFIGURATION MODES

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input


3V3
3V3
C648
100NF
10V
GND
C647
100NF
10V
GND
3V3
SW4
.1 SMT
1
2
3
4
5
6
7
8
AA22
AD23
3V3_0
3V3_0_1
SX95T_TMS
AC14
SX95T_TMS
SX95T_TCK
AB15
SX95T_TCK
SX95T_TDI
AC15
SX95T_TDI
SX95T_CCLK_0
SX95T_CCLK_0
N15
SX95T_CCLK_0
SX95T_CS_B_0
SX95T_CS_B_0
N22
SX95T_CS_B_0
SX95T_D_IN_0
SX95T_D_IN_0
P15
SX95T_D_IN_0
SX95T_D_OUT_BUSY_0
SX95T_D_OUT_BUSY_0
AD15
SX95T_D_OUT_BUSY_0
SX95T_DONE_0
SX95T_DONE_0
M15
SX95T_DONE_0
SX95T_INIT_B_0
SX95T_INIT_B_0
N14
SX95T_INIT_B_0
SX95T_M0_0
AD21
SX95T_M0_0
SX95T_M1_0
AC22
SX95T_M1_0
SX95T_M2_0
AD22
SX95T_M2_0
SX95T_PROGRAM_B_0
SX95T_PROGRAM_B_0
M22
SX95T_PROGRAM_B_0
AC23
SX95T_R_FUSE_0
SX95T_RDWR_B_0
SX95T_RDWR_B_0
N23
SX95T_RDWR_B_0
AB23
SX95T_VFS_0
GND
U12
R439
4K7
R438
4K7
R437
4K7
GND
VBATT_0
L23
SX95T_HSWAP_EN
M23
SX95T_HSWAP_EN
SX95T_TDO
AD14
SX95T_TDO
R436
4K7
GND
Xilinx
Programing Cable
JTAG
3V3
J6
13
VREF
1
NC_0
3
NC_1
7
TDO
TDI
5
SX95T_TDI
TMS
11
SX95T_TMS
TCK
9
SX95T_TCK
12
GND_7
14
GND_6
10
GND_4
8
GND_3
6
GND_2
4
GND_1
2
GND_0
GND
3V3
3V3
R434
1K
R435
1K
3V3
C646
2U2
GND
PLACE NEAR CPLD JTAG CONNECTOR
SX95T_TDI
SX95T_TCK
SX95T_TMS
SX95T_TDO