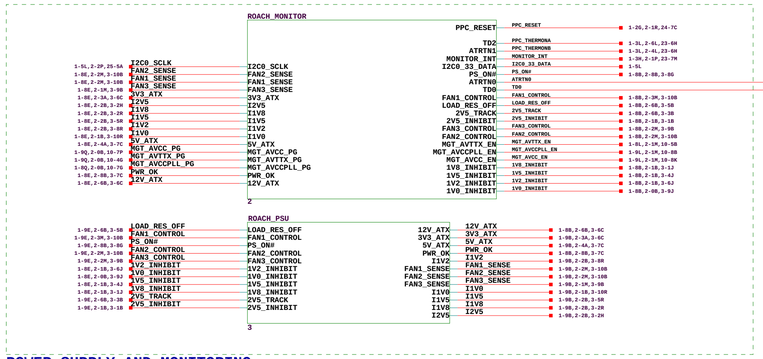
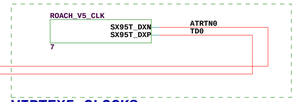
VIRTEX5

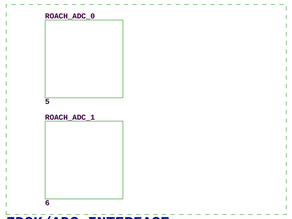
POWER SUPPLY AND MONITORING



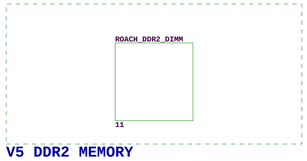
VIRTEX5 CLOCKS



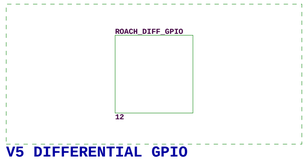
ZDOK/ADC INTERFACE



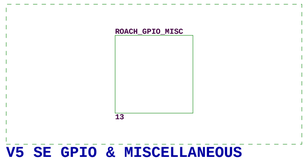
V5 DDR2 MEMORY



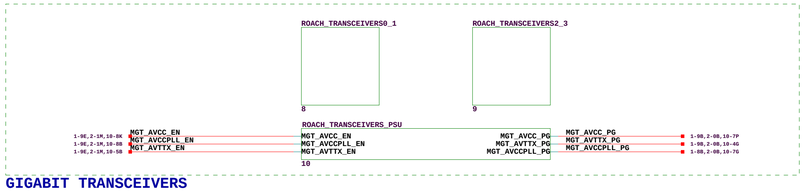
V5 DIFFERENTIAL GPIO



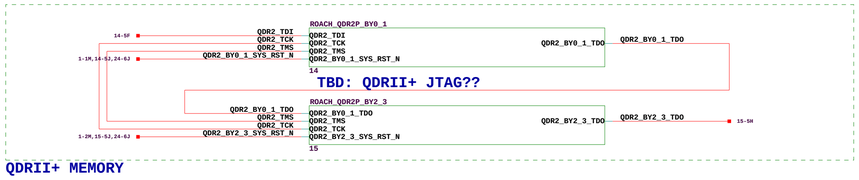
V5 SE GPIO & MISCELLANEOUS



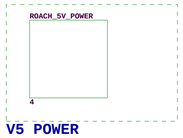
GIGABIT TRANSCEIVERS



QDRII+ MEMORY

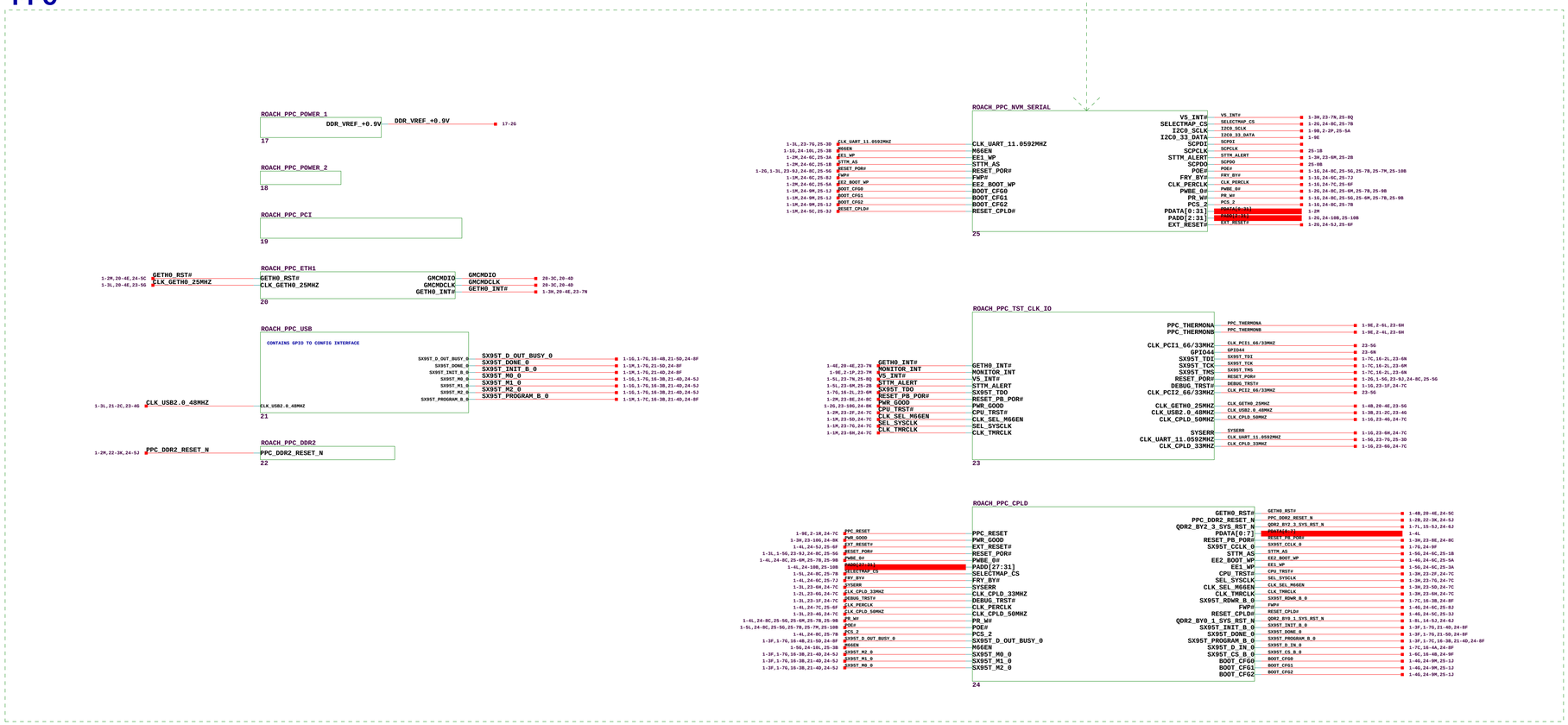


V5 POWER

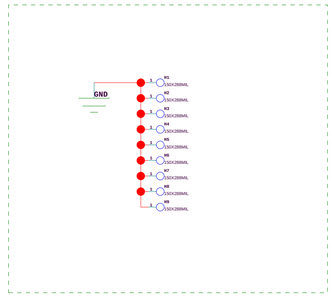


VIRTEX5 CONFIGURATION

PPC



MECHANICAL



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HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2	**ROACH_TOP**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-15-2007_17:29	DRAWN: F KAPP · APPR:
PATH PATH	CHECKED: E BAUERMEISTER · SHEET 1 OF 25

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

TIE TO GROUND IF PLL'S ARE NOT USED

PLACE AT ACTEL 3V3 POWER PINS

PLACE AT ACTEL 1V5 POWER PINS

roach_AFS600_powerpins

roach_AFS600_pcb

roach_AFS600_configpins

PB POWER SWITCH

KEY - REMOVE PIN

MONITOR RESET

XPORT - PLACE IN REAR I/O REGION

TEMPERATURE DIODE HEADER

ACTEL JTAG CONNECTOR

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

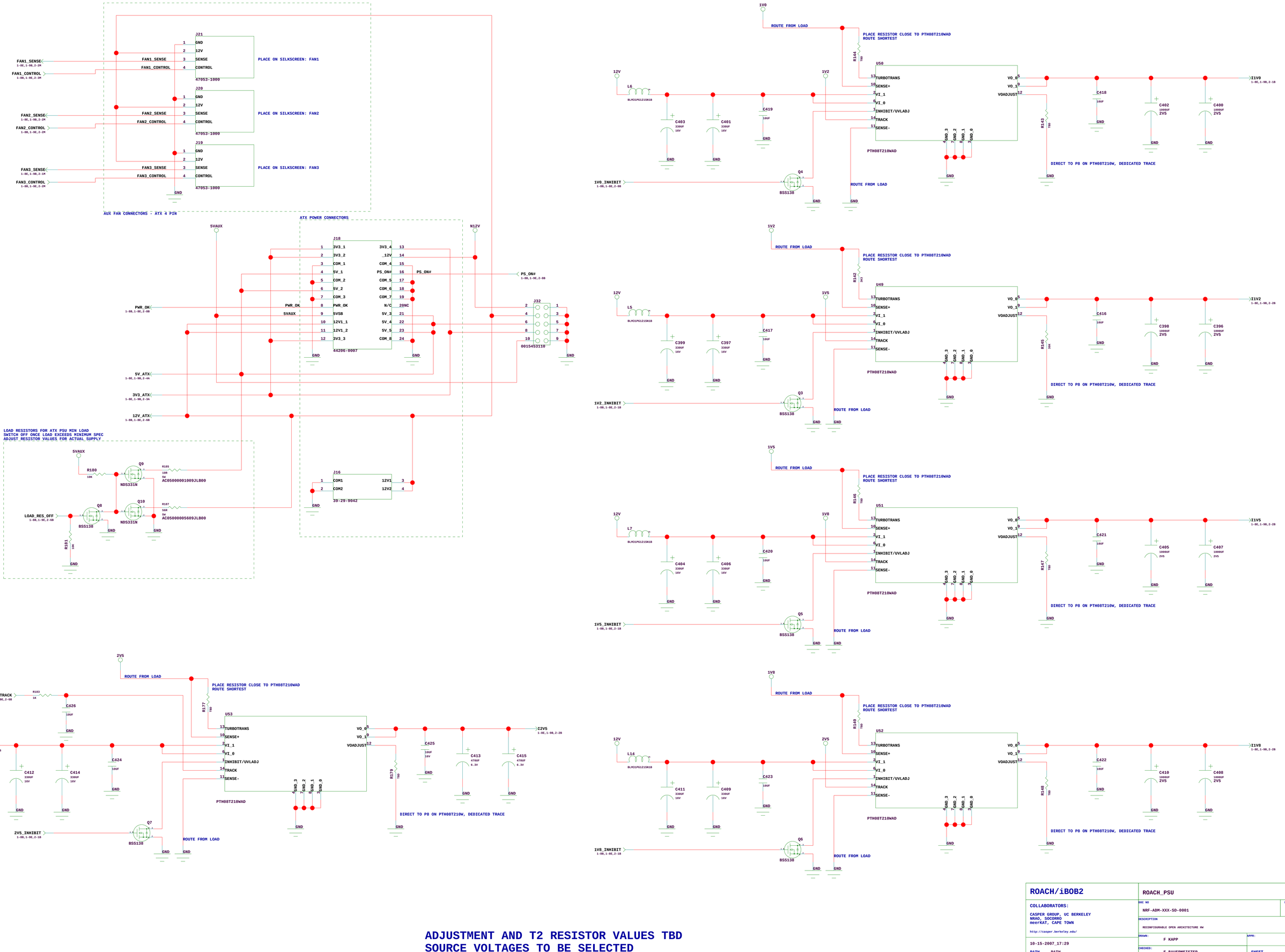
http://casper.berkeley.edu/

10-15-2007_17:29

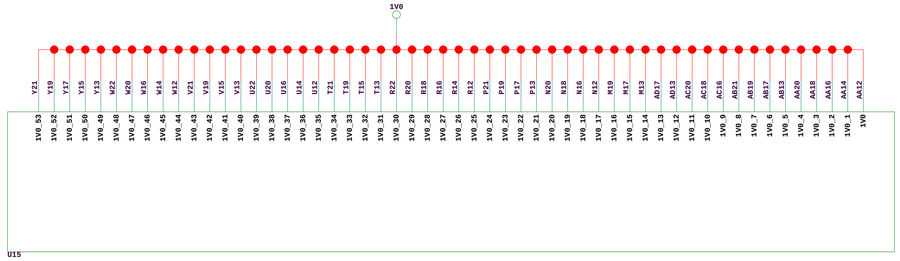
PATH PATH

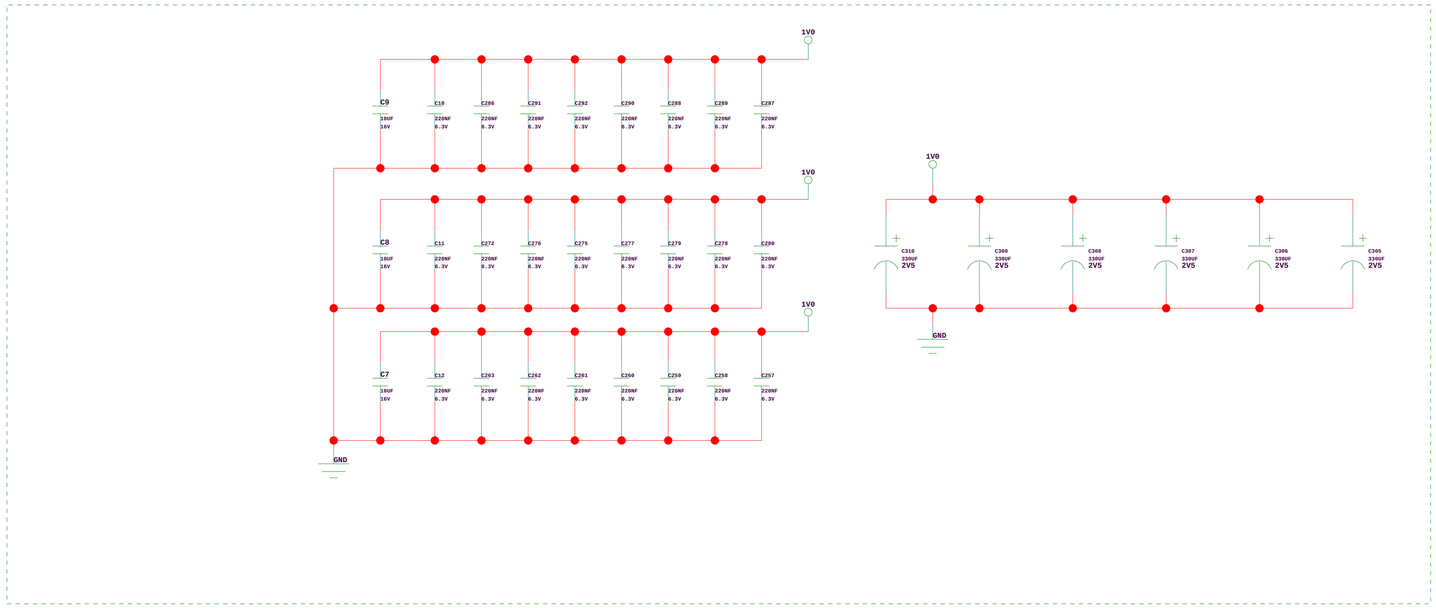
ROACH_MONITOR

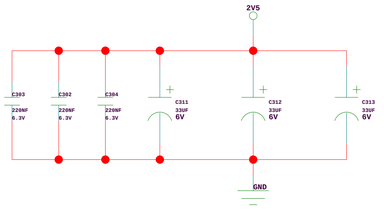
DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	2 OF 25

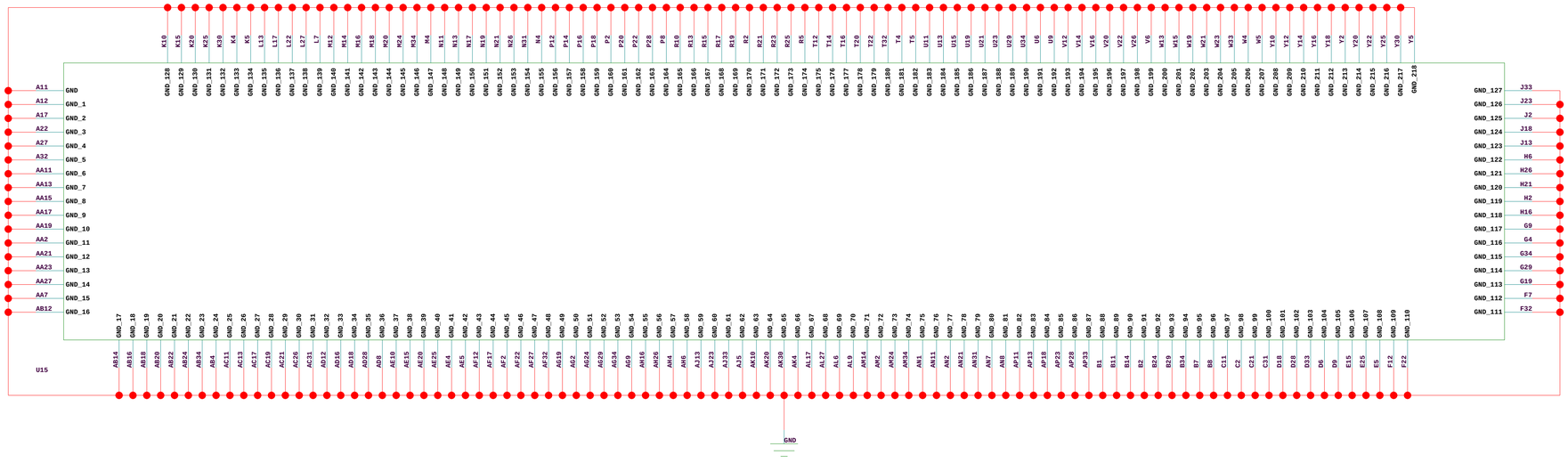


ROACH/iBOB2	ROACH_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE RW
10-15-2007_17:29	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 3 OF 25









ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
10-15-2007_17:29 PATH PATH	

ZDOK0_DP_P[37]	E6	ZDOK0_DP_P[37]	ZDOK0_DP_P[0]	A1	C1 ZDOK0_DP_P[20]
ZDOK0_DP_N[37]	E7	ZDOK0_DP_N[37]	ZDOK0_DP_N[0]	A2	C2 ZDOK0_DP_N[20]
ZDOK0_DP_P[36]	T9	ZDOK0_DP_P[36]	ZDOK0_DP_P[1]	A3	C3 ZDOK0_DP_P[21]
ZDOK0_DP_N[36]	U10	ZDOK0_DP_N[36]	ZDOK0_DP_N[1]	A4	C4 ZDOK0_DP_N[21]
ZDOK0_DP_P[35]	G6	ZDOK0_DP_P[35]	ZDOK0_DP_P[2]	A5	C5 ZDOK0_DP_P[22]
ZDOK0_DP_N[35]	G7	ZDOK0_DP_N[35]	ZDOK0_DP_N[2]	A6	C6 ZDOK0_DP_N[22]
ZDOK0_DP_P[34]	T10	ZDOK0_DP_P[34]	ZDOK0_DP_P[3]	A7	C7 ZDOK0_DP_P[23]
ZDOK0_DP_N[34]	T11	ZDOK0_DP_N[34]	ZDOK0_DP_N[3]	A8	C8 ZDOK0_DP_N[23]
ZDOK0_DP_P[33]	F5	ZDOK0_DP_P[33]	ZDOK0_DP_P[4]	A9	C9 ZDOK0_DP_P[24]
ZDOK0_DP_N[33]	F6	ZDOK0_DP_N[33]	ZDOK0_DP_N[4]	A10	C10 ZDOK0_DP_N[24]
ZDOK0_DP_P[32]	R11	ZDOK0_DP_P[32]	ZDOK0_DP_P[5]	A11	C11 ZDOK0_DP_P[25]
ZDOK0_DP_N[32]	P10	ZDOK0_DP_N[32]	ZDOK0_DP_N[5]	A12	C12 ZDOK0_DP_N[25]
ZDOK0_DP_P[31]	H5	ZDOK0_DP_P[31]	ZDOK0_DP_P[6]	A13	C13 ZDOK0_DP_P[26]
ZDOK0_DP_N[31]	G5	ZDOK0_DP_N[31]	ZDOK0_DP_N[6]	A14	C14 ZDOK0_DP_N[26]
ZDOK0_DP_P[30]	H7	ZDOK0_DP_P[30]	ZDOK0_DP_P[7]	A15	C15 ZDOK0_DP_P[27]
ZDOK0_DP_N[30]	J7	ZDOK0_DP_N[30]	ZDOK0_DP_N[7]	A16	C16 ZDOK0_DP_N[27]
ZDOK0_DP_P[29]	T8	ZDOK0_DP_P[29]	ZDOK0_DP_P[8]	A17	C17 ZDOK0_DP_P[28]
ZDOK0_DP_N[29]	U7	ZDOK0_DP_N[29]	ZDOK0_DP_N[8]	A18	C18 ZDOK0_DP_N[28]
ZDOK0_DP_P[28]	R7	ZDOK0_DP_P[28]	ZDOK0_DP_P[9]	A19	C19 ZDOK0_CLK0_P 5-7B
ZDOK0_DP_N[28]	R8	ZDOK0_DP_N[28]	ZDOK0_DP_N[9]	A20	C20 ZDOK0_CLK0_N 5-7B
ZDOK0_DP_P[27]	J6	ZDOK0_DP_P[27]	ZDOK0_DP_P[10]	D1	F1 ZDOK0_DP_P[29]
ZDOK0_DP_N[27]	J5	ZDOK0_DP_N[27]	ZDOK0_DP_N[10]	D2	F2 ZDOK0_DP_N[29]
ZDOK0_DP_P[26]	R6	ZDOK0_DP_P[26]	ZDOK0_DP_P[11]	D3	F3 ZDOK0_DP_P[30]
ZDOK0_DP_N[26]	T6	ZDOK0_DP_N[26]	ZDOK0_DP_N[11]	D4	F4 ZDOK0_DP_N[30]
ZDOK0_DP_P[25]	K7	ZDOK0_DP_P[25]	ZDOK0_DP_P[12]	D5	F5 ZDOK0_DP_P[31]
ZDOK0_DP_N[25]	K6	ZDOK0_DP_N[25]	ZDOK0_DP_N[12]	D6	F6 ZDOK0_DP_N[31]
ZDOK0_DP_P[24]	P7	ZDOK0_DP_P[24]	ZDOK0_DP_P[13]	D7	F7 ZDOK0_DP_P[32]
ZDOK0_DP_N[24]	P6	ZDOK0_DP_N[24]	ZDOK0_DP_N[13]	D8	F8 ZDOK0_DP_N[32]
ZDOK0_DP_P[23]	L4	ZDOK0_DP_P[23]	ZDOK0_DP_P[14]	D9	F9 ZDOK0_DP_P[33]
ZDOK0_DP_N[23]	L5	ZDOK0_DP_N[23]	ZDOK0_DP_N[14]	D10	F10 ZDOK0_DP_N[33]
ZDOK0_DP_P[22]	N5	ZDOK0_DP_P[22]	ZDOK0_DP_P[15]	D11	F11 ZDOK0_DP_P[34]
ZDOK0_DP_N[22]	P5	ZDOK0_DP_N[22]	ZDOK0_DP_N[15]	D12	F12 ZDOK0_DP_N[34]
ZDOK0_DP_P[21]	M7	ZDOK0_DP_P[21]	ZDOK0_DP_P[16]	D13	F13 ZDOK0_DP_P[35]
ZDOK0_DP_N[21]	L6	ZDOK0_DP_N[21]	ZDOK0_DP_N[16]	D14	F14 ZDOK0_DP_N[35]
ZDOK0_DP_P[20]	N8	ZDOK0_DP_P[20]	ZDOK0_DP_P[17]	D15	F15 ZDOK0_DP_P[36]
ZDOK0_DP_N[20]	N7	ZDOK0_DP_N[20]	ZDOK0_DP_N[17]	D16	F16 ZDOK0_DP_N[36]
ZDOK0_DP_P[19]	M6	ZDOK0_DP_P[19]	ZDOK0_DP_P[18]	D17	F17 ZDOK0_DP_P[37]
ZDOK0_DP_N[19]	M5	ZDOK0_DP_N[19]	ZDOK0_DP_N[18]	D18	F18 ZDOK0_DP_N[37]
ZDOK0_DP_P[18]	F13	ZDOK0_DP_P[18]	ZDOK0_DP_P[19]	D19	F19 ZDOK0_CLK1_P 5-7B
ZDOK0_DP_N[18]	G13	ZDOK0_DP_N[18]	ZDOK0_DP_N[19]	D20	F20 ZDOK0_CLK1_N 5-7B
ZDOK0_DP_P[17]	N10	ZDOK0_DP_P[17]			
ZDOK0_DP_N[17]	N9	ZDOK0_DP_N[17]			
ZDOK0_DP_P[16]	E12	ZDOK0_DP_P[16]			
ZDOK0_DP_N[16]	E13	ZDOK0_DP_N[16]			
ZDOK0_DP_P[15]	M10	ZDOK0_DP_P[15]			
ZDOK0_DP_N[15]	L9	ZDOK0_DP_N[15]			
ZDOK0_DP_P[14]	F11	ZDOK0_DP_P[14]			
ZDOK0_DP_N[14]	E11	ZDOK0_DP_N[14]			
ZDOK0_DP_P[13]	M8	ZDOK0_DP_P[13]			
ZDOK0_DP_N[13]	L8	ZDOK0_DP_N[13]			
ZDOK0_DP_P[12]	G11	ZDOK0_DP_P[12]			
ZDOK0_DP_N[12]	G12	ZDOK0_DP_N[12]			
ZDOK0_DP_P[11]	B13	ZDOK0_DP_P[11]			
ZDOK0_DP_N[11]	C13	ZDOK0_DP_N[11]			
ZDOK0_DP_P[10]	K8	ZDOK0_DP_P[10]			
ZDOK0_DP_N[10]	K9	ZDOK0_DP_N[10]			
ZDOK0_DP_P[9]	J10	ZDOK0_DP_P[9]			
ZDOK0_DP_N[9]	J9	ZDOK0_DP_N[9]			
ZDOK0_DP_P[8]	A13	ZDOK0_DP_P[8]			
ZDOK0_DP_N[8]	B12	ZDOK0_DP_N[8]			
ZDOK0_DP_P[7]	H10	ZDOK0_DP_P[7]			
ZDOK0_DP_N[7]	H9	ZDOK0_DP_N[7]			
ZDOK0_DP_P[6]	D12	ZDOK0_DP_P[6]			
ZDOK0_DP_N[6]	C12	ZDOK0_DP_N[6]			
ZDOK0_DP_P[5]	K11	ZDOK0_DP_P[5]			
ZDOK0_DP_N[5]	J11	ZDOK0_DP_N[5]			
ZDOK0_DP_P[4]	D11	ZDOK0_DP_P[4]			
ZDOK0_DP_N[4]	D10	ZDOK0_DP_N[4]			
ZDOK0_DP_P[3]	G8	ZDOK0_DP_P[3]			
ZDOK0_DP_N[3]	H8	ZDOK0_DP_N[3]			
ZDOK0_DP_P[2]	F10	ZDOK0_DP_P[2]			
ZDOK0_DP_N[2]	G10	ZDOK0_DP_N[2]			
ZDOK0_DP_P[1]	F9	ZDOK0_DP_P[1]			
ZDOK0_DP_N[1]	F8	ZDOK0_DP_N[1]			
ZDOK0_DP_P[0]	E9	ZDOK0_DP_P[0]			
ZDOK0_DP_N[0]	E8	ZDOK0_DP_N[0]			

W1	W1	B1	B1	E1	E1		
X1	X1	B2	B2	E2	E2		
Y1	Y1	B3	B3	E3	E3		
Z1	Z1	B4	B4	E4	E4		
W2	W2	B5	B5	E5	E5		
X2	X2	B6	B6	E6	E6		
Y2	Y2	B7	B7	E7	E7		
Z2	Z2	B8	B8	E8	E8		
W3	W3	B9	B9	E9	E9		
X3	X3	B10	B10	E10	E10		
Y3	Y3	B11	B11	E11	E11		
Z3	Z3	B12	B12	E12	E12		
W4	W4	B13	B13	E13	E13		
X4	X4	B14	B14	E14	E14		
Y4	Y4	B15	B15	E15	E15		
Z4	Z4	B16	B16	E16	E16		
W5	W5	B17	B17	E17	E17		
X5	X5	B18	B18	E18	E18		
Y5	Y5	B19	B19	E19	E19		
Z5	Z5	B20	B20	E20	E20		
W6	W6						
X6	X6						
Y6	Y6						
Z6	Z6						

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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PATH PATH

ROACH_ADC_0

DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 5 OF 25

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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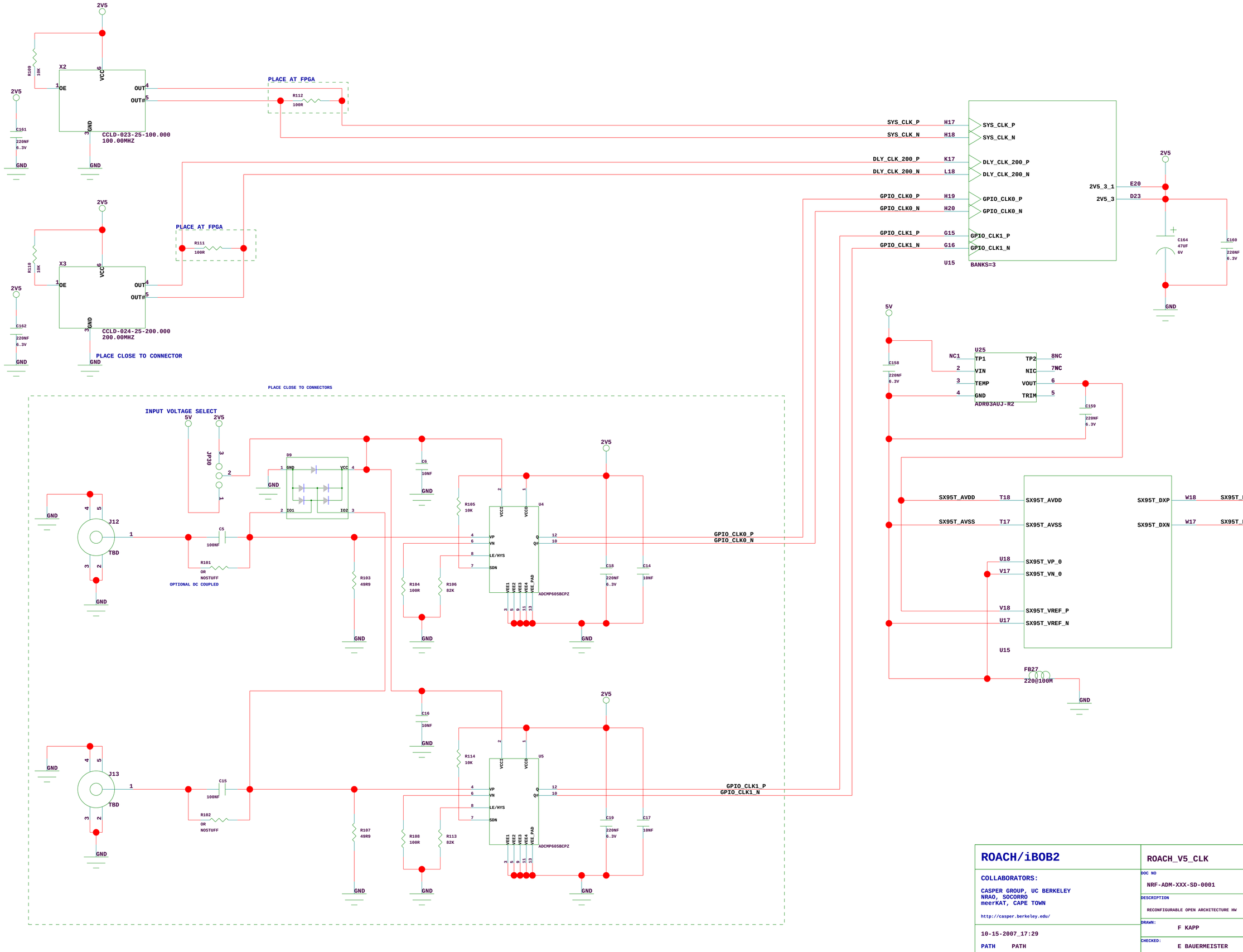
PATH PATH

ROACH_ADC_1

DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET: 6 OF 25

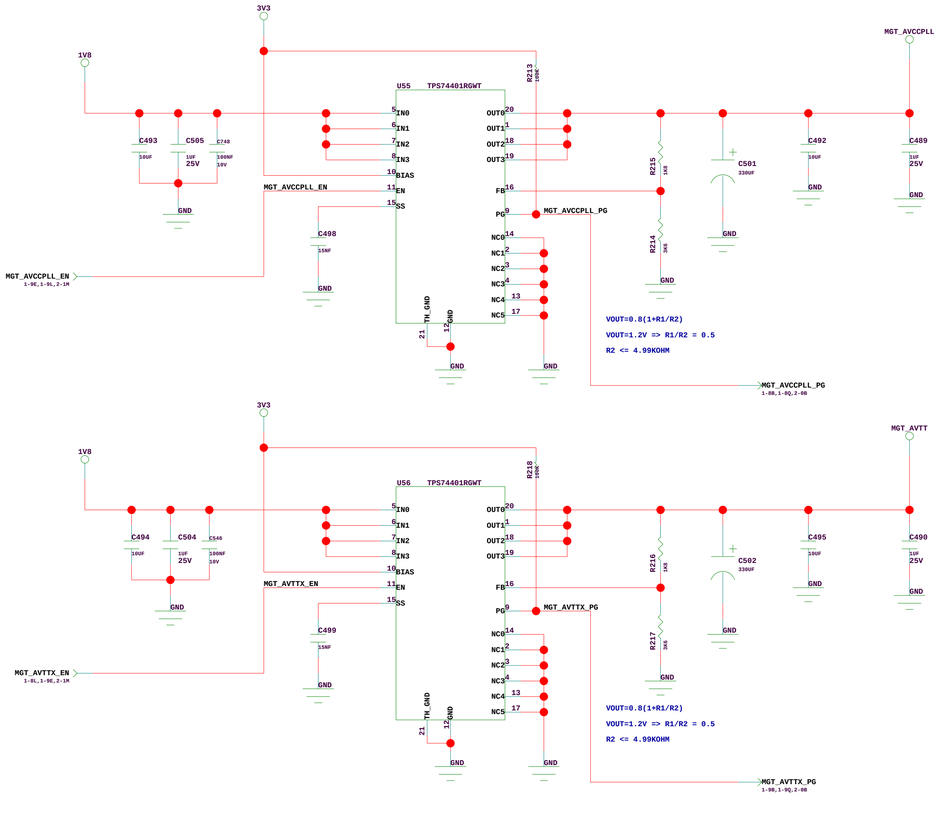


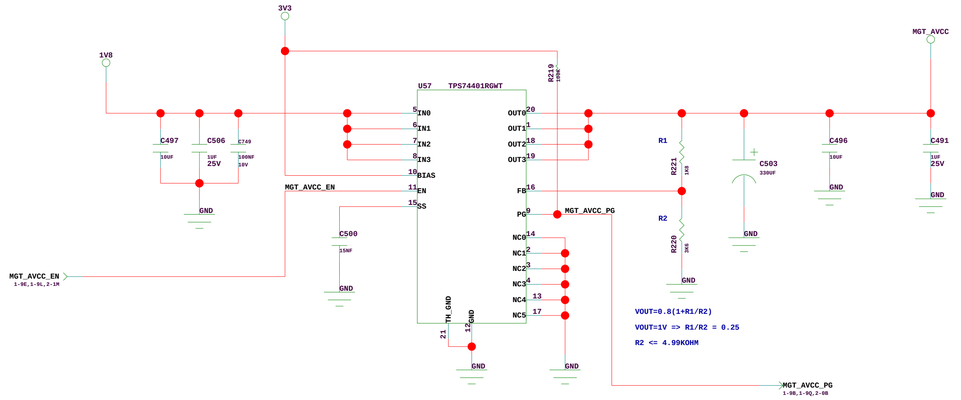
ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
10-15-2007_17:29 PATH PATH	

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB3 220@100M
FB4 220@100M
C94 220NF 6.3V
C93 220NF 6.3V
C92 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_112 R3
MGTAVCC_112_1 R4
MGTAVCCPLL_112 T3
MGTAVTTRX_112 N3
MGT_112_REF_CLK_P P4
MGT_112_REF_CLK_N P3
MGTRX0_112_P N1
MGTRX0_112_N P1
MGTRX1_112_P T1
MGTRX1_112_N R1
U15
MGTAVCC_112
MGTAVCC_112_1
MGTAVCCPLL_112
MGTAVTTRX_112
MGT_112_REF_CLK_P
MGT_112_REF_CLK_N
MGTRX0_112_P
MGTRX0_112_N
MGTRX1_112_P
MGTRX1_112_N
MGTRREF V4
MGT_VTRXC V5
MGTAVTTTX_112 M3
MGTAVTTTX_112_1 U3
MGTTX0_112_P M2
MGTTX0_112_N N2
MGTTX1_112_P U2
MGTTX1_112_N T2
MGTRREF
MGT_VTRXC
MGTAVTTTX_112
MGTAVTTTX_112_1
MGTTX0_112_P
MGTTX0_112_N
MGTTX1_112_P
MGTTX1_112_N
R56 49.9R
MGT_AVTT
FB25 220@100M
FB5 220@100M
C125 220NF 6.3V
C95 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
2V5
FB26 220@100M
C137 220NF 6.3V
R84 10K
X1
OE
VCC
OUT
OUT#
GND
CCLD-023-25-156.250
156.25MHZ
JP6
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
C104 10NF 25V
C105 10NF 25V
C106 10NF 25V
C107 10NF 25V
C109 10NF 25V
C108 10NF 25V
P3
SL0P S1
SL0N S2
SL1P S3
SL1N S4
SL2P S5
SL2N S6
SL3P S7
SL3N S8
SL4P S16
SL4N S15
SL5P S14
SL5N S13
SL6P S12
SL6N S11
SL7P S10
SL7N S9
FCN-268F036-G/3DB
SIG_GND1 G1
SIG_GND2 G2
SIG_GND3 G3
SIG_GND4 G4
SIG_GND5 G5
SIG_GND6 G6
SIG_GND7 G7
SIG_GND8 G8
SIG_GND9 G9
SIG_GND10 G19
ODIS0
FAULT0
G4 AND G8 CONNECTED IN 2X2 MODULE
JP4
C130 10NF
R50 10K
GND
3V3
R79 150R
D2
OPTICAL MODULE FAULT - RED LED
C131 10NF
R97 5K1
RS7 3K9
RS9 6K8
RS8 3K9
U21 MAX9032AKA
U20 MAX9032AKA
C127 10NF
U22 AND2 SN74AHC1G08DCKR
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB11 220@100M
FB9 220@100M
FB10 220@100M
C102 220NF 6.3V
C101 220NF 6.3V
C100 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_114 AA3
MGTAVCC_114_1 AA4
MGTAVCCPLL_114 AB3
MGTAVTTRX_114 W3
MGT_114_REF_CLK_P NC Y4
MGT_114_REF_CLK_N NC Y3
MGTRX0_114_P W1
MGTRX0_114_N Y1
MGTRX1_114_P AB1
MGTRX1_114_N AA1
U15
MGTAVCC_114
MGTAVCC_114_1
MGTAVCCPLL_114
MGTAVTTRX_114
MGT_114_REF_CLK_P
MGT_114_REF_CLK_N
MGTRX0_114_P
MGTRX0_114_N
MGTRX1_114_P
MGTRX1_114_N
MGTAVTTTX_114 AC3
MGTAVTTTX_114_1 V3
MGTTX0_114_P V2
MGTTX0_114_N W2
MGTTX1_114_P AC2
MGTTX1_114_N AB2
MGTAVTTTX_114
MGTAVTTTX_114_1
MGTTX0_114_P
MGTTX0_114_N
MGTTX1_114_P
MGTTX1_114_N
MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT
MGT_AVTT
FB8 220@100M
C99 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
C140 10NF 25V
C141 10NF 25V
C142 10NF 25V
C143 10NF 25V
P3
SL8P S19
SL8N S20
SL9P S21
SL9N S22
SL10P S23
SL10N S24
SL11P S25
SL11N S26
SL12P S34
SL12N S33
SL13P S32
SL13N S31
SL14P S30
SL14N S29
SL15P S28
SL15N S27
FCN-268F036-G/3DB
SIG_GND1 G10
SIG_GND2 G11
SIG_GND3 G12
SIG_GND4 G13
SIG_GND5 G14
SIG_GND6 G15
SIG_GND7 G16
SIG_GND8 G17
SIG_GND9 G18
SIG_GND10 G19
ODIS1
FAULT1
G4 AND G8 CONNECTED IN 2X2 MODULE
JP5
C134 10NF
R51 10K
GND
3V3
R82 150R
D3
OPTICAL MODULE FAULT - RED LED
C132 10NF
R98 5K1
R93 3K9
R94 6K8
R95 3K9
U23 AND2 SN74AHC1G08DCKR
C133 10NF
U18 TPS2031D
U19 TPS2031D
R99 10K
R100 10K
C129 10NF
C128 100NF
C138 4.7UF 16V
C90 22UF
C135 10NF
C136 100NF
C139 4.7UF 16V
C91 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB17 220@100M
FB15 220@100M
FB16 220@100M
C119 220NF 6.3V
C118 220NF 6.3V
C115 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_116 J3
MGTAVCC_116_1 J4
MGTAVCCPLL_116 K3
MGTAVTTRX_116 G3
MGT_116_REF_CLK_P NC H4
MGT_116_REF_CLK_N NC H3
MGTRX0_116_P G1
MGTRX0_116_N H1
MGTRX1_116_P K1
MGTRX1_116_N J1
U15
MGTAVCC_116
MGTAVCC_116_1
MGTAVCCPLL_116
MGTAVTTRX_116
MGT_116_REF_CLK_P
MGT_116_REF_CLK_N
MGTRX0_116_P
MGTRX0_116_N
MGTRX1_116_P
MGTRX1_116_N
MGTAVTTTX_116_1 L3
MGTAVTTTX_116 F3
MGTTX0_116_P F2
MGTTX0_116_N G2
MGTTX1_116_P L2
MGTTX1_116_N K2
MGTAVTTTX_116_1
MGTAVTTTX_116
MGTTX0_116_P
MGTTX0_116_N
MGTTX1_116_P
MGTTX1_116_N
MGT_AVTT
FB14 220@100M
C116 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
C110 10NF 25V
C111 10NF 25V
C112 10NF 25V
C113 10NF 25V
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB22 220@100M
FB24 220@100M
FB23 220@100M
C123 220NF 6.3V
C114 220NF 6.3V
C125 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_118 AG3
MGTAVCC_118_1 AG4
MGTAVCCPLL_118 AH3
MGTAVTTRX_118 AE3
MGT_118_REF_CLK_P NC AF4
MGT_118_REF_CLK_N NC AF3
MGTRX0_118_P AE1
MGTRX0_118_N AF1
MGTRX1_118_P AH1
MGTRX1_118_N AG1
U15
MGTAVCC_118
MGTAVCC_118_1
MGTAVCCPLL_118
MGTAVTTRX_118
MGT_118_REF_CLK_P
MGT_118_REF_CLK_N
MGTRX0_118_P
MGTRX0_118_N
MGTRX1_118_P
MGTRX1_118_N
MGTAVTTTX_118_1 AJ3
MGTAVTTTX_118 AD3
MGTTX0_118_P AD2
MGTTX0_118_N AE2
MGTTX1_118_P AJ2
MGTTX1_118_N AH2
MGTAVTTTX_118_1
MGTAVTTTX_118
MGTTX0_118_P
MGTTX0_118_N
MGTTX1_118_P
MGTTX1_118_N
MGT_AVTT
FB19 220@100M
C121 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
C144 10NF 25V
C145 10NF 25V
C146 10NF 25V
C147 10NF 25V

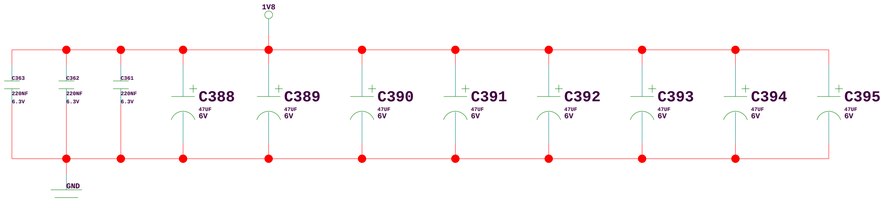
ROACH/iBOB2	**ROACH_TRANSCEIVERS0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 8 OF 25
10-15-2007_17:29	
PATH PATH	

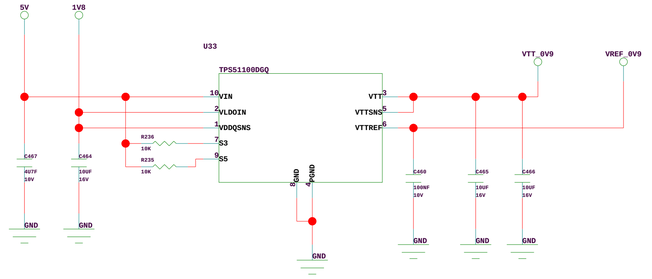
ROACH/iBOB2	**ROACH_TRANSCEIVERS2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 9 OF 25
10-15-2007_17:29	
PATH PATH	

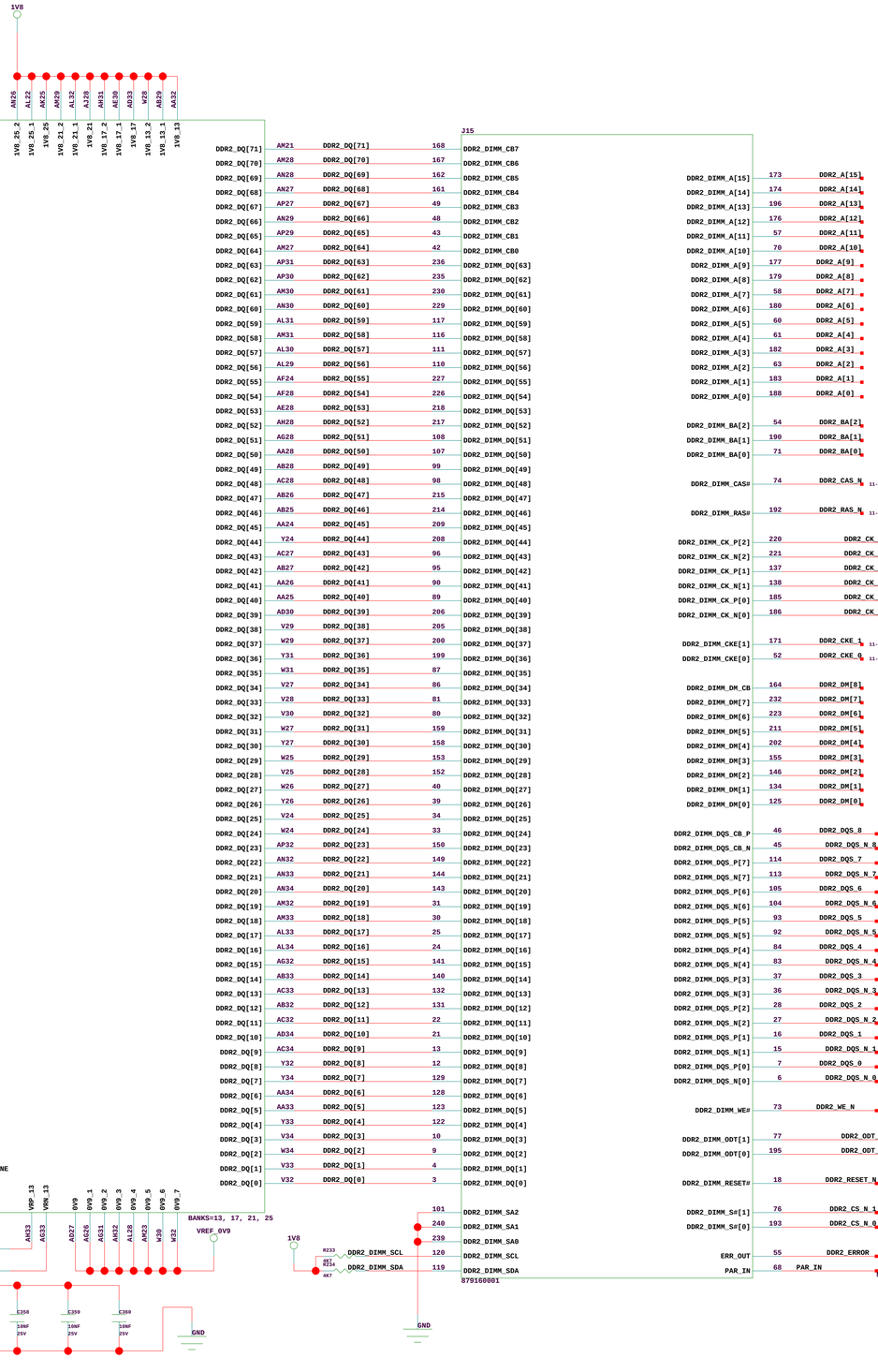


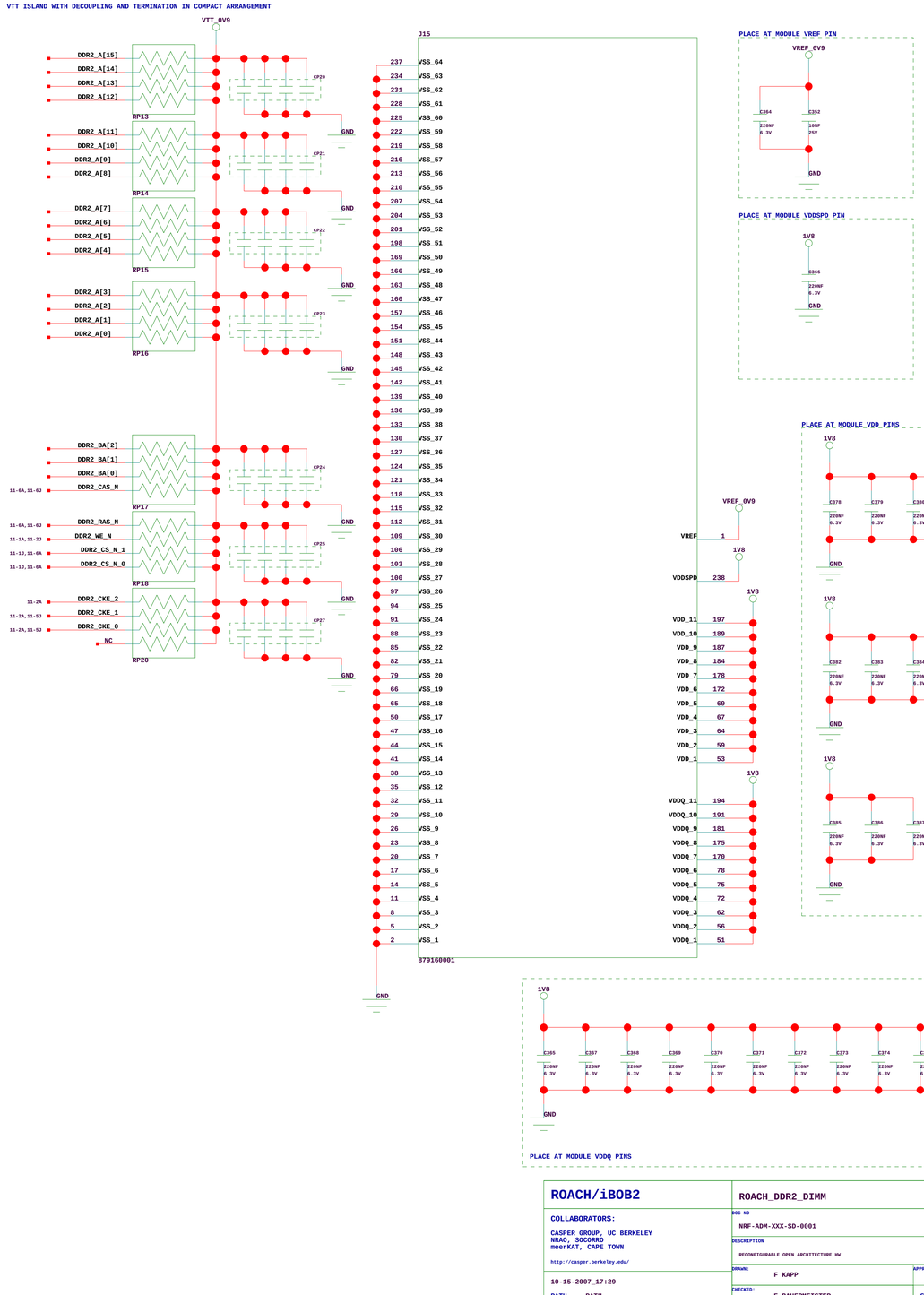


ROACH/iBOB2	**ROACH_TRANSCEIVERS_PSU**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE NW
10-15-2007_17:29	DRAWN: F KAPP · APPR:
PATH PATH	CHECKED: E BAUERMEISTER · SHEET 10 OF 25

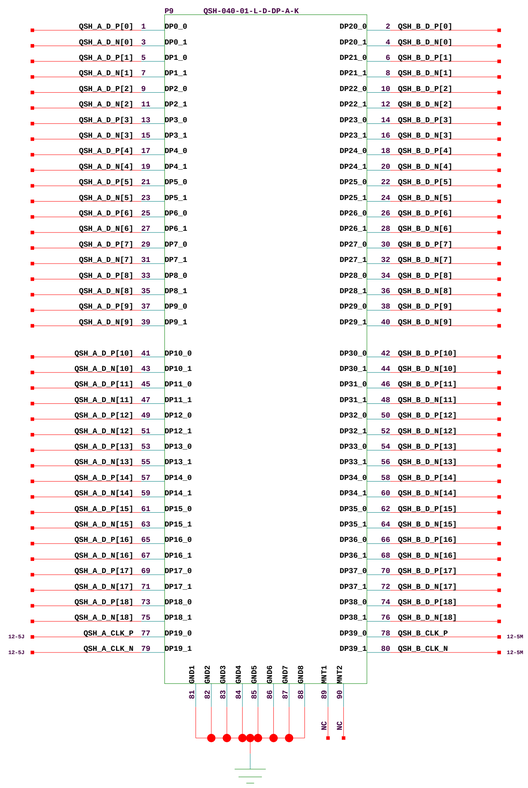


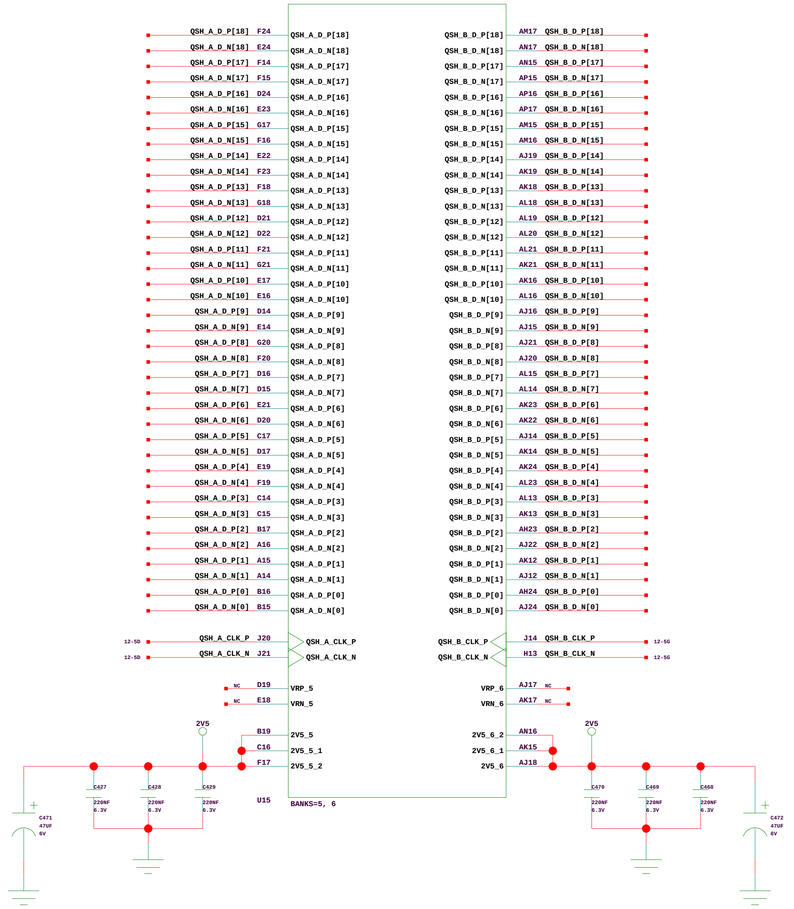






ROACH/iBOB2	ROACH_DDR2_DIMM
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-15-2007_17:29 PATH PATH	DRAWN: F KAPP APPR:
	CHECKED: E BAUERMEISTER SHEET 11 OF 25





ROACH/iBOB2	**ROACH_DIFF_GPIO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-15-2007_17:29 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 12 OF 25

GPIOLVC18[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

GPIOLVC18[20] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

IO VOLTAGE LEVEL SELECT

1-2: 3.3V
2-3: 2.5V

GPIOLVC18[4] IS DUAL FUNCTION:
1. DRIVES LED
2. CONTROLS DIRECTION ON GPIOLVC33[1-4]

IF CR10 IS ON, CLOCK CAPABLE GPIO'S ARE OUTPUTS

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

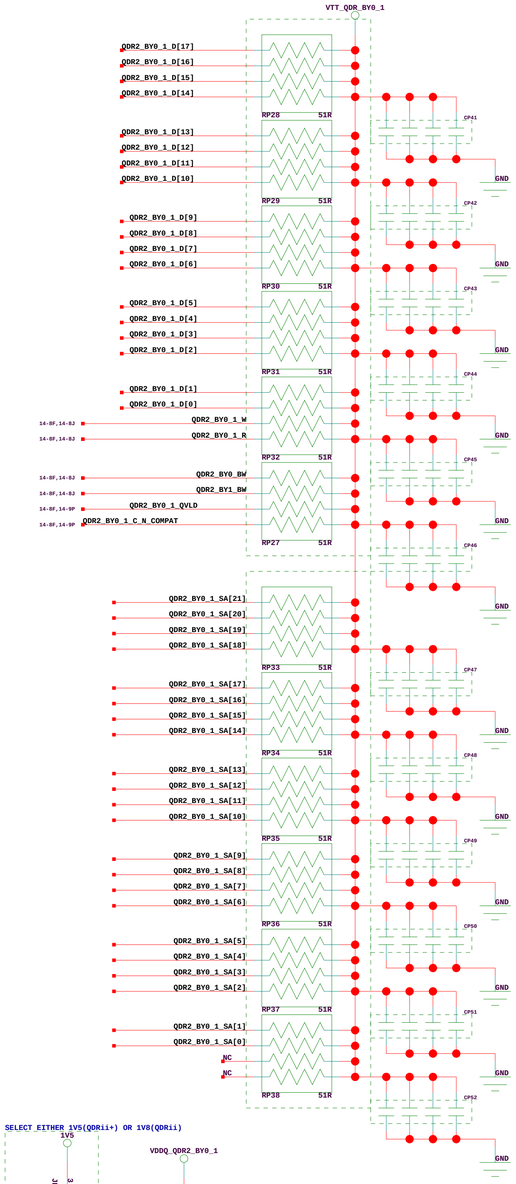
http://casper.berkeley.edu/

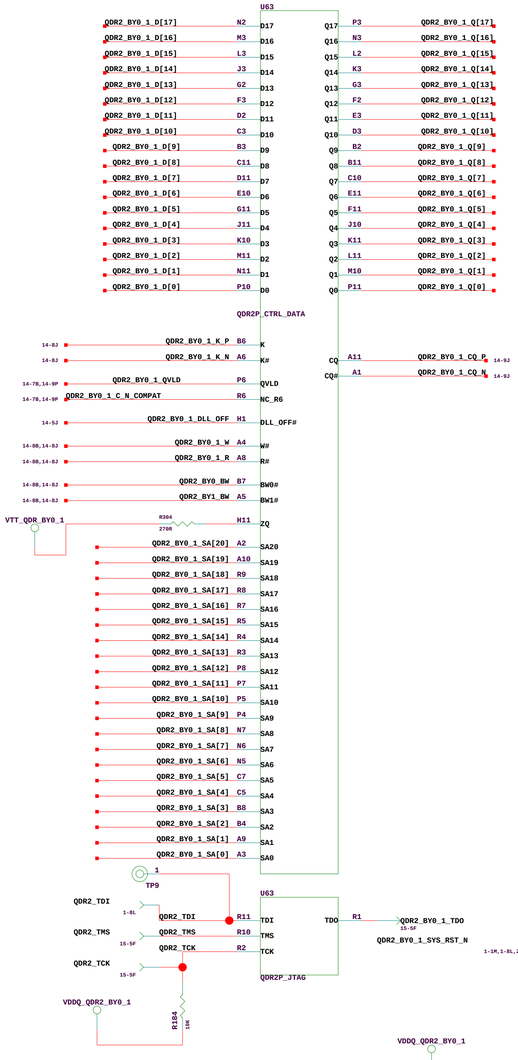
10-15-2007_17:29

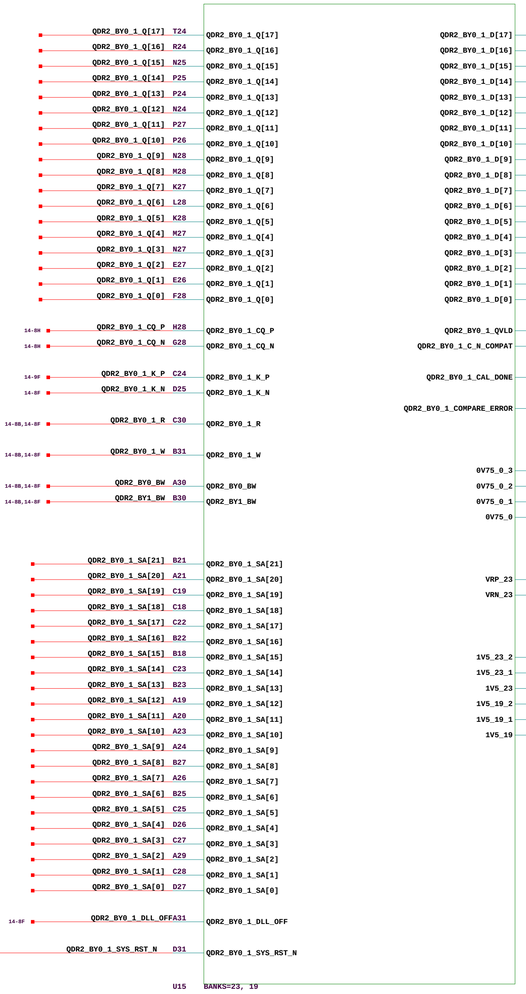
PATH PATH

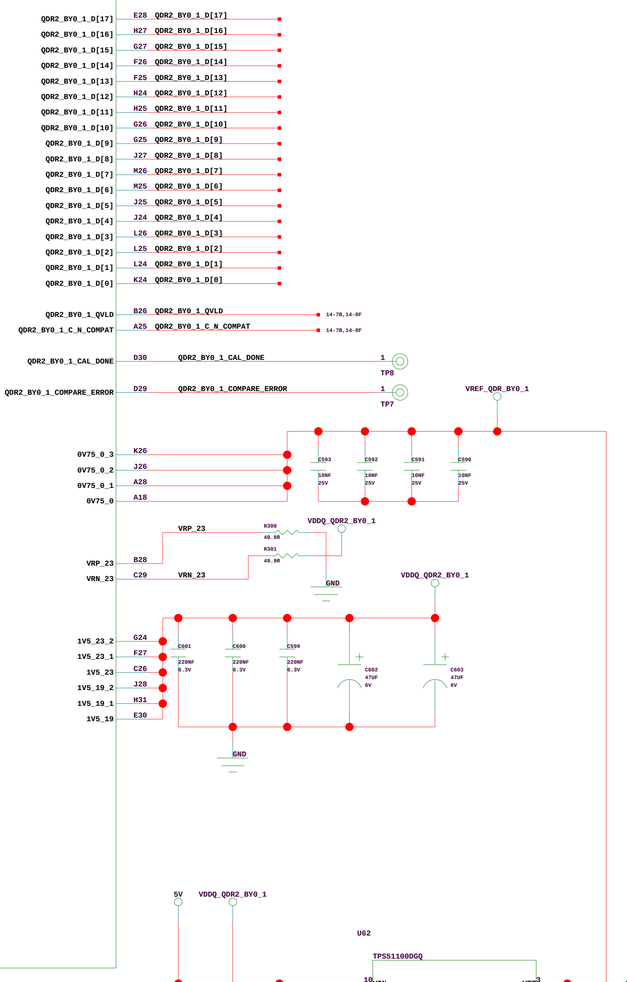
ROACH_GPIO_MISC

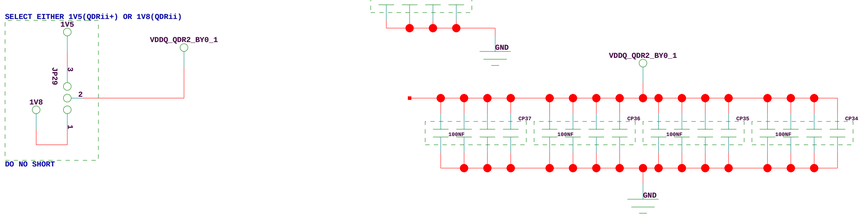
DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	13 OF 25

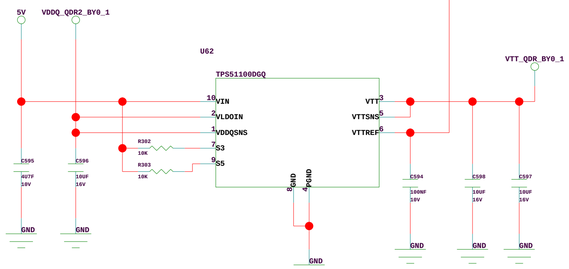




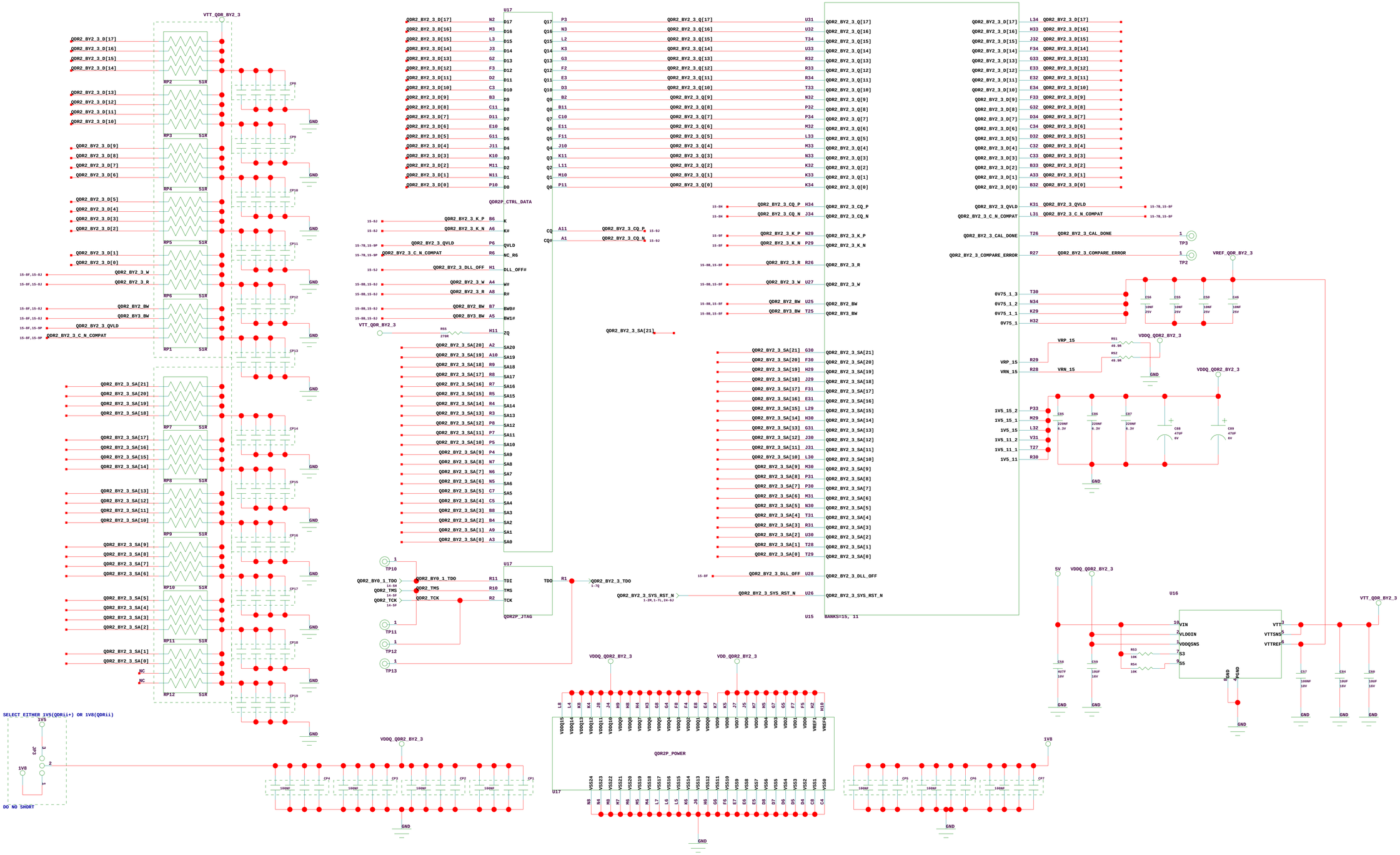








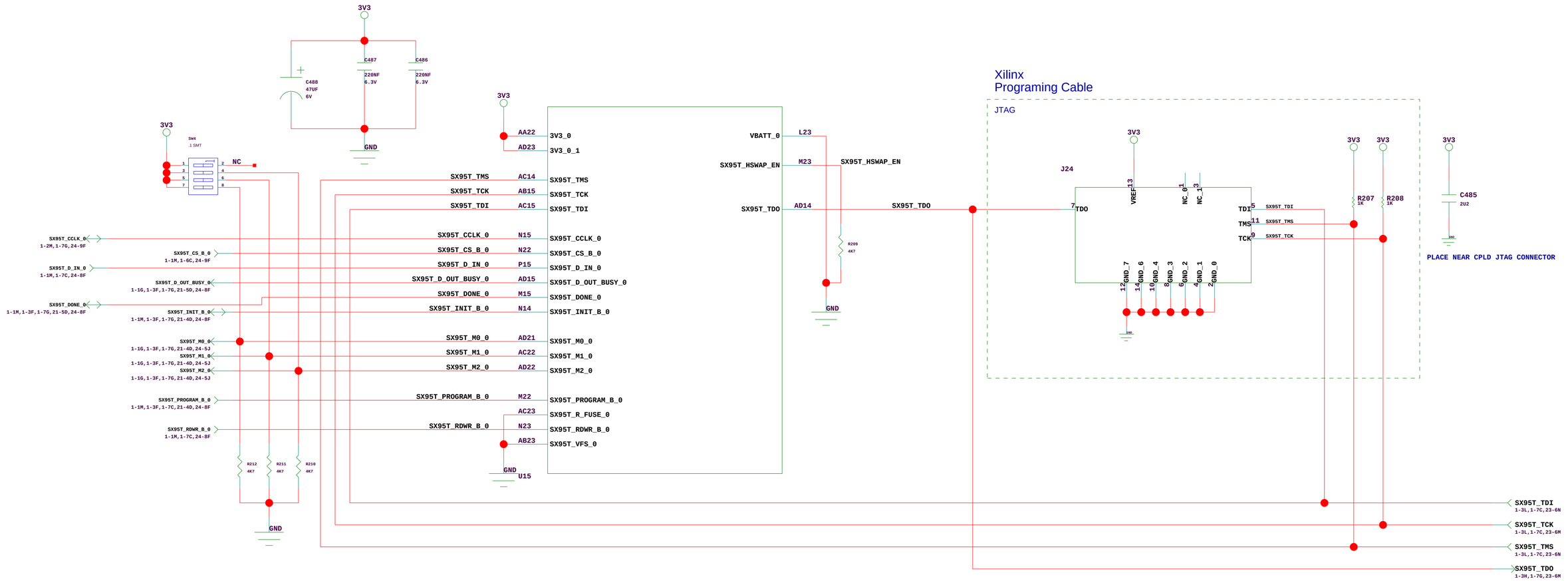
ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 14 OF 25
10-15-2007_17:29 PATH PATH	



ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET: 15 OF 25
10-15-2007_17:29 PATH PATH	

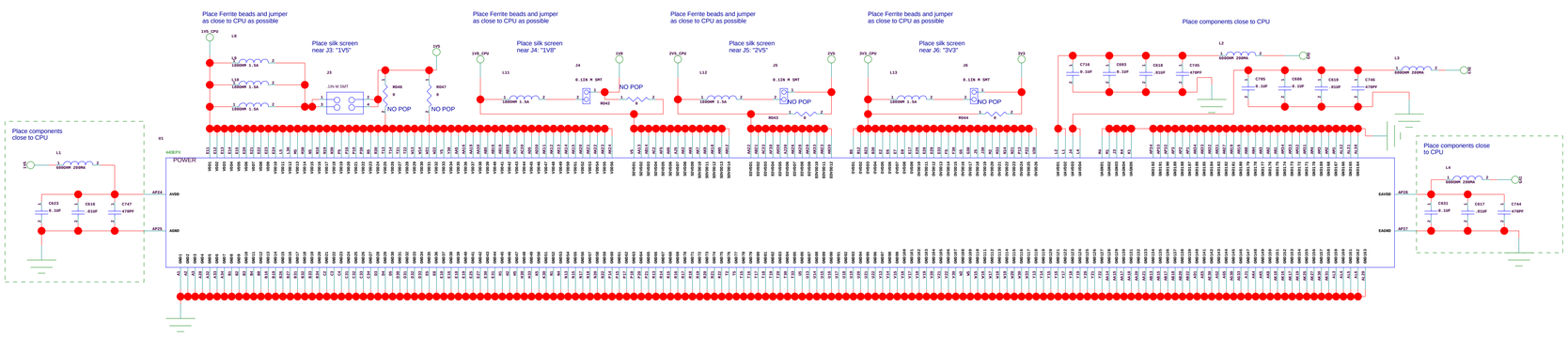
TBD

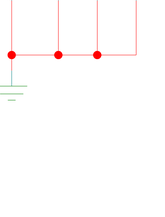
VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

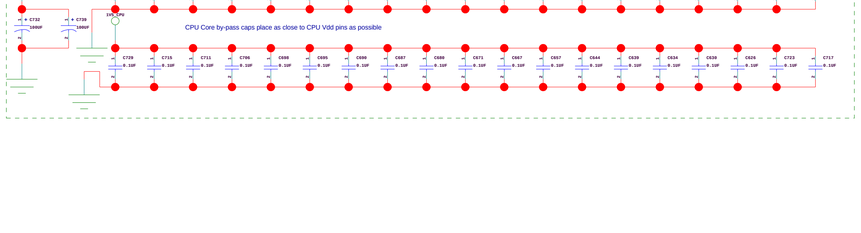


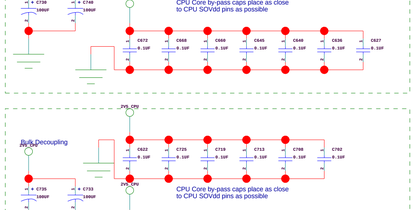
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
10-15-2007_17:29 PATH PATH	

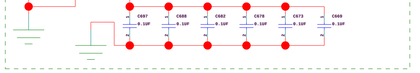
REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

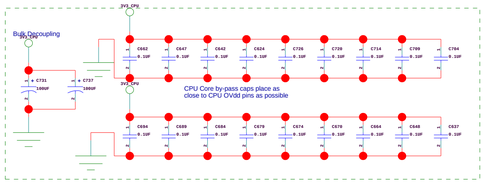


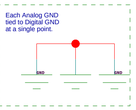


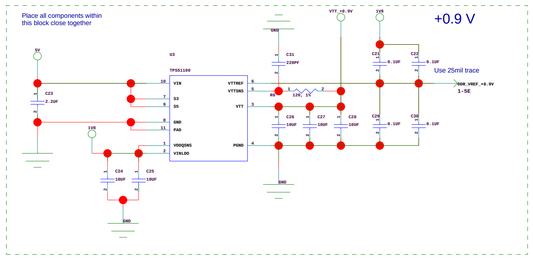


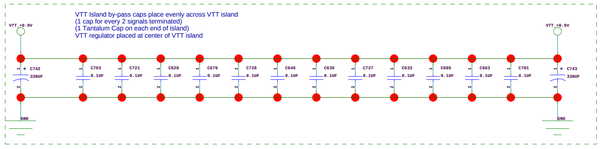






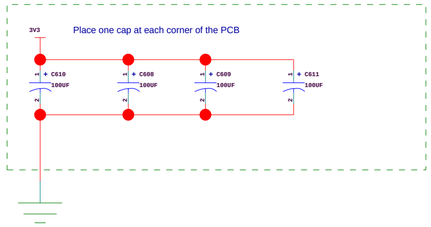






ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 17 OF 25
10-15-2007_17:29	
PATH PATH	

REMOVED 3V3 GENERATION



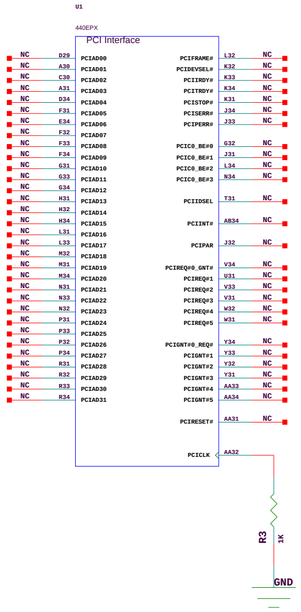
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET 18 OF 25
10-15-2007_17:29 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-15-2007_17:29 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

ROACH/iBOB2

ROACH_PPC_ETH1

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

10-15-2007_17:29

PATH PATH

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 20 OF 25

U1

USB 2.0 DEVICE

440EPX

USB2CLK — A5 — NC

GPIO28/USB2TXVAL — C6 — NC
USB2TXRDY_REFEN — B6

USB2RXACT_HOLDREQ_RCVINH — D7 — NC
USB2RXVAL_LEAKTEST2 — C8 — NC
GPIO27/USB2RXERR_EXTREQ# — A4 — SX95T_DONE_0 ↔ SX95T_DONE_0
1-1M,1-3F,1-7G,24-8F

GPIO30/USB2XCVRSEL_EXTACK# — M3 — SX95T_INIT_B_0 ↔ SX95T_INIT_B_0
GPIO31/USB2TERMSEL_BUSREQ — P4
1-1M,1-3F,1-7G,24-8F

USB2LS0_DRVINH1 — R2 — NC — SX95T_M0_0 → SX95T_M0_0
USB2LS1_LEAKTEST_HOLDPRI — P1 — NC
1-1G,1-3F,1-7G,16-3B,24-5J

GPIO32/USB2OM0 — R3 — SX95T_M1_0 → SX95T_M1_0
GPIO33/USB2OM1 — R4
1-1G,1-3F,1-7G,16-3B,24-5J

GPIO29/USB2SUSP_HOLDACK — C5 — SX95T_M2_0 → SX95T_M2_0
1-1G,1-3F,1-7G,16-3B,24-5J

SX95T_PROGRAM_B_0 → SX95T_PROGRAM_B_0
1-1M,1-3F,1-7C,16-3B,24-8F

NOTE:

USB HOST ONLY

USB 2.0 PHY
HOST/DEVICE

USB2XCVR — J2 — USB2_XCVR_D+
USB2XCVR# — J1 — USB2_XCVR_D-
USB2REXT — L3 — R182 3.40K, 1% — CHASSIS_GND
USB2XTAL — N2
USB2XTAL# — N3

CLK_USB2.0_48MHZ
1-3B,1-3L,23-4G

CRITICAL PLACEMENT

Place SP2 very close to P6

SP2 — PGB102ST23WR
SP2 — PGB102ST23WR

5V — PTC1 1206L050 500MA

C614 220UF 10V
C612 100NF 10V
C613 1NF 50V

VR4 5.5V 20A
VR3 5.5V 20A

P6
1X4 USBA
1 VCC
2 D-
3 D+
4 GND
5
6
292303-1

CHASSIS_GND

ROACH/iBOB2	ROACH_PPC_USB
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET 21 OF 25
10-15-2007_17:29 PATH PATH	

DDR_PA[15:0]

DDR_PD0[63:0]

U1

DDR SDRAM

64DEPX

DDR_PD0	AB2	MEMDATA00	MEMADDR00	AM5	DDR_PA0
DDR_PD1	AP22	MEMDATA01	MEMADDR01	AP4	DDR_PA1
DDR_PD2	AM26	MEMDATA02	MEMADDR02	AM6	DDR_PA2
DDR_PD3	AL28	MEMDATA03	MEMADDR03	AM8	DDR_PA3
DDR_PD4	AL22	MEMDATA04	MEMADDR04	AP6	DDR_PA4
DDR_PD5	AM22	MEMDATA05	MEMADDR05	AN6	DDR_PA5
DDR_PD6	AM31	MEMDATA06	MEMADDR06	AL7	DDR_PA6
DDR_PD7	AP31	MEMDATA07	MEMADDR07	AN7	DDR_PA7
DDR_PD8	AP39	MEMDATA08	MEMADDR08	AM7	DDR_PA8
DDR_PD9	AL38	MEMDATA09	MEMADDR09	AP7	DDR_PA9
DDR_PD10	AN17	MEMDATA10	MEMADDR10	AL2	DDR_PA10
DDR_PD11	AP17	MEMDATA11	MEMADDR11	AL8	DDR_PA11
DDR_PD12	AN20	MEMDATA12	MEMADDR12	AM4	DDR_PA12
DDR_PD13	AP19	MEMDATA13	MEMADDR13	AN4	DDR_PA13
DDR_PD14	AN18	MEMDATA14			
DDR_PD15	AL15	MEMDATA15			
DDR_PD16	AM16	MEMDATA16			
DDR_PD17	AP15	MEMDATA17			
DDR_PD18	AP14	MEMDATA18			
DDR_PD19	AL17	MEMDATA19			
DDR_PD20	AM17	MEMDATA20			
DDR_PD21	AN13	MEMDATA21			
DDR_PD22	AM15	MEMDATA22			
DDR_PD23	AM13	MEMDATA23			
DDR_PD24	AP11	MEMDATA24			
DDR_PD25	AN11	MEMDATA25			
DDR_PD26	AP12	MEMDATA26			
DDR_PD27	AL12	MEMDATA27			
DDR_PD28	AM14	MEMDATA28			
DDR_PD29	AM24	MEMDATA29			
DDR_PD30	AL13	MEMDATA30			
DDR_PD31	AM12	MEMDATA31			
DDR_PD32	AF3	MEMDATA32			
DDR_PD33	AF1	MEMDATA33			
DDR_PD34	AD4	MEMDATA34			
DDR_PD35	AD3	MEMDATA35			
DDR_PD36	AB3	MEMDATA36			
DDR_PD37	AF2	MEMDATA37			
DDR_PD38	AE2	MEMDATA38			
DDR_PD39	AE1	MEMDATA39			
DDR_PD40	AC3	MEMDATA40			
DDR_PD41	AC1	MEMDATA41			
DDR_PD42	AA4	MEMDATA42			
DDR_PD43	AA3	MEMDATA43			
DDR_PD44	AD2	MEMDATA44			
DDR_PD45	AC4	MEMDATA45			
DDR_PD46	AB1	MEMDATA46			
DDR_PD47	AB2	MEMDATA47			
DDR_PD48	Y3	MEMDATA48			
DDR_PD49	Y2	MEMDATA49			
DDR_PD50	Y4	MEMDATA50			
DDR_PD51	V3	MEMDATA51			
DDR_PD52	AA2	MEMDATA52			
DDR_PD53	AA1	MEMDATA53			
DDR_PD54	W3	MEMDATA54			
DDR_PD55	W1	MEMDATA55			
DDR_PD56	V1	MEMDATA56			
DDR_PD57	U2	MEMDATA57			
DDR_PD58	T4	MEMDATA58			
DDR_PD59	R1	MEMDATA59			
DDR_PD60	V5	MEMDATA60			
DDR_PD61	T1	MEMDATA61			
DDR_PD62	T3	MEMDATA62			
DDR_PD63	T2	MEMDATA63			

BA0	AJ23	DDR_PBA0	22-8K,22-8L
BA1	AK3	DDR_PBA1	22-8K,22-8L
BA2	AP8	DDR_PBA2	22-8K,22-8L
RAS#	AJ4	DDR_PRAS#	22-7K,22-7L
CAS#	AN4	DDR_PCAS#	22-7L,22-8K
WE#	AJ2	DDR_PWE#	22-3K,22-7L
DM0	AL21	DDR_PDM0	22-5K
DM1	AP18	DDR_PDM1	22-6K
DM2	AP15	DDR_PDM2	22-6K
DM3	AL14	DDR_PDM3	22-6K
DM4	AD4	DDR_PDM4	22-6K
DM5	AB3	DDR_PDM5	22-6K
DM6	Y3	DDR_PDM6	22-6K
DM7	V3	DDR_PDM7	22-6K
DM8	AN10	DDR_PDM8	22-6K
DQS0	AM21	DDR_PDQS0	22-4K
DQS1	AM19	DDR_PDQS1	22-4K
DQS2	AL16	DDR_PDQS2	22-4K
DQS3	AM23	DDR_PDQS3	22-4K
DQS4	AE3	DDR_PDQS4	22-4K
DQS5	AB4	DDR_PDQS5	22-5K
DQS6	W4	DDR_PDQS6	22-5K
DQS7	Y4	DDR_PDQS7	22-5K
DQS8	AP10	DDR_PDQS8	22-5K
MEMODT0	AN3	DDR_PODT0	22-7L
MEMODT1	AG1	DDR_PODT1	22-6L
BANKSELA0	AN2	DDR_PCS0#	22-3K,22-7L
BANKSELA1	AM1	DDR_PCS1#	22-3K,22-7L
MEMCLKEN	AN9	DDR_PCKE	22-6K,22-7L
MEMCLKOUT	AL1	DDR_CLKOUT	
MEMCLKOUT#	AM1	DDR_CLKOUT#	

ECC0	AM11	PPC_ECC0	22-9F
ECC1	AL11	PPC_ECC1	22-9F
ECC2	AN9	PPC_ECC2	22-9F
ECC3	AL9	PPC_ECC3	22-10F
ECC4	AM11	PPC_ECC4	22-10F
ECC5	AN11	PPC_ECC5	22-10F
ECC6	AM10	PPC_ECC6	22-10F
ECC7	AP9	PPC_ECC7	22-10F

SVREF1A	AL19
SVREF2A	AF4
SVREF1B	AL18
SVREF2B	AL20

R813 500ps Loop

DDR_VREF_0V9

5V

1V8

C150 0.10F

C148 0.10F

C151 0.10F 0402

C152 0.10F 0402

C148 .010F

Place parts as close to CPU as possible

U32

VIN	10	VTT	3
VLDOIN	2	VTTSNS	5
VDDQSNS	1	VTTREF	6
S3	7		
S5	9		
GND	8		
PGND	4		

R230 10K

R229 10K

C459 4U7F 10V

C456 10UF 16V

C453 100NF 10V

C457 10UF 16V

C458 10UF 16V

DDR_VTT

DDR_VREF_0V9

GND

J8

22-6D	168	PPC_ECC7	DDR2_DIMM_CB7
22-6D	167	PPC_ECC6	DDR2_DIMM_CB6
22-7D	162	PPC_ECC5	DDR2_DIMM_CB5
22-7D	161	PPC_ECC4	DDR2_DIMM_CB4
22-7D	49	PPC_ECC3	DDR2_DIMM_CB3
22-7D	48	PPC_ECC2	DDR2_DIMM_CB2
22-7D	43	PPC_ECC1	DDR2_DIMM_CB1
22-7D	42	PPC_ECC0	DDR2_DIMM_CB0
DDR_PDQ63	236		DDR2_DIMM_DQ[63]
DDR_PDQ62	235		DDR2_DIMM_DQ[62]
DDR_PDQ61	230		DDR2_DIMM_DQ[61]
DDR_PDQ60	229		DDR2_DIMM_DQ[60]
DDR_PDQ59	117		DDR2_DIMM_DQ[59]
DDR_PDQ58	116		DDR2_DIMM_DQ[58]
DDR_PDQ57	111		DDR2_DIMM_DQ[57]
DDR_PDQ56	110		DDR2_DIMM_DQ[56]
DDR_PDQ55	227		DDR2_DIMM_DQ[55]
DDR_PDQ54	226		DDR2_DIMM_DQ[54]
DDR_PDQ53	218		DDR2_DIMM_DQ[53]
DDR_PDQ52	217		DDR2_DIMM_DQ[52]
DDR_PDQ51	108		DDR2_DIMM_DQ[51]
DDR_PDQ50	107		DDR2_DIMM_DQ[50]
DDR_PDQ49	99		DDR2_DIMM_DQ[49]
DDR_PDQ48	98		DDR2_DIMM_DQ[48]
DDR_PDQ47	215		DDR2_DIMM_DQ[47]
DDR_PDQ46	214		DDR2_DIMM_DQ[46]
DDR_PDQ45	209		DDR2_DIMM_DQ[45]
DDR_PDQ44	208		DDR2_DIMM_DQ[44]
DDR_PDQ43	96		DDR2_DIMM_DQ[43]
DDR_PDQ42	95		DDR2_DIMM_DQ[42]
DDR_PDQ41	90		DDR2_DIMM_DQ[41]
DDR_PDQ40	89		DDR2_DIMM_DQ[40]
DDR_PDQ39	206		DDR2_DIMM_DQ[39]
DDR_PDQ38	205		DDR2_DIMM_DQ[38]
DDR_PDQ37	200		DDR2_DIMM_DQ[37]
DDR_PDQ36	199		DDR2_DIMM_DQ[36]
DDR_PDQ35	87		DDR2_DIMM_DQ[35]
DDR_PDQ34	86		DDR2_DIMM_DQ[34]
DDR_PDQ33	81		DDR2_DIMM_DQ[33]
DDR_PDQ32	80		DDR2_DIMM_DQ[32]
DDR_PDQ31	159		DDR2_DIMM_DQ[31]
DDR_PDQ30	158		DDR2_DIMM_DQ[30]
DDR_PDQ29	153		DDR2_DIMM_DQ[29]
DDR_PDQ28	152		DDR2_DIMM_DQ[28]
DDR_PDQ27	40		DDR2_DIMM_DQ[27]
DDR_PDQ26	39		DDR2_DIMM_DQ[26]
DDR_PDQ25	34		DDR2_DIMM_DQ[25]
DDR_PDQ24	33		DDR2_DIMM_DQ[24]
DDR_PDQ23	150		DDR2_DIMM_DQ[23]
DDR_PDQ22	149		DDR2_DIMM_DQ[22]
DDR_PDQ21	144		DDR2_DIMM_DQ[21]
DDR_PDQ20	143		DDR2_DIMM_DQ[20]
DDR_PDQ19	31		DDR2_DIMM_DQ[19]
DDR_PDQ18	30		DDR2_DIMM_DQ[18]
DDR_PDQ17	25		DDR2_DIMM_DQ[17]
DDR_PDQ16	24		DDR2_DIMM_DQ[16]
DDR_PDQ15	141		DDR2_DIMM_DQ[15]
DDR_PDQ14	140		DDR2_DIMM_DQ[14]
DDR_PDQ13	132		DDR2_DIMM_DQ[13]
DDR_PDQ12	131		DDR2_DIMM_DQ[12]
DDR_PDQ11	22		DDR2_DIMM_DQ[11]
DDR_PDQ10	21		DDR2_DIMM_DQ[10]
DDR_PDQ9	13		DDR2_DIMM_DQ[9]
DDR_PDQ8	12		DDR2_DIMM_DQ[8]
DDR_PDQ7	129		DDR2_DIMM_DQ[7]
DDR_PDQ6	128		DDR2_DIMM_DQ[6]
DDR_PDQ5	123		DDR2_DIMM_DQ[5]
DDR_PDQ4	122		DDR2_DIMM_DQ[4]
DDR_PDQ3	10		DDR2_DIMM_DQ[3]
DDR_PDQ2	9		DDR2_DIMM_DQ[2]
DDR_PDQ1	4		DDR2_DIMM_DQ[1]
DDR_PDQ0	3		DDR2_DIMM_DQ[0]
	101		DDR2_DIMM_SA2
	240		DDR2_DIMM_SA1
	239		DDR2_DIMM_SA0
	120		DDR2_DIMM_SCL
	119		DDR2_DIMM_SDA

879160001

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA1	22-8L,22-9D
DDR2_DIMM_BA[1]	190	DDR_PBA2	22-8L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-8L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	NC	
DDR2_DIMM_CK_N[2]	221	NC	
DDR2_DIMM_CK_P[1]	137	NC	
DDR2_DIMM_CK_N[1]	138	NC	
DDR2_DIMM_CK_P[0]	185	DDR_CLKOUT	
DDR2_DIMM_CK_N[0]	186	DDR_CLKOUT#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-7L,22-8D
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-9D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D
ERR_OUT	55	PPC_DDR2_ERROR	
PAR_IN	68	PAR_IN	

R226 4K7

PPC_DDR2_RESET_N

1-2B,1-2M,24-5J

C455 5PF 50V

TP4

TP5

R228 4K7

R227 4K7

PPC_DDR2_DIMM_SCL

PPC_DDR2_DIMM_SDA

1V8

GND

VTT VTT MODULE WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

DDR_VTT

DDR_PA15	RP24	CP26	
DDR_PA14			
DDR_PA13			
DDR_PA12			
DDR_PA11	RP23	CP28	GND
DDR_PA10			
DDR_PA9			
DDR_PA8			
DDR_PA7	RP22	CP29	GND
DDR_PA6			
DDR_PA5			
DDR_PA4			
DDR_PA3	RP21	CP30	GND
DDR_PA2			
DDR_PA1			
DDR_PA0			
22-8K,22-9D	RP25	CP32	
22-8K,22-9D			
22-8K,22-9D			
22-8K,22-9D			
22-7K,22-9D	RP26	CP31	GND
22-6K,22-8D			
22-3K,22-9D			
22-3K,22-8D			
22-3K,22-8D	RP19	CP33	GND
22-8D			
22-8D			
NC			

J8

237	VSS_64		
234	VSS_63		
231	VSS_62		
228	VSS_61		
225	VSS_60		
222	VSS_59		
219	VSS_58		
216	VSS_57		
213	VSS_56		
210	VSS_55		
207	VSS_54		
204	VSS_53		
201	VSS_52		
198	VSS_51		
169	VSS_50		
166	VSS_49		
163	VSS_48		
160	VSS_47		
157	VSS_46		
154	VSS_45		
151	VSS_44		
148	VSS_43		
145	VSS_42		
142	VSS_41		
139	VSS_40		
136	VSS_39		
133	VSS_38		
130	VSS_37		
127	VSS_36		
124	VSS_35		
121	VSS_34		
118	VSS_33		
115	VSS_32		
112	VSS_31		
109	VSS_30		
106	VSS_29		
103	VSS_28		
100	VSS_27		
97	VSS_26		
94	VSS_25		
91	VSS_24		
88	VSS_23		
85	VSS_22		
82	VSS_21		
79	VSS_20		
66	VSS_19		
65	VSS_18		
50	VSS_17		
47	VSS_16		
44	VSS_15		
41	VSS_14		
38	VSS_13		
35	VSS_12		
32	VSS_11		
29	VSS_10		
26	VSS_9		
23	VSS_8		
20	VSS_7		
17	VSS_6		
14	VSS_5		
11	VSS_4		
8	VSS_3		
5	VSS_2		
2	VSS_1		

879160001

VDD_11	197	VDDQ_11	194
VDD_10	189	VDDQ_10	191
VDD_9	187	VDDQ_9	181
VDD_8	184	VDDQ_8	175
VDD_7	178	VDDQ_7	170
VDD_6	172	VDDQ_6	78
VDD_5	69	VDDQ_5	75
VDD_4	67	VDDQ_4	72
VDD_3	64	VDDQ_3	62
VDD_2	59	VDDQ_2	56
VDD_1	53	VDDQ_1	51

DDR_VREF_0V9

VREF 1

1V8

VDDSPD 238

GND

DDR_VREF_0V9

1V8

C432 100NF 10V

C433 10NF 25V

C454 100NF 10V

C434 10NF 25V

C430 100NF 10V

C443 10NF 25V

C431 100NF 10V

C444 10NF 25V

C436 100NF 10V

C445 10NF 25V

C435 100NF 10V

C446 10NF 25V

C438 100NF 10V

C451 10NF 25V

C437 100NF 10V

C452 10NF 25V

C439 100NF 10V

C449 10NF 25V

C440 100NF 10V

C450 10NF 25V

C441 100NF 10V

C448 10NF 25V

C442 100NF 10V

C447 10NF 25V

PLACE NEAREST DDR2 MODULE PINS

ROACH/iBOB2

ROACH_PPC_DDR2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

10-15-2007_17:29

PATH PATH

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 22 OF 25


PWR_GOOD
RESET_PB_POR#
PWR_GOOD monitors the +1.0v, 1V5, 1V8, 2V5, and 3V3 supplies
RESET_POR#
IRQ0-9 have programmable polarity per section 10.5.7 (UIC0_PR) 440ep user manual
Critical Placement and Route Clock Rules:
Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_SYS_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz
SEL_SYSCLK
CLK_UART_11.0592MHZ
CLK_CPLD_33MHZ
CLK_TMRCLK
SYSERR
PPC_THERMONA
PPC_THERMONB
PPC440EPX-NTA533T
SYSTEM
INTERRUPTS
GETH0_INT#
MONITOR_INT
V5_INT#
STTM_ALERT
GPIO44
SX95T_TDI
SX95T_TCK
SX95T_TMS
SX95T_TDO
NO POP
RO1 - RO5
TEST POINT
Critical Placement and Route Clock Rules:
Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = CLK_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible
CLK_SEL_M66EN
CLK_PCI1_66/33MHZ
CLK_PCI2_66/33MHZ
CLK_GETH0_25MHZ
CLK_USB2.0_48MHZ
CLK_CPLD_50MHZ
TRACE & JTAG CONNECTORS
R26 is for current limiting and should be <100 Ohms.
Critical placement and routing of the Trace connector and nets. Up to CPU frequency/4
RiscWatch
JTAG
CPU_TRST#
TRACE PORT
DEBUG_TRST#
3V3
GND

ROACH/iBOB2	**ROACH_PPC_TST_CLK_IO**
COLLABORATORS:	DOC NO: NRF-ADM-XXX-SD-0001
CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN	REVISION: A
http://casper.berkeley.edu/	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-15-2007_17:29	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	SHEET 23 OF 25

Memory Bus

PADR[27:31]
1-2G,1-4L,25-10B

PADATA[0:7]
1-2M,1-4L

U54

roach_cpld_XC2C256_7VQ100C_pcb

PADR27	4	PAD4	
PADR28	7	PAD8	
PADR29	9	PAD10	
PADR30	10	PAD12	
PADR31	11	PAD15	
PDATA0	12	PAD16	
PDATA1	13	PAD17	
PDATA2	14	PAD18	
PDATA3	15	PAD19	
PDATA4	16	PAD20	
PDATA5	17	PAD21	
PDATA6	18	PAD23	
PDATA7	19	PAD28	
NC	20	PAD29	
NC	21	PAD30	
NC	22	PAD31	
NC	23	PAD32	
NC	24	PAD33	
NC	25	PAD34	
NC	26	PAD35	
	28	PAD44	
SELECTMAP_CS 1-2G,1-5L,25-7B	30	PAD48	
PCS_2 1-1G,1-4L,25-7B	31	PAD49	
PDS0 1-1G,1-5L,25-5G,25-7B,25-7M,25-10B	32	PAD50	
PR_WE 1-1G,1-4L,26-5G,26-6M,d5-7B,25-9B	33	PAD52	
PWRE_B0 1-2G,1-4L,25-6M,25-7B,25-9B	34	PAD54	
RESET_PDN0 1-2G,1-3L,1-5G,23-9J,25-5G	35	PAD55	
RESET_PR_PDN0 1-2M,1-3H,23-8E	38	PAD59	
PPC_RESET 1-2G,1-9E,2-1B	40	PAD64	
DEBUG_TRST# 1-1G,1-3L,23-1F	41	PAD65	
CPU_TRST# 1-2M,1-3M,23-2F	42	PAD66	
CLK_CPLD_33MHZ 1-1G,1-2L,23-6G	43	PAD67	
CLK_CPLD_33MHZ 1-1G,1-3L,23-4G	44	PAD68	
CLK_PXICLK 1-1G,1-4L,25-6F	45	PAD69	
CLK_TMSCLK 1-1M,1-3M,23-E6	46	PAD70	
CLK_SEL_PXIEN 1-1M,1-3M,23-5D	48	PAD73	
SEL_SYSCLK 1-1M,1-3M,23-7G	49	PAD74	
SYSERR 1-1G,1-3L,23-E6	50	PAD75	
FRY_BSY 1-1G,1-4L,25-7J	51	PAD76	
PAPDC 1-1M,1-4G,25-BJ	52	PAD77	
EE1_WP 1-2M,1-5L,25-1A	53	PAD81	
EE2_BOOT_WP 1-2M,1-4G,25-5A	54	PAD82	
ETTM_ASC 1-2M,1-5G,25-1B	56	PAD86	
	57	PAD87	
	58	PAD88	
	59	PAD89	
	60	PAD90	
	61	PAD95	
	64	PAD100	
GETH0_RST# 1-2M,1-4B,26-4E	66	PAD102	
	68	PAD105	
	69	PAD107	
	70	PAD108	
	71	PAD109	
RESET_CPLD#C 1-1M,1-4G,25-3J	74	PAD112	
PER_CCLK_EN#	75	PAD113	
	76	PAD114	
	77	PAD115	
	78	PAD117	
	80	PAD118	
	79	PAD119	
	82	PAD121	
	81	PAD120	
	83	PAD125	
	85	PAD131	
	86	PAD132	
	87	PAD133	
	88	PAD134	
	91	PAD137	
	92	PAD138	
	94	PAD142	
	95	PAD143	
	96	PAD144	
	97	PAD145	
	98	PAD146	
	100	PAD152	
	101	PAD154	
	102	PAD156	
	103	PAD158	
	104	PAD160	
	105	PAD161	
	106	PAD162	
	107	PAD163	
	110	PAD166	
	111	PAD167	
	112	PAD168	
	113	PAD169	
	114	PAD171	
	115	PAD173	
	116	PAD175	
	117	PAD176	
	118	PAD178	
	119	PAD186	
	120	PAD187	
	121	PAD190	
	124	PAD191	
	125	PAD192	
	126	PAD194	
	128	PAD195	
	129	PAD196	
	130	PAD197	
	131	PAD199	
	132	PAD204	
	133	PAD206	
	134	PAD207	
	135	PAD208	
	136	PAD211	
	137	PAD212	
	138	PAD213	
	139	PAD214	
	140	PAD217	
	142		

XC2C256_7VQ100C

RESETS

CPU_TRST# = '1' when JTAG_TRST# = '1' and RESET_PDN# = '1' else '0'; see errata sheet

CLOCKS

STATUS / MISC

FLASH

I2C

USB

Assertion of USB2_RESET may be asynchronous to CLK_USB2_CPLD
De-assertion of USB2_RESET must be synchronous to CLK_USB2_CPLD

NAND FLASH NOT USED

ETHERNET

USB_EBC_MUX

PER_CCLK_EN#

R135 10K

ENABLE PER_CLK CONNECTION TO CONFIGURATION I/F MUST CO-ORDINATE WITH SX95T_CCLK_0 AND MODE TO AVOID CLASH

SN74AHC1G125DCKT

PER_CCLK_EN# 1 OE# VCC 5
CLK_PERCLK 2 A Y 4
3 GND
U2

SX95T_CCLK_0

C13 100NF 10V

U54

roach_cpld_XC2C256_7VQ100C_powerpins

1	8	27	37	55	73	84	93	109	127	141
VCC	VAUX	VCCIO_3	VCC_1	VCCIO_4	VCCIO_5	VCC_2	VCCIO_6	VCCIO	VCCIO_1	VCCIO_2

29	36	47	62	72	89	99	99	108	123	144
GND_3	GND_4	GND_5	GND_6	GND_7	GND_8	GND_9	GND_10	GND	GND_1	GND_2

XC2C256_7VQ100C

PLACE NEAR CPLD POWER PINS

C473 C474 C475 C476 C477 C478 C479 C480 C481 C482 C483 100NF 10V

USER_DIP0
USER_DIP1
USER_DIP2
USER_DIP3

R193 10K
R194 10K
R195 10K
R196 10K
SW2 4POLE User DIP-Swith

USER_LED0
USER_LED1
SYSERR#
RESET_BUFPOR#

R200 R201 R202 R203 10K
CR2 GRN CR3 GRN CR4 GRN CR5 GRN
RED

SysErr will be used to drive Status LED (active H)

R197 R199 330
CR1 GRN CR2 GRN
5V_VIN
U35 74LVC1G66
VCC GND
3V3
C615 0.1UF 0402
PWR_GOOD 1-2G,1-3H,23-10G

CMD/DI
CLK/SCLK

J17

10	CMD/DI	DAT0/DO	2 DAT0/DO
6	CLK/SCLK	DAT1	1 DAT1
		DAT2	13 DAT2
7	VDD	DAT3	12 DAT3
8	VSS1	DAT4	11 DAT4
4	VSS2	DAT5	9 DAT5
		DAT6	5 DAT6
14	SD_CD_COM	DAT7	3 DAT7
15	SD_WP_COM	MNT1	16 NC
		MNT2	17 NC

GMC05006ASEU

SD/MMC/MMCPLUS CONNECTOR

QDR2_BY0_1_SYS_RST_N 1-1M,1-8L,34-BJ
QDR2_BY2_3_SYS_RST_N 1-2M,1-7L,15-BJ
PPC_DDR2_RESET_N 1-2G,1-2M,22-3B
EXT_RESET# 1-2G,1-4L,25-6F

SX95T_M0_0 1-1G,1-3F,1-7G,16-3B,21-4D
SX95T_M1_0 1-1G,1-3F,1-7G,16-3B,21-4D
SX95T_M2_0 1-1G,1-3F,1-7G,16-3B,21-4D

SX95T_CCLK_0 1-2M,1-7G
SX95T_CS_B_0 1-1M,1-5C,16-4B
SX95T_D_IN_0 1-1M,1-7C,16-4A
SX95T_D_OUT_BUSY_0 1-1G,1-3F,1-7G,16-4B,21-5D
SX95T_DONE_0 1-1M,1-3F,1-7G,21-5D
SX95T_INIT_B_0 1-1M,1-3F,1-7G,21-4D
SX95T_PROGRAM_B_0 1-1M,1-3F,1-7C,16-3B,21-4D
SX95T_RDWR_B_0 1-1M,1-7C,16-3B

Boot Configuration

R204 R205 R206 10K
SW3 4POLE Configuration DIP-Swith
1-1G,1-5G,25-3B

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

BOOT_CFG0 1-1M,1-4G,25-1J
BOOT_CFG1 1-1M,1-4G,25-1J
BOOT_CFG2 1-1M,1-4G,25-1J

3V3 RD10 RD11 RD14 10K

U54

roach_cpld_XC2C256_7VQ100C_configpins

NC	2	PAD1	
NC	3	PAD3	
NC	5	PAD5	
NC	6	PAD7	
NC	39	PAD62	
	63	TDI	
	65	TMS	
	67	TCK	
	122	TDO	
NC	143	PAD218	

XC2C256_7VQ100C

Xilinx
Programing Cable

JTAG

J22

3V3 R193 1K R192 1K

13	VREF	TDI	5
9	NC_9	TMS	11
11	NC_11	TCK	9
7	TDO		

12	10	8	6	4	2		
GND_7	GND_6	GND_4	GND_3	GND_2	GND_1	GND_0	

3V3 C484 20Z 0402

PLACE NEAR CPLD JTAG CONNECTOR

ROACH/iBOB2	ROACH_PPC_CPLD
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO NRF-ADM-XXX-SD-0001 REVISION A
	DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
10-15-2007_17:29 PATH PATH	DRAWN: F KAPP APPR:
	CHECKED: E BAUERMEISTER SHEET 24 OF 25


PDATA[0:31]
PADD[2:31]
PADD30 IS THE LSB FOR 16 BIT
WIDE BUS TRANSFERS
NOTE:
DMA SIGNALS
IN GREEN TEXT
PADD2 IS THE MSB
External Slave Peripheral
External Master Peripheral Interface
FLASH
EPB RESET OUTPUT
EXT_RESET#
CLK_PERCLK
BANKS=1, 2, 4
CHIP SELECT 1
U15
3V3
GND
NO POP
UART
IIC0
IIC1_SPI
NAND Flash Interface
NOT USED
UART Port 0
UART Port 1
J14
HLE-105-02-G-DV
I2C0_SCLK
I2C0_S3_DATA
EE2_BOOT_WP
EE1_WP
STTM_ALERT
STTM_AS
SCPCLK
SCPDI
SCPDO
BOOT_CFG2
BOOT_CFG1
BOOT_CFG0
RESET_CPLD#
RESET_POR#
PWBE_0#
POE#
PR_W#
PCS_2
SELECTMAP_CS
ROACH/iBOB2
ROACH_PPC_NVM_SERIAL
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
DOC NO
NRF-ADM-XXX-SD-0001
REVISION
A
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
CHECKED: E BAUERMEISTER
10-15-2007_17:29
PATH PATH
SHEET 25 OF 25