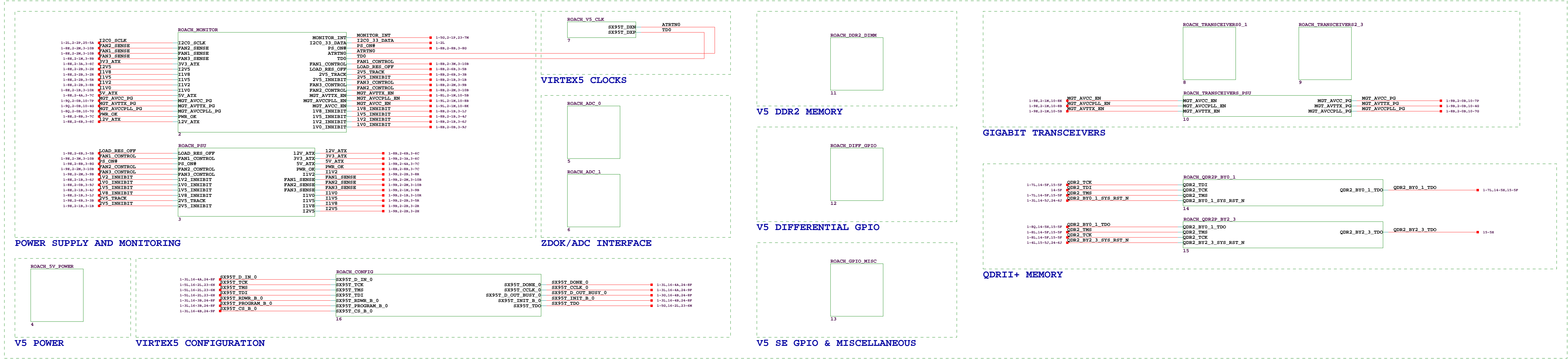
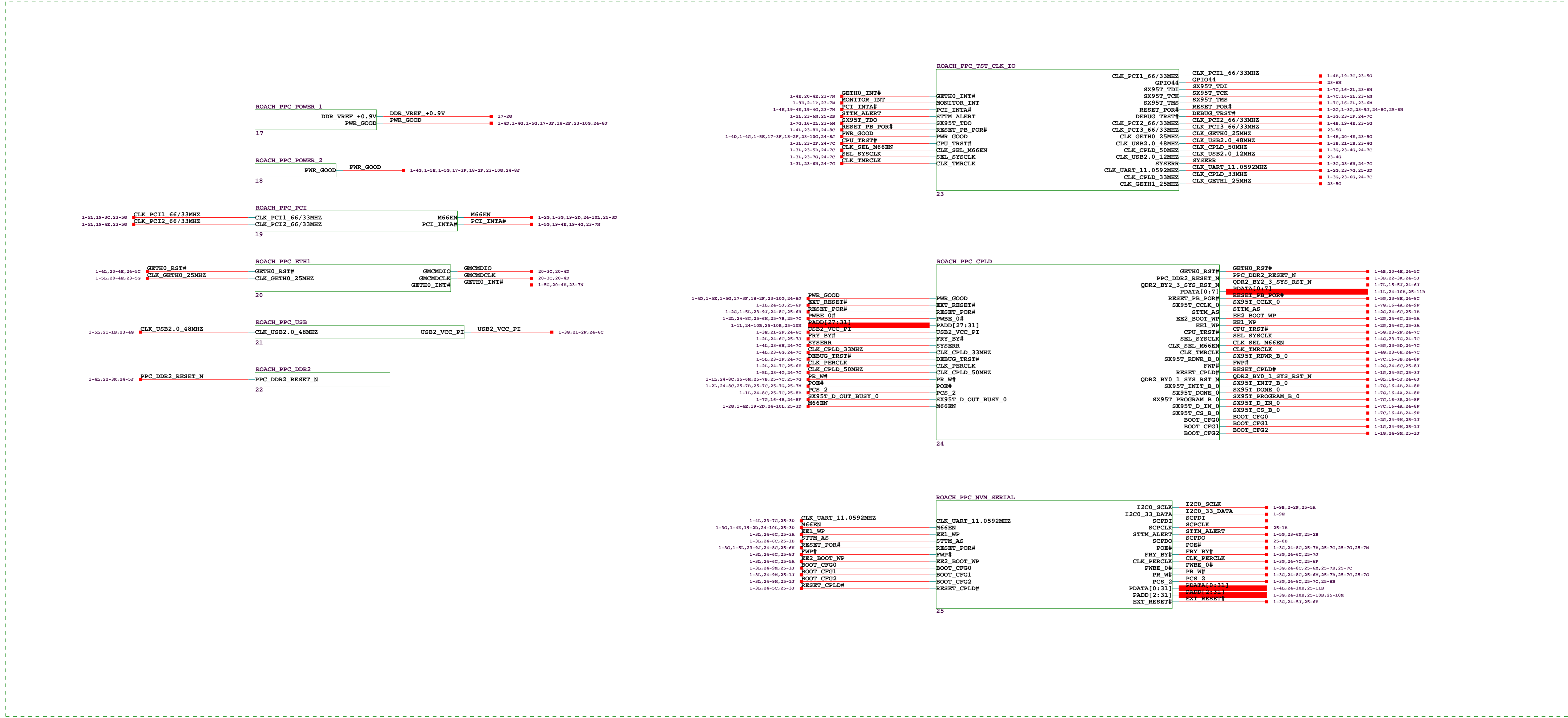


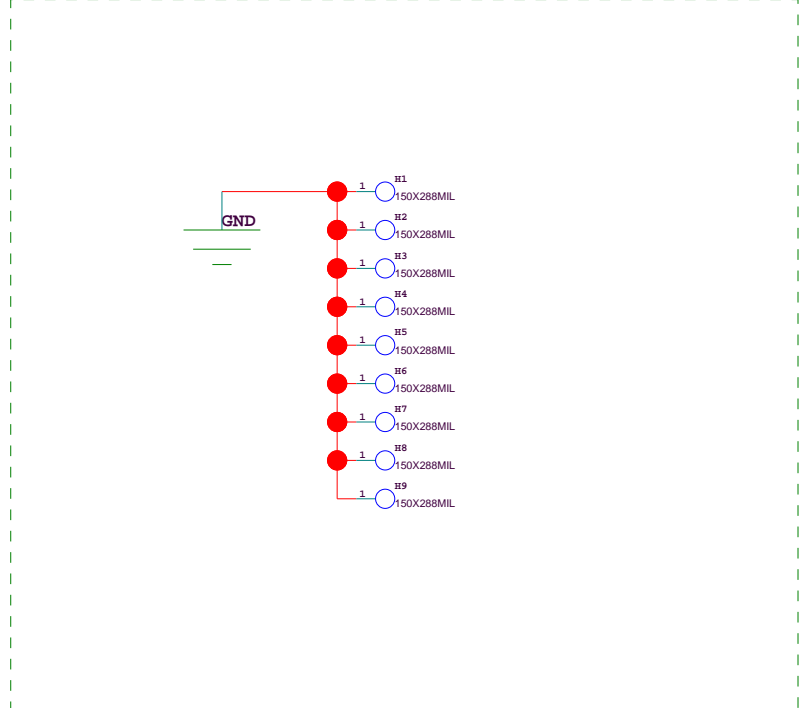
VIRTEX5

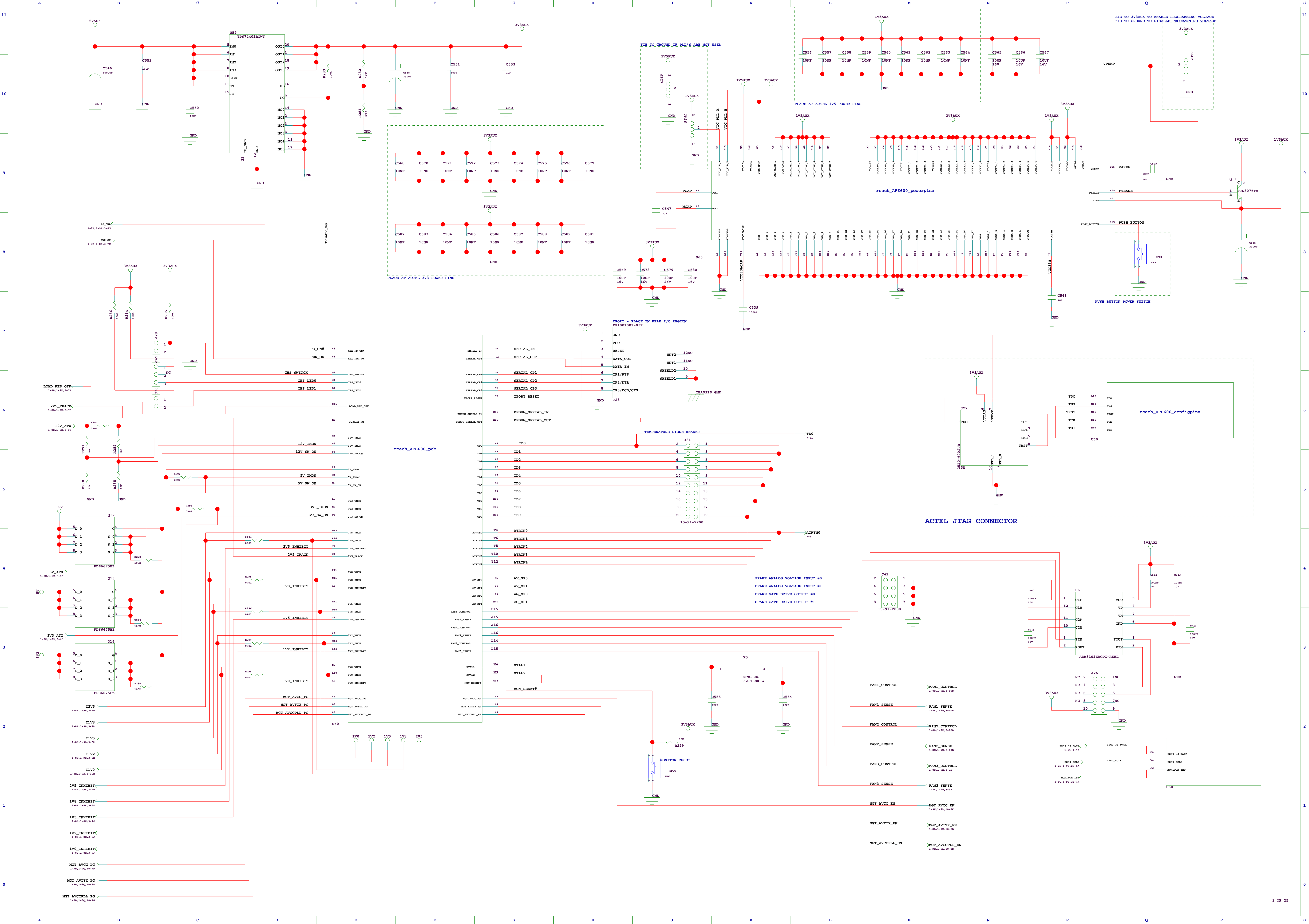


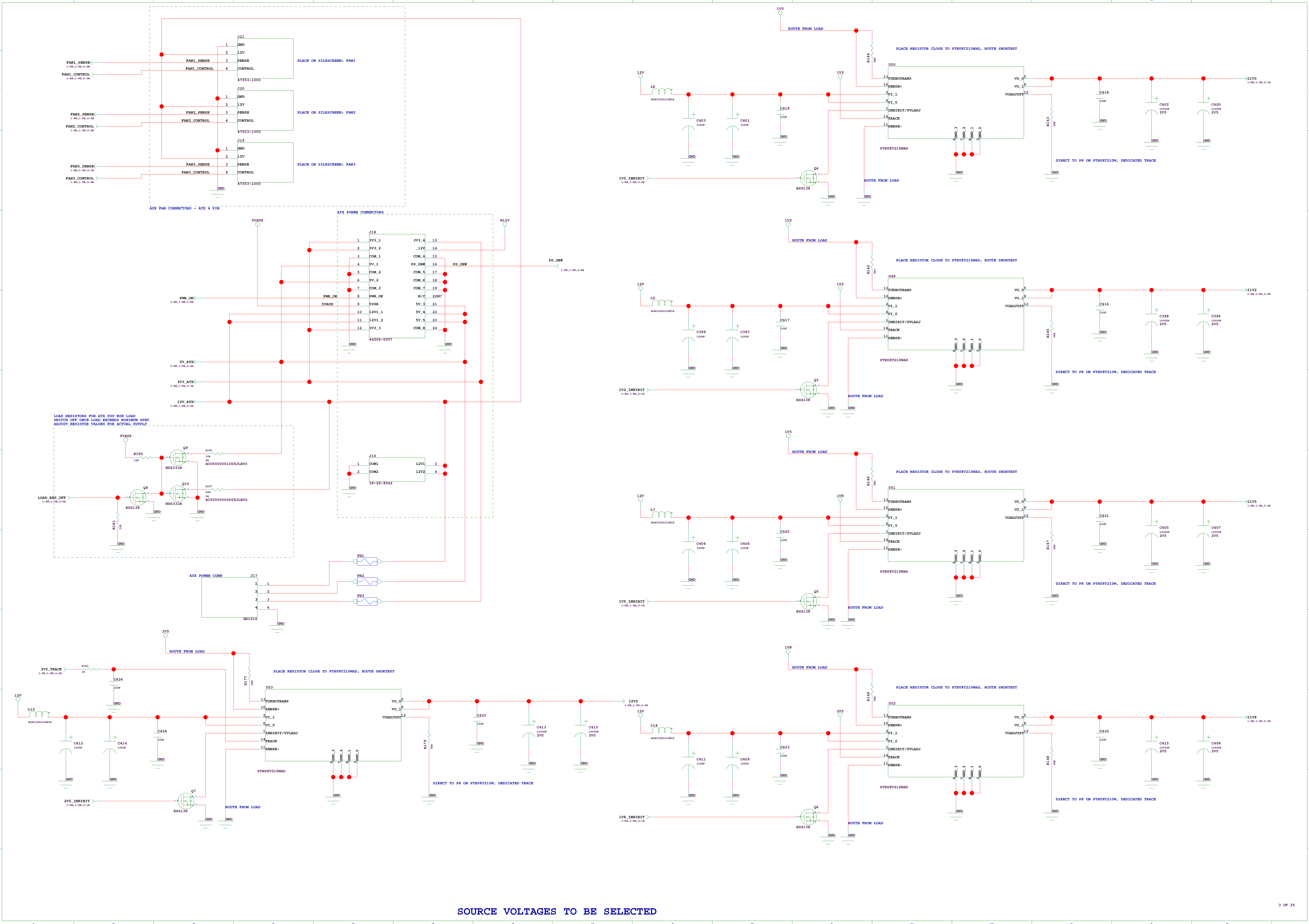
PPC



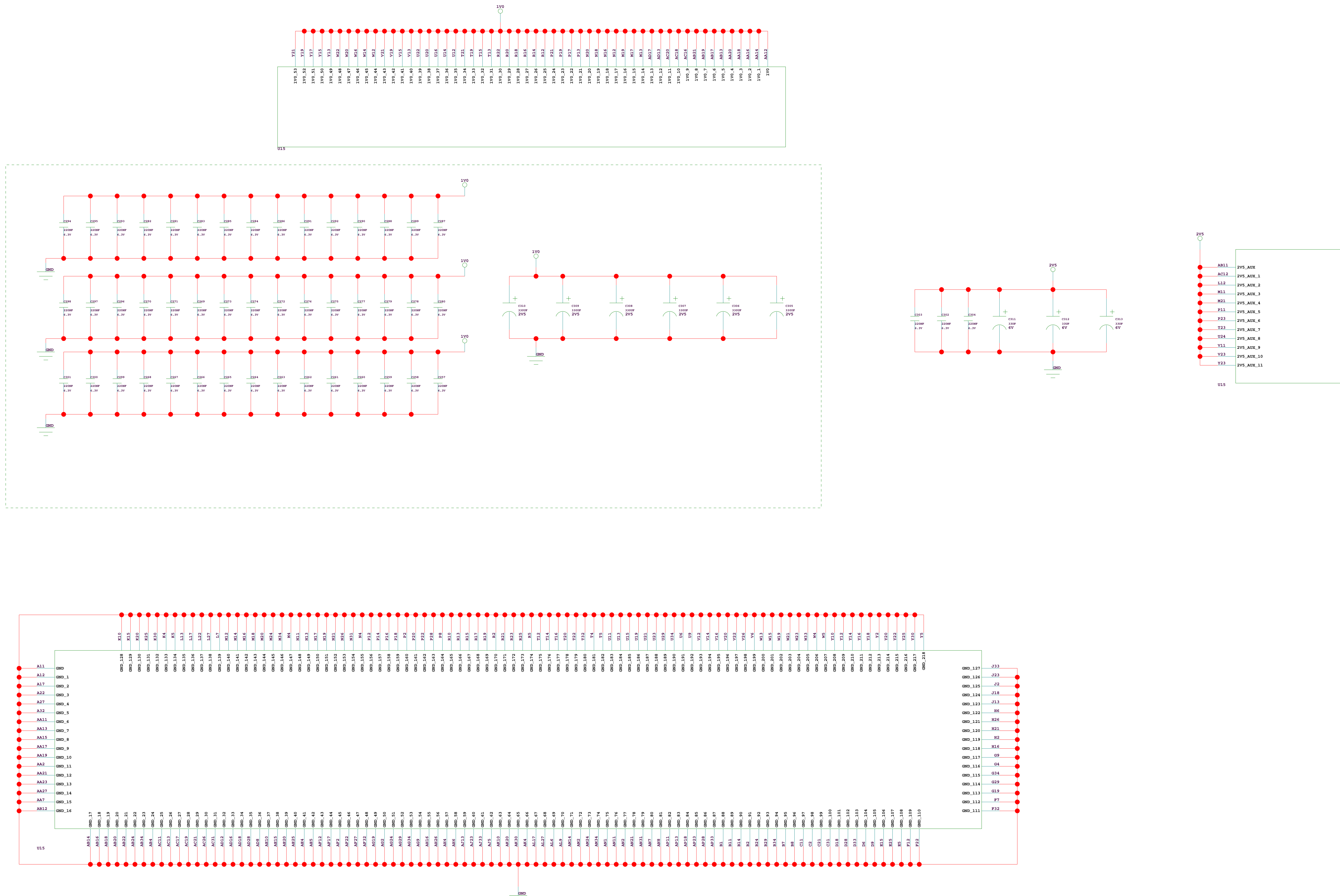
MECHANICAL





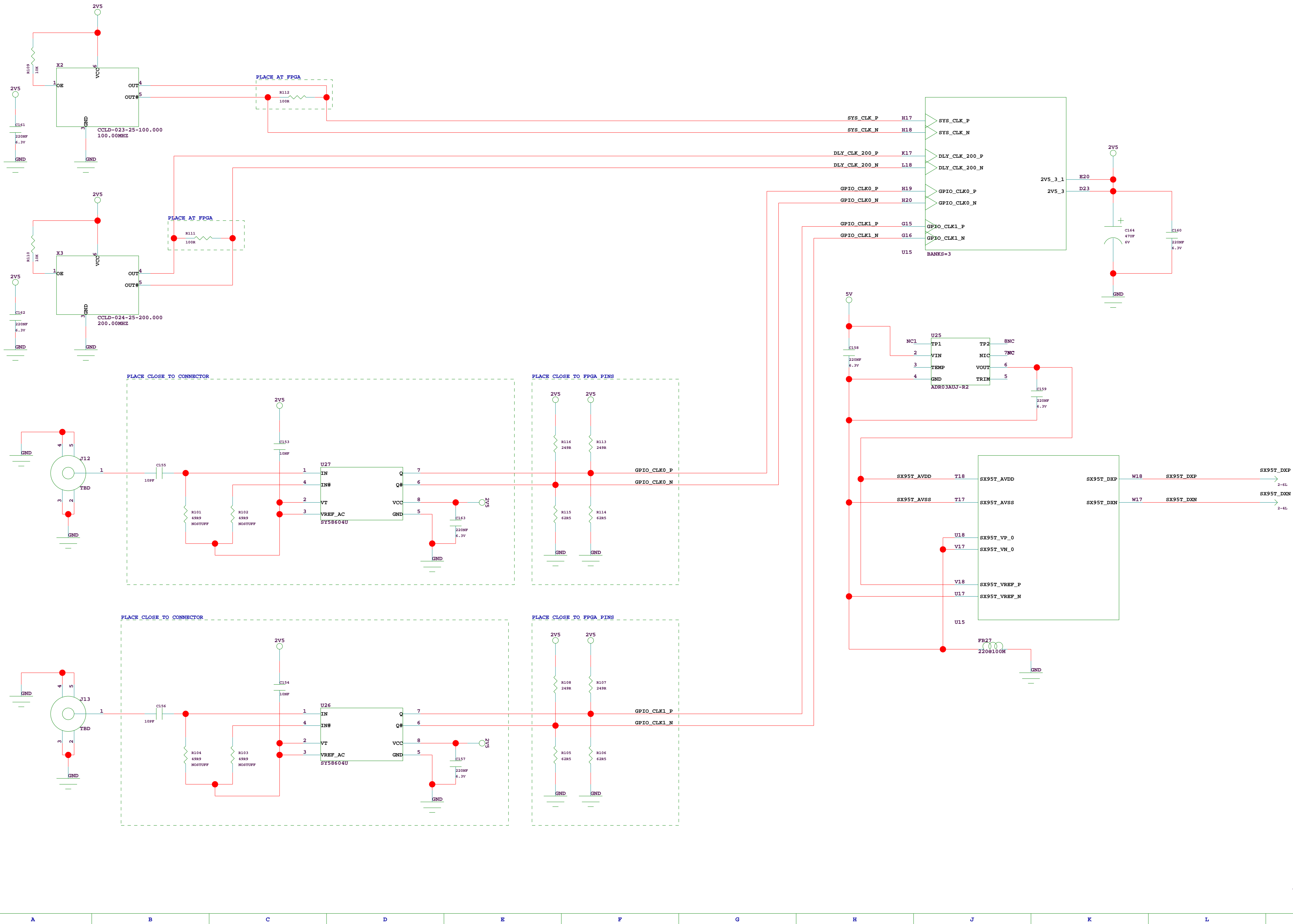


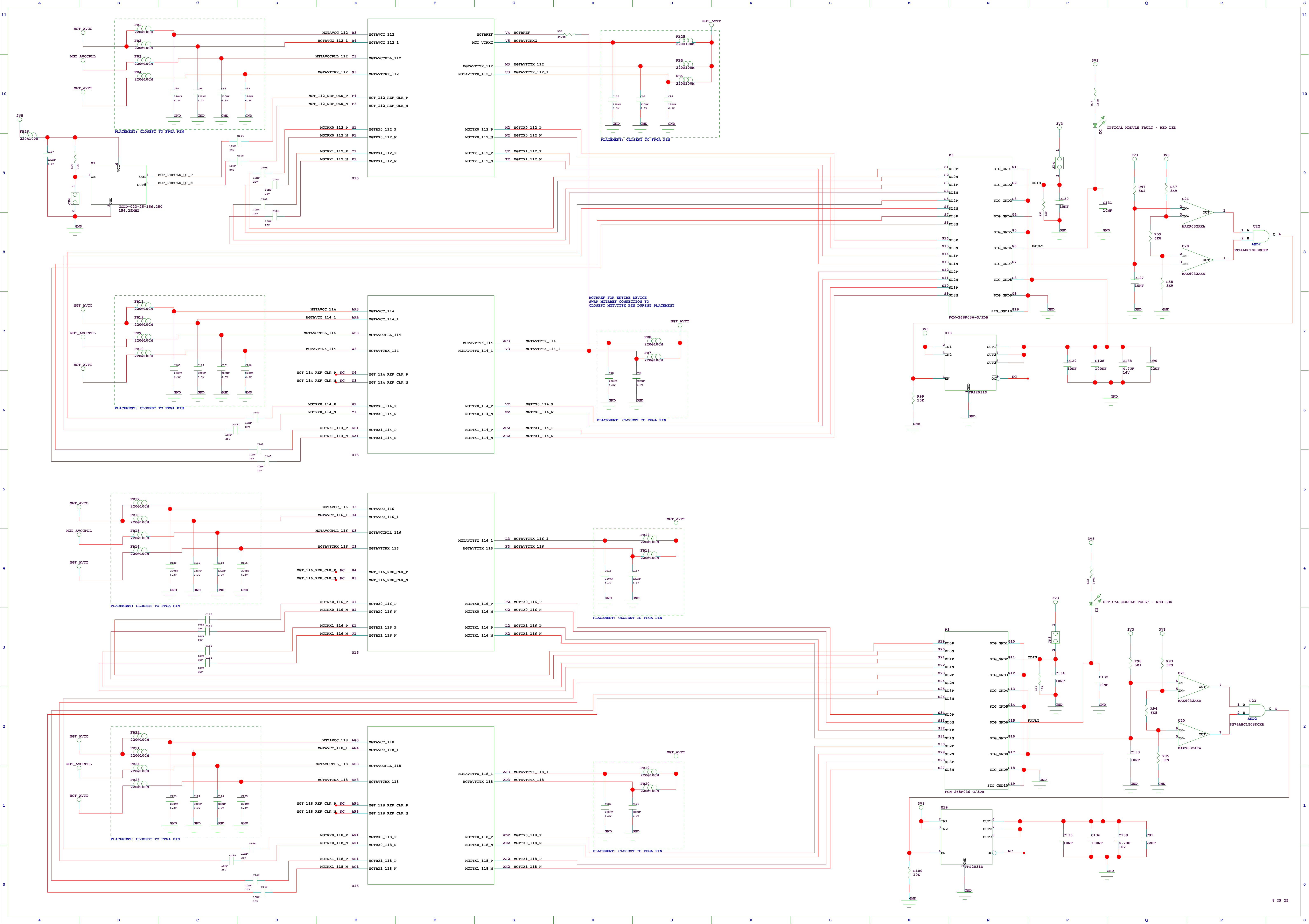
SOURCE VOLTAGES TO BE SELECTED

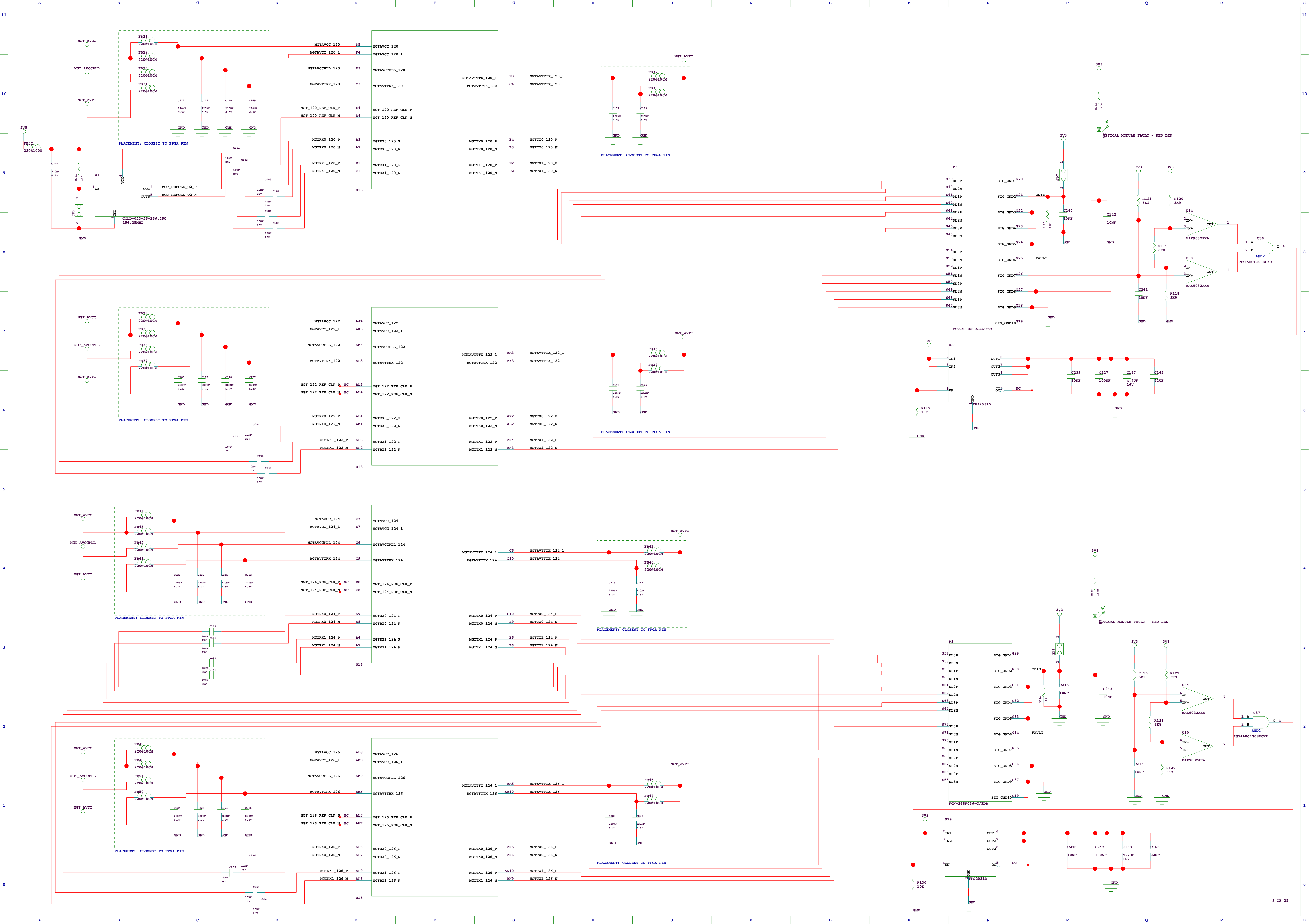


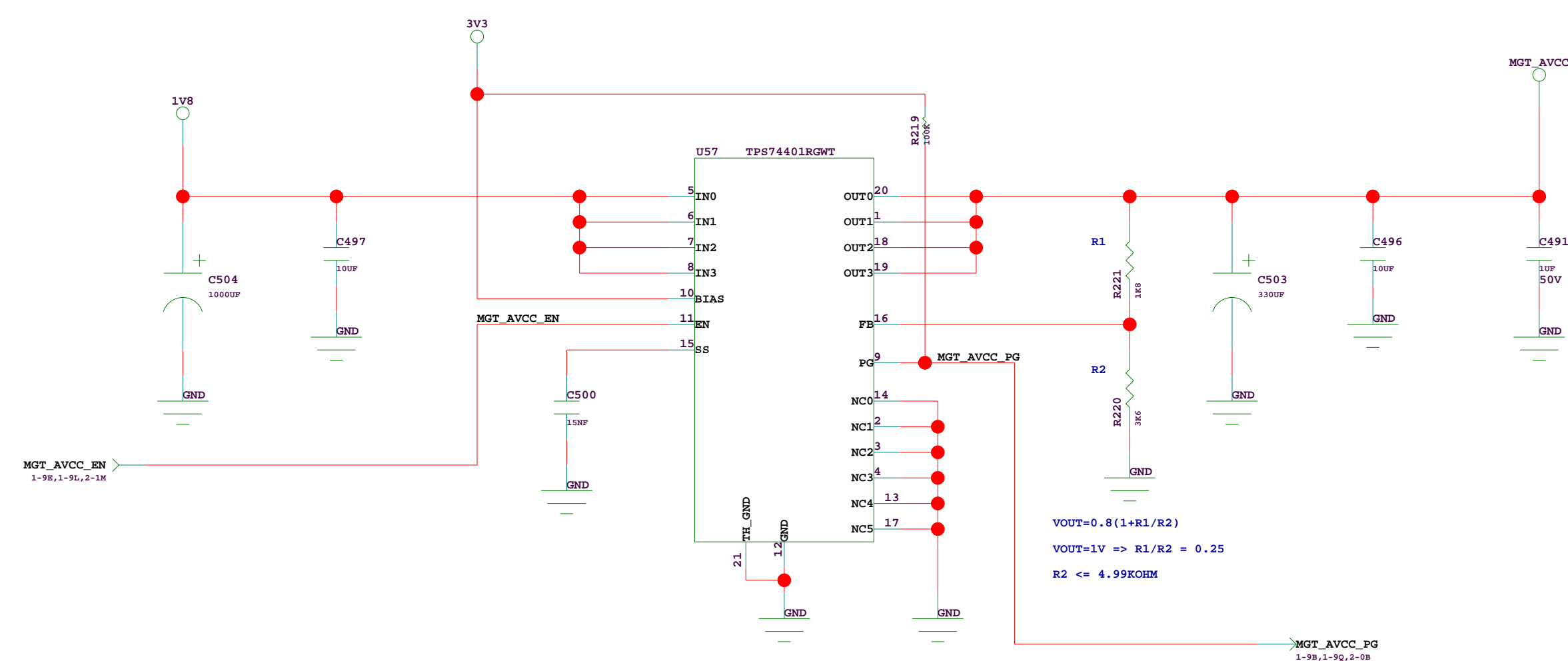
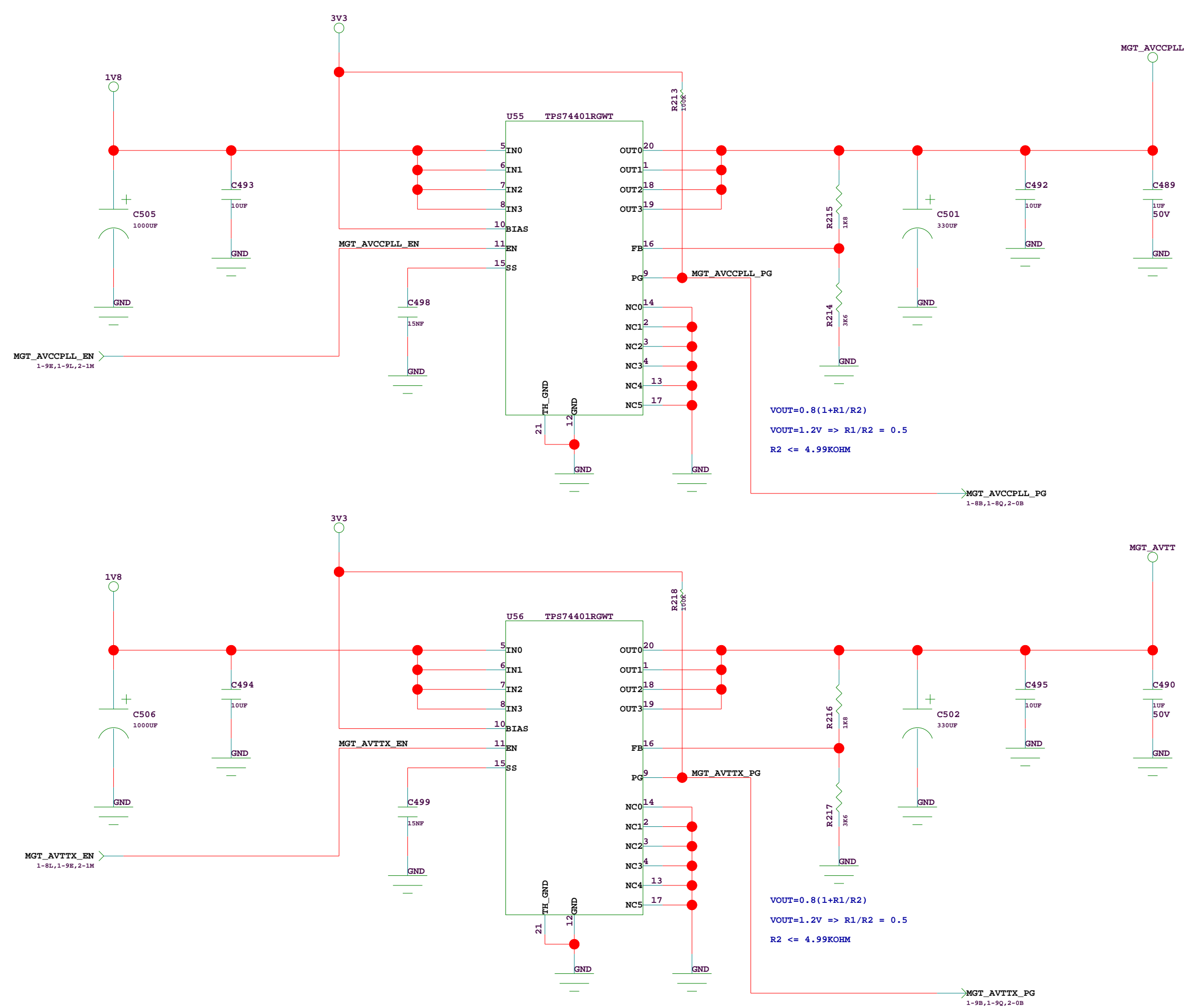




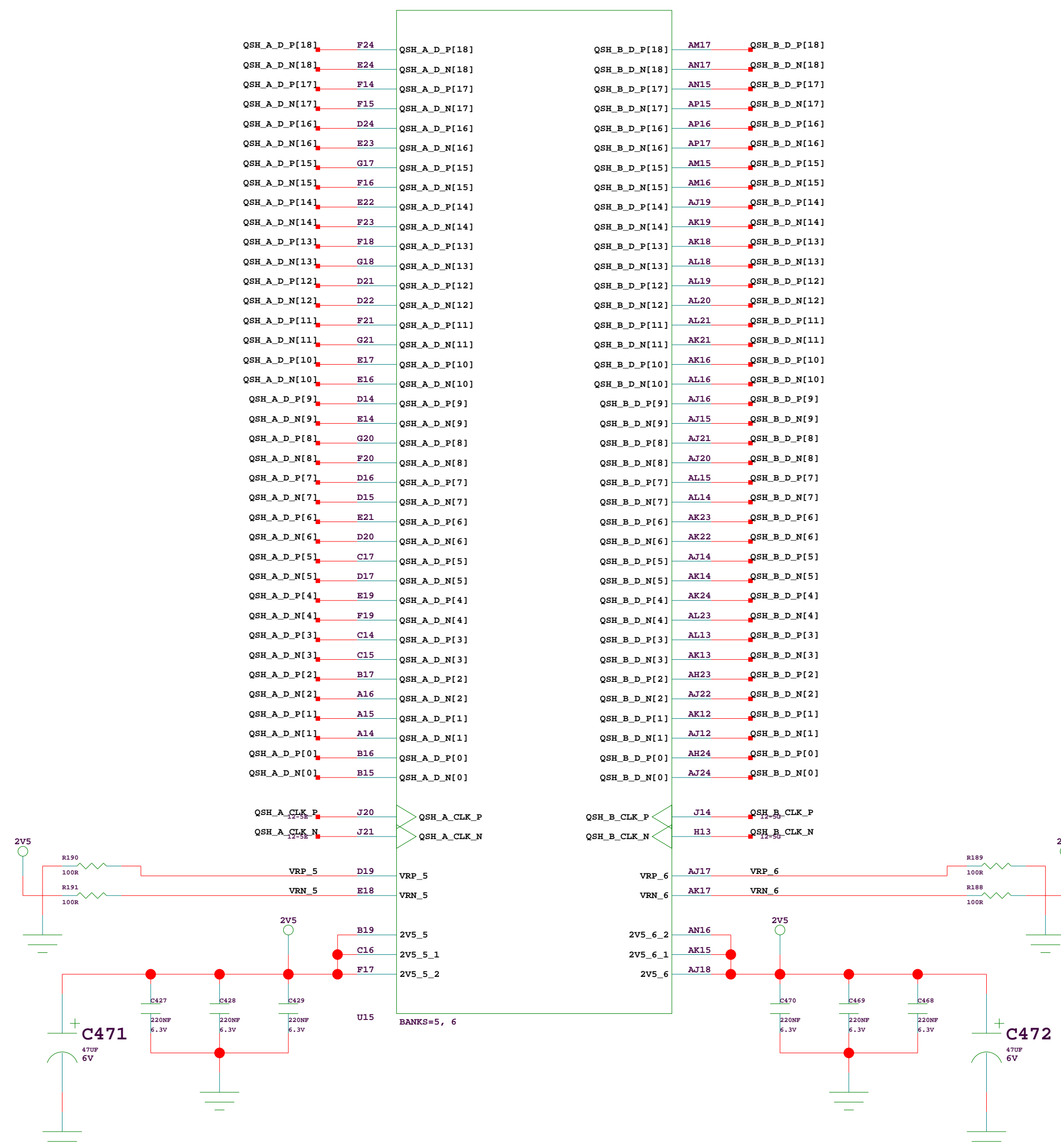
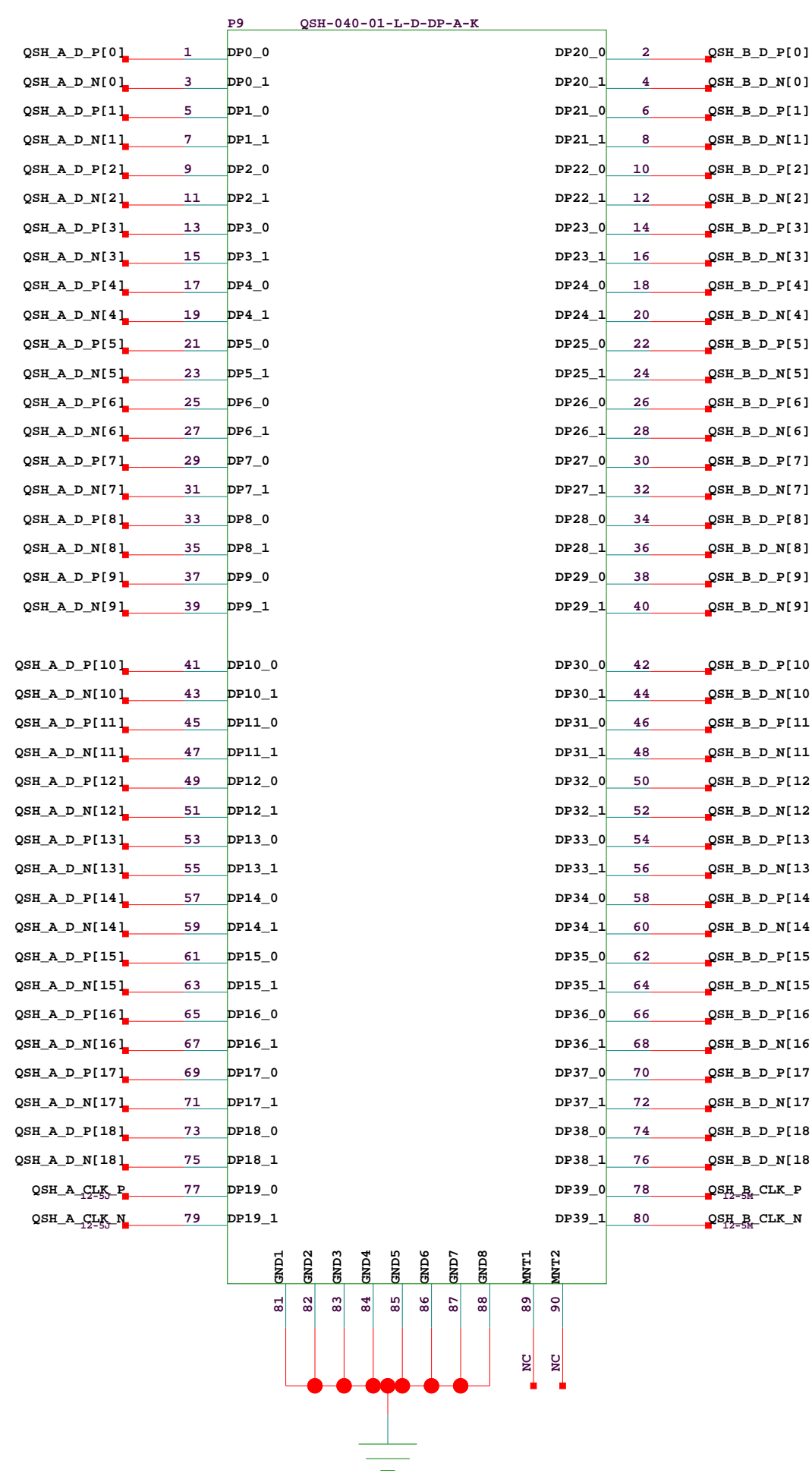


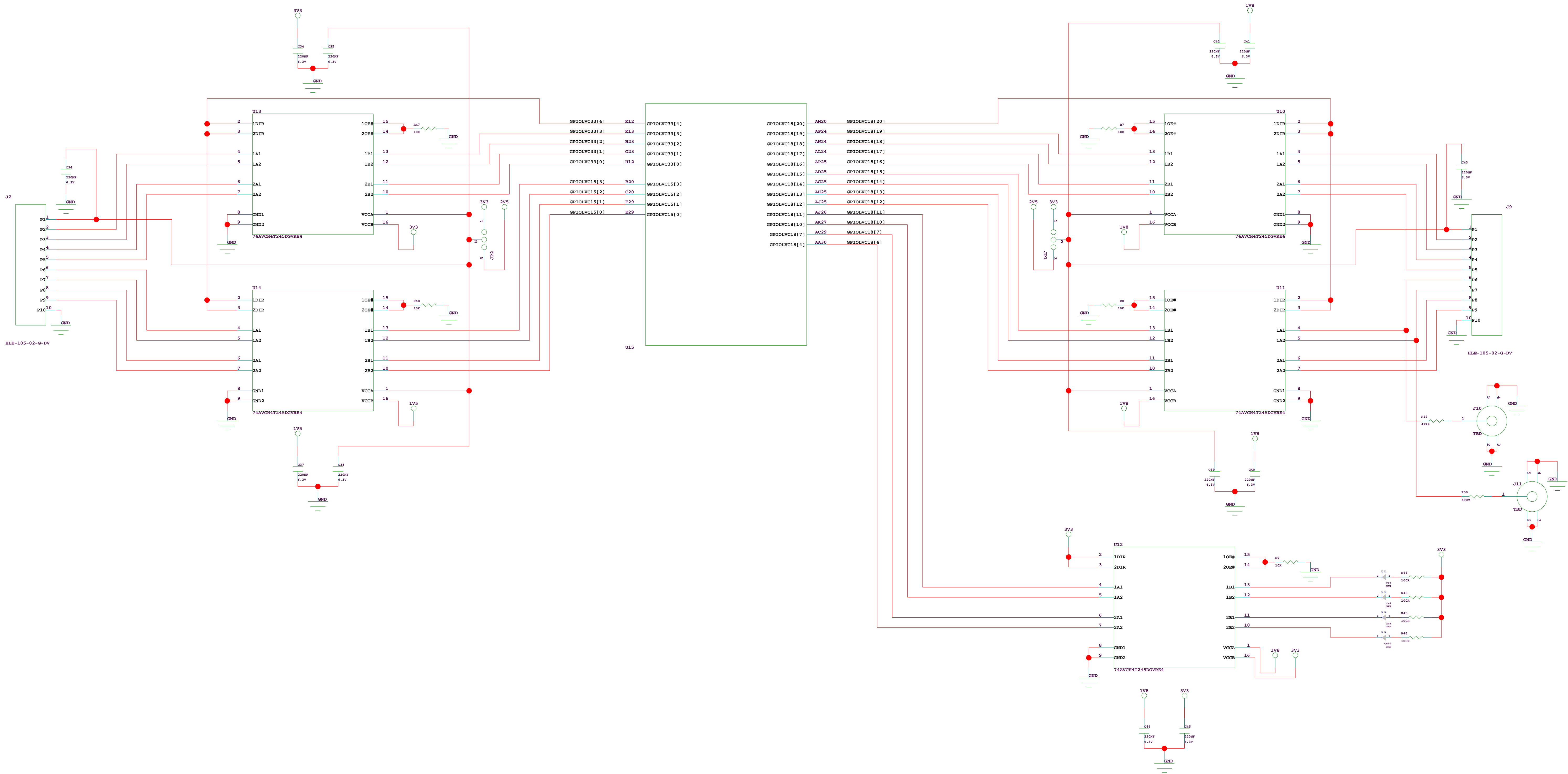


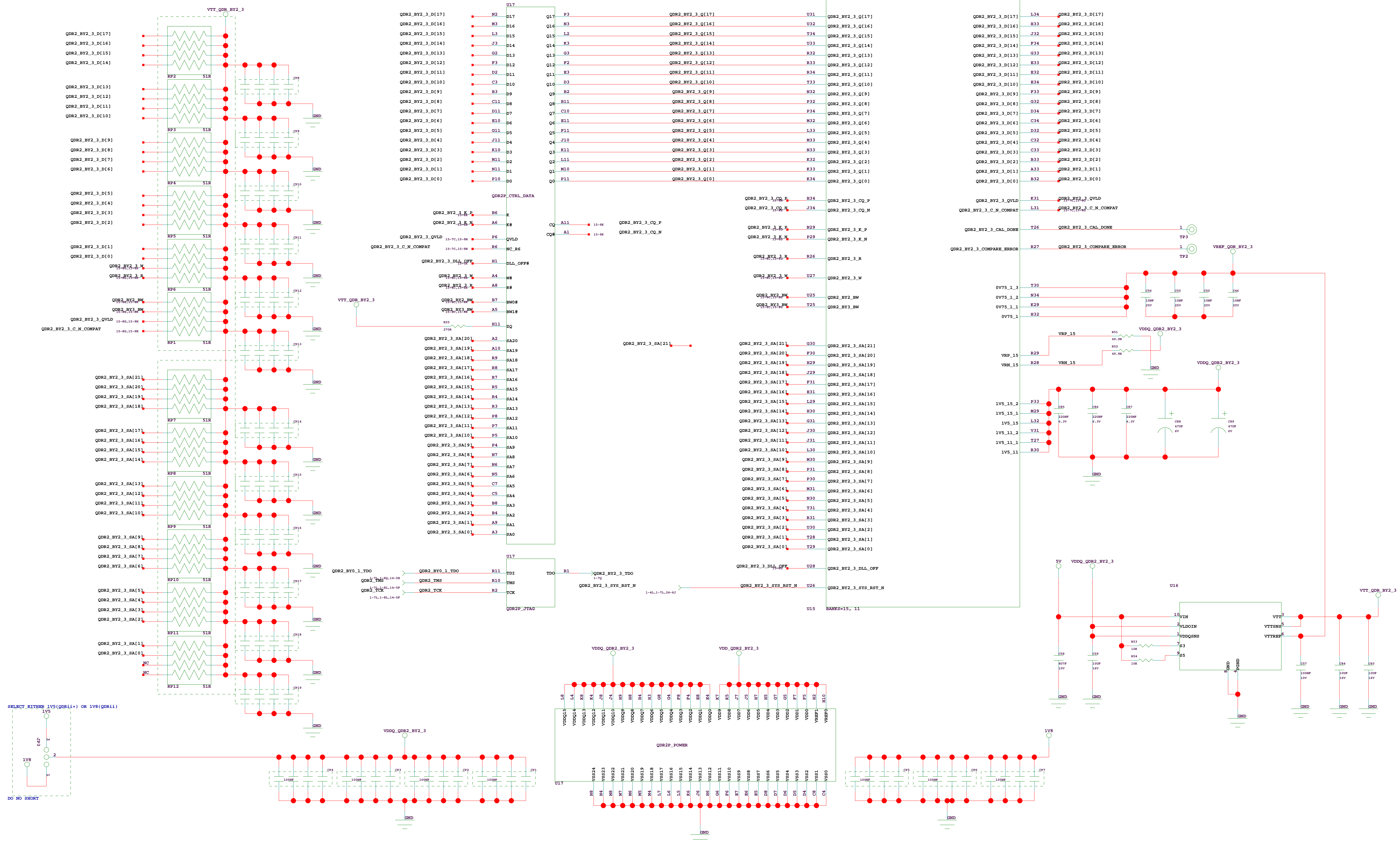






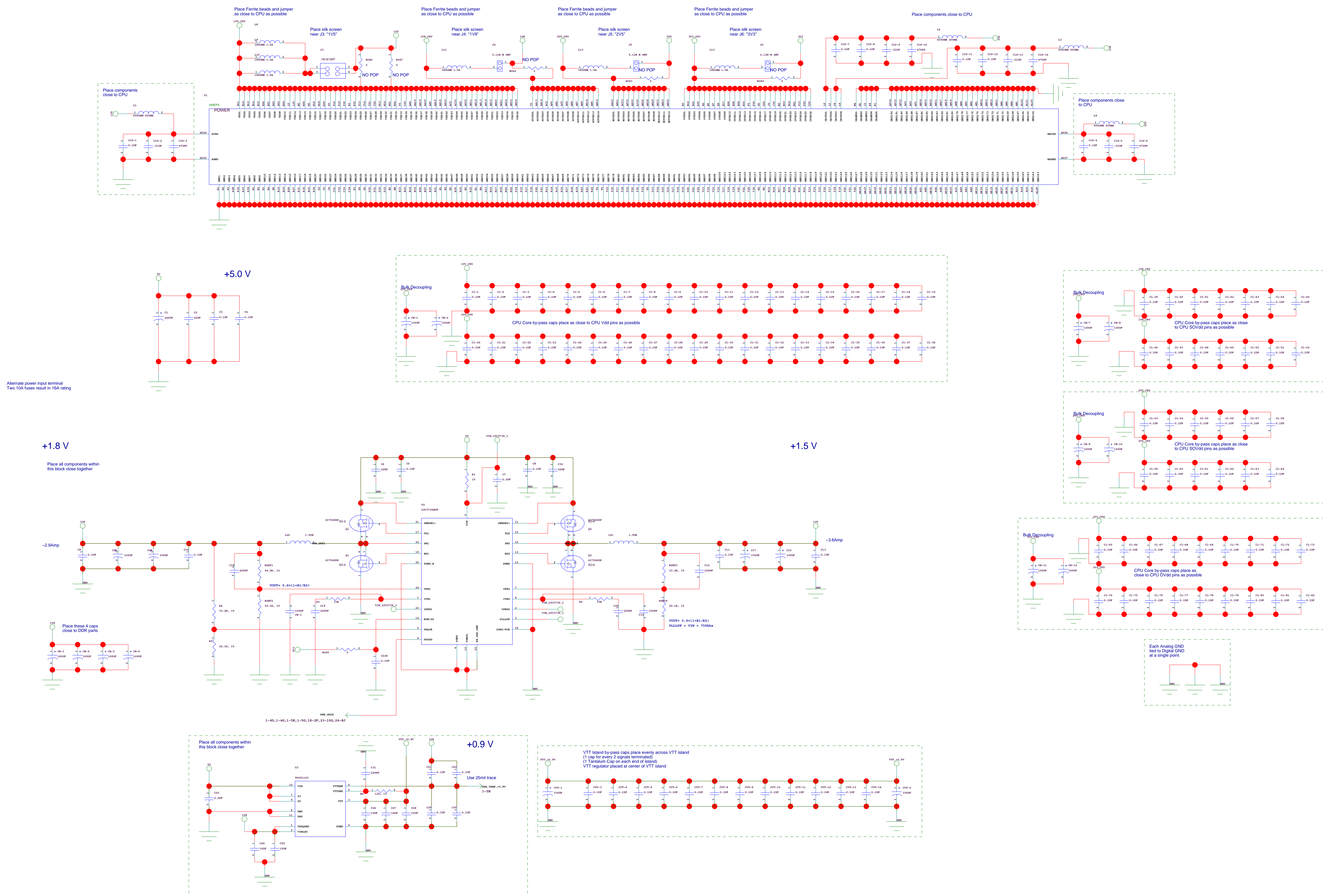


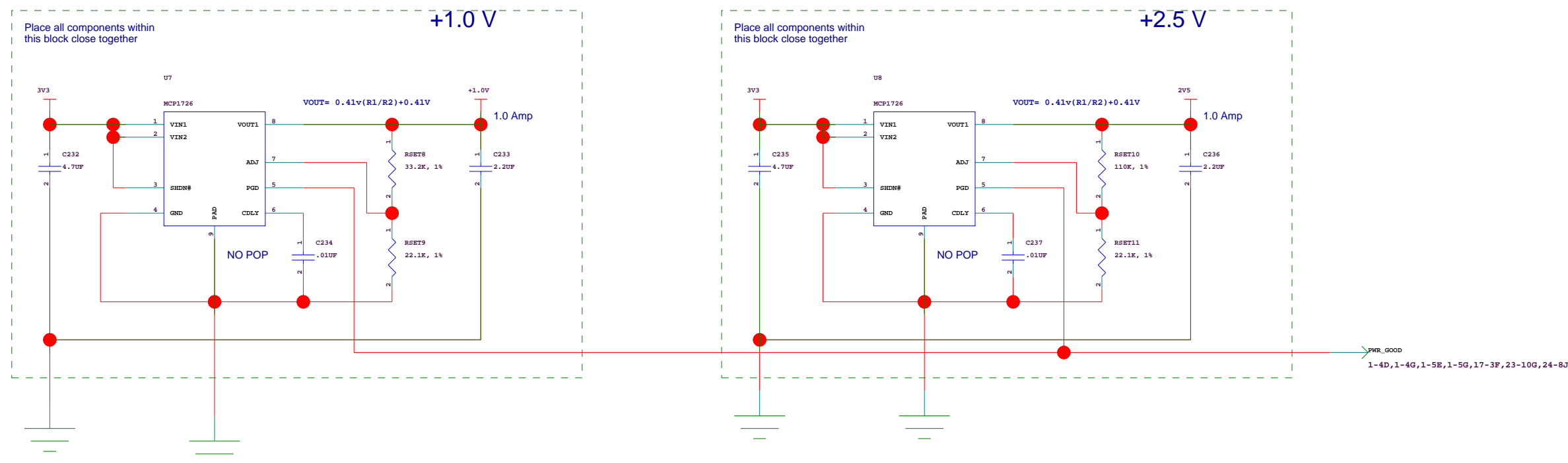
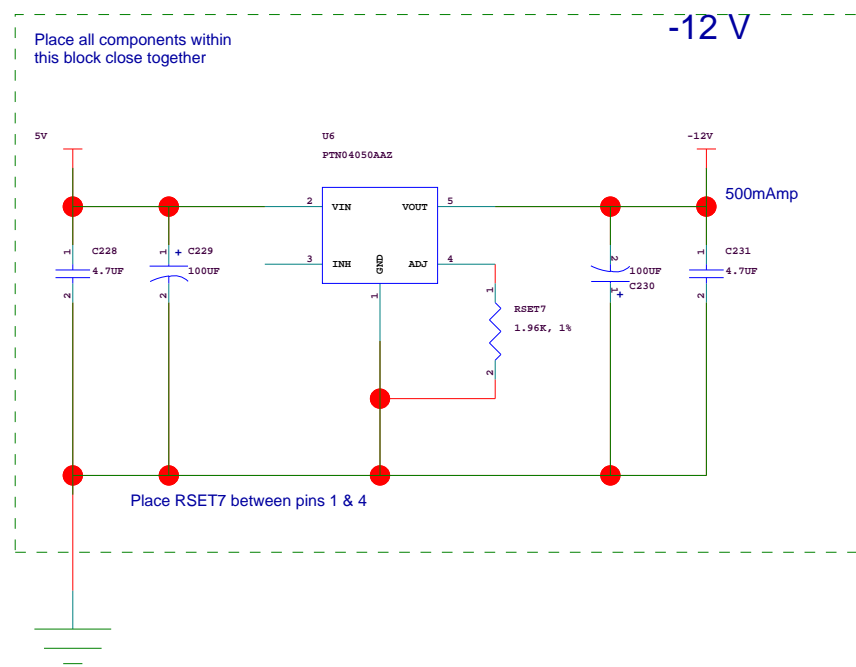
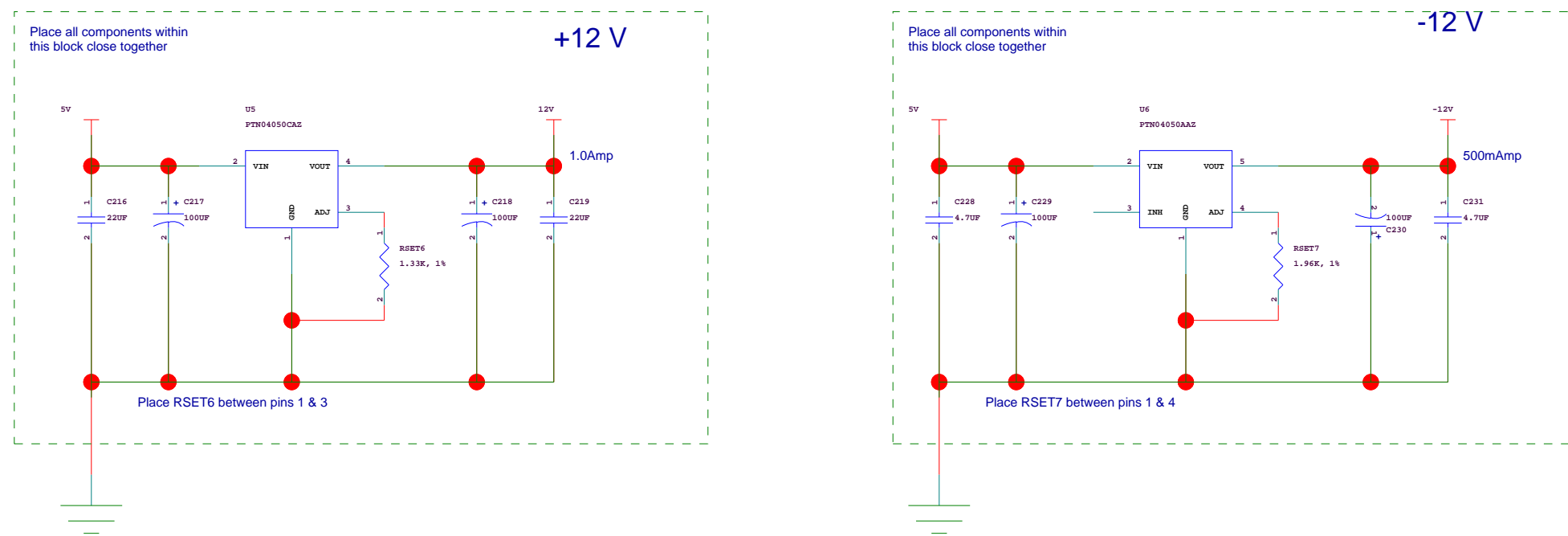
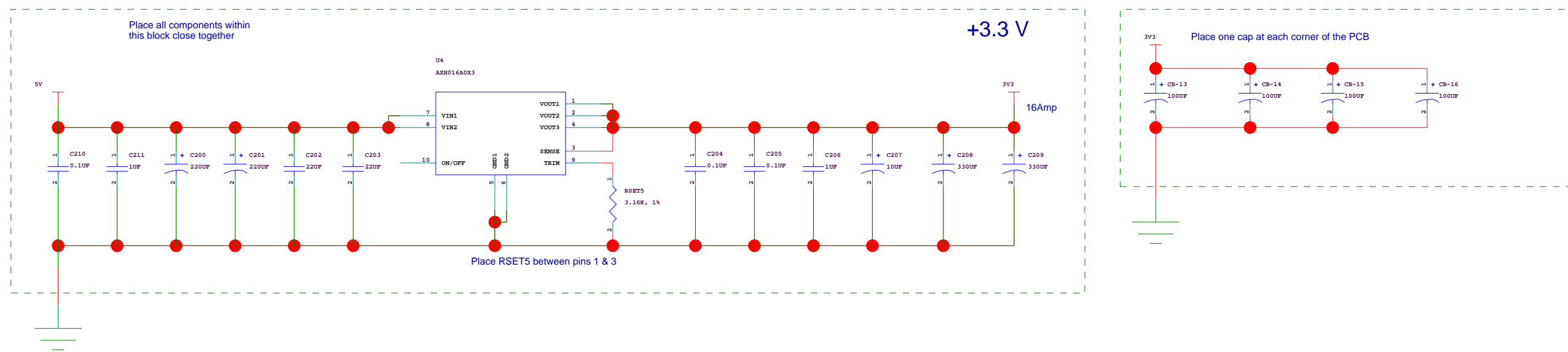




VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input







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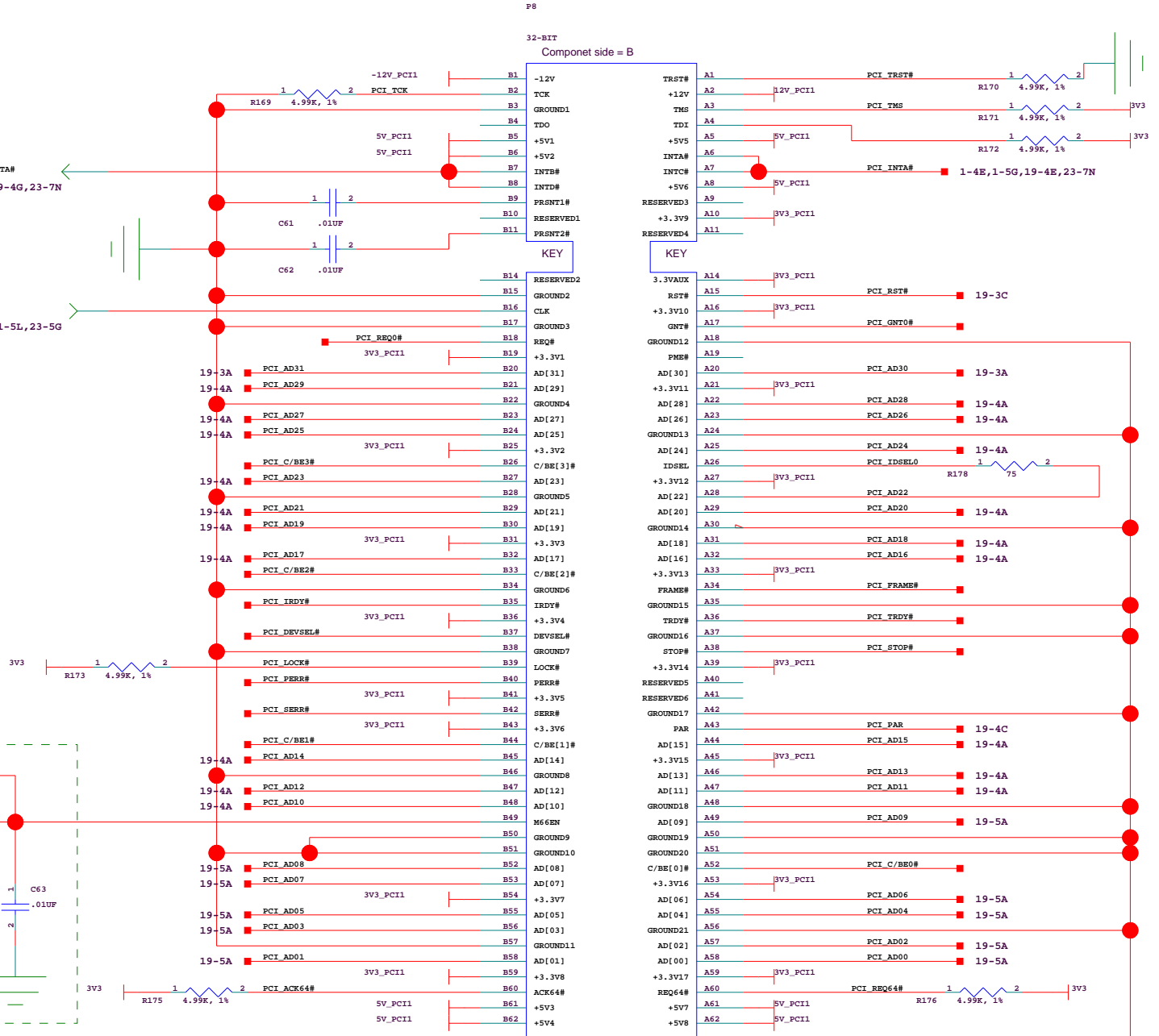
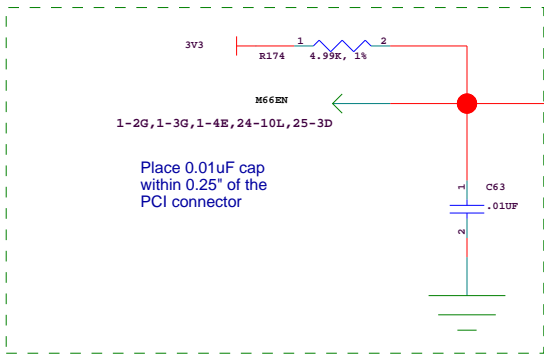
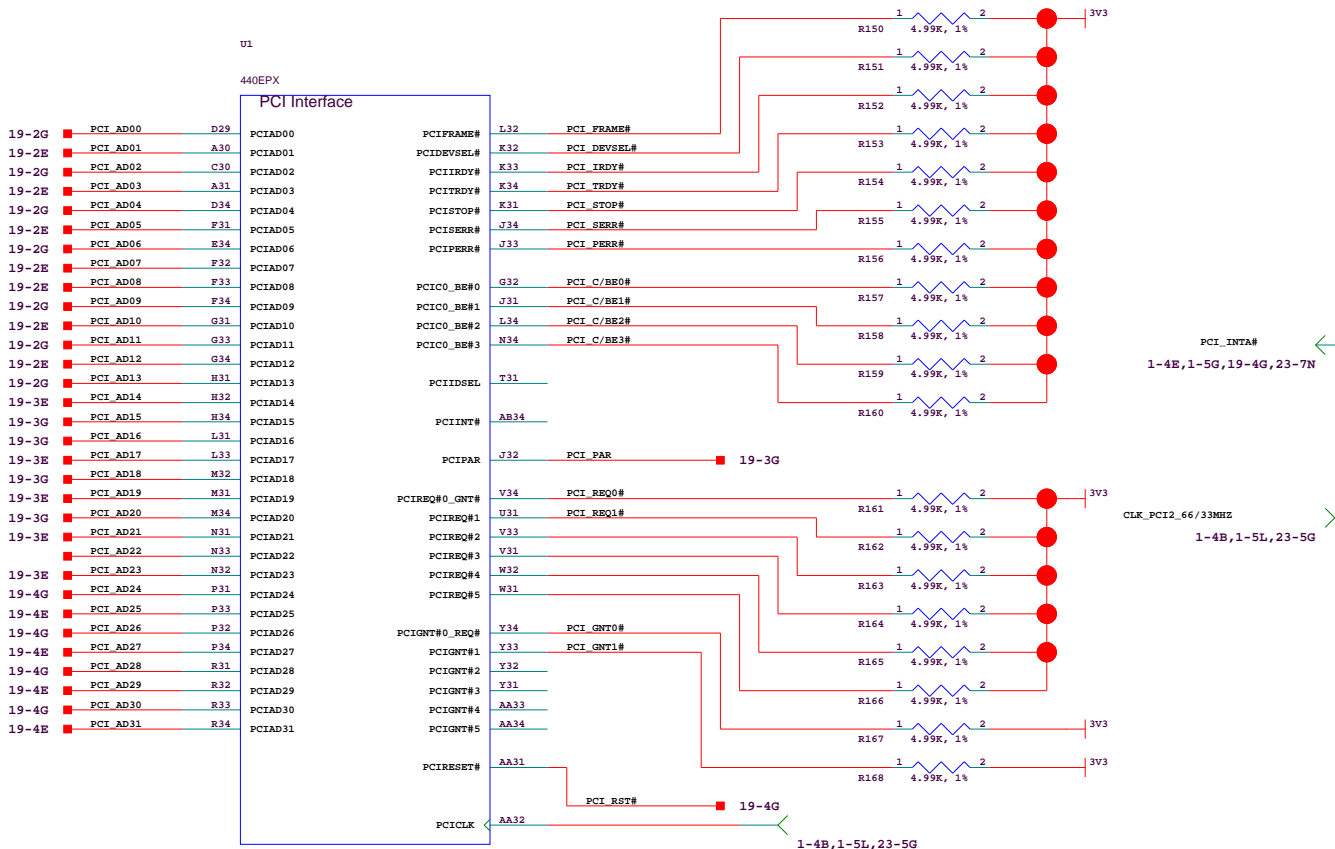
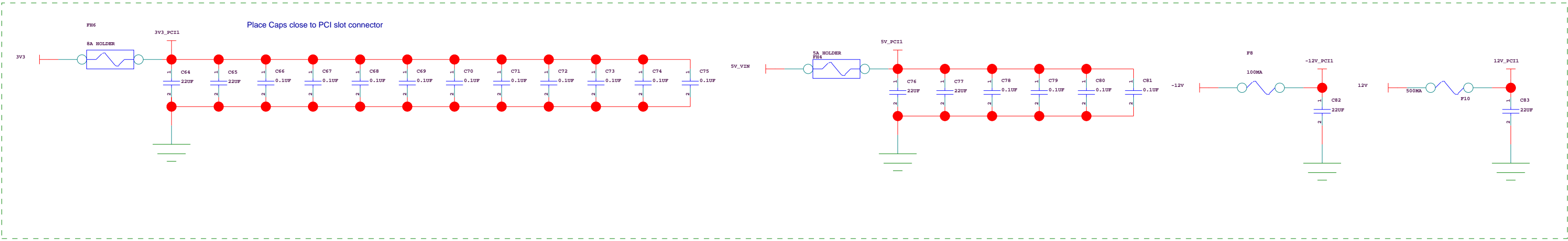
4

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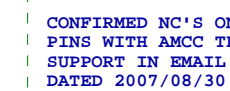
0



PCI SLOT_0

Include silkscreen text:
"SUPPORTS 3V3 IO ONLY"

Optional PRSNT signals are not used, max 25W is available		
PRSNT1#	PRSNT2#	Expansion Configuration
Open	Open	No expansion board present
Ground	Open	Expansion board present, 25 W maximum
Open	Ground	Expansion board present, 15 W maximum
Ground	Ground	Expansion board present, 7.5 W maximum



Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11.0592MHz = as short as possible
CLK_SYS_33MHz = as short as possible
CLK_CPLD_33MHz = CLK_SYS_33MHz

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PC13_66/33MHz = as short as possible
CLK_PC12_66/33MHz = CLK_PC13_66/33MHz
CLK_PC11_66/33MHz = CLK_PC12_66/33MHz + 2.5°
CLK_GETH0_25MHz = as short as possible
CLK_GETH1_25MHz = CLK_GETH0_25MHz
CLK_CPLD_50MHz = as short as possible
CLK_USB2_0_48MHz = as short as possible
CLK_USB2_0_12MHz = as short as possible

