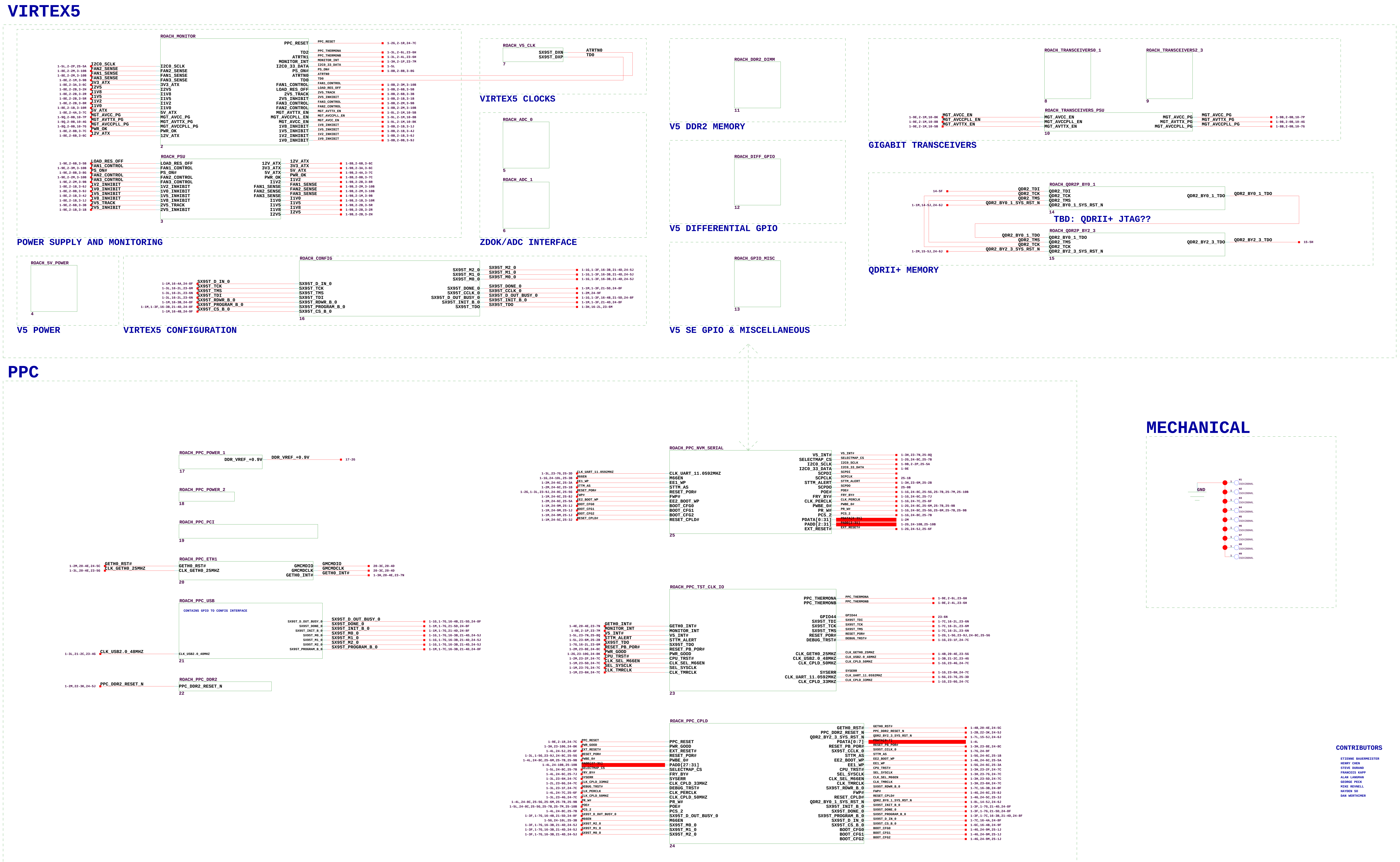
VIRTEX5
ROACH_MONITOR
ROACH_PSU
POWER SUPPLY AND MONITORING
ROACH_V5_CLK
VIRTEX5 CLOCKS
ROACH_ADC_0
ROACH_ADC_1
ZDOK/ADC INTERFACE
ROACH_DDR2_DIMM
V5 DDR2 MEMORY
ROACH_DIFF_GPIO
V5 DIFFERENTIAL GPIO
ROACH_GPIO_MISC
V5 SE GPIO & MISCELLANEOUS
ROACH_TRANSCEIVERS0_1
ROACH_TRANSCEIVERS2_3
ROACH_TRANSCEIVERS_PSU
GIGABIT TRANSCEIVERS
ROACH_QDR2P_BY0_1
ROACH_QDR2P_BY2_3
TBD: QDRII+ JTAG??
QDRII+ MEMORY
ROACH_5V_POWER
V5 POWER
ROACH_CONFIG
VIRTEX5 CONFIGURATION
PPC
ROACH_PPC_POWER_1
ROACH_PPC_POWER_2
ROACH_PPC_PCI
ROACH_PPC_ETH1
ROACH_PPC_USB
CONTAINS GPIO TO CONFIG INTERFACE
ROACH_PPC_DDR2
ROACH_PPC_NVM_SERIAL
ROACH_PPC_TST_CLK_IO
ROACH_PPC_CPLD
MECHANICAL
GND

CONTRIBUTORS

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MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2	ROACH_TOP
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO NRF-ADM-XXX-SD-0001 / REVISION A DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
10-17-2007_15:51 PATH PATH	DRAWN: F KAPP / APPR: CHECKED: E BAUERMEISTER / SHEET 1 OF 25

U59
TPS74401RGWT
5VAUX
3V3AUX
1V5AUX
TIE TO GROUND IF PLL'S ARE NOT USED
DEFAULT=POSITION 1-2
PLACE AT ACTEL 1V5 POWER PINS
TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE
DEFAULT=POSITION 2-3
JP27
JP26
JP28
VPUMP
roach_AFS600_powerpins
PLACE AT ACTEL 3V3 POWER PINS
Q11
FJD3076TM
VAREF
PTBASE
PUSH_BUTTON
J7
PB POWER SWITCH
KEY - REMOVE PIN
MONITOR RESET
CHS_SWITCH
CHS_LED0
CHS_LED1
15-91-2140
XPORT - PLACE IN REAR I/O REGION
XP1001001-03R
J28
CHASSIS_GND
roach_AFS600_pcb
U60
TEMPERATURE DIODE HEADER
J31
15-91-2200
ACTEL JTAG CONNECTOR
J27
roach_AFS600_configpins
SPARE ANALOG VOLTAGE INPUT #0
SPARE ANALOG VOLTAGE INPUT #1
SPARE GATE DRIVE OUTPUT #0
SPARE GATE DRIVE OUTPUT #1
J41
15-91-2080
U61
ADM3101EACPZ-REEL
J26
X5
ECX-306
32.768KHZ
Q12
Q13
Q14
FDS6675BZ
LOAD_RES_OFF
2V5_TRACK
12V_ATX
5V_ATX
3V3_ATX
I2V5
I1V8
I1V5
I1V2
I1V0
2V5_INHIBIT
1V8_INHIBIT
1V5_INHIBIT
1V2_INHIBIT
1V0_INHIBIT
MGT_AVCC_PG
MGT_AVTTX_PG
MGT_AVCCPLL_PG
FAN1_CONTROL
FAN1_SENSE
FAN2_CONTROL
FAN2_SENSE
FAN3_CONTROL
FAN3_SENSE
MGT_AVCC_EN
MGT_AVTTX_EN
MGT_AVCCPLL_EN
I2C0_33_DATA
I2C0_SCLK
MONITOR_INT
PPC_RESET
1-2G,1-9E,24-7C
GND

ROACH/iBOB2

COLLABORATORS:

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PATH PATH

ROACH_MONITOR

DOC NO
NRF-ADM-XXX-SD-0001

REVISION
A

DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

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SHEET 2 OF 25

AUX FAN CONNECTORS - ATX 4 PIN
J21
GND
12V
SENSE
CONTROL
47053-1000
PLACE ON SILKSCREEN: FAN1
FAN1_SENSE
FAN1_CONTROL
J20
PLACE ON SILKSCREEN: FAN2
FAN2_SENSE
FAN2_CONTROL
J19
PLACE ON SILKSCREEN: FAN3
FAN3_SENSE
FAN3_CONTROL
ATX POWER CONNECTORS
J18
3V3_1
3V3_2
COM_1
5V_1
COM_2
5V_2
COM_3
PWR_OK
5VSB
12V1_1
12V1_2
3V3_3
3V3_4
_12V
COM_4
PS_ON#
COM_5
COM_6
COM_7
N/C
5V_3
5V_4
5V_5
COM_8
20NC
44206-0007
5VAUX
N12V
PS_ON#
PWR_OK
5V_ATX
3V3_ATX
12V_ATX
J32
0015453110
J16
COM1
COM2
12V1
12V2
39-29-9042
LOAD RESISTORS FOR ATX PSU MIN LOAD
SWITCH OFF ONCE LOAD EXCEEDS MINIMUM SPEC
ADJUST RESISTOR VALUES FOR ACTUAL SUPPLY
R180
10K
Q9
NDS331N
R185
10R
5W
AC05000001009JL800
Q10
NDS331N
R187
56R
5W
AC05000005609JL800
LOAD_RES_OFF
Q8
BSS138
R181
10K
2V5
ROUTE FROM LOAD
PLACE RESISTOR CLOSE TO PTH08T210WAD
ROUTE SHORTEST
2V5_TRACK
R183
1K
C426
10UF
R177
TBD
U53
TURBOTRANS
SENSE+
VI_1
VI_0
INHIBIT/UVLADJ
TRACK
SENSE-
VO_0
VO_1
VOADJUST
GND_3
GND_2
GND_1
GND_0
PTH08T210WAD
12V
L15
BLM31PG121SN1B
C412
330UF
16V
C414
330UF
16V
C424
10UF
C425
10UF
16V
C413
470UF
6.3V
C415
470UF
6.3V
I2V5
R179
TBD
DIRECT TO P8 ON PTH08T210W, DEDICATED TRACE
2V5_INHIBIT
Q7
BSS138
1V0
U50
R144
TBD
L6
C403
330UF
16V
C401
330UF
16V
C419
10UF
1V2
C418
10UF
C402
1000UF
2V5
C400
1000UF
2V5
R143
TBD
I1V0
1V0_INHIBIT
Q4
BSS138
U49
R142
3K3
L5
C399
C397
C417
1V5
C416
C398
C396
R145
10K
I1V2
1V2_INHIBIT
Q3
U51
R146
TBD
L7
C404
C406
C420
1V8
C421
C405
C407
R147
TBD
I1V5
1V5_INHIBIT
Q5
U52
R149
TBD
L14
C411
C409
C423
C422
C410
C408
R148
TBD
I1V8
1V8_INHIBIT
Q6
GND

ADJUSTMENT AND T2 RESISTOR VALUES TBD
SOURCE VOLTAGES TO BE SELECTED

ROACH/iBOB2	**ROACH_PSU**		
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO NRF-ADM-XXX-SD-0001		REVISION A
	DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW		
10-17-2007_15:51	DRAWN: F KAPP	APPR:	
PATH PATH	CHECKED: E BAUERMEISTER	SHEET	3 OF 25

1V0
U15
1V0
C9
10UF
16V
C10
C286
C291
C292
C290
C288
C289
C287
220NF
6.3V
1V0
C8
10UF
16V
C11
C272
C276
C275
C277
C279
C278
C280
220NF
6.3V
1V0
C7
10UF
16V
C12
C263
C262
C261
C260
C259
C258
C257
220NF
6.3V
GND
1V0
C310
C309
C308
C307
C306
C305
330UF
2V5
GND
2V5
C303
C302
C304
220NF
6.3V
C311
C312
C313
33UF
6V
GND
2V5
AB11 2V5_AUX
AC12 2V5_AUX_1
L12 2V5_AUX_2
M11 2V5_AUX_3
M21 2V5_AUX_4
P11 2V5_AUX_5
P23 2V5_AUX_6
T23 2V5_AUX_7
U24 2V5_AUX_8
V11 2V5_AUX_9
V23 2V5_AUX_10
Y23 2V5_AUX_11
U15
A11 GND
A12 GND_1
A17 GND_2
A22 GND_3
A27 GND_4
A32 GND_5
AA11 GND_6
AA13 GND_7
AA15 GND_8
AA17 GND_9
AA19 GND_10
AA2 GND_11
AA21 GND_12
AA23 GND_13
AA27 GND_14
AA7 GND_15
AB12 GND_16
J33 GND_127
J23 GND_126
J2 GND_125
J18 GND_124
J13 GND_123
H6 GND_122
H26 GND_121
H21 GND_120
H2 GND_119
H16 GND_118
G9 GND_117
G4 GND_116
G34 GND_115
G29 GND_114
G19 GND_113
F7 GND_112
F32 GND_111
U15
GND

ROACH/iBOB2

COLLABORATORS:

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PATH PATH

ROACH_5V_POWER

DOC NO NRF-ADM-XXX-SD-0001	REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
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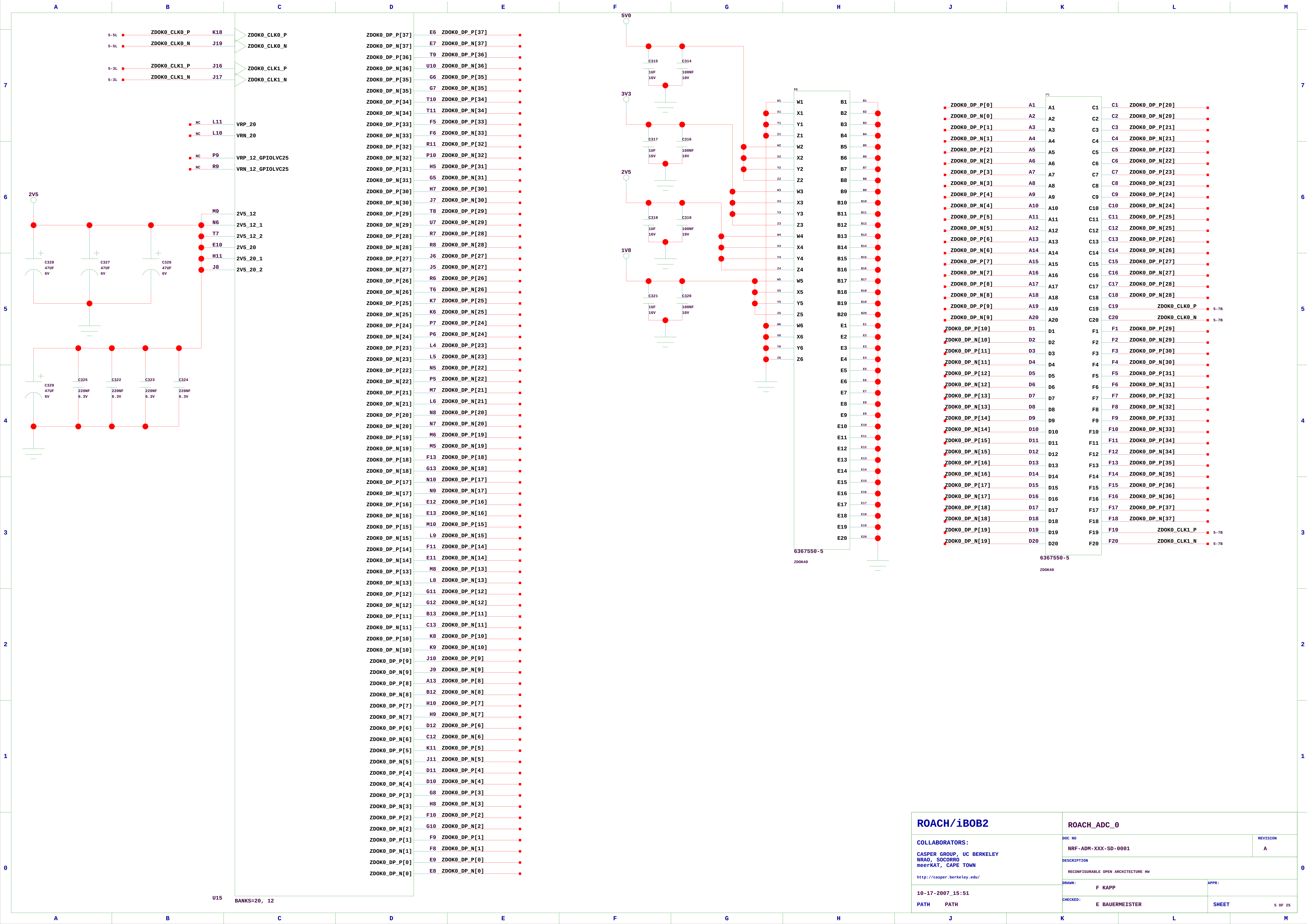
A
B
C
D
E
F
G
H
J
K
L
M
7
6
5
4
3
2
1
0
5-5L ZDOK0_CLK0_P K18 ZDOK0_CLK0_P
5-5L ZDOK0_CLK0_N J19 ZDOK0_CLK0_N
5-3L ZDOK0_CLK1_P J16 ZDOK0_CLK1_P
5-3L ZDOK0_CLK1_N J17 ZDOK0_CLK1_N
NC L11 VRP_20
NC L10 VRN_20
NC P9 VRP_12_GPIOLVC25
NC R9 VRN_12_GPIOLVC25
2V5
M9 2V5_12
N6 2V5_12_1
T7 2V5_12_2
E10 2V5_20
H11 2V5_20_1
J8 2V5_20_2
C328 47UF 6V
C327 47UF 6V
C326 47UF 6V
C329 47UF 6V
C325 220NF 6.3V
C322 220NF 6.3V
C323 220NF 6.3V
C324 220NF 6.3V
U15
BANKS=20, 12
ZDOK0_DP_P[37] E6 ZDOK0_DP_P[37]
ZDOK0_DP_N[37] E7 ZDOK0_DP_N[37]
ZDOK0_DP_P[36] T9 ZDOK0_DP_P[36]
ZDOK0_DP_N[36] U10 ZDOK0_DP_N[36]
ZDOK0_DP_P[35] G6 ZDOK0_DP_P[35]
ZDOK0_DP_N[35] G7 ZDOK0_DP_N[35]
ZDOK0_DP_P[34] T10 ZDOK0_DP_P[34]
ZDOK0_DP_N[34] T11 ZDOK0_DP_N[34]
ZDOK0_DP_P[33] F5 ZDOK0_DP_P[33]
ZDOK0_DP_N[33] F6 ZDOK0_DP_N[33]
ZDOK0_DP_P[32] R11 ZDOK0_DP_P[32]
ZDOK0_DP_N[32] P10 ZDOK0_DP_N[32]
ZDOK0_DP_P[31] H5 ZDOK0_DP_P[31]
ZDOK0_DP_N[31] G5 ZDOK0_DP_N[31]
ZDOK0_DP_P[30] H7 ZDOK0_DP_P[30]
ZDOK0_DP_N[30] J7 ZDOK0_DP_N[30]
ZDOK0_DP_P[29] T8 ZDOK0_DP_P[29]
ZDOK0_DP_N[29] U7 ZDOK0_DP_N[29]
ZDOK0_DP_P[28] R7 ZDOK0_DP_P[28]
ZDOK0_DP_N[28] R8 ZDOK0_DP_N[28]
ZDOK0_DP_P[27] J6 ZDOK0_DP_P[27]
ZDOK0_DP_N[27] J5 ZDOK0_DP_N[27]
ZDOK0_DP_P[26] R6 ZDOK0_DP_P[26]
ZDOK0_DP_N[26] T6 ZDOK0_DP_N[26]
ZDOK0_DP_P[25] K7 ZDOK0_DP_P[25]
ZDOK0_DP_N[25] K6 ZDOK0_DP_N[25]
ZDOK0_DP_P[24] P7 ZDOK0_DP_P[24]
ZDOK0_DP_N[24] P6 ZDOK0_DP_N[24]
ZDOK0_DP_P[23] L4 ZDOK0_DP_P[23]
ZDOK0_DP_N[23] L5 ZDOK0_DP_N[23]
ZDOK0_DP_P[22] N5 ZDOK0_DP_P[22]
ZDOK0_DP_N[22] P5 ZDOK0_DP_N[22]
ZDOK0_DP_P[21] M7 ZDOK0_DP_P[21]
ZDOK0_DP_N[21] L6 ZDOK0_DP_N[21]
ZDOK0_DP_P[20] N8 ZDOK0_DP_P[20]
ZDOK0_DP_N[20] N7 ZDOK0_DP_N[20]
ZDOK0_DP_P[19] M6 ZDOK0_DP_P[19]
ZDOK0_DP_N[19] M5 ZDOK0_DP_N[19]
ZDOK0_DP_P[18] F13 ZDOK0_DP_P[18]
ZDOK0_DP_N[18] G13 ZDOK0_DP_N[18]
ZDOK0_DP_P[17] N10 ZDOK0_DP_P[17]
ZDOK0_DP_N[17] N9 ZDOK0_DP_N[17]
ZDOK0_DP_P[16] E12 ZDOK0_DP_P[16]
ZDOK0_DP_N[16] E13 ZDOK0_DP_N[16]
ZDOK0_DP_P[15] M10 ZDOK0_DP_P[15]
ZDOK0_DP_N[15] L9 ZDOK0_DP_N[15]
ZDOK0_DP_P[14] F11 ZDOK0_DP_P[14]
ZDOK0_DP_N[14] E11 ZDOK0_DP_N[14]
ZDOK0_DP_P[13] M8 ZDOK0_DP_P[13]
ZDOK0_DP_N[13] L8 ZDOK0_DP_N[13]
ZDOK0_DP_P[12] G11 ZDOK0_DP_P[12]
ZDOK0_DP_N[12] G12 ZDOK0_DP_N[12]
ZDOK0_DP_P[11] B13 ZDOK0_DP_P[11]
ZDOK0_DP_N[11] C13 ZDOK0_DP_N[11]
ZDOK0_DP_P[10] K8 ZDOK0_DP_P[10]
ZDOK0_DP_N[10] K9 ZDOK0_DP_N[10]
ZDOK0_DP_P[9] J10 ZDOK0_DP_P[9]
ZDOK0_DP_N[9] J9 ZDOK0_DP_N[9]
ZDOK0_DP_P[8] A13 ZDOK0_DP_P[8]
ZDOK0_DP_N[8] B12 ZDOK0_DP_N[8]
ZDOK0_DP_P[7] H10 ZDOK0_DP_P[7]
ZDOK0_DP_N[7] H9 ZDOK0_DP_N[7]
ZDOK0_DP_P[6] D12 ZDOK0_DP_P[6]
ZDOK0_DP_N[6] C12 ZDOK0_DP_N[6]
ZDOK0_DP_P[5] K11 ZDOK0_DP_P[5]
ZDOK0_DP_N[5] J11 ZDOK0_DP_N[5]
ZDOK0_DP_P[4] D11 ZDOK0_DP_P[4]
ZDOK0_DP_N[4] D10 ZDOK0_DP_N[4]
ZDOK0_DP_P[3] G8 ZDOK0_DP_P[3]
ZDOK0_DP_N[3] H8 ZDOK0_DP_N[3]
ZDOK0_DP_P[2] F10 ZDOK0_DP_P[2]
ZDOK0_DP_N[2] G10 ZDOK0_DP_N[2]
ZDOK0_DP_P[1] F9 ZDOK0_DP_P[1]
ZDOK0_DP_N[1] F8 ZDOK0_DP_N[1]
ZDOK0_DP_P[0] E9 ZDOK0_DP_P[0]
ZDOK0_DP_N[0] E8 ZDOK0_DP_N[0]
5V0
C315 1UF 16V
C314 100NF 10V
3V3
C317 1UF 16V
C316 100NF 10V
2V5
C318 1UF 16V
C319 100NF 10V
1V8
C321 1UF 16V
C320 100NF 10V
P5
W1 X1 Y1 Z1 W2 X2 Y2 Z2 W3 X3 Y3 Z3 W4 X4 Y4 Z4 W5 X5 Y5 Z5 W6 X6 Y6 Z6
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20
E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20
6367550-5
ZDOK40
P5
ZDOK0_DP_P[0] A1 A1 C1 C1 ZDOK0_DP_P[20]
ZDOK0_DP_N[0] A2 A2 C2 C2 ZDOK0_DP_N[20]
ZDOK0_DP_P[1] A3 A3 C3 C3 ZDOK0_DP_P[21]
ZDOK0_DP_N[1] A4 A4 C4 C4 ZDOK0_DP_N[21]
ZDOK0_DP_P[2] A5 A5 C5 C5 ZDOK0_DP_P[22]
ZDOK0_DP_N[2] A6 A6 C6 C6 ZDOK0_DP_N[22]
ZDOK0_DP_P[3] A7 A7 C7 C7 ZDOK0_DP_P[23]
ZDOK0_DP_N[3] A8 A8 C8 C8 ZDOK0_DP_N[23]
ZDOK0_DP_P[4] A9 A9 C9 C9 ZDOK0_DP_P[24]
ZDOK0_DP_N[4] A10 A10 C10 C10 ZDOK0_DP_N[24]
ZDOK0_DP_P[5] A11 A11 C11 C11 ZDOK0_DP_P[25]
ZDOK0_DP_N[5] A12 A12 C12 C12 ZDOK0_DP_N[25]
ZDOK0_DP_P[6] A13 A13 C13 C13 ZDOK0_DP_P[26]
ZDOK0_DP_N[6] A14 A14 C14 C14 ZDOK0_DP_N[26]
ZDOK0_DP_P[7] A15 A15 C15 C15 ZDOK0_DP_P[27]
ZDOK0_DP_N[7] A16 A16 C16 C16 ZDOK0_DP_N[27]
ZDOK0_DP_P[8] A17 A17 C17 C17 ZDOK0_DP_P[28]
ZDOK0_DP_N[8] A18 A18 C18 C18 ZDOK0_DP_N[28]
ZDOK0_DP_P[9] A19 A19 C19 C19 ZDOK0_CLK0_P 5-7B
ZDOK0_DP_N[9] A20 A20 C20 C20 ZDOK0_CLK0_N 5-7B
ZDOK0_DP_P[10] D1 D1 F1 F1 ZDOK0_DP_P[29]
ZDOK0_DP_N[10] D2 D2 F2 F2 ZDOK0_DP_N[29]
ZDOK0_DP_P[11] D3 D3 F3 F3 ZDOK0_DP_P[30]
ZDOK0_DP_N[11] D4 D4 F4 F4 ZDOK0_DP_N[30]
ZDOK0_DP_P[12] D5 D5 F5 F5 ZDOK0_DP_P[31]
ZDOK0_DP_N[12] D6 D6 F6 F6 ZDOK0_DP_N[31]
ZDOK0_DP_P[13] D7 D7 F7 F7 ZDOK0_DP_P[32]
ZDOK0_DP_N[13] D8 D8 F8 F8 ZDOK0_DP_N[32]
ZDOK0_DP_P[14] D9 D9 F9 F9 ZDOK0_DP_P[33]
ZDOK0_DP_N[14] D10 D10 F10 F10 ZDOK0_DP_N[33]
ZDOK0_DP_P[15] D11 D11 F11 F11 ZDOK0_DP_P[34]
ZDOK0_DP_N[15] D12 D12 F12 F12 ZDOK0_DP_N[34]
ZDOK0_DP_P[16] D13 D13 F13 F13 ZDOK0_DP_P[35]
ZDOK0_DP_N[16] D14 D14 F14 F14 ZDOK0_DP_N[35]
ZDOK0_DP_P[17] D15 D15 F15 F15 ZDOK0_DP_P[36]
ZDOK0_DP_N[17] D16 D16 F16 F16 ZDOK0_DP_N[36]
ZDOK0_DP_P[18] D17 D17 F17 F17 ZDOK0_DP_P[37]
ZDOK0_DP_N[18] D18 D18 F18 F18 ZDOK0_DP_N[37]
ZDOK0_DP_P[19] D19 D19 F19 F19 ZDOK0_CLK1_P 5-7B
ZDOK0_DP_N[19] D20 D20 F20 F20 ZDOK0_CLK1_N 5-7B
6367550-5
ZDOK40

ROACH/iBOB2

ROACH_ADC_0

COLLABORATORS:

CASPER GROUP, UC BERKELEY
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PATH PATH

DOC NO NRF-ADM-XXX-SD-0001

REVISION A

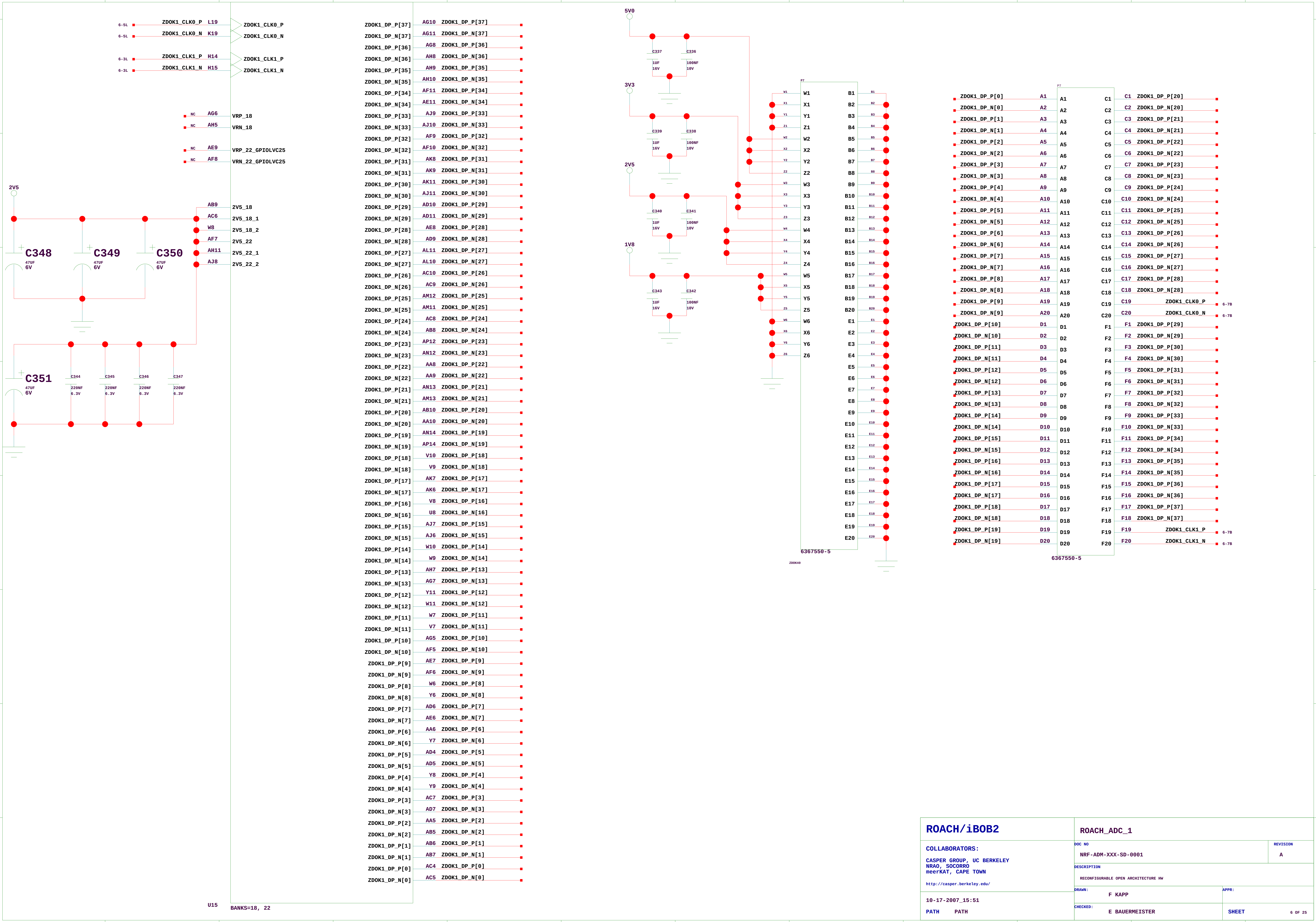
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 5 OF 25


ZDOK1_CLK0_P L19
ZDOK1_CLK0_N K19
ZDOK1_CLK1_P H14
ZDOK1_CLK1_N H15
6-5L
6-3L
NC AG6 VRP_18
NC AH5 VRN_18
NC AE9 VRP_22_GPIOLVC25
NC AF8 VRN_22_GPIOLVC25
2V5
AB9 2V5_18
AC6 2V5_18_1
W8 2V5_18_2
AF7 2V5_22
AH11 2V5_22_1
AJ8 2V5_22_2
C348 47UF 6V
C349 47UF 6V
C350 47UF 6V
C351 47UF 6V
C344 220NF 6.3V
C345 220NF 6.3V
C346 220NF 6.3V
C347 220NF 6.3V
ZDOK1_DP_P[37] AG10
ZDOK1_DP_N[37] AG11
ZDOK1_DP_P[36] AG8
ZDOK1_DP_N[36] AH8
ZDOK1_DP_P[35] AH9
ZDOK1_DP_N[35] AH10
ZDOK1_DP_P[34] AF11
ZDOK1_DP_N[34] AE11
ZDOK1_DP_P[33] AJ9
ZDOK1_DP_N[33] AJ10
ZDOK1_DP_P[32] AF9
ZDOK1_DP_N[32] AF10
ZDOK1_DP_P[31] AK8
ZDOK1_DP_N[31] AK9
ZDOK1_DP_P[30] AK11
ZDOK1_DP_N[30] AJ11
ZDOK1_DP_P[29] AD10
ZDOK1_DP_N[29] AD11
ZDOK1_DP_P[28] AE8
ZDOK1_DP_N[28] AD9
ZDOK1_DP_P[27] AL11
ZDOK1_DP_N[27] AL10
ZDOK1_DP_P[26] AC10
ZDOK1_DP_N[26] AC9
ZDOK1_DP_P[25] AM12
ZDOK1_DP_N[25] AM11
ZDOK1_DP_P[24] AC8
ZDOK1_DP_N[24] AB8
ZDOK1_DP_P[23] AP12
ZDOK1_DP_N[23] AN12
ZDOK1_DP_P[22] AA8
ZDOK1_DP_N[22] AA9
ZDOK1_DP_P[21] AN13
ZDOK1_DP_N[21] AM13
ZDOK1_DP_P[20] AB10
ZDOK1_DP_N[20] AA10
ZDOK1_DP_P[19] AN14
ZDOK1_DP_N[19] AP14
ZDOK1_DP_P[18] V10
ZDOK1_DP_N[18] V9
ZDOK1_DP_P[17] AK7
ZDOK1_DP_N[17] AK6
ZDOK1_DP_P[16] V8
ZDOK1_DP_N[16] U8
ZDOK1_DP_P[15] AJ7
ZDOK1_DP_N[15] AJ6
ZDOK1_DP_P[14] W10
ZDOK1_DP_N[14] W9
ZDOK1_DP_P[13] AH7
ZDOK1_DP_N[13] AG7
ZDOK1_DP_P[12] Y11
ZDOK1_DP_N[12] W11
ZDOK1_DP_P[11] W7
ZDOK1_DP_N[11] V7
ZDOK1_DP_P[10] AG5
ZDOK1_DP_N[10] AF5
ZDOK1_DP_P[9] AE7
ZDOK1_DP_N[9] AF6
ZDOK1_DP_P[8] W6
ZDOK1_DP_N[8] Y6
ZDOK1_DP_P[7] AD6
ZDOK1_DP_N[7] AE6
ZDOK1_DP_P[6] AA6
ZDOK1_DP_N[6] Y7
ZDOK1_DP_P[5] AD4
ZDOK1_DP_N[5] AD5
ZDOK1_DP_P[4] Y8
ZDOK1_DP_N[4] Y9
ZDOK1_DP_P[3] AC7
ZDOK1_DP_N[3] AD7
ZDOK1_DP_P[2] AA5
ZDOK1_DP_N[2] AB5
ZDOK1_DP_P[1] AB6
ZDOK1_DP_N[1] AB7
ZDOK1_DP_P[0] AC4
ZDOK1_DP_N[0] AC5
U15
BANKS=18, 22
5V0
C337 1UF 16V
C336 100NF 10V
3V3
C339 1UF 16V
C338 100NF 10V
2V5
C340 1UF 16V
C341 100NF 10V
1V8
C343 1UF 16V
C342 100NF 10V
P7
W1 X1 Y1 Z1 W2 X2 Y2 Z2 W3 X3 Y3 Z3 W4 X4 Y4 Z4 W5 X5 Y5 Z5 W6 X6 Y6 Z6
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19 B20
E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20
6367550-5
ZDOK40
P7
ZDOK1_DP_P[0] A1
ZDOK1_DP_N[0] A2
ZDOK1_DP_P[1] A3
ZDOK1_DP_N[1] A4
ZDOK1_DP_P[2] A5
ZDOK1_DP_N[2] A6
ZDOK1_DP_P[3] A7
ZDOK1_DP_N[3] A8
ZDOK1_DP_P[4] A9
ZDOK1_DP_N[4] A10
ZDOK1_DP_P[5] A11
ZDOK1_DP_N[5] A12
ZDOK1_DP_P[6] A13
ZDOK1_DP_N[6] A14
ZDOK1_DP_P[7] A15
ZDOK1_DP_N[7] A16
ZDOK1_DP_P[8] A17
ZDOK1_DP_N[8] A18
ZDOK1_DP_P[9] A19
ZDOK1_DP_N[9] A20
ZDOK1_DP_P[10] D1
ZDOK1_DP_N[10] D2
ZDOK1_DP_P[11] D3
ZDOK1_DP_N[11] D4
ZDOK1_DP_P[12] D5
ZDOK1_DP_N[12] D6
ZDOK1_DP_P[13] D7
ZDOK1_DP_N[13] D8
ZDOK1_DP_P[14] D9
ZDOK1_DP_N[14] D10
ZDOK1_DP_P[15] D11
ZDOK1_DP_N[15] D12
ZDOK1_DP_P[16] D13
ZDOK1_DP_N[16] D14
ZDOK1_DP_P[17] D15
ZDOK1_DP_N[17] D16
ZDOK1_DP_P[18] D17
ZDOK1_DP_N[18] D18
ZDOK1_DP_P[19] D19
ZDOK1_DP_N[19] D20
C1 ZDOK1_DP_P[20]
C2 ZDOK1_DP_N[20]
C3 ZDOK1_DP_P[21]
C4 ZDOK1_DP_N[21]
C5 ZDOK1_DP_P[22]
C6 ZDOK1_DP_N[22]
C7 ZDOK1_DP_P[23]
C8 ZDOK1_DP_N[23]
C9 ZDOK1_DP_P[24]
C10 ZDOK1_DP_N[24]
C11 ZDOK1_DP_P[25]
C12 ZDOK1_DP_N[25]
C13 ZDOK1_DP_P[26]
C14 ZDOK1_DP_N[26]
C15 ZDOK1_DP_P[27]
C16 ZDOK1_DP_N[27]
C17 ZDOK1_DP_P[28]
C18 ZDOK1_DP_N[28]
C19 ZDOK1_CLK0_P 6-7B
C20 ZDOK1_CLK0_N 6-7B
F1 ZDOK1_DP_P[29]
F2 ZDOK1_DP_N[29]
F3 ZDOK1_DP_P[30]
F4 ZDOK1_DP_N[30]
F5 ZDOK1_DP_P[31]
F6 ZDOK1_DP_N[31]
F7 ZDOK1_DP_P[32]
F8 ZDOK1_DP_N[32]
F9 ZDOK1_DP_P[33]
F10 ZDOK1_DP_N[33]
F11 ZDOK1_DP_P[34]
F12 ZDOK1_DP_N[34]
F13 ZDOK1_DP_P[35]
F14 ZDOK1_DP_N[35]
F15 ZDOK1_DP_P[36]
F16 ZDOK1_DP_N[36]
F17 ZDOK1_DP_P[37]
F18 ZDOK1_DP_N[37]
F19 ZDOK1_CLK1_P 6-7B
F20 ZDOK1_CLK1_N 6-7B
6367550-5
A B C D E F G H J K L M
7 6 5 4 3 2 1 0

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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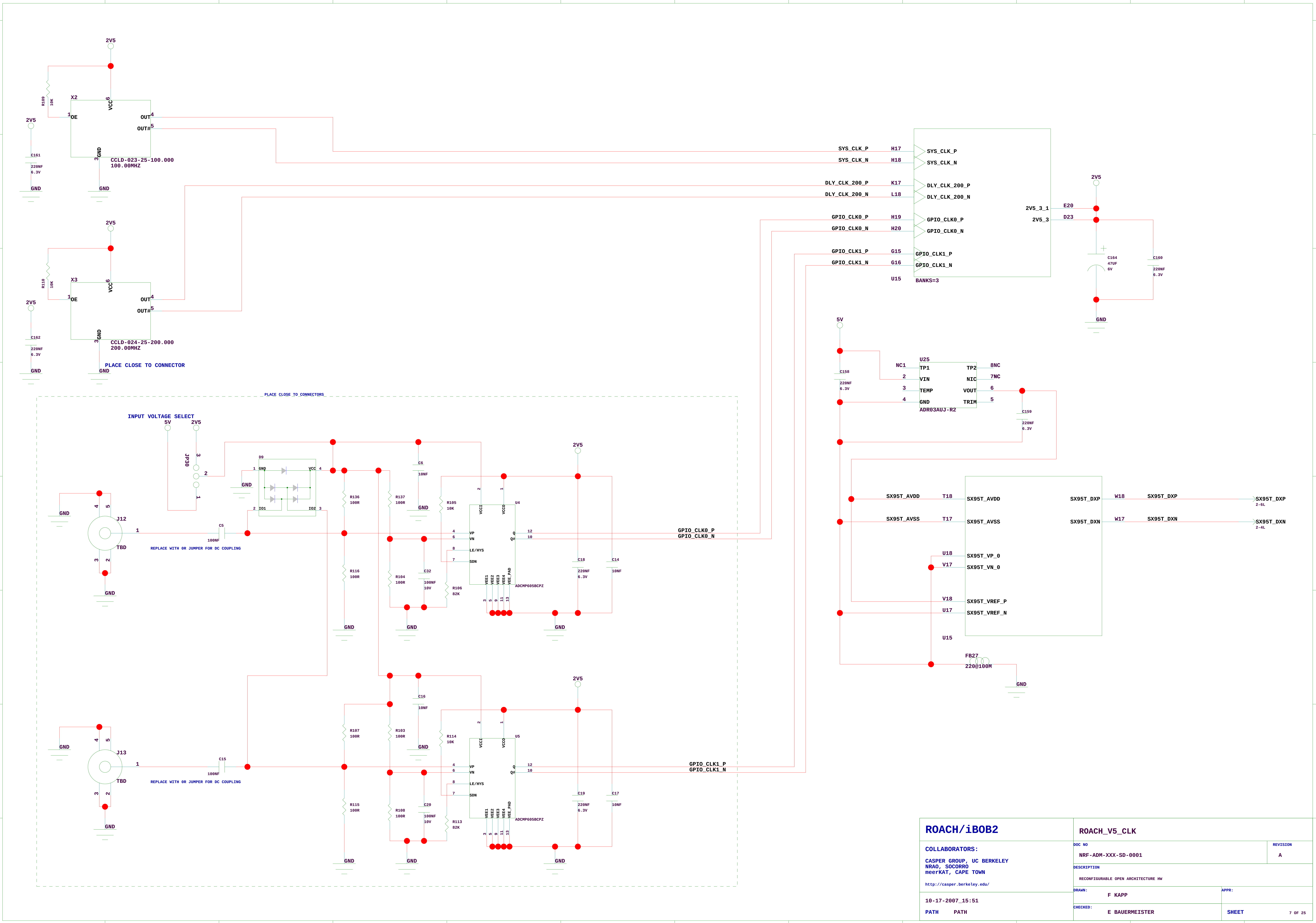
PATH PATH

ROACH_ADC_1

DOC NO NRF-ADM-XXX-SD-0001	REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 6 OF 25


2V5
R109
10K
X2
VCC
6
1
OE
OUT
4
OUT#
5
3
GND
CCLD-023-25-100.000
100.00MHZ
2V5
C161
220NF
6.3V
GND
GND
2V5
R110
10K
X3
VCC
6
1
OE
OUT
4
OUT#
5
3
GND
CCLD-024-25-200.000
200.00MHZ
2V5
C162
220NF
6.3V
GND
GND
PLACE CLOSE TO CONNECTOR
SYS_CLK_P
H17
SYS_CLK_N
H18
DLY_CLK_200_P
K17
DLY_CLK_200_N
L18
GPIO_CLK0_P
H19
GPIO_CLK0_N
H20
GPIO_CLK1_P
G15
GPIO_CLK1_N
G16
U15
SYS_CLK_P
SYS_CLK_N
DLY_CLK_200_P
DLY_CLK_200_N
GPIO_CLK0_P
GPIO_CLK0_N
GPIO_CLK1_P
GPIO_CLK1_N
BANKS=3
2V5_3_1
E20
2V5_3
D23
2V5
C164
47UF
6V
C160
220NF
6.3V
GND
5V
C158
220NF
6.3V
U25
NC1
TP1
2
VIN
3
TEMP
4
GND
ADR03AUJ-R2
TP2
8NC
NIC
7NC
VOUT
6
TRIM
5
C159
220NF
6.3V
SX95T_AVDD
T18
SX95T_AVSS
T17
U18
V17
V18
U17
SX95T_AVDD
SX95T_AVSS
SX95T_VP_0
SX95T_VN_0
SX95T_VREF_P
SX95T_VREF_N
SX95T_DXP
W18
SX95T_DXP
SX95T_DXP
2-6L
SX95T_DXN
W17
SX95T_DXN
SX95T_DXN
2-4L
U15
FB27
220@100M
GND
PLACE CLOSE TO CONNECTORS
INPUT VOLTAGE SELECT
5V
2V5
JP30
3
2
1
D9
1
GND
VCC
4
2
IO1
IO2
3
GND
GND
J12
4
5
1
TBD
3
2
GND
C5
100NF
REPLACE WITH OR JUMPER FOR DC COUPLING
C6
10NF
GND
R136
100R
R137
100R
R105
10K
R116
100R
R104
100R
C32
100NF
10V
R106
82K
GND
GND
U4
2
VCCI
1
VCCO
4
VP
6
VN
8
LE/HYS
7
SDN
Q
12
Q#
10
VEE1
VEE2
VEE3
VEE4
VEE_PAD
3
5
9
11
13
ADCMP605BCPZ
2V5
C18
220NF
6.3V
C14
10NF
GND
GPIO_CLK0_P
GPIO_CLK0_N
GND
J13
4
5
1
TBD
3
2
GND
C15
100NF
REPLACE WITH OR JUMPER FOR DC COUPLING
C16
10NF
GND
R107
100R
R103
100R
R114
10K
R115
100R
R108
100R
C20
100NF
10V
R113
82K
GND
GND
U5
2
VCCI
1
VCCO
4
VP
6
VN
8
LE/HYS
7
SDN
Q
12
Q#
10
VEE1
VEE2
VEE3
VEE4
VEE_PAD
3
5
9
11
13
ADCMP605BCPZ
2V5
C19
220NF
6.3V
C17
10NF
GND
GPIO_CLK1_P
GPIO_CLK1_N

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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PATH PATH

ROACH_V5_CLK

DOC NO
NRF-ADM-XXX-SD-0001

REVISION
A

DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 7 OF 25

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB3 220@100M
FB4 220@100M
C94 220NF 6.3V
C93 220NF 6.3V
C92 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_112 R3
R4
MGTAVCCPLL_112 T3
MGTAVTTRX_112 N3
MGT_112_REF_CLK_P P4
MGT_112_REF_CLK_N P3
MGTRX0_112_P N1
MGTRX0_112_N P1
MGTRX1_112_P T1
MGTRX1_112_N R1
U15
MGTRREF
MGT_VTRXC
V4 MGTRREF
V5 MGTAVTTRXC
R56 49.9R
MGTAVTTTX_112
MGTAVTTTX_112_1
M3 MGTAVTTTX_112
U3
MGTTX0_112_P
MGTTX0_112_N
MGTTX1_112_P
MGTTX1_112_N
M2 MGTTX0_112_P
N2 MGTTX0_112_N
U2 MGTTX1_112_P
T2 MGTTX1_112_N
FB25 220@100M
FB5 220@100M
C126 220NF 6.3V
C96 220NF 6.3V
2V5
FB26 220@100M
C137 220NF 6.3V
R96 10K
JP6
X1
OE
VCC
OUT
OUT#
GND
CCLD-023-25-156.250
156.25MHZ
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
C104 10NF 25V
C105 10NF 25V
C106 10NF 25V
C107 10NF 25V
C109 10NF 25V
C108 10NF 25V
3V3
R79 150R
D2
OPTICAL MODULE FAULT - RED LED
P3
S1 DL0P
S2 DL0N
S3 DL1P
S4 DL1N
S5 DL2P
S6 DL2N
S7 DL3P
S8 DL3N
S16 SL0P
S15 SL0N
S14 SL1P
S13 SL1N
S12 SL2P
S11 SL2N
S10 SL3P
S9 SL3N
SIG_GND1 G1
SIG_GND2 G2
SIG_GND3 G3
SIG_GND4 G4
SIG_GND5 G5
SIG_GND6 G6
SIG_GND7 G7
SIG_GND8 G8
SIG_GND9 G9
SIG_GND10 G10
FCN-268F036-G/3DB
JP4
ODIS0
R90 10K
C130 10NF
C131 10NF
FAULT0
G4 AND G8 CONNECTED IN 2X2 MODULE
R97 5K1
R57 3K9
R59 6K8
R58 3K9
C127 10NF
U21
IN-
IN+
OUT
MAX9032AKA
U20
U22
AND2
SN74AHC1G08DCKR
MGT_AVCC
FB11 220@100M
FB9 220@100M
FB10 220@100M
MGTAVCC_114 AA3
MGTAVCC_114_1 AA4
MGTAVCCPLL_114 AB3
MGTAVTTRX_114 W3
MGT_114_REF_CLK_P Y4 NC
MGT_114_REF_CLK_N Y3 NC
MGTRX0_114_P W1
MGTRX0_114_N Y1
MGTRX1_114_P AB1
MGTRX1_114_N AA1
C102 220NF 6.3V
C101 220NF 6.3V
C100 220NF 6.3V
C140 10NF 25V
C141 10NF 25V
C142 10NF 25V
C143 10NF 25V
MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT
MGTAVTTTX_114
MGTAVTTTX_114_1
AC3 MGTAVTTTX_114
V3
FB8 220@100M
C99 220NF 6.3V
MGTTX0_114_P V2
MGTTX0_114_N W2
MGTTX1_114_P AC2
MGTTX1_114_N AB2
U18
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
TPS2031D
R99 10K
C129 10NF
C128 100NF
C138 4.7UF 16V
C90 22UF
FB17 220@100M
FB15 220@100M
FB16 220@100M
MGTAVCC_116 J3
MGTAVCC_116_1 J4
MGTAVCCPLL_116 K3
MGTAVTTRX_116 G3
MGT_116_REF_CLK_P H4 NC
MGT_116_REF_CLK_N H3 NC
MGTRX0_116_P G1
MGTRX0_116_N H1
MGTRX1_116_P K1
MGTRX1_116_N J1
C119 220NF 6.3V
C118 220NF 6.3V
C115 220NF 6.3V
C110 10NF 25V
C111 10NF 25V
C112 10NF 25V
C113 10NF 25V
MGTAVTTTX_116_1 L3
MGTAVTTTX_116 F3
FB14 220@100M
C115 220NF 6.3V
MGTTX0_116_P F2
MGTTX0_116_N G2
MGTTX1_116_P L2
MGTTX1_116_N K2
R82 150R
D3
S19 DL0P
S20 DL0N
S21 DL1P
S22 DL1N
S23 DL2P
S24 DL2N
S25 DL3P
S26 DL3N
S34 SL0P
S33 SL0N
S32 SL1P
S31 SL1N
S30 SL2P
S29 SL2N
S28 SL3P
S27 SL3N
G10 G11 G12 G13 G14 G15 G16 G17 G18 G19
JP5
ODIS1
R91 10K
C134 10NF
C132 10NF
FAULT1
R98 5K1
R93 3K9
R94 6K8
R95 3K9
C133 10NF
U23
U19
R100 10K
C135 10NF
C136 100NF
C139 4.7UF 16V
C91 22UF
FB22 220@100M
FB24 220@100M
FB23 220@100M
MGTAVCC_118 AG3
MGTAVCC_118_1 AG4
MGTAVCCPLL_118 AH3
MGTAVTTRX_118 AE3
MGT_118_REF_CLK_P AF4 NC
MGT_118_REF_CLK_N AF3 NC
MGTRX0_118_P AE1
MGTRX0_118_N AF1
MGTRX1_118_P AH1
MGTRX1_118_N AG1
C123 220NF 6.3V
C114 220NF 6.3V
C125 220NF 6.3V
C144 10NF 25V
C145 10NF 25V
C146 10NF 25V
C147 10NF 25V
MGTAVTTTX_118_1 AJ3
MGTAVTTTX_118 AD3
FB19 220@100M
C121 220NF 6.3V
MGTTX0_118_P AD2
MGTTX0_118_N AE2
MGTTX1_118_P AJ2
MGTTX1_118_N AH2
A B C D E F G H J K L M N P Q R S
11 10 9 8 7 6 5 4 3 2 1 0

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ROACH_TRANSCEIVERS0_1

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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PATH PATH

DOC NO
NRF-ADM-XXX-SD-0001

REVISION
A

DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 8 OF 25

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB28 220@100M
FB30 220@100M
FB31 220@100M
C171 220NF 6.3V
C170 220NF 6.3V
C169 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_120 D5
F4
MGTAVCCPLL_120 D3
MGTAVTTRX_120 C3
MGT_120_REF_CLK_P E4
MGT_120_REF_CLK_N D4
MGTRX0_120_P A3
MGTRX0_120_N A2
MGTRX1_120_P D1
MGTRX1_120_N C1
MGTAVCC_120
MGTAVCC_120_1
MGTAVCCPLL_120
MGTAVTTRX_120
MGT_120_REF_CLK_P
MGT_120_REF_CLK_N
MGTRX0_120_P
MGTRX0_120_N
MGTRX1_120_P
MGTRX1_120_N
U15
MGTAVTTTX_120_1 E3
MGTAVTTTX_120 C4
MGTTX0_120_P B4
MGTTX0_120_N B3
MGTTX1_120_P E2
MGTTX1_120_N D2
FB32 220@100M
C173 220NF 6.3V
2V5
FB52 220@100M
C248 220NF 6.3V
R131 10K
X4
OE
VCC
OUT
OUT#
GND
JP9
CCLD-033-25-156.250
156.25MHZ
MGT_REFCLK_Q2_P
MGT_REFCLK_Q2_N
C181 10NF 25V
C182 10NF 25V
C183 10NF 25V
C184 10NF 25V
C186 10NF 25V
C185 10NF 25V
3V3
R122 100R
OPTICAL MODULE FAULT - RED LED
P3
DL0P
DL0N
DL1P
DL1N
DL2P
DL2N
DL3P
DL3N
SL0P
SL0N
SL1P
SL1N
SL2P
SL2N
SL3P
SL3N
SIG_GND1
SIG_GND2
SIG_GND3
SIG_GND4
SIG_GND5
SIG_GND6
SIG_GND7
SIG_GND8
SIG_GND9
SIG_GND10
FCN-268F036-G/3DB
JP7
ODIS2
R123 10K
C240 10NF
C242 10NF
FAULT2
G4 AND G6 CONNECTED IN 2X2 MODULE
R121 5K1
R120 3K9
R119 6K8
R118 3K9
C241 10NF
U34
U30
IN-
IN+
OUT
MAX9032AKA
U36
AND2
SN74AHC1G08DCKR
U28
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
TPS2031D
R117 10K
C239 10NF
C227 100NF
C167 4.7UF 16V
C165 22UF
FB38 220@100M
FB36 220@100M
FB37 220@100M
C179 220NF 6.3V
C178 220NF 6.3V
C177 220NF 6.3V
MGTAVCC_122 AJ4
AK5
MGTAVCCPLL_122 AM4
MGTAVTTRX_122 AL3
MGT_122_REF_CLK_P NC AL5
MGT_122_REF_CLK_N NC AL4
MGTRX0_122_P AL1
MGTRX0_122_N AM1
MGTRX1_122_P AP3
MGTRX1_122_N AP2
MGTAVCC_122
MGTAVCC_122_1
MGTAVCCPLL_122
MGTAVTTRX_122
MGTAVTTTX_122_1 AM3
MGTAVTTTX_122 AK3
MGTTX0_122_P AK2
MGTTX0_122_N AL2
MGTTX1_122_P AN4
MGTTX1_122_N AN3
FB35 220@100M
C175 220NF 6.3V
C251 10NF 25V
C252 10NF 25V
C250 10NF 25V
C249 10NF 25V
FB44 220@100M
FB42 220@100M
FB43 220@100M
C220 220NF 6.3V
C215 220NF 6.3V
C212 220NF 6.3V
MGTAVCC_124 C7
D7
MGTAVCCPLL_124 C6
MGTAVTTRX_124 C9
MGT_124_REF_CLK_P NC D8
MGT_124_REF_CLK_N NC C8
MGTRX0_124_P A9
MGTRX0_124_N A8
MGTRX1_124_P A6
MGTRX1_124_N A7
MGTAVTTTX_124_1 C5
MGTAVTTTX_124 C10
MGTTX0_124_P B10
MGTTX0_124_N B9
MGTTX1_124_P B5
MGTTX1_124_N B6
FB41 220@100M
C213 220NF 6.3V
C187 10NF 25V
C188 10NF 25V
C189 10NF 25V
C190 10NF 25V
R125 100R
P3
ODIS3
JP8
R124 10K
C245 10NF
C243 10NF
FAULT3
R126 5K1
R127 3K9
R128 6K8
R129 3K9
C244 10NF
U37
U29
R130 10K
C246 10NF
C247 100NF
C168 4.7UF 16V
C166 22UF
FB49 220@100M
FB51 220@100M
FB50 220@100M
C225 220NF 6.3V
C191 220NF 6.3V
C226 220NF 6.3V
MGTAVCC_126 AL8
AM8
MGTAVCCPLL_126 AM9
MGTAVTTRX_126 AM6
MGT_126_REF_CLK_P NC AL7
MGT_126_REF_CLK_N NC AM7
MGTRX0_126_P AP6
MGTRX0_126_N AP7
MGTRX1_126_P AP9
MGTRX1_126_N AP8
MGTAVTTTX_126_1 AM5
MGTAVTTTX_126 AM10
MGTTX0_126_P AN5
MGTTX0_126_N AN6
MGTTX1_126_P AN10
MGTTX1_126_N AN9
FB46 220@100M
C223 220NF 6.3V
C256 10NF 25V
C255 10NF 25V
C254 10NF 25V
C253 10NF 25V
A B C D E F G H J K L M N P Q R S
11 10 9 8 7 6 5 4 3 2 1 0

ROACH/iBOB2

ROACH_TRANSCEIVERS2_3

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
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10-17-2007_15:51

PATH PATH

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

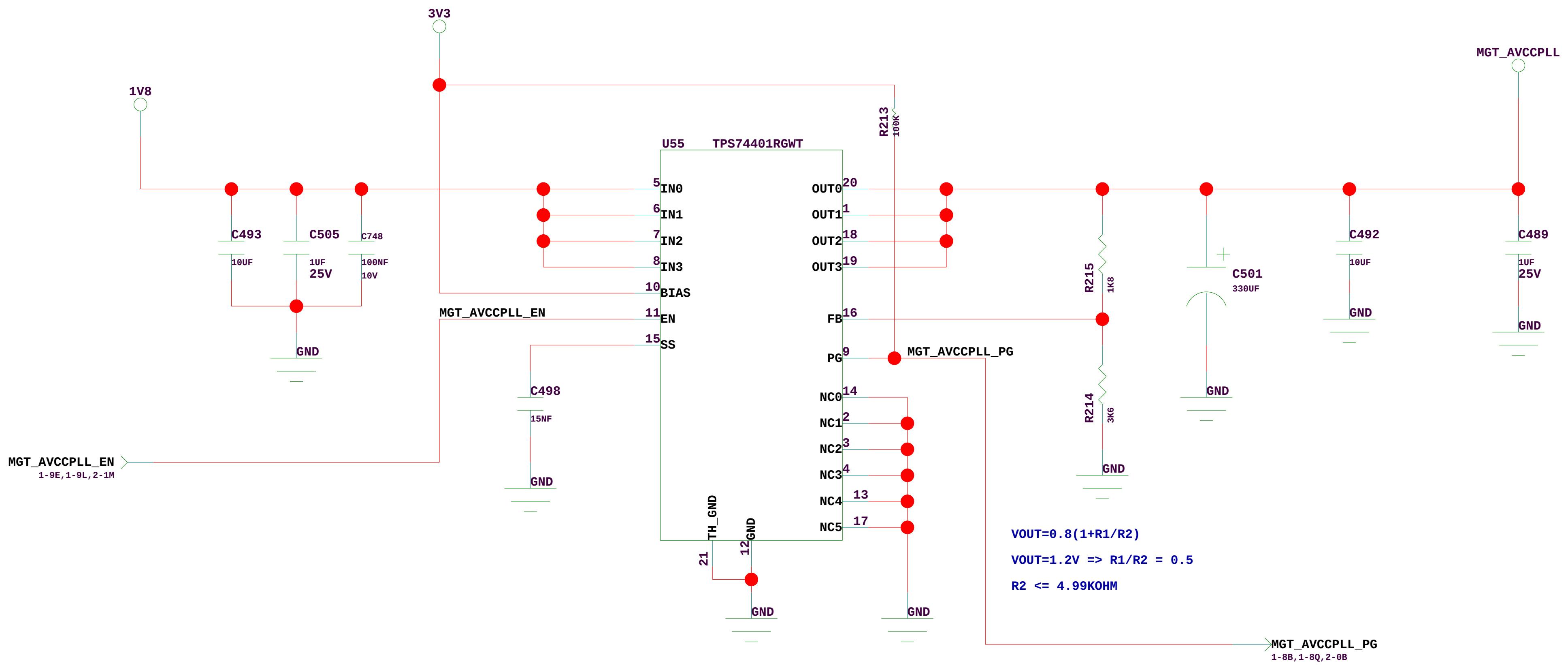
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

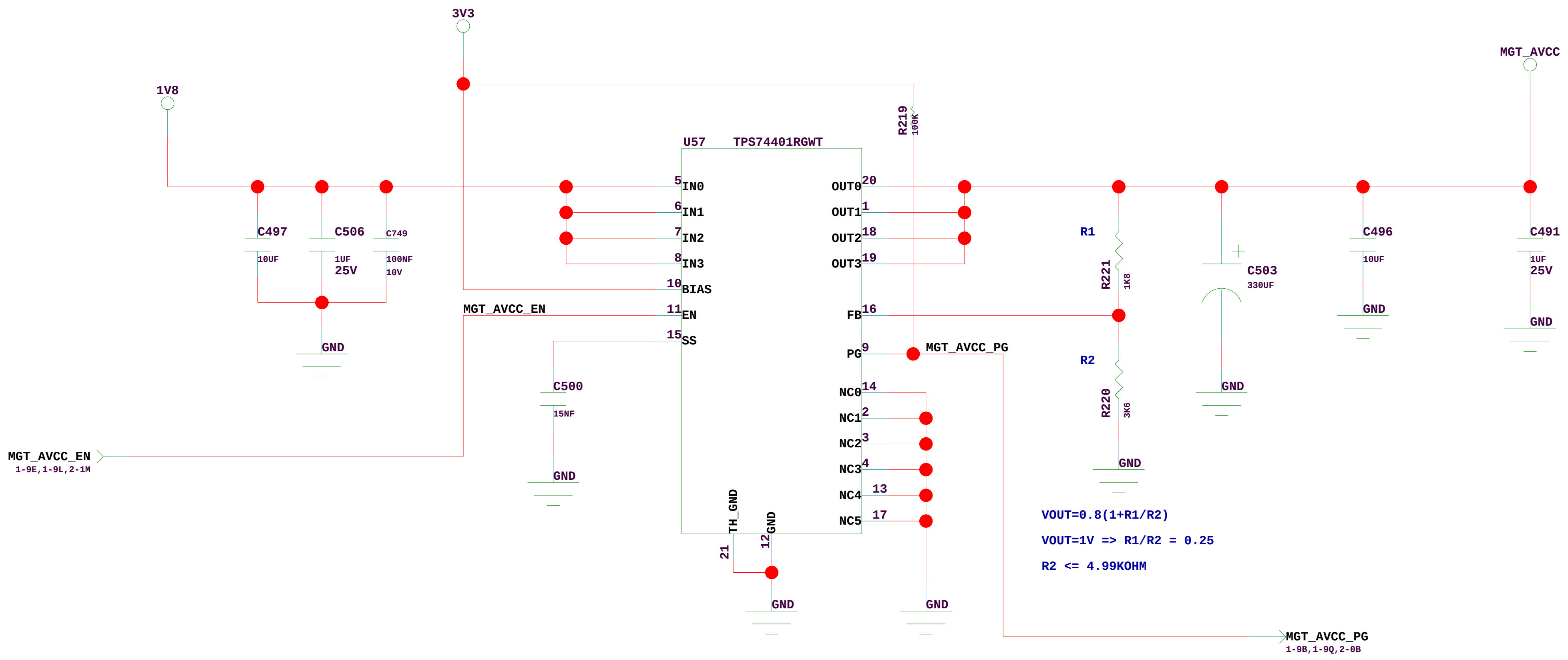
SHEET 9 OF 25


3V3
1V8
MGT_AVCCPLL
R213
100K
U55
TPS74401RGWT
5 IN0
6 IN1
7 IN2
8 IN3
10 BIAS
11 EN
15 SS
OUT0 20
OUT1 1
OUT2 18
OUT3 19
FB 16
PG 9
NC0 14
NC1 2
NC2 3
NC3 4
NC4 13
NC5 17
TH_GND 21
GND 12
C493
10UF
C505
1UF
25V
C748
100NF
10V
GND
MGT_AVCCPLL_EN
C498
15NF
GND
MGT_AVCCPLL_EN
1-9E,1-9L,2-1M
MGT_AVCCPLL_PG
R215
1K8
R214
3K6
C501
330UF
C492
10UF
C489
1UF
25V
GND
MGT_AVCCPLL_PG
1-8B,1-8Q,2-0B

VOUT=0.8(1+R1/R2)

VOUT=1.2V => R1/R2 = 0.5

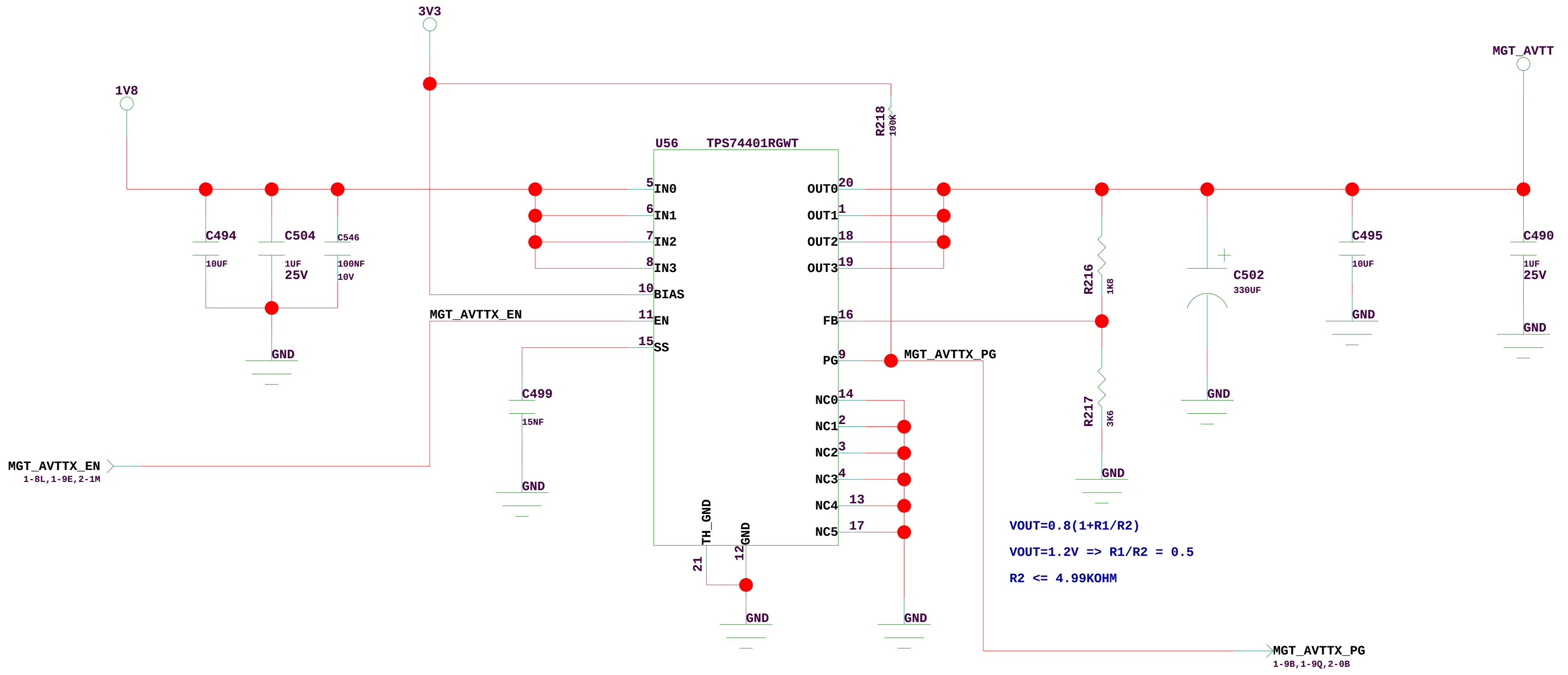
R2 <= 4.99KOHM


3V3
1V8
MGT_AVCC
R219
100K
U57
TPS74401RGWT
5 IN0
6 IN1
7 IN2
8 IN3
10 BIAS
11 EN
15 SS
OUT0 20
OUT1 1
OUT2 18
OUT3 19
FB 16
PG 9
NC0 14
NC1 2
NC2 3
NC3 4
NC4 13
NC5 17
TH_GND 21
GND 12
C497
10UF
C506
1UF
25V
C749
100NF
10V
GND
MGT_AVCC_EN
C500
15NF
GND
MGT_AVCC_EN
1-9E,1-9L,2-1M
MGT_AVCC_PG
R1
R221
1K8
R2
R220
3K6
C503
330UF
C496
10UF
C491
1UF
25V
GND
MGT_AVCC_PG
1-9B,1-9Q,2-0B

VOUT=0.8(1+R1/R2)

VOUT=1V => R1/R2 = 0.25

R2 <= 4.99KOHM


3V3
1V8
MGT_AVTT
R218
100K
U56
TPS74401RGWT
5 IN0
6 IN1
7 IN2
8 IN3
10 BIAS
11 EN
15 SS
OUT0 20
OUT1 1
OUT2 18
OUT3 19
FB 16
PG 9
NC0 14
NC1 2
NC2 3
NC3 4
NC4 13
NC5 17
TH_GND 21
GND 12
C494
10UF
C504
1UF
25V
C546
100NF
10V
GND
MGT_AVTTX_EN
C499
15NF
GND
MGT_AVTTX_EN
1-8L,1-9E,2-1M
MGT_AVTTX_PG
R216
1K8
R217
3K6
C502
330UF
C495
10UF
C490
1UF
25V
GND
MGT_AVTTX_PG
1-9B,1-9Q,2-0B

VOUT=0.8(1+R1/R2)

VOUT=1.2V => R1/R2 = 0.5

R2 <= 4.99KOHM

ROACH/iBOB2

ROACH_TRANSCEIVERS_PSU

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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DOC NO
NRF-ADM-XXX-SD-0001

REVISION
A

DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

10-17-2007_15:51

PATH PATH

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1V8
C363
C362
C361
220NF
6.3V
C388
C389
C390
C391
C392
C393
C394
C395
47UF
6V
GND
5V
U33
TPS51100DGQ
VIN
VLDOIN
VDDQSNS
S3
S5
VTT
VTTSNS
VTTREF
GND
PGND
R236
R235
10K
C467
C464
C460
C465
C466
VTT_0V9
VREF_0V9
VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
RP13
RP14
RP15
RP16
RP17
RP18
RP20
CP20
CP21
CP22
CP23
CP24
CP25
CP27
PLACE AT MODULE VREF PIN
C364
C352
PLACE AT MODULE VDDSPD PIN
C366
PLACE AT MODULE VDD PINS
C378
C379
C380
C377
C382
C383
C384
C381
C385
C386
C387
J15
879160001
VSS_64
VREF
VDDSPD
VDD_11
VDDQ_11
PLACE AT MODULE VDDQ PINS
C365
C367
C368
C369
C370
C371
C372
C373
C374
C375
C376
DDR2_A[15]
DDR2_BA[2]
DDR2_CS_N_0
DDR2_CAS_N
DDR2_RAS_N
DDR2_DQS_8
DDR2_DM[8]
DDR2_CK_2_P
DDR2_CKE_2
DDR2_ODT_1
DDR2_WE_N
DDR2_ERROR
DDR2_PHY_INIT_DONE
DDR2_RESET_N
TP6
DDR2_DQ[71]
DDR2_DIMM_CB7
DDR2_DIMM_SA2
DDR2_DIMM_SCL
DDR2_DIMM_SDA
ERR_OUT
PAR_IN
NC
BANKS=13, 17, 21, 25
U15
R140
R141
49.9R
C353
C354
C355
C356
C357
C358
C359
C360
10NF
25V
R233
R234
4K7
R231
R232

ROACH/iBOB2

COLLABORATORS:

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NRAO, SOCORRO
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PATH PATH

ROACH_DDR2_DIMM

DOC NO
NRF-ADM-XXX-SD-0001

REVISION
A

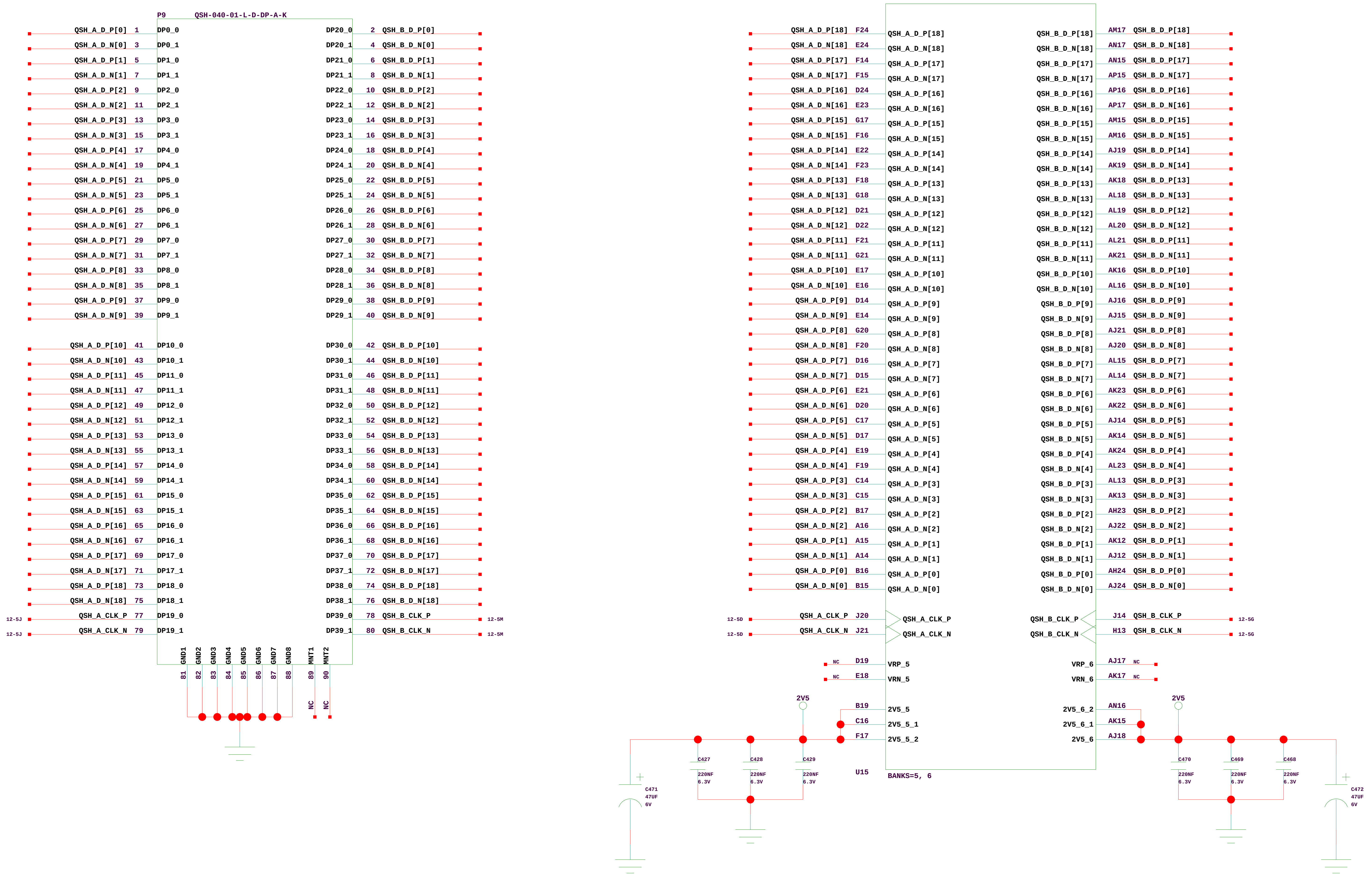
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 11 OF 25


P9 QSH-040-01-L-D-DP-A-K
QSH_A_D_P[0] 1 DP0_0
QSH_A_D_N[0] 3 DP0_1
QSH_A_D_P[1] 5 DP1_0
QSH_A_D_N[1] 7 DP1_1
QSH_A_D_P[2] 9 DP2_0
QSH_A_D_N[2] 11 DP2_1
QSH_A_D_P[3] 13 DP3_0
QSH_A_D_N[3] 15 DP3_1
QSH_A_D_P[4] 17 DP4_0
QSH_A_D_N[4] 19 DP4_1
QSH_A_D_P[5] 21 DP5_0
QSH_A_D_N[5] 23 DP5_1
QSH_A_D_P[6] 25 DP6_0
QSH_A_D_N[6] 27 DP6_1
QSH_A_D_P[7] 29 DP7_0
QSH_A_D_N[7] 31 DP7_1
QSH_A_D_P[8] 33 DP8_0
QSH_A_D_N[8] 35 DP8_1
QSH_A_D_P[9] 37 DP9_0
QSH_A_D_N[9] 39 DP9_1
QSH_A_D_P[10] 41 DP10_0
QSH_A_D_N[10] 43 DP10_1
QSH_A_D_P[11] 45 DP11_0
QSH_A_D_N[11] 47 DP11_1
QSH_A_D_P[12] 49 DP12_0
QSH_A_D_N[12] 51 DP12_1
QSH_A_D_P[13] 53 DP13_0
QSH_A_D_N[13] 55 DP13_1
QSH_A_D_P[14] 57 DP14_0
QSH_A_D_N[14] 59 DP14_1
QSH_A_D_P[15] 61 DP15_0
QSH_A_D_N[15] 63 DP15_1
QSH_A_D_P[16] 65 DP16_0
QSH_A_D_N[16] 67 DP16_1
QSH_A_D_P[17] 69 DP17_0
QSH_A_D_N[17] 71 DP17_1
QSH_A_D_P[18] 73 DP18_0
QSH_A_D_N[18] 75 DP18_1
12-5J QSH_A_CLK_P 77 DP19_0
12-5J QSH_A_CLK_N 79 DP19_1
DP20_0 2 QSH_B_D_P[0]
DP20_1 4 QSH_B_D_N[0]
DP21_0 6 QSH_B_D_P[1]
DP21_1 8 QSH_B_D_N[1]
DP22_0 10 QSH_B_D_P[2]
DP22_1 12 QSH_B_D_N[2]
DP23_0 14 QSH_B_D_P[3]
DP23_1 16 QSH_B_D_N[3]
DP24_0 18 QSH_B_D_P[4]
DP24_1 20 QSH_B_D_N[4]
DP25_0 22 QSH_B_D_P[5]
DP25_1 24 QSH_B_D_N[5]
DP26_0 26 QSH_B_D_P[6]
DP26_1 28 QSH_B_D_N[6]
DP27_0 30 QSH_B_D_P[7]
DP27_1 32 QSH_B_D_N[7]
DP28_0 34 QSH_B_D_P[8]
DP28_1 36 QSH_B_D_N[8]
DP29_0 38 QSH_B_D_P[9]
DP29_1 40 QSH_B_D_N[9]
DP30_0 42 QSH_B_D_P[10]
DP30_1 44 QSH_B_D_N[10]
DP31_0 46 QSH_B_D_P[11]
DP31_1 48 QSH_B_D_N[11]
DP32_0 50 QSH_B_D_P[12]
DP32_1 52 QSH_B_D_N[12]
DP33_0 54 QSH_B_D_P[13]
DP33_1 56 QSH_B_D_N[13]
DP34_0 58 QSH_B_D_P[14]
DP34_1 60 QSH_B_D_N[14]
DP35_0 62 QSH_B_D_P[15]
DP35_1 64 QSH_B_D_N[15]
DP36_0 66 QSH_B_D_P[16]
DP36_1 68 QSH_B_D_N[16]
DP37_0 70 QSH_B_D_P[17]
DP37_1 72 QSH_B_D_N[17]
DP38_0 74 QSH_B_D_P[18]
DP38_1 76 QSH_B_D_N[18]
DP39_0 78 QSH_B_CLK_P 12-5M
DP39_1 80 QSH_B_CLK_N 12-5M
GND1 81
GND2 82
GND3 83
GND4 84
GND5 85
GND6 86
GND7 87
GND8 88
MNT1 89 NC
MNT2 90 NC
QSH_A_D_P[18] F24 QSH_A_D_P[18]
QSH_A_D_N[18] E24 QSH_A_D_N[18]
QSH_A_D_P[17] F14 QSH_A_D_P[17]
QSH_A_D_N[17] F15 QSH_A_D_N[17]
QSH_A_D_P[16] D24 QSH_A_D_P[16]
QSH_A_D_N[16] E23 QSH_A_D_N[16]
QSH_A_D_P[15] G17 QSH_A_D_P[15]
QSH_A_D_N[15] F16 QSH_A_D_N[15]
QSH_A_D_P[14] E22 QSH_A_D_P[14]
QSH_A_D_N[14] F23 QSH_A_D_N[14]
QSH_A_D_P[13] F18 QSH_A_D_P[13]
QSH_A_D_N[13] G18 QSH_A_D_N[13]
QSH_A_D_P[12] D21 QSH_A_D_P[12]
QSH_A_D_N[12] D22 QSH_A_D_N[12]
QSH_A_D_P[11] F21 QSH_A_D_P[11]
QSH_A_D_N[11] G21 QSH_A_D_N[11]
QSH_A_D_P[10] E17 QSH_A_D_P[10]
QSH_A_D_N[10] E16 QSH_A_D_N[10]
QSH_A_D_P[9] D14 QSH_A_D_P[9]
QSH_A_D_N[9] E14 QSH_A_D_N[9]
QSH_A_D_P[8] G20 QSH_A_D_P[8]
QSH_A_D_N[8] F20 QSH_A_D_N[8]
QSH_A_D_P[7] D16 QSH_A_D_P[7]
QSH_A_D_N[7] D15 QSH_A_D_N[7]
QSH_A_D_P[6] E21 QSH_A_D_P[6]
QSH_A_D_N[6] D20 QSH_A_D_N[6]
QSH_A_D_P[5] C17 QSH_A_D_P[5]
QSH_A_D_N[5] D17 QSH_A_D_N[5]
QSH_A_D_P[4] E19 QSH_A_D_P[4]
QSH_A_D_N[4] F19 QSH_A_D_N[4]
QSH_A_D_P[3] C14 QSH_A_D_P[3]
QSH_A_D_N[3] C15 QSH_A_D_N[3]
QSH_A_D_P[2] B17 QSH_A_D_P[2]
QSH_A_D_N[2] A16 QSH_A_D_N[2]
QSH_A_D_P[1] A15 QSH_A_D_P[1]
QSH_A_D_N[1] A14 QSH_A_D_N[1]
QSH_A_D_P[0] B16 QSH_A_D_P[0]
QSH_A_D_N[0] B15 QSH_A_D_N[0]
12-5D QSH_A_CLK_P J20 QSH_A_CLK_P
12-5D QSH_A_CLK_N J21 QSH_A_CLK_N
NC D19 VRP_5
NC E18 VRN_5
2V5
B19 2V5_5
C16 2V5_5_1
F17 2V5_5_2
C427 220NF 6.3V
C428 220NF 6.3V
C429 220NF 6.3V
C471 47UF 6V
U15
BANKS=5, 6
QSH_B_D_P[18] AM17 QSH_B_D_P[18]
QSH_B_D_N[18] AN17 QSH_B_D_N[18]
QSH_B_D_P[17] AN15 QSH_B_D_P[17]
QSH_B_D_N[17] AP15 QSH_B_D_N[17]
QSH_B_D_P[16] AP16 QSH_B_D_P[16]
QSH_B_D_N[16] AP17 QSH_B_D_N[16]
QSH_B_D_P[15] AM15 QSH_B_D_P[15]
QSH_B_D_N[15] AM16 QSH_B_D_N[15]
QSH_B_D_P[14] AJ19 QSH_B_D_P[14]
QSH_B_D_N[14] AK19 QSH_B_D_N[14]
QSH_B_D_P[13] AK18 QSH_B_D_P[13]
QSH_B_D_N[13] AL18 QSH_B_D_N[13]
QSH_B_D_P[12] AL19 QSH_B_D_P[12]
QSH_B_D_N[12] AL20 QSH_B_D_N[12]
QSH_B_D_P[11] AL21 QSH_B_D_P[11]
QSH_B_D_N[11] AK21 QSH_B_D_N[11]
QSH_B_D_P[10] AK16 QSH_B_D_P[10]
QSH_B_D_N[10] AL16 QSH_B_D_N[10]
QSH_B_D_P[9] AJ16 QSH_B_D_P[9]
QSH_B_D_N[9] AJ15 QSH_B_D_N[9]
QSH_B_D_P[8] AJ21 QSH_B_D_P[8]
QSH_B_D_N[8] AJ20 QSH_B_D_N[8]
QSH_B_D_P[7] AL15 QSH_B_D_P[7]
QSH_B_D_N[7] AL14 QSH_B_D_N[7]
QSH_B_D_P[6] AK23 QSH_B_D_P[6]
QSH_B_D_N[6] AK22 QSH_B_D_N[6]
QSH_B_D_P[5] AJ14 QSH_B_D_P[5]
QSH_B_D_N[5] AK14 QSH_B_D_N[5]
QSH_B_D_P[4] AK24 QSH_B_D_P[4]
QSH_B_D_N[4] AL23 QSH_B_D_N[4]
QSH_B_D_P[3] AL13 QSH_B_D_P[3]
QSH_B_D_N[3] AK13 QSH_B_D_N[3]
QSH_B_D_P[2] AH23 QSH_B_D_P[2]
QSH_B_D_N[2] AJ22 QSH_B_D_N[2]
QSH_B_D_P[1] AK12 QSH_B_D_P[1]
QSH_B_D_N[1] AJ12 QSH_B_D_N[1]
QSH_B_D_P[0] AH24 QSH_B_D_P[0]
QSH_B_D_N[0] AJ24 QSH_B_D_N[0]
QSH_B_CLK_P J14 QSH_B_CLK_P 12-5G
QSH_B_CLK_N H13 QSH_B_CLK_N 12-5G
VRP_6 AJ17 NC
VRN_6 AK17 NC
2V5_6_2 AN16
2V5_6_1 AK15
2V5_6 AJ18
2V5
C470 220NF 6.3V
C469 220NF 6.3V
C468 220NF 6.3V
C472 47UF 6V

ROACH/iBOB2	**ROACH_DIFF_GPIO**	
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO NRF-ADM-XXX-SD-0001	REVISION A
	DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW	
10-17-2007_15:51	DRAWN: F KAPP	APPR:
PATH PATH	CHECKED: E BAUERMEISTER	SHEET 12 OF 25

GPIOLVC18[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH
GPIOLVC18[20] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH
IO VOLTAGE LEVEL SELECT
1-2: 3.3V
2-3: 2.5V
GPIOLVC18[4] IS DUAL FUNCTION:
1. DRIVES LED
2. CONTROLS DIRECTION ON GPIOLVC33[1-4]
IF CR10 IS ON, CLOCK CAPABLE GPIO'S ARE OUTPUTS
CLOCK CAPABLE
U13
U14
U10
U11
U12
U15
74AVCH4T245DGVRE4
1DIR
2DIR
1OE#
2OE#
1A1
1A2
2A1
2A2
1B1
1B2
2B1
2B2
GND1
GND2
VCCA
VCCB
GPIOLVC33[4] K12
GPIOLVC33[3] K13
GPIOLVC33[2] H23
GPIOLVC33[1] G23
GPIOLVC15[3] B20
GPIOLVC15[2] C20
GPIOLVC15[1] F29
GPIOLVC15[0] E29
GPIOLVC18[20] AM20
GPIOLVC18[19] AP24
GPIOLVC18[18] AN24
GPIOLVC18[17] AL24
GPIOLVC18[16] AP25
GPIOLVC18[15] AD25
GPIOLVC18[14] AG25
GPIOLVC18[13] AH25
GPIOLVC18[12] AJ25
GPIOLVC18[11] AJ26
GPIOLVC18[10] AK27
GPIOLVC18[7] AC29
GPIOLVC18[4] AA30
J2
J9
N2520-6V0C-RB-WE
J10
J11
TBD
JP1
JP2
R1 10K
R2 10K
R7 10K
R8 10K
R9 10K
R47 10K
R48 10K
R49 499R
R50 499R
R43 100R
R44 100R
R45 100R
R46 100R
CR7
CR8
CR9
CR10
C34
C35
C36
C37
C38
C39
C40
C41
C42
C43
C44
C45
220NF
6.3V
3V3
2V5
1V8
1V5
GND

ROACH/iBOB2

COLLABORATORS:

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NRAO, SOCORRO
meerKAT, CAPE TOWN

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10-17-2007_15:51

PATH PATH

ROACH_GPIO_MISC

DOC NO
NRF-ADM-XXX-SD-0001

REVISION
A

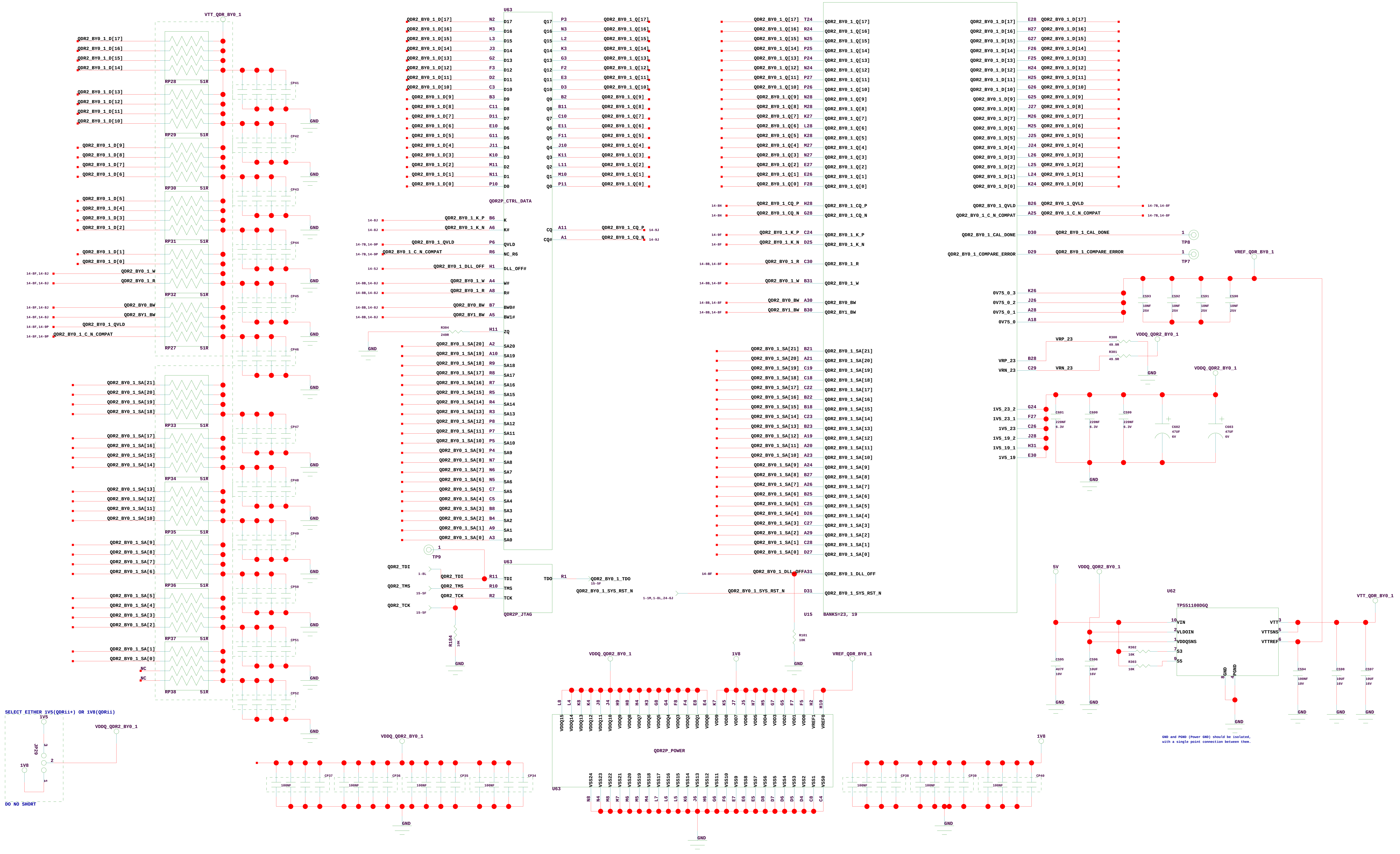
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 13 OF 25


VTT_QDR_BY0_1
QDR2_BY0_1_D[17]
QDR2_BY0_1_D[16]
QDR2_BY0_1_D[15]
QDR2_BY0_1_D[14]
RP28 51R
QDR2_BY0_1_D[13]
QDR2_BY0_1_D[12]
QDR2_BY0_1_D[11]
QDR2_BY0_1_D[10]
RP29 51R
QDR2_BY0_1_D[9]
QDR2_BY0_1_D[8]
QDR2_BY0_1_D[7]
QDR2_BY0_1_D[6]
RP30 51R
QDR2_BY0_1_D[5]
QDR2_BY0_1_D[4]
QDR2_BY0_1_D[3]
QDR2_BY0_1_D[2]
RP31 51R
QDR2_BY0_1_D[1]
QDR2_BY0_1_D[0]
QDR2_BY0_1_W
QDR2_BY0_1_R
RP32 51R
QDR2_BY0_BW
QDR2_BY1_BW
QDR2_BY0_1_QVLD
QDR2_BY0_1_C_N_COMPAT
RP27 51R
QDR2_BY0_1_SA[21]
QDR2_BY0_1_SA[20]
QDR2_BY0_1_SA[19]
QDR2_BY0_1_SA[18]
RP33 51R
QDR2_BY0_1_SA[17]
QDR2_BY0_1_SA[16]
QDR2_BY0_1_SA[15]
QDR2_BY0_1_SA[14]
RP34 51R
QDR2_BY0_1_SA[13]
QDR2_BY0_1_SA[12]
QDR2_BY0_1_SA[11]
QDR2_BY0_1_SA[10]
RP35 51R
QDR2_BY0_1_SA[9]
QDR2_BY0_1_SA[8]
QDR2_BY0_1_SA[7]
QDR2_BY0_1_SA[6]
RP36 51R
QDR2_BY0_1_SA[5]
QDR2_BY0_1_SA[4]
QDR2_BY0_1_SA[3]
QDR2_BY0_1_SA[2]
RP37 51R
QDR2_BY0_1_SA[1]
QDR2_BY0_1_SA[0]
NC
NC
RP38 51R
CP41
CP42
CP43
CP44
CP45
CP46
CP47
CP48
CP49
CP50
CP51
CP52
GND
SELECT EITHER 1V5(QDRii+) OR 1V8(QDRii)
1V5
1V8
JP29
VDDQ_QDR2_BY0_1
DO NO SHORT
U63
QDR2P_CTRL_DATA
QDR2P_JTAG
QDR2P_POWER
K
K#
QVLD
NC_R6
DLL_OFF#
W#
R#
BW0#
BW1#
ZQ
CQ
CQ#
QDR2_BY0_1_K_P
QDR2_BY0_1_K_N
QDR2_BY0_1_DLL_OFF
QDR2_BY0_1_CQ_P
QDR2_BY0_1_CQ_N
R304
249R
TP9
QDR2_TDI
QDR2_TMS
QDR2_TCK
TDI
TMS
TCK
TDO
QDR2_BY0_1_TDO
R184
10K
QDR2_BY0_1_SYS_RST_N
U15
BANKS=23, 19
QDR2_BY0_1_CAL_DONE
QDR2_BY0_1_COMPARE_ERROR
TP8
TP7
VREF_QDR_BY0_1
0V75_0_3
0V75_0_2
0V75_0_1
0V75_0
C593 C592 C591 C590
10NF 25V
VRP_23
VRN_23
R300 49.9R
R301 49.9R
1V5_23_2
1V5_23_1
1V5_23
1V5_19_2
1V5_19_1
1V5_19
C601 C600 C599
220NF 6.3V
C602 47UF 6V
C603 47UF 6V
R101 10K
U62
TPS51100DGQ
VIN
VLDOIN
VDDQSNS
S3
S5
VTT
VTTSNS
VTTREF
GND
PGND
5V
R302 10K
R303 10K
C595 4U7F 10V
C596 10UF 16V
C594 100NF 10V
C598 10UF 16V
C597 10UF 16V
GND and PGND (Power GND) should be isolated, with a single point connection between them.
CP37 CP36 CP35 CP34
CP38 CP39 CP40
100NF

ROACH/iBOB2

COLLABORATORS:

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PATH PATH

ROACH_QDR2P_BY0_1

DOC NO
NRF-ADM-XXX-SD-0001

REVISION
A

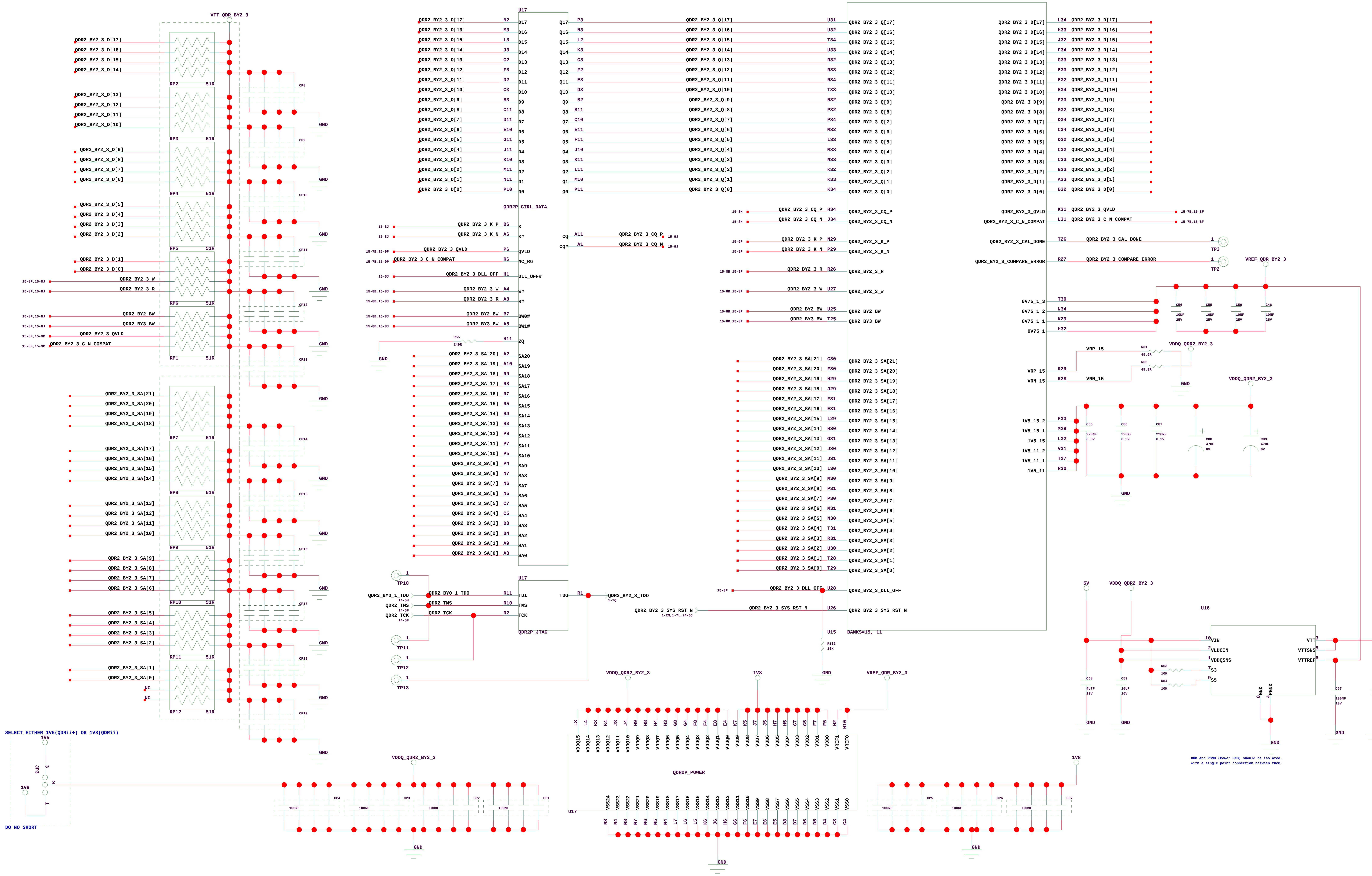
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 14 OF 25


VTT_QDR_BY2_3
RP1 51R
RP2 51R
RP3 51R
RP4 51R
RP5 51R
RP6 51R
RP7 51R
RP8 51R
RP9 51R
RP10 51R
RP11 51R
RP12 51R
CP1
CP2
CP3
CP4
CP5
CP6
CP7
CP8
CP9
CP10
CP11
CP12
CP13
CP14
CP15
CP16
CP17
CP18
CP19
GND
NC
U17
QDR2P_CTRL_DATA
QDR2P_JTAG
QDR2P_POWER
BANKS=15, 11
QDR2_BY2_3_D[17]
QDR2_BY2_3_D[0]
QDR2_BY2_3_Q[17]
QDR2_BY2_3_Q[0]
QDR2_BY2_3_SA[21]
QDR2_BY2_3_SA[0]
QDR2_BY2_3_K_P
QDR2_BY2_3_K_N
QDR2_BY2_3_CQ_P
QDR2_BY2_3_CQ_N
QDR2_BY2_3_QVLD
QDR2_BY2_3_C_N_COMPAT
QDR2_BY2_3_DLL_OFF
QDR2_BY2_3_W
QDR2_BY2_3_R
QDR2_BY2_BW
QDR2_BY3_BW
QDR2_BY2_3_CAL_DONE
QDR2_BY2_3_COMPARE_ERROR
QDR2_BY2_3_SYS_RST_N
QDR2_BY0_1_TDO
QDR2_TMS
QDR2_TCK
QDR2_BY2_3_TDO
R55 249R
R1
R51 49.9R
R52 49.9R
R102 10K
U15
TP2
TP3
TP10
TP11
TP12
TP13
VRP_15
VRN_15
VREF_QDR_BY2_3
VDDQ_QDR2_BY2_3
1V8
1V5
5V
C45 C50 C55 C56 10NF 25V
C85 C86 C87 220NF 6.3V
C88 C89 47UF 6V
SELECT EITHER 1V5(QDRii+) OR 1V8(QDRii)
JP3
DO NO SHORT
U16
VIN
VLDOIN
VDDQSNS
S3
S5
VTT
VTTSNS
VTTREF
GND
PGND
R53 10K
R54 10K
C58 4U7F 10V
C59 10UF 16V
C57 100NF 10V
C84 10UF 16V
C60 10UF 16V
100NF
GND and PGND (Power GND) should be isolated,
with a single point connection between them.

ROACH/iBOB2

COLLABORATORS:

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PATH PATH

ROACH_QDR2P_BY2_3

DOC NO NRF-ADM-XXX-SD-0001

REVISION A

DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

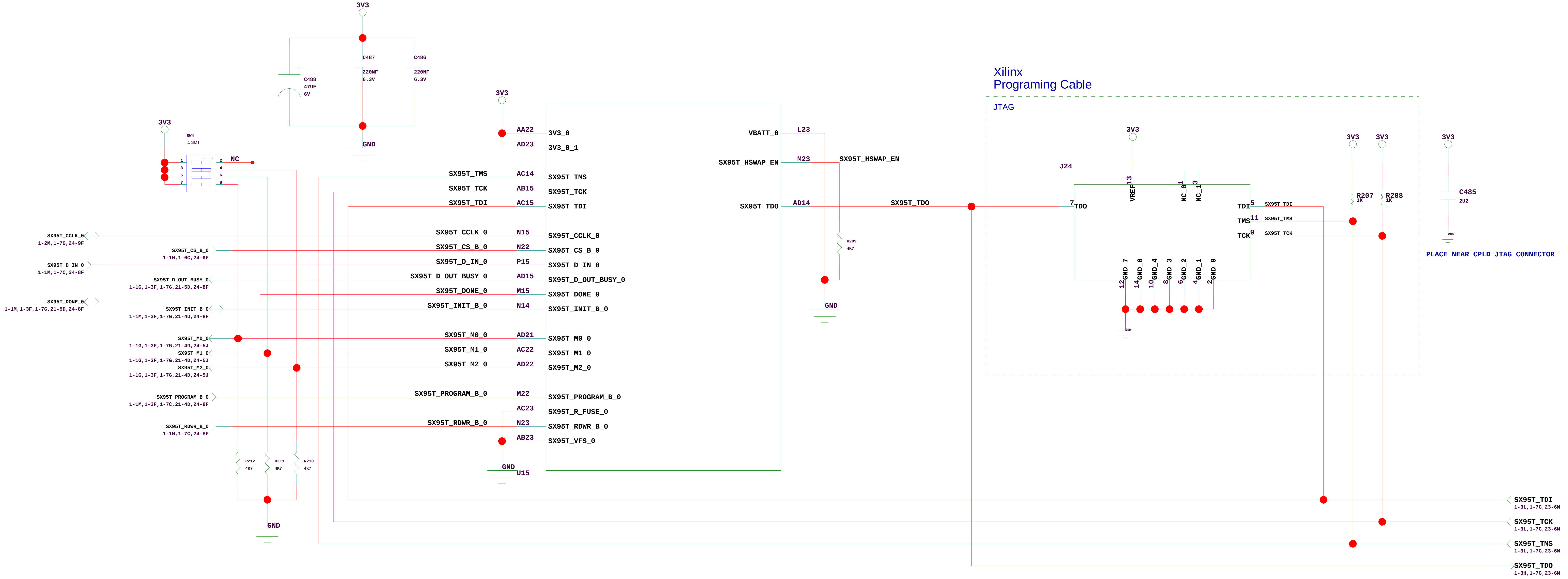
CHECKED: E BAUERMEISTER

SHEET 15 OF 25

TBD

VALID CONFIGURATION MODES

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input


3V3
C488
47UF
6V
C487
220NF
6.3V
C486
220NF
6.3V
GND
SW4
.1 SMT
1
2
3
4
5
6
7
8
NC
SX95T_CCLK_0
1-2M,1-7G,24-9F
SX95T_CS_B_0
1-1M,1-6C,24-9F
SX95T_D_IN_0
1-1M,1-7C,24-8F
SX95T_D_OUT_BUSY_0
1-1G,1-3F,1-7G,21-5D,24-8F
SX95T_DONE_0
1-1M,1-3F,1-7G,21-5D,24-8F
SX95T_INIT_B_0
1-1M,1-3F,1-7G,21-4D,24-8F
SX95T_M0_0
1-1G,1-3F,1-7G,21-4D,24-5J
SX95T_M1_0
1-1G,1-3F,1-7G,21-4D,24-5J
SX95T_M2_0
1-1G,1-3F,1-7G,21-4D,24-5J
SX95T_PROGRAM_B_0
1-1M,1-3F,1-7C,21-4D,24-8F
SX95T_RDWR_B_0
1-1M,1-7C,24-8F
R212
4K7
R211
4K7
R210
4K7
GND
AA22
AD23
AC14
AB15
AC15
N15
N22
P15
AD15
M15
N14
AD21
AC22
AD22
M22
AC23
N23
AB23
SX95T_TMS
SX95T_TCK
SX95T_TDI
SX95T_CCLK_0
SX95T_CS_B_0
SX95T_D_IN_0
SX95T_D_OUT_BUSY_0
SX95T_DONE_0
SX95T_INIT_B_0
SX95T_M0_0
SX95T_M1_0
SX95T_M2_0
SX95T_PROGRAM_B_0
SX95T_RDWR_B_0
3V3_0
3V3_0_1
SX95T_R_FUSE_0
SX95T_VFS_0
GND
U15
VBATT_0
L23
SX95T_HSWAP_EN
M23
SX95T_HSWAP_EN
SX95T_TDO
AD14
SX95T_TDO
R209
4K7
GND
Xilinx
Programing Cable
JTAG
J24
3V3
13
VREF
1
NC_0
3
NC_1
7
TDO
TDI
5
TMS
11
TCK
9
SX95T_TDI
SX95T_TMS
SX95T_TCK
12
GND_7
14
GND_6
10
GND_4
8
GND_3
6
GND_2
4
GND_1
2
GND_0
GND
3V3
3V3
R207
1K
R208
1K
3V3
C485
2U2
GND
PLACE NEAR CPLD JTAG CONNECTOR
SX95T_TDI
1-3L,1-7C,23-6N
SX95T_TCK
1-3L,1-7C,23-6M
SX95T_TMS
1-3L,1-7C,23-6N
SX95T_TDO
1-3H,1-7C,23-6M

ROACH/iBOB2

ROACH_CONFIG

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

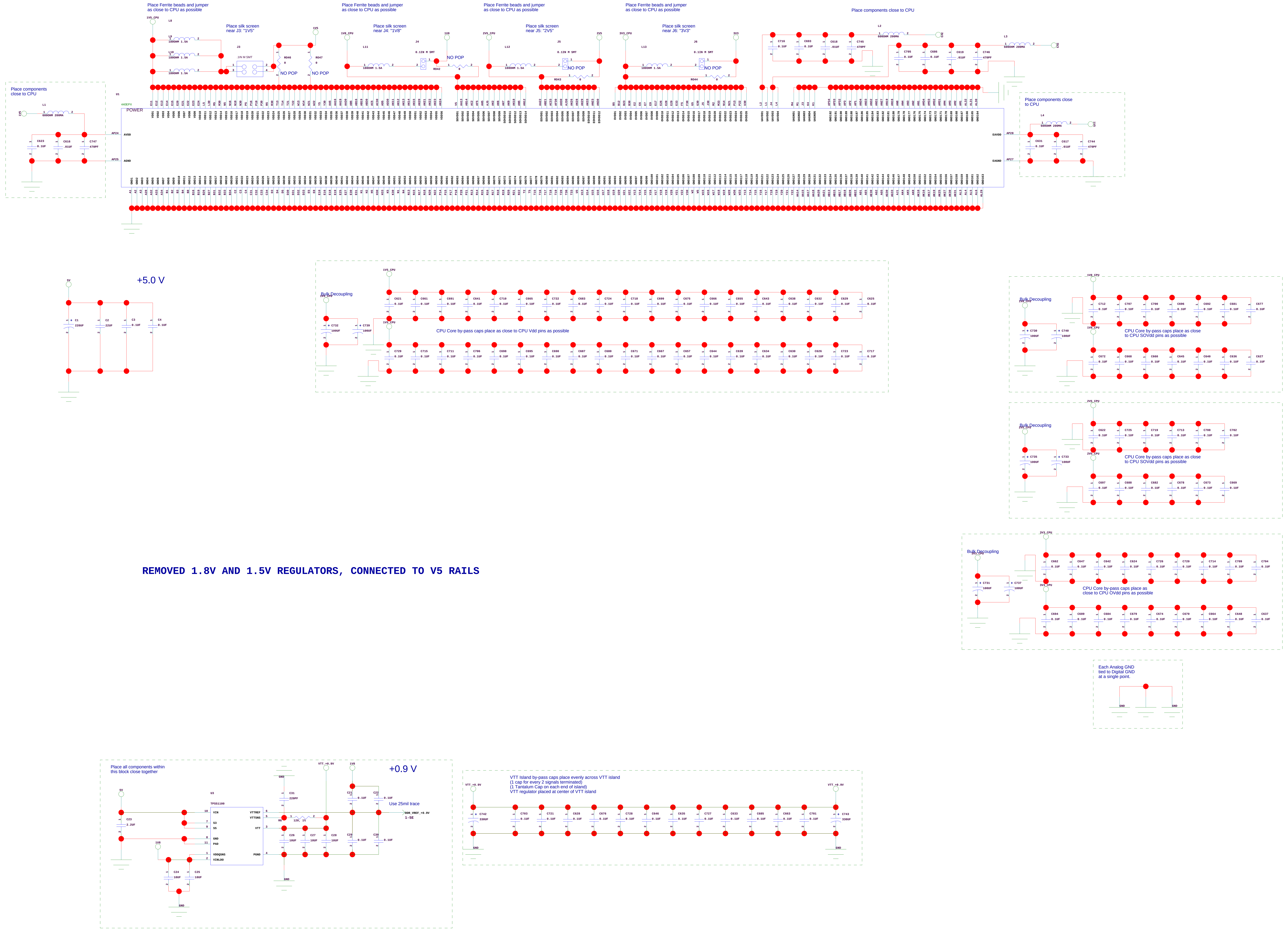
APPR:

CHECKED: E BAUERMEISTER

10-17-2007_15:51

PATH PATH

SHEET 16 OF 25


Place Ferrite beads and jumper as close to CPU as possible
Place silk screen near J3: "1V5"
Place silk screen near J4: "1V8"
Place silk screen near J5: "2V5"
Place silk screen near J6: "3V3"
NO POP
Place components close to CPU
Place components close to CPU
POWER
AVDD
AGND
SAVDD
SAGND
+5.0 V
Bulk Decoupling
CPU Core by-pass caps place as close to CPU Vdd pins as possible
CPU Core by-pass caps place as close to CPU SOVdd pins as possible
CPU Core by-pass caps place as close to CPU OVdd pins as possible
REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS
Each Analog GND tied to Digital GND at a single point.
Place all components within this block close together
TPS51100
+0.9 V
Use 25mil trace
DDR_VREF_+0.9V
VTT Island by-pass caps place evenly across VTT island
(1 cap for every 2 signals terminated)
(1 Tantalum Cap on each end of island)
VTT regulator placed at center of VTT island

ROACH/iBOB2

COLLABORATORS:

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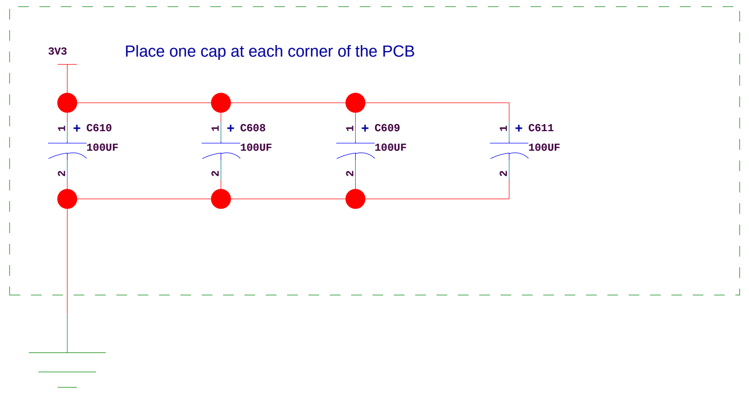
PATH PATH

ROACH_PPC_POWER_1

DOC NO NRF-ADM-XXX-SD-0001	REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 17 OF 25

REMOVED 3V3 GENERATION



Place one cap at each corner of the PCB

REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2

COLLABORATORS:

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PATH PATH

ROACH_PPC_POWER_2

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

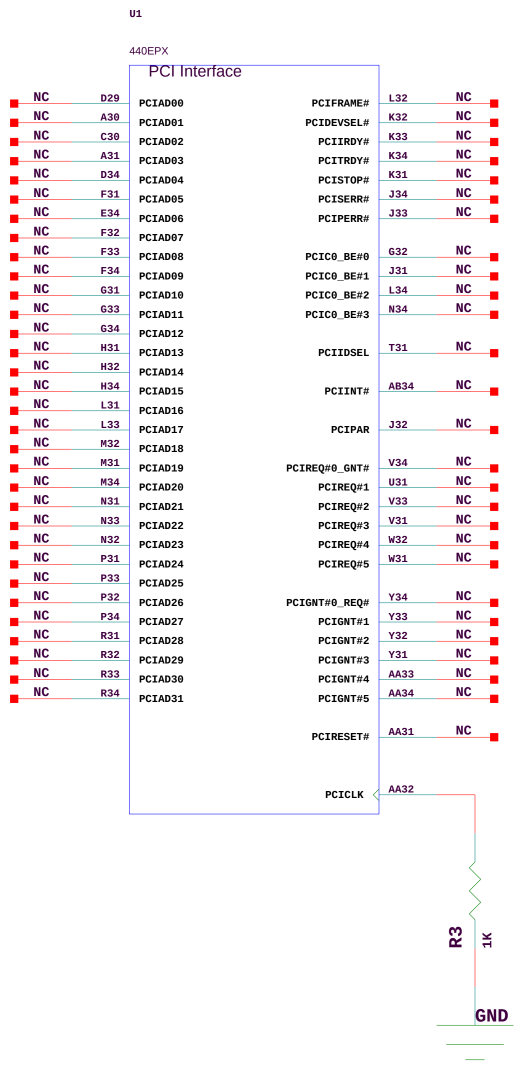
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 18 OF 25


U1
440EPX
PCI Interface
NC D29 PCIAD00
NC A30 PCIAD01
NC C30 PCIAD02
NC A31 PCIAD03
NC D34 PCIAD04
NC F31 PCIAD05
NC E34 PCIAD06
NC F32 PCIAD07
NC F33 PCIAD08
NC F34 PCIAD09
NC G31 PCIAD10
NC G33 PCIAD11
NC G34 PCIAD12
NC H31 PCIAD13
NC H32 PCIAD14
NC H34 PCIAD15
NC L31 PCIAD16
NC L33 PCIAD17
NC M32 PCIAD18
NC M31 PCIAD19
NC M34 PCIAD20
NC N31 PCIAD21
NC N33 PCIAD22
NC N32 PCIAD23
NC P31 PCIAD24
NC P33 PCIAD25
NC P32 PCIAD26
NC P34 PCIAD27
NC R31 PCIAD28
NC R32 PCIAD29
NC R33 PCIAD30
NC R34 PCIAD31
PCIFRAME# L32 NC
PCIDEVSEL# K32 NC
PCIIRDY# K33 NC
PCITRDY# K34 NC
PCISTOP# K31 NC
PCISERR# J34 NC
PCIPERR# J33 NC
PCIC0_BE#0 G32 NC
PCIC0_BE#1 J31 NC
PCIC0_BE#2 L34 NC
PCIC0_BE#3 N34 NC
PCIIDSEL T31 NC
PCIINT# AB34 NC
PCIPAR J32 NC
PCIREQ#0_GNT# V34 NC
PCIREQ#1 U31 NC
PCIREQ#2 V33 NC
PCIREQ#3 V31 NC
PCIREQ#4 W32 NC
PCIREQ#5 W31 NC
PCIGNT#0_REQ# Y34 NC
PCIGNT#1 Y33 NC
PCIGNT#2 Y32 NC
PCIGNT#3 Y31 NC
PCIGNT#4 AA33 NC
PCIGNT#5 AA34 NC
PCIRESET# AA31 NC
PCICLK AA32
R3
1K
GND

PCI BUS NOT IMPLEMENTED

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

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10-17-2007_15:51

PATH PATH

ROACH_PPC_PCI

DOC NO
NRF-ADM-XXX-SD-0001

REVISION
A

DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

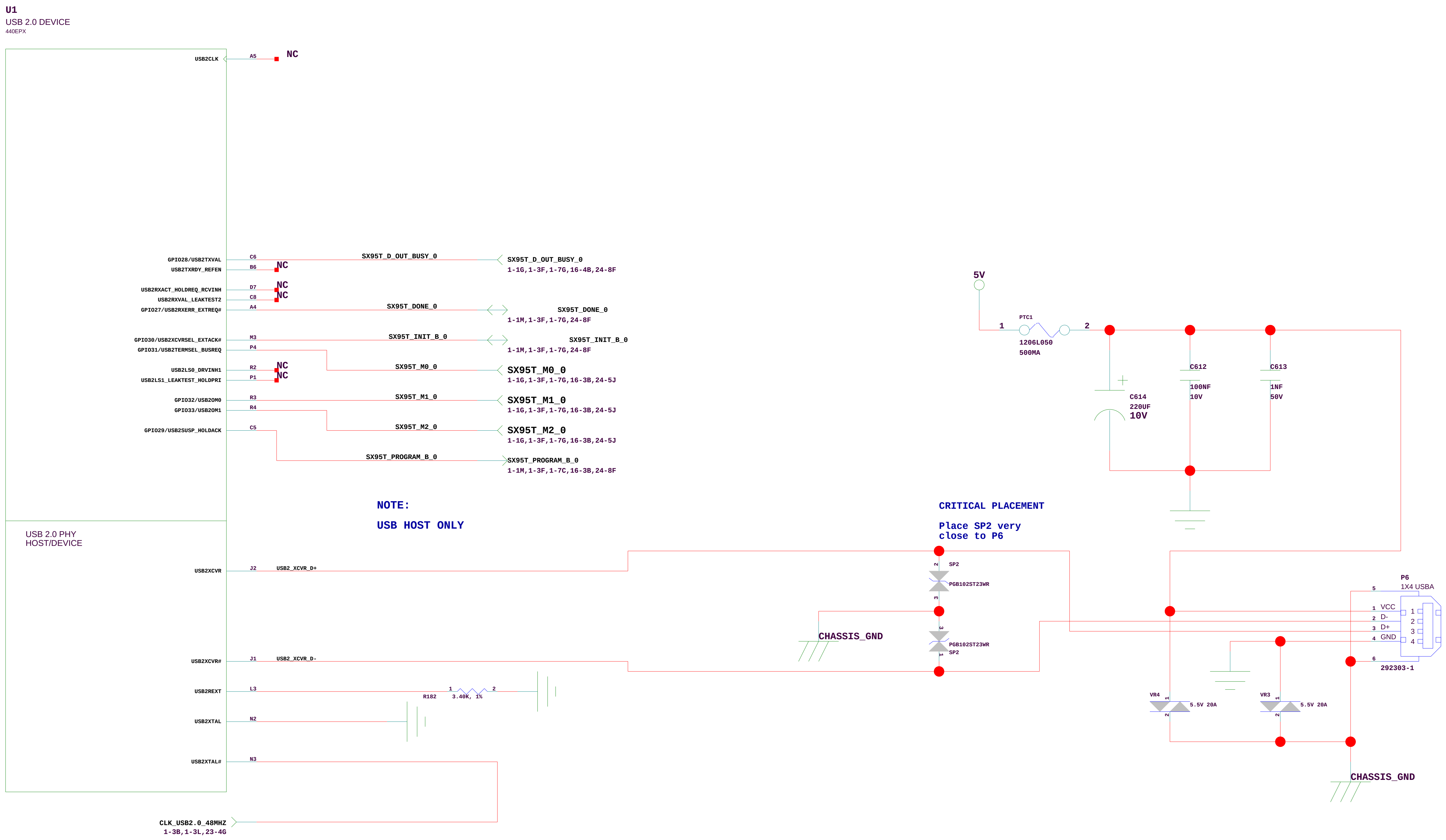
APPR:

CHECKED: E BAUERMEISTER

SHEET 19 OF 25

UNUSED SECOND ETHERNET MAC
Gig-Ethernet RGMII1
U1 440EPX
Gig-Ethernet RGMII0
ETHERNET Mgt.
GMC0_TXD0
GMC0_TXD1
GMC0_TXD2
GMC0_TXD3
GMC0_TXCTL
GMC0_TXCLK
GMCTXCLK
GMC0_RXD0
GMC0_RXD1
GMC0_RXD2
GMC0_RXD3
GMC0_RXCTL
GMC0_RXCLK
REJECTPKT0
REJECTPKT1
GMCMDCLK
GMCMDIO
GMCREFCLK
GMCREFCLK_125MHZ
The RGMII signaling is 125 MHz using both rising and falling edges of the clock.
The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.
Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.
CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30
Place resistors as close to CPU as possible and keep all traces lengths equal
Place resistors close to PHY all trace lengths equal
Place jumers in line with signals
Place nearest PHY pin 98
Place nearest PHY pin 100
Place nearest PHY pin 96
Place nearest PHY pin 101
Place as close to PHY CORE VDD power pins as possible
Place as close to PHY IO VDD power pins as possible
Place components as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible.
Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5
Ethernet LEDs
Top LED = SPEED/LINK
Green = 1000
Off = 10/100
Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY
U58
DP83865DVH
TXD0/TX0
TXD1/TX1
TXD2/TX2
TXD3/TX3
TX_EN/TXEN_ER
TX_ER
TX_CLK/RGMII_SEL1
GTX_CLK/TCK
CRS/RGMII_SEL0
COL
RXD0/RX0
RXD1/RX1
RXD2/RX2
RXD3/RX3
RX_DV/RCK
RX_ER/RXDV_ER
RX_CLK
MDC
MDIO
CLK_TO_MAC
RESET#
INTERRUPT#
CLK_IN
CLK_OUT
TDO
TDI
TCK
TMS
TRST#
MDIA_P
MDIA_N
MDIB_P
MDIB_N
MDIC_P
MDIC_N
MDID_P
MDID_N
VDD_SEL_STRAP
MAC_CLK_EN_STRAP
MDIX_EN_STRAP
MULTI_EN_STRAP
LINK1000_LED/AN_EN_STRAP
LINK100_LED/DUPLEX_STRAP
LINK10_LED/RLED/SPEED1_STRAP
ACTIVITY_LED/SPEED0_STRAP
DUPLEX_LED/PHYADDR0_STRAP
PHYADDR1_STRAP
PHYADDR2_STRAP
PHYADDR3_STRAP
PHYADDR4_STRAP
BG_REF
TX_TCLK
NON_IEEE_STRAP
RESERVED1
RESERVED2
RESERVED
GETH0_RST#
1-2M,1-4B,24-5C
GETH0_INT#
1-3H,1-4E,23-7N
CLK_GETH0_25MHZ
1-3L,1-4B,23-5G
1-4E,20-3C
1-4E,20-4D
MDI0_0P
MDI0_0N
MDI0_1P
MDI0_1N
MDI0_2P
MDI0_2N
MDI0_3P
MDI0_3N
LED0_L1000
LED0_L100
LED0_L10
LED0_ACT
LED0_DUPLEX
J25
HFJ11-1G02E-L12
CHASSIS_GND
NOSTUFF
NC
1V8
2V5
STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL
DUPLEX LED
L10 LED
L100 LED
JP10
JP11
JP12
JP13
JP14
JP15
JP16
JP17
JP18
JP19
JP20
JP21
JP22
JP23
JP24
JP25

ROACH/iBOB2	**ROACH_PPC_ETH1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-17-2007_15:51	DRAWN: F KAPP APPR:
PATH PATH	CHECKED: E BAUERMEISTER SHEET 20 OF 25


U1
USB 2.0 DEVICE
440EPX
USB2CLK
A5
NC
GPIO28/USB2TXVAL
C6
SX95T_D_OUT_BUSY_0
SX95T_D_OUT_BUSY_0
1-1G,1-3F,1-7G,16-4B,24-8F
USB2TXRDY_REFEN
B6
NC
USB2RXACT_HOLDREQ_RCVINH
D7
NC
USB2RXVAL_LEAKTEST2
C8
NC
GPIO27/USB2RXERR_EXTREQ#
A4
SX95T_DONE_0
SX95T_DONE_0
1-1M,1-3F,1-7G,24-8F
GPIO30/USB2XCVRSEL_EXTACK#
M3
SX95T_INIT_B_0
SX95T_INIT_B_0
1-1M,1-3F,1-7G,24-8F
GPIO31/USB2TERMSEL_BUSREQ
P4
SX95T_M0_0
SX95T_M0_0
1-1G,1-3F,1-7G,16-3B,24-5J
USB2LS0_DRVINH1
R2
NC
USB2LS1_LEAKTEST_HOLDPRI
P1
NC
GPIO32/USB2OM0
R3
SX95T_M1_0
SX95T_M1_0
1-1G,1-3F,1-7G,16-3B,24-5J
GPIO33/USB2OM1
R4
SX95T_M2_0
SX95T_M2_0
1-1G,1-3F,1-7G,16-3B,24-5J
GPIO29/USB2SUSP_HOLDACK
C5
SX95T_PROGRAM_B_0
SX95T_PROGRAM_B_0
1-1M,1-3F,1-7C,16-3B,24-8F
USB 2.0 PHY
HOST/DEVICE
USB2XCVR
J2
USB2_XCVR_D+
USB2XCVR#
J1
USB2_XCVR_D-
USB2REXT
L3
1
2
R182
3.40K, 1%
USB2XTAL
N2
USB2XTAL#
N3
CLK_USB2.0_48MHZ
1-3B,1-3L,23-4G
5V
PTC1
1
2
1206L050
500MA
C614
220UF
10V
C612
100NF
10V
C613
1NF
50V
SP2
2
3
PGB102ST23WR
3
1
PGB102ST23WR
SP2
CHASSIS_GND
P6
1X4 USBA
5
1 VCC
2 D-
3 D+
4 GND
1
2
3
4
6
292303-1
VR4
1
2
5.5V 20A
VR3
1
2
5.5V 20A
CHASSIS_GND

NOTE:

USB HOST ONLY

CRITICAL PLACEMENT

Place SP2 very close to P6

ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER
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VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
DDR_VTT
DDR_PA[15:0]
DDR_PDQ[63:0]
DDR SDRAM
U1
DDR_VREF_0V9
Place parts as close to CPU as possible
500ps Loop
DDR_CLKOUT
DDR_CLKOUT#
J8
879160001
RP24
RP23
RP22
RP21
RP25
RP26
RP19
CP26
CP28
CP29
CP30
CP32
CP31
CP33
GND
VREF
VDDSPD
1V8
5V
U32
VIN
VLDOIN
VDDQSNS
S3
S5
VTT
VTTSNS
VTTREF
GND
PGND
R230
R229
10K
C459
C456
C453
C457
C458
DDR_VTT
PPC_DDR2_DIMM_SCL
PPC_DDR2_DIMM_SDA
R228
R227
4K7
PPC_DDR2_RESET_N
PPC_DDR2_ERROR
PAR_IN
ERR_OUT
TP4
TP5
R226
R225
PLACE NEAREST DDR2 MODULE PINS

ROACH/iBOB2

ROACH_PPC_DDR2

COLLABORATORS:

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APPR:

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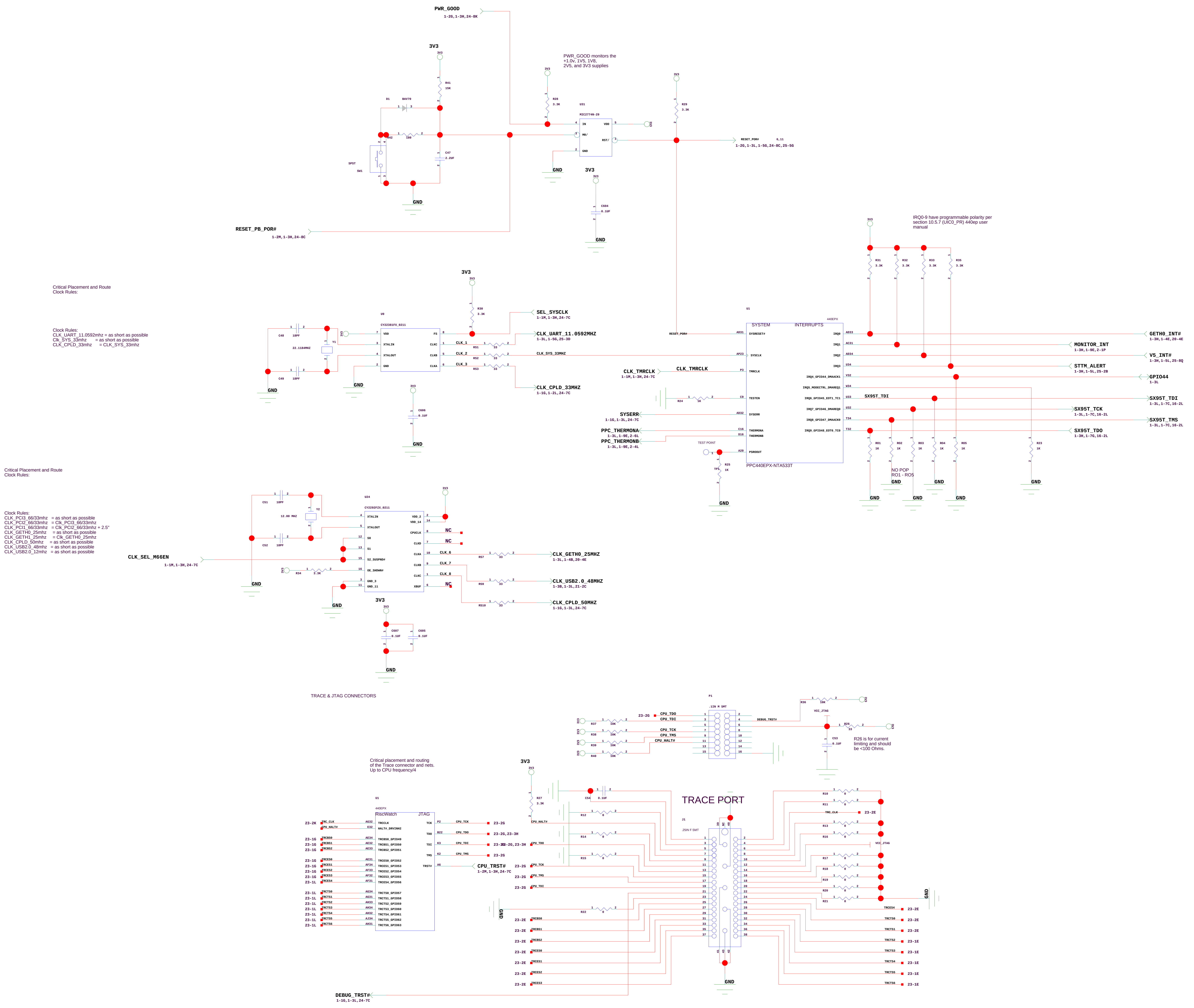
PWR_GOOD
1-2G,1-3H,24-8K
3V3
R41 15K
D1 BAV70
R42 180
C47 2.2UF
SPST SW1
GND
RESET_PB_POR#
1-2M,1-3H,24-8C
R28 3.3K
U31 MIC2774N-29
IN VDD MR/ RST/ GND
R29 3.3K
C604 0.1UF
RESET_POR# 6,11
1-2G,1-3L,1-5G,24-8C,25-5G
R30 3.3K
U9 CY2305SXI-1
22.1184MHZ
C48 10PF
C49 10PF
SEL_SYSCLK
1-1M,1-3H,24-7C
CLK_UART_11.0592MHZ
1-3L,1-5G,25-3D
CLK_SYS_33MHZ
CLK_CPLD_33MHZ
1-1G,1-2L,24-7C
C606 0.1UF
U24 CY2305ZXI-1
12.00 MHZ
C51 10PF
C52 10PF
CLK_SEL_M66EN
1-1M,1-3H,24-7C
R34 3.3K
NC
CLK_GETH0_25MHZ
1-3L,1-4B,20-4E
CLK_USB2.0_48MHZ
1-3B,1-3L,21-2C
CLK_CPLD_50MHZ
1-1G,1-3L,24-7C
C607 0.1UF
C605 0.1UF
U1 440EPX
SYSTEM
INTERRUPTS
SYSRESET#
SYSCLK
TMRCLK
TESTEN
SYSERR
THERMONA
THERMONB
PSROUT
IRQ0 IRQ1 IRQ2 IRQ3
IRQ4_GPIO44_DMAACK1
IRQ5_MODECTRL_DMAREQ1
IRQ6_GPIO45_EOT1_TC1
IRQ7_GPIO46_DMAREQ0
IRQ8_GPIO47_DMAACK0
IRQ9_GPIO48_EOT0_TC0
PPC440EPX-NTA533T
CLK_TMRCLK
1-1M,1-3H,24-7C
R24 1K
SYSERR
1-3L,24-7C
PPC_THERMONA
1-3L,1-9E,2-6L
PPC_THERMONB
1-3L,1-9E,2-4L
TEST POINT
TP1
R25 1K
R31 3.3K
R32 3.3K
R33 3.3K
R35 3.3K
GETH0_INT#
1-3H,1-4E,20-4E
MONITOR_INT
1-3H,1-9E,2-1P
V5_INT#
1-3H,1-5L,25-8Q
STTM_ALERT
1-3H,1-5L,25-2B
GPIO44
1-3L
SX95T_TDI
1-3L,1-7C,16-2L
SX95T_TCK
1-3L,1-7C,16-2L
SX95T_TMS
1-3L,1-7C,16-2L
SX95T_TDO
1-3H,1-7G,16-2L
R01 1K
R02 1K
R03 1K
R04 1K
R05 1K
R23 1K
P1 .1IN M SMT
CPU_TDO
CPU_TDI
CPU_TCK
CPU_TMS
CPU_HALT#
DEBUG_TRST#
R37 10K
R38 10K
R39 10K
R40 10K
R36 10K
VCC_JTAG
R26 33
C53 0.1UF
U1 440EPX
RiscWatch
JTAG
TRCCLK
HALT#_DRVINH2
TCK TDO TDI TMS TRST#
CPU_TRST#
1-2M,1-3H,24-7C
R27 3.3K
C54 0.1UF
TRACE PORT
J1 .25IN F SMT
TRC_CLK
R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22
23-2G
23-2E
23-1E
23-1G
23-1L
23-2K
DEBUG_TRST#
1-1G,1-3L,24-7C

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_SYS_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible

PWR_GOOD monitors the
+1.0v, 1V5, 1V8,
2V5, and 3V3 supplies

IRQ0-9 have programmable polarity per
section 10.5.7 (UIC0_PR) 440ep user
manual

NO POP
RO1 - RO5

TRACE & JTAG CONNECTORS

Critical placement and routing
of the Trace connector and nets.
Up to CPU frequency/4

R26 is for current
limiting and should
be <100 Ohms.

ROACH/iBOB2

ROACH_PPC_TST_CLK_IO

COLLABORATORS:

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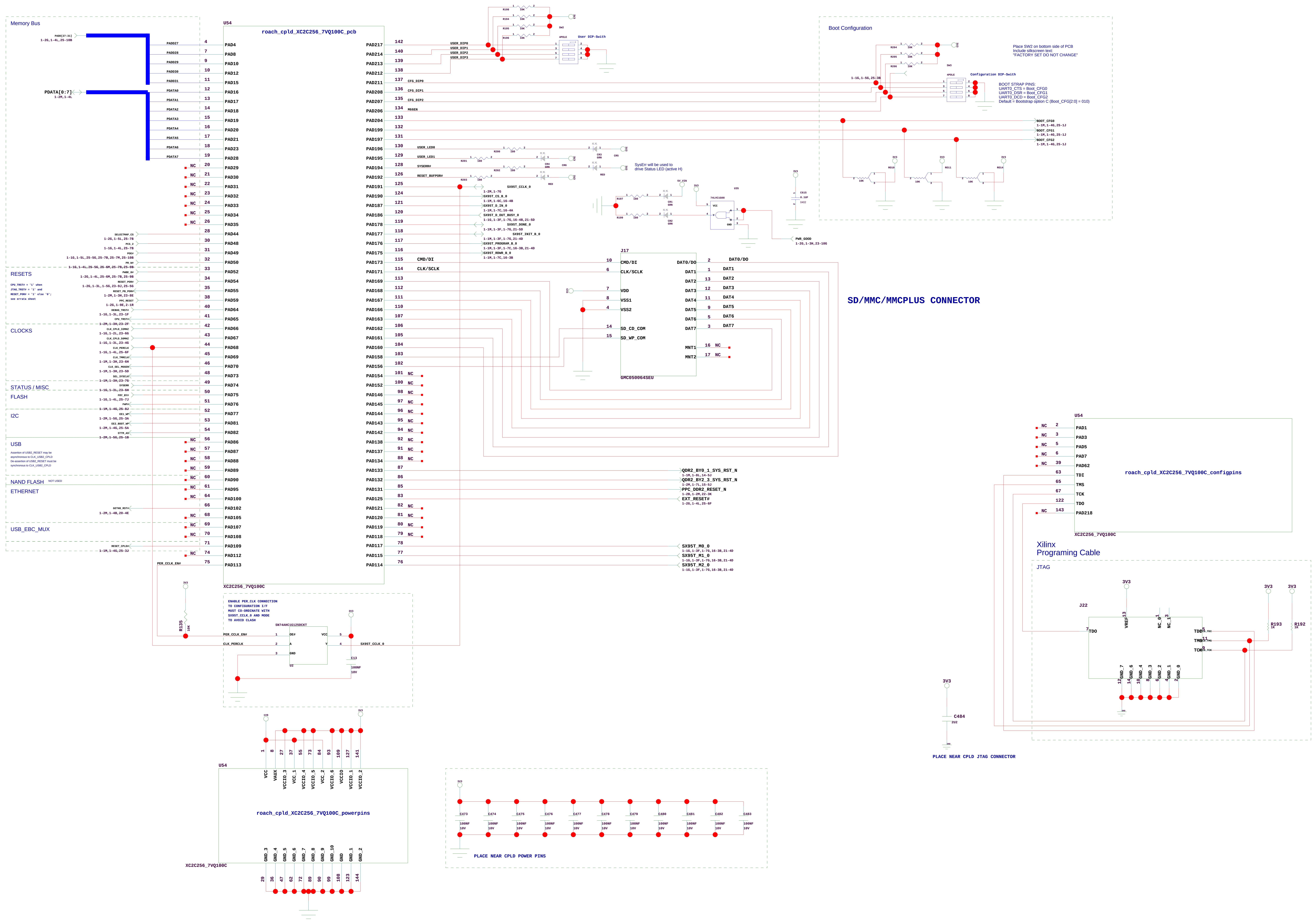
Memory Bus
PDATA[0:7]
roach_cpld_XC2C256_7VQ100C_pcb
U54
XC2C256_7VQ100C
RESETS
CLOCKS
STATUS / MISC
FLASH
I2C
USB
NAND FLASH
NOT USED
ETHERNET
USB_EBC_MUX
NC
User DIP-Swith
Boot Configuration
Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"
Configuration DIP-Swith
BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)
BOOT_CFG0
BOOT_CFG1
BOOT_CFG2
SysErr will be used to
drive Status LED (active H)
PWR_GOOD
J17
CMD/DI
CLK/SCLK
VDD
VSS1
VSS2
SD_CD_COM
SD_WP_COM
DAT0/DO
DAT1
DAT2
DAT3
DAT4
DAT5
DAT6
DAT7
MNT1
MNT2
GMC050064SEU
SD/MMC/MMCPLUS CONNECTOR
QDR2_BY0_1_SYS_RST_N
QDR2_BY2_3_SYS_RST_N
PPC_DDR2_RESET_N
EXT_RESET#
SX95T_M0_0
SX95T_M1_0
SX95T_M2_0
PER_CCLK_EN#
R135
ENABLE PER_CLK CONNECTION
TO CONFIGURATION I/F
MUST CO-ORDINATE WITH
SX95T_CCLK_0 AND MODE
TO AVOID CLASH
SN74AHC1G125DCKT
CLK_PERCLK
SX95T_CCLK_0
C13
100NF
10V
U2
roach_cpld_XC2C256_7VQ100C_powerpins
VCC
VAUX
VCCIO_3
VCC_1
VCCIO_4
VCCIO_5
VCC_2
VCCIO_6
VCCIO
VCCIO_1
VCCIO_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND
GND_1
GND_2
C473
C474
C475
C476
C477
C478
C479
C480
C481
C482
C483
100NF
10V
PLACE NEAR CPLD POWER PINS
roach_cpld_XC2C256_7VQ100C_configpins
PAD1
PAD3
PAD5
PAD7
PAD62
TDI
TMS
TCK
TDO
PAD218
XC2C256_7VQ100C
Xilinx
Programing Cable
JTAG
J22
3V3
R193
R192
TDO
VREF
NC_0
NC_1
TDI
TMS
TCK
C484
2U2
PLACE NEAR CPLD JTAG CONNECTOR

ROACH/iBOB2

ROACH_PPC_CPLD

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PDATA[0:31]
PADD[2:31]
PADD30 IS THE LSB FOR 16 BIT WIDE BUS TRANSFERS
NOTE: DMA SIGNALS IN GREEN TEXT
PADD2 IS THE MSB
External Slave Peripheral
External Master Peripheral Interface
FLASH 32Mx16 /64Mx8
EPB RESET OUTPUT
EXT_RESET#
CLK_PERCLK
FWP#
FRY_BY#
RESET_POR#
3V3
GND
U15
BANKS=1, 2, 4
CHIP SELECT 1
PER_CS0
PER_OE_N
PER_R_W_N
PER_WBE[1]
PER_WBE[0]
PER_B_LAST
PER_CLK
PER_READY
PER_INT
I2C0_SCLK
I2C0_33_DATA
EE2_BOOT_WP
EE1_WP
AT24C64N-10SU-1.8
NO POP
PI5A2157
S=0 B0 to A
MGGEN
STTM_ALERT
STTM_AS
AD7414-0
SCPCLK
SCPDI
SCPDO
UART
IIC0
IIC1_SPI
NAND Flash Interface
NOT USED
ICL3225ECA
UART Port 0
UART Port 1
J14
HLE-105-02-G-DV
BOOT_CFG2
BOOT_CFG1
BOOT_CFG0
RESET_CPLD#

ROACH/iBOB2

ROACH_PPC_NVM_SERIAL

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