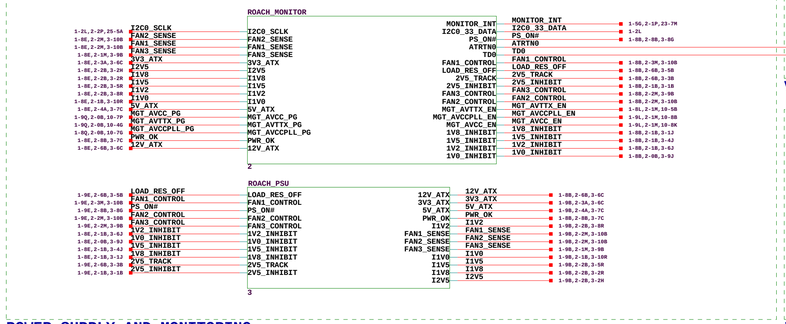
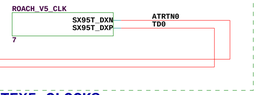
VIRTEX5

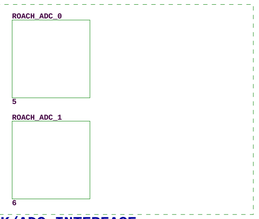
POWER SUPPLY AND MONITORING



VIRTEX5 CLOCKS

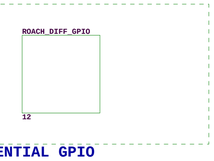


ZDOK/ADC INTERFACE



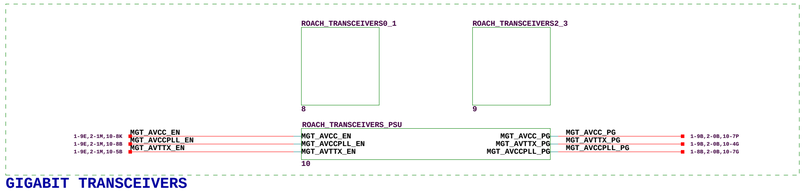
V5 DDR2 MEMORY

V5 DIFFERENTIAL GPIO

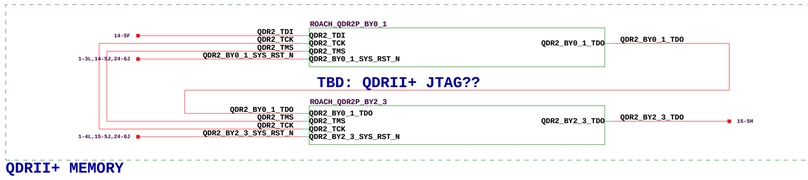


V5 SE GPIO & MISCELLANEOUS

GIGABIT TRANSCEIVERS



QDRII+ MEMORY

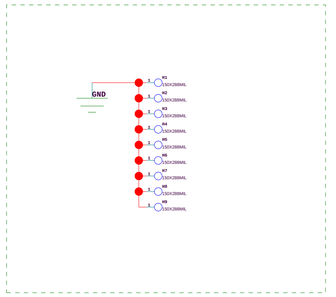


V5 POWER

VIRTEX5 CONFIGURATION

PPC

MECHANICAL



CONTRIBUTORS

ETIENNE BAUERMEISTER
HENRY CHEN
STEVE DURAND
FRANCOIS KAPP
ALAN LANDMAN
GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2	**ROACH_TOP**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-4-2007_15:06	DRAWN: F KAPP APPR:
PATH PATH	CHECKED: E BAUERMEISTER SHEET 1 OF 25

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

TIE TO GROUND IF PLL'S ARE NOT USED

PLACE AT ACTEL 1V5 POWER PINS

PLACE AT ACTEL 3V3 POWER PINS

roach_AFS600_powerpins

roach_AFS600_pcb

XPORT - PLACE IN REAR I/O REGION
XP10010001-03R

TEMPERATURE DIODE HEADER
15-91-2200

SPARE ANALOG VOLTAGE INPUT #0
SPARE ANALOG VOLTAGE INPUT #1
SPARE GATE DRIVE OUTPUT #0
SPARE GATE DRIVE OUTPUT #1
15-91-2080

PUSH BUTTON POWER SWITCH

roach_AFS600_configpins

ACTEL JTAG CONNECTOR

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

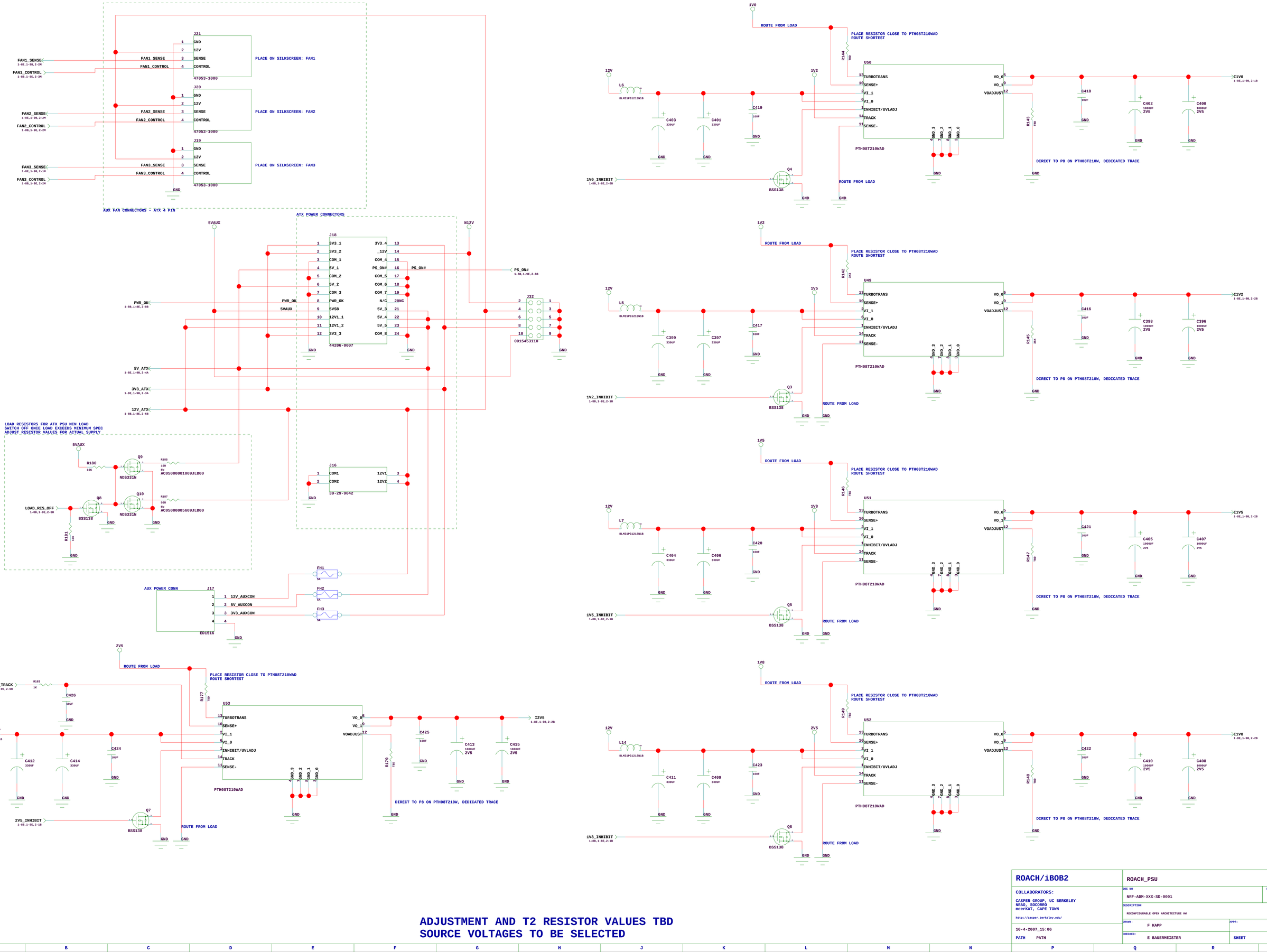
http://casper.berkeley.edu/

10-4-2007_15:06

PATH PATH

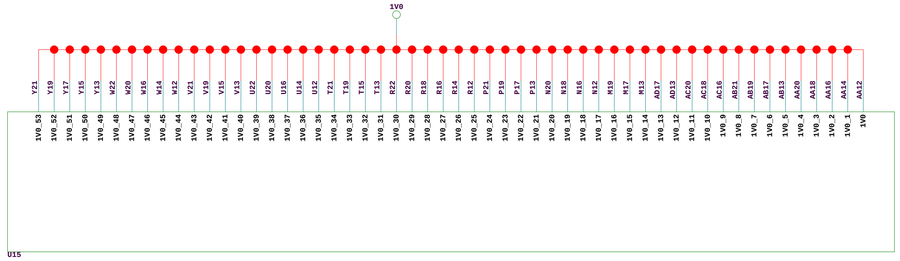
ROACH_MONITOR

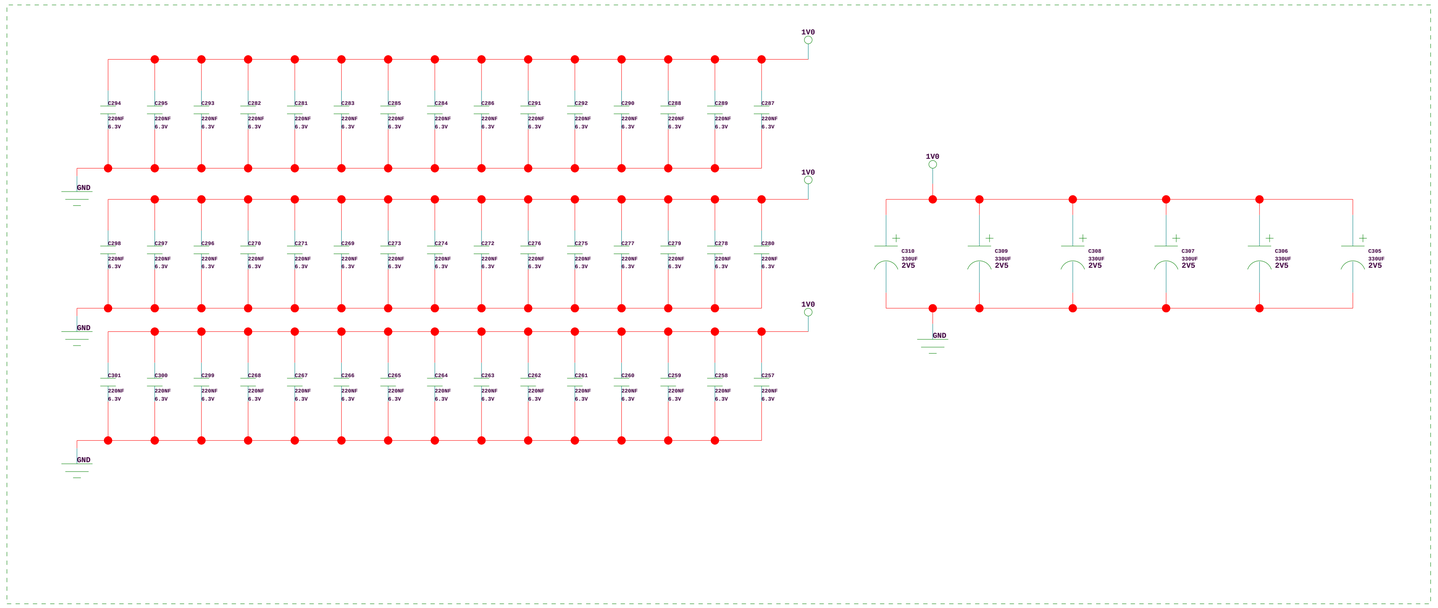
DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	2 OF 25

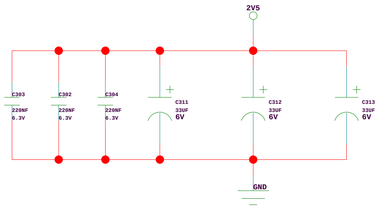


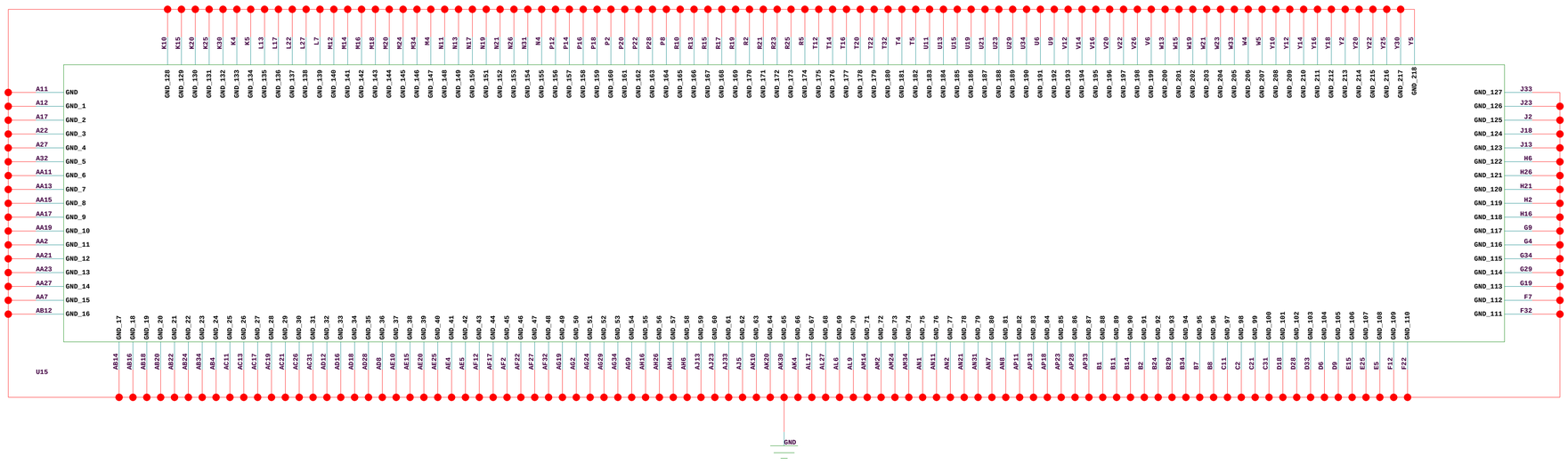
ADJUSTMENT AND T2 RESISTOR VALUES TBD
SOURCE VOLTAGES TO BE SELECTED

ROACH/iBOB2	**ROACH_PSU**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
10-4-2007_15:06	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 3 OF 25





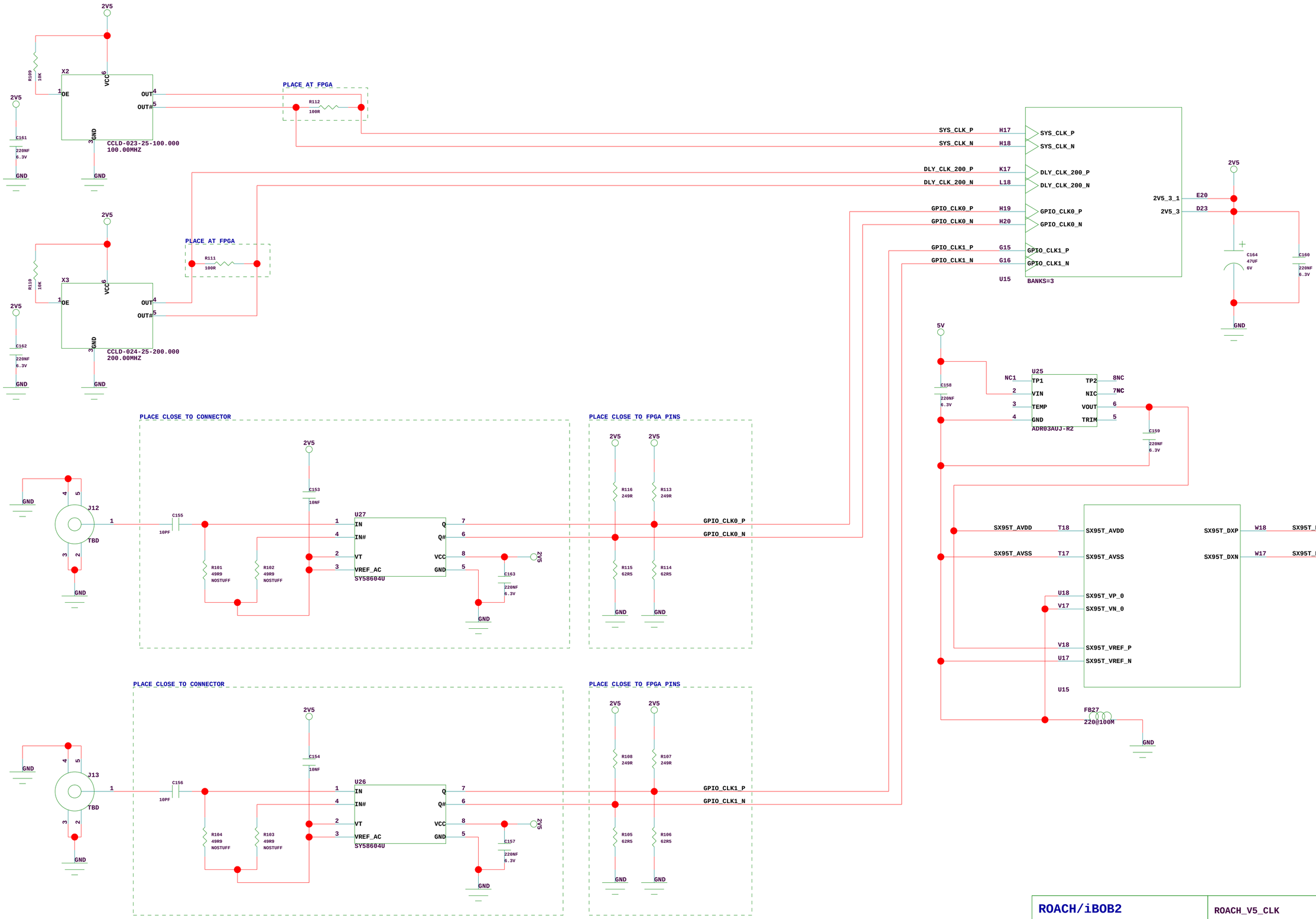




ROACH/iBOB2		**ROACH_5V_POWER**	
COLLABORATORS:		DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN		DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
http://casper.berkeley.edu/		DRAWN: F KAPP	APPR:
10-4-2007_15:06		CHECKED: E BAUERMEISTER	SHEET: 4 OF 25
PATH PATH			

ROACH/iBOB2	**ROACH_ADC_0**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 5 OF 25
10-4-2007_15:06 PATH PATH	

ROACH/iBOB2	**ROACH_ADC_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 6 OF 25
10-4-2007_15:06 PATH PATH	



ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
10-4-2007_15:06 PATH PATH	

ROACH/iBOB2

ROACH_TRANSCEIVERS0_1

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

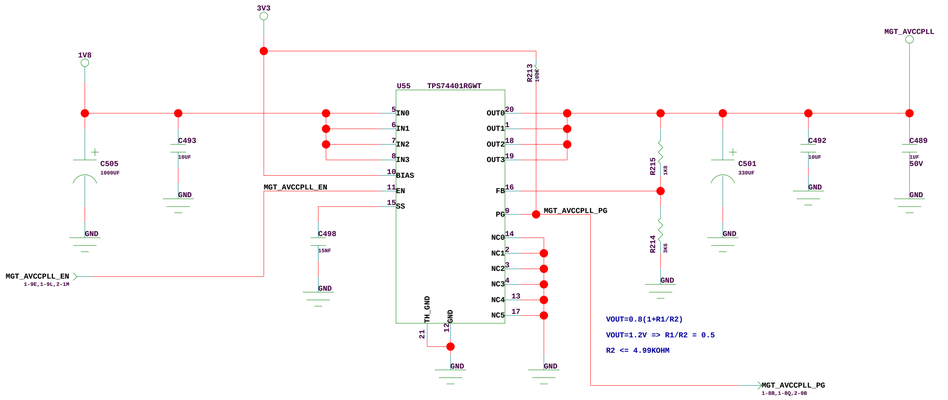
http://casper.berkeley.edu/

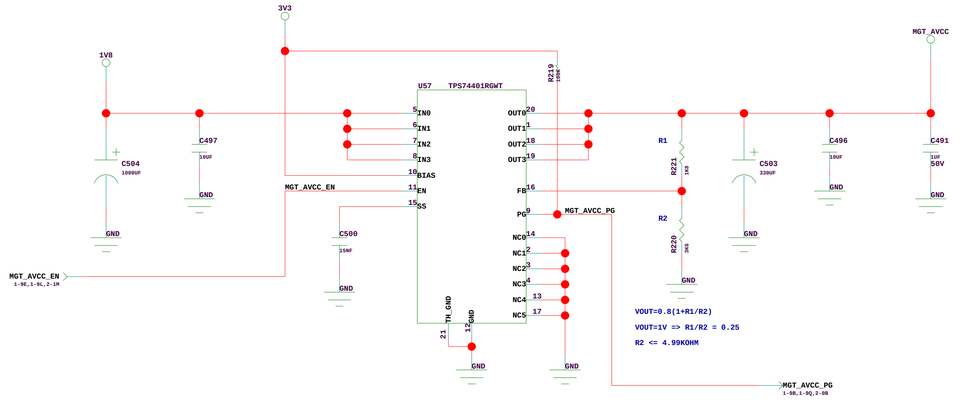
10-4-2007_15:06

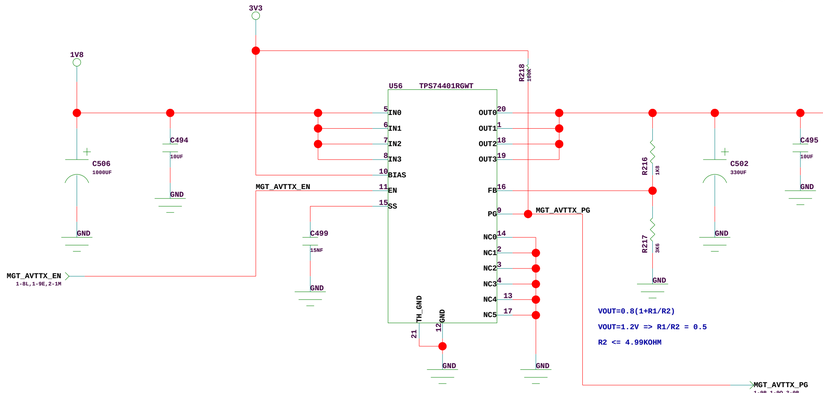
PATH PATH

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	8 OF 25

MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB28 220@100M
FB29 220@100M
FB30 220@100M
FB31 220@100M
C172 C171 C170 C169 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
2V5
FB52 220@100M
C248 220NF 6.3V
R131 10K
X4
OE
VCC
OUT
GND
JP9
CCLD-023-25-156.250
156.25MHZ
MGT_REFCLK_Q2_P
MGT_REFCLK_Q2_N
C181 C182 C183 C184 C186 C185 10NF 25V
MGTAVCC_120 D5
MGTAVCC_120_1 F4
MGTAVCCPLL_120 D3
MGTAVTTRX_120 C3
MGT_120_REF_CLK_P E4
MGT_120_REF_CLK_N D4
MGTRX0_120_P A3
MGTRX0_120_N A2
MGTRX1_120_P D1
MGTRX1_120_N C1
U15
MGTAVTTTX_120_1 E3
MGTAVTTTX_120 C4
MGTTX0_120_P B4
MGTTX0_120_N B3
MGTTX1_120_P E2
MGTTX1_120_N D2
FB32 220@100M
FB33 220@100M
C174 C173 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
P3
S39 DL0P
S40 DL0N
S41 DL1P
S42 DL1N
S43 DL2P
S44 DL2N
S45 DL3P
S46 DL3N
S54 SL0P
S53 SL0N
S52 SL1P
S51 SL1N
S50 SL2P
S49 SL2N
S48 SL3P
S47 SL3N
SIG_GND1 G20
SIG_GND2 G21
SIG_GND3 G22
SIG_GND4 G23
SIG_GND5 G24
SIG_GND6 G25
SIG_GND7 G26
SIG_GND8 G27
SIG_GND9 G28
SIG_GND10 G19
FCN-268F036-G/3DB
JP7
ODIS
FAULT
R123 10K
C240 10NF
C242 10NF
3V3
R132 150R
OPTICAL MODULE FAULT - RED LED
R121 5K1
R120 3K9
R119 6K8
R118 3K9
C241 10NF
U34 MAX9032AKA
U30 MAX9032AKA
U36 AND2 SN74AHC1G08DCKR
U37 AND2 SN74AHC1G08DCKR
U28 TPS2031D
R130 10K
R117 10K
C239 10NF
C227 100NF
C167 4.7UF 16V
C165 22UF
C246 10NF
C247 100NF
C168 4.7UF 16V
C166 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB38 220@100M
FB39 220@100M
FB36 220@100M
FB37 220@100M
C180 C179 C178 C177 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
C251 C252 C255 C256 C250 C249 C254 C253 10NF 25V
MGTAVCC_122 AJ4
MGTAVCC_122_1 AK5
MGTAVCCPLL_122 AM4
MGTAVTTRX_122 AL3
MGT_122_REF_CLK_P NC AL5
MGT_122_REF_CLK_N NC AL4
MGTRX0_122_P AL1
MGTRX0_122_N AM1
MGTRX1_122_P AP3
MGTRX1_122_N AP2
U15
MGTAVTTTX_122_1 AM3
MGTAVTTTX_122 AK3
MGTTX0_122_P AK2
MGTTX0_122_N AL2
MGTTX1_122_P AN4
MGTTX1_122_N AN3
FB35 220@100M
FB34 220@100M
C175 C176 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB44 220@100M
FB45 220@100M
FB42 220@100M
FB43 220@100M
C221 C220 C215 C212 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
C187 C188 C189 C190 10NF 25V
MGTAVCC_124 C7
MGTAVCC_124_1 D7
MGTAVCCPLL_124 C6
MGTAVTTRX_124 C9
MGT_124_REF_CLK_P NC D8
MGT_124_REF_CLK_N NC C8
MGTRX0_124_P A9
MGTRX0_124_N A8
MGTRX1_124_P A6
MGTRX1_124_N A7
U15
MGTAVTTTX_124_1 C5
MGTAVTTTX_124 C10
MGTTX0_124_P B10
MGTTX0_124_N B9
MGTTX1_124_P B5
MGTTX1_124_N B6
FB41 220@100M
FB40 220@100M
C213 C214 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
P3
S57 DL0P
S58 DL0N
S59 DL1P
S60 DL1N
S61 DL2P
S62 DL2N
S63 DL3P
S64 DL3N
S72 SL0P
S71 SL0N
S70 SL1P
S69 SL1N
S68 SL2P
S67 SL2N
S66 SL3P
S65 SL3N
SIG_GND1 G29
SIG_GND2 G30
SIG_GND3 G31
SIG_GND4 G32
SIG_GND5 G33
SIG_GND6 G34
SIG_GND7 G35
SIG_GND8 G36
SIG_GND9 G37
SIG_GND10 G19
FCN-268F036-G/3DB
JP8
ODIS
FAULT
R124 10K
C245 10NF
C243 10NF
3V3
R132 150R
OPTICAL MODULE FAULT - RED LED
R126 5K1
R127 3K9
R128 6K8
R129 3K9
C244 10NF
U34 MAX9032AKA
U30 MAX9032AKA
U37 AND2 SN74AHC1G08DCKR
U29 TPS2031D
R133 10K
C248 C247 C168 C166 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB49 220@100M
FB48 220@100M
FB51 220@100M
FB50 220@100M
C224 C225 C191 C226 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
C255 C256 C250 C249 C254 C253 10NF 25V
MGTAVCC_126 AL8
MGTAVCC_126_1 AM8
MGTAVCCPLL_126 AM9
MGTAVTTRX_126 AM6
MGT_126_REF_CLK_P NC AL7
MGT_126_REF_CLK_N NC AM7
MGTRX0_126_P AP6
MGTRX0_126_N AP7
MGTRX1_126_P AP9
MGTRX1_126_N AP8
U15
MGTAVTTTX_126_1 AM5
MGTAVTTTX_126 AM10
MGTTX0_126_P AN5
MGTTX0_126_N AN6
MGTTX1_126_P AN10
MGTTX1_126_N AN9
FB46 220@100M
FB47 220@100M
C223 C222 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
10-4-2007_15:06
PATH PATH
ROACH_TRANSCEIVERS2_3
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
CHECKED: E BAUERMEISTER
APPR:
SHEET 9 OF 25







ROACH/iBOB2

ROACH_TRANSCEIVERS_PSU

COLLABORATORS:

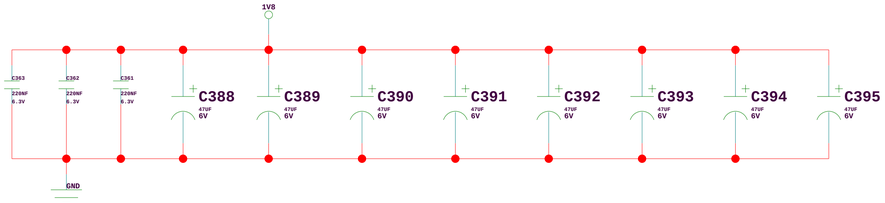
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

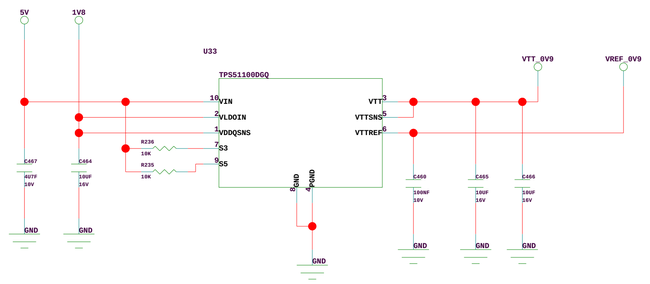
http://casper.berkeley.edu/

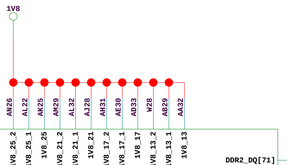
10-4-2007_15:06

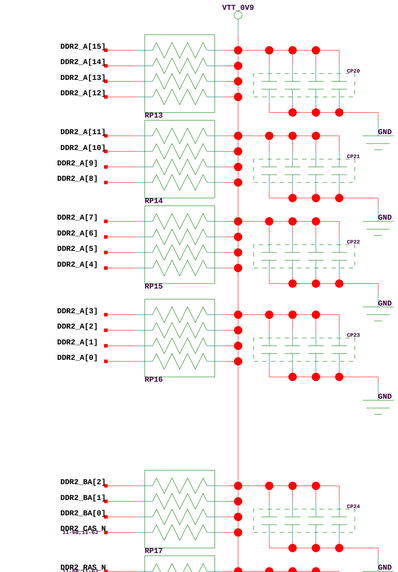
PATH PATH

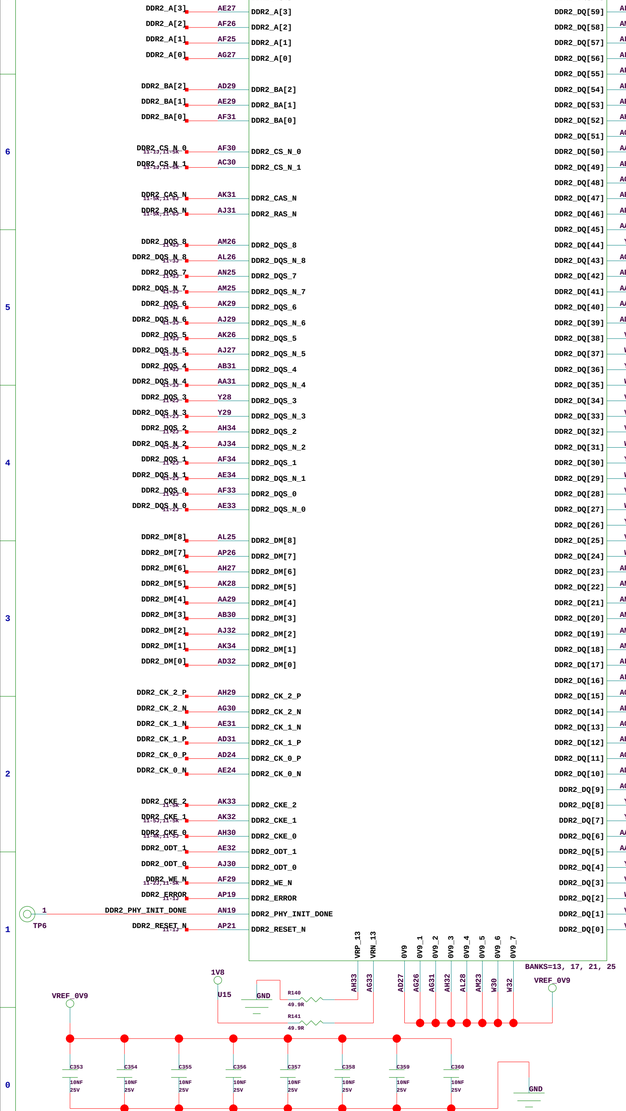
DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	10 OF 25

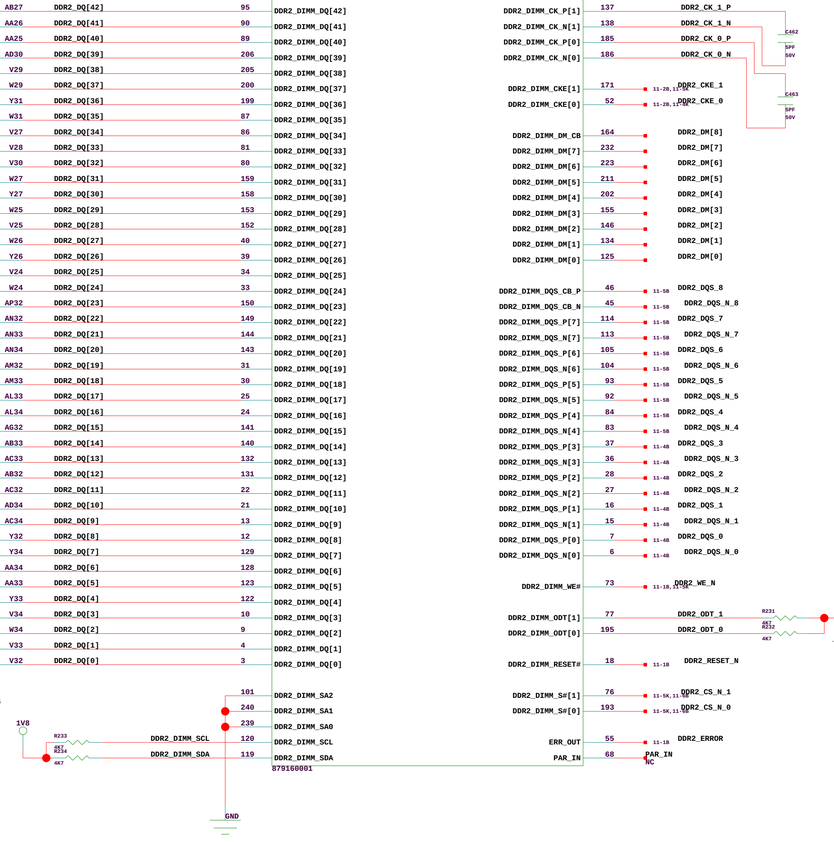




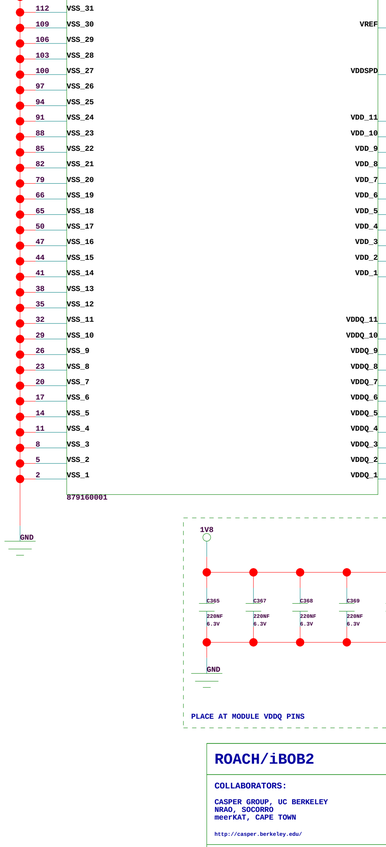




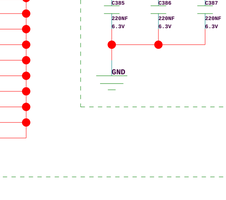




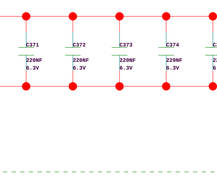
VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT



PLACE AT MODULE VREF PIN



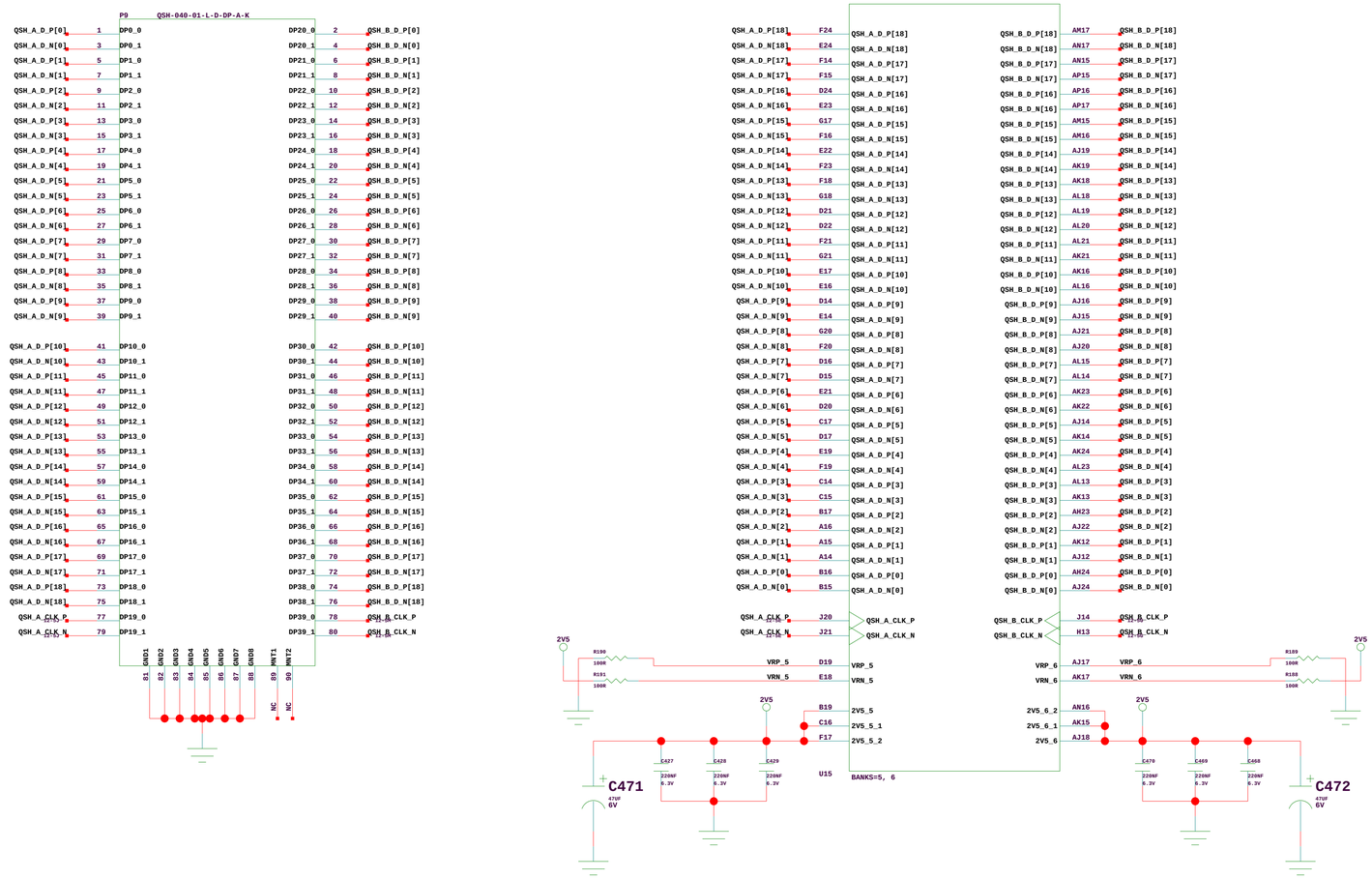
PLACE AT MODULE VDDSPD PIN



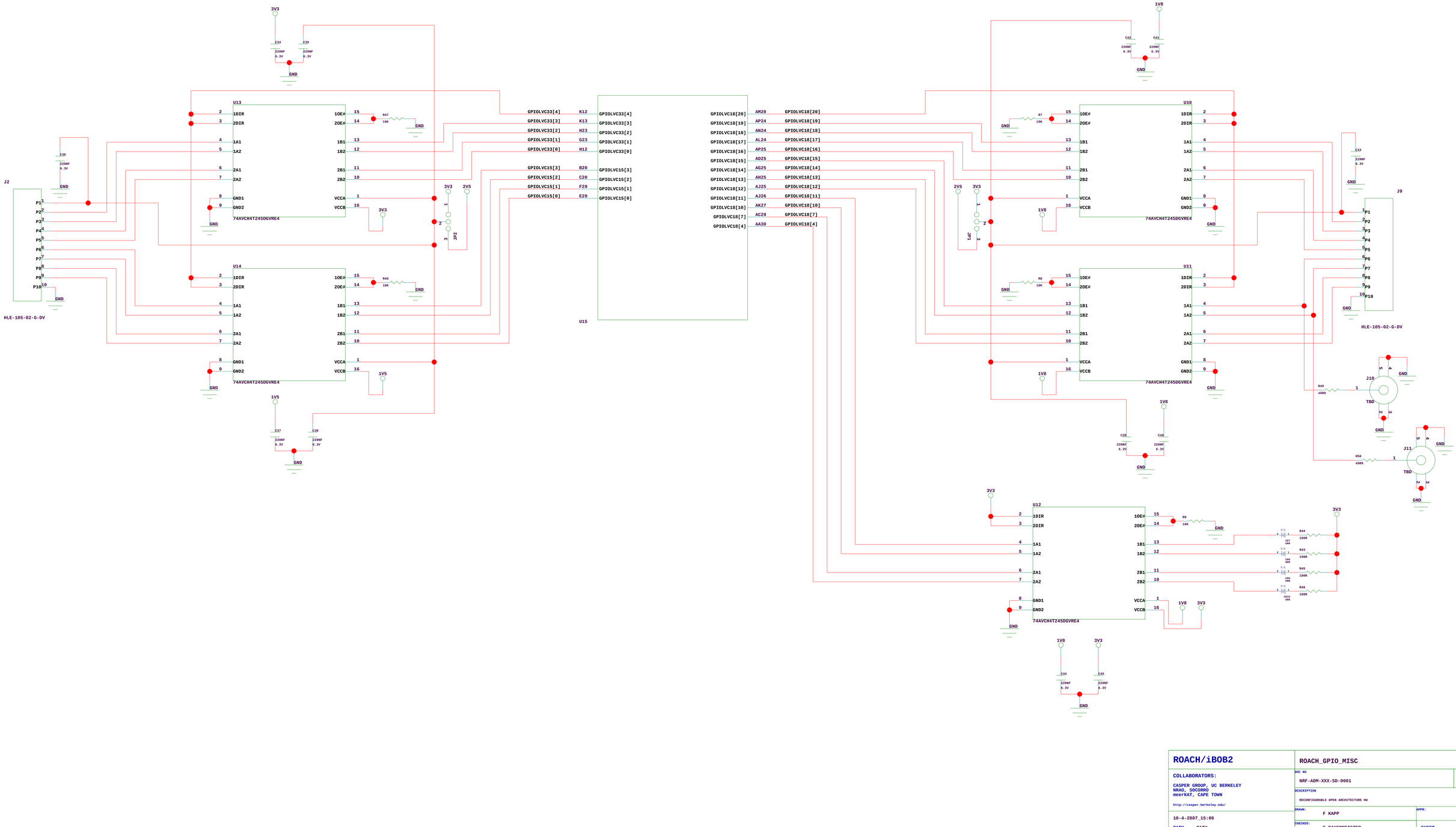
PLACE AT MODULE VDD PINS

PLACE AT MODULE VDDQ PINS

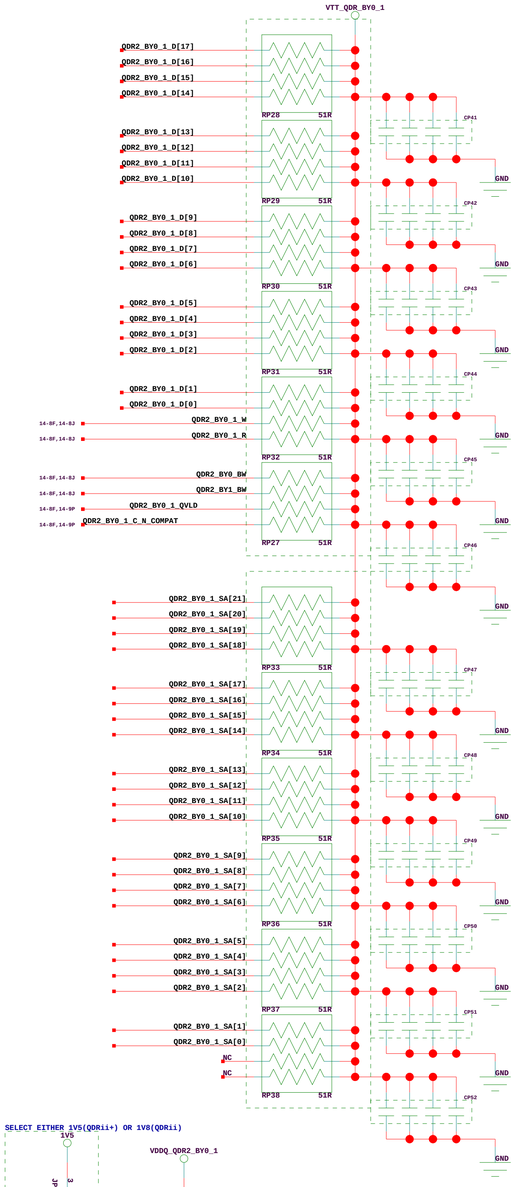
ROACH/iBOB2	**ROACH_DDR2_DIMM**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-4-2007_15:06 PATH PATH	DRAWN: F KAPP APPR:
	CHECKED: E BAUERMEISTER SHEET 11 OF 25

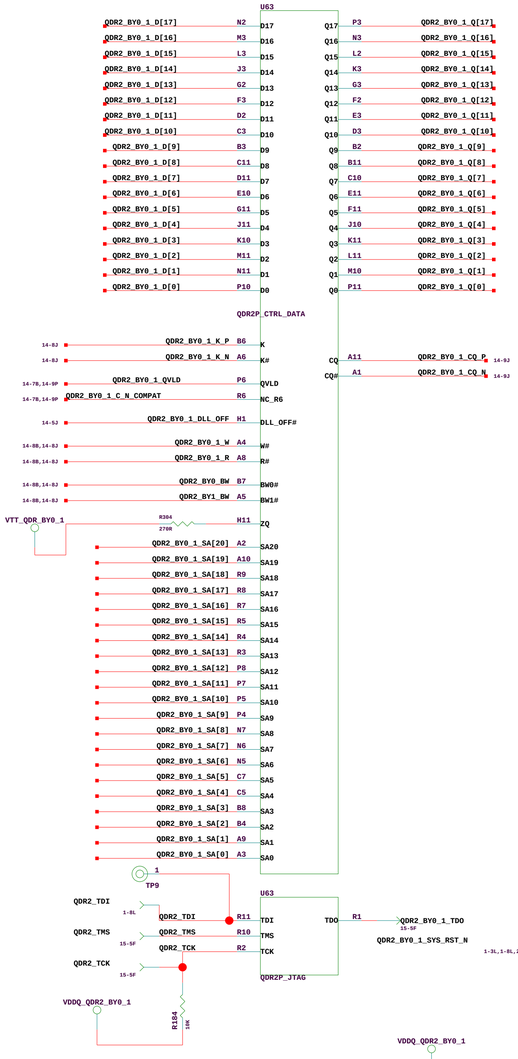


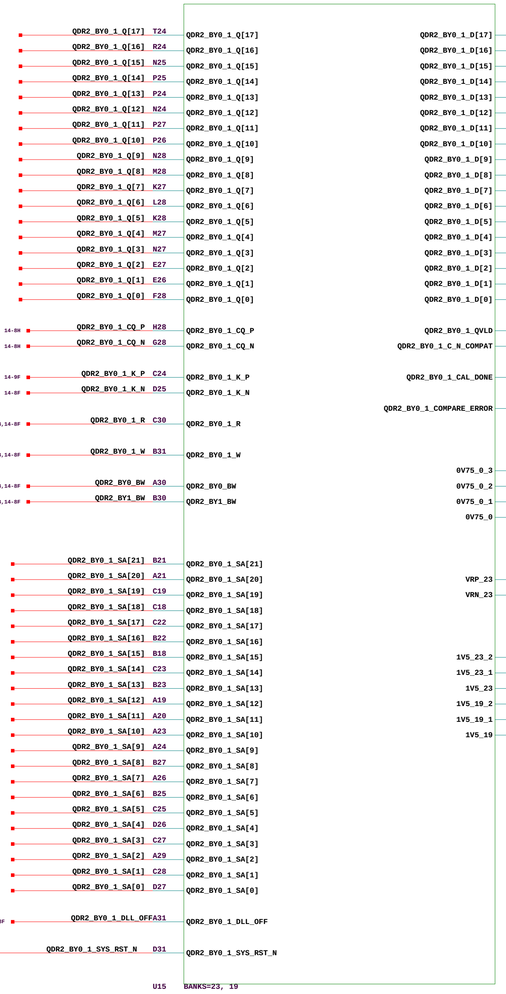
ROACH/iBOB2	**ROACH_DIFF_GPIO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-4-2007_15:06 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 12 OF 25

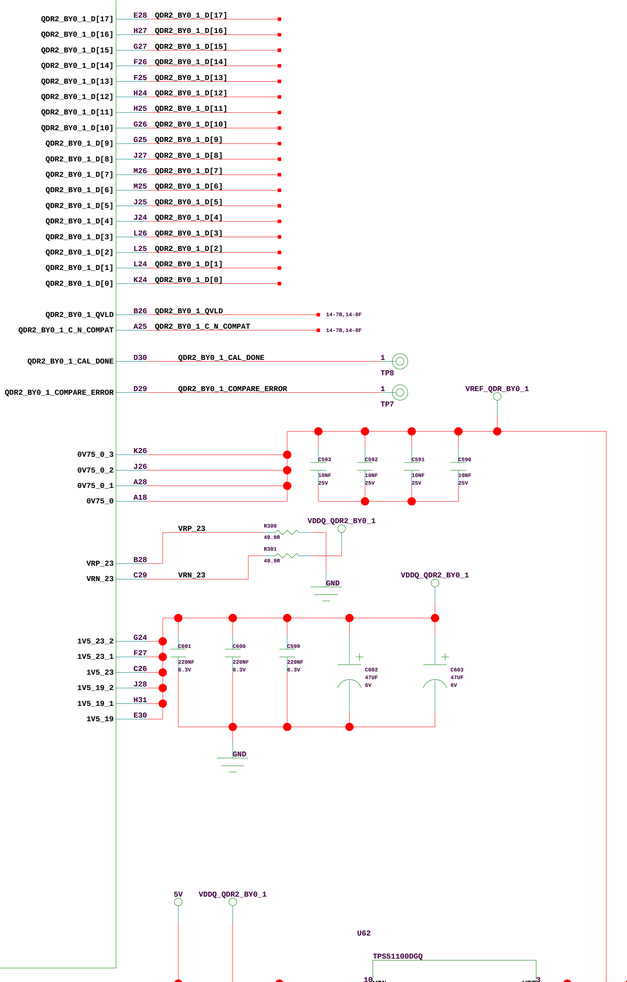


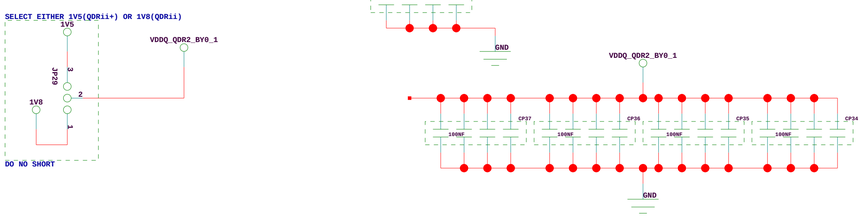
ROACH/iBOB2	**ROACH_GPIO_MISC**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 13 OF 25
10-4-2007_15:06 PATH PATH	

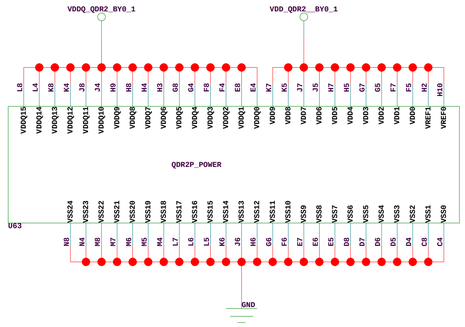


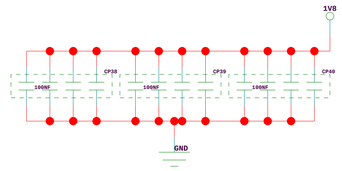


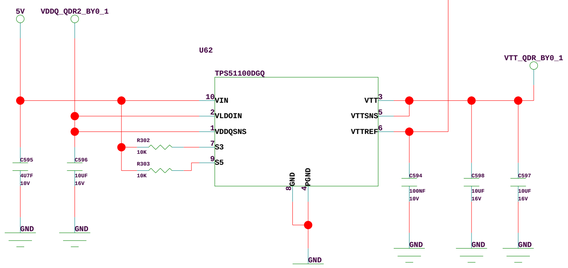




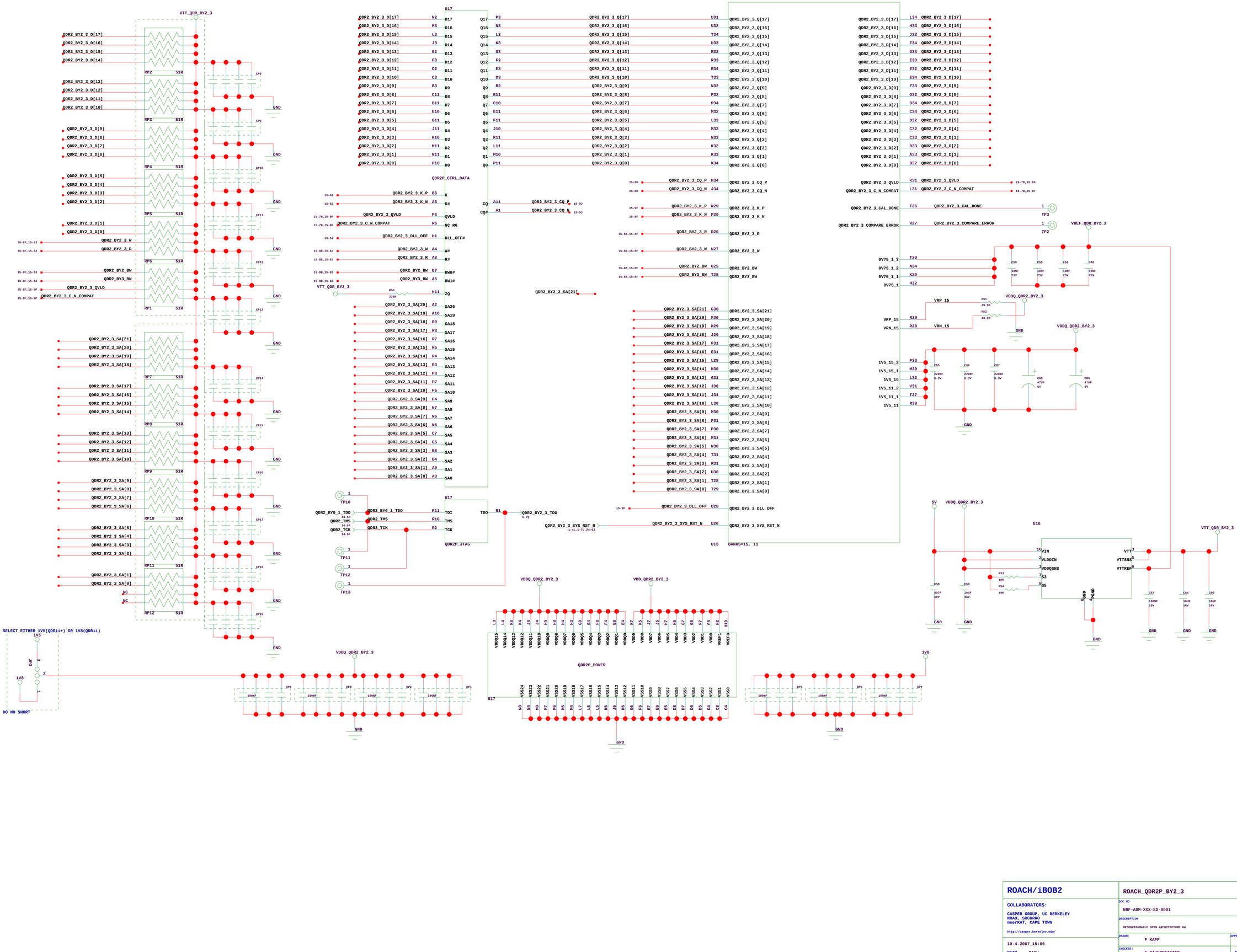








ROACH/iBOB2	ROACH_QDR2P_BY0_1	
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
10-4-2007_15:06	DRAWN: F KAPP	APPR:
PATH PATH	CHECKED: E BAUERMEISTER	SHEET 14 OF 25

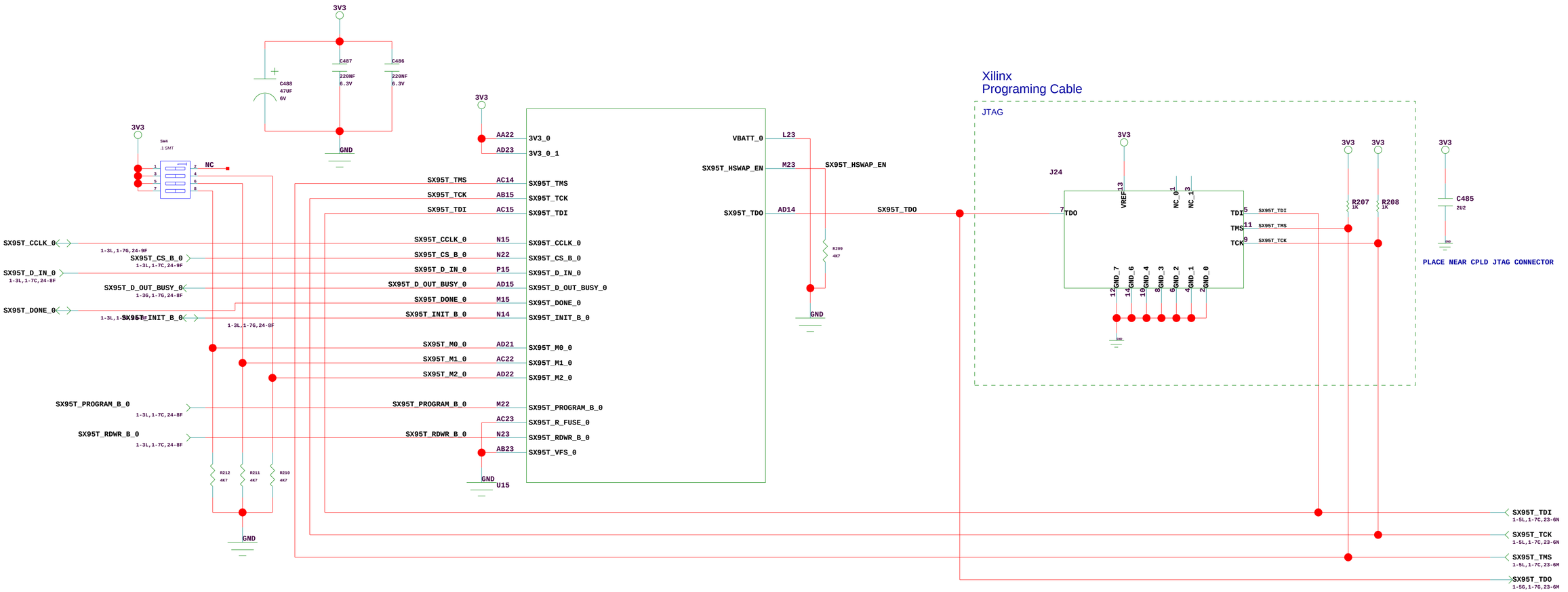


ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET: 15 OF 25
10-4-2007_15:06	
PATH PATH	

TBD

VALID CONFIGURATION MODES

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input



ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
10-4-2007_15:06 PATH PATH	

Place components close to CPU

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J3: "1V5"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J4: "1V8"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J5: "2V5"

Place Ferrite beads and jumper as close to CPU as possible

Place silk screen near J6: "3V3"

Place components close to CPU

Place components close to CPU

Alternate power input terminal
Two 10A fuses result in 16A rating

+5.0 V

Bulk Decoupling

CPU Core by-pass caps place as close to CPU Vdd pins as possible

CPU Core by-pass caps place as close to CPU SOVdd pins as possible

CPU Core by-pass caps place as close to CPU DVdd pins as possible

Each Analog GND tied to Digital GND at a single point.

+1.8 V

Place all components within this block close together

~2.9Amp

~3.6Amp

Place these 4 caps close to DDR parts

VOUT= 0.6v(1+R1/R2)

+1.5 V

VOUT= 0.6v(1+R1/R2)
PLLLPF = VIN = 750khz

PWR_GOOD

1-4D,1-4G,1-5E,1-5G,18-2F,23-19G,24-8K

Place all components within this block close together

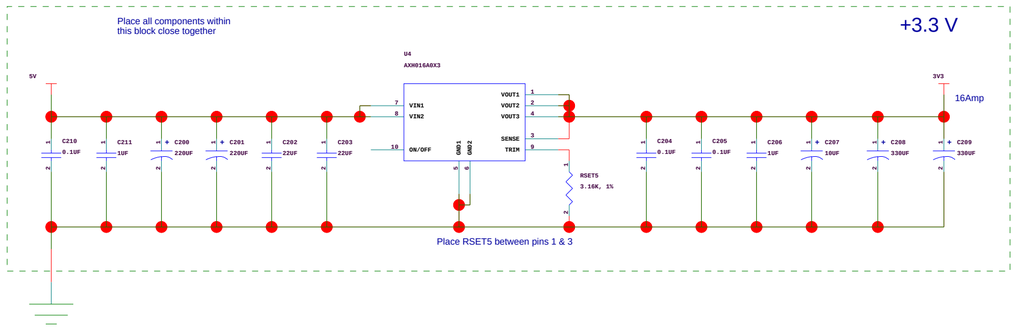
+0.9 V

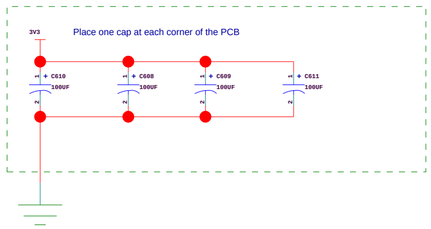
Use 25mil trace

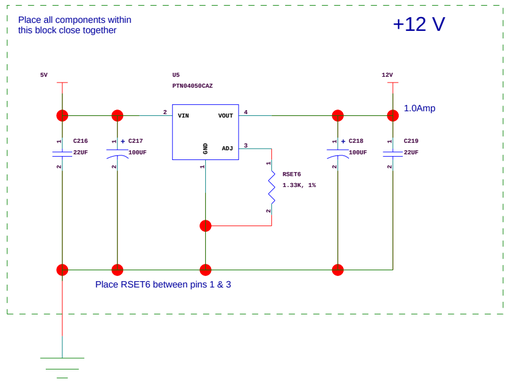
VTT_+0.9V
1-5E

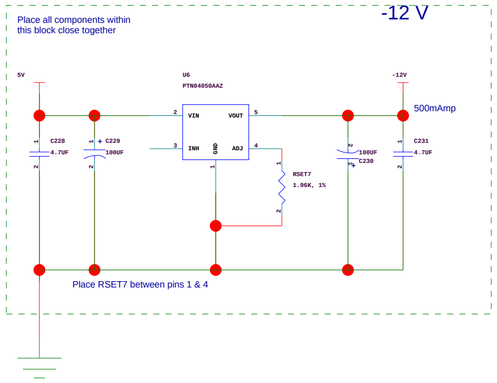
VTT island by-pass caps place evenly across VTT island
(1 cap for every 2 signals terminated)
(1 Tantalum Cap on each end of island)
VTT regulator placed at center of VTT island

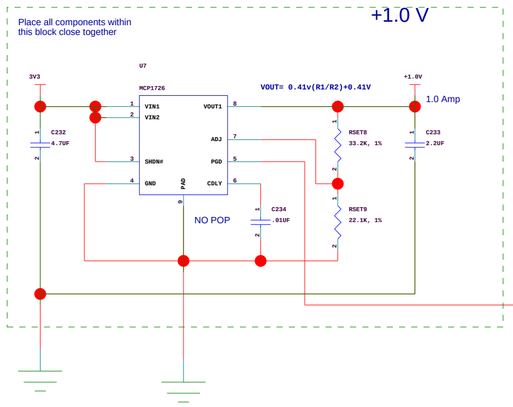
ROACH/iBOB2	ROACH_PPC_POWER_1
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-4-2007_15:06	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 17 OF 25

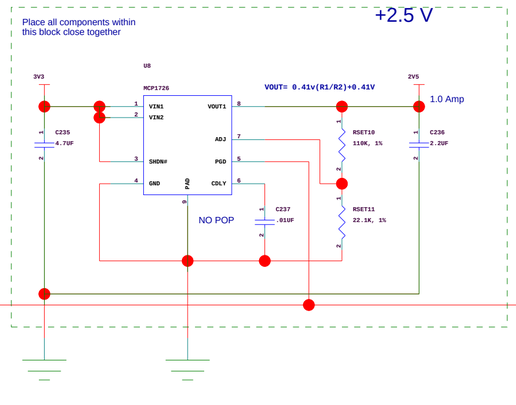


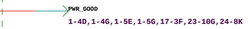




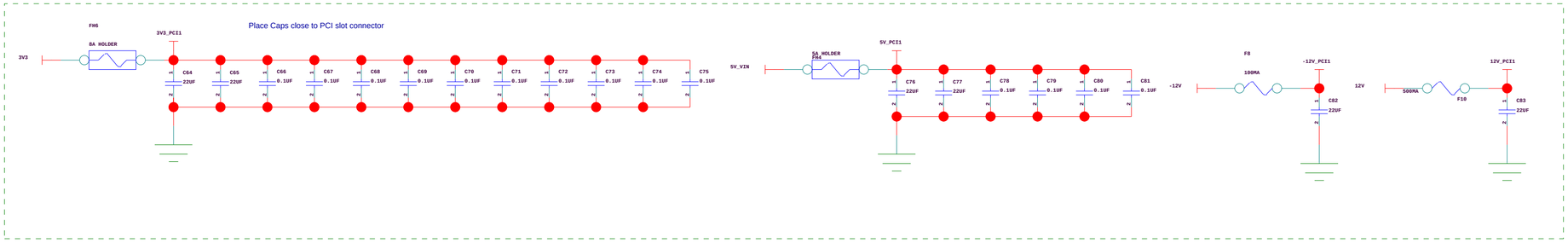


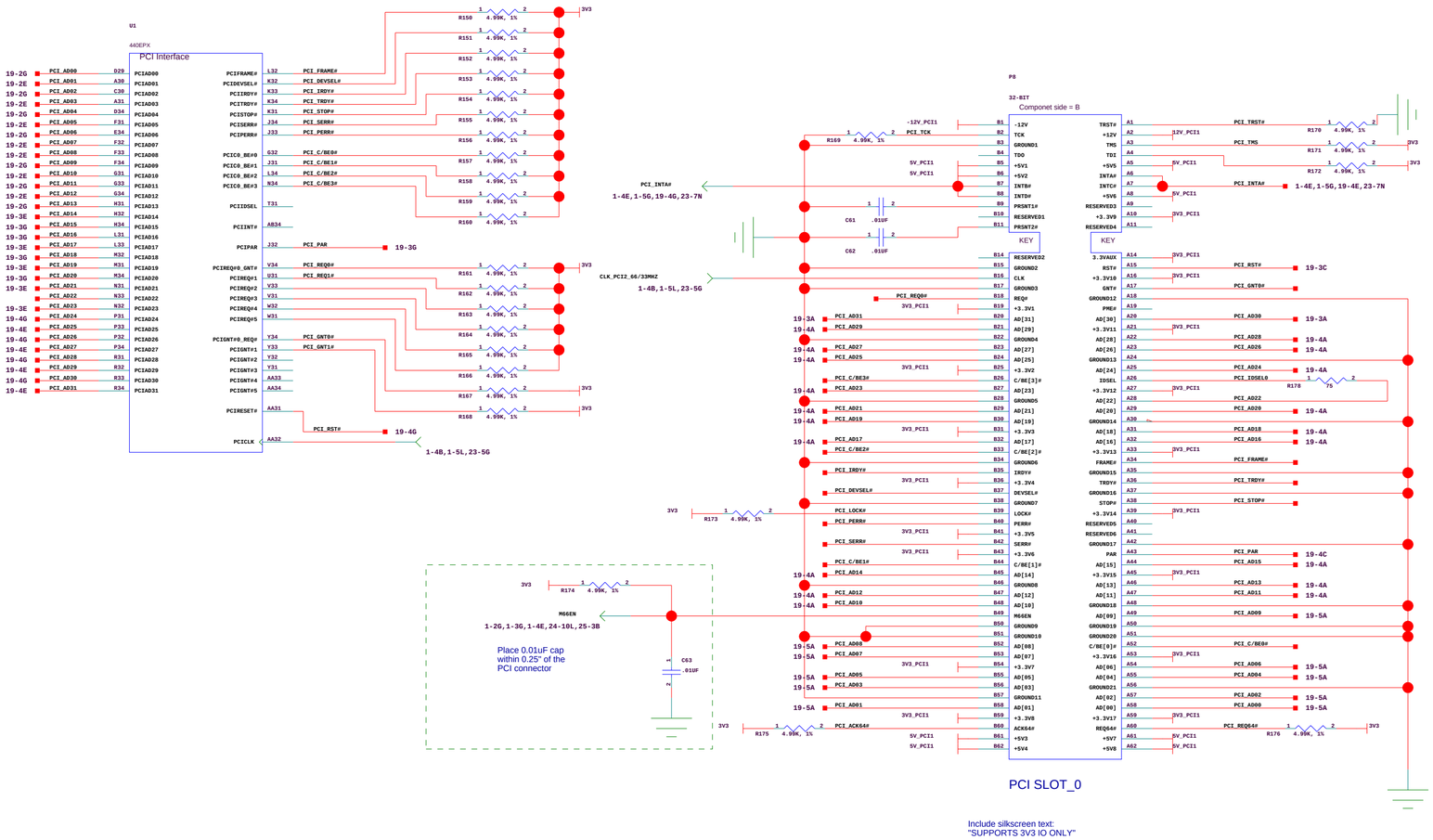






ROACH/iBOB2	**ROACH_PPC_POWER_2**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET 18 OF 25
10-4-2007_15:06 PATH PATH	





Include silkscreen text:
"SUPPORTS 3V3 IO ONLY"

Optional PRSNT signals are not used, max 25W is available		
PRSNT1#	PRSNT2#	Expansion Configuration
Open	Open	No expansion board present
Ground	Open	Expansion board present, 25 W maximum
Open	Ground	Expansion board present, 15 W maximum
Ground	Ground	Expansion board present, 7.5 W maximum

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

10-4-2007_15:06

PATH PATH

ROACH_PPC_PCI

DOC NO	REVISION
NRF-ADM-XXX-SD-0001	A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN:	APPR:
F KAPP	
CHECKED: E BAUERMEISTER	SHEET 19 OF 25

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.
Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

Place nearest PHY pin 96

Place nearest PHY pin 101

Place nearest PHY pin 98

Place nearest PHY pin 100

Place as close to PHY CORE VDD power pins as possible

Place as close to PHY IO VDD power pins as possible

UNUSED SECOND ETHERNET MAC

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place jumpers in line with signals

Place decoupling C close to termination R All traces 50Ohm WRT GND or 2V5

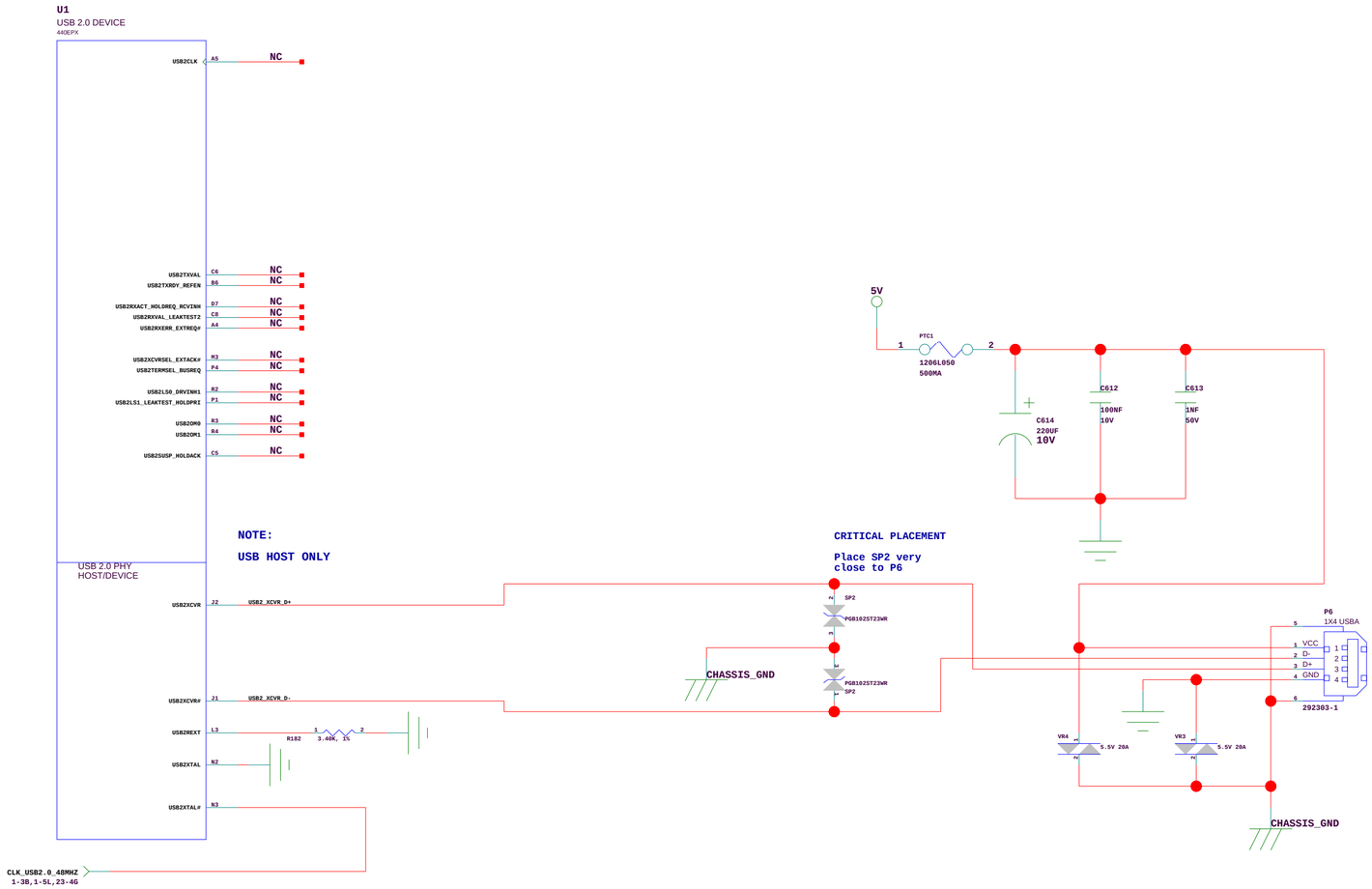
Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

ROACH/iBOB2	ROACH_PPC_ETH1
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
10-4-2007_15:06	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 20 OF 25



ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25
10-4-2007_15:06 PATH PATH	

DDR_PA[15:0]

DDR_PD0[63:0]

U1

DDR SDRAM

64DEPX

DDR_PD0	MEMDATA00	MEMADDR00	DDR_PA0
DDR_PD1	MEMDATA01	MEMADDR01	DDR_PA1
DDR_PD2	MEMDATA02	MEMADDR02	DDR_PA2
DDR_PD3	MEMDATA03	MEMADDR03	DDR_PA3
DDR_PD4	MEMDATA04	MEMADDR04	DDR_PA4
DDR_PD5	MEMDATA05	MEMADDR05	DDR_PA5
DDR_PD6	MEMDATA06	MEMADDR06	DDR_PA6
DDR_PD7	MEMDATA07	MEMADDR07	DDR_PA7
DDR_PD8	MEMDATA08	MEMADDR08	DDR_PA8
DDR_PD9	MEMDATA09	MEMADDR09	DDR_PA9
DDR_PD10	MEMDATA10	MEMADDR10	DDR_PA10
DDR_PD11	MEMDATA11	MEMADDR11	DDR_PA11
DDR_PD12	MEMDATA12	MEMADDR12	DDR_PA12
DDR_PD13	MEMDATA13	MEMADDR13	DDR_PA13
DDR_PD14	MEMDATA14		
DDR_PD15	MEMDATA15	BA0	DDR_PBA0
DDR_PD16	MEMDATA16	BA1	DDR_PBA1
DDR_PD17	MEMDATA17	BA2	DDR_PBA2
DDR_PD18	MEMDATA18		
DDR_PD19	MEMDATA19	RAS#	DDR_PRAS#
DDR_PD20	MEMDATA20	CAS#	DDR_PCAS#
DDR_PD21	MEMDATA21	WE#	DDR_PWE#
DDR_PD22	MEMDATA22		
DDR_PD23	MEMDATA23	DM0	DDR_PDM0
DDR_PD24	MEMDATA24	DM1	DDR_PDM1
DDR_PD25	MEMDATA25	DM2	DDR_PDM2
DDR_PD26	MEMDATA26	DM3	DDR_PDM3
DDR_PD27	MEMDATA27	DM4	DDR_PDM4
DDR_PD28	MEMDATA28	DM5	DDR_PDM5
DDR_PD29	MEMDATA29	DM6	DDR_PDM6
DDR_PD30	MEMDATA30	DM7	DDR_PDM7
DDR_PD31	MEMDATA31	DM8	DDR_PDM8
DDR_PD32	MEMDATA32		
DDR_PD33	MEMDATA33	DQS0	DDR_PDQS0
DDR_PD34	MEMDATA34	DQS1	DDR_PDQS1
DDR_PD35	MEMDATA35	DQS2	DDR_PDQS2
DDR_PD36	MEMDATA36	DQS3	DDR_PDQS3
DDR_PD37	MEMDATA37	DQS4	DDR_PDQS4
DDR_PD38	MEMDATA38	DQS5	DDR_PDQS5
DDR_PD39	MEMDATA39	DQS6	DDR_PDQS6
DDR_PD40	MEMDATA40	DQS7	DDR_PDQS7
DDR_PD41	MEMDATA41	DQS8	DDR_PDQS8
DDR_PD42	MEMDATA42		
DDR_PD43	MEMDATA43	MEMODT0	DDR_PODT0
DDR_PD44	MEMDATA44	MEMODT1	DDR_PODT1
DDR_PD45	MEMDATA45		
DDR_PD46	MEMDATA46	BANKSELA0	DDR_PCS0#
DDR_PD47	MEMDATA47	BANKSELA1	DDR_PCS1#
DDR_PD48	MEMDATA48		
DDR_PD49	MEMDATA49	MEMCLKEN	DDR_PCKE
DDR_PD50	MEMDATA50		
DDR_PD51	MEMDATA51	MEMCLKOUT	DDR_CLKOUT
DDR_PD52	MEMDATA52		
DDR_PD53	MEMDATA53	MEMCLKOUT#	DDR_CLKOUT#
DDR_PD54	MEMDATA54		
DDR_PD55	MEMDATA55		
DDR_PD56	MEMDATA56		
DDR_PD57	MEMDATA57		
DDR_PD58	MEMDATA58		
DDR_PD59	MEMDATA59		
DDR_PD60	MEMDATA60		
DDR_PD61	MEMDATA61		
DDR_PD62	MEMDATA62		
DDR_PD63	MEMDATA63		

ECC0	SVREF1A	PPC_ECC0
ECC1	SVREF1B	PPC_ECC1
ECC2	SVREF2A	PPC_ECC2
ECC3	SVREF2B	PPC_ECC3
ECC4		PPC_ECC4
ECC5		PPC_ECC5
ECC6		PPC_ECC6
ECC7		PPC_ECC7

DDR_CLKOUT

DDR_CLKOUT#

R813

500ps Loop

DDR_VREF_0V9

5V

1V8

C158 0.10F

C148 0.10F

C151 0.10F 0402

C152 0.10F 0402

C148 0.01F

Place parts as close to CPU as possible

U32

VIN

VLDOIN

VDDQSNS

S3

S5

GND

GND

VTT

VTTSNS

VTTREF

R230 10K

R229 10K

C459 .027F 10V

C456 .10UF 16V

C453 .100NF 10V

C457 .10UF 16V

C458 .10UF 16V

DDR_VTT

DDR_VREF_0V9

J8

22-6D	PPC_ECC7	168	DDR2_DIMM_CB7
22-6D	PPC_ECC6	167	DDR2_DIMM_CB6
22-7D	PPC_ECC5	162	DDR2_DIMM_CB5
22-7D	PPC_ECC4	161	DDR2_DIMM_CB4
22-7D	PPC_ECC3	49	DDR2_DIMM_CB3
22-7D	PPC_ECC2	48	DDR2_DIMM_CB2
22-7D	PPC_ECC1	43	DDR2_DIMM_CB1
22-7D	PPC_ECC0	42	DDR2_DIMM_CB0
DDR_PDQ63		236	DDR2_DIMM_DQ[63]
DDR_PDQ62		235	DDR2_DIMM_DQ[62]
DDR_PDQ61		230	DDR2_DIMM_DQ[61]
DDR_PDQ60		229	DDR2_DIMM_DQ[60]
DDR_PDQ59		117	DDR2_DIMM_DQ[59]
DDR_PDQ58		116	DDR2_DIMM_DQ[58]
DDR_PDQ57		111	DDR2_DIMM_DQ[57]
DDR_PDQ56		110	DDR2_DIMM_DQ[56]
DDR_PDQ55		227	DDR2_DIMM_DQ[55]
DDR_PDQ54		226	DDR2_DIMM_DQ[54]
DDR_PDQ53		218	DDR2_DIMM_DQ[53]
DDR_PDQ52		217	DDR2_DIMM_DQ[52]
DDR_PDQ51		108	DDR2_DIMM_DQ[51]
DDR_PDQ50		107	DDR2_DIMM_DQ[50]
DDR_PDQ49		99	DDR2_DIMM_DQ[49]
DDR_PDQ48		98	DDR2_DIMM_DQ[48]
DDR_PDQ47		215	DDR2_DIMM_DQ[47]
DDR_PDQ46		214	DDR2_DIMM_DQ[46]
DDR_PDQ45		209	DDR2_DIMM_DQ[45]
DDR_PDQ44		208	DDR2_DIMM_DQ[44]
DDR_PDQ43		96	DDR2_DIMM_DQ[43]
DDR_PDQ42		95	DDR2_DIMM_DQ[42]
DDR_PDQ41		90	DDR2_DIMM_DQ[41]
DDR_PDQ40		89	DDR2_DIMM_DQ[40]
DDR_PDQ39		206	DDR2_DIMM_DQ[39]
DDR_PDQ38		205	DDR2_DIMM_DQ[38]
DDR_PDQ37		200	DDR2_DIMM_DQ[37]
DDR_PDQ36		199	DDR2_DIMM_DQ[36]
DDR_PDQ35		87	DDR2_DIMM_DQ[35]
DDR_PDQ34		86	DDR2_DIMM_DQ[34]
DDR_PDQ33		81	DDR2_DIMM_DQ[33]
DDR_PDQ32		80	DDR2_DIMM_DQ[32]
DDR_PDQ31		159	DDR2_DIMM_DQ[31]
DDR_PDQ30		158	DDR2_DIMM_DQ[30]
DDR_PDQ29		153	DDR2_DIMM_DQ[29]
DDR_PDQ28		152	DDR2_DIMM_DQ[28]
DDR_PDQ27		40	DDR2_DIMM_DQ[27]
DDR_PDQ26		39	DDR2_DIMM_DQ[26]
DDR_PDQ25		34	DDR2_DIMM_DQ[25]
DDR_PDQ24		33	DDR2_DIMM_DQ[24]
DDR_PDQ23		150	DDR2_DIMM_DQ[23]
DDR_PDQ22		149	DDR2_DIMM_DQ[22]
DDR_PDQ21		144	DDR2_DIMM_DQ[21]
DDR_PDQ20		143	DDR2_DIMM_DQ[20]
DDR_PDQ19		31	DDR2_DIMM_DQ[19]
DDR_PDQ18		30	DDR2_DIMM_DQ[18]
DDR_PDQ17		25	DDR2_DIMM_DQ[17]
DDR_PDQ16		24	DDR2_DIMM_DQ[16]
DDR_PDQ15		141	DDR2_DIMM_DQ[15]
DDR_PDQ14		140	DDR2_DIMM_DQ[14]
DDR_PDQ13		132	DDR2_DIMM_DQ[13]
DDR_PDQ12		131	DDR2_DIMM_DQ[12]
DDR_PDQ11		22	DDR2_DIMM_DQ[11]
DDR_PDQ10		21	DDR2_DIMM_DQ[10]
DDR_PDQ9		13	DDR2_DIMM_DQ[9]
DDR_PDQ8		12	DDR2_DIMM_DQ[8]
DDR_PDQ7		129	DDR2_DIMM_DQ[7]
DDR_PDQ6		128	DDR2_DIMM_DQ[6]
DDR_PDQ5		123	DDR2_DIMM_DQ[5]
DDR_PDQ4		122	DDR2_DIMM_DQ[4]
DDR_PDQ3		10	DDR2_DIMM_DQ[3]
DDR_PDQ2		9	DDR2_DIMM_DQ[2]
DDR_PDQ1		4	DDR2_DIMM_DQ[1]
DDR_PDQ0		3	DDR2_DIMM_DQ[0]
		101	DDR2_DIMM_SA2
		240	DDR2_DIMM_SA1
		239	DDR2_DIMM_SA0
	PPC_DDR2_DIMM_SCL	120	DDR2_DIMM_SCL
	PPC_DDR2_DIMM_SDA	119	DDR2_DIMM_SDA

879160001

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA1	22-8L,22-9D
DDR2_DIMM_BA[1]	190	DDR_PBA2	22-8L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-8L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	NC	
DDR2_DIMM_CK_N[2]	221	NC	
DDR2_DIMM_CK_P[1]	137	NC	
DDR2_DIMM_CK_N[1]	138	NC	
DDR2_DIMM_CK_P[0]	185	DDR_CLKOUT	
DDR2_DIMM_CK_N[0]	186	DDR_CLKOUT#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-7L,22-8D
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-9D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D
ERR_OUT	55	PPC_DDR2_ERROR	
PAR_IN	68	PAR_IN	

C455 .5PF 50V

R226 49R9 4K7

PPC_DDR2_RESET_N

1-3B,1-4L,24-5J

TP4

TP5

DDR_VTT

DDR_PA15
DDR_PA14
DDR_PA13
DDR_PA12

RP24

DDR_PA11
DDR_PA10
DDR_PA9
DDR_PA8

RP23

DDR_PA7
DDR_PA6
DDR_PA5
DDR_PA4

RP22

DDR_PA3
DDR_PA2
DDR_PA1
DDR_PA0

RP21

CP26 CP28 CP29 CP30

GND

22-8K,22-9D DDR_PBA1
22-8K,22-9D DDR_PBA2
22-8K,22-9D DDR_PBA0
22-8K,22-9D DDR_PCAS#

RP25

22-7K,22-9D DDR_PRAS#
22-6K,22-8D DDR_PCKE
22-3K,22-9D DDR_PWE#
22-3K,22-8D DDR_PCS0#

RP26

22-3K,22-8D DDR_PCS1#
22-8D DDR_PODT0
22-8D DDR_PODT1

NC

RP19

CP31 CP32 CP33

J8

	237	VSS_64	
	234	VSS_63	
	231	VSS_62	
	228	VSS_61	
	225	VSS_60	
	222	VSS_59	
	219	VSS_58	
	216	VSS_57	
	213	VSS_56	
	210	VSS_55	
	207	VSS_54	
	204	VSS_53	
	201	VSS_52	
	198	VSS_51	
	169	VSS_50	
	166	VSS_49	
	163	VSS_48	
	160	VSS_47	
	157	VSS_46	
	154	VSS_45	
	151	VSS_44	
	148	VSS_43	
	145	VSS_42	
	142	VSS_41	
	139	VSS_40	
	136	VSS_39	
	133	VSS_38	
	130	VSS_37	
	127	VSS_36	
	124	VSS_35	
	121	VSS_34	
	118	VSS_33	
	115	VSS_32	
	112	VSS_31	
	109	VSS_30	
	106	VSS_29	
	103	VSS_28	
	100	VSS_27	
	97	VSS_26	
	94	VSS_25	
	91	VSS_24	
	88	VSS_23	
	85	VSS_22	
	82	VSS_21	
	79	VSS_20	
	66	VSS_19	
	65	VSS_18	
	50	VSS_17	
	47	VSS_16	
	44	VSS_15	
	41	VSS_14	
	38	VSS_13	
	35	VSS_12	
	32	VSS_11	
	29	VSS_10	
	26	VSS_9	
	23	VSS_8	
	20	VSS_7	
	17	VSS_6	
	14	VSS_5	
	11	VSS_4	
	8	VSS_3	
	5	VSS_2	
	2	VSS_1	

879160001

DDR_VREF_0V9

VREF 1

1V8

VDDSPD 238

1V8

VDD_11	197	
VDD_10	189	
VDD_9	187	
VDD_8	184	
VDD_7	178	
VDD_6	172	
VDD_5	69	
VDD_4	67	
VDD_3	64	
VDD_2	59	
VDD_1	53	

1V8

VDDQ_11	194	
VDDQ_10	191	
VDDQ_9	181	
VDDQ_8	175	
VDDQ_7	170	
VDDQ_6	78	
VDDQ_5	75	
VDDQ_4	72	
VDDQ_3	62	
VDDQ_2	56	
VDDQ_1	51	

GND

DDR_VREF_0V9

1V8

C432 100NF 10V

C433 .10NF 25V

C454 100NF 10V

C434 .10NF 25V

C430 100NF 10V

C443 .10NF 25V

C431 100NF 10V

C444 .10NF 25V

C436 100NF 10V

C445 .10NF 25V

C435 100NF 10V

C446 .10NF 25V

GND

C438 100NF 10V

C451 .10NF 25V

C437 100NF 10V

C452 .10NF 25V

C439 100NF 10V

C449 .10NF 25V

C440 100NF 10V

C450 .10NF 25V

C441 100NF 10V

C448 .10NF 25V

C442 100NF 10V

C447 .10NF 25V

PLACE NEAREST DDR2 MODULE PINS

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

ROACH/iBOB2	ROACH_PPC_DDR2
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-4-2007_15:06	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 22 OF 25

PWR_GOOD
1-4G,1-4G,1-5E,1-5G,17-3F,18-2F,24-8K

3V3

PWR_GOOD monitors the +1.0v, 1V5, 1V8, 2V5, and 3V3 supplies

D1 BAV70

R41 10K

R42 100

SPST SW1

C47 2.2UF

GND

U31 MIC2779R-29

R28 2.2K

R29 3.3K

RESET_PORW 6,11
1-29,1-3G,1-5L,24-8C,25-5G

C604 0.1UF

RESET_PB_POR#
1-4L,1-5G,24-8C

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_3V3_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz

U9 CY22381FX_8211

C48 18PF

22.1184MHZ

Y1

C49 18PF

R30 2.2K

R31 33

R32 33

R33 33

SEL_SYSCLK
1-3L,1-5G,24-7C

CLK_UART_11.0592MHZ
1-2L,1-4L,25-3B

CLK_SYS_33MHZ

CLK_CPLD_33MHZ
1-3G,1-4L,24-7C

C606 0.1UF

U1 SYSTEM INTERRUPTS 440EPX

RESET_PORW

CLK_TMRCLK
1-3L,1-5G,24-7C

R24 1K

SYSERR
1-3G,1-5L,24-7C

TEST POINT

TP5

R25 1K

PPC440EPX-NTA533T

R31 3.3K

R32 2.2K

R33 3.3K

R35 3.3K

IRQ0-9 have programmable polarity per section 10.5.7 (UIC0_PR) 440ep user manual

GETH0_INT#
1-4B,1-5G,20-4E

MONITOR_INT
1-5G,1-9E,2-1P

PCI_INTA#
1-4B,1-5G,19-4E,19-4G

STTM_ALERT
1-2L,1-5G,25-2B

GPIO44
1-5L

SX95T_TDI
1-5L,1-7C,16-2L

SX95T_TCK
1-5L,1-7C,16-2L

SX95T_TMS
1-5L,1-7C,16-2L

SX95T_TDO
1-5G,1-7G,16-2L

R01 1K

R02 1K

R03 1K

R04 1K

R05 1K

R23 1K

NO POP
RO1 - RO5

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible

CS1 18PF

12.00 MHZ

Y2

CS2 18PF

U24 CY27033FXA_8211

R34 2.2K

CLK_SEL_M66EN
1-3L,1-5G,24-7C

R54 33

R55 33

R57 33

R59 33

R510 33

CLK_PCI1_66/33MHZ
1-4B,1-5L,19-3C

CLK_PCI2_66/33MHZ
1-4B,1-5L,19-4B

CLK_GETH0_25MHZ
1-4B,1-5L,20-4B

CLK_USB2.0_48MHZ
1-3B,1-5L,21-2C

CLK_CPLD_50MHZ
1-3G,1-5L,24-7C

C607 0.1UF

C605 0.1UF

TRACE & JTAG CONNECTORS

P1 .12X H SMT

R36 10K

VCC_JTAG

R37 10K

R38 10K

R39 10K

R40 10K

23-2G CPU_TDO
CPU_TDI
CPU_TCK
CPU_TMS
CPU_HALT#
DEBUG_TRST#

C53 0.1UF

R29 33

R26 is for current limiting and should be <100 Ohms.

Critical placement and routing of the Trace connector and nets. Up to CPU frequency/4

U1 440EPX PROBEWatch JTAG

R27 2.2K

C54 0.1UF

CPU_HALT#

R12 0

R14 0

R15 0

R22 0

CPU_TRST#
1-3L,1-5G,24-7C

TRACE PORT

J1 JSUN F SMT

R18 0

R11 0

TRC_CLK 23-2E

R13 0

R16 0

R17 0

R18 0

R19 0

R20 0

R21 0

TRCES4 23-2E
TRCTS0 23-2E
TRCTS1 23-2E
TRCTS2 23-1E
TRCTS3 23-1E
TRCTS4 23-1E
TRCTS5 23-1E
TRCTS6 23-1E

DEBUG_TRST#
1-3G,1-5L,24-7C

Memory Bus

PADR[27:31]
1-11,1-3G,25-10B,25-10M

PADATA[0:7]
1-11,1-4L

PADD27
PADD28
PADD29
PADD30
PADD31
PDATA0
PDATA1
PDATA2
PDATA3
PDATA4
PDATA5
PDATA6
PDATA7

RESETS

CPU_TRSTn = '1' when JTAG_TRSTn = '1' and RESET_PDMn = '1' else '0';
see errata sheet

PADE_0n
1-2L,1-3G,25-6M,25-7B,25-9B
RESET_PDMn
1-2G,1-3G,1-5L,23-9J,25-5G
RESET_FB_PDMn
1-4L,1-5G,23-8E

CLOCKS

DEBUG_TRSTn
1-3G,1-5L,23-1F
CPU_TRSTn
1-3L,1-5G,23-2F
CLK_CPLD_33MHZ
1-3G,1-4L,23-6G
CLK_CPLD_33MHZ
1-3G,1-5L,23-4G
CLK_FXSCLK
1-2L,1-3G,25-6F
CLK_TMSCLKC
1-3L,1-5G,23-6H
CLK_SEL_PXSCHC
1-3L,1-5G,23-5D
SCL_SYSCLKC
1-3L,1-5G/23-7G
SYSERR
1-3G,1-5L/23-8H
FRY_BSY
1-2L,1-3G,25-7J
FWPHC
1-2G,1-3L,25-8J
EE1_WPC
1-2G,1-2L,25-1A
EE2_BOOT_WPC
1-2G,1-2L,25-5A
SYTH_AUC
1-2G,1-3L,25-1B

STATUS / MISC

FLASH

I2C

USB

Assertion of USB2_RESET may be asynchronous to CLK_USB2_CPLD
De-assertion of USB2_RESET must be synchronous to CLK_USB2_CPLD

NAND FLASH NOT USED

ETHERNET

GETH0_RSTn
1-4B,1-4L,20-4E

USB_EBC_MUX

RESET_CPLDnC
1-1G,1-3L,25-3J

roach_cpld_XC2C256_7VQ100C_pcb

NC	4	PAD4	
NC	7	PAD8	
NC	9	PAD10	
NC	10	PAD12	
NC	11	PAD15	
PDATA0	12	PAD16	
PDATA1	13	PAD17	
PDATA2	14	PAD18	
PDATA3	15	PAD19	
PDATA4	16	PAD20	
PDATA5	17	PAD21	
PDATA6	18	PAD23	
PDATA7	19	PAD28	
NC	20	PAD29	
NC	21	PAD30	
NC	22	PAD31	
NC	23	PAD32	
NC	24	PAD33	
NC	25	PAD34	
NC	26	PAD35	
NC	28	PAD44	
PCS_2	30	PAD48	
PDB9	31	PAD49	
PB_WE	32	PAD50	
	33	PAD52	
	34	PAD54	
	35	PAD55	
NC	38	PAD59	
	40	PAD64	
	41	PAD65	
	42	PAD66	
	43	PAD67	
	44	PAD68	
	45	PAD69	
	46	PAD70	
	48	PAD73	
	49	PAD74	
	50	PAD75	
	51	PAD76	
	52	PAD77	
	53	PAD81	
	54	PAD82	
NC	56	PAD86	
NC	57	PAD87	
NC	58	PAD88	
NC	59	PAD89	
NC	60	PAD90	
NC	61	PAD95	
NC	64	PAD100	
	66	PAD102	
NC	68	PAD105	
NC	69	PAD107	
	71	PAD108	
NC	70	PAD109	
NC	74	PAD112	
NC	75	PAD113	

	142	PAD217	
	140	PAD214	
	139	PAD213	
	138	PAD212	
	137	PAD211	CFG_DIP0
	136	PAD208	CFG_DIP1
	135	PAD207	CFG_DIP2
	134	PAD206	M66EN
	133	PAD204	
	132	PAD199	
	131	PAD197	
	130	PAD196	USER_LED0
	129	PAD195	USER_LED1
	128	PAD194	SYSERR#
	126	PAD192	RESET_BUFPOR#
	125	PAD191	SX95T_CCLK_0
	124	PAD190	SX95T_CS_B_0
	121	PAD187	SX95T_D_IN_0
	120	PAD186	SX95T_D_OUT_BUSY_0
	119	PAD178	SX95T_DONE_0
	118	PAD177	SX95T_INIT_B_0
	117	PAD176	SX95T_PROGRAM_B_0
	116	PAD175	SX95T_RDWR_B_0
CMD/DI	115	PAD173	
CLK/SCLK	114	PAD171	
	113	PAD169	
	112	PAD168	
	111	PAD167	
	110	PAD166	
	107	PAD163	
	106	PAD162	
	105	PAD161	
	104	PAD160	
	103	PAD158	
NC	102	PAD156	
NC	101	PAD154	
NC	100	PAD152	
NC	98	PAD146	
NC	97	PAD145	
NC	96	PAD144	
NC	95	PAD143	
NC	94	PAD142	
NC	92	PAD138	
NC	91	PAD137	
NC	88	PAD134	
	87	PAD133	
	86	PAD132	
	85	PAD131	
	83	PAD125	
NC	82	PAD121	
NC	81	PAD120	
NC	80	PAD119	
NC	79	PAD118	
NC	78	PAD117	
NC	77	PAD115	
NC	76	PAD114	

USER DIP-Swith

USER_DIP0
USER_DIP1
USER_DIP2
USER_DIP3

Boot Configuration

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

Configuration DIP-Swith

1-2G,1-3G,1-4E,19-2D,25-3B

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

1-2G,1-3L,25-1J
1-1G,1-3L,25-1J
1-1G,1-3L,25-1J

SysErr will be used to drive Status LED (active H)

PWR_GOOD
1-4D,1-4G,1-5E,1-5G,17-3F,18-2F,23-10G

J23

CMD/DI	2	DAT0/DO	7
CLK/SCLK	5	DAT1	8
		DAT2	9
VDD	4	DAT3	1
VSS1	3	DAT4	10
VSS2	6	DAT5	11
		DAT6	12
SW	14	DAT7	13
GND1	15		
GND2	16	MNT1	19NC
GND3	17	MNT2	20NC
GND4	18		

GMMC001LEU

DAT0/DO
DAT1
DAT2
DAT3
DAT4
DAT5
DAT6
DAT7

QDR2_BY0_1_SYS_RST_N
1-3L,1-8L,14-5J
QDR2_BY2_3_SYS_RST_N
1-4L,1-7L,15-5J
PPC_DDR2_RESET_N
1-3G,1-4L,22-3B
EXT_RESET#
1-1L,1-3G,25-6F

roach_cpld_XC2C256_7VQ100C_powerpins

VCC	1	GND_3	29
VAUX	8	GND_4	36
VCCIO_3	27	GND_5	47
VCC_1	37	GND_6	62
VCCIO_4	55	GND_7	72
VCCIO_5	73	GND_8	89
VCC_2	84	GND_9	90
VCCIO_6	93	GND_10	99
VCCIO	109	GND	108
VCCIO_1	127	GND_1	123
VCCIO_2	141	GND_2	144

U54

PLACE NEAR CPLD POWER PINS

PLACE NEAR CPLD JTAG CONNECTOR

roach_cpld_XC2C256_7VQ100C_configpins

NC	2	PAD1	
NC	3	PAD3	
NC	5	PAD5	
NC	6	PAD7	
NC	39	PAD62	
	63	TDI	
	65	TMS	
	67	TCK	
	122	TDO	
NC	143	PAD218	

U54

Xilinx
Programing Cable

JTAG

J22

	13	VREF	
	9	NC_0	
	3	NC_1	
TDO	7	TDI	5
		TMS	11
		TCK	9
GND_7	12		
GND_6	10		
GND_4	8		
GND_3	6		
GND_2	4		
GND_1	2		
GND_0	1		

R193 1K
R192 1K

ROACH/iBOB2	ROACH_PPC_CPLD
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-4-2007_15:06; PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 24 OF 25

ROACH/iBOB2	ROACH_PPC_NVM_SERIAL	
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
10-4-2007_15:06	DRAWN: F KAPP	APPR:
PATH PATH	CHECKED: E BAUERMEISTER	SHEET 25 OF 25