VIRTEX5

POWER SUPPLY AND MONITORING

ROACH_MONITOR

I2C0_SCLK	I2C0_SCLK	PPC_RESET	PPC_RESET
FAN2_SENSE	FAN2_SENSE	SYS_CONFIG[0:7]	SYS_CONFIG[0:7] 1-36,2-28,24-6B
FAN1_SENSE	FAN1_SENSE	TDI	PPC_THERMONA
FAN3_SENSE	FAN3_SENSE	ATRTN1	PPC_THERMONB
3V3_ATX	3V3_ATX	MONITOR_INT	MONITOR_INT
I2V5	I2V5	I2C0_33_DATA	I2C0_SDATA
I1V8	I1V8	PS_ON#	PS_ON#
I1V5	I1V5	ATRTN0	
I1V0	I1V0	TDO	TDO
5V_ATX	5V_ATX	FAN1_CONTROL	FAN1_CONTROL
MGT_AVCC_PG	MGT_AVCC_PG	LOAD_RES_OFF	LOAD_RES_OFF
MGT_AVTTX_PG	MGT_AVTTX_PG	2V5_TRACK	2V5_TRACK
MGT_AVCCPLL_PG	MGT_AVCCPLL_PG	2V5_INHIBIT	2V5_INHIBIT
PWR_OK	PWR_OK	FAN3_CONTROL	FAN3_CONTROL
12V_ATX	12V_ATX	FAN2_CONTROL	FAN2_CONTROL
		MGT_AVTTX_EN	MGT_AVTTX_EN
		MGT_AVCCPLL_EN	MGT_AVCCPLL_EN
		MGT_AVCC_EN	MGT_AVCC_EN
		1V8_INHIBIT	1V8_INHIBIT
		1V5_INHIBIT	1V5_INHIBIT
		1V0_INHIBIT	1V0_INHIBIT

2

ROACH_PSU

LOAD_RES_OFF	LOAD_RES_OFF	12V_ATX	12V_ATX
FAN1_CONTROL	FAN1_CONTROL	3V3_ATX	3V3_ATX
PS_ON#	PS_ON#	5V_ATX	5V_ATX
FAN2_CONTROL	FAN2_CONTROL	PWR_OK	PWR_OK
FAN3_CONTROL	FAN3_CONTROL		
1V0_INHIBIT	1V0_INHIBIT	FAN1_SENSE	FAN1_SENSE
1V5_INHIBIT	1V5_INHIBIT	FAN2_SENSE	FAN2_SENSE
1V8_INHIBIT	1V8_INHIBIT	FAN3_SENSE	FAN3_SENSE
2V5_TRACK	2V5_TRACK	I1V0	I1V0
2V5_INHIBIT	2V5_INHIBIT	I1V5	I1V5
		I1V8	I1V8
		I2V5	I2V5

3

VIRTEX5 CLOCKS

ROACH_V5_CLK

SX95T_DXN	ATRTN0	
SX95T_DXP		

7

ZDOK/ADC INTERFACE

ROACH_ADC_0

5

ROACH_ADC_1

6

V5 DDR2 MEMORY

ROACH_DDR2_DIMM

11

V5 DIFFERENTIAL GPIO

ROACH_DIFF_GPIO

12

V5 SE GPIO & MISCELLANEOUS

ROACH_GPIO_MISC

13

GIGABIT TRANSCEIVERS

ROACH_TRANSCEIVERS0_1

MGT_REFCLK_Q1_1_P	MGT_REFCLK_Q2_0_P
MGT_REFCLK_Q1_1_N	MGT_REFCLK_Q2_0_N
MGT_REFCLK_Q2_0_P	MGT_REFCLK_Q1_1_P
MGT_REFCLK_Q2_0_N	MGT_REFCLK_Q1_1_N

8

ROACH_TRANSCEIVERS2_3

MGT_REFCLK_Q2_0_P	MGT_REFCLK_Q2_0_P
MGT_REFCLK_Q2_0_N	MGT_REFCLK_Q2_0_N
MGT_REFCLK_Q1_1_P	MGT_REFCLK_Q1_1_P
MGT_REFCLK_Q1_1_N	MGT_REFCLK_Q1_1_N

9

ROACH_TRANSCEIVERS_PSU

MGT_AVCC_EN	MGT_AVCC_EN	MGT_AVCC_PG	MGT_AVCC_PG
MGT_AVCCPLL_EN	MGT_AVCCPLL_EN	MGT_AVTTX_PG	MGT_AVTTX_PG
MGT_AVTTX_EN	MGT_AVTTX_EN	MGT_AVCCPLL_PG	MGT_AVCCPLL_PG

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QDRII+ MEMORY

ROACH_QDR2P_BY0_1

QDR2_TDI	QDR2_BY0_1_TDO
QDR2_TCK	
QDR2_TMS	

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ROACH_QDR2P_BY2_3

QDR2_BY0_1_TDO	QDR2_BY2_3_TDO
QDR2_TMS	
QDR2_TCK	

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QDR2_BY0_1_TDO

QDR2_BY2_3_TDO

QDR2_TDI

QDR2_TCK

QDR2_TMS

P6
2x5
.1IN H SMT

1	2
3	4
5	6
7	8
9	10
11	12
13	14
15	16

R161 10K

R162 10K

R163 10K

R164 33R

C614 100NF 10V

POWER SUPPLY AND MONITORING

ROACH_5V_POWER

4

V5 POWER

VIRTEX5 CONFIGURATION

ROACH_CONFIG

SX95T_D_IN_0	SX95T_D_IN_0	SX95T_M2_0	SX95T_M2_0
SX95T_TCK	SX95T_TCK	SX95T_M1_0	SX95T_M1_0
SX95T_TMS	SX95T_TMS	SX95T_M0_0	SX95T_M0_0
CPLD_TDO	CPLD_TDO	SX95T_DONE_0	SX95T_DONE_0
SX95T_ROWR_B_0	SX95T_ROWR_B_0	SX95T_DONE_0	SX95T_CCLK_0
SX95T_PROGRAM_B_0	SX95T_PROGRAM_B_0	SX95T_D_OUT_BUSY_0	SX95T_D_OUT_BUSY_0
SX95T_CS_B_0	SX95T_CS_B_0	SX95T_INIT_B_0	SX95T_INIT_B_0
		SX95T_TDO	SX95T_TDO

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PPC

ROACH_PPC_POWER_1

17

ROACH_PPC_POWER_2

18

ROACH_PPC_PCI

19

ROACH_PPC_ETH1

GETH0_RST#	GETH0_RST#	GMCMDIO	GMCMDIO
CLK_GETH0_25MHZ	CLK_GETH0_25MHZ	GMCMDCLK	GMCMDCLK
		GETH0_INT#	GETH0_INT#

20

ROACH_PPC_USB

CONTAINS GPIO TO CONFIG INTERFACE

		SX95T_D_OUT_BUSY_0	SX95T_D_OUT_BUSY_0
		SX95T_DONE_0	SX95T_DONE_0
		SX95T_INIT_B_0	SX95T_INIT_B_0
		SX95T_M0_0	SX95T_M0_0
		SX95T_M1_0	SX95T_M1_0
		SX95T_M2_0	SX95T_M2_0
		SX95T_PROGRAM_B_0	SX95T_PROGRAM_B_0
CLK_USB2_48MHZ	CLK_USB2_48MHZ		

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ROACH_PPC_DDR2

I2C0_SCLK	I2C0_SCLK	
I2C0_SDATA	I2C0_SDATA	
PPC_DDR2_RESET_N	PPC_DDR2_RESET_N	

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ROACH_PPC_NVM_SERIAL

SX95T_D_IN_0	SX95T_D_IN_0	V5_INT#	V5_INT#
CLK_UART_11_0592MHZ	CLK_UART_11_0592MHZ	SELECTMAP_CS	SELECTMAP_CS
		I2C0_SCLK	I2C0_SCLK
		I2C0_SDATA	I2C0_SDATA
EE1_WP	EE1_WP	STTM_ALERT	STTM_ALERT
STTM_AS	STTM_AS		
RESET_POR#	RESET_POR#	POE#	POE#
FWP#	FWP#	FRY_BY#	FRY_BY#
EE2_BOOT_WP	EE2_BOOT_WP	CLK_PERCLK	CLK_PERCLK
BOOT_CFG0	BOOT_CFG0	PWBE_0#	PWBE_0#
BOOT_CFG1	BOOT_CFG1	PR_WE	PR_WE
BOOT_CFG2	BOOT_CFG2	PCS_2	PCS_2
RESET_CPLD#	RESET_CPLD#	PDATA[0:31]	PDATA[0:31] 1-3M
PREADY	PREADY	PADD[2:31]	PADD[2:31] 1-3G,24-9B
		EXT_RESET#	EXT_RESET#

25

ROACH_PPC_TST_CLK_IO

		PPC_THERMONA	PPC_THERMONA
		PPC_THERMONB	PPC_THERMONB
CPLD_INT	CPLD_INT	GPIO44	GPIO44
GETH0_INT#	GETH0_INT#		
MONITOR_INT	MONITOR_INT	RESET_POR#	RESET_POR#
V5_INT#	V5_INT#	DEBUG_TRST#	DEBUG_TRST#
STTM_ALERT	STTM_ALERT		
RESET_PB_POR#	RESET_PB_POR#	CLK_GETH0_25MHZ	CLK_GETH0_25MHZ
PWR_GOOD	PWR_GOOD	CLK_USB2_48MHZ	CLK_USB2_48MHZ
CPU_TRST#	CPU_TRST#	CLK_CPLD_50MHZ	CLK_CPLD_50MHZ
CLK_SEL_M66EN	CLK_SEL_M66EN		
SEL_SYSCLK	SEL_SYSCLK	SYSERR	SYSERR
CLK_TMRCLK	CLK_TMRCLK	CLK_UART_11_0592MHZ	CLK_UART_11_0592MHZ
		CLK_CPLD_33MHZ	CLK_CPLD_33MHZ

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ROACH_PPC_CPLD

SX95T_TMS	SX95T_TMS	CPLD_TDO	CPLD_TDO
SX95T_TCK	SX95T_TCK		
SX95T_TDO	SX95T_TDO	GETH0_RST#	GETH0_RST#
		PPC_DDR2_RESET_N	PPC_DDR2_RESET_N
SYS_CONFIG[0:7] 1-16E,2-2H,24-6B	SYS_CONFIG[0:7]	CPLD_INT	CPLD_INT
		PDATA[0:7]	PDATA[0:7] 1-5L
PPC_RESET	PPC_RESET	RESET_PB_POR#	RESET_PB_POR#
PWR_GOOD	PWR_GOOD	SX95T_CCLK_0	SX95T_CCLK_0
EXT_RESET#	EXT_RESET#	STTM_AS	STTM_AS
RESET_POR#	RESET_POR#	EE2_BOOT_WP	EE2_BOOT_WP
PWBE_0#	PWBE_0#	EE1_WP	EE1_WP
PADD[27:31] 1-5L,24-9B	PADD[27:31]	CPU_TRST#	CPU_TRST#
SELECTMAP_CS	SELECTMAP_CS	SEL_SYSCLK	SEL_SYSCLK
FRY_BY#	FRY_BY#	CLK_SEL_M66EN	CLK_SEL_M66EN
SYSERR	SYSERR	CLK_TMRCLK	CLK_TMRCLK
CLK_CPLD_33MHZ	CLK_CPLD_33MHZ	SX95T_ROWR_B_0	SX95T_ROWR_B_0
DEBUG_TRST#	DEBUG_TRST#	FWP#	FWP#
CLK_PERCLK	CLK_PERCLK	RESET_CPLD#	RESET_CPLD#
CLK_CPLD_50MHZ	CLK_CPLD_50MHZ	PREADY	PREADY
PR_WE	PR_WE	SX95T_INIT_B_0	SX95T_INIT_B_0
PCE#	PCE#	SX95T_DONE_0	SX95T_DONE_0
PCS_2	PCS_2	SX95T_PROGRAM_B_0	SX95T_PROGRAM_B_0
SX95T_D_OUT_BUSY_0	SX95T_D_OUT_BUSY_0	SX95T_D_IN_0	SX95T_D_IN_0
M66EN	M66EN	SX95T_CS_B_0	SX95T_CS_B_0
SX95T_M2_0	SX95T_M0_0	BOOT_CFG0	BOOT_CFG0
SX95T_M1_0	SX95T_M1_0	BOOT_CFG1	BOOT_CFG1
SX95T_M0_0	SX95T_M2_0	BOOT_CFG2	BOOT_CFG2

24

PLACE OVER PLANE SPLIT AT BOTTOM OF PCB NEAR ADC CONNECTORS

2V5 — C294 C294 C294 C294 — 100NF 10V

5VAUX — C294 C294 C294 C294 — 100NF 10V

5V — C294 C294 C294 C294 — 100NF 10V

1V0 — C294 C294 C294 C294 — 100NF 10V

3V3_ATX — C414 C414 C414 C414 — 100NF 10V

3V3 — C414 C414 C414 C414 — 100NF 10V

1V8 — C398 C398 C398 C398 — 100NF 10V

12V — C398 C398 C398 C398 — 100NF 10V

GND

1V5 — C414 C414 C414 C414 — 100NF 10V

MECHANICAL

GND

H1 H2 H3 H4 H5 H6 H7 H8 H9 — 3.5X6.2X6MM

H10

H11

BOARD FIDUCIALS

PLACE TOP

PLACE BOTTOM

PLACE TOP ON BORDER TAB

PLACE BOTTOM ON BORDER TAB

NC= 1 1

FU1 FU2 FU3 FU4 FU5 FU6 FU9 FU8 FU7 FU12 FU11 FU10

LOGO'S

PLACEHOLDER FOR PCB MEERKAT LOGO

PLACEHOLDER FOR PCB CASPER LOGO

PLACEHOLDER FOR PCB ROACH LOGO

PLACEHOLDER FOR PCB NRAO LOGO

BOARD SERIAL NUMBER

CONTRIBUTORS

ETIENNE BAUERMEISTER
HENRY CHEN
STEVE DURAND
DAVID GEORGE
FRANCOIS KAPP
ALAN LANGMAN
GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2

ROACH_TOP

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

DOC NO	ROACH
REVISION	1.0.2
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	1 OF 25

11-27-2008_13:45

PATH PATH

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

TIE TO GROUND IF PLL'S ARE NOT USED

PLACE AT ACTEL 1V5 POWER PINS

PLACE AT ACTEL 3V3 POWER PINS

roach_AFS600_powerpins

roach_AFS600_configpins

roach_AFS600_pcb

XPORT - PLACE IN REAR I/O REGION
XP10010001-03R

TEMPERATURE DIODE HEADER

15-91-2200

15-91-2140

15-91-2080

N2520-6V0C-RB-WE

ACTEL JTAG CONNECTOR

2510-6002UB

ECX-306
32.768KHZ

TL7700CPSR

ADM3101EACPZ-REEL

74AVCH4T245DGVRE4

SN74LVC1G07DBVT

FJD3076TM

PB POWER SWITCH

KEY - REMOVE PIN

MONITOR RESET

DEFAULT GPIO DIRECTION: OUTPUT

REFERENCE RESISTOR/ADC VALUES

VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)	FOR 8 BIT ADC USING 2.56V REFERENCE: ADC COUNT AT MAX POWER	CURRENT/BIT (A)
12V	0R01	3.36	0.11	33	0.1
5V	0R0047	6.78	0.22	31	0.21
3V3	0R01	3.47	0.12	34	0.1
2V5	0R01	3.56	0.13	35	0.1
1V8	0R0022	12.91	0.37	28	0.45
1V5	0R0047	6.77	0.22	31	0.21
1V0	0R001	26.79	0.72	26	1.0

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

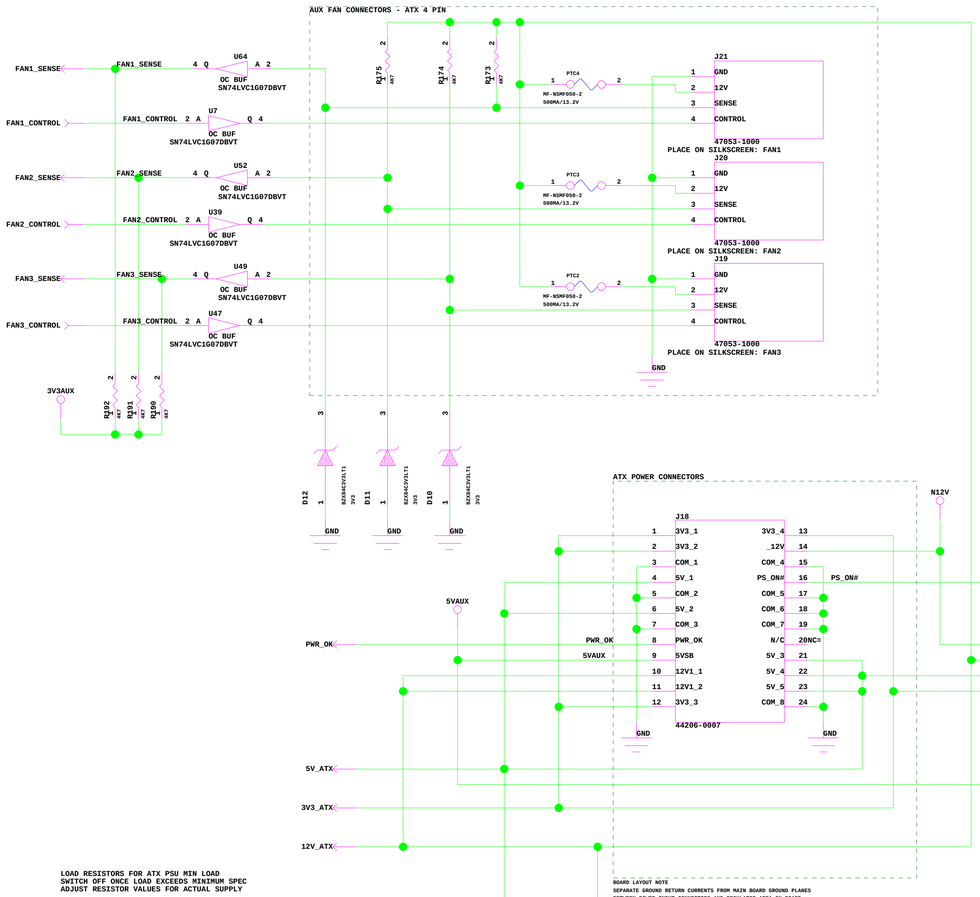
http://casper.berkeley.edu/

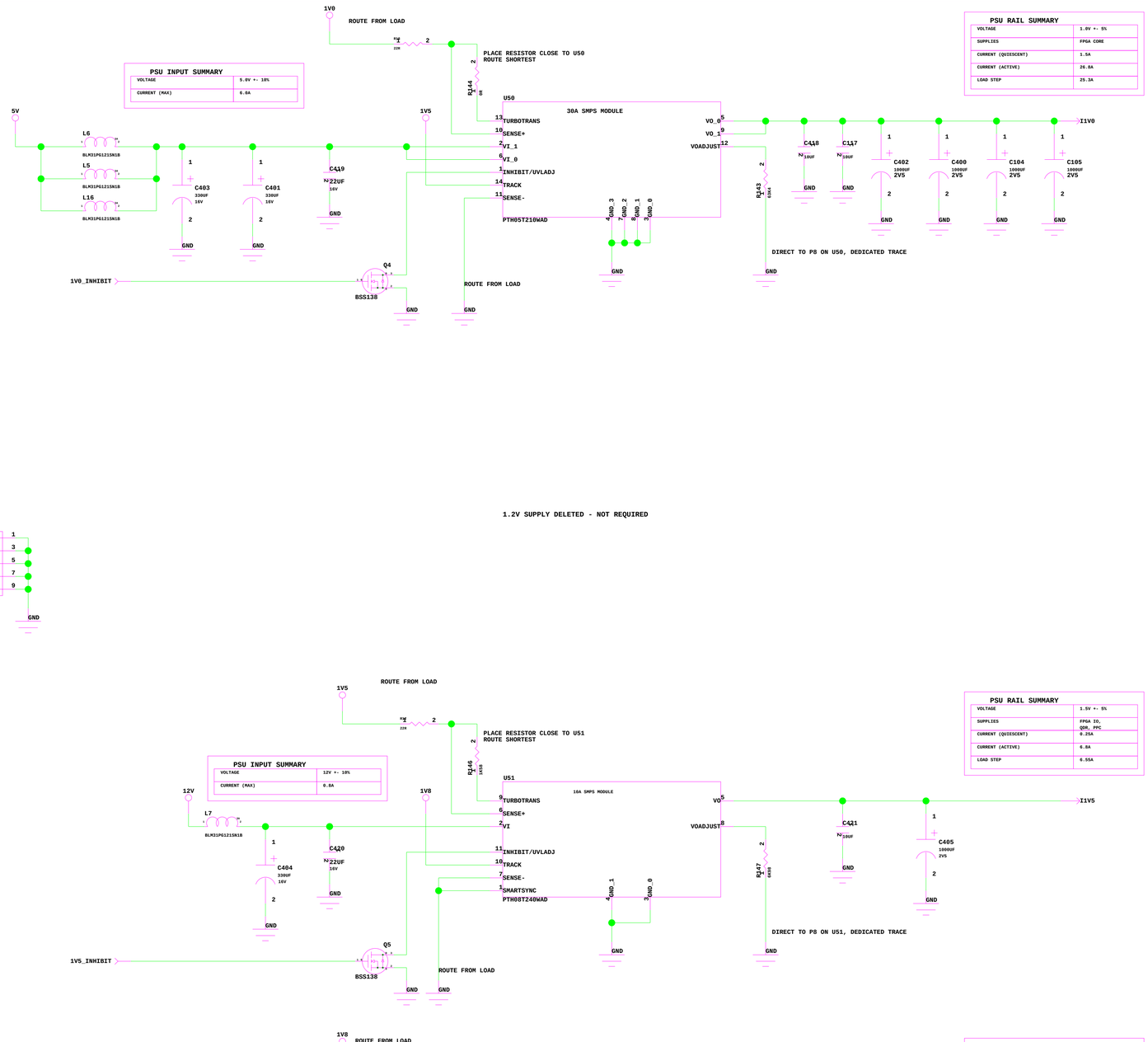
11-27-2008_13:45

PATH PATH

ROACH_MONITOR

DOC NO: NRF-ADM-XXX-SD-0001
REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET: 2 OF 25





ROACH/iBOB2

ROACH_PSU

COLLABORATORS:

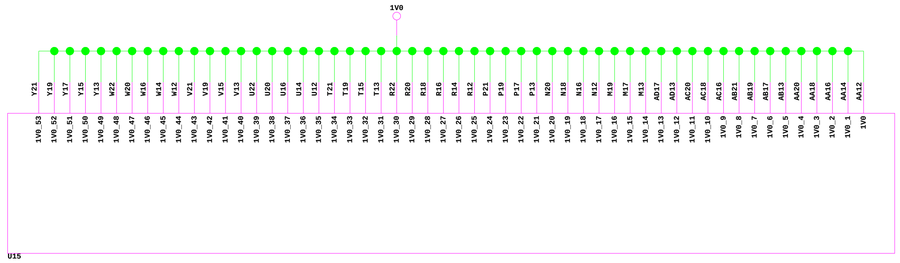
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

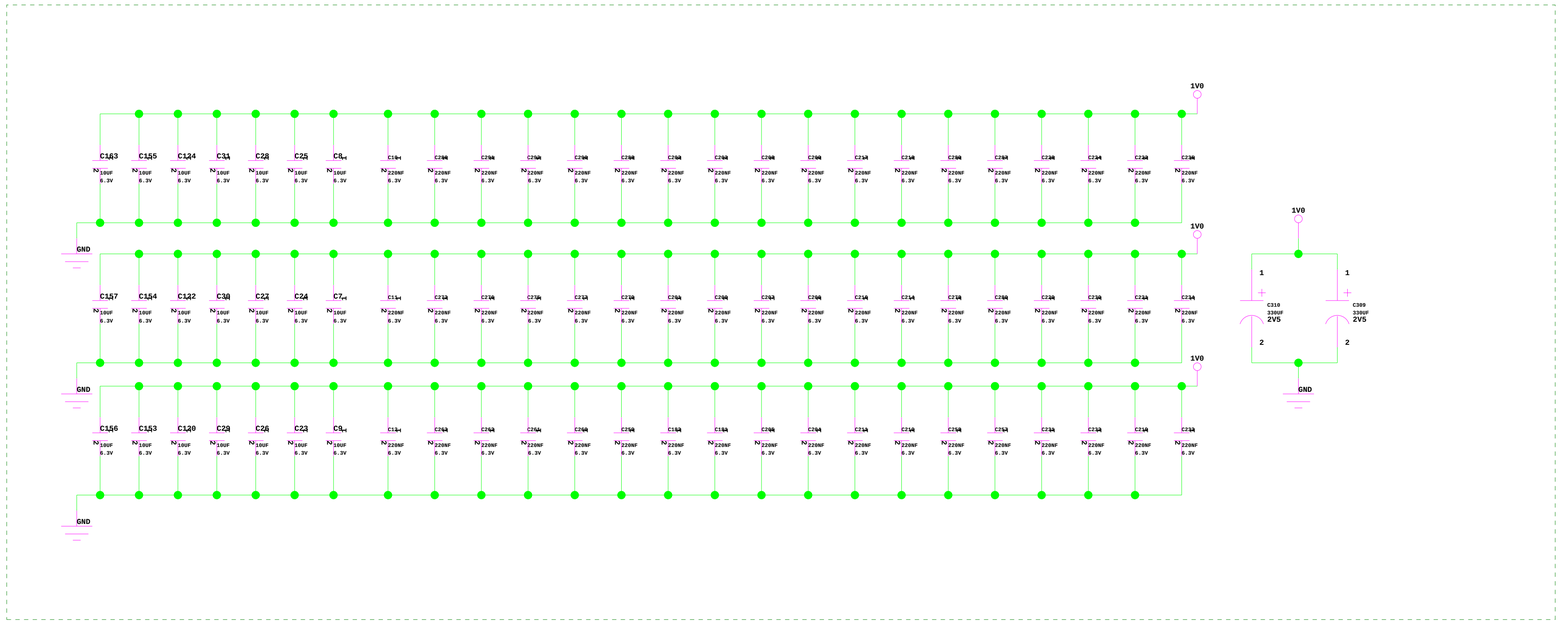
http://casper.berkeley.edu/

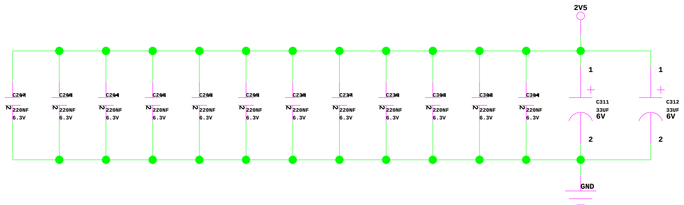
11-27-2008_13:45

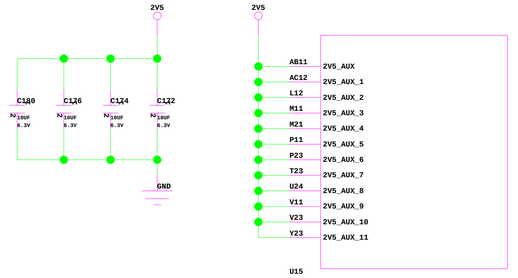
PATH PATH

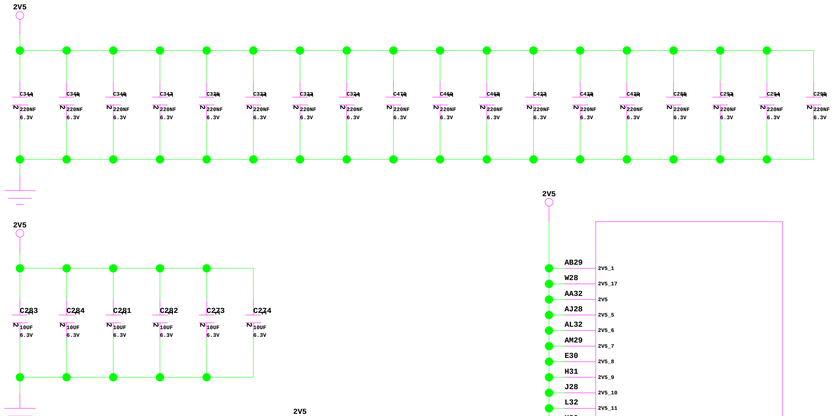
DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	3 OF 25

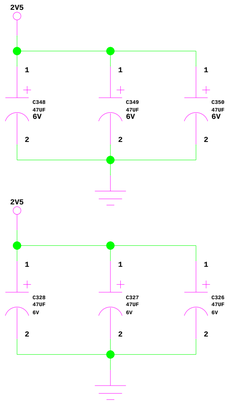




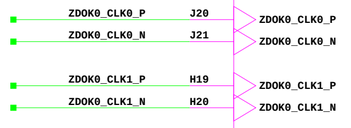


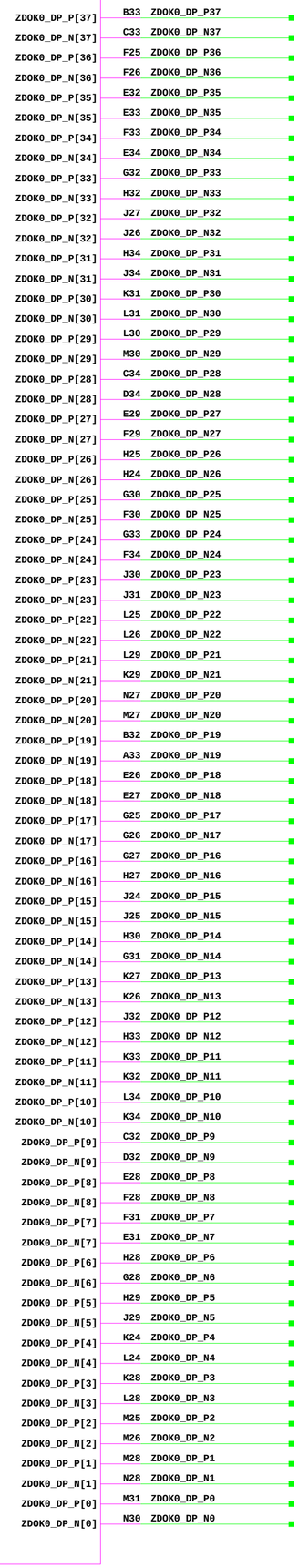


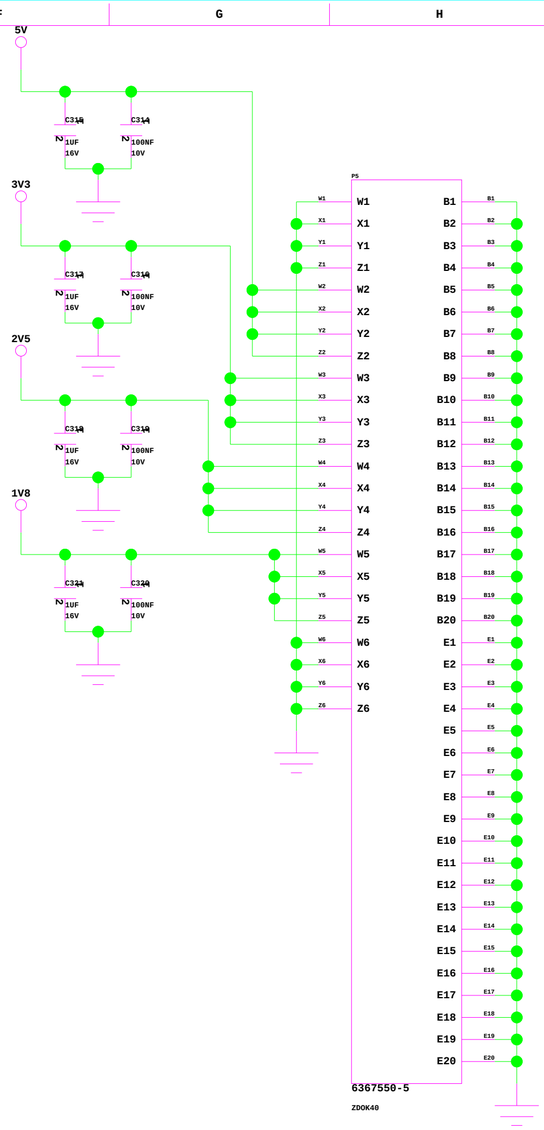


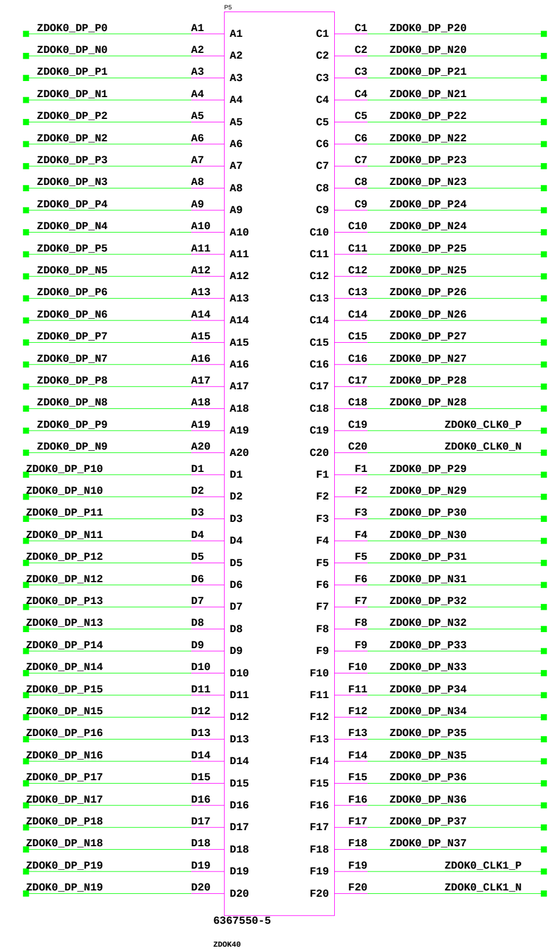


ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 4 OF 25
11-27-2008_13:45 PATH PATH	



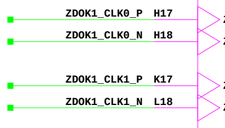


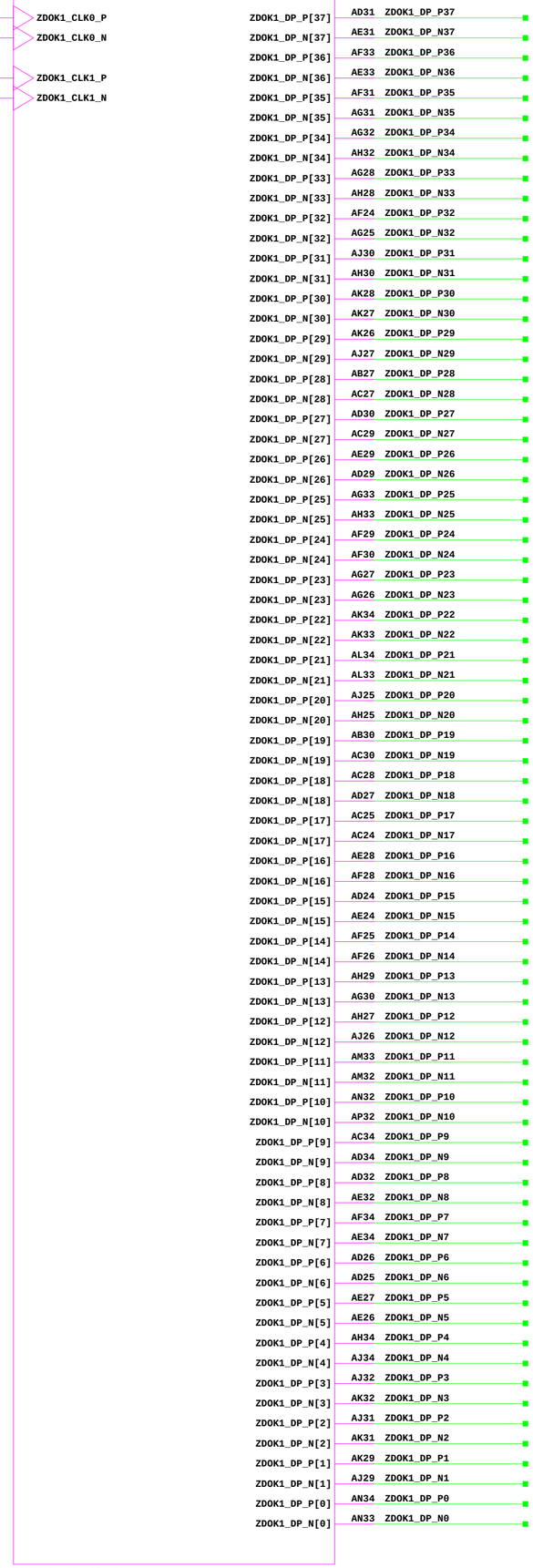


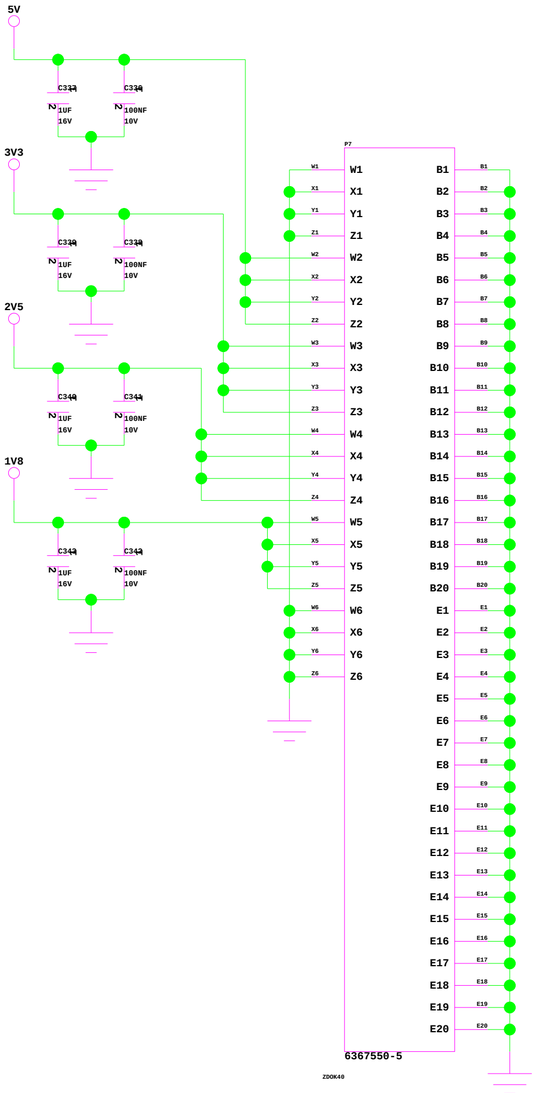


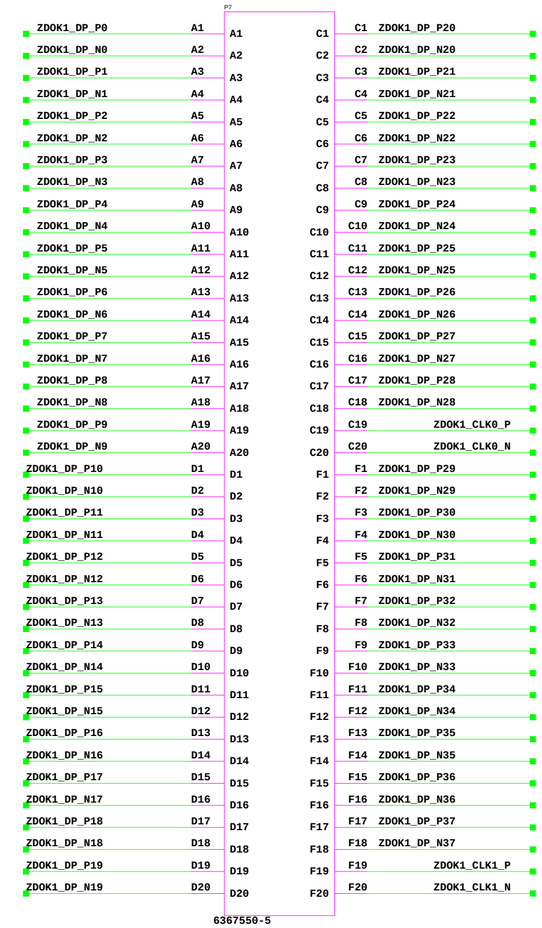
PLACE TEXT ON PCB: ZDOK0

ROACH/iBOB2	**ROACH_ADC_0**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR:
11-27-2008_13:45 PATH PATH	CHECKED: E BAUERMEISTER SHEET 5 OF 25



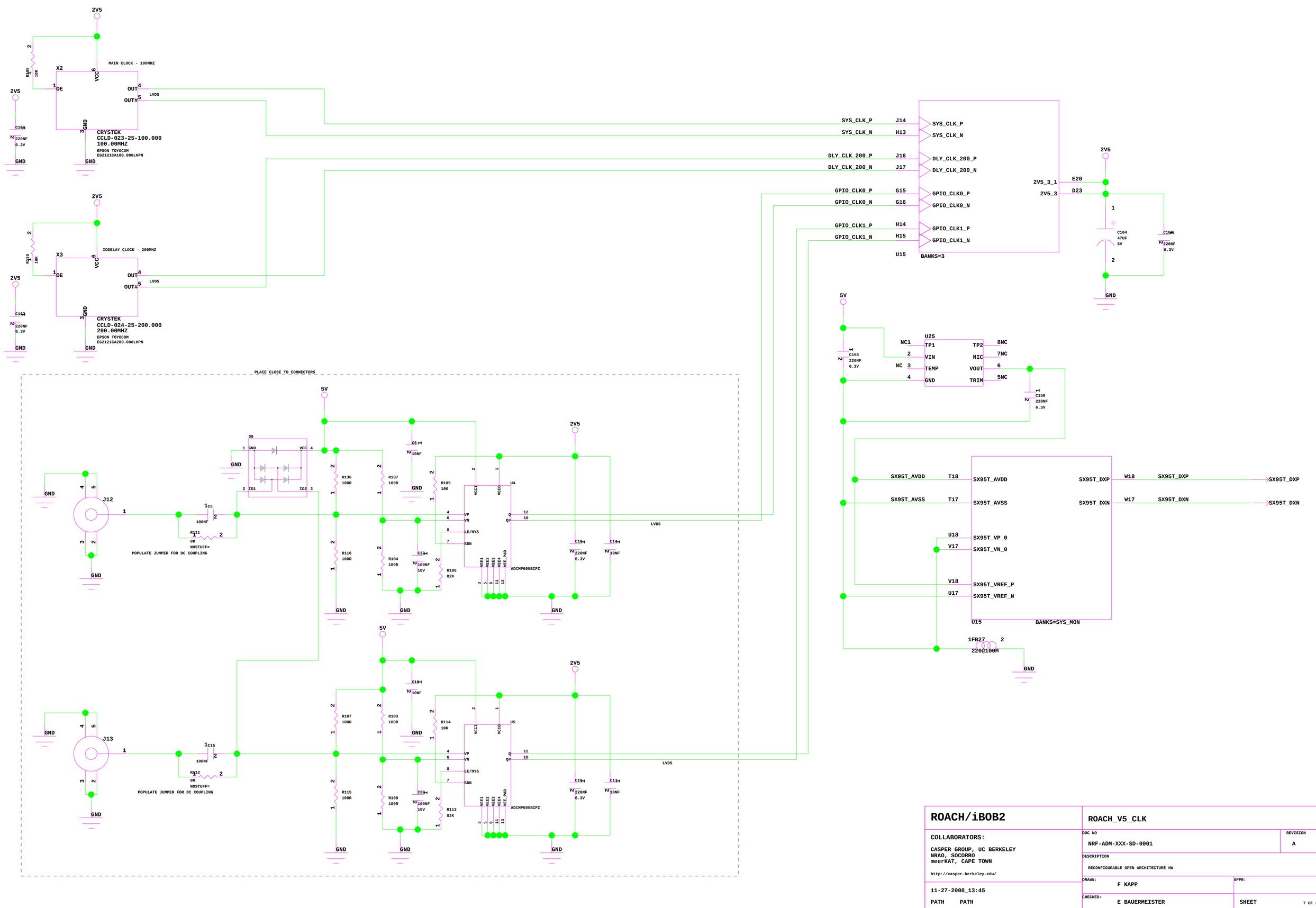






PLACE TEXT ON PCB: ZDOK1

ROACH/iBOB2	**ROACH_ADC_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET: 6 OF 25
11-27-2008_13:45 PATH PATH	



ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

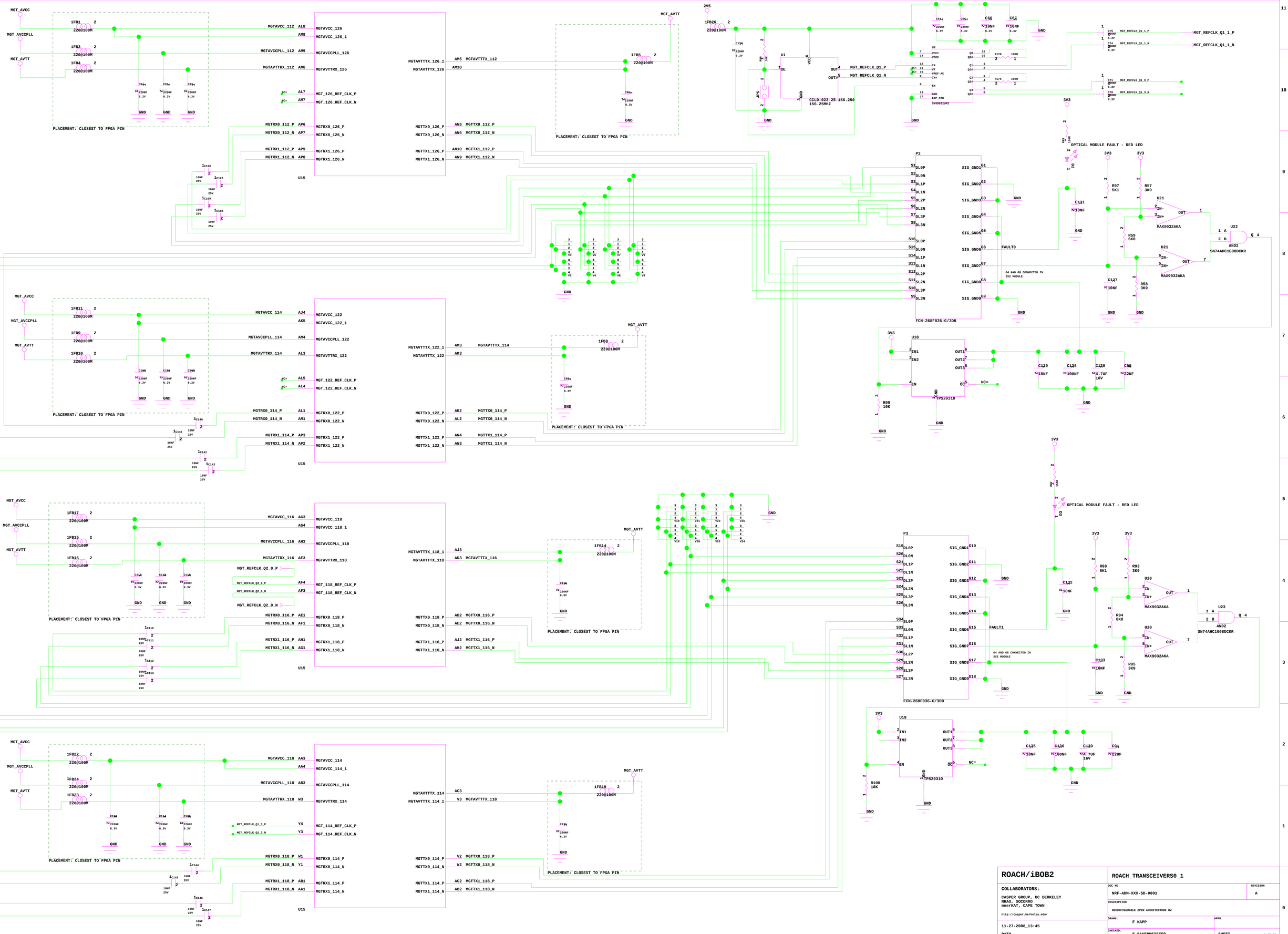
http://casper.berkeley.edu/

11-27-2008_13:45

PATH PATH

ROACH_V5_CLK

DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 7 OF 25


MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
1FB1 2 220@100M
1FB3 2 220@100M
1FB4 2 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_112 AL8 MGTAVCC_126
AM8 MGTAVCC_126_1
MGTAVCCPLL_112 AM9 MGTAVCCPLL_126
MGTAVTTRX_112 AM6 MGTAVTTRX_126
AL7 MGT_126_REF_CLK_P
AM7 MGT_126_REF_CLK_N
MGTRX0_112_P AP6 MGTRX0_126_P
MGTRX0_112_N AP7 MGTRX0_126_N
MGTRX1_112_P AP9 MGTRX1_126_P
MGTRX1_112_N AP8 MGTRX1_126_N
U15
MGTAVTTTX_126_1 AM5 MGTAVTTTX_112
MGTAVTTTX_126 AM10
MGTTX0_126_P AN5 MGTTX0_112_P
MGTTX0_126_N AN6 MGTTX0_112_N
MGTTX1_126_P AN10 MGTTX1_112_P
MGTTX1_126_N AN9 MGTTX1_112_N
1FB5 2 220@100M
2V5
1FB26 2 220@100M
X1
OUT MGT_REFCLK_Q1_P
OUT MGT_REFCLK_Q1_N
CCLD-023-25-156.250 156.25MHZ
SY89832UMI
MGT_REFCLK_Q1_1_P
MGT_REFCLK_Q1_1_N
MGT_REFCLK_Q1_3_P
MGT_REFCLK_Q1_3_N
P3
FCN-268F036-G/3DB
FAULT0
FAULT1
G4 AND G8 CONNECTED IN 2X2 MODULE
OPTICAL MODULE FAULT - RED LED
MAX9032AKA
SN74AHC1G08DCKR
TPS2031D
R100 10K
3V3
GND
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
1FB11 2 220@100M
1FB9 2 220@100M
1FB10 2 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_114 AJ4 MGTAVCC_122
AK5 MGTAVCC_122_1
MGTAVCCPLL_114 AM4 MGTAVCCPLL_122
MGTAVTTRX_114 AL3 MGTAVTTRX_122
AL5 MGT_122_REF_CLK_P
AL4 MGT_122_REF_CLK_N
MGTRX0_114_P AL1 MGTRX0_122_P
MGTRX0_114_N AM1 MGTRX0_122_N
MGTRX1_114_P AP3 MGTRX1_122_P
MGTRX1_114_N AP2 MGTRX1_122_N
U15
MGTAVTTTX_122_1 AM3 MGTAVTTTX_114
MGTAVTTTX_122 AK3
MGTTX0_122_P AK2 MGTTX0_114_P
MGTTX0_122_N AL2 MGTTX0_114_N
MGTTX1_122_P AN4 MGTTX1_114_P
MGTTX1_122_N AN3 MGTTX1_114_N
1FB8 2 220@100M
1FB19 2 220@100M
R99 10K
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
1FB17 2 220@100M
1FB15 2 220@100M
1FB16 2 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_116 AG3 MGTAVCC_118
AG4 MGTAVCC_118_1
MGTAVCCPLL_116 AH3 MGTAVCCPLL_118
MGTAVTTRX_116 AE3 MGTAVTTRX_118
MGT_REFCLK_Q2_0_P
MGT_REFCLK_Q2_0_N
AF4 MGT_118_REF_CLK_P
AF3 MGT_118_REF_CLK_N
MGTRX0_116_P AE1 MGTRX0_118_P
MGTRX0_116_N AF1 MGTRX0_118_N
MGTRX1_116_P AH1 MGTRX1_118_P
MGTRX1_116_N AG1 MGTRX1_118_N
U15
MGTAVTTTX_118_1 AJ3
MGTAVTTTX_118 AD3 MGTAVTTTX_116
MGTTX0_118_P AD2 MGTTX0_116_P
MGTTX0_118_N AE2 MGTTX0_116_N
MGTTX1_118_P AJ2 MGTTX1_116_P
MGTTX1_118_N AH2 MGTTX1_116_N
1FB14 2 220@100M
R98 5K1
R93 3K9
R94 6K8
R95 3K9
R97 5K1
RS7 3K9
RS9 6K8
RS8 3K9
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
1FB22 2 220@100M
1FB24 2 220@100M
1FB23 2 220@100M
PLACEMENT: CLOSEST TO FPGA PIN
MGTAVCC_118 AA3 MGTAVCC_114
AA4 MGTAVCC_114_1
MGTAVCCPLL_118 AB3 MGTAVCCPLL_114
MGTAVTTRX_118 W3 MGTAVTTRX_114
Y4 MGT_114_REF_CLK_P
Y3 MGT_114_REF_CLK_N
MGTRX0_118_P W1 MGTRX0_114_P
MGTRX0_118_N Y1 MGTRX0_114_N
MGTRX1_118_P AB1 MGTRX1_114_P
MGTRX1_118_N AA1 MGTRX1_114_N
U15
MGTAVTTTX_114 AC3
MGTAVTTTX_114_1 V3 MGTAVTTTX_118
MGTTX0_114_P V2 MGTTX0_118_P
MGTTX0_114_N W2 MGTTX0_118_N
MGTTX1_114_P AC2 MGTTX1_118_P
MGTTX1_114_N AB2 MGTTX1_118_N
1FB19 2 220@100M
R100 10K
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
11-27-2008_13:45
PATH
ROACH_TRANSCEIVERS0_1
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 8 OF 25

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

G4 AND G8 CONNECTED IN 2X2 MODULE

OPTICAL MODULE FAULT - RED LED

FCN-268F036-G/3DB

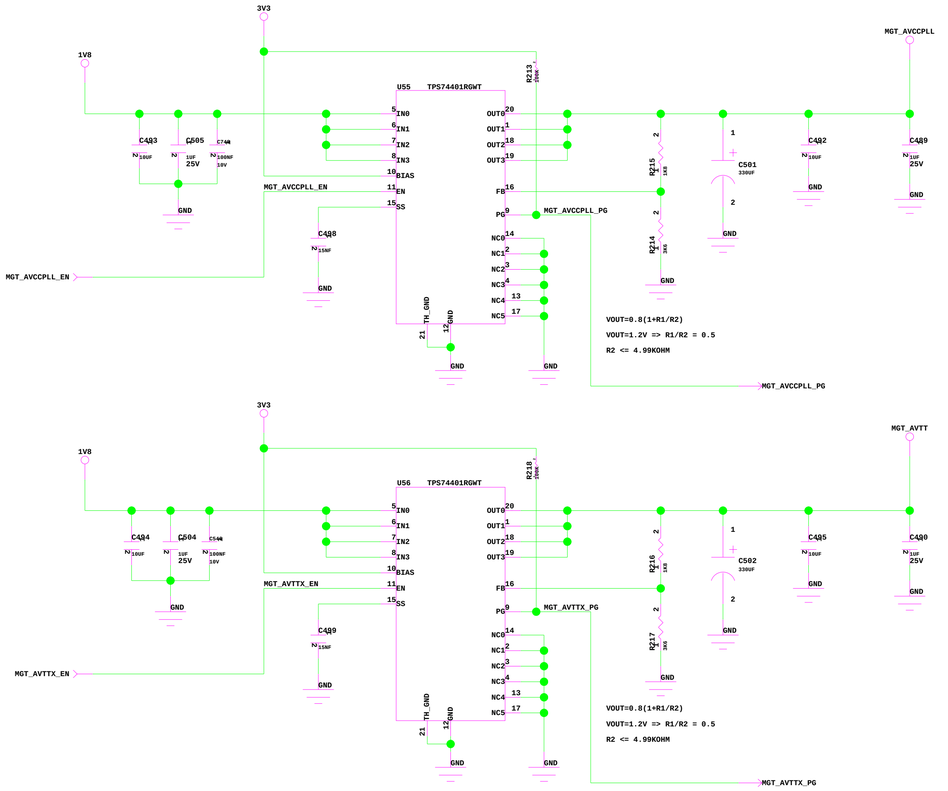
CCLD-023-25-156.250 156.25MHZ

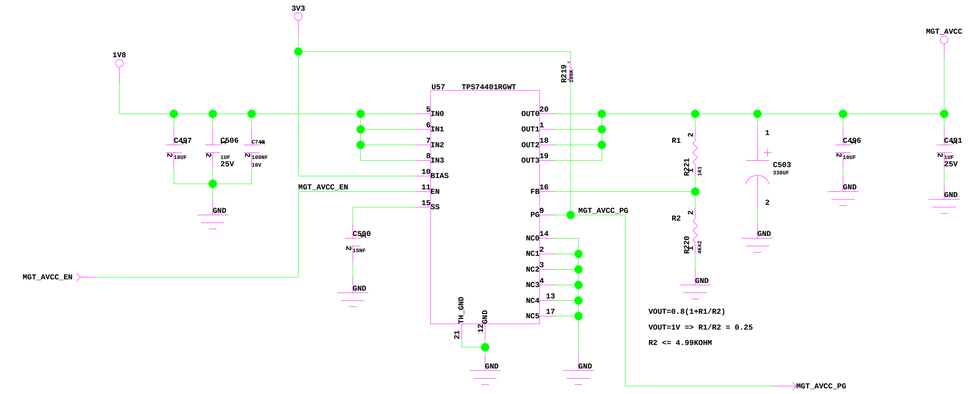
TPS2031D

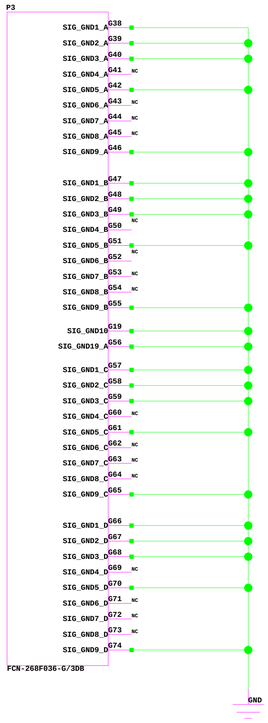
SN74AHC1G08DCKR

MAX9032AKA

ROACH/iBOB2	ROACH_TRANSCEIVERS2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A; DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45 PATH PATH	DRAWN: F KAPP; APPR: ; CHECKED: E BAUERMEISTER; SHEET 9 OF 25







ROACH/iBOB2	**ROACH_TRANSCEIVERS_PSU**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerkat, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR:
11-27-2008_13:45 PATH PATH	CHECKED: E BAUERMEISTER SHEET 10 OF 25

C364 C365 C366 220NF 6.3V

C388 C389 C390 C391 C392 C393 C394 C395 47UF 6V

1V8 GND

1V8 AK26 AL22 AK25 AJ8 AH11 AF7 W6 AG6 AB9 AK15 AK13 AJ18 1V8_25_2 1V8_25_1 1V8_25 1V8_22_2 1V8_22_1 1V8_22 1V8_18_2 1V8_18_1 1V8_18 1V8_6_2 1V8_6_1 1V8_6

DDR2_A15 AE7 DDR2_A[15]
DDR2_A14 AH7 DDR2_A[14]
DDR2_A13 AC4 DDR2_A[13]
DDR2_A12 AJ7 DDR2_A[12]
DDR2_A11 Y7 DDR2_A[11]
DDR2_A10 AD6 DDR2_A[10]
DDR2_A9 AK7 DDR2_A[9]
DDR2_A8 AK6 DDR2_A[8]
DDR2_A7 AC7 DDR2_A[7]
DDR2_A6 W6 DDR2_A[6]
DDR2_A5 AA6 DDR2_A[5]
DDR2_A4 AE6 DDR2_A[4]
DDR2_A3 Y6 DDR2_A[3]
DDR2_A2 AF6 DDR2_A[2]
DDR2_A1 AB6 DDR2_A[1]
DDR2_A0 AJ6 DDR2_A[0]

DDR2_BA2 AB7 DDR2_BA[2]
DDR2_BA1 AB5 DDR2_BA[1]
DDR2_BA0 AA5 DDR2_BA[0]

DDR2_CS_N_0 AM21 DDR2_CS_N_0
DDR2_CS_N_1 AN19 DDR2_CS_N_1

DDR2_CAS_N AD4 DDR2_CAS_N
DDR2_RAS_N AD5 DDR2_RAS_N

DDR2_DQS_0 AM26 DDR2_DQS_0
DDR2_DQS_N_0 AL26 DDR2_DQS_N_0
DDR2_DQS_1 AN25 DDR2_DQS_1
DDR2_DQS_N_1 AM25 DDR2_DQS_N_1
DDR2_DQS_2 AL21 DDR2_DQS_2
DDR2_DQS_N_2 AK21 DDR2_DQS_N_2
DDR2_DQS_3 AJ21 DDR2_DQS_3
DDR2_DQS_N_3 AJ20 DDR2_DQS_N_3
DDR2_DQS_4 AK11 DDR2_DQS_4
DDR2_DQS_N_4 AJ11 DDR2_DQS_N_4
DDR2_DQS_5 AD10 DDR2_DQS_5
DDR2_DQS_N_5 AD11 DDR2_DQS_N_5
DDR2_DQS_6 AE8 DDR2_DQS_6
DDR2_DQS_N_6 AD9 DDR2_DQS_N_6
DDR2_DQS_7 W7 DDR2_DQS_7
DDR2_DQS_N_7 V7 DDR2_DQS_N_7
DDR2_DQS_8 AJ16 DDR2_DQS_8
DDR2_DQS_N_8 AJ15 DDR2_DQS_N_8

DDR2_DM8 AN17 DDR2_DM[8]
DDR2_DM7 AM12 DDR2_DM[7]
DDR2_DM6 AG10 DDR2_DM[6]
DDR2_DM5 AA8 DDR2_DM[5]
DDR2_DM4 AK14 DDR2_DM[4]
DDR2_DM3 V9 DDR2_DM[3]
DDR2_DM2 AK23 DDR2_DM[2]
DDR2_DM1 AM27 DDR2_DM[1]
DDR2_DM0 AM30 DDR2_DM[0]

DDR2_CK_2_P AG8 DDR2_CK_2_P
DDR2_CK_2_N AH8 DDR2_CK_2_N
DDR2_CK_1_P AK16 DDR2_CK_1_P
DDR2_CK_1_N AL16 DDR2_CK_1_N
DDR2_CK_0_P AG5 DDR2_CK_0_P
DDR2_CK_0_N AF5 DDR2_CK_0_N

DDR2_CKE_1 AK12 DDR2_CKE_1
DDR2_CKE_0 AL11 DDR2_CKE_0
DDR2_ODT_1 AM20 DDR2_ODT_1
DDR2_ODT_0 AN20 DDR2_ODT_0
DDR2_WE_N AC5 DDR2_WE_N

DDR2_RESET_N AM18 DDR2_RESET_N
DDR2_PAR_IN AN18 DDR2_PAR_IN
DDR2_PAR_OUT AD7 DDR2_PAR_OUT

DDR2_DQ[71] AL14 DDR2_DQ71
DDR2_DQ[70] AN15 DDR2_DQ70
DDR2_DQ[69] AM16 DDR2_DQ69
DDR2_DQ[68] AL15 DDR2_DQ68
DDR2_DQ[67] AP15 DDR2_DQ67
DDR2_DQ[66] AL13 DDR2_DQ66
DDR2_DQ[65] AJ12 DDR2_DQ65
DDR2_DQ[64] AP16 DDR2_DQ64
DDR2_DQ[63] Y8 DDR2_DQ63
DDR2_DQ[62] W10 DDR2_DQ62
DDR2_DQ[61] U8 DDR2_DQ61
DDR2_DQ[60] Y11 DDR2_DQ60
DDR2_DQ[59] W9 DDR2_DQ59
DDR2_DQ[58] Y8 DDR2_DQ58
DDR2_DQ[57] Y10 DDR2_DQ57
DDR2_DQ[56] W11 DDR2_DQ56
DDR2_DQ[55] AK9 DDR2_DQ55
DDR2_DQ[54] AN9 DDR2_DQ54
DDR2_DQ[53] AB8 DDR2_DQ53
DDR2_DQ[52] AJ10 DDR2_DQ52
DDR2_DQ[51] AA9 DDR2_DQ51
DDR2_DQ[50] AA8 DDR2_DQ50
DDR2_DQ[49] AL10 DDR2_DQ49
DDR2_DQ[48] AC8 DDR2_DQ48
DDR2_DQ[47] AJ9 DDR2_DQ47
DDR2_DQ[46] AN13 DDR2_DQ46
DDR2_DQ[45] AC9 DDR2_DQ45
DDR2_DQ[44] AB10 DDR2_DQ44
DDR2_DQ[43] AM11 DDR2_DQ43
DDR2_DQ[42] AP12 DDR2_DQ42
DDR2_DQ[41] AN10 DDR2_DQ41
DDR2_DQ[40] AF9 DDR2_DQ40
DDR2_DQ[39] AG11 DDR2_DQ39
DDR2_DQ[38] AP14 DDR2_DQ38
DDR2_DQ[37] AE11 DDR2_DQ37
DDR2_DQ[36] AN14 DDR2_DQ36
DDR2_DQ[35] AF11 DDR2_DQ35
DDR2_DQ[34] AC10 DDR2_DQ34
DDR2_DQ[33] AA10 DDR2_DQ33
DDR2_DQ[32] AM13 DDR2_DQ32
DDR2_DQ[31] AM15 DDR2_DQ31
DDR2_DQ[30] AK18 DDR2_DQ30
DDR2_DQ[29] AP17 DDR2_DQ29
DDR2_DQ[28] AN23 DDR2_DQ28
DDR2_DQ[27] AK13 DDR2_DQ27
DDR2_DQ[26] AJ14 DDR2_DQ26
DDR2_DQ[25] AM17 DDR2_DQ25
DDR2_DQ[24] AL19 DDR2_DQ24
DDR2_DQ[23] AJ24 DDR2_DQ23
DDR2_DQ[22] AL20 DDR2_DQ22
DDR2_DQ[21] AK24 DDR2_DQ21
DDR2_DQ[20] AN24 DDR2_DQ20
DDR2_DQ[19] AJ22 DDR2_DQ19
DDR2_DQ[18] AK22 DDR2_DQ18
DDR2_DQ[17] AK19 DDR2_DQ17
DDR2_DQ[16] AJ19 DDR2_DQ16
DDR2_DQ[15] AN23 DDR2_DQ15
DDR2_DQ[14] AP27 DDR2_DQ14
DDR2_DQ[13] AN28 DDR2_DQ13
DDR2_DQ[12] AP29 DDR2_DQ12
DDR2_DQ[11] AN22 DDR2_DQ11
DDR2_DQ[10] AN22 DDR2_DQ10
DDR2_DQ[9] AP30 DDR2_DQ9
DDR2_DQ[8] AN28 DDR2_DQ8
DDR2_DQ[7] AM27 DDR2_DQ7
DDR2_DQ[6] AN29 DDR2_DQ6
DDR2_DQ[5] AL29 DDR2_DQ5
DDR2_DQ[4] AM31 DDR2_DQ4
DDR2_DQ[3] AN30 DDR2_DQ3
DDR2_DQ[2] AP31 DDR2_DQ2
DDR2_DQ[1] AL31 DDR2_DQ1
DDR2_DQ[0] AL30 DDR2_DQ0

DDR2_SDA AP19 DDR2_DIMM_SDA
DDR2_SCL AP20 DDR2_DIMM_SCL

J15

DDR2_DIMM_A[15] 173 DDR2_A15
DDR2_DIMM_A[14] 174 DDR2_A14
DDR2_DIMM_A[13] 196 DDR2_A13
DDR2_DIMM_A[12] 176 DDR2_A12
DDR2_DIMM_A[11] 57 DDR2_A11
DDR2_DIMM_A[10] 70 DDR2_A10
DDR2_DIMM_A[9] 177 DDR2_A9
DDR2_DIMM_A[8] 179 DDR2_A8
DDR2_DIMM_A[7] 58 DDR2_A7
DDR2_DIMM_A[6] 180 DDR2_A6
DDR2_DIMM_A[5] 60 DDR2_A5
DDR2_DIMM_A[4] 61 DDR2_A4
DDR2_DIMM_A[3] 182 DDR2_A3
DDR2_DIMM_A[2] 63 DDR2_A2
DDR2_DIMM_A[1] 183 DDR2_A1
DDR2_DIMM_A[0] 188 DDR2_A0

DDR2_DIMM_BA[2] 54 DDR2_BA2
DDR2_DIMM_BA[1] 190 DDR2_BA1
DDR2_DIMM_BA[0] 71 DDR2_BA0

DDR2_DIMM_CAS# 74 DDR2_CAS_N

DDR2_DIMM_RAS# 192 DDR2_RAS_N

DDR2_DIMM_CK_P[2] 220 DDR2_CK_2_P
DDR2_DIMM_CK_N[2] 221 DDR2_CK_2_N
DDR2_DIMM_CK_P[1] 137 DDR2_CK_1_P
DDR2_DIMM_CK_N[1] 138 DDR2_CK_1_N
DDR2_DIMM_CK_P[0] 185 DDR2_CK_0_P
DDR2_DIMM_CK_N[0] 186 DDR2_CK_0_N

DDR2_DIMM_CKE[1] 171 DDR2_CKE_1
DDR2_DIMM_CKE[0] 52 DDR2_CKE_0

DDR2_DIMM_DM_CB 164 DDR2_DM8
DDR2_DIMM_DM[7] 232 DDR2_DM7
DDR2_DIMM_DM[6] 223 DDR2_DM6
DDR2_DIMM_DM[5] 211 DDR2_DM5
DDR2_DIMM_DM[4] 202 DDR2_DM4
DDR2_DIMM_DM[3] 155 DDR2_DM3
DDR2_DIMM_DM[2] 146 DDR2_DM2
DDR2_DIMM_DM[1] 134 DDR2_DM1
DDR2_DIMM_DM[0] 125 DDR2_DM0

DDR2_DIMM_DQS_CB_P 46 DDR2_DQS_8
DDR2_DIMM_DQS_CB_N 45 DDR2_DQS_N_8
DDR2_DIMM_DQS_P[7] 114 DDR2_DQS_7
DDR2_DIMM_DQS_N[7] 113 DDR2_DQS_N_7
DDR2_DIMM_DQS_P[6] 105 DDR2_DQS_6
DDR2_DIMM_DQS_N[6] 104 DDR2_DQS_N_6
DDR2_DIMM_DQS_P[5] 93 DDR2_DQS_5
DDR2_DIMM_DQS_N[5] 92 DDR2_DQS_N_5
DDR2_DIMM_DQS_P[4] 84 DDR2_DQS_4
DDR2_DIMM_DQS_N[4] 83 DDR2_DQS_N_4
DDR2_DIMM_DQS_P[3] 37 DDR2_DQS_3
DDR2_DIMM_DQS_N[3] 36 DDR2_DQS_N_3
DDR2_DIMM_DQS_P[2] 28 DDR2_DQS_2
DDR2_DIMM_DQS_N[2] 27 DDR2_DQS_N_2
DDR2_DIMM_DQS_P[1] 16 DDR2_DQS_1
DDR2_DIMM_DQS_N[1] 15 DDR2_DQS_N_1
DDR2_DIMM_DQS_P[0] 7 DDR2_DQS_0
DDR2_DIMM_DQS_N[0] 6 DDR2_DQS_N_0

DDR2_DIMM_WE# 73 DDR2_WE_N

DDR2_DIMM_ODT[1] 77 DDR2_ODT_1
DDR2_DIMM_ODT[0] 195 DDR2_ODT_0

DDR2_DIMM_RESET# 18 DDR2_RESET_N

DDR2_DIMM_S#[1] 76 DDR2_CS_N_1
DDR2_DIMM_S#[0] 193 DDR2_CS_N_0

PAR_OUT 55 DDR2_PAR_OUT
PAR_IN 68 DDR2_PAR_IN

DDR2_DIMM_SA2 101
DDR2_DIMM_SA1 240
DDR2_DIMM_SA0 239
DDR2_DIMM_SCL 120
DDR2_DIMM_SDA 119

879160001

C434 C435 C436 5PF 50V

1V8 GND

18, 22, 6, 25 VDD_25 VDD_22 VDD_18 VDD_6 VDD

U15

AF24 AG24 AG9 AF8 AG6 AH5 AJ17 AK17 AF10 AG7 AL18 AL23 AL28 AM23 AM12 Y9 VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8

R156 R157 R154 R153 R152 R141 R155 R150 2 49.9R

GND

VREF_0V9 1V8

R133 2 4K7 R134 2 4K7 DDR2_DIMM_SCL DDR2_DIMM_SDA

GND

C354 C355 C356 C357 C358 C359 C360 C361 10NF 25V

GND

5V 1V8

C440 4U7F 10V C444 100NF 10V

GND GND

U33 TPS51100DGQ

10 VIN 2 VLDOIN 1 VDDQSNS 7 S3 9 S5 11 PPAD 3 GND 4 GND

R136 10K R135 10K 2

GND

VTT 3 VTTSNS 5 VTTREF 6

CONNECT VTTSNS POINT TO CENTRE OF VTT ISLAND

R138 120R 2

C441 100NF 10V C22 22PF C442 100NF 10V C443 100NF 10V

GND GND GND GND

VTT_0V9 VREF_0V9

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
PLACE ONE 10uF CAPACITOR ON EITHER END OF ISLAND

VTT_0V9

C234 100NF 16V

GND

DDR2_A15 DDR2_A14 DDR2_BA2 DDR2_A12 RP13 49.9R CP20 100NF
DDR2_A11 DDR2_A9 DDR2_A7 DDR2_A8 RP14 49.9R CP21 100NF
DDR2_A6 DDR2_A5 DDR2_A4 DDR2_A3 RP15 49.9R CP22 100NF
DDR2_A1 DDR2_A2 DDR2_A0 DDR2_A10 RP16 49.9R CP23 100NF
DDR2_BA1 DDR2_BA0 DDR2_RAS_N DDR2_CS_N_0 RP17 49.9R CP24 100NF
DDR2_WE_N DDR2_CAS_N DDR2_A13 DDR2_CS_N_1 RP18 49.9R CP25 100NF
NC= DDR2_CKE_1 DDR2_CKE_0 NC= RP20 49.9R CP27 100NF

GND

C234 100NF 16V

GND

R131 2 4K7 R132 2 4K7

GND

J15

VSS_64 VSS_63 VSS_62 VSS_61 VSS_60 VSS_59 VSS_58 VSS_57 VSS_56 VSS_55 VSS_54 VSS_53 VSS_52 VSS_51 VSS_50 VSS_49 VSS_48 VSS_47 VSS_46 VSS_45 VSS_44 VSS_43 VSS_42 VSS_41 VSS_40 VSS_39 VSS_38 VSS_37 VSS_36 VSS_35 VSS_34 VSS_33 VSS_32 VSS_31 VSS_30 VSS_29 VSS_28 VSS_27 VSS_26 VSS_25 VSS_24 VSS_23 VSS_22 VSS_21 VSS_20 VSS_19 VSS_18 VSS_17 VSS_16 VSS_15 VSS_14 VSS_13 VSS_12 VSS_11 VSS_10 VSS_9 VSS_8 VSS_7 VSS_6 VSS_5 VSS_4 VSS_3 VSS_2 VSS_1

879160001

GND

PLACE AT MODULE VREF PIN

VREF_0V9

C364 C365 220NF 6.3V C366 10NF 25V

GND

PLACE AT MODULE VDDSPD PIN

1V8

C364 220NF 6.3V

GND

PLACE AT MODULE VDD PINS

1V8

C364 C365 C366 C367 220NF 6.3V

GND

1V8

C364 C365 C366 C367 220NF 6.3V

GND

1V8

C364 C365 C366 220NF 6.3V

GND

VREF_0V9

VREF 1

1V8

VDDSPD 238

1V8

VDD_11 197 VDD_10 189 VDD_9 187 VDD_8 184 VDD_7 178 VDD_6 172 VDD_5 69 VDD_4 67 VDD_3 64 VDD_2 59 VDD_1 53

1V8

VDDQ_11 194 VDDQ_10 191 VDDQ_9 181 VDDQ_8 175 VDDQ_7 170 VDDQ_6 78 VDDQ_5 75 VDDQ_4 72 VDDQ_3 62 VDDQ_2 56 VDDQ_1 51

1V8

C364 C365 C366 C367 C368 C369 C370 C371 C372 C373 C374 220NF 6.3V

GND

PLACE AT MODULE VDDQ PINS

ROACH/iBOB2	**ROACH_DDR2_DIMM**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 11 OF 25
11-27-2008_13:45 PATH PATH	

ROACH/iBOB2	**ROACH_DIFF_GPIO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 12 OF 25

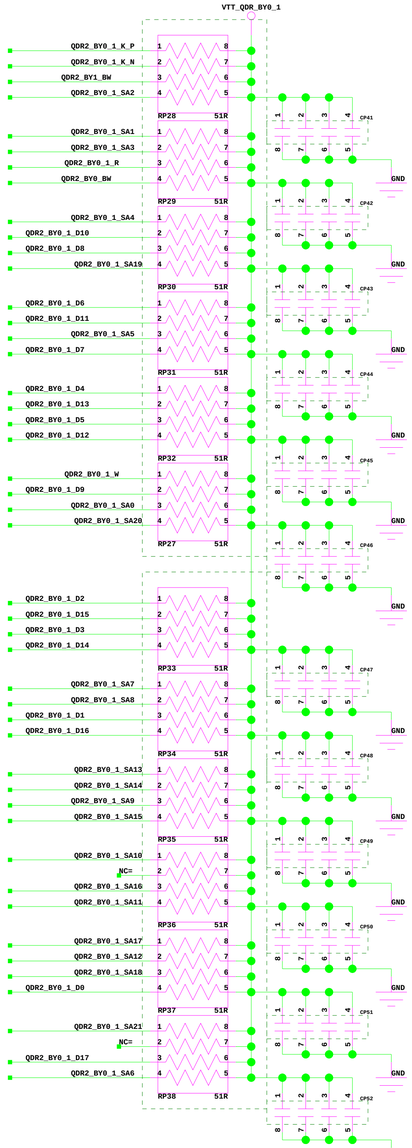
GPIOLVC33[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

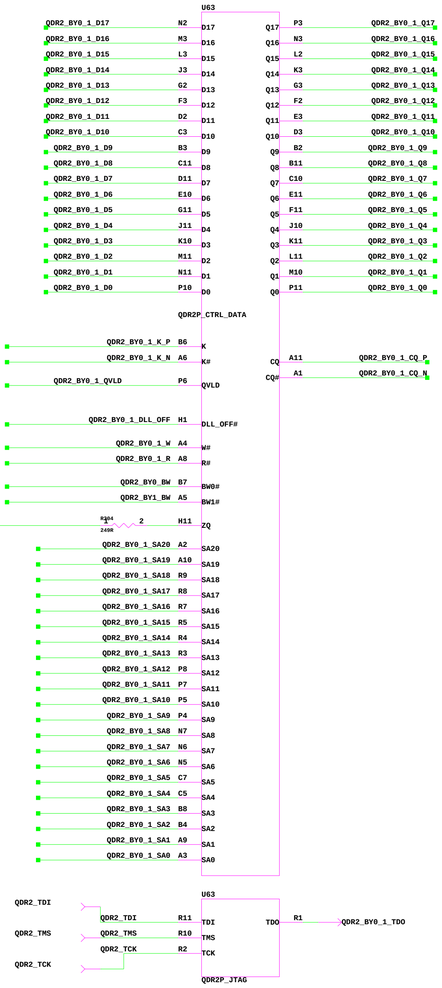
GPIOLVC33[3] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

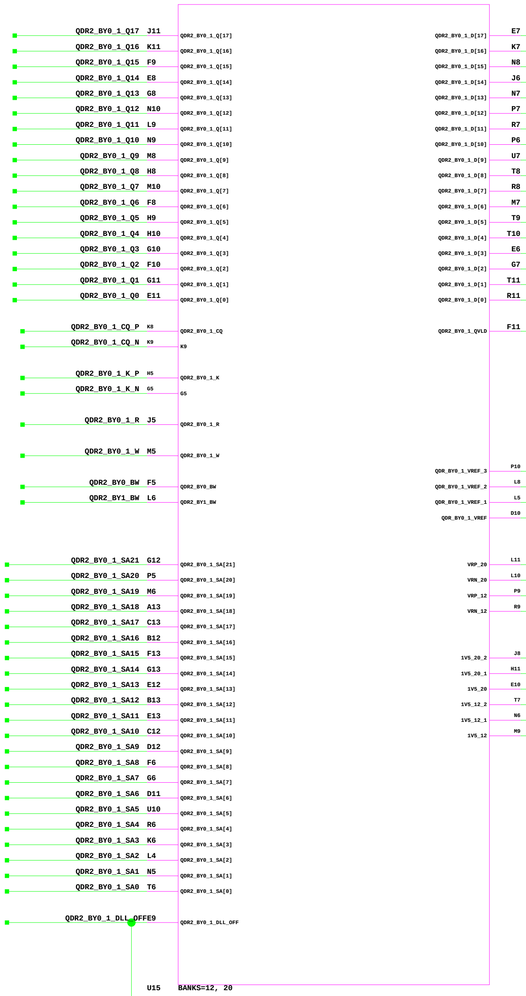
U15
BANKS=5, 11, 25

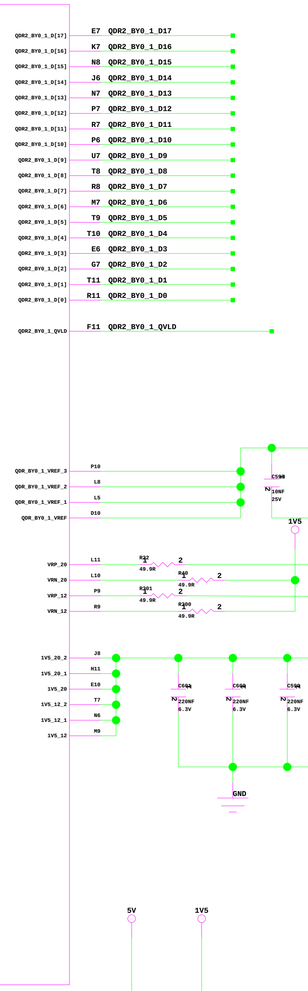
IF CR10 IS ON, CLOCK CAPABLE GPIO'S ARE OUTPUTS

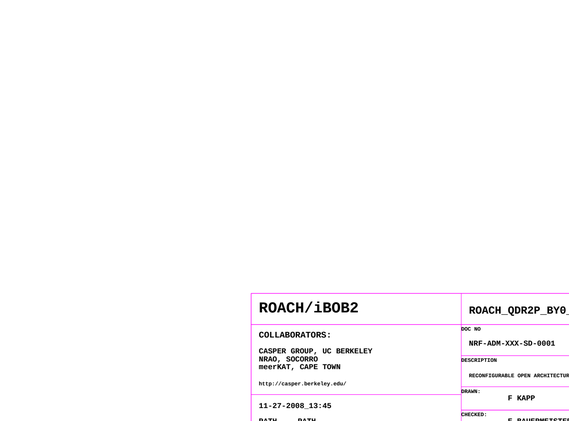
ROACH/iBOB2	ROACH_GPIO_MISC
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 13 OF 25

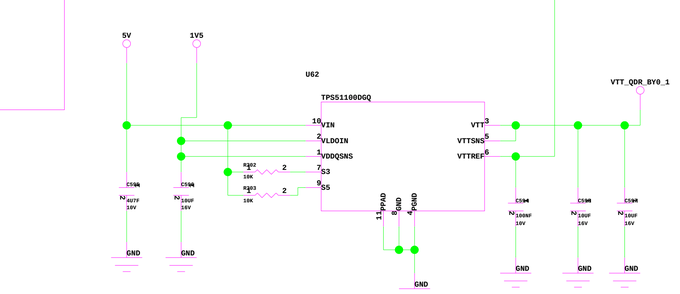


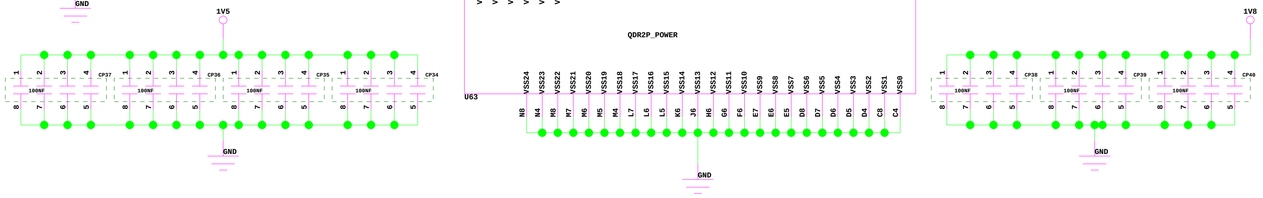












ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 14 OF 25
11-27-2008_13:45 PATH PATH	

VTT_QDR_BY2_3

QDR2_BY2_3_K_P
QDR2_BY2_3_K_N
QDR3_BW
QDR2_BY2_3_SA2
RP2 51R
QDR2_BY2_3_SA1
QDR2_BY2_3_SA3
QDR2_BY2_3_R
QDR2_BY2_BW
RP3 51R
QDR2_BY2_3_SA5
QDR2_BY2_3_D8
QDR2_BY2_3_SA4
QDR2_BY2_3_SA19
RP4 51R
QDR2_BY2_3_D6
QDR2_BY2_3_D11
QDR2_BY2_3_D7
QDR2_BY2_3_D10
RP5 51R
QDR2_BY2_3_D4
QDR2_BY2_3_D13
QDR2_BY2_3_D5
QDR2_BY2_3_D12
RP6 51R
QDR2_BY2_3_W
QDR2_BY2_3_D9
QDR2_BY2_3_SA0
QDR2_BY2_3_SA20
RP1 51R
CP8 CP9 CP10 CP11 CP12 CP13
GND

QDR2_BY2_3_D16
QDR2_BY2_3_D15
QDR2_BY2_3_D3
QDR2_BY2_3_D14
RP7 51R
QDR2_BY2_3_SA21
NC=
QDR2_BY2_3_D17
QDR2_BY2_3_SA6
RP8 51R
QDR2_BY2_3_SA17
QDR2_BY2_3_SA12
QDR2_BY2_3_SA18
QDR2_BY2_3_D0
RP9 51R
QDR2_BY2_3_SA10
NC=
QDR2_BY2_3_SA16
QDR2_BY2_3_SA11
RP10 51R
QDR2_BY2_3_SA13
QDR2_BY2_3_SA14
QDR2_BY2_3_SA9
QDR2_BY2_3_SA15
RP11 51R
QDR2_BY2_3_SA7
QDR2_BY2_3_SA8
QDR2_BY2_3_D1
QDR2_BY2_3_D2
RP12 51R
CP14 CP15 CP16 CP17 CP18 CP19
GND

U17

QDR2_BY2_3_D17	N2	D17	Q17 P3
QDR2_BY2_3_D16	M3	D16	Q16 N3
QDR2_BY2_3_D15	L3	D15	Q15 L2
QDR2_BY2_3_D14	J3	D14	Q14 K3
QDR2_BY2_3_D13	G2	D13	Q13 G3
QDR2_BY2_3_D12	F3	D12	Q12 F2
QDR2_BY2_3_D11	D2	D11	Q11 E3
QDR2_BY2_3_D10	C3	D10	Q10 D3
QDR2_BY2_3_D9	B3	D9	Q9 B2
QDR2_BY2_3_D8	C11	D8	Q8 B11
QDR2_BY2_3_D7	D11	D7	Q7 C10
QDR2_BY2_3_D6	E10	D6	Q6 E11
QDR2_BY2_3_D5	G11	D5	Q5 F11
QDR2_BY2_3_D4	J11	D4	Q4 J10
QDR2_BY2_3_D3	K10	D3	Q3 K11
QDR2_BY2_3_D2	M11	D2	Q2 L11
QDR2_BY2_3_D1	N11	D1	Q1 M10
QDR2_BY2_3_D0	P10	D0	Q0 P11

QDR2P_CTRL_DATA

QDR2_BY2_3_K_P	B6	K	
QDR2_BY2_3_K_N	A6	K#	
QDR2_BY2_3_QVLD	P6	QVLD	
QDR2_BY2_3_DLL_OFF	H1	DLL_OFF#	
QDR2_BY2_3_W	A4	W#	
QDR2_BY2_3_R	A8	R#	
QDR2_BY2_BW	B7	BW0#	
QDR2_BY3_BW	A5	BW1#	
RS1 240R	H11	ZQ	

QDR2_BY2_3_SA20	A2	SA20	
QDR2_BY2_3_SA19	A10	SA19	
QDR2_BY2_3_SA18	R9	SA18	
QDR2_BY2_3_SA17	R8	SA17	
QDR2_BY2_3_SA16	R7	SA16	
QDR2_BY2_3_SA15	R5	SA15	
QDR2_BY2_3_SA14	R4	SA14	
QDR2_BY2_3_SA13	R3	SA13	
QDR2_BY2_3_SA12	P8	SA12	
QDR2_BY2_3_SA11	P7	SA11	
QDR2_BY2_3_SA10	P5	SA10	
QDR2_BY2_3_SA9	P4	SA9	
QDR2_BY2_3_SA8	N7	SA8	
QDR2_BY2_3_SA7	N6	SA7	
QDR2_BY2_3_SA6	N5	SA6	
QDR2_BY2_3_SA5	C7	SA5	
QDR2_BY2_3_SA4	C5	SA4	
QDR2_BY2_3_SA3	B8	SA3	
QDR2_BY2_3_SA2	B4	SA2	
QDR2_BY2_3_SA1	A9	SA1	
QDR2_BY2_3_SA0	A3	SA0	

GND

CQ	A11	QDR2_BY2_3_CQ_P	
CQ#	A1	QDR2_BY2_3_CQ_N	

QDR2_BY2_3_CQ_P	C24	QDR2_BY2_3_CQ	
QDR2_BY2_3_CQ_N	D25		
QDR2_BY2_3_K_P	D14	QDR2_BY2_3_K	
QDR2_BY2_3_K_N	E14		
QDR2_BY2_3_R	C15	QDR2_BY2_3_R	
QDR2_BY2_3_W	F15	QDR2_BY2_3_W	
QDR2_BY2_BW	D15	QDR2_BY2_BW	
QDR3_BW	D16	QDR3_BW	

QDR2_BY2_3_SA21	D31	QDR2_BY2_3_SA[21]	
QDR2_BY2_3_SA20	F14	QDR2_BY2_3_SA[20]	
QDR2_BY2_3_SA19	A14	QDR2_BY2_3_SA[19]	
QDR2_BY2_3_SA18	D27	QDR2_BY2_3_SA[18]	
QDR2_BY2_3_SA17	A30	QDR2_BY2_3_SA[17]	
QDR2_BY2_3_SA16	B30	QDR2_BY2_3_SA[16]	
QDR2_BY2_3_SA15	C30	QDR2_BY2_3_SA[15]	
QDR2_BY2_3_SA14	B31	QDR2_BY2_3_SA[14]	
QDR2_BY2_3_SA13	D30	QDR2_BY2_3_SA[13]	
QDR2_BY2_3_SA12	B26	QDR2_BY2_3_SA[12]	
QDR2_BY2_3_SA11	A29	QDR2_BY2_3_SA[11]	
QDR2_BY2_3_SA10	B29	QDR2_BY2_3_SA[10]	
QDR2_BY2_3_SA9	A31	QDR2_BY2_3_SA[9]	
QDR2_BY2_3_SA8	G17	QDR2_BY2_3_SA[8]	
QDR2_BY2_3_SA7	C27	QDR2_BY2_3_SA[7]	
QDR2_BY2_3_SA6	C28	QDR2_BY2_3_SA[6]	
QDR2_BY2_3_SA5	E16	QDR2_BY2_3_SA[5]	
QDR2_BY2_3_SA4	E17	QDR2_BY2_3_SA[4]	
QDR2_BY2_3_SA3	A15	QDR2_BY2_3_SA[3]	
QDR2_BY2_3_SA2	B15	QDR2_BY2_3_SA[2]	
QDR2_BY2_3_SA1	C14	QDR2_BY2_3_SA[1]	
QDR2_BY2_3_SA0	B16	QDR2_BY2_3_SA[0]	
QDR2_BY2_3_DLL_OFF	D20	QDR2_BY2_3_DLL_OFF	

U15
R102 10K
BANKS=5, 23

QDR2_BY2_3_Q17	D26	QDR2_BY2_3_Q[17]	
QDR2_BY2_3_Q16	C25	QDR2_BY2_3_Q[16]	
QDR2_BY2_3_Q15	B25	QDR2_BY2_3_Q[15]	
QDR2_BY2_3_Q14	C23	QDR2_BY2_3_Q[14]	
QDR2_BY2_3_Q13	C22	QDR2_BY2_3_Q[13]	
QDR2_BY2_3_Q12	A23	QDR2_BY2_3_Q[12]	
QDR2_BY2_3_Q11	C20	QDR2_BY2_3_Q[11]	
QDR2_BY2_3_Q10	B20	QDR2_BY2_3_Q[10]	
QDR2_BY2_3_Q9	C19	QDR2_BY2_3_Q[9]	
QDR2_BY2_3_Q8	B18	QDR2_BY2_3_Q[8]	
QDR2_BY2_3_Q7	A19	QDR2_BY2_3_Q[7]	
QDR2_BY2_3_Q6	C18	QDR2_BY2_3_Q[6]	
QDR2_BY2_3_Q5	A20	QDR2_BY2_3_Q[5]	
QDR2_BY2_3_Q4	A21	QDR2_BY2_3_Q[4]	
QDR2_BY2_3_Q3	B21	QDR2_BY2_3_Q[3]	
QDR2_BY2_3_Q2	B22	QDR2_BY2_3_Q[2]	
QDR2_BY2_3_Q1	B23	QDR2_BY2_3_Q[1]	
QDR2_BY2_3_Q0	A24	QDR2_BY2_3_Q[0]	

QDR2_BY2_3_Q[17]	F24	QDR2_BY2_3_D17	
QDR2_BY2_3_Q[16]	F23	QDR2_BY2_3_D16	
QDR2_BY2_3_Q[15]	E23	QDR2_BY2_3_D15	
QDR2_BY2_3_Q[14]	E22	QDR2_BY2_3_D14	
QDR2_BY2_3_Q[13]	D22	QDR2_BY2_3_D13	
QDR2_BY2_3_Q[12]	E21	QDR2_BY2_3_D12	
QDR2_BY2_3_Q[11]	D21	QDR2_BY2_3_D11	
QDR2_BY2_3_Q[10]	F18	QDR2_BY2_3_D10	
QDR2_BY2_3_Q[9]	A16	QDR2_BY2_3_D9	
QDR2_BY2_3_Q[8]	B17	QDR2_BY2_3_D8	
QDR2_BY2_3_Q[7]	C17	QDR2_BY2_3_D7	
QDR2_BY2_3_Q[6]	D17	QDR2_BY2_3_D6	
QDR2_BY2_3_Q[5]	F16	QDR2_BY2_3_D5	
QDR2_BY2_3_Q[4]	E19	QDR2_BY2_3_D4	
QDR2_BY2_3_Q[3]	F20	QDR2_BY2_3_D3	
QDR2_BY2_3_Q[2]	G20	QDR2_BY2_3_D2	
QDR2_BY2_3_Q[1]	F21	QDR2_BY2_3_D1	
QDR2_BY2_3_Q[0]	G21	QDR2_BY2_3_D0	

QDR2_BY2_3_QVLD A25 QDR2_BY2_3_QVLD

VREF_QDR_BY2_3

QDR2_BY2_3_VREF_3 G18
QDR_BY2_3_VREF_2 F19
QDR_BY2_3_VREF_1 A28
QDR_BY2_3_VREF A18
C59 10NF 25V

VRP_5 D19 RS1 49.9R
VRN_5 E18 RS2 49.9R
VRP_23 B28 RS11 49.9R
VRN_23 C29 RS12 49.9R
1V5
GND

1V5_5_2 F17
1V5_5_1 C16
1V5_5 B19
1V5_23_2 G24
1V5_23_1 F27
1V5_23 C26
C54 220NF 6.3V
C88 470UF 6V
C89 470UF 6V

5V 1V5

U16

VIN	10		
VLDOIN	2		
VDDQSNS	1		
S3	7		
S5	9		
VTT	3	VTT_QDR_BY2_3	
VTTSNS	5		
VTTREF	6		
PGND	11		
GND	8		
PGND	4		

R83 10K
R84 10K
C58 AUTO 10V
C57 100NF 10V
C53 100NF 10V
C84 100NF 10V
C85 100NF 10V
GND

GND and PGND (Power GND) should be isolated, with a single point connection between them.

QDR2_BY0_1_TDO
QDR2_TMS
QDR2_TCK

U17

QDR2_BY0_1_TDO	R11	TDI	TDO R1 QDR2_BY2_3_TDO
QDR2_TMS	R10	TMS	
QDR2_TCK	R2	TCK	
		QDR2P_JTAG	

1V5 1V8 VREF_QDR_BY2_3

QDR2P_POWER

VDDQ15 L8
VDDQ14 L4
VDDQ13 K8
VDDQ12 K4
VDDQ11 J8
VDDQ10 J4
VDDQ9 H9
VDDQ8 H8
VDDQ7 H4
VDDQ6 H3
VDDQ5 G8
VDDQ4 G4
VDDQ3 F8
VDDQ2 F4
VDDQ1 E8
VDDQ0 E4
VDD9 K7
VDD8 K5
VDD7 J7
VDD6 J5
VDD5 H7
VDD4 H5
VDD3 G7
VDD2 G5
VDD1 F7
VDD0 F5
VREF1 H2
VREF0 H10

VSS24 N8
VSS23 M8
VSS22 M4
VSS21 M7
VSS20 M6
VSS19 M5
VSS18 M4
VSS17 L7
VSS16 L6
VSS15 L5
VSS14 K6
VSS13 J6
VSS12 H6
VSS11 G6
VSS10 F6
VSS9 E7
VSS8 E6
VSS7 E5
VSS6 D8
VSS5 D7
VSS4 D6
VSS3 D5
VSS2 D4
VSS1 C8
VSS0 C4

U17

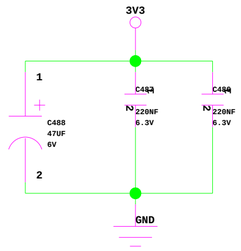
CP1 CP2 CP3 CP4 CP5 CP6 CP7
100NF
1V5 1V8
GND

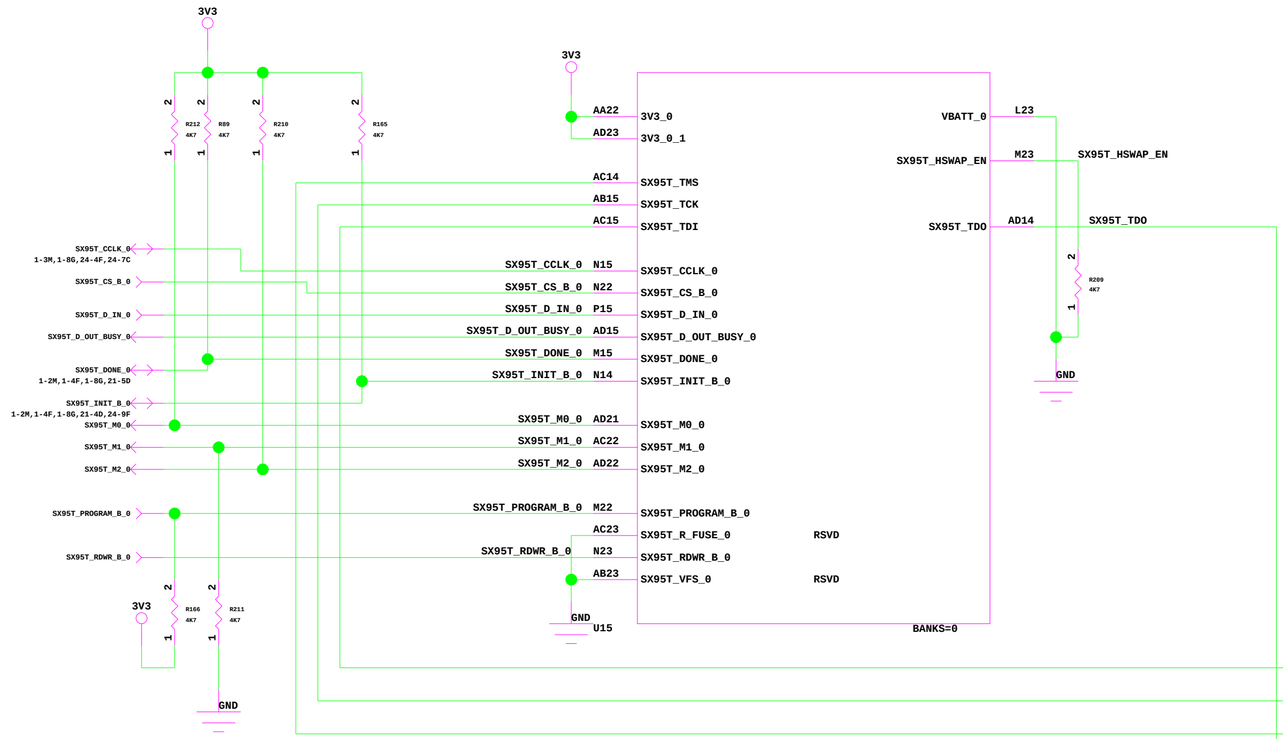
ROACH/iBOB2		ROACH_QDR2P_BY2_3	
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/		DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
		DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
11-27-2008_13:45		DRAWN: F KAPP	APPR:
PATH PATH		CHECKED: E BAUERMEISTER	SHEET 15 OF 25

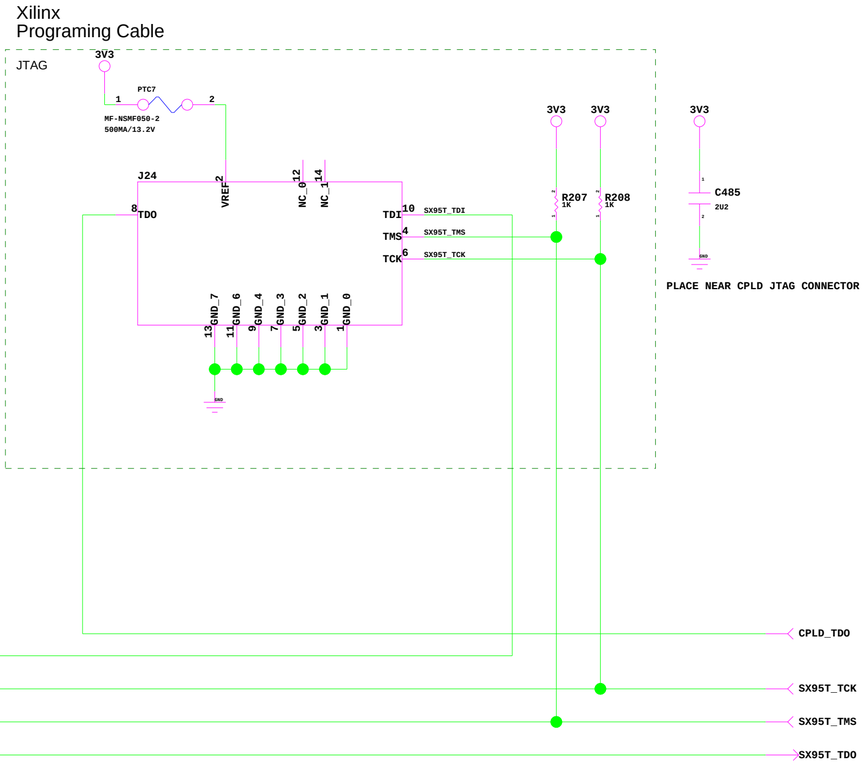
TBD

VALID CONFIGURATION MODES

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

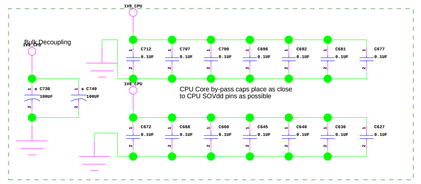


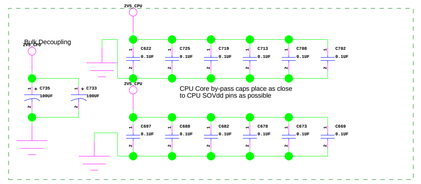


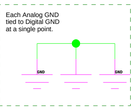


PLACE NEAR CPLD JTAG CONNECTOR

ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR:
11-27-2008_13:45 PATH PATH	CHECKED: E BAUERMEISTER SHEET 16 OF 25





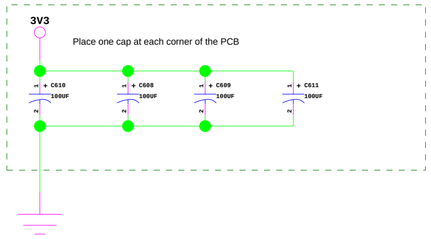


REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 17 OF 25

REMOVED 3V3 GENERATION



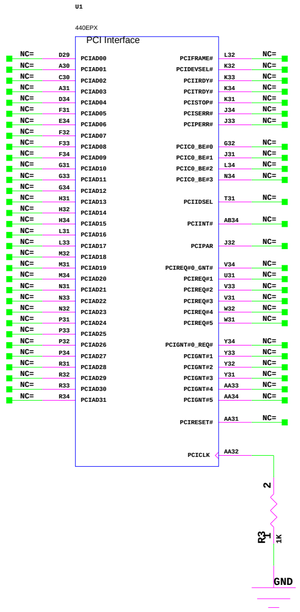
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	**ROACH_PPC_POWER_2**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 18 OF 25
11-27-2008_13:45 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups. Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

Place nearest PHY pin 96

Place nearest PHY pin 101

Place nearest PHY pin 98

Place nearest PHY pin 100

Place as close to PHY CORE VDD power pins as possible

Place as close to PHY IO VDD power pins as possible

UNUSED SECOND ETHERNET MAC

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place components as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible.

Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5

Place jumers in line with signals

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

JUMPER DEFAULTS

JP10, JP11	2 - 3	PHY ADD0 = 1
JP12, JP13	1 - 2	Adertised Modes 1000BASE-T, 100BASE-TX, 10BASE-T
JP14, JP15	1 - 2	
JP16, JP17	2 - 3	FULL DUPLEX
JP18, JP19	2 - 3	AUTO NEGOTIATION ENABLED
JP20-23	1 - 2	PHY ADD4:1 = 1111

ROACH/iBOB2	**ROACH_PPC_ETH1**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-27-2008_13:45	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 20 OF 25

U1

USB 2.0 DEVICE

440EPX

USB2CLK — A5 — NC=

SECOND USB INTERFACE NOT IMPLEMENTED

NOTE:

SX95T_D_IN_0 ON SHEET 25, GPIO10

GPIO28/USB2TXVAL	C6	SX95T_D_OUT_BUSY_0	SX95T_D_OUT_BUSY_0
USB2TXRDY_REFEN	B6	NC=	
USB2RXACT_HOLDREQ_RCVINH	D7	NC=	
USB2RXVAL_LEAKTEST2	C8	NC=	
GPIO27/USB2RXERR_EXTREQ#	A4	SX95T_DONE_0	SX95T_DONE_0
GPIO30/USB2XCVRSEL_EXTACK#	M3	SX95T_INIT_B_0	SX95T_INIT_B_0
GPIO31/USB2TERMSEL_BUSREQ	P4		
USB2LS0_DRVINH1	R2	SX95T_M0_0	SX95T_M0_0
USB2LS1_LEAKTEST_HOLDPRI	P1	NC=	
GPIO32/USB2OM0	R3	SX95T_M1_0	SX95T_M1_0
GPIO33/USB2OM1	R4		
GPIO29/USB2SUSP_HOLDACK	C5	SX95T_M2_0	SX95T_M2_0
		SX95T_PROGRAM_B_0	SX95T_PROGRAM_B_0

NOTE:

USB HOST ONLY

USB 2.0 PHY
HOST/DEVICE

USB2XCVR	J2	USB2_XCVR_D+	
USB2XCVR#	J1	USB2_XCVR_D-	
USB2REXT	L3	R182 3K4 0402	
USB2XTAL	N2		
USB2XTAL#	N3		
CLK_USB2_48MHZ		CLK_USB2_48MHZ	

CRITICAL PLACEMENT

Place SP2 very close to P6

SP2 — SOT23 — PGB102ST23WR

SP2 — SOT23 — PGB102ST23WR

GND

5V

PTC1 — 1206L050 500MA

C614 220UF 10V

C613 100NF 10V

C612 1NF 50V

GND

V84 — 5.5V 20A — 0603

P6 — 1X4 USBA — 89485-8001

1	VCC
2	D-
3	D+
4	GND
5	
6	

GND

ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: **CASPER GROUP, UC BERKELEY** **NRAO, SOCORRO** **meerKAT, CAPE TOWN** http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25
11-27-2008_13:45 PATH PATH	

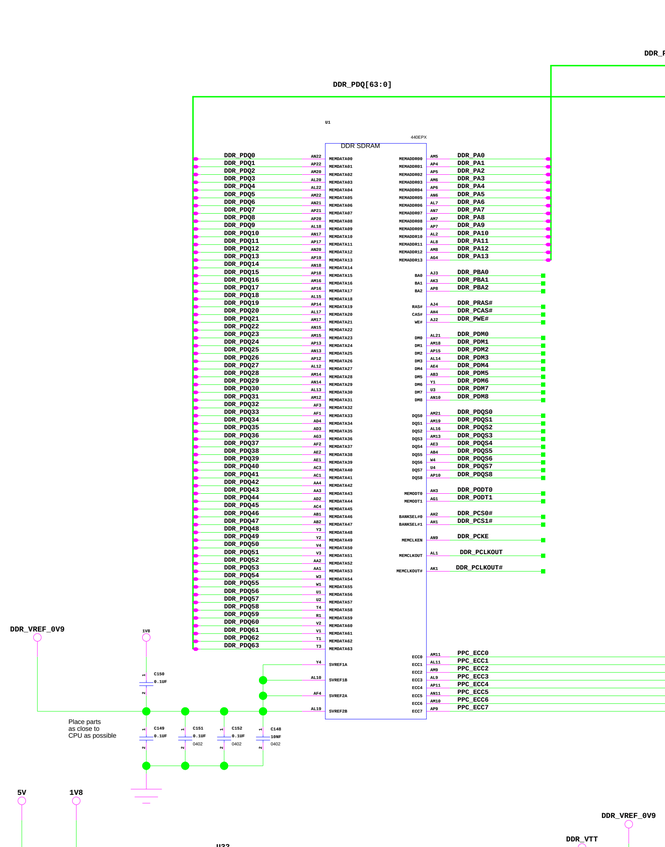
Z_ADDR

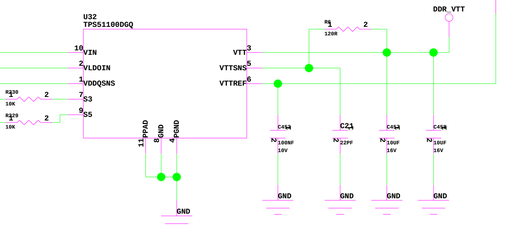
DDR_PA[15:0]

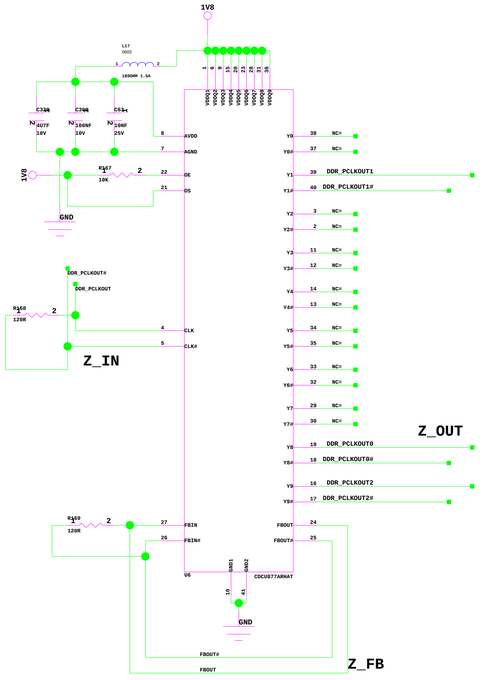
DDR_PDQ[63:0]

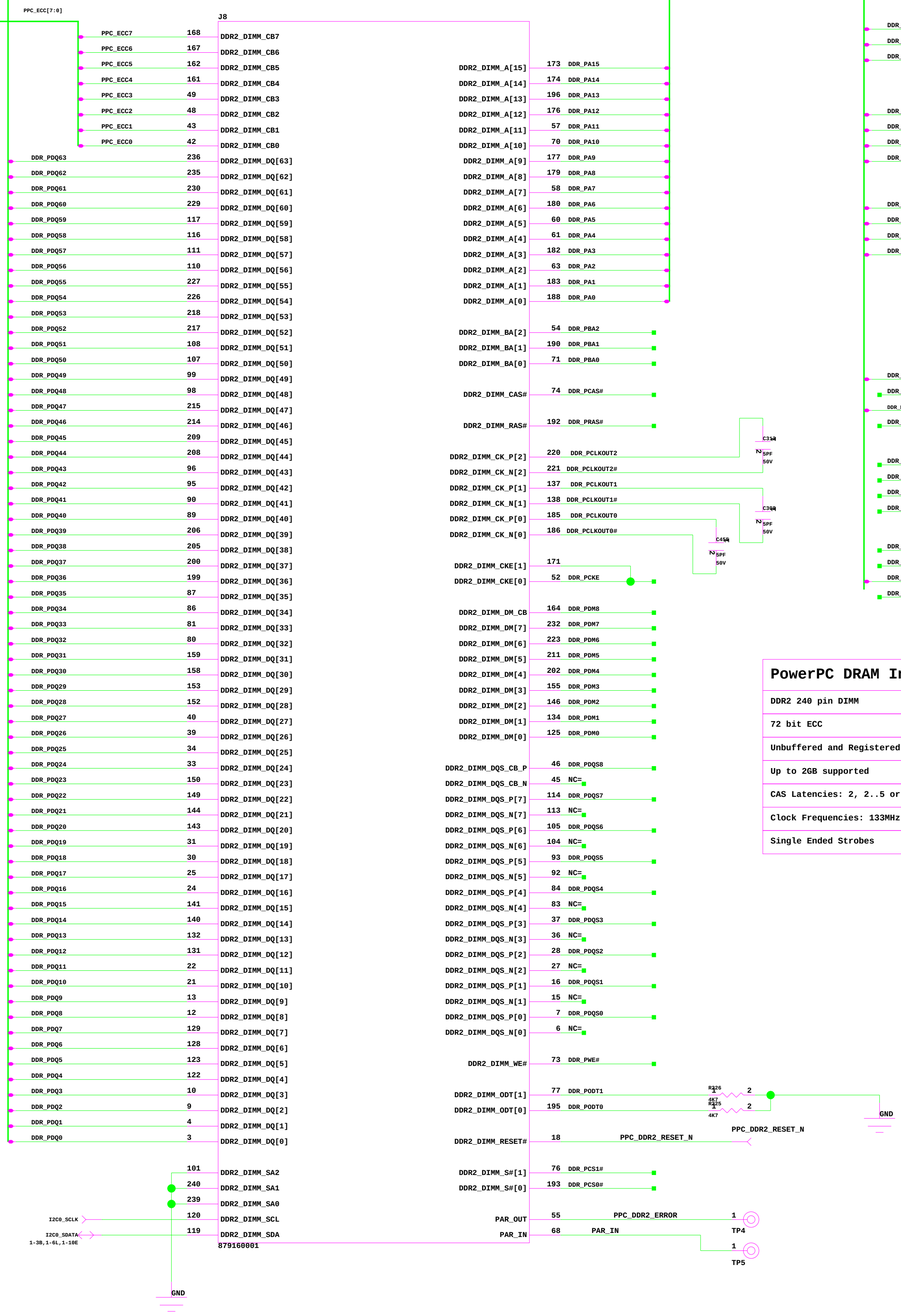
PPC_ECC[7:0]

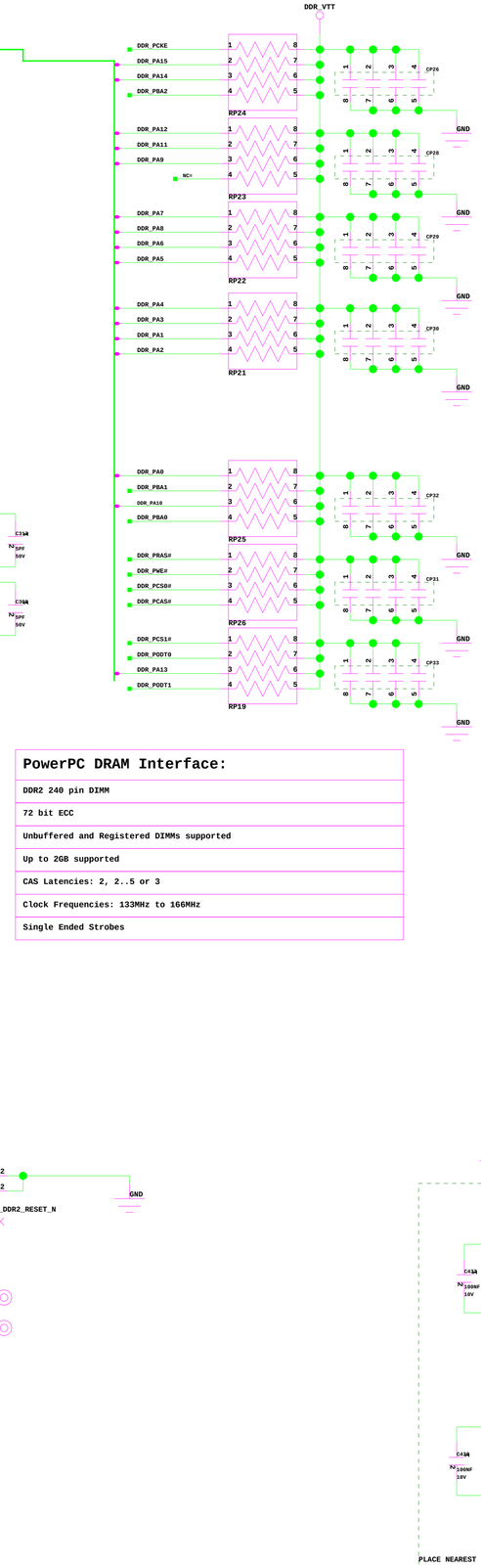
VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

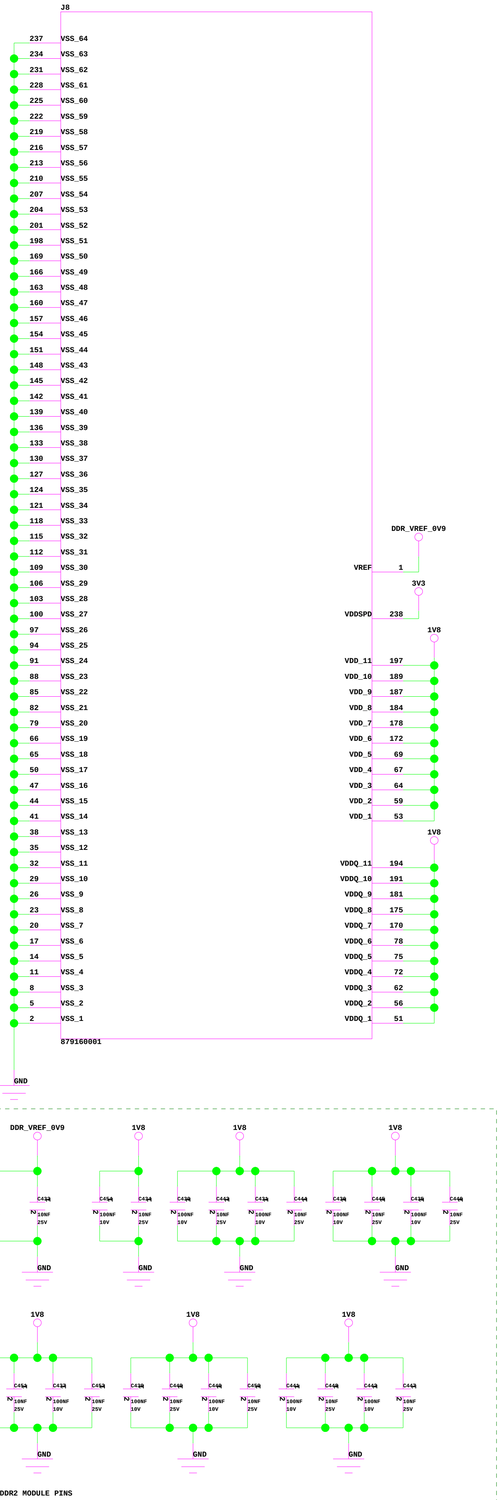












PowerPC DRAM Interface:

DDR2 240 pin DIMM
72 bit ECC
Unbuffered and Registered DIMMs supported
Up to 2GB supported
CAS Latencies: 2, 2..5 or 3
Clock Frequencies: 133MHz to 166MHz
Single Ended Strobes

PPC DDR2 LAYOUT NOTES

ROUTE ALL DDR CLOCKS AS LENGTH MATCHED ONLY - DIFFERENTIAL ROUTING NOT REQUIRED
CLOCK DELAYS MUST ADHERE TO THE FOLLOWING: Z_IN + Z_OUT - Z_FB = Z_ADDR + 500 ps (+-25 ps) WHERE: Z_IN = PROPAGATION DELAY ON DDR_PCLKOUT/DDR_PCLKOUT# Z_OUT = PROPAGATION DELAY ON DDR_PCLKOUTn/DDR_PCLKOUTn# Z_FB = PROPAGATION DELAY ON FBOUT/FBOUT# Z_ADDR = PROPAGATION DELAY ON DDR_PADD[13:0]
DDR_PCLKOUTn/DDR_PCLKOUTn# NETS CAN BE SWAPPED ON CLOCK BUFFER TO EASE ROUTING
ALL DQ, DQS, DM, ADDR, CMD AND CTRL LINES LENGTH MATCHED TO 400 ps MATCHING WITHIN BYTE LANE: 50 ps 209 ps < TRACE LENGTH < 800 ps
U6 THERMAL TAB TO BE CONNECTED TO GND PLANE WITH THERMAL VIAS

ROACH/iBOB2

ROACH_PPC_DDR2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	22 OF 25

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PATH PATH

PWR_GOOD

3V3

PWR_GOOD monitors the +1.0v, 1VS, 1V8, 2VS, and 3V3 supplies

RESET_PB_POR#

RESET_POR# 8,11

SEL_SYSCLK

CLK_UART_11_0592MHZ

CLK_CPLD_33MHZ

UART:11.0592MHZ

SYSTEM:33MHZ

CPLD:33MHZ

PLACE NEAR U9

IRQ0-9 have programmable polarity per section 10.5.7 (UICD_PR) 440ep user manual

GETH0_INT#

MONITOR_INT

VS_INT#

STTM_ALERT

GPIO44

CPLD_INT

CLK_TMRCLK

SYSERR

PPC_THERMONA

PPC_THERMONB

NO POP
RO1 - RO5

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_3V3_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz

Critical Placement and Route
Clock Rules:

Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible

CLK_SEL_M66EN

CLK_GETH0_25MHZ

CLK_USB2_48MHZ

CLK_CPLD_50MHZ

PLACE NEAR U24

TRACE & JTAG CONNECTORS

Critical placement and routing of the Trace connector and nets. Up to CPU frequency/4

TRACE PORT

R26 is for current limiting and should be <100 Ohms.

CPU_TRST#

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

11-27-2008_13:45

PATH PATH

ROACH_PPC_TST_CLK_IO

DOC NO	REVISION
NRF-ADM-XXX-SD-0001	A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN:	APPR:
F KAPP	
CHECKED: E BAUERMEISTER	SHEET 23 OF 25

RESETS

CPU_TRST# = '1' when
JTAG_TRST# = '1' and
RESET_PORF = '1' else '0';
see errata sheet

roach_cpld_XC2C256_7VQ100C_pcb

CLK_TMCLK	4	PAD4	
SYSERR	7	PAD8	
EXT_RESET#	9	PAD10	
SX95T_PROGRAM_B_0	10	PAD12	
SX95T_DONE_0 1-2M,1-4F,1-8G,21-5D	11	PAD15	
PCS_2	12	PAD16	
PB_NF	13	PAD17	
DEBUG_TRST#	14	PAD18	
CPU_TRST#	15	PAD19	
PWBE_0#	16	PAD20	
PAD0[27:31]	17	PAD21	PAD027
	18	PAD23	PAD028
	19	PAD28	PAD029
	20	PAD29	PAD030
	21	PAD30	PAD031
PDATA[0:7] 1-3M,1-5L	22	PAD31	PDATA0
	23	PAD32	PDATA1
	24	PAD33	PDATA2
	25	PAD34	PDATA3
	26	PAD35	PDATA4
	28	PAD44	PDATA7
CLK_CPLD_33MHZ	30	PAD48	
	31	PAD49	PDATA6
	32	PAD50	CLK_PERCLK
	33	PAD52	PDATA5
POE#	34	PAD54	
SX95T_RDWR_B_0	35	PAD55	
CLK_CPLD_50MHZ	38	PAD59	
SX95T_D_IN_0	40	PAD64	
SX95T_D_OUT_BUSY_0	41	PAD65	
PER_CCLK_EN#	42	PAD66	
SX95T_CCLK_0	43	PAD67	
FRY_BY#	44	PAD68	
FWP#	45	PAD69	
EE1_WP	46	PAD70	
EE2_BOOT_WP	48	PAD73	
STTM_AS	49	PAD74	
SELECTMAP_CS	50	PAD75	
PREADY	51	PAD76	
SX95T_CS_B_0	52	PAD77	
CPLD_INT	53	PAD81	
PPC_RESET	54	PAD82	
SYS_CONFIG[0:7]	56	PAD86	SYS_CONFIG0
	57	PAD87	SYS_CONFIG1
	58	PAD88	SYS_CONFIG2
	59	PAD89	SYS_CONFIG3
	60	PAD90	SYS_CONFIG4
	61	PAD95	SYS_CONFIG5
	64	PAD100	SYS_CONFIG6
	66	PAD102	SYS_CONFIG7
NC=	68	PAD105	
NC=	69	PAD107	
NC=	70	PAD108	
RESET_CPLD#	71	PAD109	
NC=	74	PAD112	
NC=	75	PAD113	
NC=	76	PAD114	
NC=	77	PAD115	
NC=	78	PAD117	
NC=	79	PAD118	
NC=	80	PAD119	
NC=	81	PAD120	
NC=	83	PAD121	
NC=	85	PAD125	
NC=	86	PAD131	
NC=	88	PAD133	
	91	PAD134	
	92	PAD137	
	94	PAD138	
	95	PAD143	
	96	PAD144	
	97	PAD145	
	98	PAD146	
	100	PAD152	
	101	PAD154	
	102	PAD156	
	103	PAD158	RESET_PB_POR#
	104	PAD160	
	105	PAD161	SX95T_M2_0
	106	PAD162	SX95T_M1_0
	107	PAD163	SX95T_M0_0
	108	PAD167	
	109	PAD168	
	110	PAD169	MMC_CD
	111	PAD171	DAT2
	112	PAD173	DAT3
	113	PAD175	CMD_DI
	114	PAD176	DAT4
	115	PAD177	DAT5
	116	PAD178	CLK_SCLK
	117	PAD186	DAT6
	118	PAD187	DAT1
	119	PAD189	DAT0_DO
	120	PAD190	DAT7
	121	PAD191	MMC_WP
	122	PAD192	
	123	PAD194	
	124	PAD195	
	125	PAD196	
	126	PAD197	
	128	PAD199	
	129	PAD204	
	131	PAD206	SX95T_INIT_B_0
	132	PAD207	
	133	PAD208	
	134	PAD211	CLK_SEL_MGGEN
	135	PAD212	PPC_DDR2_RESET_N
	136	PAD213	GETH0_RST#
	137	PAD214	
	138	PAD217	
	139		
	140		
	142		

U54 XC2C256_7VQ144C

ENABLE PER_CLK CONNECTION
TO CONFIGURATION I/F
MUST CO-ORDINATE WITH
SX95T_CCLK_0 AND MODE
TO AVOID CLASH

SN74AHC1G125DCKT
PER_CCLK_EN# 1 OE# VCC 5
CLK_PERCLK 2 A Y 4 SX95T_CCLK_0
3 GND
U2

R235 1K 2
R305 330R 2
R306 330R 2
C113 100NF 10V
CLK_PERCLK
PLACE AT END OF DAISY CHAIN
SX95T_CCLK_0

U54 XC2C256_7VQ144C

roach_cpld_XC2C256_7VQ100C_powerpins

VCC	1	29	GND_3
VAUX	8	36	GND_4
VCCIO_3	27	47	GND_5
VCC_1	37	62	GND_6
VCCIO_4	55	72	GND_7
VCCIO_5	73	89	GND_8
VCC_2	84	90	GND_9
VCCIO_6	93	99	GND_10
VCCIO	109	108	GND
VCCIO_1	127	123	GND_1
VCCIO_2	141	144	GND_2

PLACE NEAR CPLD POWER PINS

C43 C44 C45 C46 C47 C48 C49 C50 C51 C52 — 100NF 10V

SD/MMC/MMCPLUS CONNECTOR

J17 SDSR13-A0-0005

4	CMD/DI	DAT0/DO	13
9	CLK/SCLK	DAT1	14
		DAT2	1
8	VDD	DAT3	2
7	VSS1	DAT4	3
11	VSS2	DAT5	5
		DAT6	10
6	SD_CD_COM	DAT7	12
15	SD_WP_COM		
		MNT1	16
		MNT2	17

BOOT_CFG0
BOOT_CFG1
BOOT_CFG2
R010 R011 R014 — 0Ω POP

RESETS

SysErr will be used to drive Status LED (active H)

R200 R201 R202 R203 — 180R
R204 R205 R206 — 10K
R207 R208 R209 R210 — 10K
SW2 User DIP-Switch
SW3 Configuration DIP-Switch
USER_DIP0 USER_DIP1 USER_DIP2 USER_DIP3
CFG_DIP0 CFG_DIP1 CFG_DIP2 MGGEN

Boot Configuration

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

R337 330R
R339 330R
U35 74LVC1G08 SC70-5
C515 0.1UF
PWR_GOOD

U54 XC2C256_7VQ144C

NC=	2	PAD1	
NC=	3	PAD3	
NC=	5	PAD5	
NC=	6	PAD7	
NC=	39	PAD62	
SX95T_TDO	63	TDI	
SX95T_TMS	65	TMS	
SX95T_TCK	67	TCK	
CPLD_TDO	122	TDO	
RESET_PORF	143	PAD218	

roach_cpld_XC2C256_7VQ100C_configpins

ROACH/iBOB2	ROACH_PPC_CPLD	
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
11-27-2008_13:45 PATH PATH	DRAWN: F KAPP	APPR:
	CHECKED: E BAUERMEISTER	SHEET 24 OF 25

PDATA[0:31]
1-3M,1-5L

PADD[2:31]

PADD[2:31]
1-3G,1-5L,24-9B

PADD30 IS THE LSB FOR 16 BIT WIDE BUS TRANSFERS

**NOTE:
DMA SIGNALS
IN GREEN TEXT**

PADD2 IS THE MSB

CHIP SELECTS CONFIG	
CS0	NOR FLASH - U42
CS1	FPGA - U15
CS2	CPLD - U54
CS3	FPGA - U15
CS4	SELECTMAP_CS
CS5	GPIO - SX95_D_IN

External Slave Peripheral
AKEPX

External Master Peripheral
Interface

FLASH
32Mx16
4Gb

UART
IIC0
IIC1_SPI
NAND Flash
Interface
NOT USED

**ROUTE AS DAISY CHAIN - U1 - U15 - U2 - U54 - TERMINATION
KEEP STUBS AS SHORT AS POSSIBLE**

EPB RESET OUTPUT
EXT_RESET#

UART Port 0

UART Port 1

HLE-105-02-G-DV

PER_A[30]
PER_A[29]
PER_A[28]
PER_A[27]
PER_A[26]
PER_A[25]
PER_A[24]
PER_A[23]
PER_A[22]
PER_A[21]
PER_A[20]
PER_A[19]
PER_A[18]
PER_A[17]
PER_SP_A[16]
PER_SP_A[15]
PER_SP_A[14]
PER_SP_A[13]
PER_SP_A[12]
PER_SP_A[11]
PER_SP_A[10]
PER_SP_A[9]
PER_SP_A[8]
PER_SP_A[7]
PER_SP_A[6]
PER_SP_A[5]
PER_SP_A[4]
PER_SP_A[3]
PER_SP_A[2]
PER_CS0
PER_CS1
PER_OE_N
PER_R_W_N
PER_WBE[1]
PER_WBE[0]
PER_B_LAST

BANKS=1, 2, 4
CHIP SELECT 1

PER_D[15]
PER_D[14]
PER_D[13]
PER_D[12]
PER_D[11]
PER_D[10]
PER_D[9]
PER_D[8]
PER_D[7]
PER_D[6]
PER_D[5]
PER_D[4]
PER_D[3]
PER_D[2]
PER_D[1]
PER_D[0]

PER_D_PAR[1]
PER_D_PAR[0]

PER_INT
PER_READY
PER_CLK

ROACH/iBOB2

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ROACH_PPC_NVM_SERIAL

DOC NO	REVISION
NRF-ADM-XXX-SD-0001	A

DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN:	APPR:
F KAPP	
CHECKED: E BAUERMEISTER	SHEET 25 OF 25

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PATH PATH