VIRTEX5

POWER SUPPLY AND MONITORING

ROACH_MONITOR

1-5L,21-5A,22-2P	I2C0_SCLK	I2C0_SCLK	
1-8E,14-10B,22-2M	FAN2_SENSE	FAN2_SENSE	
1-8E,14-10B,22-2M	FAN1_SENSE	FAN1_SENSE	
1-8E,14-9B,22-1M	FAN3_SENSE	FAN3_SENSE	
1-8E,14-6C,22-3A	3V3_ATX	3V3_ATX	
1-8E,14-2H,22-2B	2V5	I2V5	
1-8E,14-2H,22-2B	1V8	I1V8	
1-8E,14-5B,22-2B	1V5	I1V5	
1-8E,14-10B,22-1B	I1V0	I1V0	
1-8E,14-7C,22-4A	5V_ATX	5V_ATX	
1-9Q,17-7P,22-0B	MGT_AVCC_PG	MGT_AVCC_PG	
1-9Q,17-4G,22-0B	MGT_AVTTX_PG	MGT_AVTTX_PG	
1-9Q,17-7G,22-0B	MGT_AVCCPLL_PG	MGT_AVCCPLL_PG	
1-8E,14-7C,22-0B	PWR_OK	PWR_OK	
1-8E,14-6C,22-6B	12V_ATX	12V_ATX	
	I1V0	2	

	PPC_RESET	PPC_RESET	1-2G,15-6C,22-2R
	SYS_CONFIG[0:7]	SYS_CONFIG[0:7]	1-8E,15-6B,22-2R
	TDZ	PPC_THERMONA	1-2G,15-8B,22-2B
	ATRTN1	PPC_THERMONB	1-2L,22-6L,23-6H
	MONITOR_INT	MONITOR_INT	1-3L,22-4L,23-6H
	I2C0_33_DATA	I2C0_33_DATA	1-3H,22-1P,23-7H
	PS_ONB	PS_ONB	1-5L
	ATRTN0	ATRTN0	1-8B,14-8G,22-8B
	TD0	TD0	
	FAN1_CONTROL	FAN1_CONTROL	1-8B,14-10B,22-2M
	LOAD_RES_OFF	LOAD_RES_OFF	1-8B,14-5B,22-6B
	2V5_TRACK	2V5_TRACK	1-8B,14-3B,22-6B
	2V5_INHIBIT	2V5_INHIBIT	1-8B,14-1B,22-1B
	FAN3_CONTROL	FAN3_CONTROL	1-8B,14-9B,22-2M
	FAN2_CONTROL	FAN2_CONTROL	1-8B,14-10B,22-2M
	MGT_AVTTX_EN	MGT_AVTTX_EN	1-9L,17-5B,22-1M
	MGT_AVCCPLL_EN	MGT_AVCCPLL_EN	1-9L,17-8B,22-1M
	MGT_AVCC_EN	MGT_AVCC_EN	1-9L,17-6B,22-1M
	1V8_INHIBIT	1V8_INHIBIT	1-8B,14-12,22-1B
	1V5_INHIBIT	1V5_INHIBIT	1-8B,14-4J,22-1B
	1V0_INHIBIT	1V0_INHIBIT	1-8B,14-9J,22-0B
		3	

ROACH_PSU

1-9E,14-5B,22-6B	LOAD_RES_OFF	LOAD_RES_OFF	
1-9E,14-10B,22-3M	FAN1_CONTROL	FAN1_CONTROL	
1-8E,14-9G,22-0B	PS_ONB	PS_ONB	
1-9E,14-10B,22-2M	FAN2_CONTROL	FAN2_CONTROL	
1-9E,14-9B,22-2M	FAN3_CONTROL	FAN3_CONTROL	
1-8E,14-9J,22-0B	1V0_INHIBIT	1V0_INHIBIT	
1-8E,14-4J,22-1B	1V5_INHIBIT	1V5_INHIBIT	
1-8E,14-1J,22-1B	1V8_INHIBIT	1V8_INHIBIT	
1-9E,14-3B,22-6B	2V5_TRACK	2V5_TRACK	
1-8E,14-1B,22-1B	2V5_INHIBIT	2V5_INHIBIT	
	12V_ATX	12V_ATX	1-8B,14-6C,22-6B
	3V3_ATX	3V3_ATX	1-9B,14-6C,22-3A
	5V_ATX	5V_ATX	1-8B,14-7C,22-4A
	PWR_OK	PWR_OK	1-8B,14-7C,22-8B
	FAN1_SENSE	FAN1_SENSE	1-9B,14-10B,22-2M
	FAN2_SENSE	FAN2_SENSE	1-8B,14-10B,22-2M
	FAN3_SENSE	FAN3_SENSE	1-9B,14-9B,22-1M
	I1V0	I1V0	1-9B,14-10B,22-1B
	I1V5	I1V5	1-9B,14-5B,22-2B
	I1V8	I1V8	1-9B,14-2H,22-2B
	I2V5	I2V5	1-9B,14-2H,22-2B
		3	

VIRTEX5 CLOCKS

ROACH_V5_CLK

SX95T_DXN	ATRTN0	
SX95T_DXP	TD0	
7		

ZDOK/ADC INTERFACE

ROACH_ADC_0

5

ROACH_ADC_1

6

V5 DDR2 MEMORY

ROACH_DDR2_DIMM

11

V5 DIFFERENTIAL GPIO

ROACH_DIFF_GPIO

12

V5 SE GPIO & MISCELLANEOUS

ROACH_GPIO_MISC

13

GIGABIT TRANSCEIVERS

ROACH_TRANSCEIVERS0_1

8

ROACH_TRANSCEIVERS2_3

9

ROACH_TRANSCEIVERS_PSU

1-9E,17-8K,22-1M	MGT_AVCC_EN	MGT_AVCC_EN	MGT_AVCC_PG	MGT_AVCC_PG
1-9E,17-8B,22-1M	MGT_AVCCPLL_EN	MGT_AVCCPLL_EN	MGT_AVTTX_PG	MGT_AVTTX_PG
1-9E,17-5B,22-1M	MGT_AVTTX_EN	MGT_AVTTX_EN	MGT_AVCCPLL_PG	MGT_AVCCPLL_PG
		10		

QDRII+ MEMORY

ROACH_QDR2P_BY0_1

24-5F	QDR2_TDI	QDR2_TDI	QDR2_BY0_1_TDO
	QDR2_TCK	QDR2_TCK	
	QDR2_TMS	QDR2_TMS	
		14	

ROACH_QDR2P_BY2_3

QDR2_BY0_1_TDO	QDR2_BY0_1_TDO	QDR2_BY2_3_TDO	QDR2_BY2_3_TDO
QDR2_TMS	QDR2_TMS		25-5H
QDR2_TCK	QDR2_TCK		
	15		

V5 POWER

ROACH_5V_POWER

4

VIRTEX5 CONFIGURATION

ROACH_CONFIG

1-1M,15-7C,16-4A	SX95T_D_IN_0	SX95T_D_IN_0	
1-3L,16-2L,23-6H	SX95T_TCK	SX95T_TCK	
1-3L,16-2L,23-6H	SX95T_TMS	SX95T_TMS	
1-3L,16-2L,23-6H	SX95T_TDI	SX95T_TDI	
1-1M,15-8C,16-3B	SX95T_RDWR_B_0	SX95T_RDWR_B_0	
1-1M,1-3F,8-4D,15-10C,16-3B	SX95T_PROGRAM_B_0	SX95T_PROGRAM_B_0	
1-1M,15-9C,16-4B	SX95T_CS_B_0	SX95T_CS_B_0	
		16	
	SX95T_M2_0	SX95T_M2_0	1-1G,1-3F,8-4D,15-7F,16-3B
	SX95T_M1_0	SX95T_M1_0	1-1G,1-3F,8-4D,15-7F,16-3B
	SX95T_M0_0	SX95T_M0_0	1-1G,1-3F,8-4D,15-7F,16-3B
	SX95T_DONE_0	SX95T_DONE_0	1-1M,1-3F,8-5D,15-10C
	SX95T_CCLK_0	SX95T_CCLK_0	1-2M,15-4F,15-7C
	SX95T_D_OUT_BUSY_0	SX95T_D_OUT_BUSY_0	1-1G,1-3F,8-5D,15-7C,16-4B
	SX95T_INIT_B_0	SX95T_INIT_B_0	1-1M,1-3F,8-4D,15-9F
	SX95T_TDO	SX95T_TDO	1-3H,16-2L,23-6H

V5 PPC

ROACH_PPC_POWER_1

17

ROACH_PPC_POWER_2

18

ROACH_PPC_PCI

19

ROACH_PPC_ETH1

1-2M,15-10F,18-4E	GETH0_RST#	GETH0_RST#	GMCMDIO	GMCMDIO
1-3L,18-4E,23-5G	CLK_GETH0_25MHZ	CLK_GETH0_25MHZ	GMCMDCLK	GMCMDCLK
			GETH0_INT#	GETH0_INT#
		20		

ROACH_PPC_USB

CONTAINS GPIO TO CONFIG INTERFACE

SX95T_D_OUT_BUSY_0	SX95T_D_OUT_BUSY_0		1-1G,1-7G,8-5D,15-7C,16-4B
SX95T_DONE_0	SX95T_DONE_0		1-1M,1-7G,8-5D,15-10C
SX95T_INIT_B_0	SX95T_INIT_B_0		1-1M,1-7G,8-4D,15-9F
SX95T_M0_0	SX95T_M0_0		1-1G,1-7G,8-4D,15-7F,16-3B
SX95T_M1_0	SX95T_M1_0		1-1G,1-7G,8-4D,15-7F,16-3B
SX95T_M2_0	SX95T_M2_0		1-1G,1-7G,8-4D,15-7F,16-3B
SX95T_PROGRAM_B_0	SX95T_PROGRAM_B_0		1-1M,1-7G,8-4D,15-10C,16-3B
1-3L,8-2C,23-4G	CLK_USB2.0_48MHZ	CLK_USB2.0_48MHZ	
		21	

ROACH_PPC_DDR2

1-2M,11-3K,15-10F	PPC_DDR2_RESET_N	PPC_DDR2_RESET_N
		22

ROACH_PPC_NVM_SERIAL

1-3L,23-3D,23-7G	CLK_UART_11.0592MHZ	CLK_UART_11.0592MHZ	
1-1G,15-5H,21-3B	M66EN	M66EN	
1-2M,15-7C,21-3A	EE1_WP	EE1_WP	
1-2M,15-7C,21-1B	STTM_AS	STTM_AS	
1-2G,1-3L,15-7F,21-5G,23-9J	RESET_POR#	RESET_POR#	
1-1M,15-7C,21-8J	FWP#	FWP#	
1-2M,15-7C,21-5A	EE2_BOOT_WP	EE2_BOOT_WP	
1-1M,15-11M,21-1J	BOOT_CFG0	BOOT_CFG0	
1-1M,15-11M,21-1J	BOOT_CFG1	BOOT_CFG1	
1-1M,15-10M,21-1J	BOOT_CFG2	BOOT_CFG2	
1-1M,15-5C,21-3J	RESET_CPLD#	RESET_CPLD#	
		25	

	VS_INT#	VS_INT#	1-3H,21-8Q,23-7B
	SELECTMAP_CS	SELECTMAP_CS	1-2G,15-6C,21-7B
	I2C0_SCLK	I2C0_SCLK	1-9B,21-5A,22-2P
	I2C0_33_DATA	I2C0_33_DATA	1-9E
	SCPDI	SCPDI	
	SCPCLK	SCPCLK	21-1B
	STTM_ALERT	STTM_ALERT	1-3H,21-2B,23-6M
	SCPDO	SCPDO	23-6B
	PDE#	PDE#	1-1G,15-8C,21-5G,21-7B,21-7M,21-10B
	FRY_BY#	FRY_BY#	1-1G,15-7C,21-7J
	CLK_PERCLK	CLK_PERCLK	1-1G,15-4C,15-7C,23-6F
	PWBE_0#	PWBE_0#	1-2G,15-9C,21-6M,21-7B,21-9B
	PB_WI	PB_WI	1-1G,15-9C,21-5G,21-6M,21-7B,21-9B
	PCS_2	PCS_2	1-1G,15-9C,21-7B
	PDATA[8:31]	PDATA[8:31]	1-2M
	PADD[2:31]	PADD[2:31]	1-2G,15-9B,21-10B
	EXT_RESET#	EXT_RESET#	1-2G,15-10C,21-6F

ROACH_PPC_TST_CLK_IO

	PPC_THERMONA	PPC_THERMONA	1-9E,22-6L,23-6H
	PPC_THERMONB	PPC_THERMONB	1-9E,22-4L,23-6H
	GPIO44	GPIO44	23-6N
	SX95T_TDI	SX95T_TDI	1-7C,16-2L,23-6N
	SX95T_TCK	SX95T_TCK	1-7C,16-2L,23-6M
	SX95T_TMS	SX95T_TMS	1-7C,16-2L,23-6N
	RESET_PORH	RESET_PORH	1-2G,1-5B,15-7F,21-5G,23-9J
	DEBUG_TRST#	DEBUG_TRST#	1-1G,15-9C,23-1F
	CLK_GETH0_25MHZ	CLK_GETH0_25MHZ	1-4B,18-4E,23-5G
	CLK_USB2.0_48MHZ	CLK_USB2.0_48MHZ	1-3B,8-2C,23-4G
	CLK_CPLD_50MHZ	CLK_CPLD_50MHZ	1-1G,15-10F,23-4G
	SYSERR	SYSERR	1-1G,15-10C,23-6H
	CLK_UART_11.0592MHZ	CLK_UART_11.0592MHZ	1-5G,21-3D,23-7G
	CLK_CPLD_33MHZ	CLK_CPLD_33MHZ	1-1G,15-10F,23-6G
		23	

1-4E,18-4E,23-7N	GETH0_INT#	GETH0_INT#	
1-9E,22-1F,23-7M	MONITOR_INT	MONITOR_INT	
1-5L,21-9Q,23-7N	VS_INT#	VS_INT#	
1-5L,21-2B,23-6M	STTM_ALERT	STTM_ALERT	
1-7G,16-2L,23-6M	SX95T_TDO	SX95T_TDO	
1-2M,15-7F,23-8E	RESET_PB_POR#	RESET_PB_POR#	
1-2G,15-9B,23-10G	PWR_GOOD	PWR_GOOD	
1-2M,15-9C,23-2F	CPU_TRST#	CPU_TRST#	
1-1M,15-10F,23-5D	CLK_SEL_M66EN	CLK_SEL_M66EN	
1-1M,15-10F,23-7G	SEL_SYSCLK	SEL_SYSCLK	
1-1M,15-10C,23-6H	CLK_TMRCLK	CLK_TMRCLK	

ROACH_PPC_CPLD

1-9E,15-6B,22-2R	SYS_CONFIG[0:7]	SYS_CONFIG[0:7]	
1-9E,15-6C,22-2R	PPC_RESET	PPC_RESET	
1-3H,15-8R,23-10G	PWR_GOOD	PWR_GOOD	
1-4L,15-10C,23-6F	EXT_RESET#	EXT_RESET#	
1-3L,1-5G,15-7F,21-5G,23-9J	RESET_PORH	RESET_POR#	
1-4L,15-9C,21-6M,21-7B,21-9B	PWBE_0#	PWBE_0#	
1-4L,15-9B,21-10B	PADD[27:31]	PADD[27:31]	
1-5L,15-8C,21-7B	SELECTMAP_CS	SELECTMAP_CS	
1-4L,15-7C,23-6F	FRY_BY#	FRY_BY#	
1-3L,15-10C,23-6H	SYSERR	SYSERR	
1-2L,15-10F,23-4G	CLK_CPLD_33MHZ	CLK_CPLD_33MHZ	
1-3L,15-9C,23-1F	DEBUG_TRST#	DEBUG_TRST#	
1-4L,15-4C,15-7C,23-6F	CLK_PERCLK	CLK_PERCLK	
1-3L,15-10F,23-4G	CLK_CPLD_50MHZ	CLK_CPLD_50MHZ	
1-4L,15-9C,21-5G,21-6M,21-7B,21-9B	PB_WI	PB_WI	
1-5L,15-8C,21-5G,21-7B,21-7M,21-10B	PDE#	POE#	
1-4L,15-9C,21-7B	PCS_2	PCS_2	
1-3F,1-7G,8-5D,15-7C,16-4B	SX95T_D_OUT_BUSY_0	SX95T_D_OUT_BUSY_0	
1-5G,15-5H,21-3B	M66EN	M66EN	
1-3F,1-7G,8-4D,15-7F,16-3B	SX95T_M2_0	SX95T_M0_0	
1-3F,1-7G,8-4D,15-7F,16-3B	SX95T_M1_0	SX95T_M1_0	
1-3F,1-7G,8-4D,15-7F,16-3B	SX95T_M0_0	SX95T_M2_0	
		24	

	GETH0_RST#	GETH0_RST#	1-4B,15-10F,18-4E
	PPC_DDR2_RESET_N	PPC_DDR2_RESET_N	1-2B,11-3K,15-10F
	PDATA[0:7]	PDATA[0:7]	1-4L
	RESET_PB_POR#	RESET_PB_POR#	1-3H,15-7F,23-8E
	SX95T_CCLK_0	SX95T_CCLK_0	1-7G,15-4F,15-7C
	STTM_AS	STTM_AS	1-5G,15-7C,21-1B
	EE2_BOOT_WP	EE2_BOOT_WP	1-4G,15-7C,21-5A
	EE1_WP	EE1_WP	1-5G,15-7C,21-3A
	CPU_TRST#	CPU_TRST#	1-3H,15-9J,23-2F
	SEL_SYSCLK	SEL_SYSCLK	1-3H,15-10F,23-7G
	CLK_SEL_M66EN	CLK_SEL_M66EN	1-3H,15-10F,23-5D
	CLK_TMRCLK	CLK_TMRCLK	1-3H,15-10C,23-6H
	SX95T_ROWR_B_0	SX95T_ROWR_B_0	1-7C,15-8C,16-3B
	FWP#	FWP#	1-4G,15-7C,21-8J
	RESET_CPLD#	RESET_CPLD#	1-4G,15-5C,21-3J
	SX95T_INIT_B_0	SX95T_INIT_B_0	1-3F,1-7G,8-4D,15-9F
	SX95T_DONE_0	SX95T_DONE_0	1-3F,1-7G,8-5D,15-10C
	SX95T_PROGRAM_B_0	SX95T_PROGRAM_B_0	1-3F,1-7C,8-4D,15-10C,16-3B
	SX95T_D_IN_0	SX95T_D_IN_0	1-7C,15-7C,16-4A
	SX95T_CS_B_0	SX95T_CS_B_0	1-6C,15-6C,16-4B
	BOOT_CFG0	BOOT_CFG0	1-4G,15-11M,21-1J
	BOOT_CFG1	BOOT_CFG1	1-4G,15-11M,21-1J
	BOOT_CFG2	BOOT_CFG2	1-4G,15-10M,21-1J
		24	

MECHANICAL

GND

H1 H2 H3 H4 H5 H6 H7 H8 H9 — 3.5X4.2X6MM

CONTRIBUTORS

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ROACH/iBOB2	ROACH_TOP
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
12-14-2007_14:51	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 1 OF 25

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

TIE TO GROUND IF PLL'S ARE NOT USED

PLACE AT ACTEL 3V3 POWER PINS

PLACE AT ACTEL 1V5 POWER PINS

roach_AFS600_powerpins

roach_AFS600_configpins

roach_AFS600_pcb

PB POWER SWITCH

KEY - REMOVE PIN

MONITOR RESET

XPORT - PLACE IN REAR I/O REGION
XP1001001-03R

TEMPERATURE DIODE HEADER

ACTEL JTAG CONNECTOR

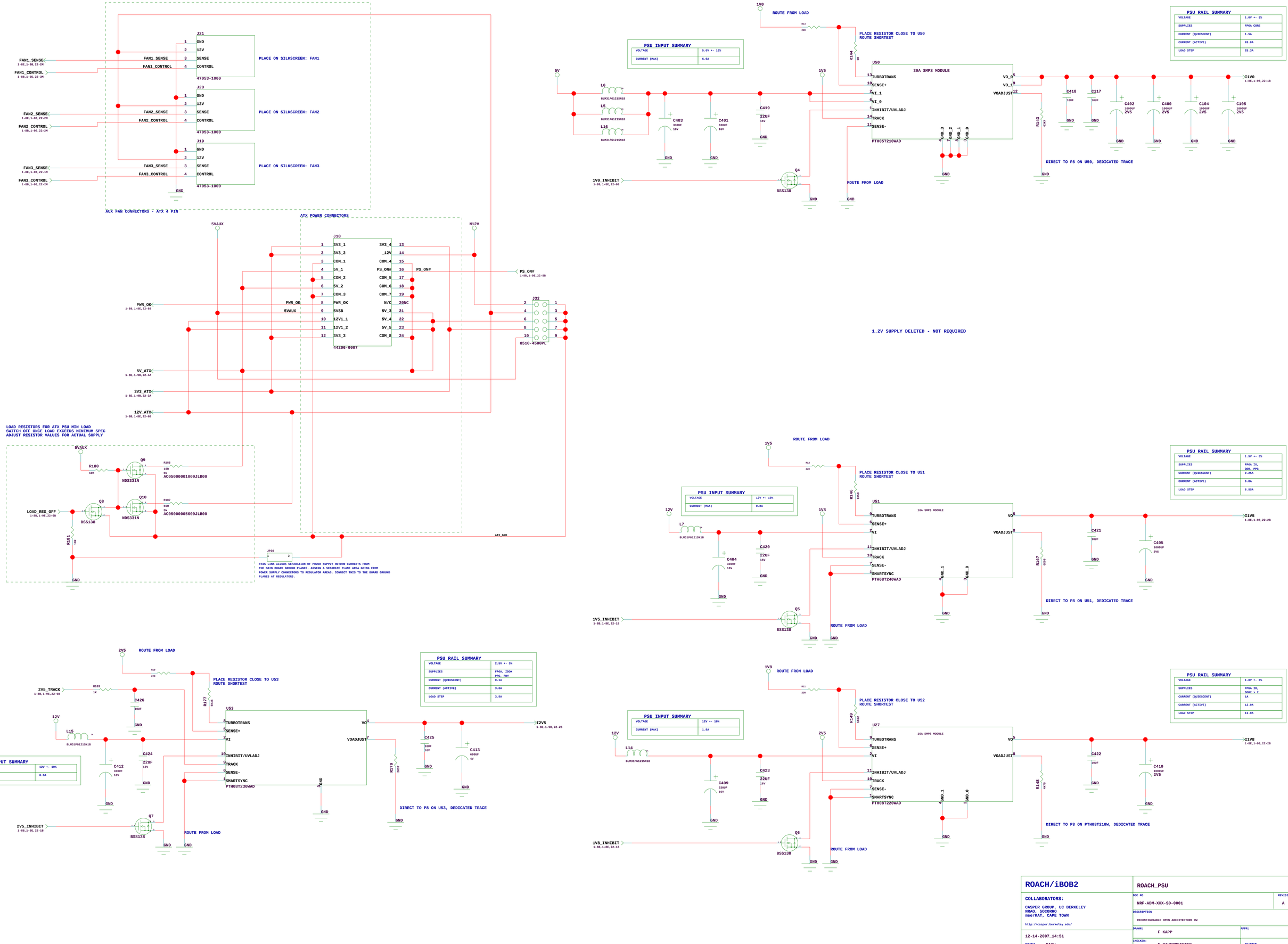
REFERENCE RESISTOR/ADC VALUES

VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)
12V	0R01	3.36	0.11
5V	0R0047	6.78	0.22
3V3	0R01	3.47	0.12
2V5	0R01	3.56	0.13
1V8	0R0022	12.91	0.37
1V5	0R0047	6.77	0.22
1V0	0R001	26.79	0.72

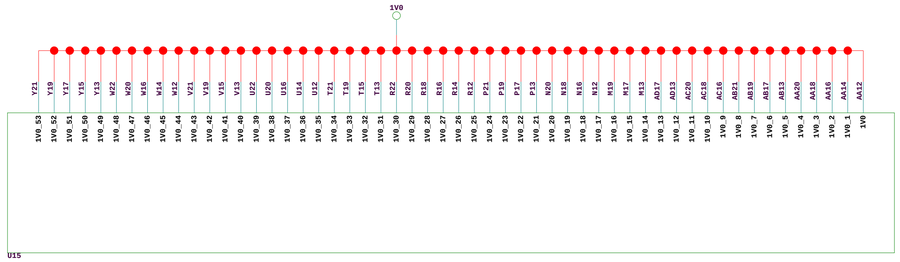
FOR 8 BIT ADC USING 2.56V REFERENCE:

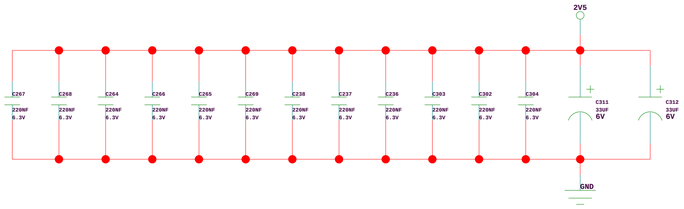
ADC COUNT AT MAX POWER	CURRENT/BIT (A)
33	0.1
31	0.21
34	0.1
35	0.1
28	0.45
31	0.21
26	1.0

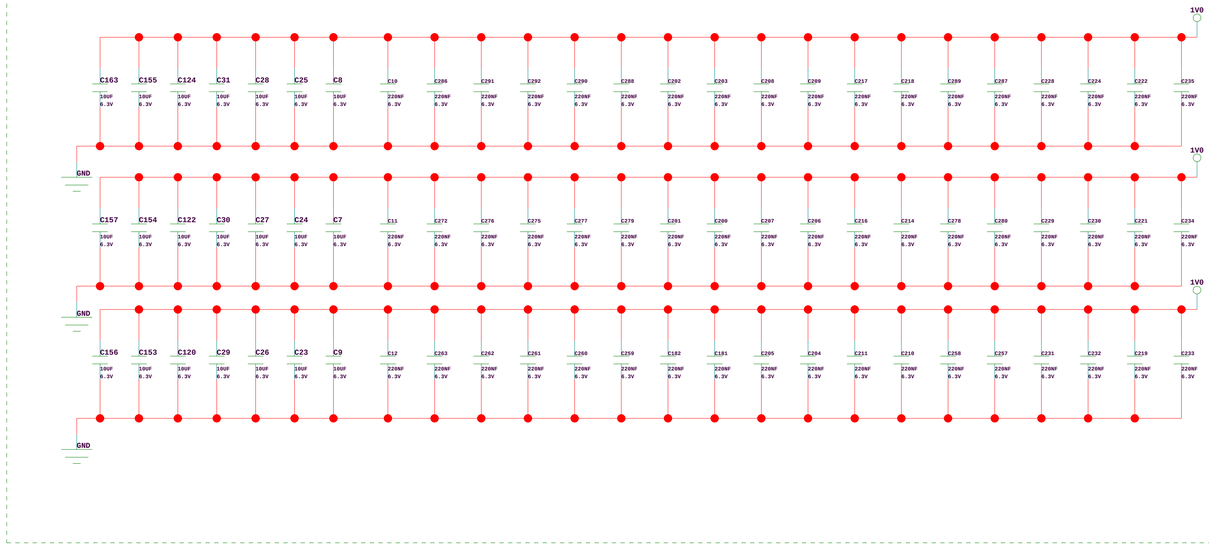
ROACH/iBOB2	ROACH_MONITOR
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
12-14-2007_14:51	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 22 OF 25

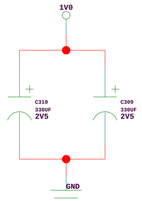


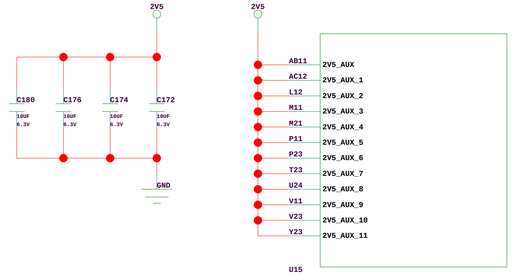
ROACH/iBOB2	ROACH_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO NRF-ADM-XXX-SD-0001 REVISION A
	DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
12-14-2007_14:51	DRAWN: F KAPP APPR:
PATH PATH	CHECKED: E BAUERMEISTER SHEET 14 OF 25

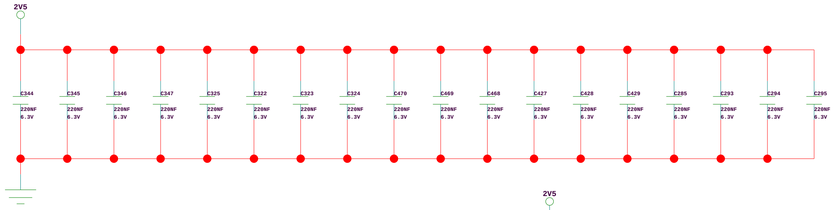


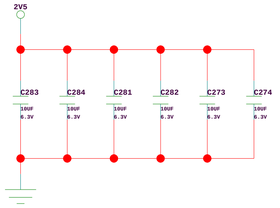


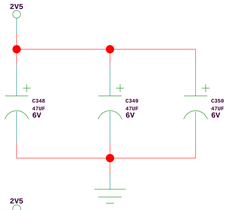


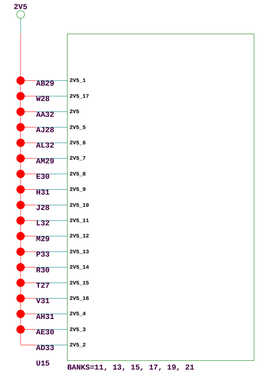


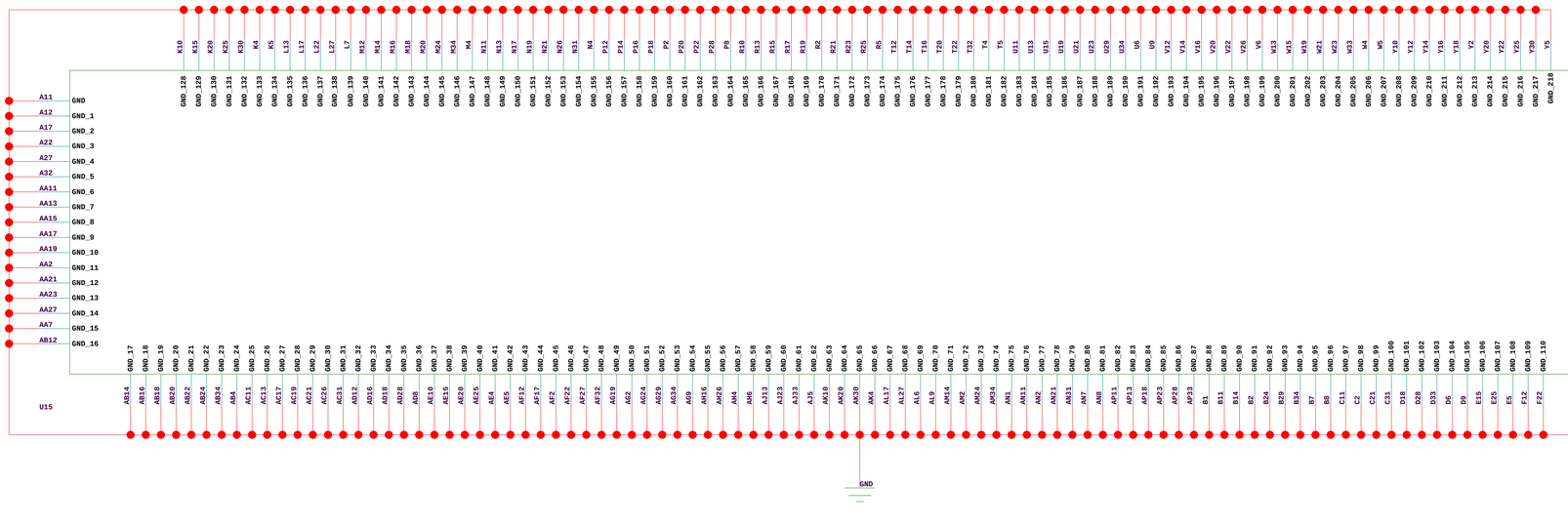












ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 13 OF 25
12-14-2007_14:51 PATH PATH	

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

12-14-2007_14:51

PATH PATH

ROACH_ADC_0

DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 4 OF 25

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

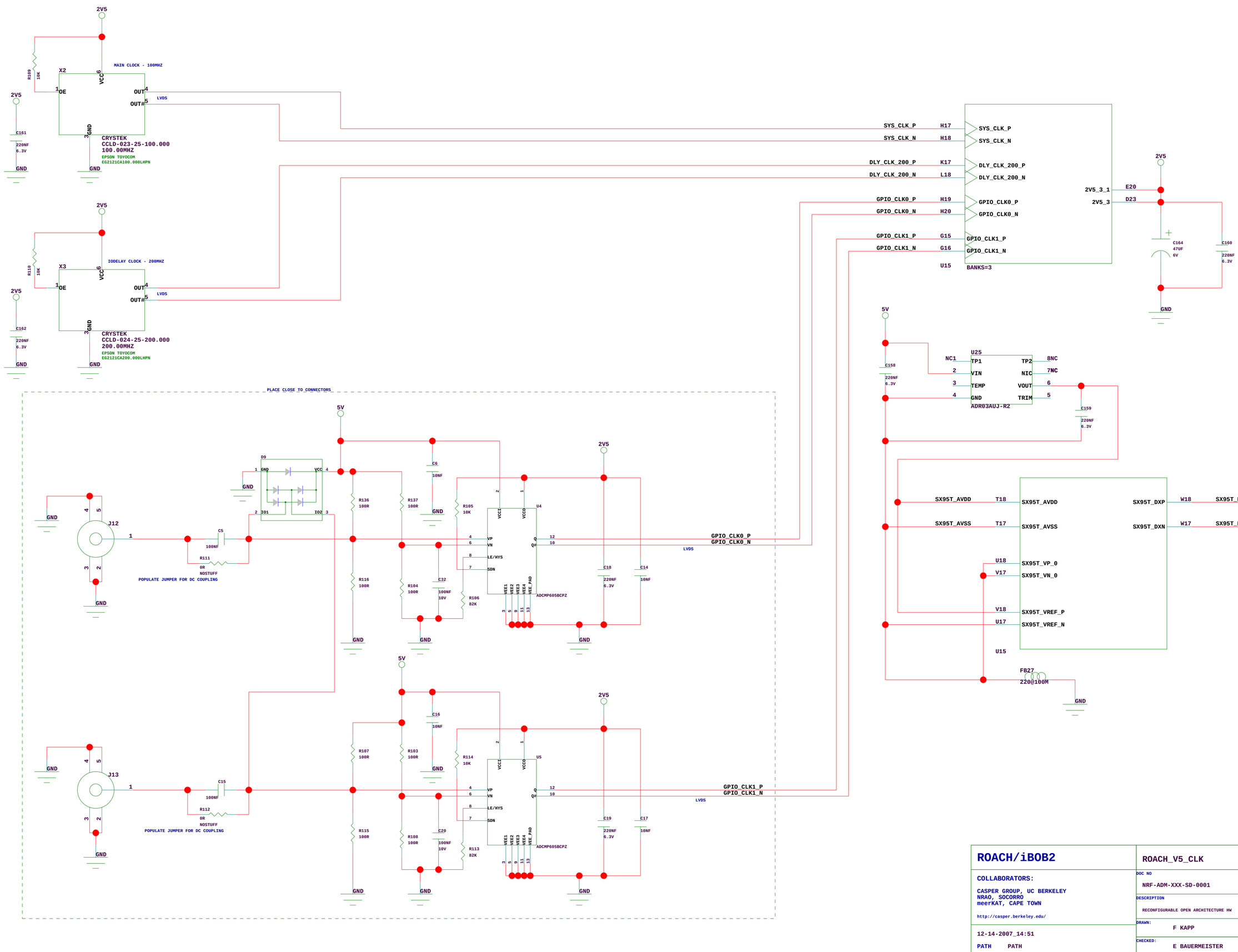
http://casper.berkeley.edu/

12-14-2007_14:51

PATH PATH

ROACH_ADC_1

DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 5 OF 25



ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 12 OF 25
12-14-2007_14:51 PATH PATH	

ROACH/iBOB2	**ROACH_TRANSCEIVERS0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 2 OF 25
12-14-2007_14:51 PATH PATH	

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

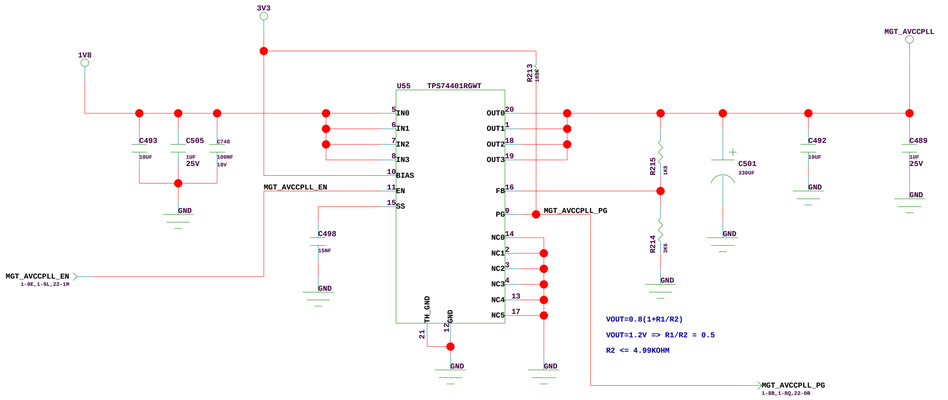
G4 AND G8 CONNECTED IN 2X2 MODULE

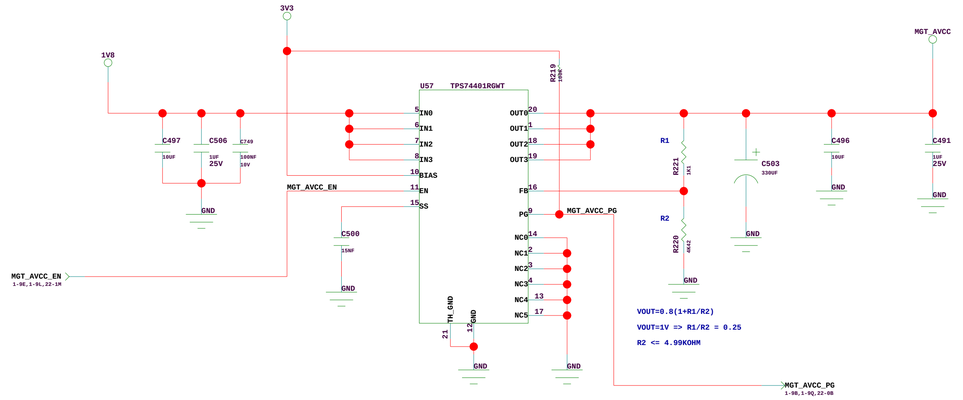
OPTICAL MODULE FAULT - RED LED

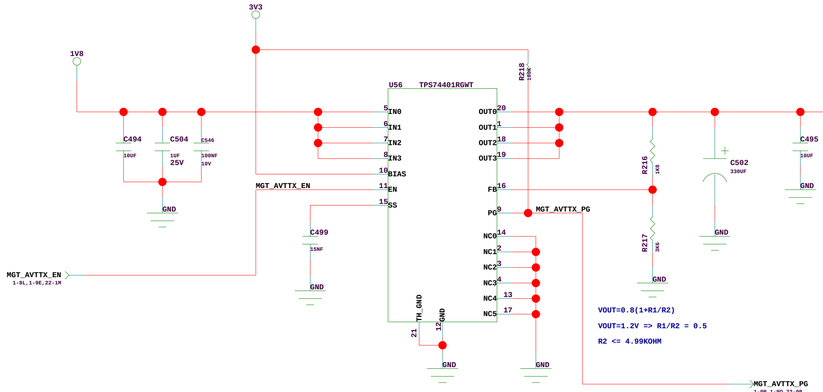
CCLD-023-25-156.250
156.25MHZ

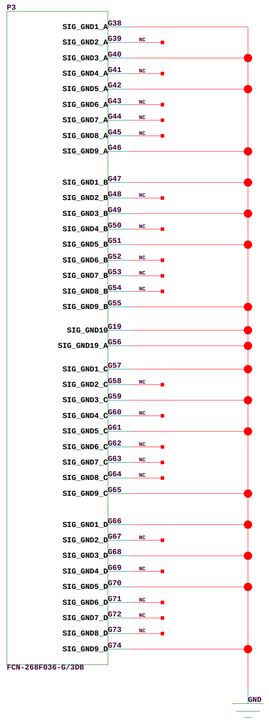
FCN-268F036-G/3DB

ROACH/iBOB2	ROACH_TRANSCEIVERS2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
12-14-2007_14:51	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 3 OF 25

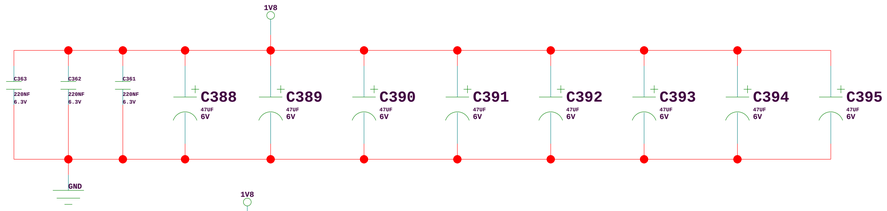


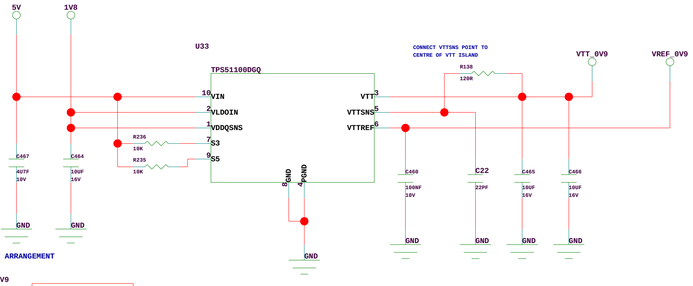


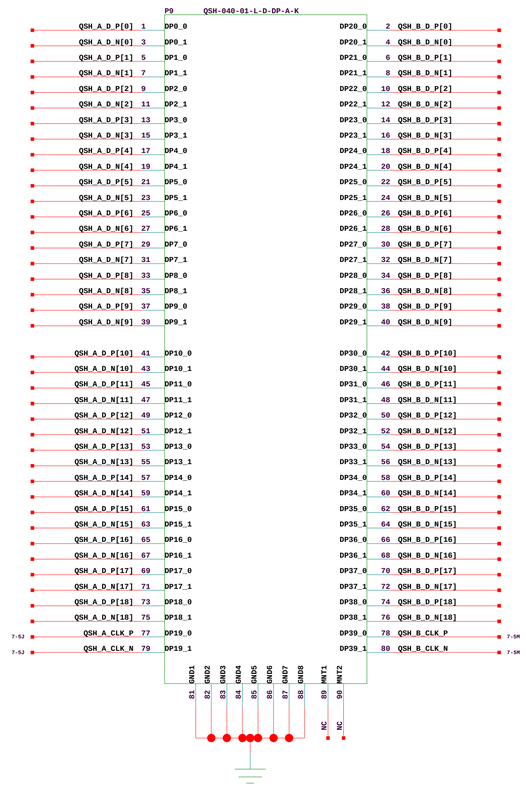


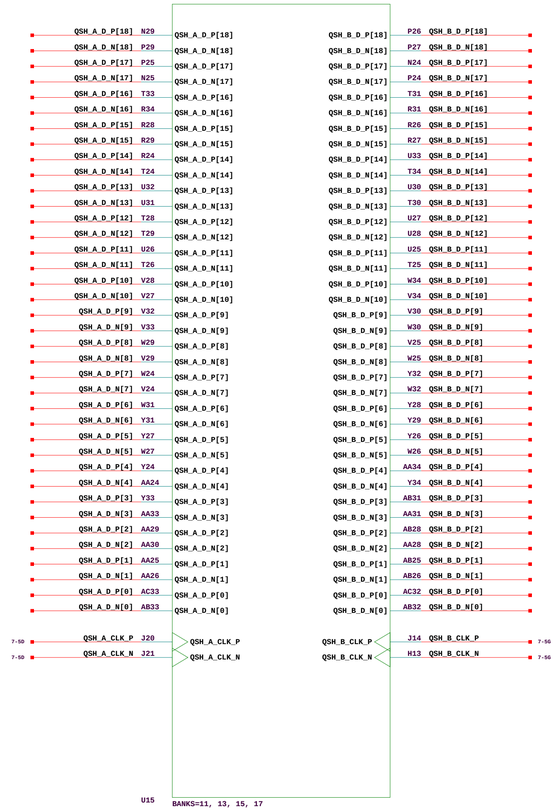


ROACH/iBOB2	**ROACH_TRANSCEIVERS_PSU**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
12-14-2007_14:51	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 17 OF 25


1V8
C353 220NF 6.3V
C352 220NF 6.3V
C351 220NF 6.3V
C388 47UF 6V
C389 47UF 6V
C390 47UF 6V
C391 47UF 6V
C392 47UF 6V
C393 47UF 6V
C394 47UF 6V
C395 47UF 6V
GND


5V
1V8
U33
TPS51100DGQ
VIN
VLDOIN
VDDQSNS
S3
S5
R236 10K
R235 10K
C657 4U7F 10V
C664 100F 16V
GND
CONNECT VTTSNS POINT TO CENTRE OF VTT ISLAND
R138 120R
VTT
VTTSNS
VTTREF
VTT_0V9
VREF_0V9
C669 100NF 10V
C22 22PF
C665 10UF 16V
C666 10UF 16V





ROACH/iBOB2	**ROACH_DIFF_GPIO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
12-14-2007_14:51 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25

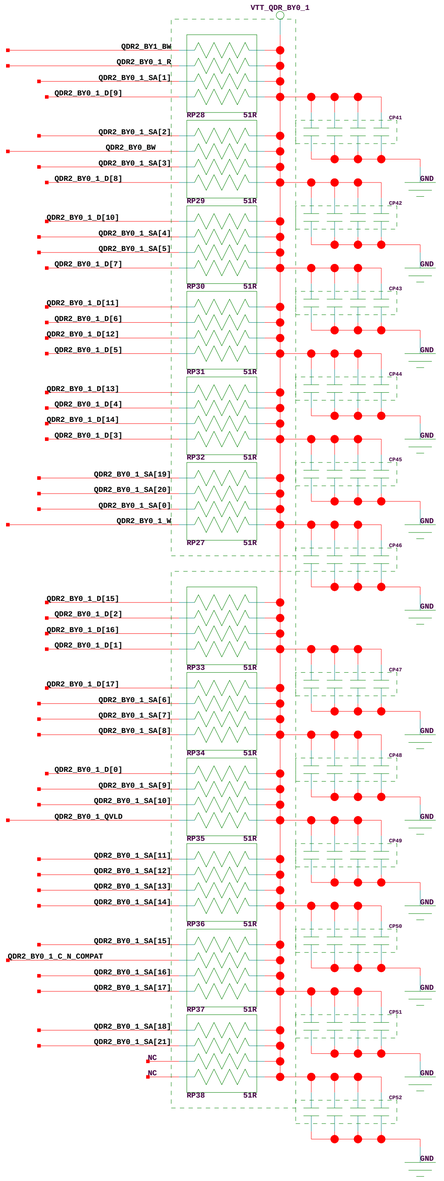
GPIOLVC18[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

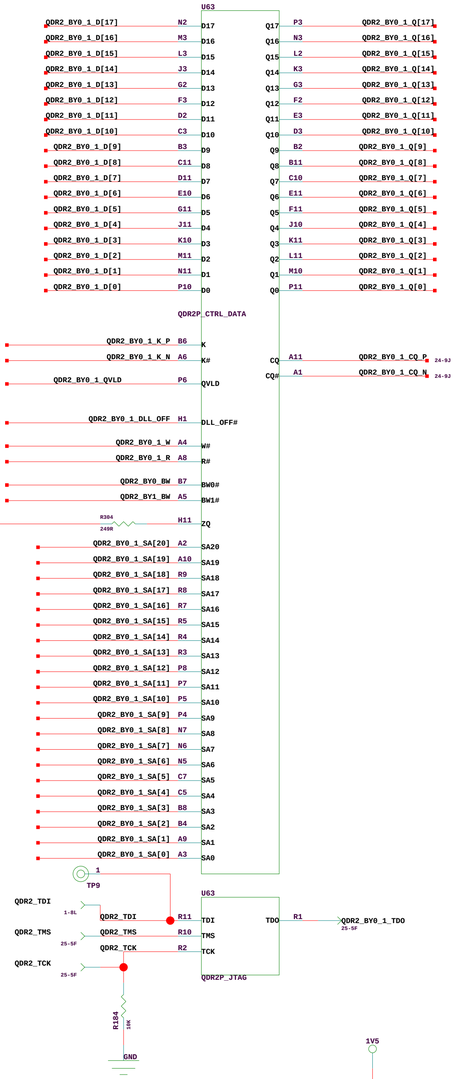
GPIOLVC25[0] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

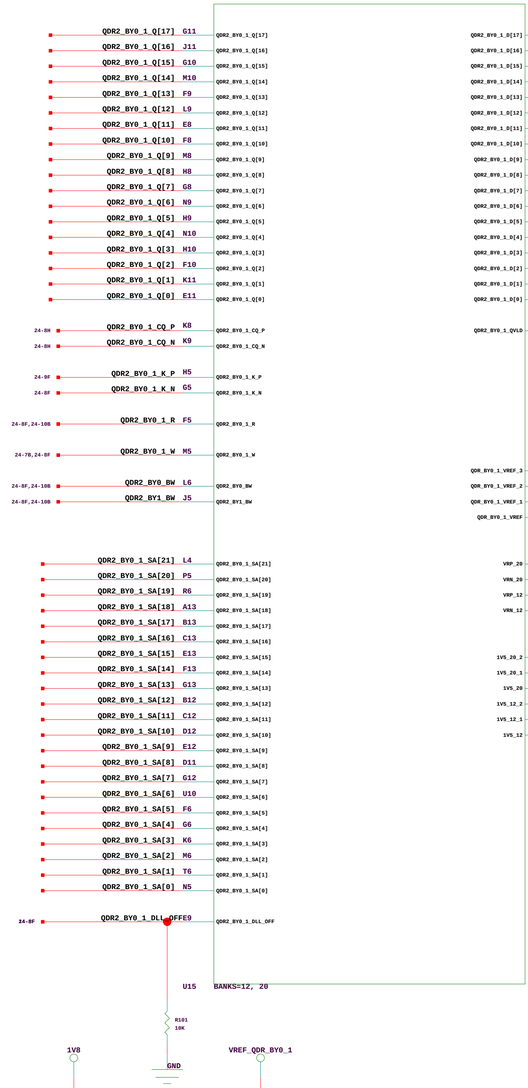
IO VOLTAGE LEVEL SELECT	
1-2: 3.3V	DEFAULT
2-3: 2.5V	

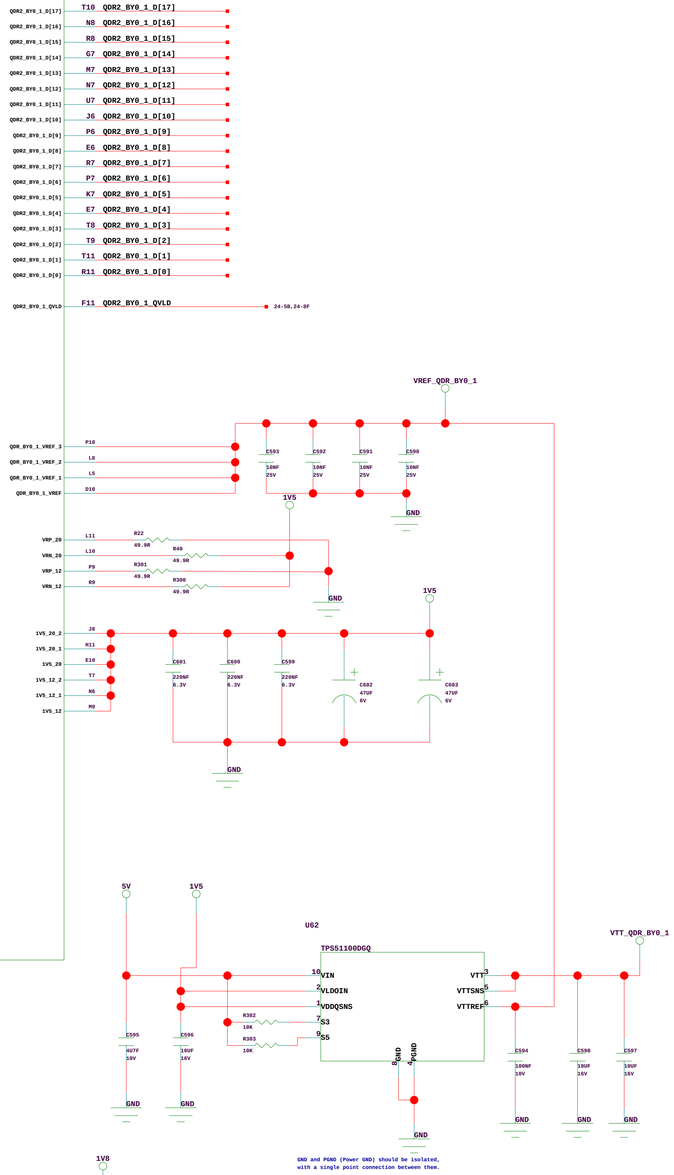
IF CR10 IS ON, CLOCK CAPABLE GPIO'S ARE OUTPUTS

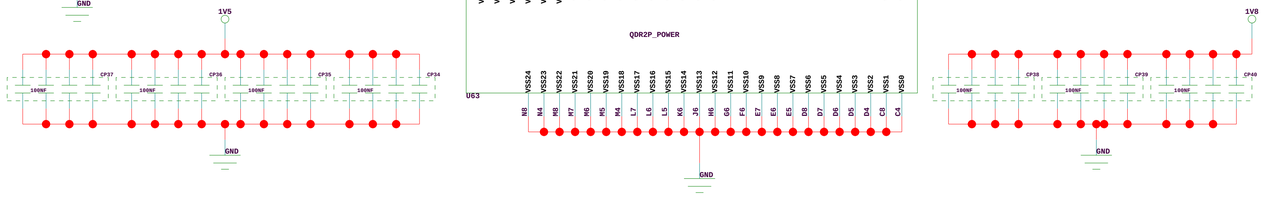
ROACH/iBOB2	ROACH_GPIO_MISC
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
12-14-2007_14:51 PATH PATH	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MM
	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 10 OF 25



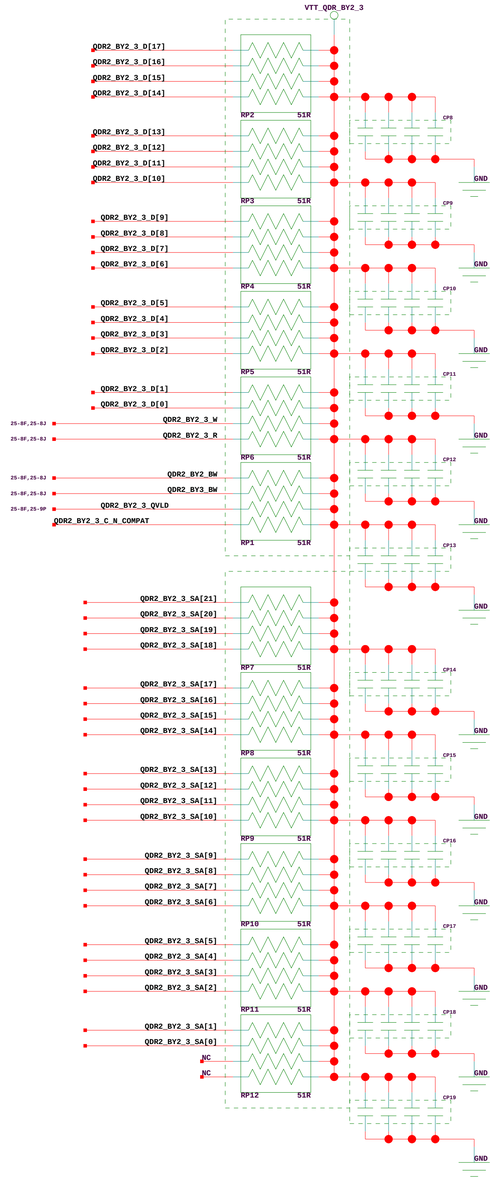


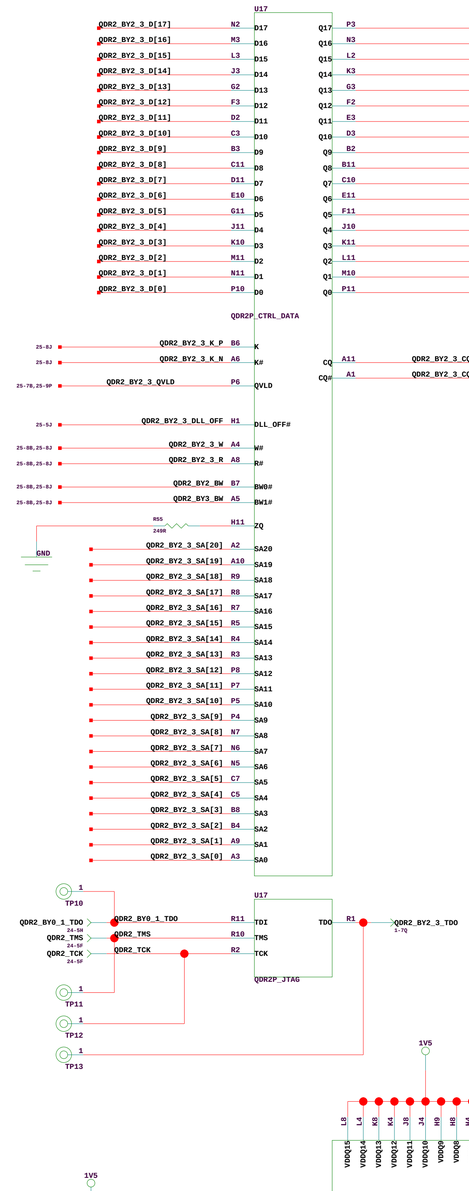


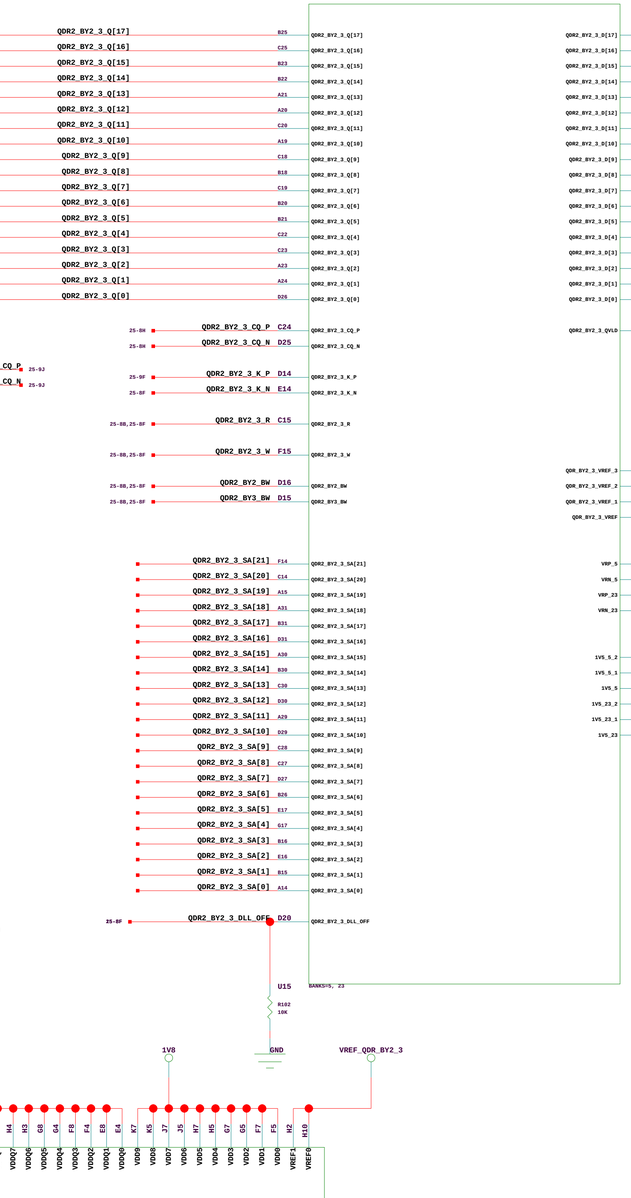


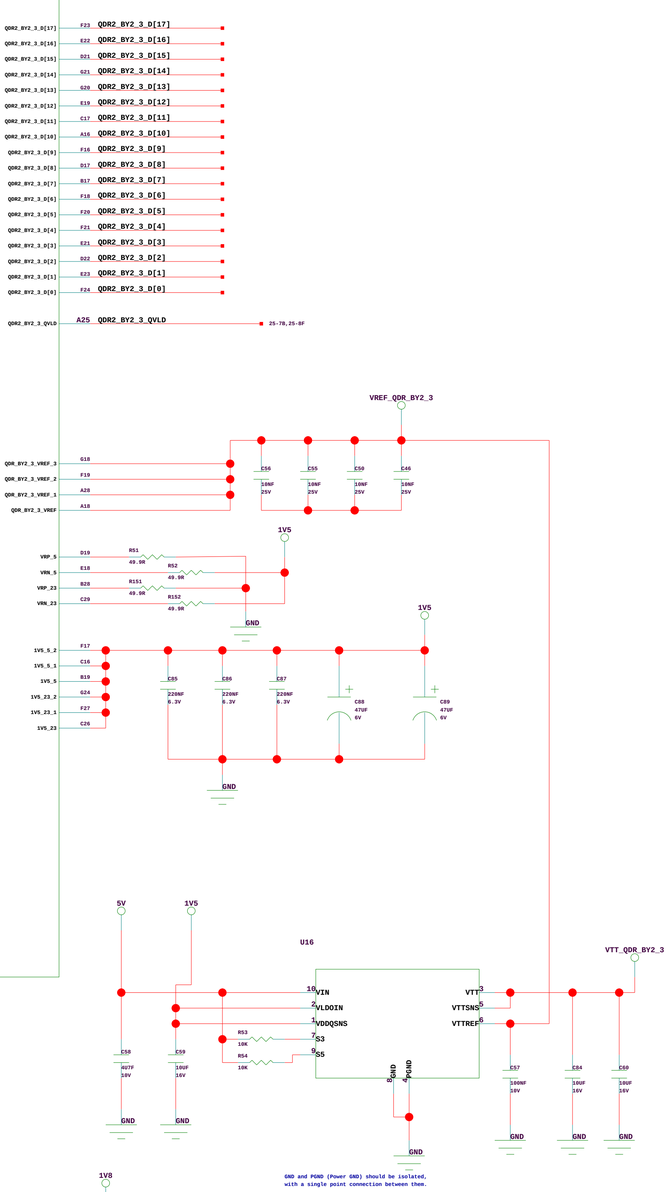


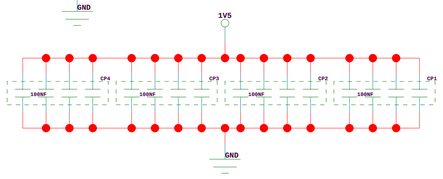
ROACH/iBOB2		**ROACH_QDR2P_BY0_1**	
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/		DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
		DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
12-14-2007_14:51 PATH PATH		DRAWN: F KAPP	APPR:
		CHECKED: E BAUERMEISTER	SHEET: 24 OF 25

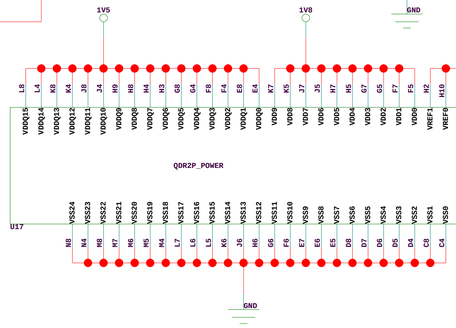


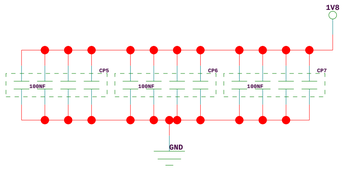








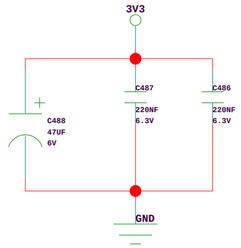


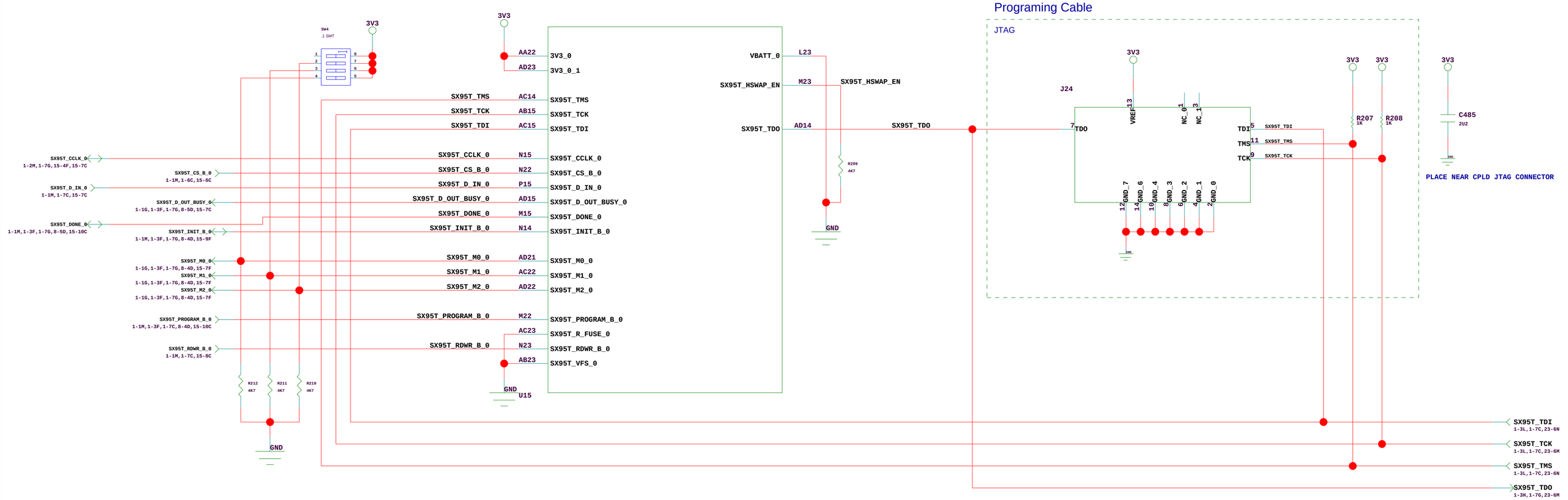


ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 25 OF 25
12-14-2007_14:51 PATH PATH	

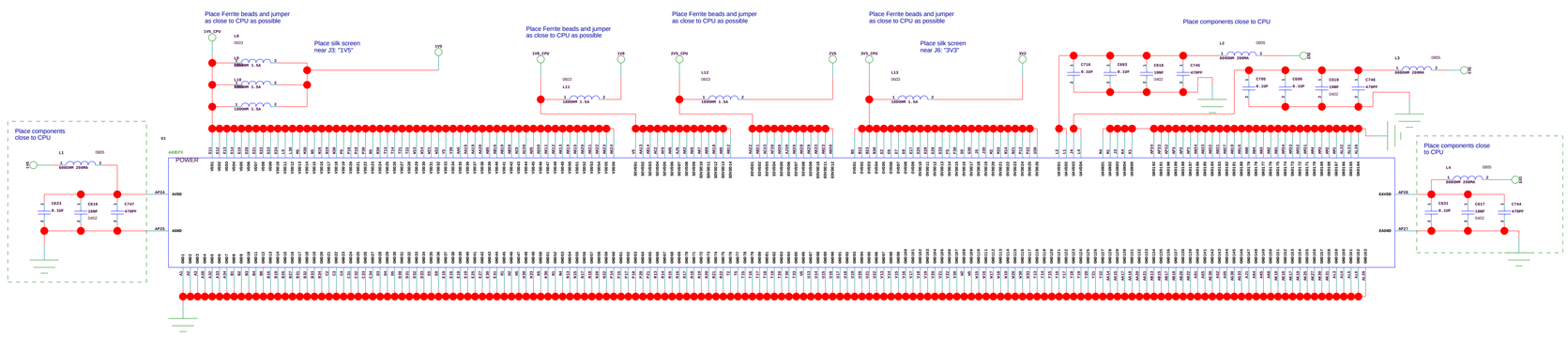
TBD

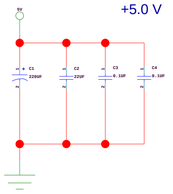
VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

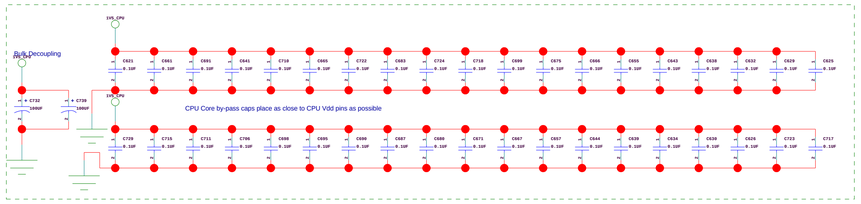


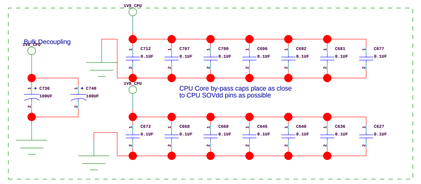


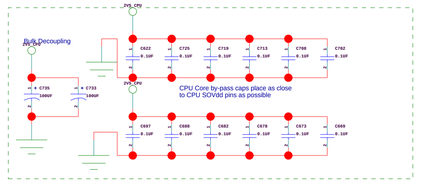
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
12-14-2007_14:51 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25

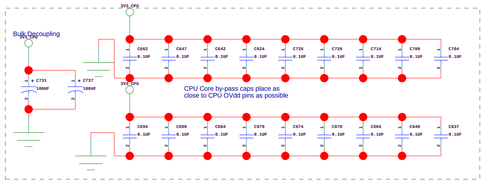


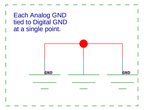










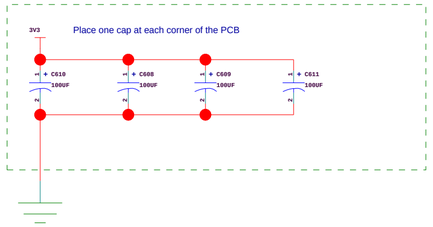


REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: **CASPER GROUP, UC BERKELEY** **NRAO, SOCORRO** **meerKAT, CAPE TOWN** http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MK DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET: 20 OF 25
12-14-2007_14:51 PATH PATH	

REMOVED 3V3 GENERATION



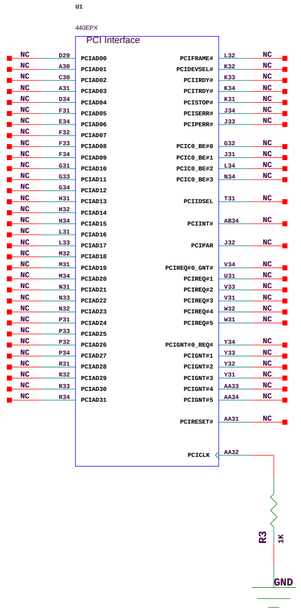
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET: 9 OF 25
12-14-2007_14:51 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
12-14-2007_14:51 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

Place nearest PHY pin 96

2V5 C533 10NF

Place nearest PHY pin 101

2V5 C534 10NF

Place nearest PHY pin 98

1V8 R233 1R C536 22UF C511 10NF

Place nearest PHY pin 100

1V8 R232 1R C535 22UF C512 10NF

Place as close to PHY CORE VDD power pins as possible

1V8 C526 10NF C527 100NF C525 10NF C528 100NF C530 10NF C529 100NF C531 10NF C532 100NF

Place as close to PHY IO VDD power pins as possible

2V5 C513 10NF C514 100NF C515 10NF C516 100NF C517 10NF C518 100NF C519 10NF C520 100NF C521 10NF C522 100NF C523 10NF C524 100NF

U3 440EP4 Gig-Ethernet RGMII1

GMC1_TXD0 AF26 NC
GMC1_TXD1 AL26 NC
GMC1_TXD2 AN26 NC
GMC1_TXD3 AK26 NC
GMC1_TXCTL AK24 NC
GMC1_TXCLK AK32 NC
GMC1_RXD0 AK29 NC
GMC1_RXD1 AF30 NC
GMC1_RXD2 AF31 NC
GMC1_RXD3 AK30 NC
GMC1_RXCTL AL33 NC
GMC1_RXCLK AJ32 NC

UNUSED SECOND ETHERNET MAC

U1 440EP4 Gig-Ethernet RGMII0

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups. Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

Place resistors as close to CPU as possible and keep all traces lengths equal

GMCRXD0 AL24 R241 22R
GMCRXD1 AN23 R240 22R
GMCRXD2 AP25 R237 22R
GMCRXD3 AL25 R242 22R
GMCRXCTL AN24 R243 22R
GMCRXCLK AP27 R244 22R
GMCTXCLK AL27 R229 22R
GMCTXD0 AL28 R245 22R
GMCTXD1 AP29 R246 22R
GMCTXD2 AP28 R247 22R
GMCTXD3 AL29 R248 22R
GMCTXCTL AJ31 R249 22R
GMCTXCLK AN28 R250 22R

ETHERNET Mgt.

GMCMDCLK AL34
GMCMDIO AK34
GMCREFCLK_125MHZ AJ33

R267 1K 1-4E,18-3C GMCMDCLK
R268 1K 1-4E,18-3C GMCMDIO
R269 1K 2V5

Place resistors close to PHY all trace lengths equal

R274 22R GMCRXD0
R275 22R GMCRXD1
R276 22R GMCRXD2
R278 22R GMCRXD3
R279 22R GMCRXCLK
R277 22R GMCMDCLK

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

NC RDJECTPKT0 AM23
NC RDJECTPKT1 AL23

U56 DP83865DVH

GMCRXD0 75 TXD0/TX0
GMCRXD1 76 TXD1/TX1
GMCRXD2 72 TXD2/TX2
GMCRXD3 73 TXD3/TX3
69 TXD4
67 TXD5
65 TXD6
63 TXD7
GMCRXCTL 62 TX_EN/TXEN_ER
61 TX_ER
GMCRXCLK 60 TX_CLK/RGMII_SEL1
59 CRS/RGMII_SEL0
58 COL
55 RXD0/RX0
54 RXD1/RX1
53 RXD2/RX2
51 RXD3/RX3
50 RXD4
47 RXD5
45 RXD6
44 RXD7
43 RX_DV/RCK
41 RX_ER/RXDV_ER
57 RX_CLK
81 MDC
80 MDIO
85 CLK_TO_MAC
33 RESETn
3 INTERRUPTn
86 CLK_IN
87 CLK_OUT
28 TDO
31 TDI
26 TCK
27 TMS
32 TRSTn

GETH0_RST# 1-2M,1-4B,15-10F
GETH0_INT# 1-3H,1-4E,23-7N
CLK_GETH0_25MHZ 1-3L,1-4B,23-5G

R136 2K7

Place jumpers in line with signals

1-4E,18-4D GMCMDIO JP24
1-4E,18-4D GMCMDCLK JP25

MDC_P 100 MDIO_0P
MDC_N 109 MDIO_0N
MDIO_P 114 MDIO_1P
MDIO_N 115 MDIO_1N
MDC_P 120 MDIO_2P
MDC_N 121 MDIO_2N
MDIO_P 126 MDIO_3P
MDIO_N 127 MDIO_3N

R254 49.9R 1% C507 10NF
R257 49.9R 1% C508 10NF
R258 49.9R 1% C509 10NF
R260 49.9R 1% C510 10NF

Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5

VDD_SEL_STRAP 34
MAC_CLK_EN_STRAP 88
MDIX_EN_STRAP 89
MULTI_EN_STRAP 84
L10_L100 10
L100_L100 9
L10_L10 8
LED_ACT 7
LED_DUPLEX 13
PHYAD0_STRAP 14
PHYAD1_STRAP 17
PHYAD2_STRAP 16
PHYAD3_STRAP 15
PHYAD4_STRAP 95

LINK1000_LED/GM_EN_STRAP
LINK100_LED/DUPLEX_STRAP
LINK10_LED/RLED/SPEED1_STRAP
ACTIVITY_LED/SPEED0_STRAP
DUPLEX_LED/PHYAD0_STRAP

R265 2K2 NOSTUFF
R264 2K2 NOSTUFF
R266 2K2 NOSTUFF

BG_REF 102 R253 9K76
TX_TCLK NC
NON_IEEE_STRAP NC
RESERVED1 NC
RESERVED2 NC
RESERVED NC

Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

Bottom LED
Green/Toggle = ACTIVITY

J26 HFJ11-1G02E-L12
GRN GRN_YEL
TRDP 1 TRDN 2 TRCP 3 TRCN 4 TDDP 5 TDDN 6 TDCP 7 TDCN 8
VCC 9 GND 10 MNT1 15 MNT2 16 NC NC
CASE1 17 CASE2 18 GND
2V5 C537 22UF

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

R284 2K2 JP20 R269 2K2 JP21 R270 2K2 JP22 R271 2K2 JP23

JP11 R243 2K2 R244 330R DUPLEX LED D6 JP10
JP13 R245 2K2 R246 330R JP12
JP15 R247 2K2 R248 330R L10 LED D7 JP14
JP17 R249 2K2 R250 330R L100 LED D8 JP16
JP18 R252 2K2 R251 330R JP19

ROACH/iBOB2	ROACH_PPC_ETH1
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
12-14-2007_14:51 PATH PATH	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 18 OF 25

U1
USB 2.0 DEVICE
440EPX

USB2CLK — A5 — NC

GPIO28/USB2TXVAL — C6 — NC
USB2TXRDY_REFEN — B6
USB2RXACT_HOLDREQ_RCVINH — D7 — NC
USB2RXVAL_LEAKTEST2 — C8 — NC
GPIO27/USB2RXERR_EXTREQ# — A4 — SX95T_DONE_0 ⟷ SX95T_DONE_0
1-1M,1-3F,1-7G,15-10C

GPIO30/USB2XCVRSEL_EXTACK# — M3 — SX95T_INIT_B_0 ⟷ SX95T_INIT_B_0
GPIO31/USB2TERMSEL_BUSREQ — P4
1-1M,1-3F,1-7G,15-9F

USB2LS0_DRVINH1 — R2 — NC — SX95T_M0_0
USB2LS1_LEAKTEST_HOLDPRI — P1 — NC
1-1G,1-3F,1-7G,15-7F,16-3B

GPIO32/USB2OM0 — R3 — SX95T_M1_0
GPIO33/USB2OM1 — R4
1-1G,1-3F,1-7G,15-7F,16-3B

GPIO29/USB2SUSP_HOLDACK — C5 — SX95T_M2_0
1-1G,1-3F,1-7G,15-7F,16-3B

SX95T_PROGRAM_B_0
1-1M,1-3F,1-7C,15-10C,16-3B

NOTE:
USB HOST ONLY

USB 2.0 PHY
HOST/DEVICE

USB2XCVR — J2 — USB2_XCVR_D+
USB2XCVR# — J1 — USB2_XCVR_D-
USB2REXT — L3 — R182 3K4 0402
USB2XTAL — N2
USB2XTAL# — N3

CLK_USB2.0_48MHZ
1-3B,1-3L,23-4G

5V
PTC1 1206L050 500MA
C614 220UF 10V
C612 100NF 10V
C613 1NF 50V

CRITICAL PLACEMENT
Place SP2 very close to P6

SP2 SOT23 PGB102ST23WR
PGB102ST23WR SP2
GND
VR4 0603 5.5V 20A

P6 NONE 1X4 USBA
1 VCC
2 D-
3 D+
4 GND
5
6
292303-1
GND

ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 8 OF 25
12-14-2007_14:51 PATH PATH	

DDR_PA[15:0]

DDR_PD[63:0]

U1

DDR SDRAM

44GEPX

DDR_PD0	AB2	MEMDATA00	MEMADDR00
DDR_PD1	AF2	MEMDATA01	MEMADDR01
DDR_PD2	AK5	MEMDATA02	MEMADDR02
DDR_PD3	AL28	MEMDATA03	MEMADDR03
DDR_PD4	AL22	MEMDATA04	MEMADDR04
DDR_PD5	AK22	MEMDATA05	MEMADDR05
DDR_PD6	AK21	MEMDATA06	MEMADDR06
DDR_PD7	AF21	MEMDATA07	MEMADDR07
DDR_PD8	AF28	MEMDATA08	MEMADDR08
DDR_PD9	AL18	MEMDATA09	MEMADDR09
DDR_PD10	AK17	MEMDATA10	MEMADDR10
DDR_PD11	AF17	MEMDATA11	MEMADDR11
DDR_PD12	AK26	MEMDATA12	MEMADDR12
DDR_PD13	AF16	MEMDATA13	MEMADDR13
DDR_PD14	AK16	MEMDATA14	
DDR_PD15	AL15	MEMDATA15	
DDR_PD16	AK10	MEMDATA16	
DDR_PD17	AF10	MEMDATA17	
DDR_PD18	AL11	MEMDATA18	
DDR_PD19	AF14	MEMDATA19	
DDR_PD20	AL17	MEMDATA20	
DDR_PD21	AK17	MEMDATA21	
DDR_PD22	AK15	MEMDATA22	
DDR_PD23	AK15	MEMDATA23	
DDR_PD24	AF13	MEMDATA24	
DDR_PD25	AK13	MEMDATA25	
DDR_PD26	AF12	MEMDATA26	
DDR_PD27	AL12	MEMDATA27	
DDR_PD28	AK14	MEMDATA28	
DDR_PD29	AK14	MEMDATA29	
DDR_PD30	AL13	MEMDATA30	
DDR_PD31	AK12	MEMDATA31	
DDR_PD32	AF3	MEMDATA32	
DDR_PD33	AF1	MEMDATA33	
DDR_PD34	AD4	MEMDATA34	
DDR_PD35	AD3	MEMDATA35	
DDR_PD36	AB3	MEMDATA36	
DDR_PD37	AF2	MEMDATA37	
DDR_PD38	AE2	MEMDATA38	
DDR_PD39	AE1	MEMDATA39	
DDR_PD40	AC3	MEMDATA40	
DDR_PD41	AC1	MEMDATA41	
DDR_PD42	AA4	MEMDATA42	
DDR_PD43	AA3	MEMDATA43	
DDR_PD44	AD2	MEMDATA44	
DDR_PD45	AC4	MEMDATA45	
DDR_PD46	AB1	MEMDATA46	
DDR_PD47	AB2	MEMDATA47	
DDR_PD48	Y3	MEMDATA48	
DDR_PD49	Y2	MEMDATA49	
DDR_PD50	Y4	MEMDATA50	
DDR_PD51	V3	MEMDATA51	
DDR_PD52	AA2	MEMDATA52	
DDR_PD53	AA1	MEMDATA53	
DDR_PD54	W3	MEMDATA54	
DDR_PD55	W1	MEMDATA55	
DDR_PD56	V1	MEMDATA56	
DDR_PD57	U2	MEMDATA57	
DDR_PD58	T4	MEMDATA58	
DDR_PD59	R1	MEMDATA59	
DDR_PD60	V2	MEMDATA60	
DDR_PD61	T1	MEMDATA61	
DDR_PD62	T3	MEMDATA62	
DDR_PD63	T2	MEMDATA63	

		MEMADDR00	AM5
		MEMADDR01	AP4
		MEMADDR02	AP5
		MEMADDR03	AM6
		MEMADDR04	AP6
		MEMADDR05	AN6
		MEMADDR06	AL7
		MEMADDR07	AN7
		MEMADDR08	AM7
		MEMADDR09	AP7
		MEMADDR10	AL8
		MEMADDR11	AL9
		MEMADDR12	AN8
		MEMADDR13	AN4
DDR_PBA0	AJ3	BA0	
DDR_PBA1	AN3	BA1	
DDR_PBA2	AP8	BA2	
DDR_PRAS#	AJ4	RAS#	
DDR_PCAS#	AN4	CAS#	
DDR_PWE#	AJ2	WE#	
DDR_PDM0	AL21	DM0	
DDR_PDM1	AP18	DM1	
DDR_PDM2	AP15	DM2	
DDR_PDM3	AL14	DM3	
DDR_PDM4	AD4	DM4	
DDR_PDM5	AB3	DM5	
DDR_PDM6	Y3	DM6	
DDR_PDM7	Y2	DM7	
DDR_PDM8	AP10	DM8	
DDR_PDQS0	AR21	DQS0	
DDR_PDQS1	AM19	DQS1	
DDR_PDQS2	AL16	DQS2	
DDR_PDQS3	AM13	DQS3	
DDR_PDQS4	AE3	DQS4	
DDR_PDQS5	AB4	DQS5	
DDR_PDQS6	W3	DQS6	
DDR_PDQS7	U4	DQS7	
DDR_PDQS8	AP10	DQS8	
DDR_PODT0	AN3	MEMODT0	
DDR_PODT1	AR1	MEMODT1	
DDR_PCS0#	AN2	BANKSELA0	
DDR_PCS1#	AM1	BANKSELA1	
DDR_PCKE	AN9	MEMCKE0	
DDR_CLKOUT	AL1	MEMCLKOUT0	
DDR_CLKOUT#	AM1	MEMCLKOUT0	

PPC_ECC0	AR11	ECC0	
PPC_ECC1	AL11	ECC1	
PPC_ECC2	AM9	ECC2	
PPC_ECC3	AL9	ECC3	
PPC_ECC4	AP11	ECC4	
PPC_ECC5	AN11	ECC5	
PPC_ECC6	AM10	ECC6	
PPC_ECC7	AP9	ECC7	

SVREF1A	Y4	
SVREF2A	AL19	
SVREF1B	AF4	
SVREF2B	AL19	

DDR2 Clock line must be 500ps longer than Address/Command lines
To compensate for additional loading when using unbuffered DIMM's
See P84 of PPC440EPx for more information

Place parts as close to CPU as possible

5V 1V8 DDR_VREF_0V9

C158 0.10F
C148 0.10F
C151 0.10F 0402
C152 0.10F 0402
C149 10NF 0402

U32

TPS51100DGQ

VIN	10	5V
VLDOIN	2	1V8
VDDQSNS	1	DDR_VTT
S3	7	5V
S5	9	5V
VTT	3	DDR_VTT
VTTSNS	5	DDR_VTT
VTTREF	6	DDR_VREF_0V9
GND	8	GND
PGND	4	GND

R230 10K
R229 10K
R6 120R

C459 4U7F 10V
C456 10UF 16V
C453 100NF 10V
C21 22PF
C457 10UF 16V
C458 10UF 16V

GND

J8

PPC_ECC7	11-6D	168	DDR2_DIMM_CB7
PPC_ECC6	11-6D	167	DDR2_DIMM_CB6
PPC_ECC5	11-7D	162	DDR2_DIMM_CB5
PPC_ECC4	11-7D	161	DDR2_DIMM_CB4
PPC_ECC3	11-7D	49	DDR2_DIMM_CB3
PPC_ECC2	11-7D	48	DDR2_DIMM_CB2
PPC_ECC1	11-7D	43	DDR2_DIMM_CB1
PPC_ECC0	11-7D	42	DDR2_DIMM_CB0
DDR_PDQ63		236	DDR2_DIMM_DQ[63]
DDR_PDQ62		235	DDR2_DIMM_DQ[62]
DDR_PDQ61		230	DDR2_DIMM_DQ[61]
DDR_PDQ60		229	DDR2_DIMM_DQ[60]
DDR_PDQ59		117	DDR2_DIMM_DQ[59]
DDR_PDQ58		116	DDR2_DIMM_DQ[58]
DDR_PDQ57		111	DDR2_DIMM_DQ[57]
DDR_PDQ56		110	DDR2_DIMM_DQ[56]
DDR_PDQ55		227	DDR2_DIMM_DQ[55]
DDR_PDQ54		226	DDR2_DIMM_DQ[54]
DDR_PDQ53		218	DDR2_DIMM_DQ[53]
DDR_PDQ52		217	DDR2_DIMM_DQ[52]
DDR_PDQ51		108	DDR2_DIMM_DQ[51]
DDR_PDQ50		107	DDR2_DIMM_DQ[50]
DDR_PDQ49		99	DDR2_DIMM_DQ[49]
DDR_PDQ48		98	DDR2_DIMM_DQ[48]
DDR_PDQ47		215	DDR2_DIMM_DQ[47]
DDR_PDQ46		214	DDR2_DIMM_DQ[46]
DDR_PDQ45		209	DDR2_DIMM_DQ[45]
DDR_PDQ44		208	DDR2_DIMM_DQ[44]
DDR_PDQ43		96	DDR2_DIMM_DQ[43]
DDR_PDQ42		95	DDR2_DIMM_DQ[42]
DDR_PDQ41		90	DDR2_DIMM_DQ[41]
DDR_PDQ40		89	DDR2_DIMM_DQ[40]
DDR_PDQ39		206	DDR2_DIMM_DQ[39]
DDR_PDQ38		205	DDR2_DIMM_DQ[38]
DDR_PDQ37		200	DDR2_DIMM_DQ[37]
DDR_PDQ36		199	DDR2_DIMM_DQ[36]
DDR_PDQ35		87	DDR2_DIMM_DQ[35]
DDR_PDQ34		86	DDR2_DIMM_DQ[34]
DDR_PDQ33		81	DDR2_DIMM_DQ[33]
DDR_PDQ32		80	DDR2_DIMM_DQ[32]
DDR_PDQ31		159	DDR2_DIMM_DQ[31]
DDR_PDQ30		158	DDR2_DIMM_DQ[30]
DDR_PDQ29		153	DDR2_DIMM_DQ[29]
DDR_PDQ28		152	DDR2_DIMM_DQ[28]
DDR_PDQ27		40	DDR2_DIMM_DQ[27]
DDR_PDQ26		39	DDR2_DIMM_DQ[26]
DDR_PDQ25		34	DDR2_DIMM_DQ[25]
DDR_PDQ24		33	DDR2_DIMM_DQ[24]
DDR_PDQ23		150	DDR2_DIMM_DQ[23]
DDR_PDQ22		149	DDR2_DIMM_DQ[22]
DDR_PDQ21		144	DDR2_DIMM_DQ[21]
DDR_PDQ20		143	DDR2_DIMM_DQ[20]
DDR_PDQ19		31	DDR2_DIMM_DQ[19]
DDR_PDQ18		30	DDR2_DIMM_DQ[18]
DDR_PDQ17		25	DDR2_DIMM_DQ[17]
DDR_PDQ16		24	DDR2_DIMM_DQ[16]
DDR_PDQ15		141	DDR2_DIMM_DQ[15]
DDR_PDQ14		140	DDR2_DIMM_DQ[14]
DDR_PDQ13		132	DDR2_DIMM_DQ[13]
DDR_PDQ12		131	DDR2_DIMM_DQ[12]
DDR_PDQ11		22	DDR2_DIMM_DQ[11]
DDR_PDQ10		21	DDR2_DIMM_DQ[10]
DDR_PDQ9		13	DDR2_DIMM_DQ[9]
DDR_PDQ8		12	DDR2_DIMM_DQ[8]
DDR_PDQ7		129	DDR2_DIMM_DQ[7]
DDR_PDQ6		128	DDR2_DIMM_DQ[6]
DDR_PDQ5		123	DDR2_DIMM_DQ[5]
DDR_PDQ4		122	DDR2_DIMM_DQ[4]
DDR_PDQ3		10	DDR2_DIMM_DQ[3]
DDR_PDQ2		9	DDR2_DIMM_DQ[2]
DDR_PDQ1		4	DDR2_DIMM_DQ[1]
DDR_PDQ0		3	DDR2_DIMM_DQ[0]
		101	DDR2_DIMM_SA2
		240	DDR2_DIMM_SA1
		239	DDR2_DIMM_SA0
		120	DDR2_DIMM_SCL
		119	DDR2_DIMM_SDA

879160001

1V8 R228 2K2 PPC_DDR2_DIMM_SCL PPC_DDR2_DIMM_SDA 4K7

GND

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA1	11-90,11-10L
DDR2_DIMM_BA[1]	190	DDR_PBA2	11-8L,11-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	11-7L,11-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	11-7L,11-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	11-7L,11-9D
DDR2_DIMM_CK_P[2]	220	NC	
DDR2_DIMM_CK_N[2]	221	NC	
DDR2_DIMM_CK_P[1]	137	NC	
DDR2_DIMM_CK_N[1]	138	NC	
DDR2_DIMM_CK_P[0]	185	DDR_CLKOUT	
DDR2_DIMM_CK_N[0]	186	DDR_CLKOUT#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	11-8D,11-11L
DDR2_DIMM_DM_CB	164	DDR_PDM8	11-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	11-9D
DDR2_DIMM_DM[6]	223	DDR_PDM6	11-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	11-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	11-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	11-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	11-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	11-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	11-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	11-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	11-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	11-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	11-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	11-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	11-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	11-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	11-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	11-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	11-7L,11-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	
DDR2_DIMM_S#[1]	76	DDR_PCS1#	11-7L,11-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	11-7L,11-8D
PAR_OUT	55	PPC_DDR2_ERROR	1 TP4
PAR_IN	68	PAR_IN	1 TP5

879160001

R226 22R 4K7

PPC_DDR2_RESET_N 1-2B,1-2M,15-10F

C455 5PF 50V

GND

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

DDR_VTT

11-6K,11-8D	DDR_PCKE	RP24	CP26
	DDR_PA15		
	DDR_PA14		
11-8K,11-9D	DDR_PBA1		
	DDR_PA12	RP23	CP28
	DDR_PA11		
	DDR_PA9		
	NC		
	DDR_PA7	RP22	CP29
	DDR_PA8		
	DDR_PA6		
	DDR_PA5		
	DDR_PA4	RP21	CP30
	DDR_PA3		
	DDR_PA1		
	DDR_PA2		
11-8K,11-9D	DDR_PA0	RP25	CP32
	DDR_PBA2		
11-3K,11-9D	DDR_PA10		
11-8K,11-9D	DDR_PBA0		
11-7K,11-9D	DDR_PRAS#	RP26	CP31
11-3K,11-9D	DDR_PWE#		
11-3K,11-9D	DDR_PCS0#		
11-8K,11-9D	DDR_PCAS#		
11-3K,11-9D	DDR_PCS1#	RP19	CP33
11-9D	DDR_PODT0		
	DDR_PA13		
11-8D	DDR_PODT1		

GND

J8

VSS_64	237	69	VDD_5
VSS_63	234	67	VDD_4
VSS_62	231	64	VDD_3
VSS_61	228	59	VDD_2
VSS_60	225	53	VDD_1
VSS_59	222		
VSS_58	219		
VSS_57	216		
VSS_56	213		
VSS_55	210		
VSS_54	207		
VSS_53	204		
VSS_52	201		
VSS_51	198		
VSS_50	169		
VSS_49	166		
VSS_48	163		
VSS_47	160		
VSS_46	157		
VSS_45	154		
VSS_44	151		
VSS_43	148		
VSS_42	145		
VSS_41	142		
VSS_40	139		
VSS_39	136		
VSS_38	133		
VSS_37	130		
VSS_36	127		
VSS_35	124		
VSS_34	121		
VSS_33	118		
VSS_32	115		
VSS_31	112		
VSS_30	109		
VSS_29	106		
VSS_28	103		
VSS_27	100		
VSS_26	97		
VSS_25	94		
VSS_24	91		
VSS_23	88		
VSS_22	85		
VSS_21	82		
VSS_20	79		
VSS_19	66		
VSS_18	65		
VSS_17	50		
VSS_16	47		
VSS_15	44		
VSS_14	41		
VSS_13	38		
VSS_12	35		
VSS_11	32	VDDQ_11	194
VSS_10	29	VDDQ_10	191
VSS_9	26	VDDQ_9	181
VSS_8	23	VDDQ_8	175
VSS_7	20	VDDQ_7	170
VSS_6	17	VDDQ_6	78
VSS_5	14	VDDQ_5	75
VSS_4	11	VDDQ_4	72
VSS_3	8	VDDQ_3	62
VSS_2	5	VDDQ_2	56
VSS_1	2	VDDQ_1	51

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GND

DDR_VREF_0V9 VREF 1

1V8 VDDSPD 238

1V8 VDD_11 197 VDD_10 189 VDD_9 187 VDD_8 184 VDD_7 178 VDD_6 172 VDD_5 69 VDD_4 67 VDD_3 64 VDD_2 59 VDD_1 53

1V8 VDDQ_11 194 VDDQ_10 191 VDDQ_9 181 VDDQ_8 175 VDDQ_7 170 VDDQ_6 78 VDDQ_5 75 VDDQ_4 72 VDDQ_3 62 VDDQ_2 56 VDDQ_1 51

DDR_VREF_0V9 1V8 1V8 1V8

C432 100NF 10V
C433 10NF 25V
C454 100NF 10V
C434 10NF 25V
C430 100NF 10V
C443 10NF 25V
C431 100NF 10V
C444 10NF 25V
C436 100NF 10V
C445 10NF 25V
C435 100NF 10V
C446 10NF 25V

GND

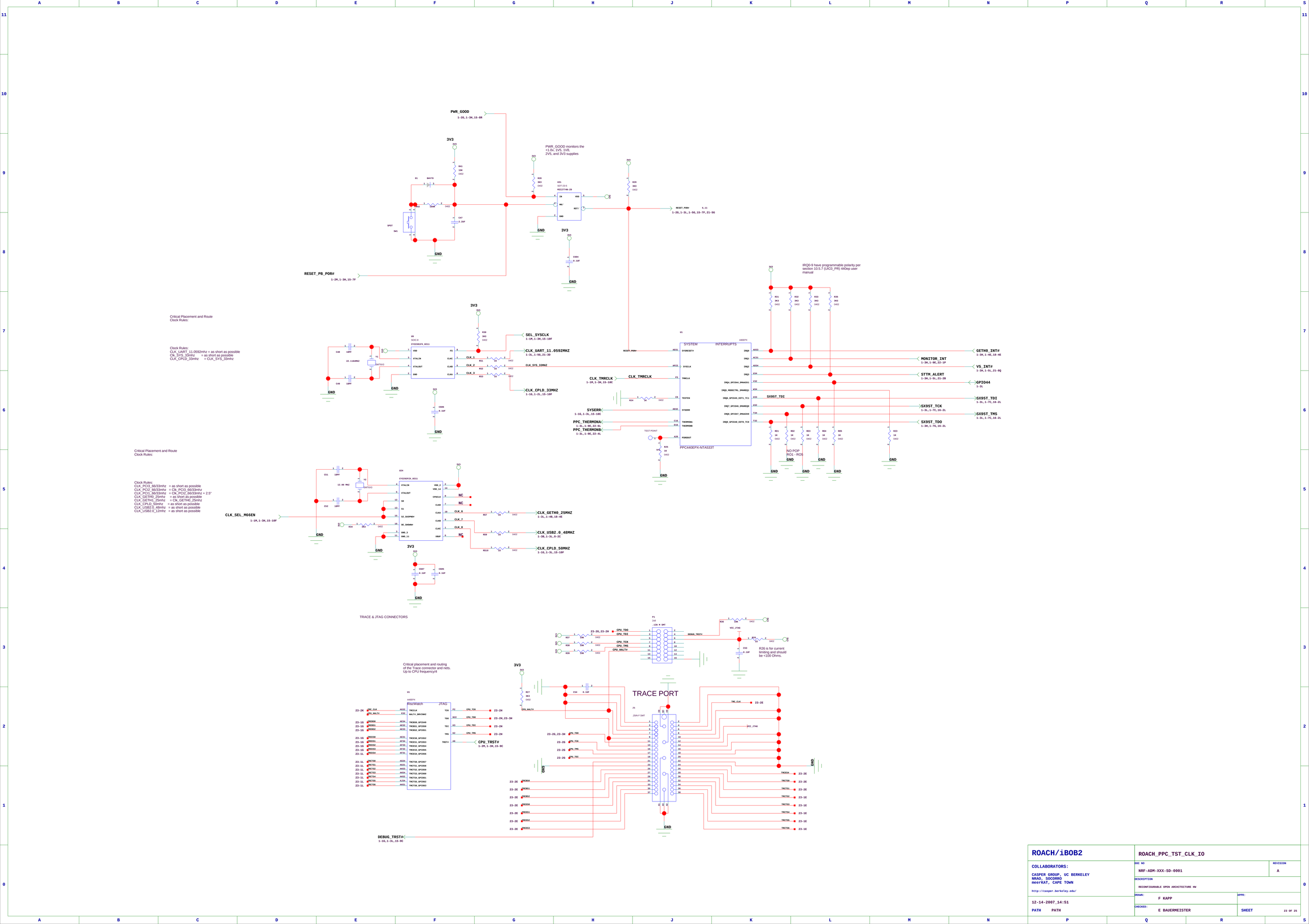
1V8 1V8 1V8

C438 100NF 10V
C451 10NF 25V
C437 100NF 10V
C452 10NF 25V
C439 100NF 10V
C449 10NF 25V
C440 100NF 10V
C450 10NF 25V
C441 100NF 10V
C448 10NF 25V
C442 100NF 10V
C447 10NF 25V

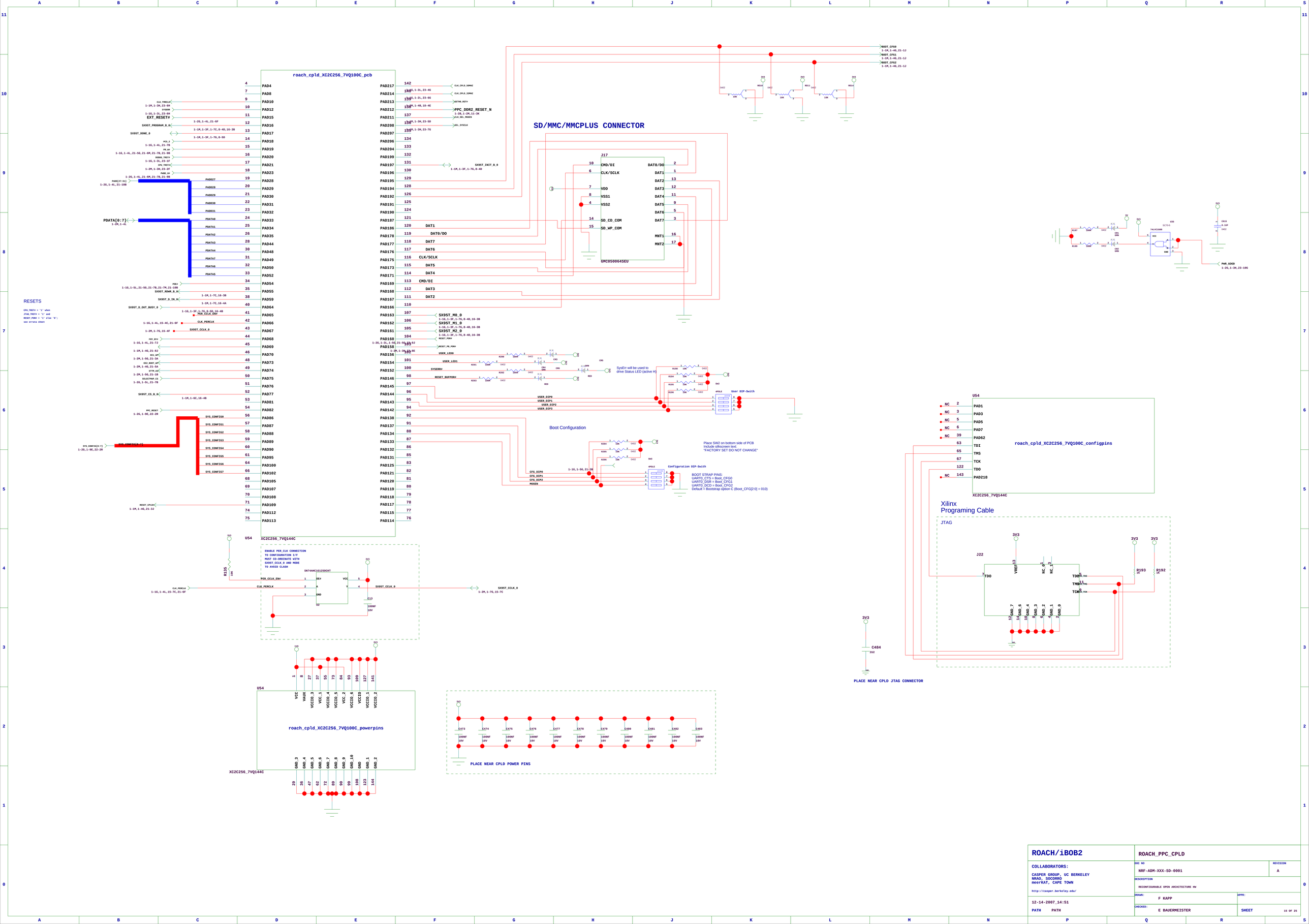
GND

PLACE NEAREST DDR2 MODULE PINS

ROACH/iBOB2	ROACH_PPC_DDR2
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
12-14-2007_14:51	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 11 OF 25



ROACH/iBOB2	**ROACH_PPC_TST_CLK_IO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
12-14-2007_14:51	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 23 OF 25



ROACH/iBOB2	**ROACH_PPC_CPLD**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
12-14-2007_14:51	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 15 OF 25

PDATA[0:31]
1-2M,1-4L

PADD[20:31]
1-2G,1-4L,15-9B,21-10B

PADD[2:31]

PADD30 IS THE LSB FOR 16 BIT WIDE BUS TRANSFERS

**NOTE:
DMA SIGNALS
IN GREEN TEXT**

PADD2 IS THE MSB

3V3

PCS_3_SPI2010 21-7C
PDEV 1-10,1-5L,15-8C,21-5G,21-7B,21-7M
PB_WP 1-10,1-4L,15-9C,21-5G,21-6M,21-7B
PWBE_0# 1-26,1-4L,15-9C,21-6M,21-7B
PWBE_1# 21-6M,21-7C
PWBE_2# 21-7C
PWBE_3# 21-7C
PREADY 21-7C,21-8Q
PBLAST# 21-6M,21-7C
PCS_0
PCS_1
PCS_2

R64 3K3 0402
R65 3K3 0402
R66 3K3 0402
R67 3K3 0402
R68 3K3 0402
R69 3K3 0402
R70 3K3 0402
R71 3K3 0402
R72 3K3 0402

U1
External Slave Peripheral
A43EPX

PERDATA31 NC M5
PERDATA30 NC M4
PERDATA29 NC N1
PERDATA28 NC N2
PERDATA27 NC N3
PERDATA26 NC N5
PERDATA25 NC P1
PERDATA24 NC P2
PERDATA23 NC P3
PERDATA22 NC P4
PERDATA21 NC R1
PERDATA20 NC R2
PERDATA19 NC R4
PERDATA18 NC R5
PERDATA17 NC T1
PERDATA16 NC T2
PERDATA15 C16
PERDATA14 B16
PERDATA13 A16
PERDATA12 B15
PERDATA11 C14
PERDATA10 B14
PERDATA9 A15
PERDATA8 A14
PERDATA7 C13
PERDATA6 A13
PERDATA5 B13
PERDATA4 A12
PERDATA3 B12
PERDATA2 A11
PERDATA1 B11
PERDATA0 C11

PCS_0 B10
PCS_1 B9
PCS_2 B8
PERCS5# B7
PERCS4#_GPIO09 C7
PERCS3#_GPIO10 C6
PERRD#
PERWR_WP
PERWBE_0#
PERWBE_1#
PERWBE_2#
PERWBE_3#
PEREADY
PERBLAST#

PERADDR31 R10 PA0031
PERADDR30 A10 PA0030
PERADDR29 B10 PA0029
PERADDR28 A9 PA0028
PERADDR27 B9 PA0027
PERADDR26 C9 PA0026
PERADDR25 B6 PA0025
PERADDR24 C8 PA0024
PERADDR23 A8 PA0023
PERADDR22 B8 PA0022
PERADDR21 A7 PA0021
PERADDR20 B7 PA0020
PERADDR19 A6 PA0019
PERADDR18 A5 PA0018
PERADDR17 C5 PA0017
PERADDR16 B5 PA0016
PERADDR15 A3 PA0015
PERADDR14 A4 PA0014
PERADDR13 B3 PA0013
PERADDR12 B4 PA0012
PERADDR11 C4 PA0011
PERADDR10 D4 PA0010
PERADDR09 A2 PA009
PERADDR08 B2 PA008

PERADDR07_GPIO06_DMAREQ2 C25 PA006 DMAREQ2
PERADDR06_GPIO01_DMAACK2 D25 PA005 DMAACK2
PERADDR05_GPIO02_EOT2_TC2 A26 PA004 EOT2/TC2
GPIO03_PERADDR04_DMAREQ3 B26 PA003 DMAREQ3
GPIO04_PERADDR03_DMAACK3 C26 PA002 DMAACK3
GPIO05_PERADDR02_EOT3_TC3 D26 PA002 EOT3/TC3

EXTRESET# R6
PERCLK A7
PERERR_GPIO11 C7
R6 22R
CLK_PERCLK
R85 1K 0402
EXT_RESET#
EPB RESET OUTPUT
1-26,1-4L,15-10C
CLK_PERCLK
1-1G,1-4L,15-4C,15-7C

External Master Peripheral Interface

R134 3K3
R133 3K3
R132 3K3
R84 3K3
R83 3K3
R5 3K3

U42
FBGA64
32Mx16 HIGHER BIT
FLASH 32Mx16 64Mx8

PADD30 D2
PADD29 D4
PADD28 C2
PADD27 A2
PADD26 B2
PADD25 B1
PADD24 C3
PADD23 A1
PADD22 B5
PADD21 A3
PADD20 B6
PADD19 D6
PADD18 D5
PADD17 A7
PADD16 C6
PADD15 B7
PADD14 A6
PADD13 B3
PADD12 C5
PADD11 D3
PADD10 D6
PADD9 C7
PADD8 B7
PADD7 DMAREQ2 H2
PADD6 DMAACK2 L4
PADD5 EOT2/TC2 K4
PADD4 DMAREQ3 K3
PADD3 DMAACK3 K2
PADD2 EOT3/TC3 J12

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21_A0MB A22_16MB A23_32MB A24_512MB A25_1GB A26_2GB BYTE#
CE# OE# WE# RESET#
WP#/ACC
DQ0 E3 PDATA15
DQ1 H3 PDATA14
DQ2 E4 PDATA13
DQ3 H4 PDATA12
DQ4 H5 PDATA11
DQ5 E5 PDATA10
DQ6 H6 PDATA9
DQ7 E6 PDATA8
DQ8 F3 PDATA7
DQ9 G3 PDATA6
DQ10 F4 PDATA5
DQ11 G4 PDATA4
DQ12 F5 PDATA3
DQ13 G5 PDATA2
DQ14 F6 PDATA1
DQ15/A-1 G7 PDATA0
BY/RY# A4
NC1 A5
NC2 A8
NC3 C3
NC5 D1
NC6 E1
NC8 G1
NC10 H1
NC11 H8
VCC1 A3 VCC2 E2 VCC3 J1
VSS1 A7 VSS2 E7 VSS3 J8

WP#
1-1M,1-4G,15-7C
R4 3K3 0402
R81 3K3 0402
RY_BY#
1-1G,1-4L,15-7C
R5 3K3 0402
C64 0.1UF 0402
C65 0.1UF 0402
C59 0.1UF 0402

PCS_0
1-1G,1-4L,15-9C
PCS_1
SELECTMAP_CS
1-2G,1-5L,15-6C
PCS_2
1-1G,1-4L,15-9C
SELECTMAP_CS 21-10B
PCS_3_SPI2010 21-10B
PDEV
1-1G,1-5L,15-8C,21-5G,21-7B,21-7M,21-10B
PB_WP
1-1G,1-4L,15-9C,21-5G,21-6M,21-9B
PWBE_0#
1-2G,1-4L,15-9C,21-6M,21-9B
PWBE_1# 21-6M,21-9B
PWBE_2# 21-9B
PWBE_3# 21-9B
PREADY 21-6M,21-9B
PBLAST# 21-6M,21-9B

3V3 AL12 3V3_4_1
3V3 AG14 3V3_4_2
3V3 AM19 3V3_3_2
3V3 AM21 3V3_2_1
3V3 G14 3V3_1_1
3V3 D13 3V3_1

PADD30 AE12 PER_A[30]
PADD29 AF23 PER_A[29]
PADD28 AG23 PER_A[28]
PADD27 AF13 PER_A[27]
PADD26 AG12 PER_A[26]
PADD25 AE22 PER_A[25]
PADD24 AE23 PER_A[24]
PADD23 AG20 PER_A[23]
PADD22 AH15 PER_A[22]
PADD21 AG15 PER_A[21]
PADD20 AG18 PER_A[20]
PADD19 AF19 PER_A[19]
PADD18 AH17 PER_A[18]
PADD17 AG16 PER_A[17]
PADD16 L21 PER_SP_A[16]
PADD15 L20 PER_SP_A[15]
PADD14 L15 PER_SP_A[14]
PADD13 L16 PER_SP_A[13]
PADD12 J22 PER_SP_A[12]
PADD11 K21 PER_SP_A[11]
PADD10 K16 PER_SP_A[10]
PADD9 J15 PER_SP_A[9]
PADD8 G22 PER_SP_A[8]
PADD7 DMAREQ2 H22 PER_SP_A[7]
PADD6 DMAACK2 L14 PER_SP_A[6]
PADD5 EOT2/TC2 K14 PER_SP_A[5]
PADD4 DMAREQ3 K23 PER_SP_A[4]
PADD3 DMAACK3 K22 PER_SP_A[3]
PADD2 EOT3/TC3 J12 PER_SP_A[2]

PCS_1 AE14 PER_CS0
POE# AF21 PER_OE_N
PR_W# AF20 PER_R_W_N
PWBE_1# AF18 PER_WBE[1]
PWBE_0# AF14 PER_WBE[0]
PBLAST# AE18 PER_B_LAST

U15
BANKS=1, 2, 4
CHIP SELECT 1

PER_D[15] AF15 PDATA15
PER_D[14] AE16 PDATA14
PER_D[13] AE21 PDATA13
PER_D[12] AD20 PDATA12
PER_D[11] AF16 PDATA11
PER_D[10] AE17 PDATA10
PER_D[9] AE19 PDATA9
PER_D[8] AD19 PDATA8
PER_D[7] AG22 PDATA7
PER_D[6] AH22 PDATA6
PER_D[5] AH12 PDATA5
PER_D[4] AG13 PDATA4
PER_D[3] AH20 PDATA3
PER_D[2] AH19 PDATA2
PER_D[1] AH14 PDATA1
PER_D[0] AH13 PDATA0

PER_D_PAR[1] AG21 NC
PER_D_PAR[0] AE13 NC
PER_D_PAR[1]
PER_D_PAR[0]

PER_INT H12 VS_INT#
VS_INT#
1-3H,1-5L,23-7N

PER_READY AH18 PREADY
PREADY 21-7C,21-9B

PER_CLK AG17 CLK_PERCLK

C334 470F 6V
C335 470F 6V
C330 220NF 6.3V
C331 220NF 6.3V
C332 220NF 6.3V
C333 220NF 6.3V
GND

I2C0_SCLK
1-5L,1-9B,22-2F
I2C0_33_DATA
1-5L,1-9E

EE2_BOOT_WP
1-2M,1-4G,15-7C
ATMEL 24C04N
ATZ24C04N-10SU-1.8
R88 15K 0402
I2C0_33_SCLK
I2C0_33_DATA

I2C0_SCLK
I2C0_66_DATA
R89 15K 0402
I2C0_66_SCLK
I2C0_66_DATA
R89 0R
NO POP
BUFFs_ZA-6
PI5A3157
S=B BO TO A

M66EN
1-1G,1-5G,15-5H

EE1_WP
1-2M,1-5G,15-7C
I2C0_SCLK
I2C0_SDATA

R73 3K3 0402
R74 3K3 0402
R75 3K3 0402
R76 3K3 0402
R77 3K3 0402
R78 3K3 0402
R79 3K3 0402
R80 3K3 0402

R85 VT 0.12k H SMT
R86 VT 0.12k H SMT

STTM_ALERT
1-3H,1-5L,23-6M
STTM_AS
1-2M,1-5G,15-7C
SOT23-6
AD7414-0
I2C0_SCLK
I2C0_SDATA

SCPCLK
SCPDI
SCPDO

U1
UART
UARTSERCLK
CLK_UART_11.0592MHZ
1-3L,1-5G,23-7G

UART1_TX_UART0_TX D27 UART1_TX
UART1_RX_UART0_RX C27 UART1_RX
UART1_RTS#_UART0_RTS# B29
UART1_CTS#_UART0_CTS# A29
UART2_TX_UART0_DTR# D28 UART2_TX
UART2_RX_UART0_RI# B28 UART2_RX
UART2_RTS#_UART0_DSR# C29 CPU_UART0_DSR#
UART2_CTS#_UART0_DCD# C28 CPU_UART0_DCD#

IIC0
IIC0SCLK AB32
IIC0SDATA AB33
IIC1_SPI
SCPCLKOUT_IIC1SCLK AC34
SCPDI_IIC1SDATA AC32
SCPDO AB31
NAND Flash Interface
NOT USED
NFALE R17 NC
NFCLE A18 NC
NFREN# D17 NC
NFWEN# A16 NC
NFRDYBUSY# A17
NFCE3#_PERCS3# D8

SCPCLK 1-5L
SCPDI 1-5L
SCPDO 1-5L

SCPCLK AC34
SCPDI AC32
SCPDO AB31
SCPEE
SCPDS

R87 VT 0.12k H SMT

U44
SSOP20
ICL3225ECA
C2P C2N C1P C1N VCC V+ V- T1IN T2IN R1OUT R2OUT FORCEOFF FORCEON INVALID READY GND
C192 0.1UF 0402
C194 0.1UF 0402
C193 0.1UF 0402
C195 0.1UF 0402
X_UART1_TX
X_UART1_RX
X_UART1_RTS#
X_UART1_CTS#
R84 10K 0402
C652 0.1UF 0402

U43
SSOP20
ICL3225ECA
C2P C2N C1P C1N VCC V+ V- T1IN T2IN R1OUT R2OUT FORCEOFF FORCEON INVALID READY GND
C196 0.1UF 0402
C198 0.1UF 0402
C197 0.1UF 0402
C199 0.1UF 0402
X_UART2_TX
X_UART2_RX
X_UART2_RTS#
X_UART2_CTS#
R87 10K 0402
C653 0.1UF 0402
C649 0.1UF 0402

P2
DSUB9_FEMALE
RF BOOB MALE
UART1_CTS#
UART1_TX
UART1_RTS#
UART1_RX
UART Port 0

J14
UART Port 1
NC P1
X_UART2_RX P2
X_UART2_TX P3
P4
P5
NC P6
X_UART2_RTS# P7
P8
NC P9
NC P10
HLE-105-02-G-DV

U40 TDFN_ZA-6 PI5A3157
S=B BO TO A
UART1_CTS#
R82 3K3 0402
RESET_CPLD#
1-1M,1-4G,15-5C

U45 TDFN_ZA-6 PI5A3157
S=B BO TO A
UART2_RTS#

U46 TDFN_ZA-6 PI5A3157
S=B BO TO A
UART2_CTS#

BOOT_CFG2
1-1M,1-4G,15-10M
BOOT_CFG1
1-1M,1-4G,15-11M
BOOT_CFG0
1-1M,1-4G,15-11M

C652 0.1UF 0402
C650 0.1UF 0402
C658 0.1UF 0402
C660 0.1UF 0402

UART1_TX
UART1_RX
PERPARB_UART1_RTS#
PERPARB_UART1_CTS#
UART2_TX
UART2_RX

1-1G,1-5L,15-8C,21-7B,21-7M,21-10B PDEV
1-1G,1-4L,15-9C,21-6M,21-7B,21-9B PB_WP
RESET_PORB
1-2G,1-3L,1-5G,15-7F,23-9J