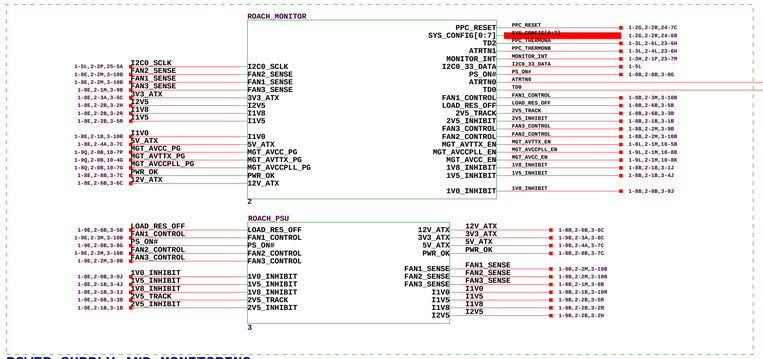
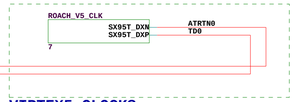
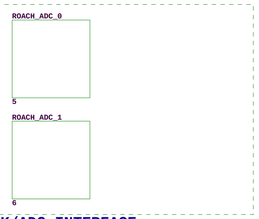
VIRTEX5

POWER SUPPLY AND MONITORING



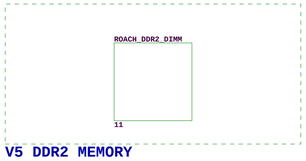
VIRTEX5 CLOCKS



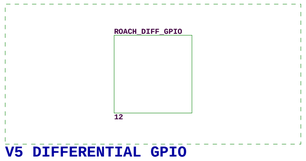


ZDOK/ADC INTERFACE

V5 DDR2 MEMORY

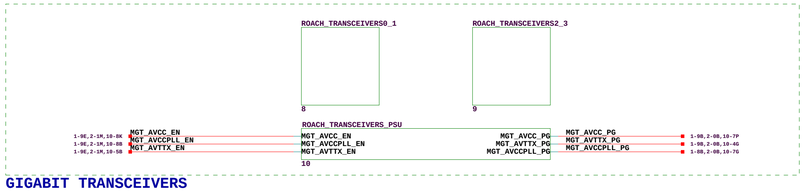


V5 DIFFERENTIAL GPIO

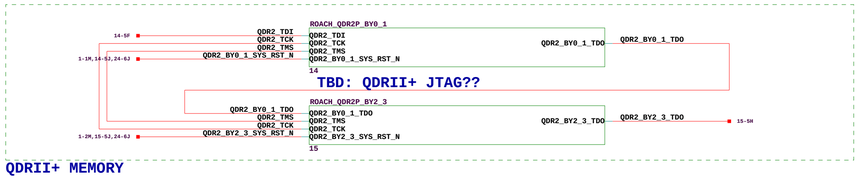


V5 SE GPIO & MISCELLANEOUS

GIGABIT TRANSCEIVERS



QDRII+ MEMORY

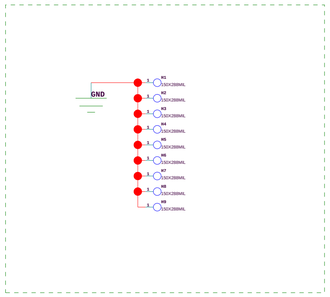


V5 POWER

VIRTEX5 CONFIGURATION

PPC

MECHANICAL



CONTRIBUTORS

ETIENNE BAUERMEISTER
HENRY CHEN
STEVE DURAND
FRANCOIS KAPP
ALAN LANDMAN
GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2	**ROACH_TOP**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-15-2007_15:53 PATH PATH	DRAWN: F KAPP APPR:
	CHECKED: E BAUERMEISTER SHEET 1 OF 25

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

TIE TO GROUND IF PLL'S ARE NOT USED

PLACE AT ACTEL 3V3 POWER PINS

PLACE AT ACTEL 1V5 POWER PINS

roach_AFS600_powerpins

roach_AFS600_configpins

roach_AFS600_pcb

PB POWER SWITCH

KEY - REMOVE PIN

MONITOR RESET

XPORT - PLACE IN REAR I/O REGION

TEMPERATURE DIODE HEADER

ACTEL JTAG CONNECTOR

REFERENCE RESISTOR/ADC VALUES

FOR 8 BIT ADC USING 2.56V REFERENCE:

VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)	ADC COUNT AT MAX POWER	CURRENT/BIT (A)
12V	0R01	3.36	0.11	33	0.1
5V	0R0047	6.78	0.22	31	0.21
3V3	0R01	3.47	0.12	34	0.1
2V5	0R01	3.56	0.13	35	0.1
1V8	0R0022	12.91	0.37	28	0.45
1V5	0R0047	6.77	0.22	31	0.21
1V0	0R001	26.79	0.72	26	1.0

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

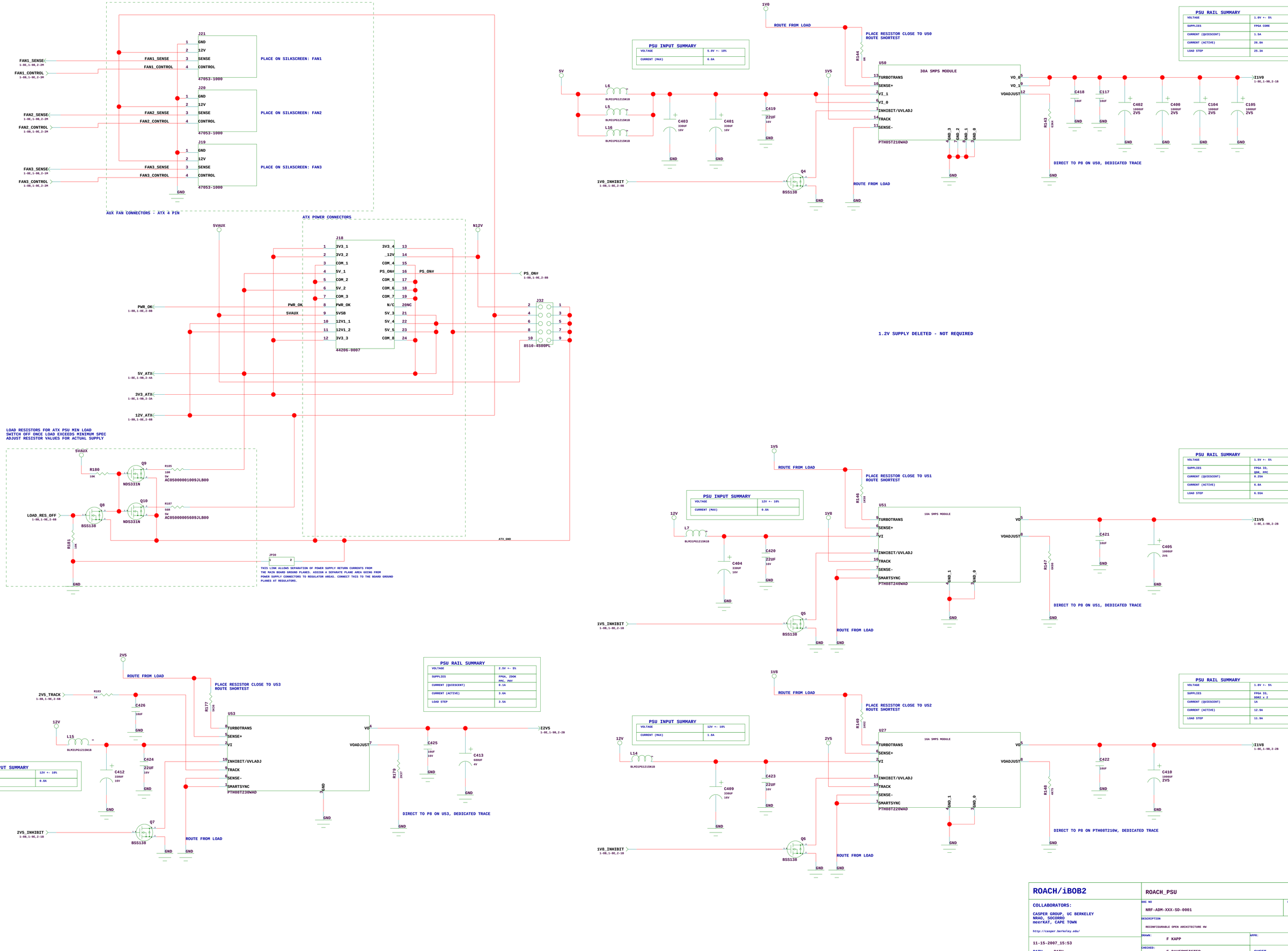
http://casper.berkeley.edu/

11-15-2007_15:53

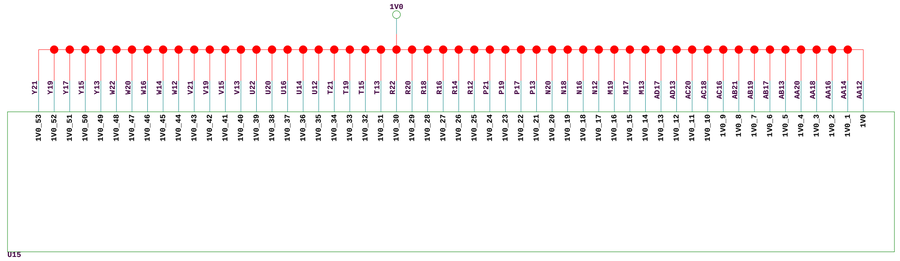
PATH PATH

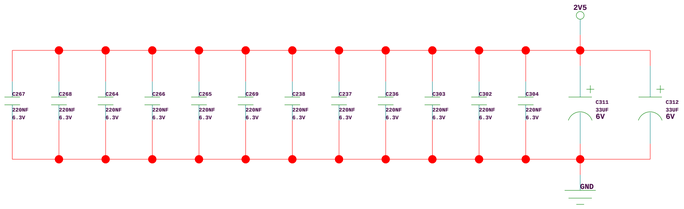
ROACH_MONITOR

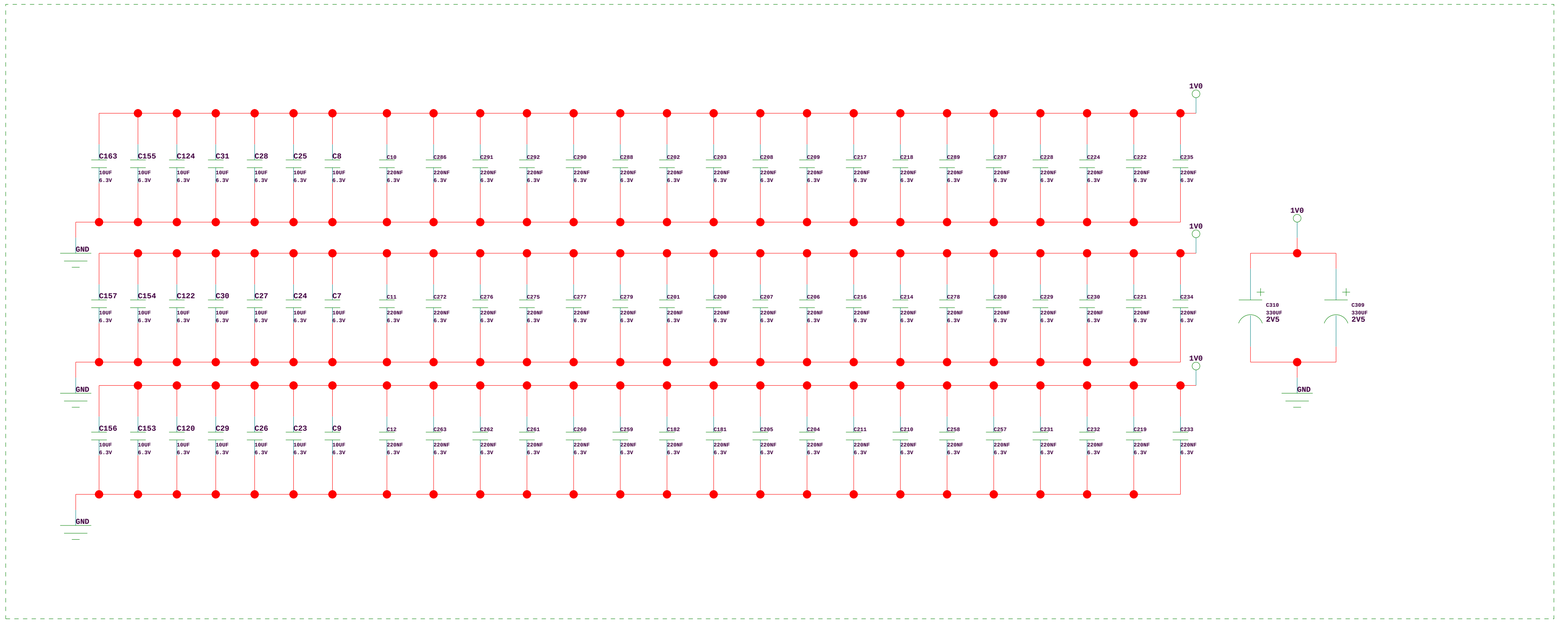
DOC NO	NRF-ADM-XXX-SD-0001
REVISION	A
DESCRIPTION	RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:	F KAPP
APPR:	
CHECKED:	E BAUERMEISTER
SHEET	2 OF 25

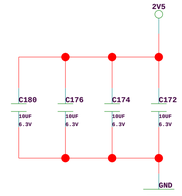


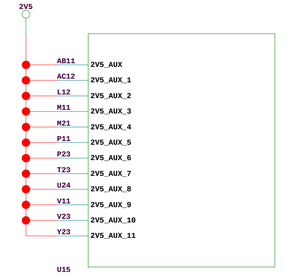
ROACH/iBOB2	**ROACH_PSU**
COLLABORATORS:	DOC NO: NRF-ADM-XXX-SD-0001
CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerkat, CAPE TOWN	REVISION: A
http://casper.berkeley.edu/	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-15-2007_15:53	DRAWN: F KAPP APPR:
PATH PATH	CHECKED: E BAUERMEISTER SHEET 3 OF 25

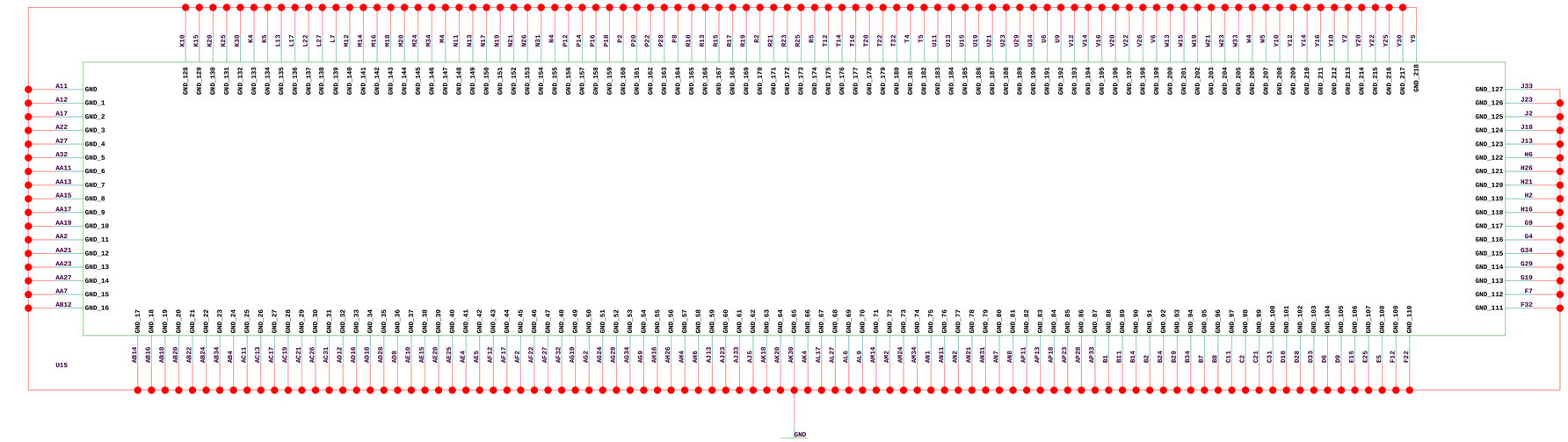












ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
11-15-2007_15:53 PATH PATH	


ZDOK0_CLK0_P K18
ZDOK0_CLK0_N J19
ZDOK0_CLK1_P J16
ZDOK0_CLK1_N J17
VRP_20 L11
VRN_20 L10
VRP_12_GPIOLVC25 P9
VRN_12_GPIOLVC25 R9
2V5
2V5_12 M9
2V5_12_1 N6
2V5_12_2 T7
2V5_20 E10
2V5_20_1 H11
2V5_20_2 J8
C328 47UF 6V
C327 47UF 6V
C326 47UF 6V
C329 47UF 6V
C325 220NF 6.3V
C322 220NF 6.3V
C323 220NF 6.3V
C324 220NF 6.3V
U15
BANKS=20, 12
5V
3V3
2V5
1V8
C315 1UF 16V
C314 100NF 10V
C317 1UF 16V
C316 100NF 10V
C318 1UF 16V
C319 100NF 10V
C321 1UF 16V
C320 100NF 10V
P5
6367550-5
ZDOK40
ZDOK0_CLK0_P 5-7B
ZDOK0_CLK1_P 5-7B
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
11-15-2007_15:53
PATH PATH
ROACH_ADC_0
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 5 OF 25

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

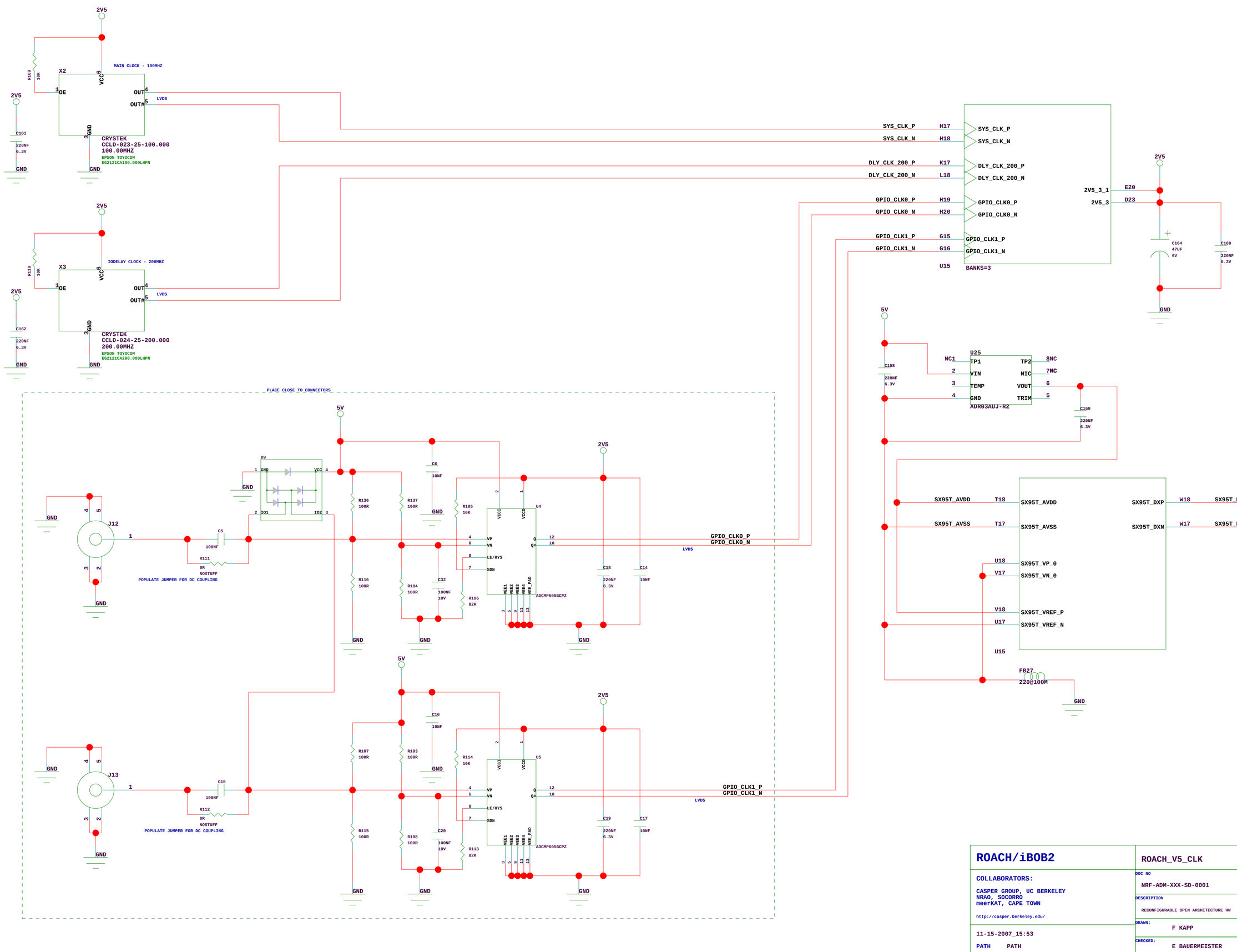
http://casper.berkeley.edu/

11-15-2007_15:53

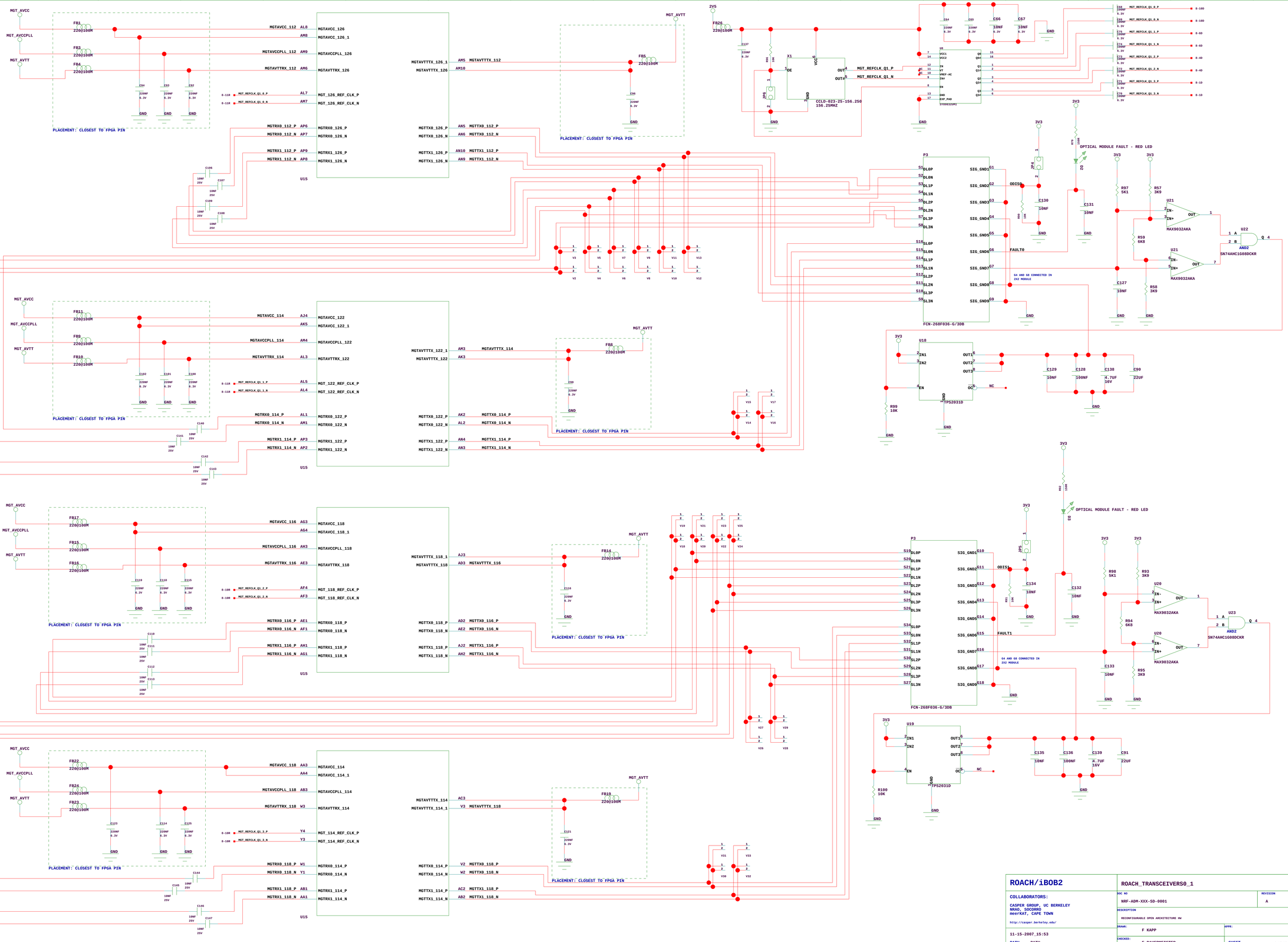
PATH PATH

ROACH_ADC_1

DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET: 6 OF 25



ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
11-15-2007_15:53 PATH PATH	


MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB3 220@100M
FB4 220@100M
MGTAVCC_112 AL8 MGTAVCC_126
AM8 MGTAVCC_126_1
MGTAVCCPLL_112 AM9 MGTAVCCPLL_126
MGTAVTTRX_112 AM6 MGTAVTTRX_126
C84 220NF 6.3V
C93 220NF 6.3V
C92 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
B-11R MGT_REFCLK_Q1_0_P AL7 MGT_126_REF_CLK_P
B-11R MGT_REFCLK_Q1_0_N AM7 MGT_126_REF_CLK_N
MGTRX0_112_P AP6 MGTRX0_126_P
MGTRX0_112_N AP7 MGTRX0_126_N
MGTRX1_112_P AP9 MGTRX1_126_P
MGTRX1_112_N AP8 MGTRX1_126_N
U15
MGTAVTTTX_126_1 AM5 MGTAVTTTX_112
MGTAVTTTX_126 AM10
MGTTX0_126_P AN5 MGTTX0_112_P
MGTTX0_126_N AN6 MGTTX0_112_N
MGTTX1_126_P AN10 MGTTX1_112_P
MGTTX1_126_N AN9 MGTTX1_112_N
MGT_AVTT
FB5 220@100M
C96 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
C106 10NF 25V
C107 10NF 25V
C109 10NF 25V
C108 10NF 25V
V3 V5 V7 V9 V11 V13
V2 V4 V6 V8 V10 V12
2V5
FB26 220@100M
C137 220NF 6.3V
R88 10K
X1
OE
VCC
OUT
GND
JP6
CCLD-023-25-156.250 156.25MHZ
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
C64 220NF 6.3V
C65 220NF 6.3V
C66 10NF 6.3V
C67 10NF 6.3V
GND
U8 VCC1 VCC2 IN VT VREF-AC ZBW EN GND EXP_PAD SY89832UMI
Q0 Q0# Q1 Q1# Q2 Q2# Q3 Q3#
C68 100NF 6.3V MGT_REFCLK_Q1_0_P B-10D
C69 100NF 6.3V MGT_REFCLK_Q1_0_N B-10D
C75 100NF 6.3V MGT_REFCLK_Q1_1_P B-6D
C74 100NF 6.3V MGT_REFCLK_Q1_1_N B-6D
C73 100NF 6.3V MGT_REFCLK_Q1_2_P B-4D
C72 100NF 6.3V MGT_REFCLK_Q1_2_N B-4D
C71 100NF 6.3V MGT_REFCLK_Q1_3_P B-1D
C70 100NF 6.3V MGT_REFCLK_Q1_3_N B-1D
P3
DL0P DL0N DL1P DL1N DL2P DL2N DL3P DL3N
SL0P SL0N SL1P SL1N SL2P SL2N SL3P SL3N
SIG_GND1 SIG_GND2 SIG_GND3 SIG_GND4 SIG_GND5 SIG_GND6 SIG_GND7 SIG_GND8 SIG_GND9
FCN-268F036-G/3DB
3V3
JP4
R89 10K
ODIS0
C130 10NF
GND
FAULT0
G4 AND G8 CONNECTED IN 2X2 MODULE
R89 10K
OPTICAL MODULE FAULT - RED LED
C131 10NF
R97 5K1
RS7 3K9
RS9 6K8
RS8 3K9
U21 MAX9032AKA
U22 AND2 SN74AHC1G08DCKR
C127 10NF
U18 IN1 IN2 EN OUT1 OUT2 OUT3 OC NC TPS2031D
R99 10K
C129 10NF
C128 100NF
C138 4.7UF 16V
C90 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB11 220@100M
FB9 220@100M
FB10 220@100M
MGTAVCC_114 AJ4 MGTAVCC_122
AK5 MGTAVCC_122_1
MGTAVCCPLL_114 AM4 MGTAVCCPLL_122
MGTAVTTRX_114 AL3 MGTAVTTRX_122
C102 220NF 6.3V
C101 220NF 6.3V
C100 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
B-11R MGT_REFCLK_Q3_1_P AL5 MGT_122_REF_CLK_P
B-11R MGT_REFCLK_Q3_1_N AL4 MGT_122_REF_CLK_N
MGTRX0_114_P AL1 MGTRX0_122_P
MGTRX0_114_N AM1 MGTRX0_122_N
MGTRX1_114_P AP3 MGTRX1_122_P
MGTRX1_114_N AP2 MGTRX1_122_N
U15
C140 10NF 25V
C141 10NF 25V
C142 10NF 25V
C143 10NF 25V
MGTAVTTTX_122_1 AM3 MGTAVTTTX_114
MGTAVTTTX_122 AK3
MGTTX0_122_P AK2 MGTTX0_114_P
MGTTX0_122_N AL2 MGTTX0_114_N
MGTTX1_122_P AN4 MGTTX1_114_P
MGTTX1_122_N AN3 MGTTX1_114_N
MGT_AVTT
FB8 220@100M
C99 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
V15 V17
V14 V16
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB17 220@100M
FB15 220@100M
FB16 220@100M
MGTAVCC_116 AG3 MGTAVCC_118
AG4 MGTAVCC_118_1
MGTAVCCPLL_116 AH3 MGTAVCCPLL_118
MGTAVTTRX_116 AE3 MGTAVTTRX_118
C119 220NF 6.3V
C118 220NF 6.3V
C115 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
B-10R MGT_REFCLK_Q3_2_P AF4 MGT_118_REF_CLK_P
B-10R MGT_REFCLK_Q3_2_N AF3 MGT_118_REF_CLK_N
MGTRX0_116_P AE1 MGTRX0_118_P
MGTRX0_116_N AF1 MGTRX0_118_N
MGTRX1_116_P AH1 MGTRX1_118_P
MGTRX1_116_N AG1 MGTRX1_118_N
U15
C110 10NF 25V
C111 10NF 25V
C112 10NF 25V
C113 10NF 25V
MGTAVTTTX_118_1 AJ3
MGTAVTTTX_118 AD3 MGTAVTTTX_116
MGTTX0_118_P AD2 MGTTX0_116_P
MGTTX0_118_N AE2 MGTTX0_116_N
MGTTX1_118_P AJ2 MGTTX1_116_P
MGTTX1_118_N AH2 MGTTX1_116_N
MGT_AVTT
FB14 220@100M
C116 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
V19 V21 V23 V25
V18 V20 V22 V24
V27 V29
V26 V28
P3
DL0P DL0N DL1P DL1N DL2P DL2N DL3P DL3N
SL0P SL0N SL1P SL1N SL2P SL2N SL3P SL3N
SIG_GND1 SIG_GND2 SIG_GND3 SIG_GND4 SIG_GND5 SIG_GND6 SIG_GND7 SIG_GND8 SIG_GND9
FCN-268F036-G/3DB
3V3
JP5
R90 10K
ODIS1
C134 10NF
GND
FAULT1
G4 AND G8 CONNECTED IN 2X2 MODULE
R90 10K
OPTICAL MODULE FAULT - RED LED
C132 10NF
R98 5K1
R93 3K9
R94 6K8
R95 3K9
U20 MAX9032AKA
U23 AND2 SN74AHC1G08DCKR
C133 10NF
U19 IN1 IN2 EN OUT1 OUT2 OUT3 OC NC TPS2031D
R100 10K
C135 10NF
C136 100NF
C139 4.7UF 16V
C91 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB22 220@100M
FB24 220@100M
FB23 220@100M
MGTAVCC_118 AA3 MGTAVCC_114
AA4 MGTAVCC_114_1
MGTAVCCPLL_118 AB3 MGTAVCCPLL_114
MGTAVTTRX_118 W3 MGTAVTTRX_114
C123 220NF 6.3V
C114 220NF 6.3V
C125 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
B-10R MGT_REFCLK_Q3_3_P Y4 MGT_114_REF_CLK_P
B-10R MGT_REFCLK_Q3_3_N Y3 MGT_114_REF_CLK_N
MGTRX0_118_P W1 MGTRX0_114_P
MGTRX0_118_N Y1 MGTRX0_114_N
MGTRX1_118_P AB1 MGTRX1_114_P
MGTRX1_118_N AA1 MGTRX1_114_N
U15
C144 10NF 25V
C145 10NF 25V
C146 10NF 25V
C147 10NF 25V
MGTAVTTTX_114 AC3
MGTAVTTTX_114_1 V3 MGTAVTTTX_118
MGTTX0_114_P V2 MGTTX0_118_P
MGTTX0_114_N W2 MGTTX0_118_N
MGTTX1_114_P AC2 MGTTX1_118_P
MGTTX1_114_N AB2 MGTTX1_118_N
MGT_AVTT
FB19 220@100M
C121 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
V31 V33
V30 V32
P3
DL0P DL0N DL1P DL1N DL2P DL2N DL3P DL3N
SL0P SL0N SL1P SL1N SL2P SL2N SL3P SL3N
SIG_GND1 SIG_GND2 SIG_GND3 SIG_GND4 SIG_GND5 SIG_GND6 SIG_GND7 SIG_GND8 SIG_GND9
FCN-268F036-G/3DB
3V3
JP5
R91 10K
ODIS1
C134 10NF
GND
FAULT1
G4 AND G8 CONNECTED IN 2X2 MODULE
R91 10K
OPTICAL MODULE FAULT - RED LED
C132 10NF
R98 5K1
R93 3K9
R94 6K8
R95 3K9
U20 MAX9032AKA
U23 AND2 SN74AHC1G08DCKR
C133 10NF
U19 IN1 IN2 EN OUT1 OUT2 OUT3 OC NC TPS2031D
R100 10K
C135 10NF
C136 100NF
C139 4.7UF 16V
C91 22UF
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
11-15-2007_15:53
PATH PATH
ROACH_TRANSCEIVERS0_1
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE MK
DRAWN: F KAPP
CHECKED: E BAUERMEISTER
APPR:
SHEET 8 OF 25

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

G4 AND G8 CONNECTED IN
2X2 MODULE

OPTICAL MODULE FAULT - RED LED

CCLD-023-25-156.250
156.25MHZ

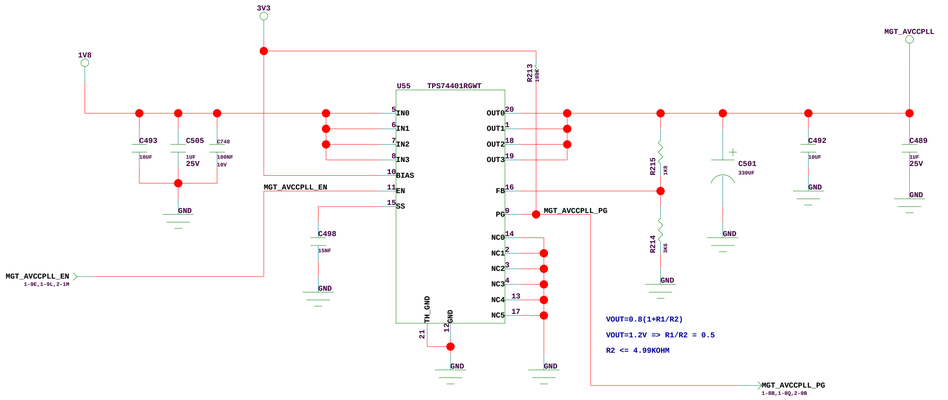
FCN-268F036-G/3DB

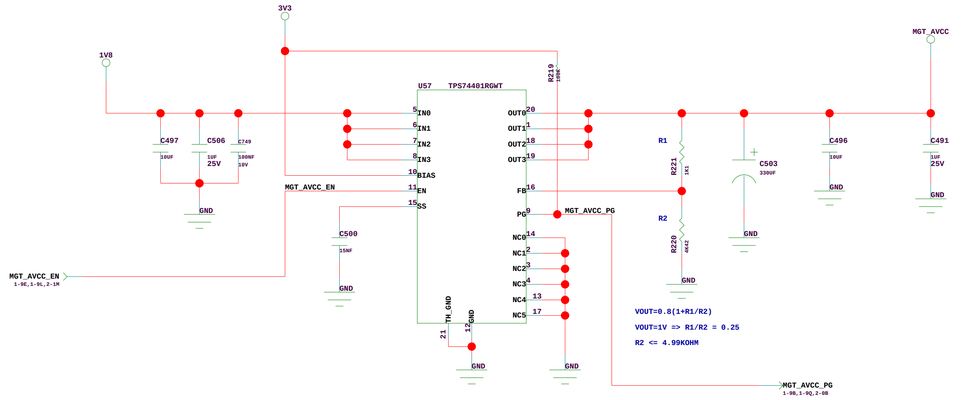
TPS2031D

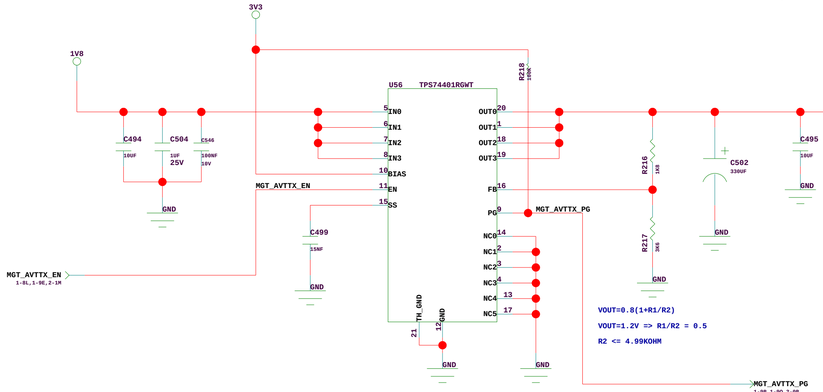
MAX9032AKA

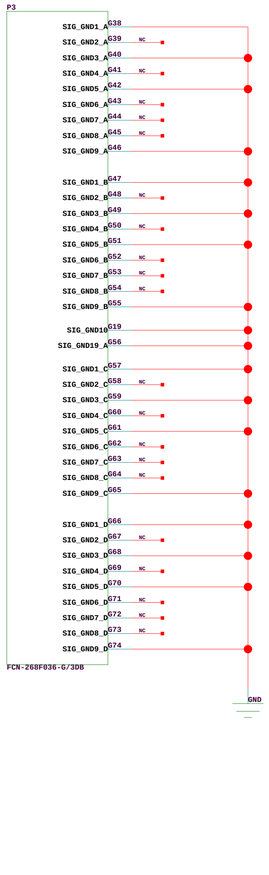
SN74AHC1G08DCKR

ROACH/iBOB2	ROACH_TRANSCEIVERS2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
11-15-2007_15:53	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 9 OF 25

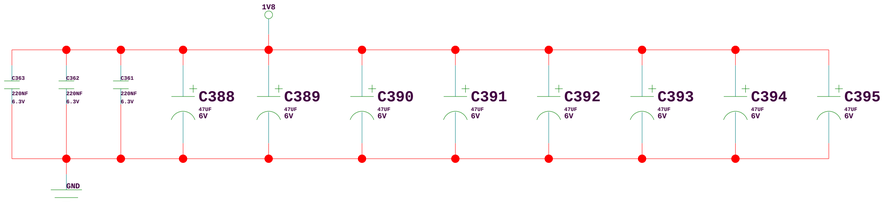


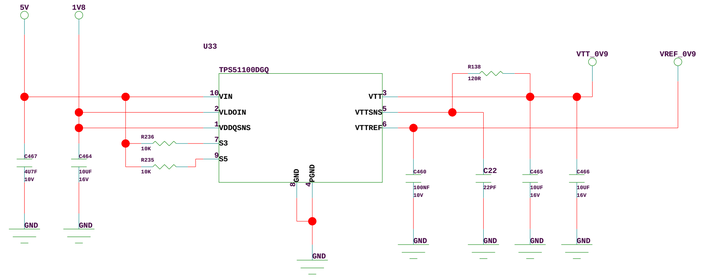


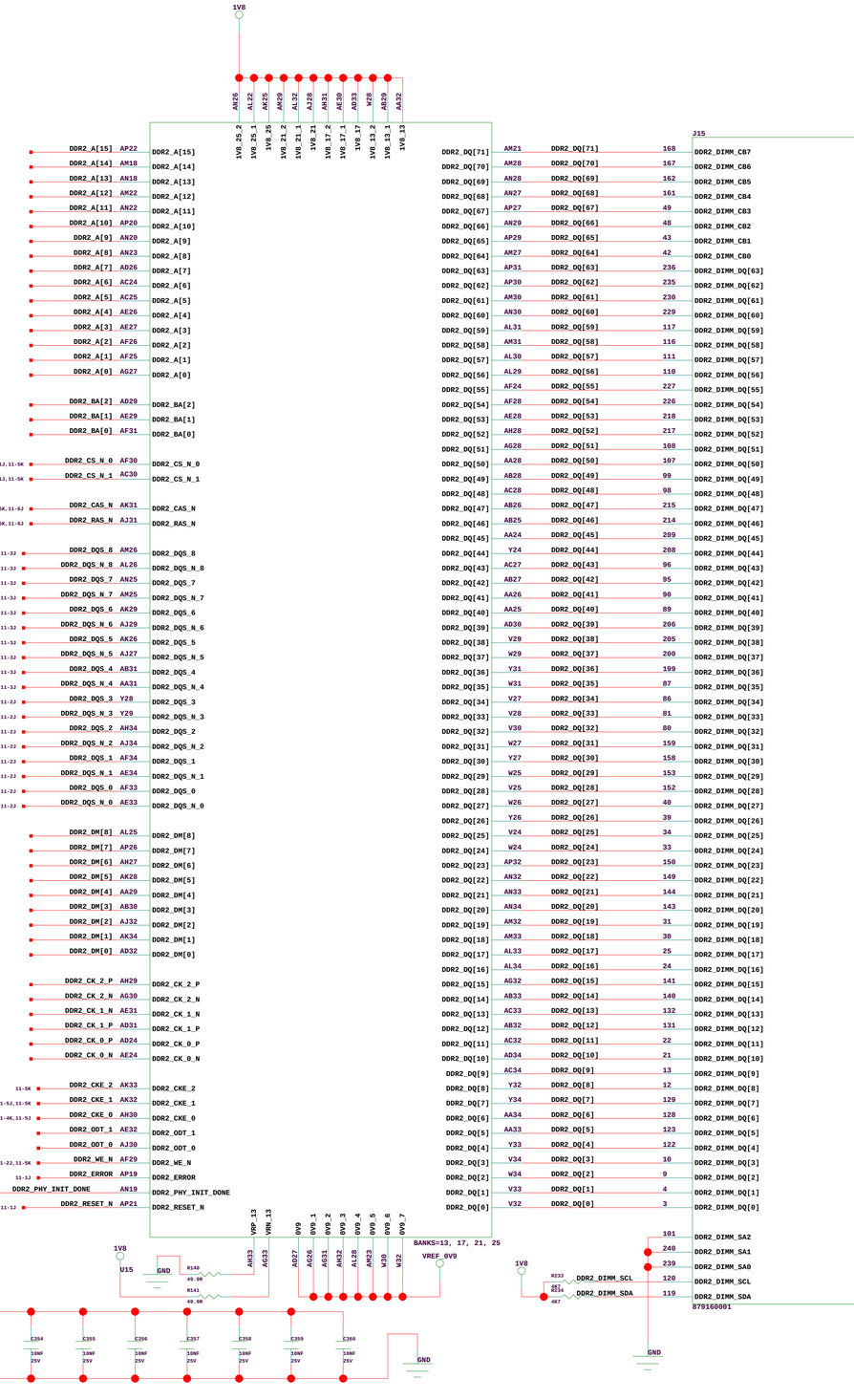




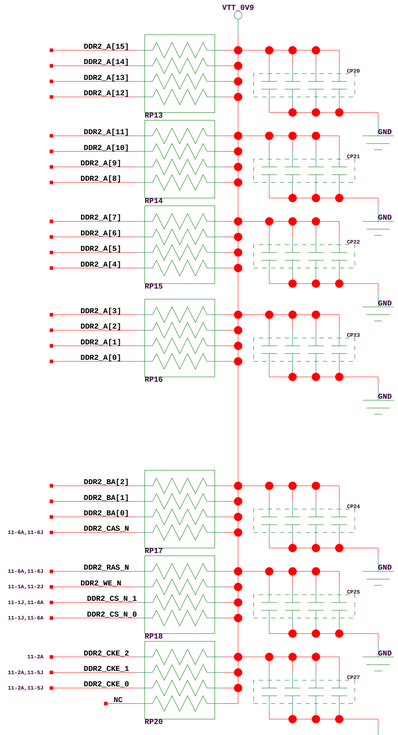
ROACH/iBOB2	**ROACH_TRANSCEIVERS_PSU**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-15-2007_15:53	DRAWN: F KAPP
PATH PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 10 OF 25

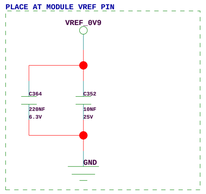


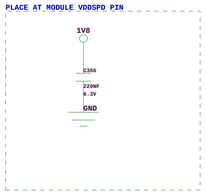


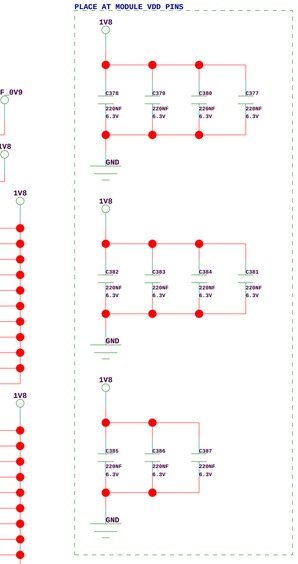


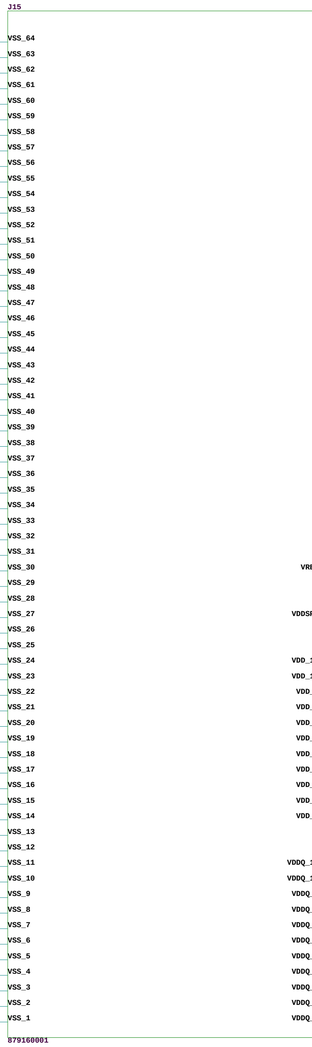
VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

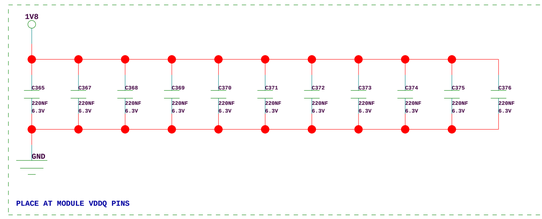




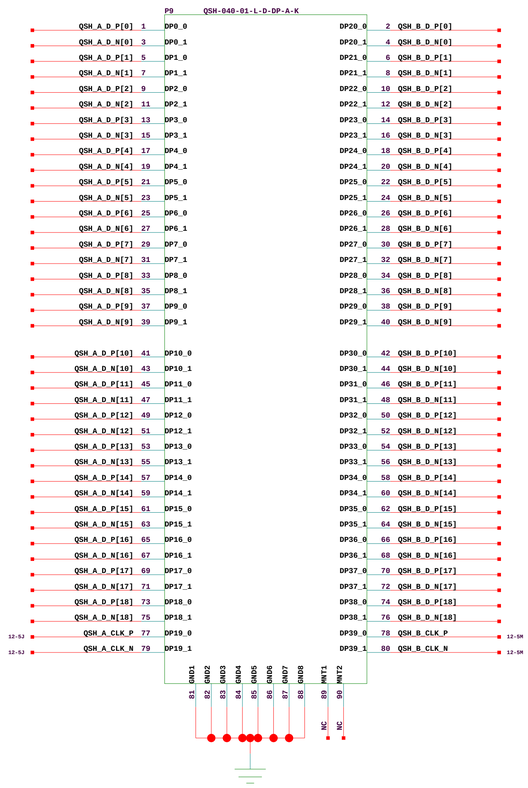


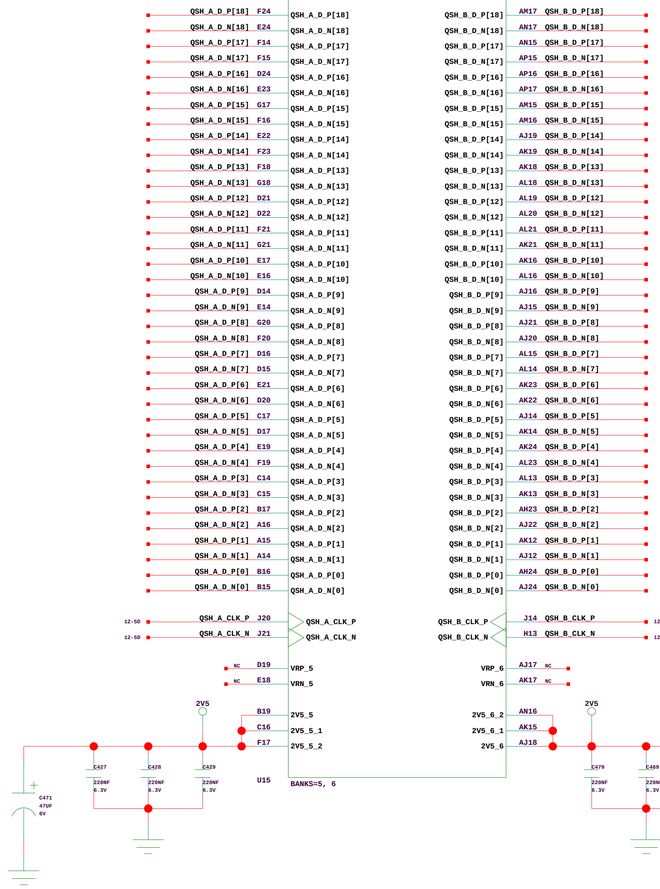






ROACH/iBOB2	**ROACH_DDR2_DIMM**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-15-2007_15:53 PATH PATH	DRAWN: F KAPP APPR:
	CHECKED: E BAUERMEISTER SHEET 11 OF 25





ROACH/iBOB2	**ROACH_DIFF_GPIO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-15-2007_15:53 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 12 OF 25

GPIOLVC18[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

GPIOLVC18[20] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

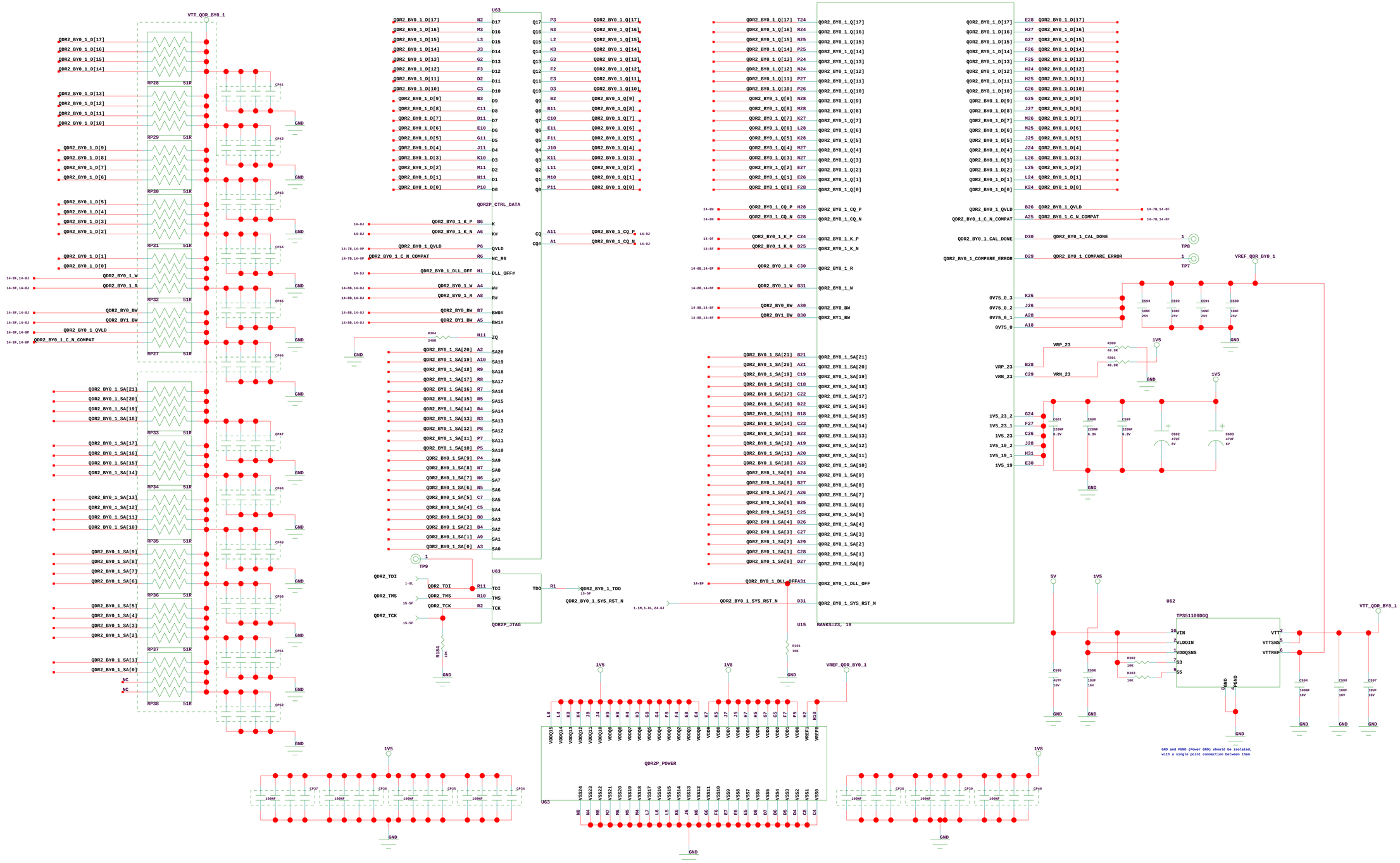
IO VOLTAGE LEVEL SELECT

1-2: 3.3V	DEFAULT
2-3: 2.5V	

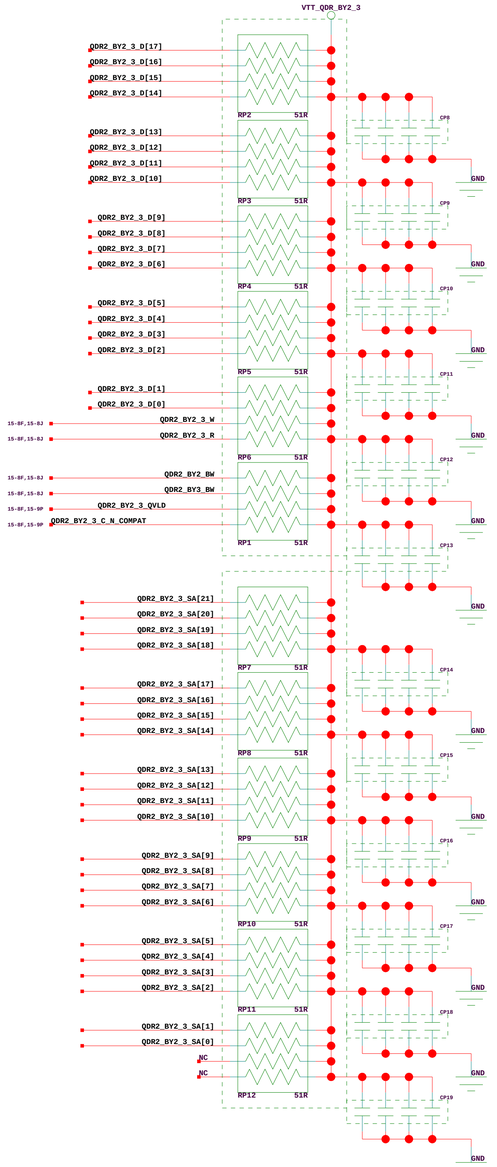
GPIOLVC18[4] IS DUAL FUNCTION:
1. DRIVES LED
2. CONTROLS DIRECTION ON GPIOLVC33[1-4]

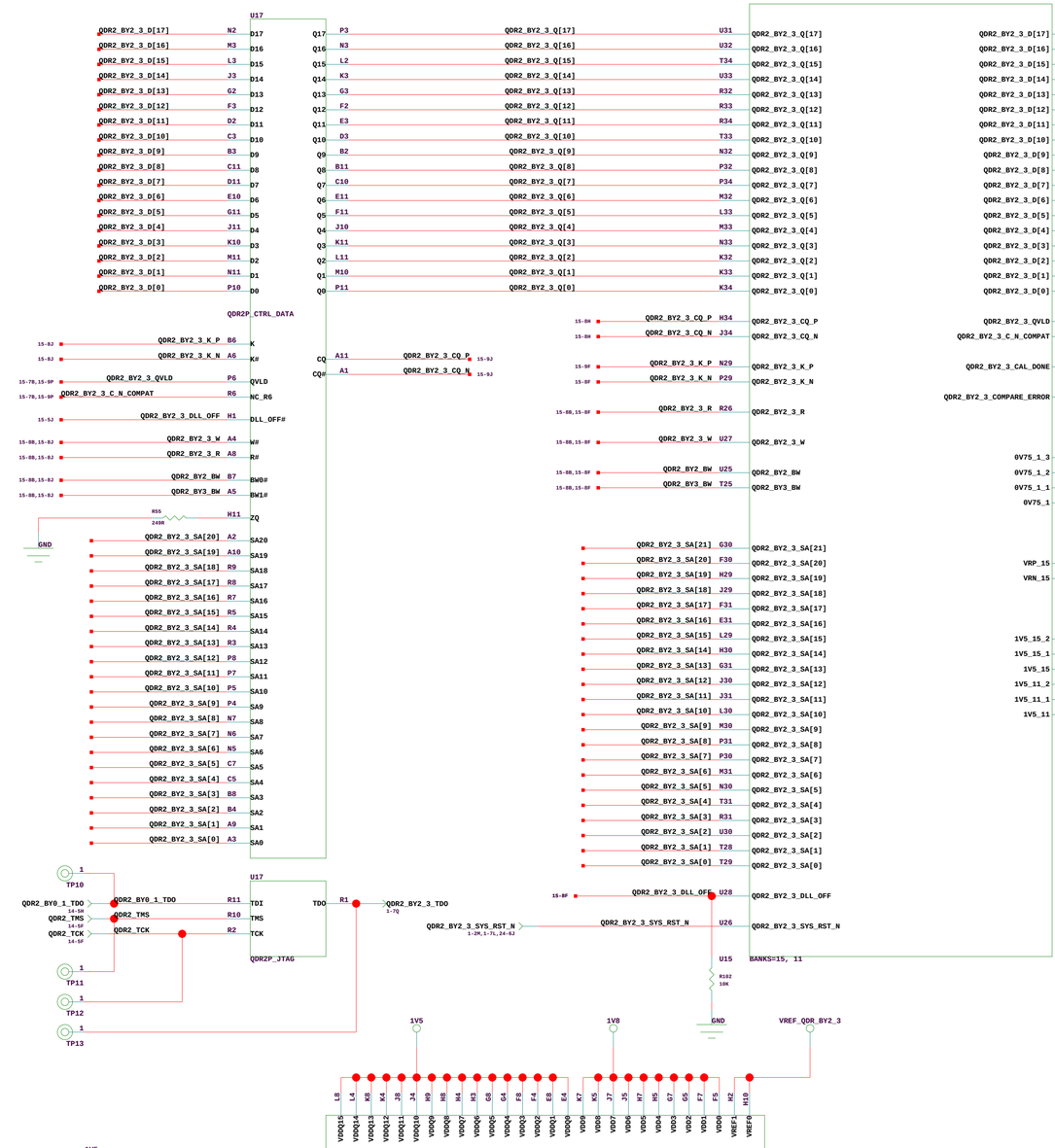
IF CR18 IS ON, CLOCK CAPABLE GPIO'S ARE OUTPUTS

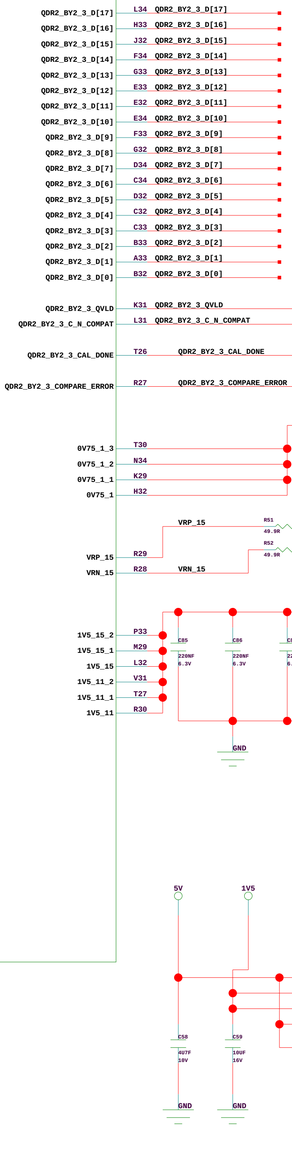
ROACH/iBOB2	ROACH_GPIO_MISC
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
11-15-2007_15:53 PATH PATH	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 13 OF 25

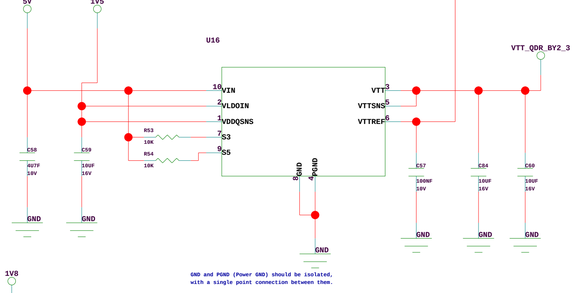


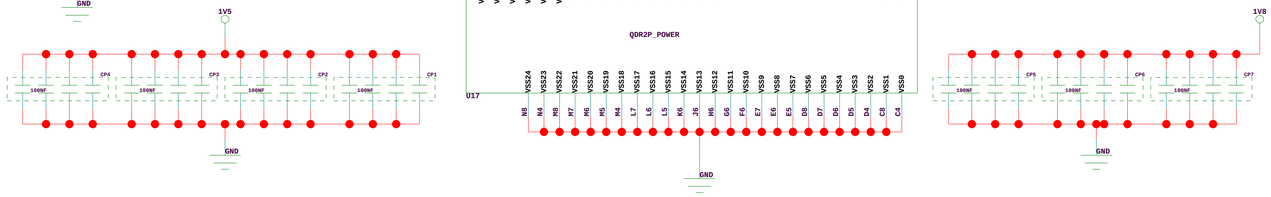
ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 14 OF 25
11-15-2007_15:53 PATH PATH	







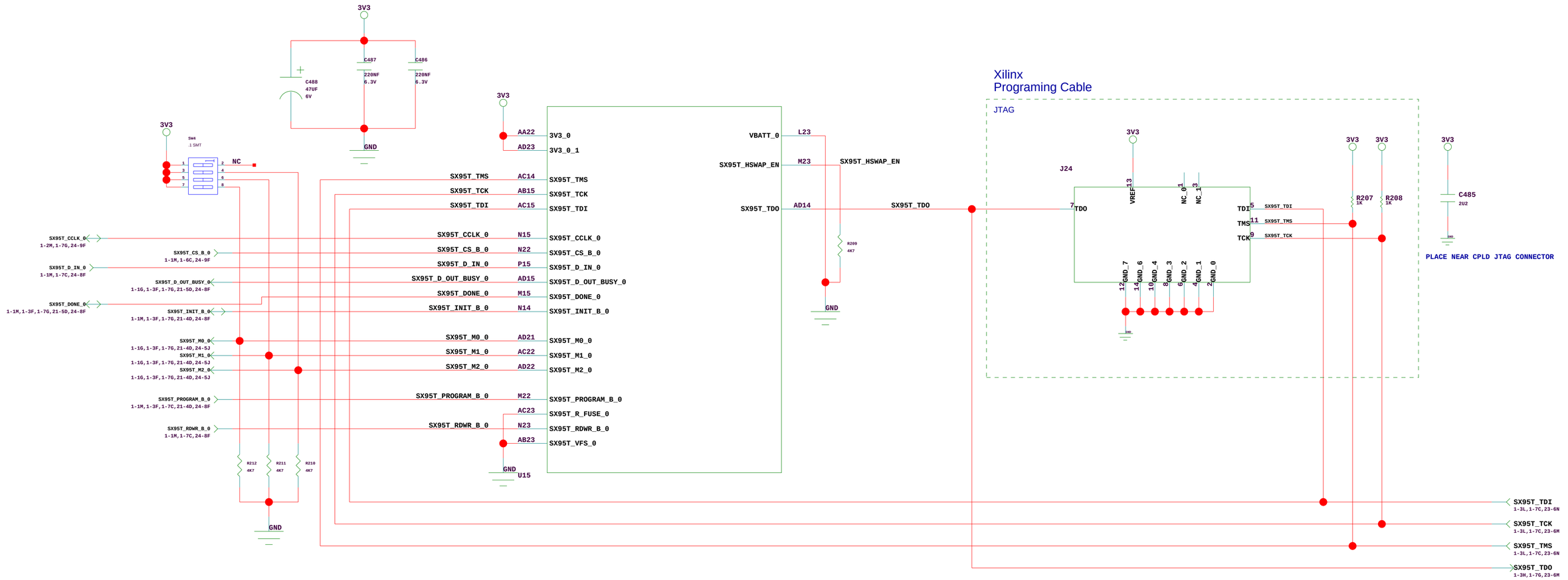




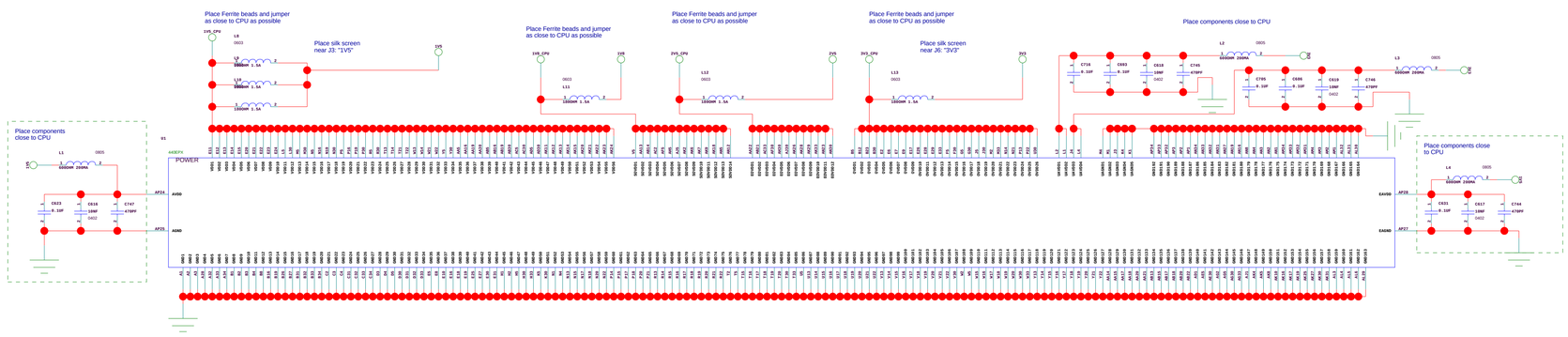
ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 15 OF 25
11-15-2007_15:53 PATH PATH	

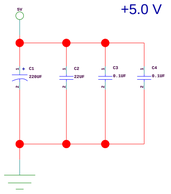
TBD

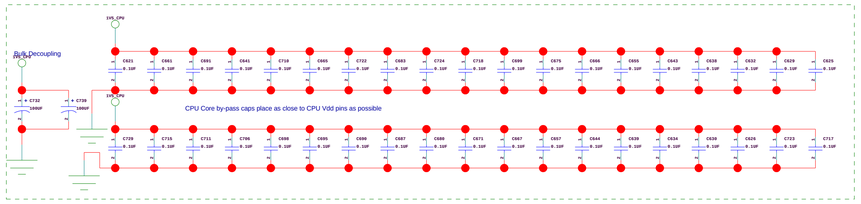
VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

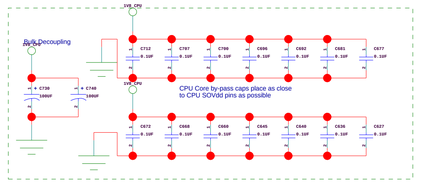


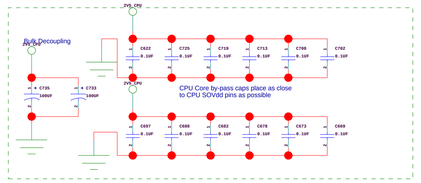
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
11-15-2007_15:53 PATH PATH	

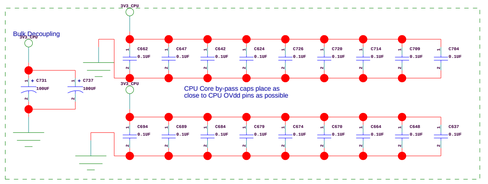


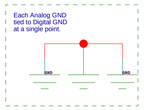










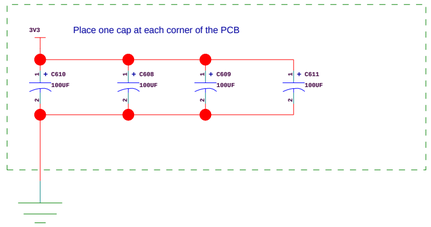


REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: **CASPER GROUP, UC BERKELEY** **NRAO, SOCORRO** **meerKAT, CAPE TOWN** http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET: 17 OF 25
11-15-2007_15:53 PATH PATH	

REMOVED 3V3 GENERATION



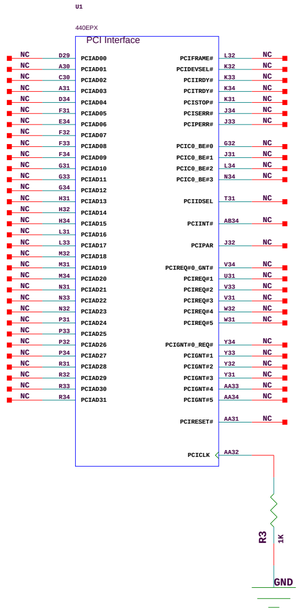
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	**ROACH_PPC_POWER_2**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 18 OF 25
11-15-2007_15:53 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-15-2007_15:53 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

Place nearest PHY pin 96

Place nearest PHY pin 101

Place nearest PHY pin 98

Place nearest PHY pin 100

Place as close to PHY CORE VDD power pins as possible

Place as close to PHY IO VDD power pins as possible

UNUSED SECOND ETHERNET MAC

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups. Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

Place resistors as close to CPU as possible and keep all traces lengths equal

Place resistors close to PHY all trace lengths equal

Place jumpers in line with signals

Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5

Place decoupling C as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible.

Ethernet LEDs

Top LED = SPEED/LINK
Green = 1000
Off = 10/100

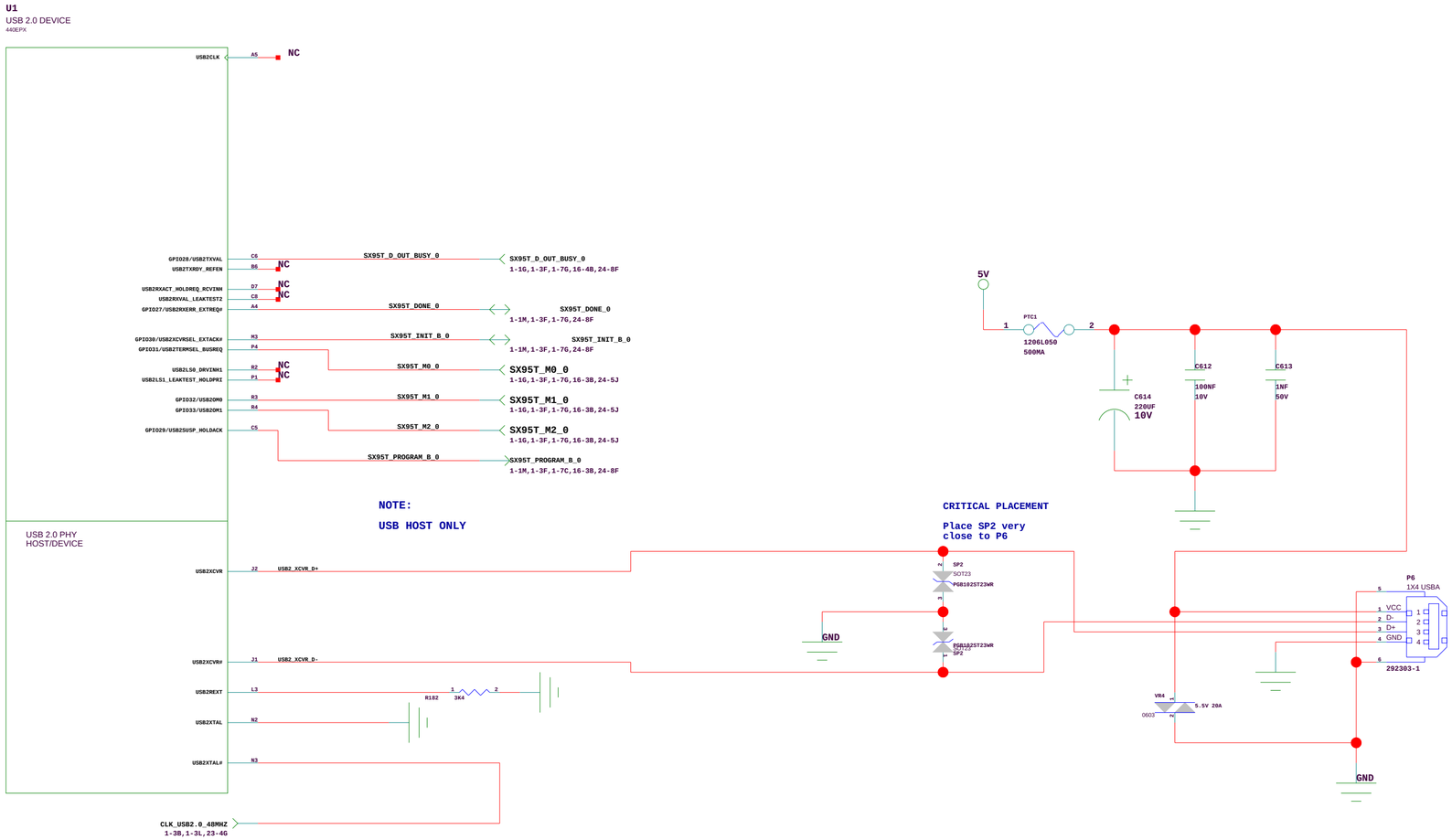
Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30

ETHERNET Mgt.

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

ROACH/iBOB2	ROACH_PPC_ETH1
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
11-15-2007_15:53	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 20 OF 25



ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25
11-15-2007_15:53 PATH PATH	

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

11-15-2007_15:53

PATH PATH

ROACH_PPC_DDR2

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

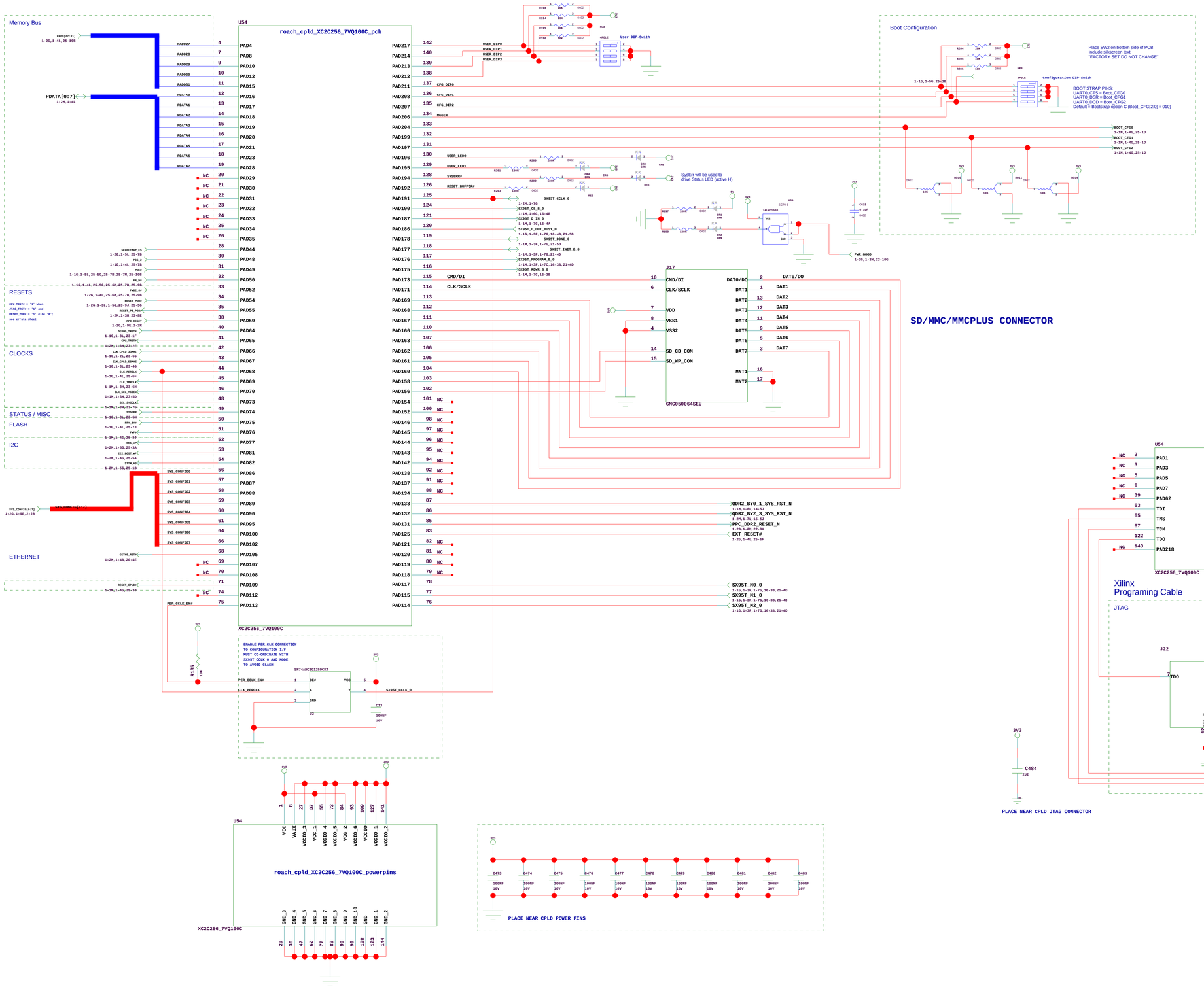
APPR:

CHECKED: E BAUERMEISTER

SHEET 22 OF 25


PWR_GOOD
1-2G,1-3H,24-8K
3V3
R41 15K 0402
D1 BAV70
R42 180R 0402
SPST SW1
C47 2.2UF
GND
RESET_PB_POR#
1-2M,1-3H,24-8C
PWR_GOOD monitors the +1.0v, 1V5, 1V8, 2V5, and 3V3 supplies
R28 3K3 0402
U31 SOT-23-5 MIC2774N-29
IN VDD MR/ RST/ GND
C604 0.1UF
R29 3K3 0402
RESET_POR# 6,11
1-2G,1-3L,1-5G,24-8C,25-5G
Critical Placement and Route
Clock Rules:
Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_SYS_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz
C48 18PF
C49 18PF
22.1184MHZ
Y1 SMT6X3
U9 SOIC-8 CY22381FX_0211
VDD XTALIN XTALOUT GND FS CLKC CLKB CLKA
R30 3K3 0402
SEL_SYSCLK
1-1M,1-3H,24-7C
CLK_1 CLK_2 CLK_3
RS1 33 0402
RS2 33 0402
RS3 33 0402
CLK_UART_11.0592MHZ
1-3L,1-5G,25-3D
CLK_SYS_33MHZ
CLK_CPLD_33MHZ
1-1G,1-2L,24-7C
C606 0.1UF
CLK_TMRCLK
1-1M,1-3H,24-7C
R24 1K 0402
SYSERR
1-1G,1-3L,24-7C
PPC_THERMONA
1-3L,1-9E,2-6L
PPC_THERMONB
1-3L,1-9E,2-4L
TEST POINT
TP1 R25 1K 0402
U1 440EPX
SYSTEM INTERRUPTS
SYSRESET# SYSCLK TMRCLK TESTEN SYSERR THERMONA THERMONB PSROOUT
IRQ0 IRQ1 IRQ2 IRQ3 IRQ4_GPIO44_DMAACK1 IRQ5_MODECTRL_DMAREQ1 IRQ6_GPIO45_EOT1_TC1 IRQ7_GPIO46_DMAREQ0 IRQ8_GPIO47_DMAACK0 IRQ9_GPIO48_EOT0_TC0
PPC440EPX-NTA533T
IRQ0-9 have programmable polarity per section 10.5.7 (UIC0_PR) 440ep user manual
R31 3K3 0402
R32 3K3 0402
R33 3K3 0402
R35 3K3 0402
GETH0_INT#
1-3H,1-4E,20-4E
MONITOR_INT
1-3H,1-9E,2-1P
V5_INT#
1-3H,1-5L,25-8Q
STTM_ALERT
1-3H,1-5L,25-2B
GPIO44
1-3L
SX95T_TDI
1-3L,1-7C,16-2L
SX95T_TCK
1-3L,1-7C,16-2L
SX95T_TMS
1-3L,1-7C,16-2L
SX95T_TDO
1-3H,1-7G,16-2L
RO1 1K 0402
RO2 1K 0402
RO3 1K 0402
RO4 1K 0402
RO5 1K 0402
R23 1K 0402
NO POP
RO1 - RO5
Critical Placement and Route
Clock Rules:
Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible
C51 18PF
C52 18PF
12.00 MHZ
Y2 SMT6X3
U24 CY2292FZX_0211
XTALIN XTALOUT S0 S1 S2_SUSPND# OE_SHDWN# GND_3 GND_11
VDD_2 VDD_14 CPUCLK CLKD CLKA CLKB CLKC XBUF
NC
CLK_SEL_M66EN
1-1M,1-3H,24-7C
R34 3K3 0402
CLK_6 CLK_7 CLK_8
RS7 33 0402
RS9 33 0402
RS10 33 0402
CLK_GETH0_25MHZ
1-3L,1-4B,20-4E
CLK_USB2.0_48MHZ
1-3B,1-3L,21-2C
CLK_CPLD_50MHZ
1-1G,1-3L,24-7C
C607 0.1UF
C605 0.1UF
TRACE & JTAG CONNECTORS
P1 2x8 .1IN M SMT
R37 10K 0402
R38 10K 0402
R39 10K 0402
CPU_TDO CPU_TDI CPU_TCK CPU_TMS CPU_HALT#
DEBUG_TRST#
R36 10K 0402
VCC_JTAG
R26 33 0402
C53 0.1UF
R26 is for current limiting and should be <100 Ohms.
Critical placement and routing of the Trace connector and nets. Up to CPU frequency/4
R27 3K3 0402
C54 0.1UF
TRACE PORT
J1 .25IN F SMT
TRC_CLK
U1 440EPX
RiscWatch JTAG
TRCCLK HALT#_DRVINH2
TRCBS0_GPIO49 TRCBS1_GPIO50 TRCBS2_GPIO51
TRCES0_GPIO52 TRCES1_GPIO53 TRCES2_GPIO54 TRCES3_GPIO55 TRCES4_GPIO56
TRCTS0_GPIO57 TRCTS1_GPIO58 TRCTS2_GPIO59 TRCTS3_GPIO60 TRCTS4_GPIO61 TRCTS5_GPIO62 TRCTS6_GPIO63
TCK TDO TDI TMS TRST#
CPU_TRST#
1-2M,1-3H,24-7C
DEBUG_TRST#
1-1G,1-3L,24-7C

ROACH/iBOB2	**ROACH_PPC_TST_CLK_IO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-15-2007_15:53	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 23 OF 25



ROACH/iBOB2	**ROACH_PPC_CPLD**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-15-2007_15:53 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 24 OF 25

PADD30 IS THE LSB FOR 16 BIT
WIDE BUS TRANSFERS

NOTE:
DMA SIGNALS
IN GREEN TEXT

PADD2 IS THE MSB

PDATA[0:31]
1-2M,1-4L

PADD[2:31]

PADD[2:31]
1-2G,1-4L,24-10B,25-10B

External Slave Peripheral

External Master Peripheral Interface

FLASH 32Mx16 4Mx8

UART

IIC0

IIC1_SPI

NAND Flash Interface

NOT USED

NO POP

UART Port 0

UART Port 1

J14

HLE-105-02-G-DV

U15

BANKS=1, 2, 4

CHIP SELECT 1

ROACH/iBOB2	ROACH_PPC_NVM_SERIAL
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
11-15-2007_15:53 PATH PATH	DRAWN: F KAPP APPR:
	CHECKED: E BAUERMEISTER SHEET 25 OF 25