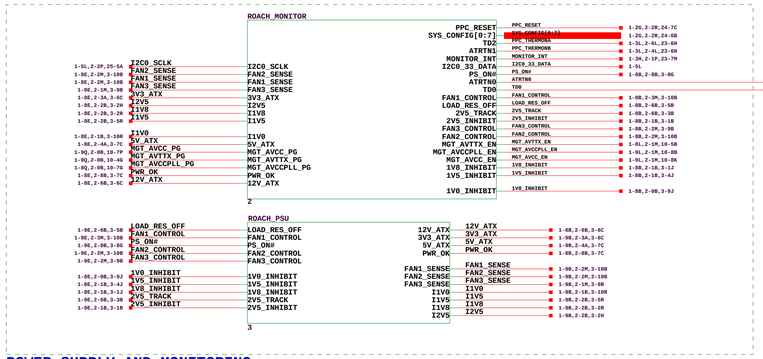
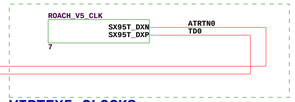
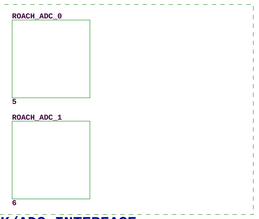
VIRTEX5

POWER SUPPLY AND MONITORING



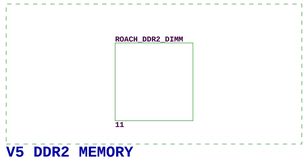
VIRTEX5 CLOCKS



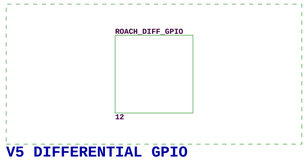


ZDOK/ADC INTERFACE

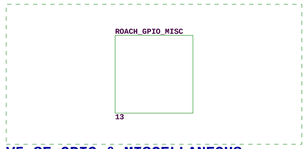
V5 DDR2 MEMORY



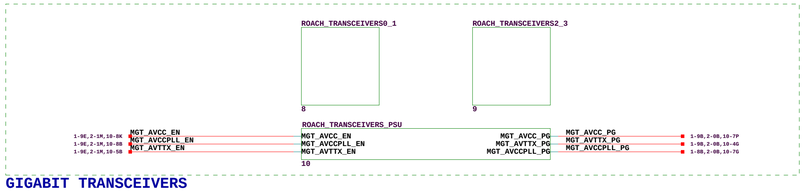
V5 DIFFERENTIAL GPIO



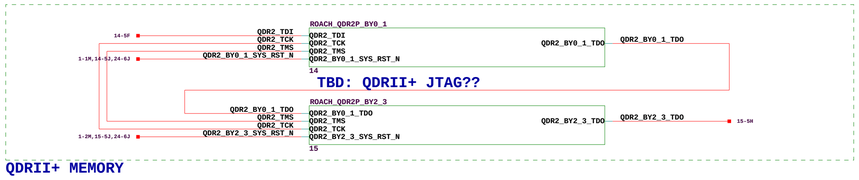
V5 SE GPIO & MISCELLANEOUS



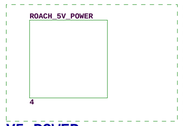
GIGABIT TRANSCEIVERS



QDRII+ MEMORY

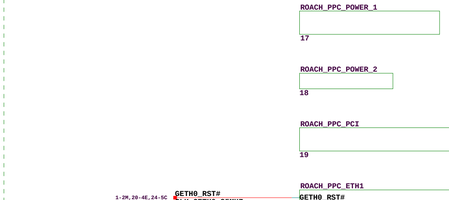


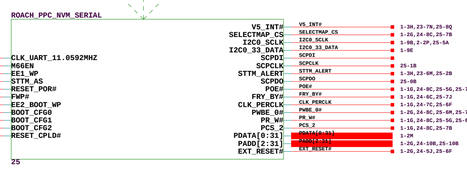
V5 POWER

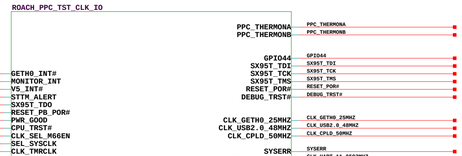


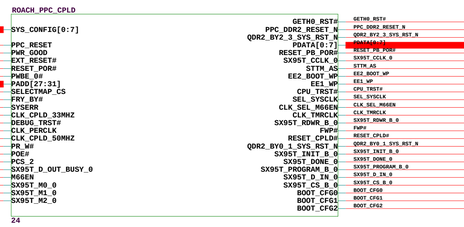
VIRTEX5 CONFIGURATION

PPC

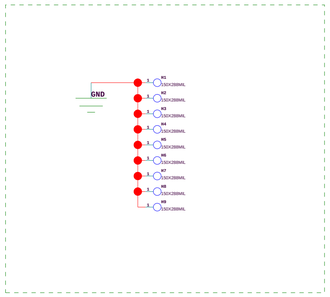








MECHANICAL



CONTRIBUTORS

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HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2	**ROACH_TOP**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-25-2007_14:59	DRAWN: F KAPP APPR:
PATH PATH	CHECKED: E BAUERMEISTER SHEET 1 OF 25

TIE TO 3V3AUX TO ENABLE PROGRAMMING VOLTAGE
TIE TO GROUND TO DISABLE PROGRAMMING VOLTAGE

TIE TO GROUND IF PLL'S ARE NOT USED

PLACE AT ACTEL 3V3 POWER PINS

PLACE AT ACTEL 1V5 POWER PINS

roach_AFS600_powerpins

roach_AFS600_pcb

roach_AFS600_configpins

PB POWER SWITCH

KEY - REMOVE PIN

MONITOR RESET

XPORT - PLACE IN REAR I/O REGION

ACTEL JTAG CONNECTOR

ROACH/iBOB2	ROACH_MONITOR
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-25-2007_14:59	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 2 OF 25

AUX FAN CONNECTORS - ATX 4 PIN

J21
1 GND
2 12V
3 SENSE
4 CONTROL
47053-1000
PLACE ON SILKSCREEN: FAN1
FAN1_SENSE 3
FAN1_CONTROL 4
FAN1_SENSE 1-8B,1-9B,2-2M
FAN1_CONTROL 1-8B,1-9E,2-2M

J20
1 GND
2 12V
3 SENSE
4 CONTROL
47053-1000
PLACE ON SILKSCREEN: FAN2
FAN2_SENSE 3
FAN2_CONTROL 4
FAN2_SENSE 1-8E,1-9B,2-2M
FAN2_CONTROL 1-8B,1-9E,2-2M

J19
1 GND
2 12V
3 SENSE
4 CONTROL
47053-1000
PLACE ON SILKSCREEN: FAN3
FAN3_SENSE 3
FAN3_CONTROL 4
FAN3_SENSE 1-8E,1-9B,2-1M
FAN3_CONTROL 1-8B,1-9E,2-2M

GND

ATX POWER CONNECTORS

5VAUX
N12V

J18
1 3V3_1
2 3V3_2
3 COM_1
4 5V_1
5 COM_2
6 5V_2
7 COM_3
8 PWR_OK
9 5VSB
10 12V1_1
11 12V1_2
12 3V3_3
13 3V3_4
14 _12V
15 COM_4
16 PS_ON#
17 COM_5
18 COM_6
19 COM_7
20 NC
21 5V_3
22 5V_4
23 5V_5
24 COM_8
44286-0007

PS_ON# 16
PS_ON# 1-8B,1-9E,2-8B
PWR_OK 8
PWR_OK 1-8B,1-8E,2-8B
5VAUX 9

J32
2 4 6 8 10
1 3 5 7 9
0015453110

5V_ATX 1-8E,1-9B,2-4A
3V3_ATX 1-8E,1-9B,2-3A
12V_ATX 1-8B,1-8E,2-6B

LOAD RESISTORS FOR ATX PSU MIN LOAD
SWITCH OFF ONCE LOAD EXCEEDS MINIMUM SPEC
ADJUST RESISTOR VALUES FOR ACTUAL SUPPLY

5VAUX
R180 10K
Q9 NDS331N
R185 10R 5W AC05000001009JLB00
Q8 BSS138
Q10 NDS331N
R187 56R 5W AC05000005609JLB00
LOAD_RES_OFF 1-8B,1-9B,2-8B
R181 1MEG
GND

J16
1 COM1
2 COM2
39-29-9042
12V1 3
12V2 4
GND

1V0
ROUTE FROM LOAD
PLACE RESISTOR CLOSE TO U50
ROUTE SHORTEST
R144 0R

PSU INPUT SUMMARY
VOLTAGE	5.0V +- 10%
CURRENT (MAX)	6.0A

5V
CHANGE!!
L6 BLM31PG121SN1B
C403 330UF 16V
C401 330UF 16V
C419 22UF 16V
GND

U50
30A SMPS MODULE
13 TURBOTRANS
10 SENSE+
2 VI_1
6 VI_0
1 INHIBIT/UVLADJ
14 TRACK
11 SENSE-
PTH05T210WAD
4 GND_3
7 GND_2
8 GND_1
3 GND_0

1V5
1V0_INHIBIT 1-8B,1-8E,2-6B
Q4 BSS138
ROUTE FROM LOAD

VO_0 5
VO_1 9
VOADJUST 12
R143 634K
DIRECT TO P8 ON U50, DEDICATED TRACE
C418 10UF
C117 10UF
C402 100UF 2V5
C400 100UF 2V5
C104 100UF 2V5
C105 100UF 2V5
I1V0 1-8E,1-9D,2-1B

PSU RAIL SUMMARY
VOLTAGE	1.0V +- 5%
SUPPLIES	FPGA CORE
CURRENT (QUIESCENT)	1.5A
CURRENT (ACTIVE)	26.8A
LOAD STEP	25.3A

1.2V SUPPLY DELETED - NOT REQUIRED

1V5
ROUTE FROM LOAD
PLACE RESISTOR CLOSE TO U51
ROUTE SHORTEST
R146 1K02

PSU INPUT SUMMARY
VOLTAGE	12V +- 10%
CURRENT (MAX)	0.8A

12V
L7 BLM31PG121SN1B
C404 330UF 16V
C420 22UF 16V
GND

U51
16A SMPS MODULE
6 TURBOTRANS
6 SENSE+
2 VI
11 INHIBIT/UVLADJ
10 TRACK
7 SENSE-
1 SMARTSYNC
PTH08T240WAD
4 GND_1
5 GND_0

1V8
1V5_INHIBIT 1-8B,1-8E,2-1B
Q5 BSS138
ROUTE FROM LOAD

VO 5
VOADJUST 8
R147 604R
DIRECT TO P8 ON U51, DEDICATED TRACE
C421 10UF
C405 100UF 2V5
I1V5 1-8E,1-9D,2-2B

PSU RAIL SUMMARY
VOLTAGE	1.5V +- 5%
SUPPLIES	FPGA IO, QDR, PPC
CURRENT (QUIESCENT)	0.25A
CURRENT (ACTIVE)	0.8A
LOAD STEP	0.55A

2V5
ROUTE FROM LOAD
PLACE RESISTOR CLOSE TO U53
ROUTE SHORTEST
R177 604R
2V5_TRACK 1-8B,1-9E,2-6B
R183 1K
C426 10UF

PSU INPUT SUMMARY
VOLTAGE	12V +- 10%
CURRENT (MAX)	0.8A

12V
L15 BLM31PG121SN1B
C412 330UF 16V
C424 22UF 16V
GND

U53
8 TURBOTRANS
6 SENSE+
2 VI
10 INHIBIT/UVLADJ
5 TRACK
6 SENSE-
1 SMARTSYNC
PTH08T230WAD
3 GND

2V5_INHIBIT 1-8B,1-9E,2-1B
Q7 BSS138
ROUTE FROM LOAD

VO 4
VOADJUST 7
R179 2K37
DIRECT TO P8 ON U53, DEDICATED TRACE
C425 10UF 16V
C413 680UF 4V
I2V5 1-8E,1-9D,2-2B

PSU RAIL SUMMARY
VOLTAGE	2.5V +- 5%
SUPPLIES	FPGA, ZDOK PPC, PHY
CURRENT (QUIESCENT)	0.1A
CURRENT (ACTIVE)	3.6A
LOAD STEP	3.5A

1V8
ROUTE FROM LOAD
PLACE RESISTOR CLOSE TO U52
ROUTE SHORTEST
R149 1K02

PSU INPUT SUMMARY
VOLTAGE	12V +- 10%
CURRENT (MAX)	1.8A

12V
L14 BLM31PG121SN1B
C409 330UF 16V
C423 22UF 16V
GND

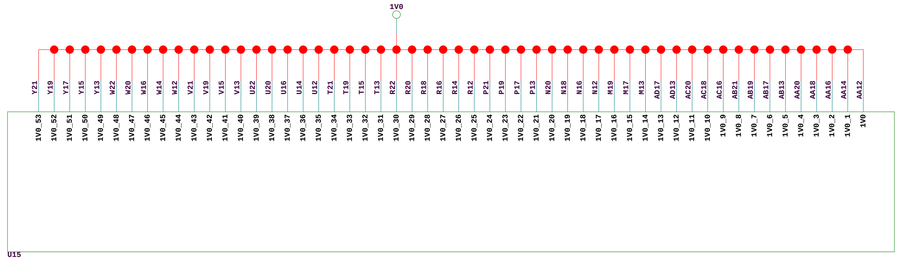
U27
16A SMPS MODULE
6 TURBOTRANS
6 SENSE+
2 VI
11 INHIBIT/UVLADJ
10 TRACK
7 SENSE-
1 SMARTSYNC
PTH08T220WAD
4 GND_1
5 GND_0

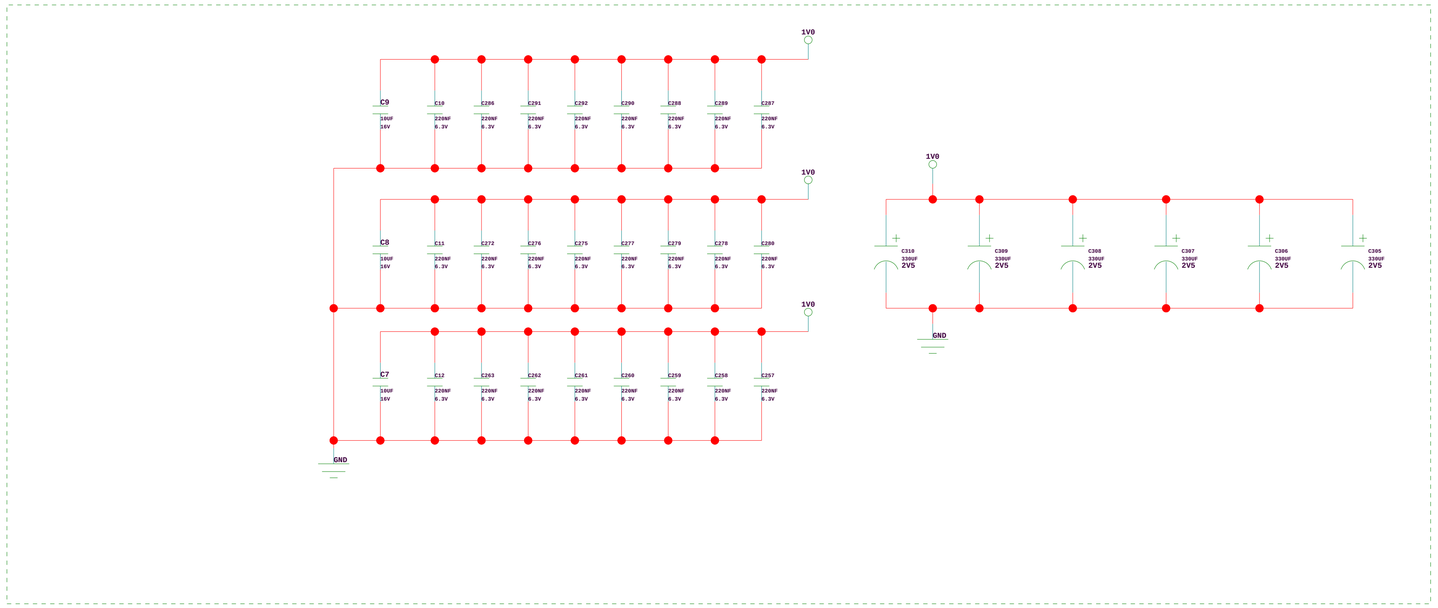
2V5
1V8_INHIBIT 1-8B,1-8E,2-1B
Q6 BSS138
ROUTE FROM LOAD

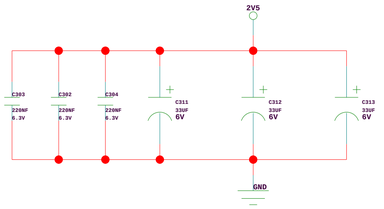
VO 5
VOADJUST 8
R148 487R
DIRECT TO P8 ON PTH08T210W, DEDICATED TRACE
C422 10UF
C410 100UF 2V5
I1V8 1-8E,1-9D,2-2B

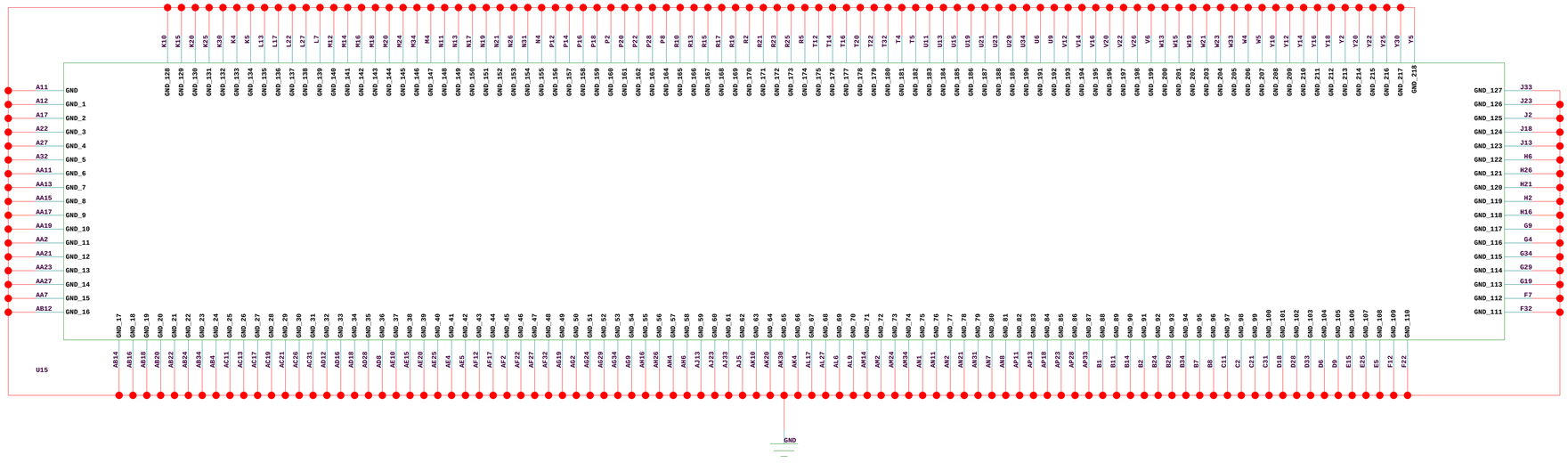
PSU RAIL SUMMARY
VOLTAGE	1.8V +- 5%
SUPPLIES	FPGA IO, DDR2 x 2
CURRENT (QUIESCENT)	1A
CURRENT (ACTIVE)	12.9A
LOAD STEP	11.9A

ROACH/iBOB2	ROACH_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-25-2007_14:59 PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 3 OF 25









ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
10-25-2007_14:59 PATH PATH	

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

10-25-2007_14:59

PATH PATH

ROACH_ADC_0

DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 5 OF 25

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

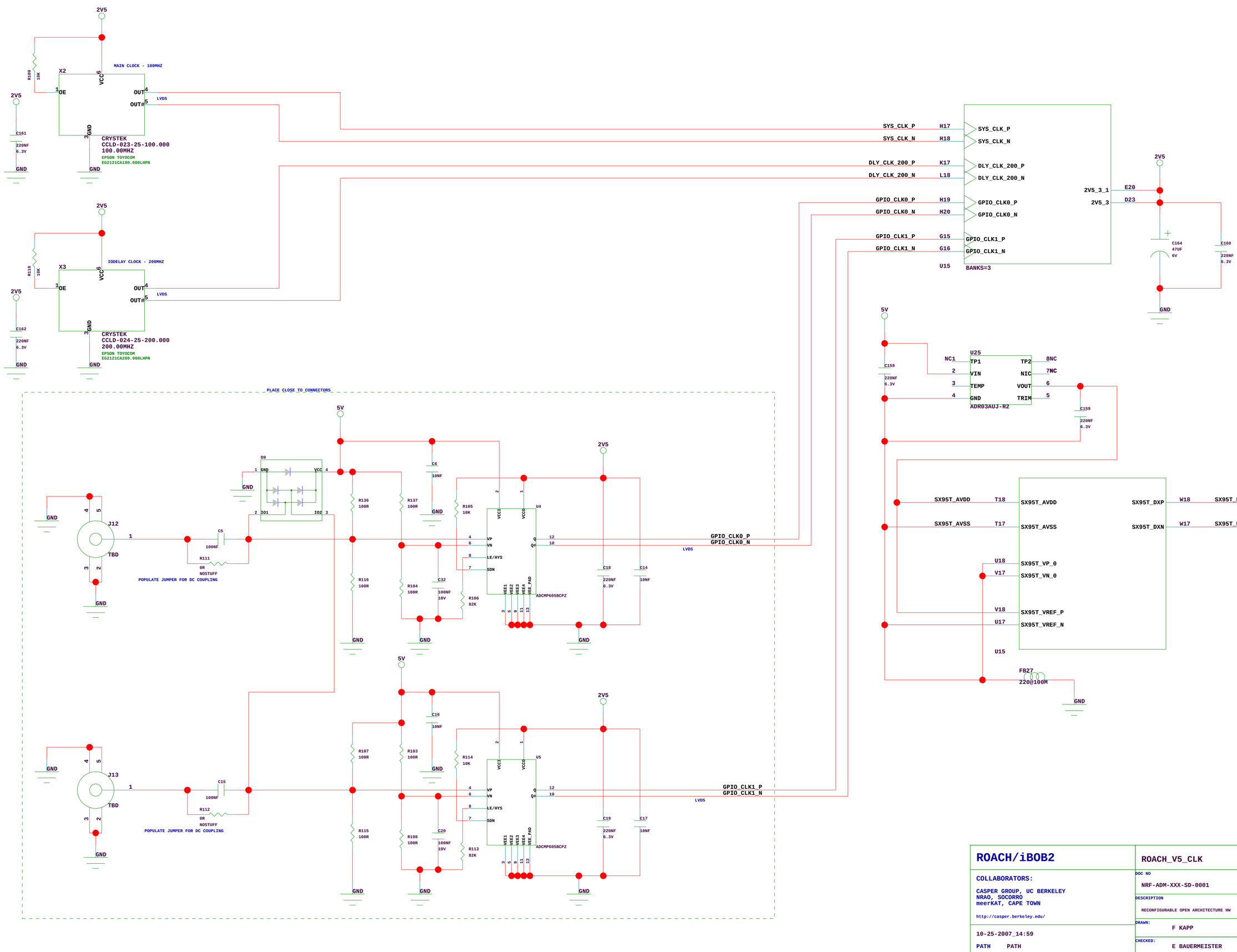
http://casper.berkeley.edu/

10-25-2007_14:59

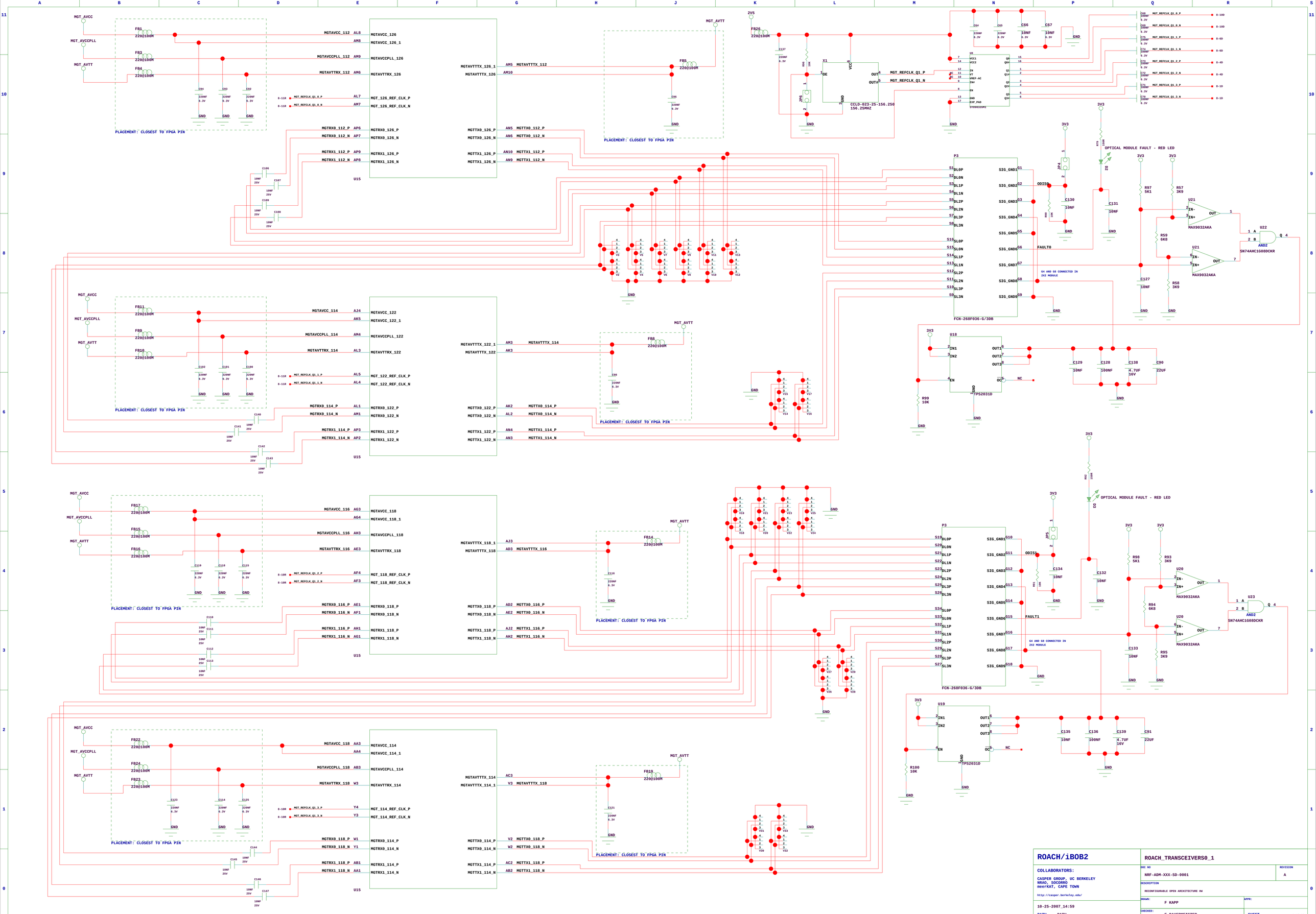
PATH PATH

ROACH_ADC_1

DOC NO: NRF-ADM-XXX-SD-0001	REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW	
DRAWN: F KAPP	APPR:
CHECKED: E BAUERMEISTER	SHEET 6 OF 25



ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
10-25-2007_14:59 PATH PATH	


MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB1 220@100M
FB3 220@100M
FB4 220@100M
MGTAVCC_112 AL8
AM8
MGTAVCCPLL_112 AM9
MGTAVTTRX_112 AM6
MGTAVCC_126
MGTAVCC_126_1
MGTAVCCPLL_126
MGTAVTTRX_126
C84 220NF 6.3V
C93 220NF 6.3V
C92 220NF 6.3V
GND
PLACEMENT: CLOSEST TO FPGA PIN
MGT_AVTT
FB5 220@100M
C96 220NF 6.3V
MGTAVTTTX_126_1 AM5 MGTAVTTTX_112
MGTAVTTTX_126 AM10
PLACEMENT: CLOSEST TO FPGA PIN
2V5
FB26 220@100M
C137 220NF 6.3V
R84 10K
X1
JP6
OE
VCC
OUT
CCLD-023-25-156.250
156.25MHZ
C64 220NF 6.3V
C65 220NF 6.3V
C66 10NF 6.3V
C67 10NF 6.3V
U8
VCC1
VCC2
IN
VT
VREF-AC
ZBW
EN
GND
EXP_PAD
SY89832UMI
MGT_REFCLK_Q1_P
MGT_REFCLK_Q1_N
Q0
Q0#
Q1
Q1#
Q2
Q2#
Q3
Q3#
C68 100NF 6.3V
C69 100NF 6.3V
C75 100NF 6.3V
C74 100NF 6.3V
C73 100NF 6.3V
C72 100NF 6.3V
C71 100NF 6.3V
C70 100NF 6.3V
MGT_REFCLK_Q1_0_P
MGT_REFCLK_Q1_0_N
MGT_REFCLK_Q1_1_P
MGT_REFCLK_Q1_1_N
MGT_REFCLK_Q1_2_P
MGT_REFCLK_Q1_2_N
MGT_REFCLK_Q1_3_P
MGT_REFCLK_Q1_3_N
B-10D
B-6D
B-4D
B-1D
MGTRX0_112_P AP6
MGTRX0_112_N AP7
MGTRX1_112_P AP9
MGTRX1_112_N AP8
MGTRX0_126_P
MGTRX0_126_N
MGTRX1_126_P
MGTRX1_126_N
MGTTX0_126_P AN5 MGTTX0_112_P
MGTTX0_126_N AN6 MGTTX0_112_N
MGTTX1_126_P AN10 MGTTX1_112_P
MGTTX1_126_N AN9 MGTTX1_112_N
U15
C106 10NF 25V
C107 10NF 25V
C109 10NF 25V
C108 10NF 25V
B-11R MGT_REFCLK_Q1_0_P AL7
B-11R MGT_REFCLK_Q1_0_N AM7
MGT_126_REF_CLK_P
MGT_126_REF_CLK_N
P3
DL0P
DL0N
DL1P
DL1N
DL2P
DL2N
DL3P
DL3N
SL0P
SL0N
SL1P
SL1N
SL2P
SL2N
SL3P
SL3N
SIG_GND1
SIG_GND2
SIG_GND3
SIG_GND4
SIG_GND5
SIG_GND6
SIG_GND7
SIG_GND8
SIG_GND9
FCN-268F036-G/3DB
3V3
JP4
ODIS0
R85 10K
C130 10NF
GND
FAULT0
G4 AND G8 CONNECTED IN 2X2 MODULE
R79 100R
D2
OPTICAL MODULE FAULT - RED LED
C131 10NF
R97 5K1
RS7 3K9
RS9 6K8
RS8 3K9
U21 MAX9032AKA
U22 SN74AHC1G08DCKR
AND2
C127 10NF
V1 V2 V3 V4 V5 V6 V7 V8 V9 V10 V11 V12 V13
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB11 220@100M
FB9 220@100M
FB10 220@100M
MGTAVCC_114 AJ4
AK5
MGTAVCCPLL_114 AM4
MGTAVTTRX_114 AL3
MGTAVCC_122
MGTAVCC_122_1
MGTAVCCPLL_122
MGTAVTTRX_122
C102 220NF 6.3V
C101 220NF 6.3V
C100 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTRX0_114_P AL1
MGTRX0_114_N AM1
MGTRX1_114_P AP3
MGTRX1_114_N AP2
MGTRX0_122_P
MGTRX0_122_N
MGTRX1_122_P
MGTRX1_122_N
C140 10NF 25V
C141 10NF 25V
C142 10NF 25V
C143 10NF 25V
B-11R MGT_REFCLK_Q1_1_P AL5
B-11R MGT_REFCLK_Q1_1_N AL4
MGT_122_REF_CLK_P
MGT_122_REF_CLK_N
MGTAVTTTX_122_1 AM3 MGTAVTTTX_114
MGTAVTTTX_122 AK3
MGTTX0_122_P AK2 MGTTX0_114_P
MGTTX0_122_N AL2 MGTTX0_114_N
MGTTX1_122_P AN4 MGTTX1_114_P
MGTTX1_122_N AN3 MGTTX1_114_N
FB8 220@100M
C99 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
V14 V15 V16 V17
U18
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
TPS2031D
R99 10K
C129 10NF
C128 100NF
C138 4.7UF 16V
C90 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB17 220@100M
FB15 220@100M
FB16 220@100M
MGTAVCC_116 AG3
AG4
MGTAVCCPLL_116 AH3
MGTAVTTRX_116 AE3
MGTAVCC_118
MGTAVCC_118_1
MGTAVCCPLL_118
MGTAVTTRX_118
C119 220NF 6.3V
C118 220NF 6.3V
C115 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTRX0_116_P AE1
MGTRX0_116_N AF1
MGTRX1_116_P AH1
MGTRX1_116_N AG1
MGTRX0_118_P
MGTRX0_118_N
MGTRX1_118_P
MGTRX1_118_N
C110 10NF 25V
C111 10NF 25V
C112 10NF 25V
C113 10NF 25V
B-10R MGT_REFCLK_Q1_2_P AF4
B-10R MGT_REFCLK_Q1_2_N AF3
MGT_118_REF_CLK_P
MGT_118_REF_CLK_N
MGTTX0_118_P AD2 MGTTX0_116_P
MGTTX0_118_N AE2 MGTTX0_116_N
MGTTX1_118_P AJ2 MGTTX1_116_P
MGTTX1_118_N AH2 MGTTX1_116_N
FB14 220@100M
C116 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
V18 V19 V20 V21 V22 V23 V24 V25 V26 V27 V28 V29
R98 5K1
R93 3K9
R94 6K8
R95 3K9
U20 MAX9032AKA
U23 SN74AHC1G08DCKR
C132 10NF
C133 10NF
R92 100R
D3
OPTICAL MODULE FAULT - RED LED
JP5
ODIS1
R91 10K
C134 10NF
FAULT1
G4 AND G8 CONNECTED IN 2X2 MODULE
FCN-268F036-G/3DB
U19
IN1
IN2
EN
OUT1
OUT2
OUT3
OC
NC
TPS2031D
R100 10K
C135 10NF
C136 100NF
C139 4.7UF 16V
C91 22UF
MGT_AVCC
MGT_AVCCPLL
MGT_AVTT
FB22 220@100M
FB24 220@100M
FB23 220@100M
MGTAVCC_118 AA3
AA4
MGTAVCCPLL_118 AB3
MGTAVTTRX_118 W3
MGTAVCC_114
MGTAVCC_114_1
MGTAVCCPLL_114
MGTAVTTRX_114
C123 220NF 6.3V
C114 220NF 6.3V
C125 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
MGTRX0_118_P W1
MGTRX0_118_N Y1
MGTRX1_118_P AB1
MGTRX1_118_N AA1
MGTRX0_114_P
MGTRX0_114_N
MGTRX1_114_P
MGTRX1_114_N
C144 10NF 25V
C145 10NF 25V
C146 10NF 25V
C147 10NF 25V
B-10R MGT_REFCLK_Q1_3_P Y4
B-10R MGT_REFCLK_Q1_3_N Y3
MGT_114_REF_CLK_P
MGT_114_REF_CLK_N
MGTTX0_114_P V2 MGTTX0_118_P
MGTTX0_114_N W2 MGTTX0_118_N
MGTTX1_114_P AC2 MGTTX1_118_P
MGTTX1_114_N AB2 MGTTX1_118_N
FB19 220@100M
C121 220NF 6.3V
PLACEMENT: CLOSEST TO FPGA PIN
V30 V31 V32 V33
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
10-25-2007_14:59
PATH PATH
ROACH_TRANSCEIVERS0_1
DOC NO NRF-ADM-XXX-SD-0001
REVISION A
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 8 OF 25

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

CCLD-023-25-156.250
156.25MHZ

OPTICAL MODULE FAULT - RED LED

G4 AND G8 CONNECTED IN
2X2 MODULE

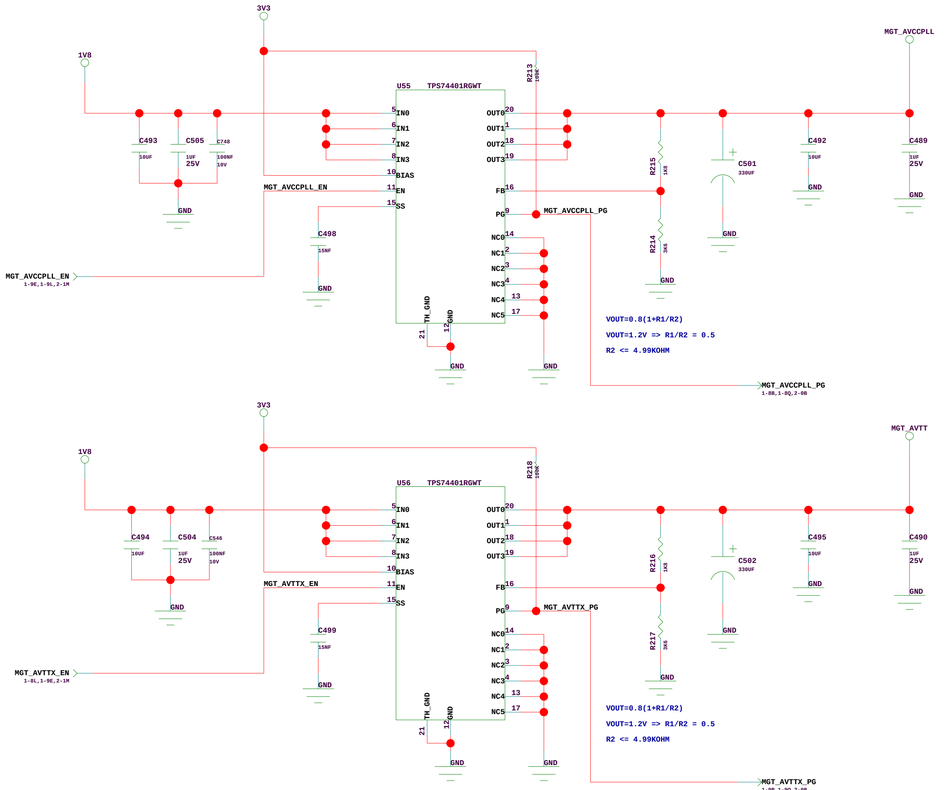
FCN-268F036-G/3DB

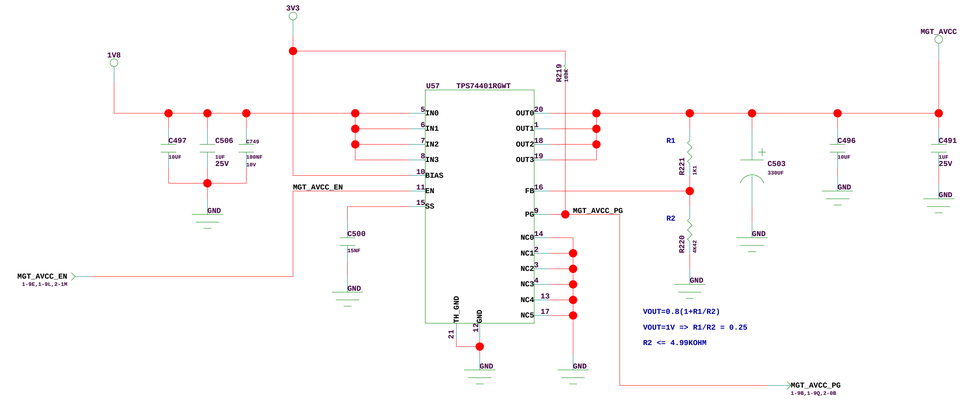
MAX9032AKA

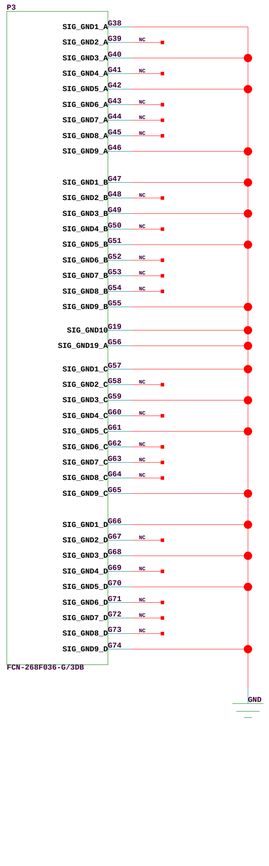
AND2
SN74AHC1G08DCKR

TPS2031D

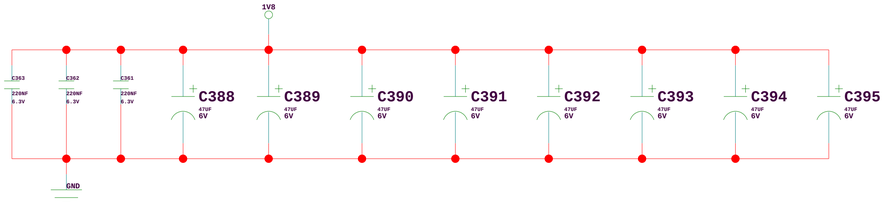
ROACH/iBOB2	ROACH_TRANSCEIVERS2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-25-2007_14:59	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 9 OF 25

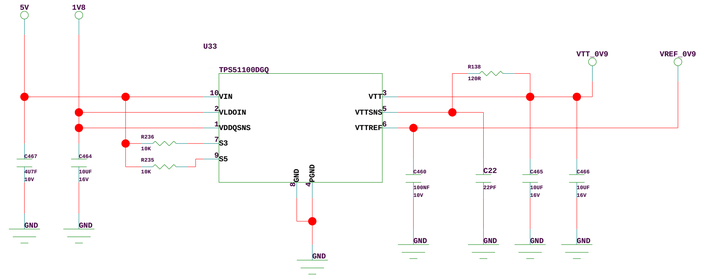


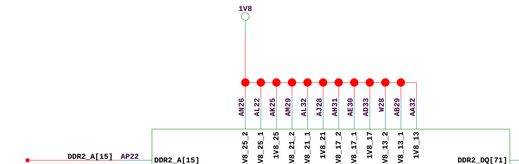


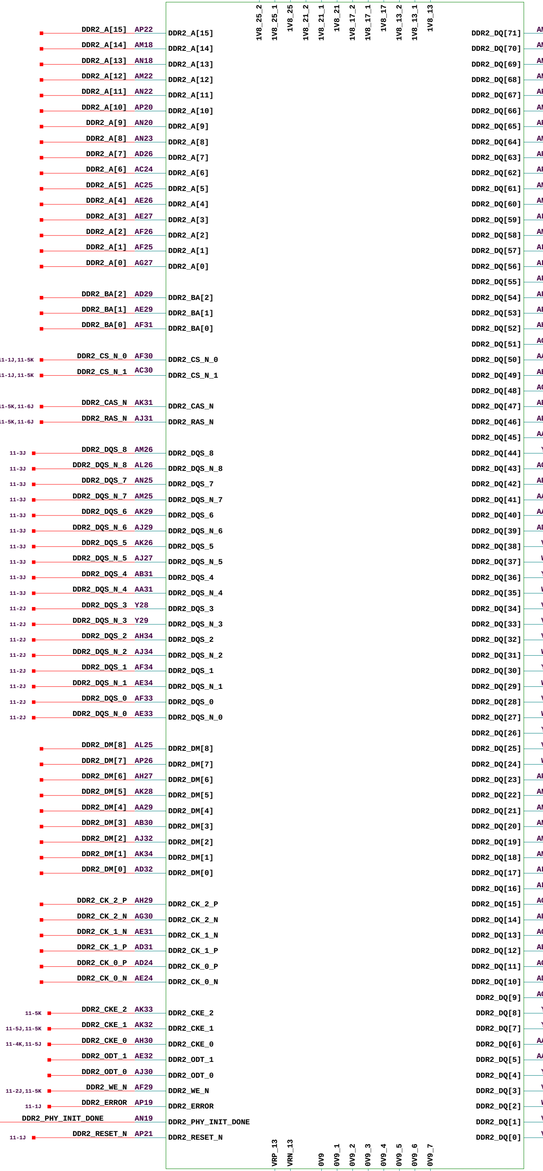


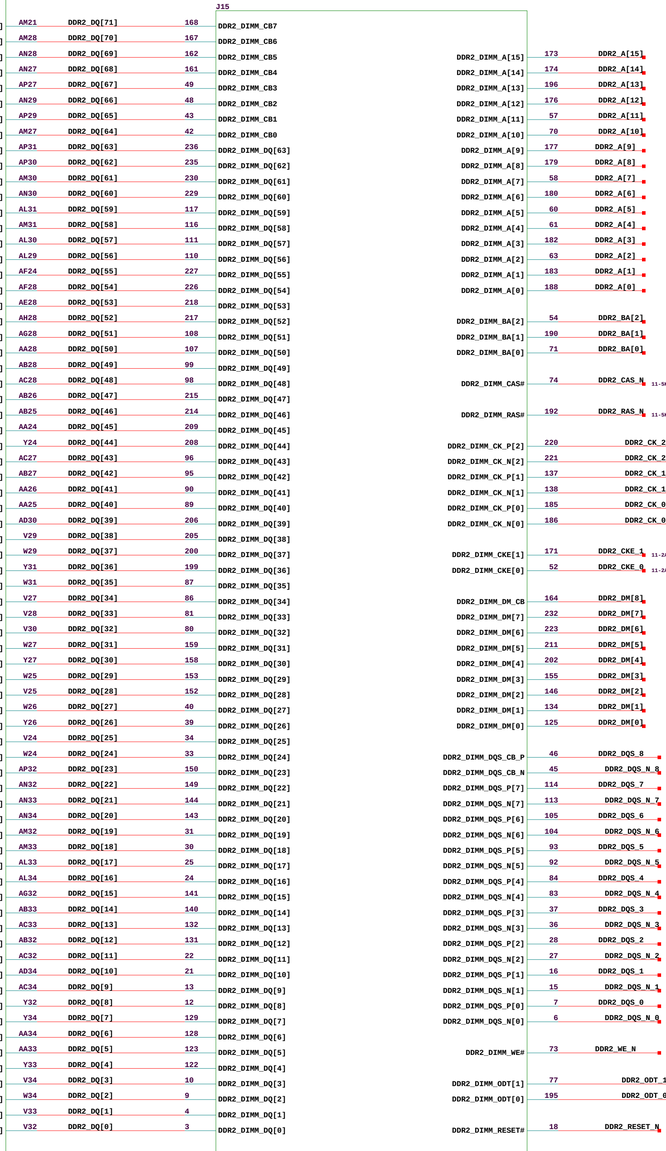
ROACH/iBOB2	ROACH_TRANSCEIVERS_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-25-2007_14:59 PATH PATH	DRAWN: F KAPP · APPR:
	CHECKED: E BAUERMEISTER · SHEET 10 OF 25

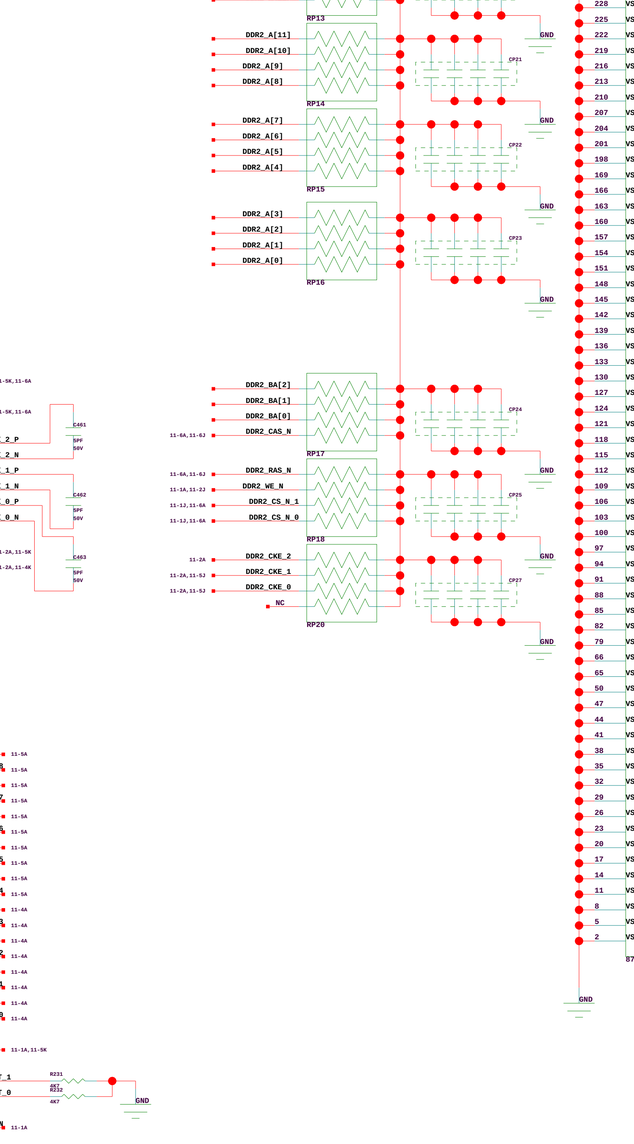


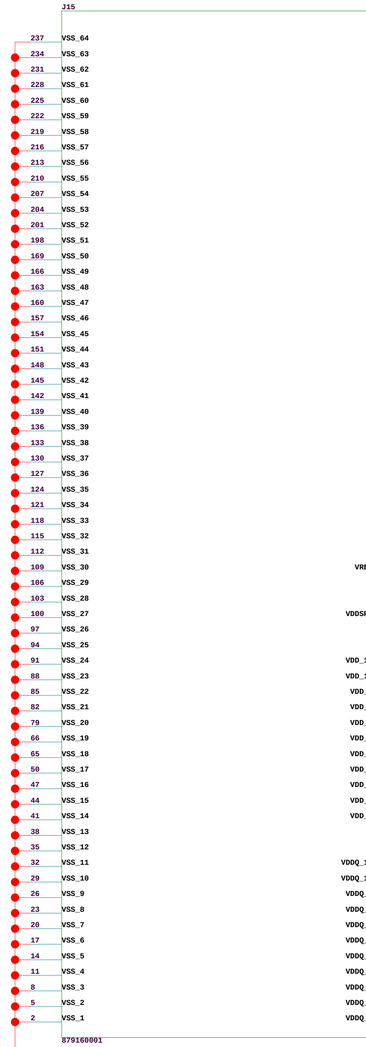


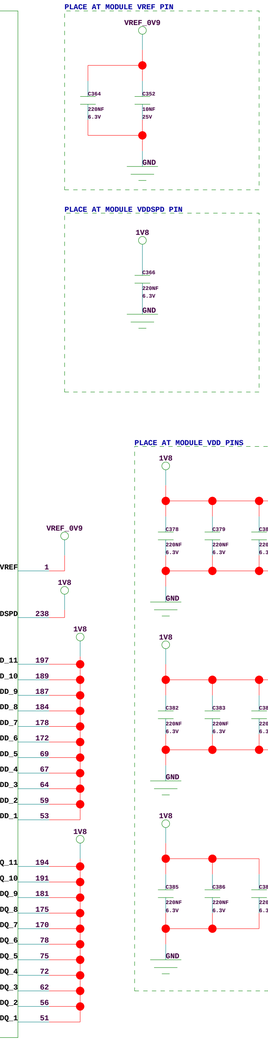


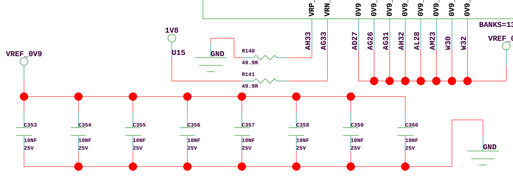


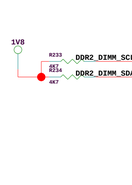




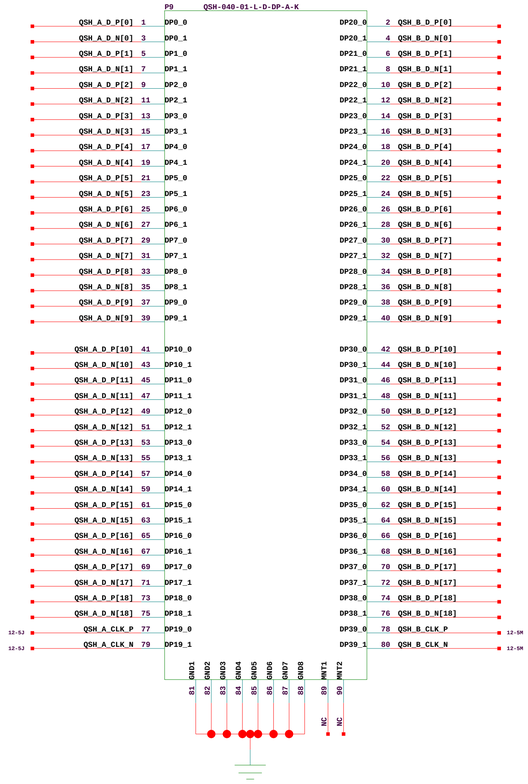


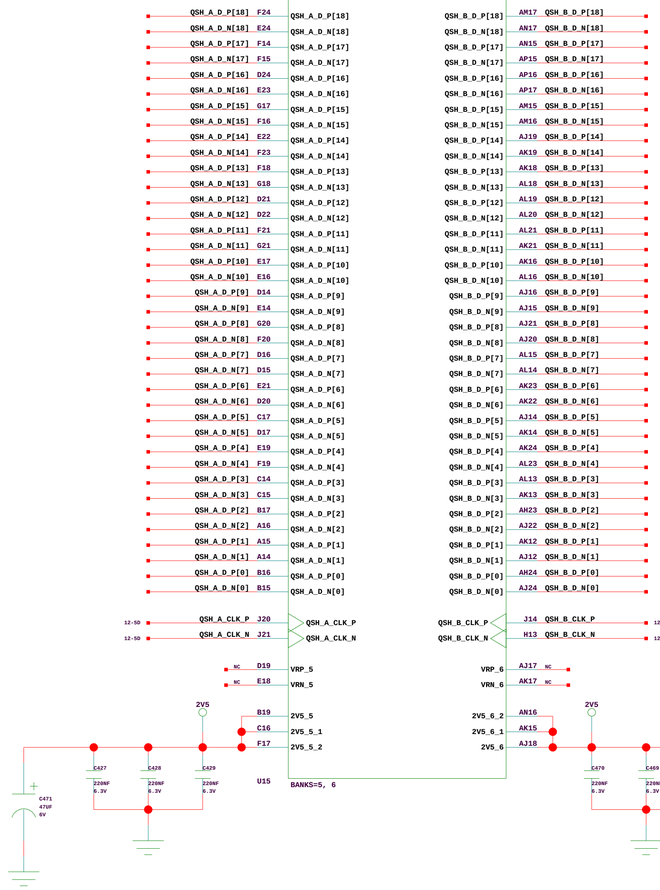






ROACH/iBOB2	**ROACH_DDR2_DIMM**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-25-2007_14:59 PATH PATH	DRAWN: F KAPP APPR:
	CHECKED: E BAUERMEISTER SHEET 11 OF 25





ROACH/iBOB2	**ROACH_DIFF_GPIO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-25-2007_14:59 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 12 OF 25

GPIOLVC18[4] SELECTS DIRECTION
ON U13 AND U14:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

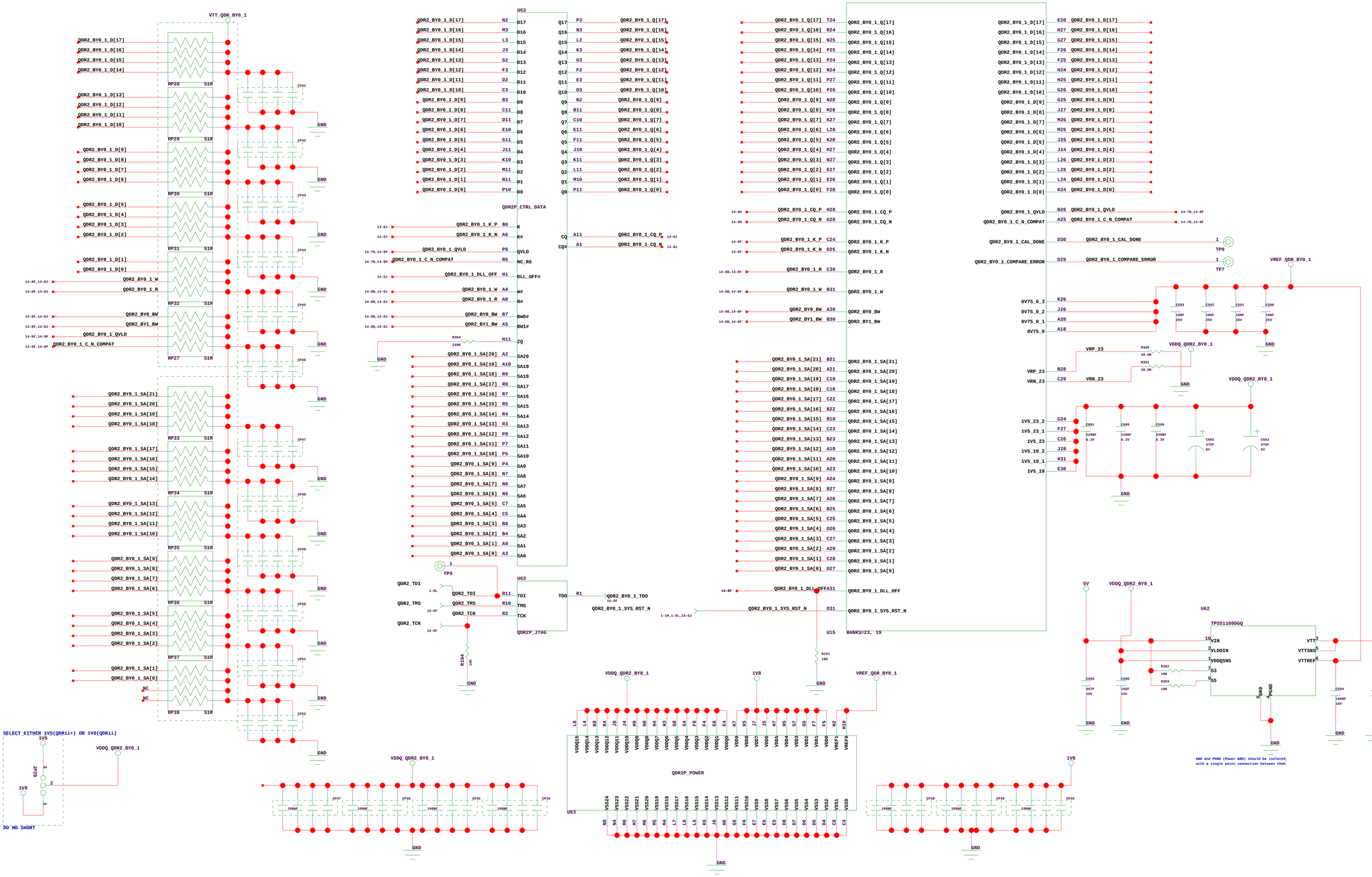
GPIOLVC18[20] SELECTS DIRECTION
ON U10 AND U11:
LOW - OUTPUT FROM ROACH
HIGH - INPUT TO ROACH

IO VOLTAGE LEVEL SELECT	
1-2: 3.3V	DEFAULT
2-3: 2.5V	

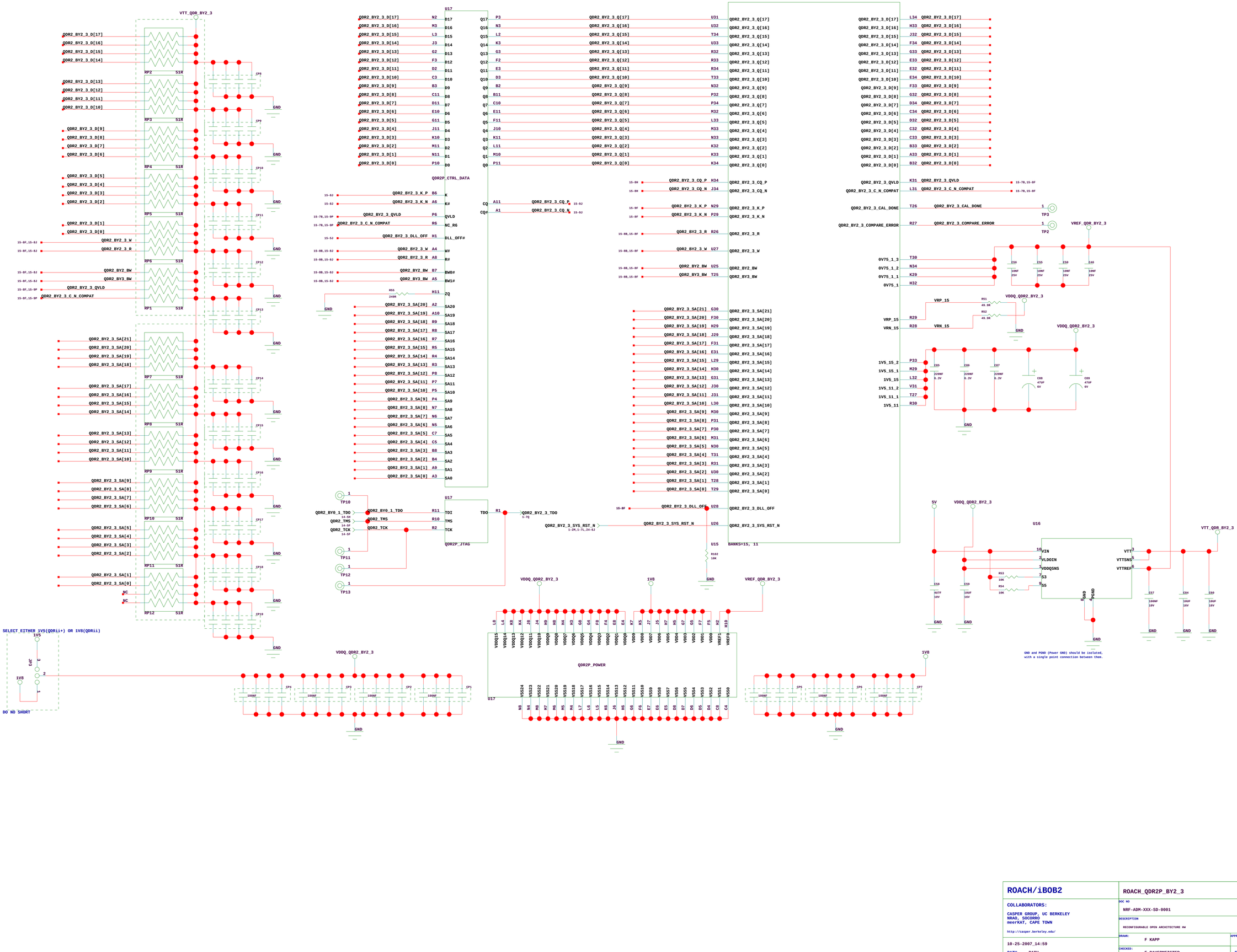
GPIOLVC18[4] IS DUAL FUNCTION:
1. DRIVES LED
2. CONTROLS DIRECTION ON GPIOLVC33[1-4]

IF CR18 IS ON, CLOCK CAPABLE GPIO'S ARE OUTPUTS

ROACH/iBOB2	ROACH_GPIO_MISC
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
10-25-2007_14:59 PATH PATH	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 13 OF 25



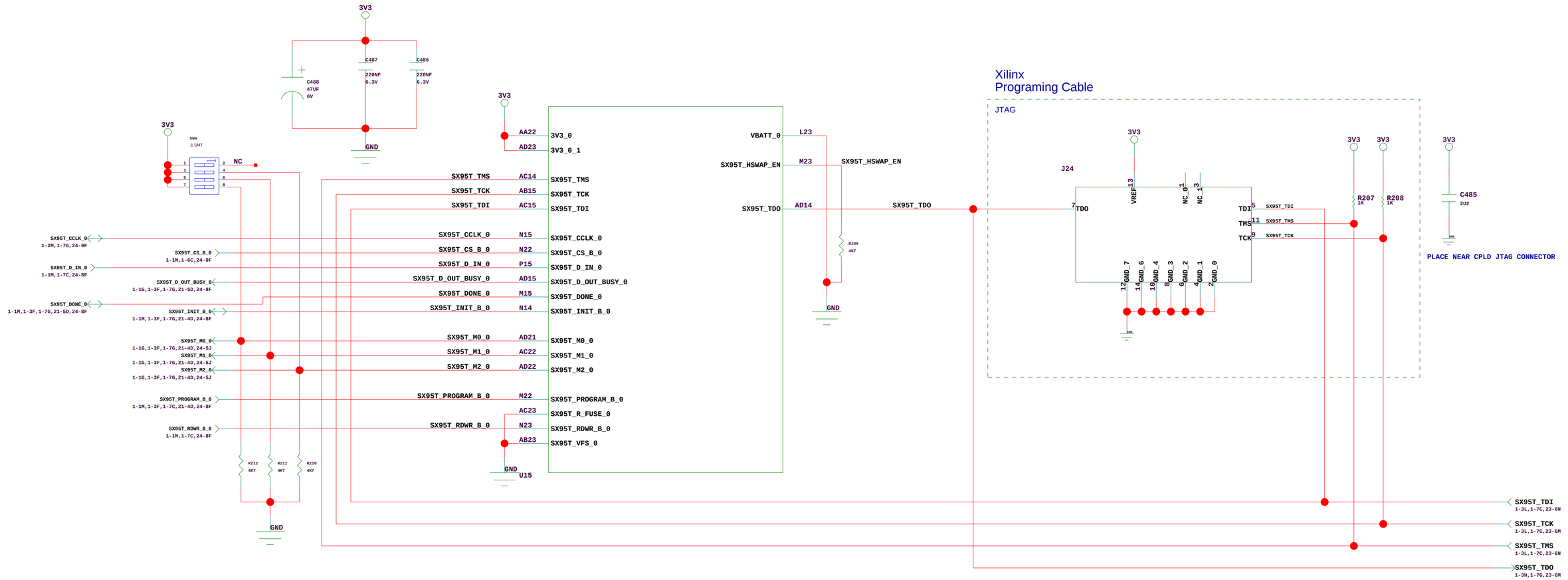
ROACH/iBOB2	ROACH_QDR2P_BY0_1
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-25-2007_14:59	DRAWN: F KAPP
PATH PATH	CHECKED: E BAUERMEISTER
	APPR:
	SHEET 14 OF 25



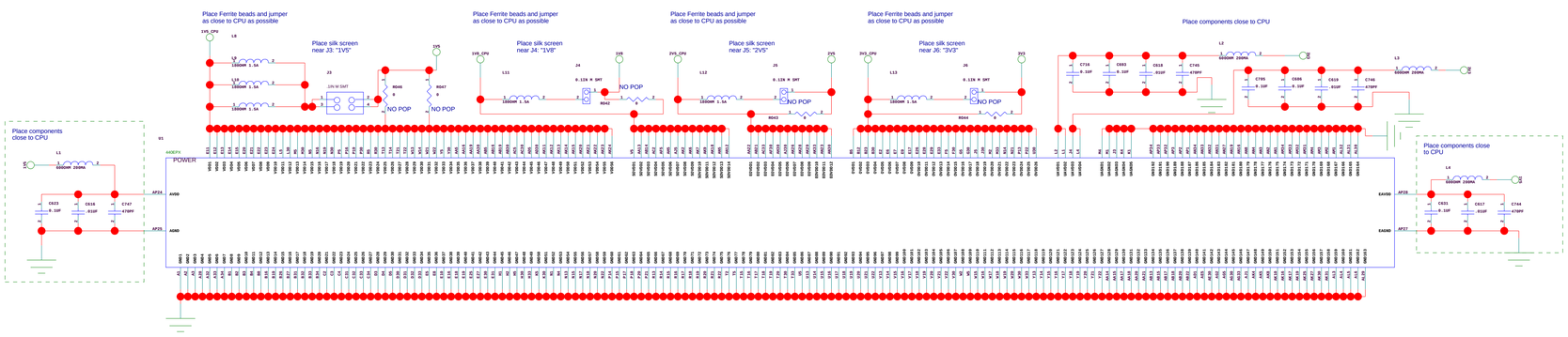
ROACH/iBOB2	**ROACH_QDR2P_BY2_3**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET: 15 OF 25
10-25-2007_14:59	
PATH PATH	

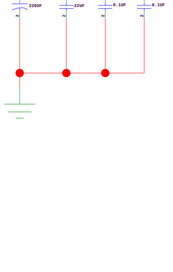
TBD

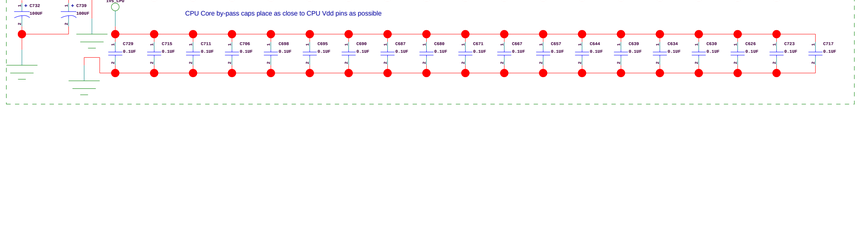
VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

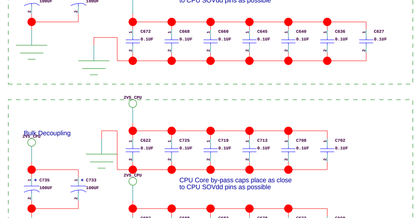


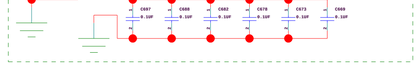
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
10-25-2007_14:59 PATH PATH	

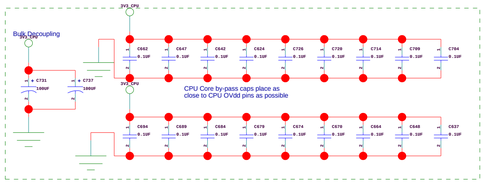


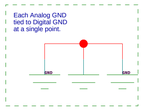










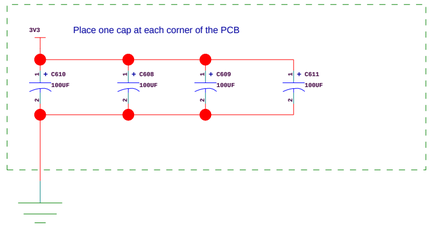


REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: **CASPER GROUP, UC BERKELEY** **NRAO, SOCORRO** **meerKAT, CAPE TOWN** http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 17 OF 25
10-25-2007_14:59 PATH PATH	

REMOVED 3V3 GENERATION



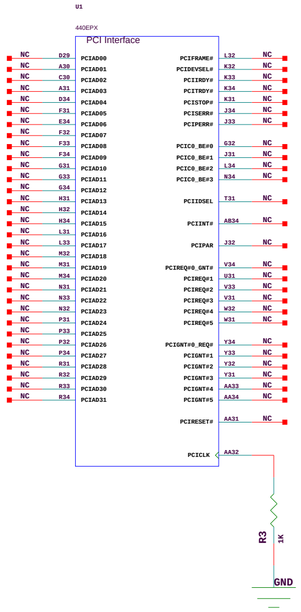
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

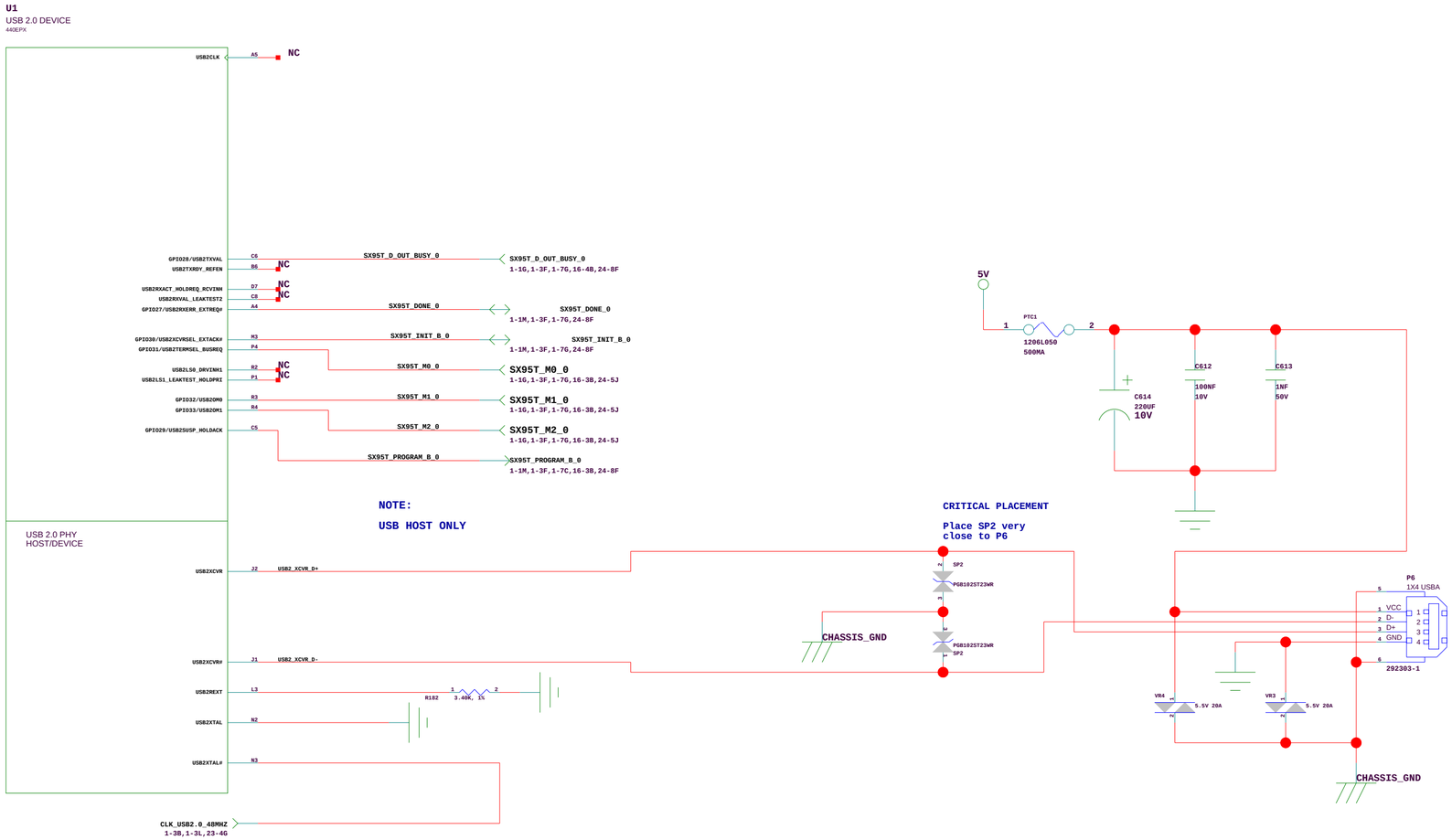
ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET: 18 OF 25
10-25-2007_14:59 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-25-2007_14:59 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

Place nearest PHY pin 96
Place nearest PHY pin 101
Place nearest PHY pin 98
Place nearest PHY pin 100
Place as close to PHY CORE VDD power pins as possible
Place as close to PHY IO VDD power pins as possible
UNUSED SECOND ETHERNET MAC
Gig-Ethernet RGMII1
Gig-Ethernet RGMII0
ETHERNET Mgt.
Place resistors as close to CPU as possible and keep all traces lengths equal
Place resistors close to PHY all trace lengths equal
Place components as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible.
Place decoupling C close to termination R. All traces 50Ohm WRT GND or 2V5
The RGMII signaling is 125 MHz using both rising and falling edges of the clock.
The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups.
Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.
CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30
Place jumers in line with signals
Ethernet LEDs
Top LED = SPEED/LINK
Green = 1000
Yellow = 100
Off = 10/100
Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY
HFJ11-1G02E-L12
CHASSIS_GND
DP83865DVH
NOSTUFF
DUPLEX LED
L10 LED
L100 LED
STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL
ROACH/iBOB2
COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/
10-25-2007_14:59
ROACH_PPC_ETH1
DOC NO
NRF-ADM-XXX-SD-0001
REVISION
A
DESCRIPTION
RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN:
F KAPP
CHECKED:
E BAUERMEISTER
SHEET
20 OF 25



ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 21 OF 25
10-25-2007_14:59 PATH PATH	

DDR_PA[15:0]

DDR_PD0[63:0]

U1

DDR SDRAM

64DEPX

DDR_PD0	AB2	MEMDATA00	
DDR_PD1	AF2	MEMDATA01	
DDR_PD2	AK5	MEMDATA02	
DDR_PD3	AL28	MEMDATA03	
DDR_PD4	AL22	MEMDATA04	
DDR_PD5	AK22	MEMDATA05	
DDR_PD6	AK21	MEMDATA06	
DDR_PD7	AP21	MEMDATA07	
DDR_PD8	AP28	MEMDATA08	
DDR_PD9	AL18	MEMDATA09	
DDR_PD10	AK17	MEMDATA10	
DDR_PD11	AP17	MEMDATA11	
DDR_PD12	AN28	MEMDATA12	
DDR_PD13	AP18	MEMDATA13	
DDR_PD14	AK18	MEMDATA14	
DDR_PD15	AP16	MEMDATA15	
DDR_PD16	AM16	MEMDATA16	
DDR_PD17	AP15	MEMDATA17	
DDR_PD18	AL15	MEMDATA18	
DDR_PD19	AP14	MEMDATA19	
DDR_PD20	AL17	MEMDATA20	
DDR_PD21	AM17	MEMDATA21	
DDR_PD22	AK15	MEMDATA22	
DDR_PD23	AM15	MEMDATA23	
DDR_PD24	AP13	MEMDATA24	
DDR_PD25	AK13	MEMDATA25	
DDR_PD26	AP12	MEMDATA26	
DDR_PD27	AL12	MEMDATA27	
DDR_PD28	AK14	MEMDATA28	
DDR_PD29	AK11	MEMDATA29	
DDR_PD30	AL13	MEMDATA30	
DDR_PD31	AM12	MEMDATA31	
DDR_PD32	AF3	MEMDATA32	
DDR_PD33	AF1	MEMDATA33	
DDR_PD34	AD4	MEMDATA34	
DDR_PD35	AD3	MEMDATA35	
DDR_PD36	AB3	MEMDATA36	
DDR_PD37	AF2	MEMDATA37	
DDR_PD38	AE2	MEMDATA38	
DDR_PD39	AE1	MEMDATA39	
DDR_PD40	AC3	MEMDATA40	
DDR_PD41	AC1	MEMDATA41	
DDR_PD42	AA4	MEMDATA42	
DDR_PD43	AA3	MEMDATA43	
DDR_PD44	AD2	MEMDATA44	
DDR_PD45	AC4	MEMDATA45	
DDR_PD46	AB1	MEMDATA46	
DDR_PD47	AB2	MEMDATA47	
DDR_PD48	Y3	MEMDATA48	
DDR_PD49	Y2	MEMDATA49	
DDR_PD50	Y4	MEMDATA50	
DDR_PD51	V3	MEMDATA51	
DDR_PD52	AA2	MEMDATA52	
DDR_PD53	AA1	MEMDATA53	
DDR_PD54	W3	MEMDATA54	
DDR_PD55	W1	MEMDATA55	
DDR_PD56	V1	MEMDATA56	
DDR_PD57	U2	MEMDATA57	
DDR_PD58	T4	MEMDATA58	
DDR_PD59	R1	MEMDATA59	
DDR_PD60	V5	MEMDATA60	
DDR_PD61	T5	MEMDATA61	
DDR_PD62	T3	MEMDATA62	
DDR_PD63	T2	MEMDATA63	

DDR_PA0	AM5	MEMADDR00	
DDR_PA1	AP4	MEMADDR01	
DDR_PA2	AP5	MEMADDR02	
DDR_PA3	AM6	MEMADDR03	
DDR_PA4	AP6	MEMADDR04	
DDR_PA5	AM7	MEMADDR05	
DDR_PA6	AL7	MEMADDR06	
DDR_PA7	AN7	MEMADDR07	
DDR_PA8	AM8	MEMADDR08	
DDR_PA9	AP7	MEMADDR09	
DDR_PA10	AL2	MEMADDR10	
DDR_PA11	AL8	MEMADDR11	
DDR_PA12	AN8	MEMADDR12	
DDR_PA13	AN4	MEMADDR13	
DDR_PBA0	AJ3	BA0	22-8K,22-8L
DDR_PBA1	AN3	BA1	22-8K,22-8L
DDR_PBA2	AP8	BA2	22-8K,22-8L
DDR_PRAS#	AJ4	RAS#	22-7K,22-7L
DDR_PCAS#	AN6	CAS#	22-7L,22-8K
DDR_PWE#	AJ2	WE#	22-3K,22-7L
DDR_PDM0	AL21	DM0	22-5K
DDR_PDM1	AP18	DM1	22-6K
DDR_PDM2	AP15	DM2	22-6K
DDR_PDM3	AL14	DM3	22-6K
DDR_PDM4	AD4	DM4	22-6K
DDR_PDM5	AB3	DM5	22-6K
DDR_PDM6	Y3	DM6	22-6K
DDR_PDM7	V3	DM7	22-6K
DDR_PDM8	AP10	DM8	22-6K
DDR_PODT0	AN3	MEMODT0	22-7L
DDR_PODT1	AN1	MEMODT1	22-6L
DDR_PCS0#	AN2	BANKSELA0	22-3K,22-7L
DDR_PCS1#	AM1	BANKSELA1	22-3K,22-7L
DDR_PCKE	AN9	MEMCLKEN	22-6K,22-7L
DDR_CLKOUT	AL1	MEMCLKOUT	
DDR_CLKOUT#	AM1	MEMCLKOUT#	

PPC_ECC0	AM11	ECC0	22-9F
PPC_ECC1	AL11	ECC1	22-9F
PPC_ECC2	AM9	ECC2	22-9F
PPC_ECC3	AL9	ECC3	22-10F
PPC_ECC4	AP11	ECC4	22-10F
PPC_ECC5	AN11	ECC5	22-10F
PPC_ECC6	AM10	ECC6	22-10F
PPC_ECC7	AP9	ECC7	22-10F

VREF	AF4	SVREF1A	
VREF	AL10	SVREF1B	
VREF	AF4	SVREF2A	
VREF	AL19	SVREF2B	

R012 22R 1%

R013 22R 1%

500ps Loop

DDR_VREF_0V9

1V8

C158 0.1UF

C148 0.1UF

C151 0.1UF 0402

C152 0.1UF 0402

C148 0.01UF

Place parts as close to CPU as possible

5V

1V8

U32

TPS51100DGQ

VIN	10		
VLDOIN	2		
VDDQSNS	1	VTT	3
S3	7	VTTSNS	5
S5	9	VTTREF	6
GND	8	PGND	4

R230 10K

R229 10K

R6 120R

C459 4U7F 10V

C456 10UF 16V

C453 100NF 10V

C21 22PF

C457 10UF 16V

C458 10UF 16V

DDR_VTT

DDR_VREF_0V9

GND

J8

PPC_ECC7	22-6D	168	DDR2_DIMM_CB7
PPC_ECC6	22-6D	167	DDR2_DIMM_CB6
PPC_ECC5	22-7D	162	DDR2_DIMM_CB5
PPC_ECC4	22-7D	161	DDR2_DIMM_CB4
PPC_ECC3	22-7D	49	DDR2_DIMM_CB3
PPC_ECC2	22-7D	48	DDR2_DIMM_CB2
PPC_ECC1	22-7D	43	DDR2_DIMM_CB1
PPC_ECC0	22-7D	42	DDR2_DIMM_CB0
DDR_PDQ63		236	DDR2_DIMM_DQ[63]
DDR_PDQ62		235	DDR2_DIMM_DQ[62]
DDR_PDQ61		230	DDR2_DIMM_DQ[61]
DDR_PDQ60		229	DDR2_DIMM_DQ[60]
DDR_PDQ59		117	DDR2_DIMM_DQ[59]
DDR_PDQ58		116	DDR2_DIMM_DQ[58]
DDR_PDQ57		111	DDR2_DIMM_DQ[57]
DDR_PDQ56		110	DDR2_DIMM_DQ[56]
DDR_PDQ55		227	DDR2_DIMM_DQ[55]
DDR_PDQ54		226	DDR2_DIMM_DQ[54]
DDR_PDQ53		218	DDR2_DIMM_DQ[53]
DDR_PDQ52		217	DDR2_DIMM_DQ[52]
DDR_PDQ51		108	DDR2_DIMM_DQ[51]
DDR_PDQ50		107	DDR2_DIMM_DQ[50]
DDR_PDQ49		99	DDR2_DIMM_DQ[49]
DDR_PDQ48		98	DDR2_DIMM_DQ[48]
DDR_PDQ47		215	DDR2_DIMM_DQ[47]
DDR_PDQ46		214	DDR2_DIMM_DQ[46]
DDR_PDQ45		209	DDR2_DIMM_DQ[45]
DDR_PDQ44		208	DDR2_DIMM_DQ[44]
DDR_PDQ43		96	DDR2_DIMM_DQ[43]
DDR_PDQ42		95	DDR2_DIMM_DQ[42]
DDR_PDQ41		90	DDR2_DIMM_DQ[41]
DDR_PDQ40		89	DDR2_DIMM_DQ[40]
DDR_PDQ39		206	DDR2_DIMM_DQ[39]
DDR_PDQ38		205	DDR2_DIMM_DQ[38]
DDR_PDQ37		200	DDR2_DIMM_DQ[37]
DDR_PDQ36		199	DDR2_DIMM_DQ[36]
DDR_PDQ35		87	DDR2_DIMM_DQ[35]
DDR_PDQ34		86	DDR2_DIMM_DQ[34]
DDR_PDQ33		81	DDR2_DIMM_DQ[33]
DDR_PDQ32		80	DDR2_DIMM_DQ[32]
DDR_PDQ31		159	DDR2_DIMM_DQ[31]
DDR_PDQ30		158	DDR2_DIMM_DQ[30]
DDR_PDQ29		153	DDR2_DIMM_DQ[29]
DDR_PDQ28		152	DDR2_DIMM_DQ[28]
DDR_PDQ27		40	DDR2_DIMM_DQ[27]
DDR_PDQ26		39	DDR2_DIMM_DQ[26]
DDR_PDQ25		34	DDR2_DIMM_DQ[25]
DDR_PDQ24		33	DDR2_DIMM_DQ[24]
DDR_PDQ23		150	DDR2_DIMM_DQ[23]
DDR_PDQ22		149	DDR2_DIMM_DQ[22]
DDR_PDQ21		144	DDR2_DIMM_DQ[21]
DDR_PDQ20		143	DDR2_DIMM_DQ[20]
DDR_PDQ19		31	DDR2_DIMM_DQ[19]
DDR_PDQ18		30	DDR2_DIMM_DQ[18]
DDR_PDQ17		25	DDR2_DIMM_DQ[17]
DDR_PDQ16		24	DDR2_DIMM_DQ[16]
DDR_PDQ15		141	DDR2_DIMM_DQ[15]
DDR_PDQ14		140	DDR2_DIMM_DQ[14]
DDR_PDQ13		132	DDR2_DIMM_DQ[13]
DDR_PDQ12		131	DDR2_DIMM_DQ[12]
DDR_PDQ11		22	DDR2_DIMM_DQ[11]
DDR_PDQ10		21	DDR2_DIMM_DQ[10]
DDR_PDQ9		13	DDR2_DIMM_DQ[9]
DDR_PDQ8		12	DDR2_DIMM_DQ[8]
DDR_PDQ7		129	DDR2_DIMM_DQ[7]
DDR_PDQ6		128	DDR2_DIMM_DQ[6]
DDR_PDQ5		123	DDR2_DIMM_DQ[5]
DDR_PDQ4		122	DDR2_DIMM_DQ[4]
DDR_PDQ3		10	DDR2_DIMM_DQ[3]
DDR_PDQ2		9	DDR2_DIMM_DQ[2]
DDR_PDQ1		4	DDR2_DIMM_DQ[1]
DDR_PDQ0		3	DDR2_DIMM_DQ[0]
		101	DDR2_DIMM_SA2
		240	DDR2_DIMM_SA1
		239	DDR2_DIMM_SA0
		120	DDR2_DIMM_SCL
		119	DDR2_DIMM_SDA

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1V8

R228 4K7

R227 4K7

PPC_DDR2_DIMM_SCL

PPC_DDR2_DIMM_SDA

GND

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	
DDR2_DIMM_BA[2]	54	DDR_PBA1	22-8L,22-9D
DDR2_DIMM_BA[1]	190	DDR_PBA2	22-8L,22-9D
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-8L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D
DDR2_DIMM_CK_P[2]	220	NC	
DDR2_DIMM_CK_N[2]	221	NC	
DDR2_DIMM_CK_P[1]	137	NC	
DDR2_DIMM_CK_N[1]	138	NC	
DDR2_DIMM_CK_P[0]	185	DDR_CLKOUT	
DDR2_DIMM_CK_N[0]	186	DDR_CLKOUT#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-7L,22-8D
DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-9D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D
DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	
DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	
DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D
ERR_OUT	55	PPC_DDR2_ERROR	1
PAR_IN	68	PAR_IN	1

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R226 4K7

PPC_DDR2_RESET_N

1-2B,1-2M,24-5J

C455 5PF 50V

TP4

TP5

GND

VTT VOLTAGE WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

DDR_VTT

DDR_PA15	RP24	CP26
DDR_PA14		
DDR_PA13		
DDR_PA12		
DDR_PA11	RP23	CP28
DDR_PA10		
DDR_PA9		
DDR_PA8		
DDR_PA7	RP22	CP29
DDR_PA6		
DDR_PA5		
DDR_PA4		
DDR_PA3	RP21	CP30
DDR_PA2		
DDR_PA1		
DDR_PA0		
22-8K,22-9D	RP25	CP32
22-8K,22-9D		
22-8K,22-9D		
22-8K,22-9D		
22-7K,22-9D	RP26	CP31
22-6K,22-8D		
22-3K,22-9D		
22-3K,22-8D		
22-3K,22-8D	RP19	CP33
22-8D		
22-8D		
NC		

GND

J8

VSS_64	237	69	VDD_5
VSS_63	234	67	VDD_4
VSS_62	231	64	VDD_3
VSS_61	228	59	VDD_2
VSS_60	225	53	VDD_1
VSS_59	222		
VSS_58	219		
VSS_57	216		
VSS_56	213		
VSS_55	210		
VSS_54	207		
VSS_53	204		
VSS_52	201		
VSS_51	198		
VSS_50	169		
VSS_49	166		
VSS_48	163		
VSS_47	160		
VSS_46	157		
VSS_45	154		
VSS_44	151		
VSS_43	148		
VSS_42	145		
VSS_41	142		
VSS_40	139		
VSS_39	136		
VSS_38	133		
VSS_37	130		
VSS_36	127		
VSS_35	124		
VSS_34	121		
VSS_33	118		
VSS_32	115		
VSS_31	112		
VSS_30	109		
VSS_29	106		
VSS_28	103		
VSS_27	100		
VSS_26	97		
VSS_25	94		
VSS_24	91		
VSS_23	88		
VSS_22	85		
VSS_21	82		
VSS_20	79		
VSS_19	66		
VSS_18	65		
VSS_17	50		
VSS_16	47		
VSS_15	44		
VSS_14	41		
VSS_13	38		
VSS_12	35		
VSS_11	32		
VSS_10	29		
VSS_9	26		
VSS_8	23		
VSS_7	20		
VSS_6	17		
VSS_5	14		
VSS_4	11		
VSS_3	8		
VSS_2	5		
VSS_1	2		

VREF	1		
VDDSPD	238		
VDD_11	197	VDDQ_11	194
VDD_10	189	VDDQ_10	191
VDD_9	187	VDDQ_9	181
VDD_8	184	VDDQ_8	175
VDD_7	178	VDDQ_7	170
VDD_6	172	VDDQ_6	78
VDD_5	69	VDDQ_5	75
VDD_4	67	VDDQ_4	72
VDD_3	64	VDDQ_3	62
VDD_2	59	VDDQ_2	56
VDD_1	53	VDDQ_1	51

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DDR_VREF_0V9

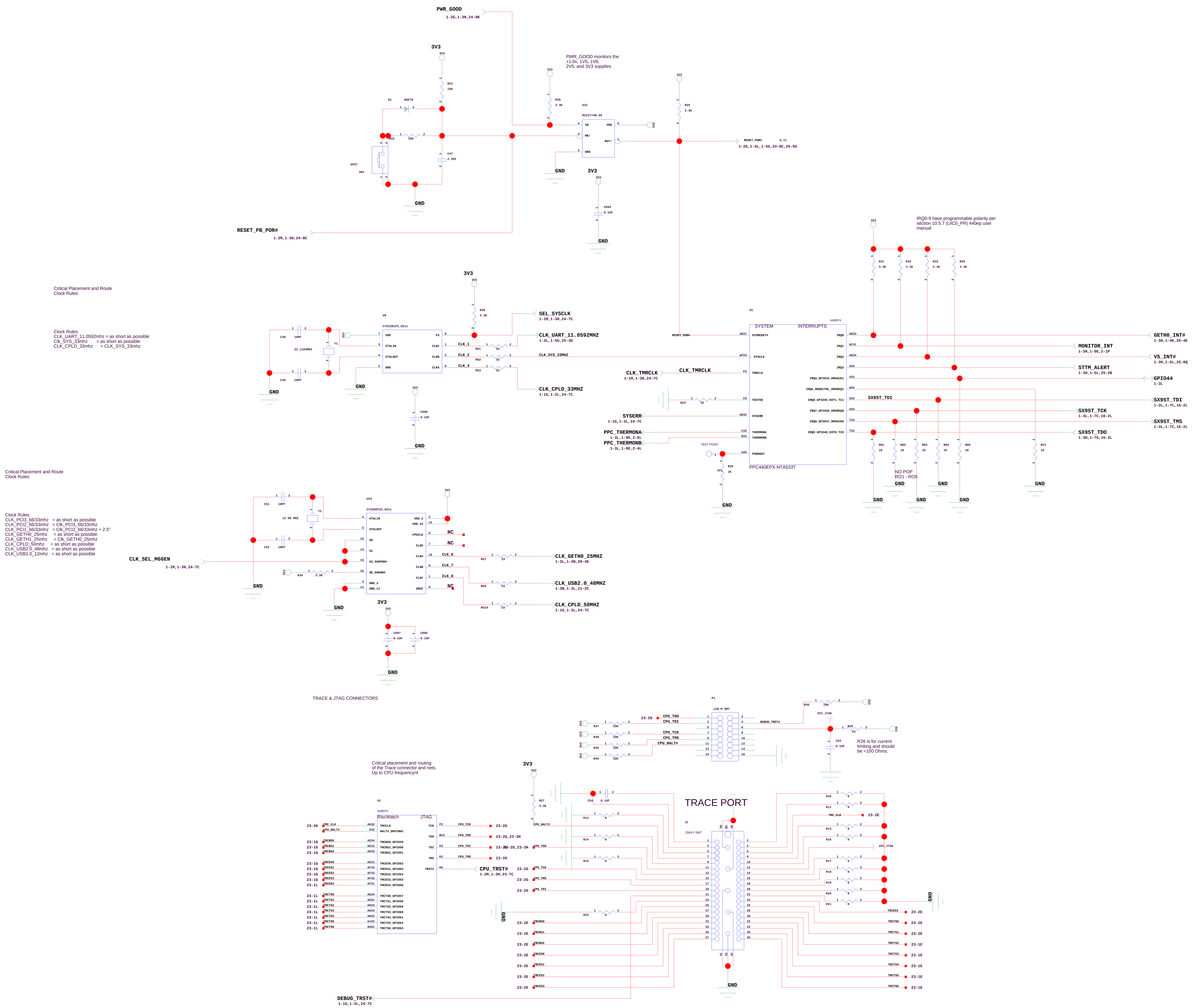
1V8

GND

PLACE NEAREST DDR2 MODULE PINS

C432	100NF 10V	C433	10NF 25V
C454	100NF 10V	C434	10NF 25V
C430	100NF 10V	C443	10NF 25V
C431	100NF 10V	C444	10NF 25V
C436	100NF 10V	C445	10NF 25V
C435	100NF 10V	C446	10NF 25V
C438	100NF 10V	C451	10NF 25V
C437	100NF 10V	C452	10NF 25V
C439	100NF 10V	C449	10NF 25V
C440	100NF 10V	C450	10NF 25V
C441	100NF 10V	C448	10NF 25V
C442	100NF 10V	C447	10NF 25V

ROACH/iBOB2	ROACH_PPC_DDR2
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN	DOC NO: NRF-ADM-XXX-SD-0001
http://casper.berkeley.edu/	REVISION: A
10-25-2007_14:59	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
PATH PATH	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 22 OF 25


PWR_GOOD
PWR_GOOD monitors the +1.0v, 1V5, 1V8, 2V5, and 3V3 supplies
RESET_PB_POR#
Critical Placement and Route Clock Rules:
Clock Rules:
CLK_UART_11.0592mhz = as short as possible
Clk_SYS_33mhz = as short as possible
CLK_CPLD_33mhz = CLK_SYS_33mhz
SEL_SYSCLK
CLK_UART_11.0592MHZ
CLK_CPLD_33MHZ
CLK_TMRCLK
SYSERR
PPC_THERMONA
PPC_THERMONB
IRQ0-9 have programmable polarity per section 10.5.7 (UIC0_PR) 440ep user manual
PPC440EPX-NTA533T
GETH0_INT#
MONITOR_INT
V5_INT#
STTM_ALERT
GPIO44
SX95T_TDI
SX95T_TCK
SX95T_TMS
SX95T_TDO
NO POP RO1 - RO5
Critical Placement and Route Clock Rules:
Clock Rules:
CLK_PCI3_66/33mhz = as short as possible
CLK_PCI2_66/33mhz = Clk_PCI3_66/33mhz
CLK_PCI1_66/33mhz = Clk_PCI2_66/33mhz + 2.5"
CLK_GETH0_25mhz = as short as possible
CLK_GETH1_25mhz = Clk_GETH0_25mhz
CLK_CPLD_50mhz = as short as possible
CLK_USB2.0_48mhz = as short as possible
CLK_USB2.0_12mhz = as short as possible
CLK_SEL_M66EN
CLK_GETH0_25MHZ
CLK_USB2.0_48MHZ
CLK_CPLD_50MHZ
TRACE & JTAG CONNECTORS
R26 is for current limiting and should be <100 Ohms.
Critical placement and routing of the Trace connector and nets. Up to CPU frequency/4
TRACE PORT
CPU_TRST#
DEBUG_TRST#

ROACH/iBOB2	ROACH_PPC_TST_CLK_IO	
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO NRF-ADM-XXX-SD-0001 DESCRIPTION RECONFIGURABLE OPEN ARCHITECTURE HW	REVISION A
10-25-2007_14:59 PATH PATH	DRAWN: F KAPP CHECKED: E BAUERMEISTER	APPR: SHEET 23 OF 25

Memory Bus

PAD#[27:31]
1-2G,1-4L,25-10B

PADATA[0:7]
1-2M,1-4L

U54

roach_cpld_XC2C256_7VQ100C_pcb

PADD27	4	PAD4
PADD28	7	PAD8
PADD29	9	PAD10
PADD30	10	PAD12
PADD31	11	PAD15
PDATA0	12	PAD16
PDATA1	13	PAD17
PDATA2	14	PAD18
PDATA3	15	PAD19
PDATA4	16	PAD20
PDATA5	17	PAD21
PDATA6	18	PAD23
PDATA7	19	PAD28
NC	20	PAD29
NC	21	PAD30
NC	22	PAD31
NC	23	PAD32
NC	24	PAD33
NC	25	PAD34
NC	26	PAD35
	28	PAD44
SELECTMAP_CS 1-2G,1-5L,25-7B	30	PAD48
PCS_2 1-1G,1-4L,25-7B	31	PAD49
PDS0 1-1G,1-5L,25-5G,25-7B,25-7M,25-10B	32	PAD50
PR_WE 1-1G,1-4L,25-5G,26-6M,d5-7B,25-9B	33	PAD52
PWRE_B# 1-2G,1-4L,25-6M,25-7B,25-9B	34	PAD54
RESET_PDN# 1-2G,1-3L,1-5G,23-9J,25-5G	35	PAD55
RESET_PB_PDN# 1-2M,1-3H,23-8E	38	PAD59
PPC_RESET 1-2G,1-9E,2-2R	40	PAD64
DEBUG_TRST# 1-1G,1-3L,23-1F	41	PAD65
CPU_TRST# 1-2M,1-3M,23-2F	42	PAD66
CLK_CPLD_33MHZ 1-1G,1-2L,23-6G	43	PAD67
CLK_CPLD_33MHZ 1-1G,1-3L,23-4G	44	PAD68
CLK_PXICLK 1-1G,1-4L,25-6F	45	PAD69
CLK_TMSCLK 1-1M,1-3H,23-6H	46	PAD70
CLK_SEL_PXIEN# 1-1M,1-3H,23-5D	48	PAD73
SEL_SYSCLK 1-1M,1-3H,23-7G	49	PAD74
SYSEN# 1-1G,1-3L,23-8H	50	PAD75
FPS_BSY 1-1G,1-4L,25-7J	51	PAD76
PAPG# 1-1M,1-4G,25-8J	52	PAD77
EE1_WP 1-2M,1-5L,25-1A	53	PAD81
EE2_BOOT_WP 1-2M,1-4G,25-5A	54	PAD82
ETTM_ASC 1-2M,1-5G,25-1B	56	PAD86
SYS_CONFIG0	57	PAD87
SYS_CONFIG1	58	PAD88
SYS_CONFIG2	59	PAD89
SYS_CONFIG3	60	PAD90
SYS_CONFIG4	61	PAD95
SYS_CONFIG5	64	PAD100
SYS_CONFIG6	66	PAD102
GETH0_RST# 1-2M,1-4B,20-4E	68	PAD105
NC	69	PAD107
NC	70	PAD108
	71	PAD109
RESET_CPLD# 1-1M,1-4G,25-3J	74	PAD112
PER_CCLK_EN#	75	PAD113
	76	PAD114
	77	PAD115
	78	PAD117
	80	PAD118
	79	PAD119
	82	PAD120
	81	PAD121
	83	PAD125
	85	PAD131
	86	PAD132
	87	PAD133
	88	PAD134
	91	PAD137
	92	PAD138
	94	PAD142
	95	PAD143
	96	PAD144
	97	PAD145
	98	PAD146
	100	PAD152
	101	PAD154
	102	PAD156
	103	PAD158
	104	PAD160
	105	PAD161
	106	PAD162
	107	PAD163
	110	PAD166
	111	PAD167
	112	PAD168
	113	PAD169
	116	PAD175
	117	PAD176
	118	PAD177
	119	PAD178
	120	PAD186
	121	PAD187
	124	PAD190
	125	PAD191
	126	PAD192
	128	PAD194
	129	PAD195
	130	PAD196
	131	PAD197
	132	PAD199
	133	PAD204
	134	PAD206
	136	PAD207
	137	PAD208
	138	PAD211
	139	PAD212
	140	PAD213
	142	PAD214
	143	PAD217

XC2C256_7VQ100C

RESETS

CPU_TRST# = '1' when JTAG_TRST# = '1' and RESET_PDN# = '1' else '0';
see errata sheet

CLOCKS

STATUS / MISC

FLASH

I2C

ETHERNET

SYS_CONFIG[6:7]
1-2G,1-9E,2-2R

SYS_CONFIG[6:7]

ENABLE PER_CLK CONNECTION
TO CONFIGURATION I/F
MUST CO-ORDINATE WITH
SX95T_CCLK_0 AND MODE
TO AVOID CLASH

SN74AHC1G125DCKT

PER_CCLK_EN#
CLK_PERCLK
SX95T_CCLK_0
U2

R135 10K

C13 100NF 10V

U54

roach_cpld_XC2C256_7VQ100C_powerpins

VCC	1
VAUX	8
VCCIO_3	27
VCC_1	37
VCCIO_4	55
VCCIO_5	73
VCC_2	84
VCCIO_6	93
VCCIO	109
VCCIO_1	127
VCCIO_2	141
GND_3	29
GND_4	36
GND_5	47
GND_6	62
GND_7	72
GND_8	89
GND_9	99
GND_10	108
GND_1	123
GND_2	144

XC2C256_7VQ100C

PLACE NEAR CPLD POWER PINS

C473	100NF 10V
C474	100NF 10V
C475	100NF 10V
C476	100NF 10V
C477	100NF 10V
C478	100NF 10V
C479	100NF 10V
C480	100NF 10V
C481	100NF 10V
C482	100NF 10V
C483	100NF 10V

User DIP-Swith

USER_DIP0	142
USER_DIP1	140
USER_DIP2	139
USER_DIP3	138

R198 10K
R194 10K
R195 10K
R196 10K
SW2 4POLE

USER_LED0 129
USER_LED1 128
SYSERR# 126
RESET_BUFPOR# 125

R200 10K
R201 10K
R202 10K
R203 10K
CR2 GRN
CR4 GRN
CR5 GRN
CR6 GRN
CR5
RED
RED

SysErr will be used to drive Status LED (active H)

R197 330
R199 330
CR1 GRN
CR2 GRN
5V_VIN
3V3
U35
74LVC1G66
VCC
GND
C615 0.1 CAP 0402
PWR_GOOD 1-2G,1-3H,23-10G

SX95T_CCLK_0 1-2M,1-7G
SX95T_CS_B_0 1-1M,1-9C,16-4B
SX95T_D_IN_0 1-1M,1-7C,16-4A
SX95T_D_OUT_BUSY_0 1-1G,1-3F,1-7G,16-4B,21-5D
SX95T_DONE_0 1-1M,1-3F,1-7G,21-5D
SX95T_INIT_B_0 1-1M,1-3F,1-7G,21-4D
SX95T_PROGRAM_B_0 1-1M,1-3F,1-7C,16-3B,21-4D
SX95T_RDWR_B_0 1-1M,1-7C,16-3B

CMD/DI 115
CLK/SCLK 114

J17

CMD/DI	10	DAT0/DO	2
CLK/SCLK	6	DAT1	1
VDD	7	DAT2	13
VSS1	8	DAT3	12
VSS2	4	DAT4	11
SD_CD_COM	14	DAT5	9
SD_WP_COM	15	DAT6	5
		DAT7	3
		MNT1	16 NC
		MNT2	17 NC

GMC050064SEU

SD/MMC/MMCPLUS CONNECTOR

QDR2_BY0_1_SYS_RST_N 1-1M,1-8L,14-5J
QDR2_BY2_3_SYS_RST_N 1-2M,1-7L,15-5J
PPC_DDR2_RESET_N 1-2G,1-2M,22-2B
EXT_RESET# 1-2G,1-4L,25-6F

SX95T_M0_0 1-1G,1-3F,1-7G,16-3B,21-4D
SX95T_M1_0 1-1G,1-3F,1-7G,16-3B,21-4D
SX95T_M2_0 1-1G,1-3F,1-7G,16-3B,21-4D

Boot Configuration

1-1G,1-5G,25-3B

R204 10K
R205 10K
R206 10K
SW3 4POLE

Configuration DIP-Swith

Place SW2 on bottom side of PCB
Include silkscreen text:
"FACTORY SET DO NOT CHANGE"

BOOT STRAP PINS:
UART0_CTS = Boot_CFG0
UART0_DSR = Boot_CFG1
UART0_DCD = Boot_CFG2
Default = Bootstrap option C (Boot_CFG[2:0] = 010)

BOOT_CFG0 1-1M,1-4G,25-1J
BOOT_CFG1 1-1M,1-4G,25-1J
BOOT_CFG2 1-1M,1-4G,25-1J

3V3 RD10 10K
3V3 RD11 10K
3V3 RD14 10K

U54

roach_cpld_XC2C256_7VQ100C_configpins

NC	2	PAD1
NC	3	PAD3
NC	5	PAD5
NC	6	PAD7
NC	39	PAD62
	63	TDI
	65	TMS
	67	TCK
	122	TDO
NC	143	PAD218

XC2C256_7VQ100C

Xilinx
Programing Cable

JTAG

J22

VREF	13
NC_0	8
NC_1	14
TDO	7
TDI	5
TMS	11
TCK	9
GND_7	12
GND_6	10
GND_4	8
GND_3	6
GND_2	4
GND_1	2
GND_0	1

3V3
R193 1K
R192 1K

3V3
C484 20Z

PLACE NEAR CPLD JTAG CONNECTOR

ROACH/iBOB2	ROACH_PPC_CPLD
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
10-25-2007_14:59 PATH PATH	DRAWN: F KAPP; APPR:
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ROACH/iBOB2

ROACH_PPC_NVM_SERIAL

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

CHECKED: E BAUERMEISTER

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PATH PATH

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