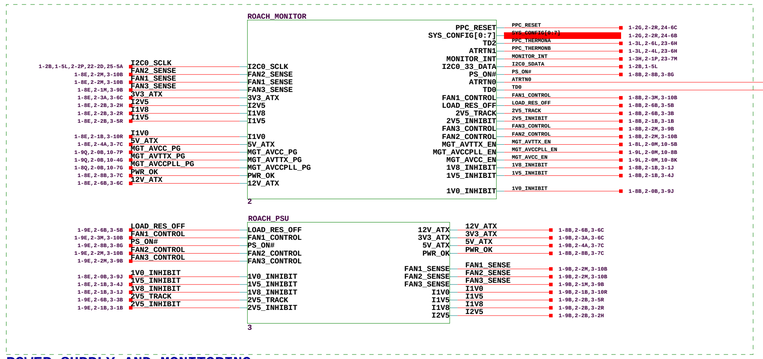
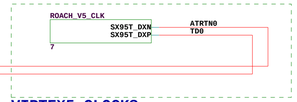
VIRTEX5

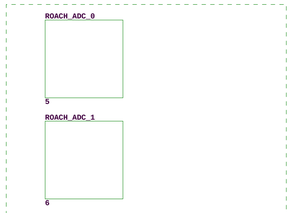
POWER SUPPLY AND MONITORING



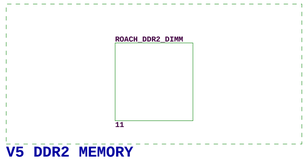
VIRTEX5 CLOCKS



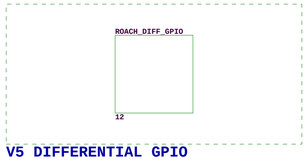
ZDOK/ADC INTERFACE



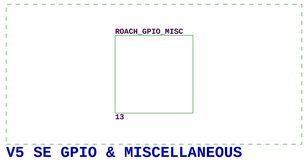
V5 DDR2 MEMORY



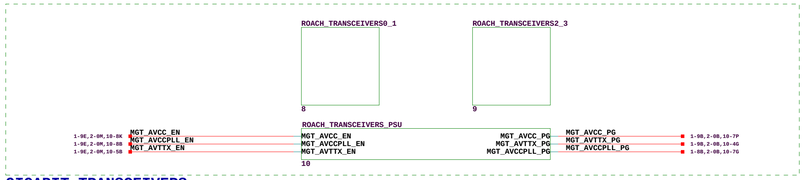
V5 DIFFERENTIAL GPIO



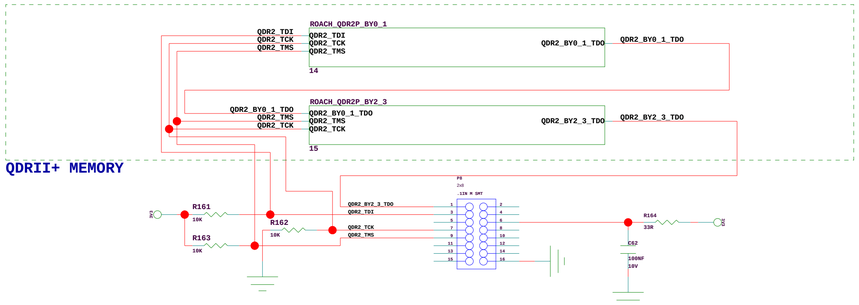
V5 SE GPIO & MISCELLANEOUS



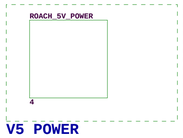
GIGABIT TRANSCEIVERS



QDRII+ MEMORY



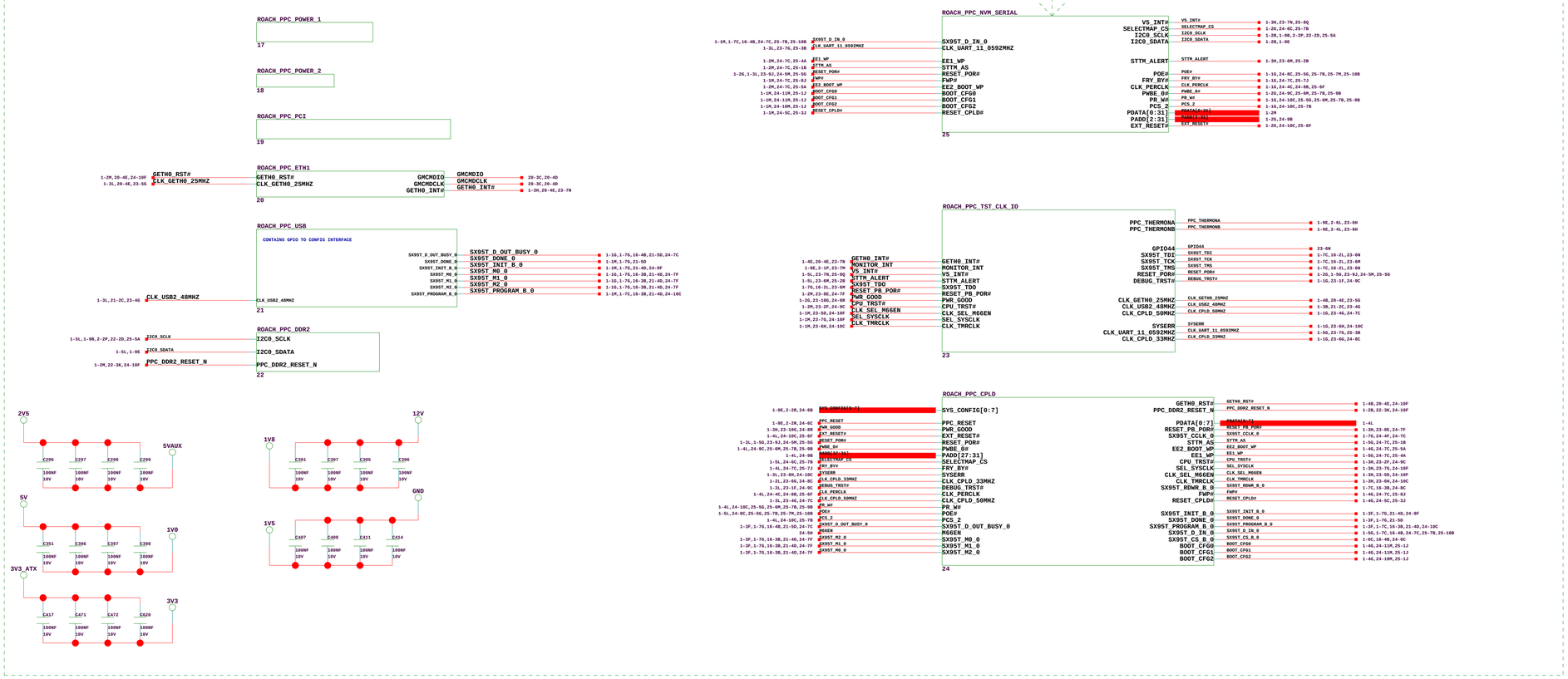
V5 POWER



VIRTEX5 CONFIGURATION

V5 SE GPIO & MISCELLANEOUS

PPC



MECHANICAL

BOARD FIDUCIALS

LOGO'S

PLACEHOLDER FOR PCB
MEERKAT LOGO

PLACEHOLDER FOR PCB
CASPER LOGO

PLACEHOLDER FOR PCB
ROACH LOGO

PLACEHOLDER FOR PCB
NRAO LOGO

BOARD SERIAL NUMBER

CONTRIBUTORS

ETIENNE BAUERMEISTER
HENRY CHEN
STEVE DURAND
FRANCOIS KAPP
ALAN LANGMAN
GEORGE PECK
MIKE REVNELL
HAYDEN SO
DAN WERTHIMER

ROACH/iBOB2

COLLABORATORS:

CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN

http://casper.berkeley.edu/

6-10-2008_15:47

PATH PATH

ROACH_TOP

DOC NO: NRF-ADM-XXX-SD-0001

REVISION: A

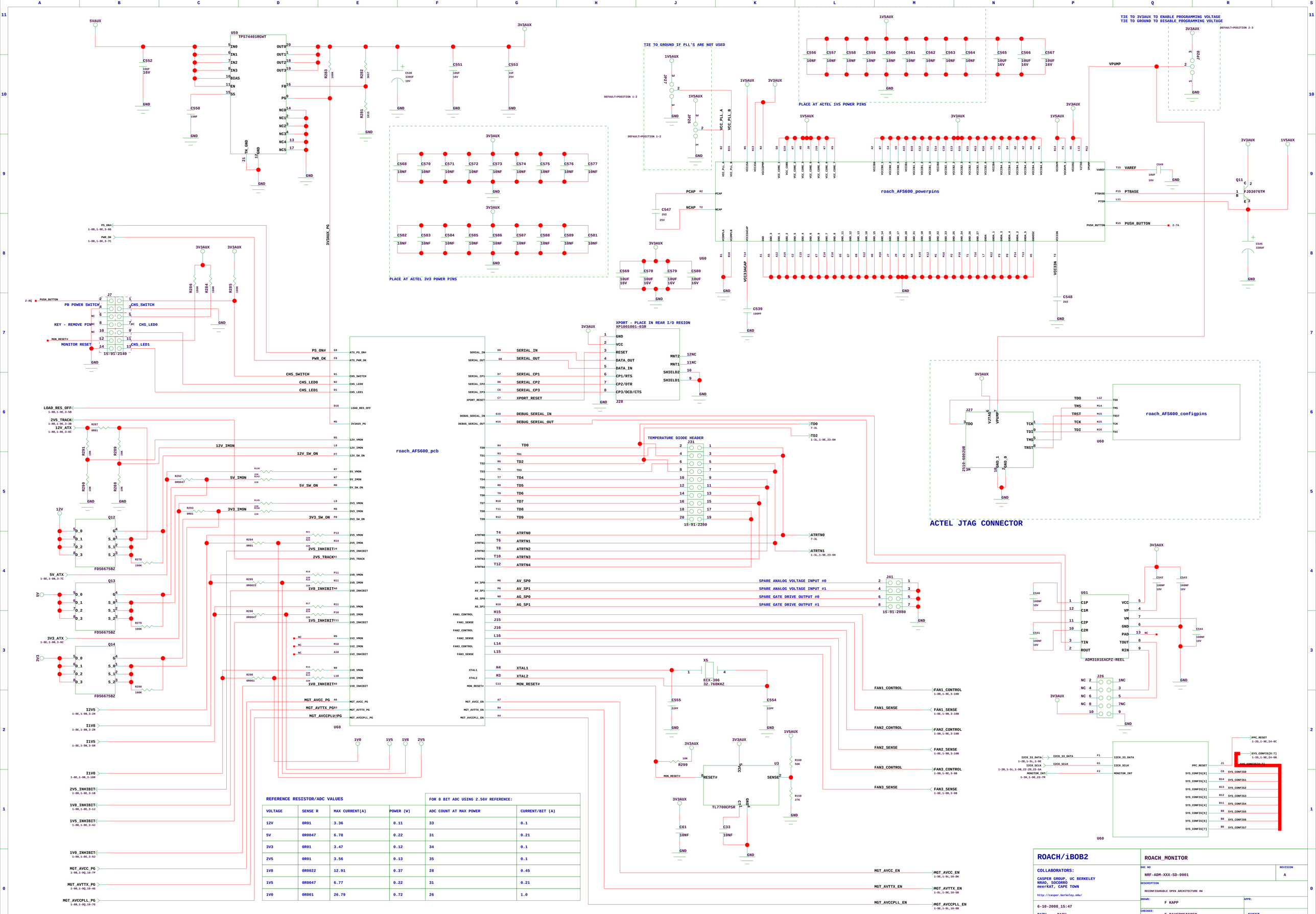
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW

DRAWN: F KAPP

APPR:

CHECKED: E BAUERMEISTER

SHEET 1 OF 25



REFERENCE RESISTOR/ADC VALUES

VOLTAGE	SENSE R	MAX CURRENT(A)	POWER (W)	FOR 8 BIT ADC USING 2.56V REFERENCE: ADC COUNT AT MAX POWER	CURRENT/BIT (A)
12V	0R01	3.36	0.11	33	0.1
5V	0R0047	6.78	0.22	31	0.21
3V3	0R01	3.47	0.12	34	0.1
2V5	0R01	3.56	0.13	35	0.1
1V8	0R0022	12.91	0.37	28	0.45
1V5	0R0047	6.77	0.22	31	0.21
1V0	0R001	26.79	0.72	26	1.0

ROACH/iBOB2

COLLABORATORS:
CASPER GROUP, UC BERKELEY
NRAO, SOCORRO
meerKAT, CAPE TOWN
http://casper.berkeley.edu/

6-10-2008_15:47
PATH PATH

ROACH_MONITOR

DOC NO: NRF-ADM-XXX-SD-0001
REVISION: A
DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
DRAWN: F KAPP
APPR:
CHECKED: E BAUERMEISTER
SHEET 2 OF 25

AUX FAN CONNECTORS - ATX 4 PIN

J21
1 GND
2 12V
3 SENSE
4 CONTROL
47053-1000

FAN1_SENSE 1-8E,1-9B,2-2B
FAN1_CONTROL 1-8B,1-9E,2-2M
FAN1_SENSE
FAN1_CONTROL
PLACE ON SILKSCREEN: FAN1

J20
1 GND
2 12V
3 SENSE
4 CONTROL
47053-1000

FAN2_SENSE 1-8E,1-9B,2-2M
FAN2_CONTROL 1-8B,1-9E,2-2M
FAN2_SENSE
FAN2_CONTROL
PLACE ON SILKSCREEN: FAN2

J19
1 GND
2 12V
3 SENSE
4 CONTROL
47053-1000

FAN3_SENSE 1-8E,1-9B,2-1K
FAN3_CONTROL 1-8B,1-9E,2-2H
FAN3_SENSE
FAN3_CONTROL
PLACE ON SILKSCREEN: FAN3

GND

ATX POWER CONNECTORS

5VAUX
N12V

J18
1 3V3_1
2 3V3_2
3 COM_1
4 5V_1
5 COM_2
6 5V_2
7 COM_3
8 PWR_OK
9 5VSB
10 12V1_1
11 12V1_2
12 3V3_3
13 3V3_4
14 _12V
15 COM_4
16 PS_ON#
17 COM_5
18 COM_6
19 COM_7
20 NC
21 5V_3
22 5V_4
23 5V_5
24 COM_8
44206-0007

PS_ON# 1-8B,1-9E,2-8B
PWR_OK 1-8B,1-8E,2-8B
PWR_OK
5VAUX
PS_ON#

J32
2 4 6 8 10
1 3 5 7 9
8510-4500PL

5V_ATX 1-8E,1-9B,2-4A
3V3_ATX 1-8E,1-9B,2-3A
12V_ATX 1-8B,1-8E,2-6B

GND

LOAD RESISTORS FOR ATX PSU MIN LOAD
SWITCH OFF ONCE LOAD EXCEEDS MINIMUM SPEC
ADJUST RESISTOR VALUES FOR ACTUAL SUPPLY

BOARD LAYOUT NOTE
SEPARATE GROUND RETURN CURRENTS FROM MAIN BOARD GROUND PLANES
BETWEEN POWER INPUT CONNECTORS AND REGULATOR AREA ON BOARD.

5VAUX
R180 10K
Q9 NDS331N
R185 10R 5W AC05000001009JL800
Q8 BSS138
Q10 NDS331N
R187 56R 5W AC05000005609JL800
LOAD_RES_OFF 1-8B,1-9E,2-6B
R181 10K
GND

30A SMPS MODULE

1V0
ROUTE FROM LOAD
R13 22R
PLACE RESISTOR CLOSE TO U50
ROUTE SHORTEST
R144 6R

PSU INPUT SUMMARY

VOLTAGE	5.0V +- 10%
CURRENT (MAX)	6.0A

5V
L6 BLM31PG121SN1B
L5 BLM31PG121SN1B
L16 BLM31PG121SN1B
C403 330UF 16V
C401 330UF 16V
C419 22UF 16V
GND

U50
13 TURBOTRANS
10 SENSE+
2 VI_1
6 VI_0
1 INHIBIT/UVLADJ
14 TRACK
11 SENSE-
PTH05T210WAD

1V5
1V0_INHIBIT 1-8B,1-8E,2-6B
Q4 BSS138
ROUTE FROM LOAD

4 GND_3
7 GND_2
8 GND_1
3 GND_0

VO_0 5
VO_1 9
VOADJUST 12
R143 634R
DIRECT TO P8 ON U50, DEDICATED TRACE

C418 10UF
C117 10UF
C402 1000UF 2V5
C400 1000UF 2V5
C104 1000UF 2V5
C105 1000UF 2V5
I1V0 1-8E,1-9B,2-1B

PSU RAIL SUMMARY

VOLTAGE	1.0V +- 5%
SUPPLIES	FPGA CORE
CURRENT (QUIESCENT)	1.5A
CURRENT (ACTIVE)	26.8A
LOAD STEP	25.3A

1.2V SUPPLY DELETED - NOT REQUIRED

16A SMPS MODULE

1V5
ROUTE FROM LOAD
R12 22R
PLACE RESISTOR CLOSE TO US1
ROUTE SHORTEST
R146 243R

PSU INPUT SUMMARY

VOLTAGE	12V +- 10%
CURRENT (MAX)	0.8A

12V
L7 BLM31PG121SN1B
C404 330UF 16V
C420 22UF 16V
GND

U51
9 TURBOTRANS
6 SENSE+
2 VI
11 INHIBIT/UVLADJ
10 TRACK
7 SENSE-
1 SMARTSYNC
PTH08T240WAD

1V8
1V5_INHIBIT 1-8B,1-8E,2-1B
Q5 BSS138
ROUTE FROM LOAD

4 GND_1
3 GND_0

VO 5
VOADJUST 8
R147 649R
DIRECT TO P8 ON US1, DEDICATED TRACE

C421 10UF
C405 1000UF 2V5
I1V5 1-8E,1-9B,2-2B

PSU RAIL SUMMARY

VOLTAGE	1.5V +- 5%
SUPPLIES	FPGA IO, QDR, PPC
CURRENT (QUIESCENT)	0.25A
CURRENT (ACTIVE)	6.8A
LOAD STEP	6.55A

16A SMPS MODULE

2V5
ROUTE FROM LOAD
R10 22R
PLACE RESISTOR CLOSE TO U53
ROUTE SHORTEST
R177 845R

PSU INPUT SUMMARY

VOLTAGE	12V +- 10%
CURRENT (MAX)	0.8A

2V5_TRACK 1-8B,1-9E,2-6B
R183 1K
C426 10UF
12V
L15 BLM31PG121SN1B
C412 330UF 16V
C424 22UF 16V
GND

U53
8 TURBOTRANS
5 SENSE+
2 VI
10 INHIBIT/UVLADJ
9 TRACK
6 SENSE-
1 SMARTSYNC
PTH08T230WAD

2V5_INHIBIT 1-8B,1-9E,2-1B
Q7 BSS138
ROUTE FROM LOAD

VO 4
VOADJUST 7
R179 2K87
C425 10UF 16V
C413 680UF 4V
I2V5 1-8E,1-9B,2-2B
DIRECT TO P8 ON U53, DEDICATED TRACE

PSU RAIL SUMMARY

VOLTAGE	2.5V +- 5%
SUPPLIES	FPGA, ZDOK PPC, PHY
CURRENT (QUIESCENT)	0.1A
CURRENT (ACTIVE)	3.6A
LOAD STEP	3.5A

16A SMPS MODULE

1V8
ROUTE FROM LOAD
R11 22R
PLACE RESISTOR CLOSE TO U52
ROUTE SHORTEST
R149 243R

PSU INPUT SUMMARY

VOLTAGE	12V +- 10%
CURRENT (MAX)	1.8A

12V
L14 BLM31PG121SN1B
C409 330UF 16V
C423 22UF 16V
GND

U27
9 TURBOTRANS
6 SENSE+
2 VI
11 INHIBIT/UVLADJ
10 TRACK
7 SENSE-
1 SMARTSYNC
PTH08T220WAD

2V5
1V8_INHIBIT 1-8B,1-8E,2-1B
Q6 BSS138
ROUTE FROM LOAD

4 GND_1
3 GND_0

VO 5
VOADJUST 8
R148 487R
DIRECT TO P8 ON PTH08T210W, DEDICATED TRACE

C422 10UF
C410 1000UF 2V5
I1V8 1-8E,1-9B,2-2B

PSU RAIL SUMMARY

VOLTAGE	1.8V +- 5%
SUPPLIES	FPGA IO, DDR2 x 2
CURRENT (QUIESCENT)	1A
CURRENT (ACTIVE)	12.9A
LOAD STEP	11.9A

ROACH/iBOB2	ROACH_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
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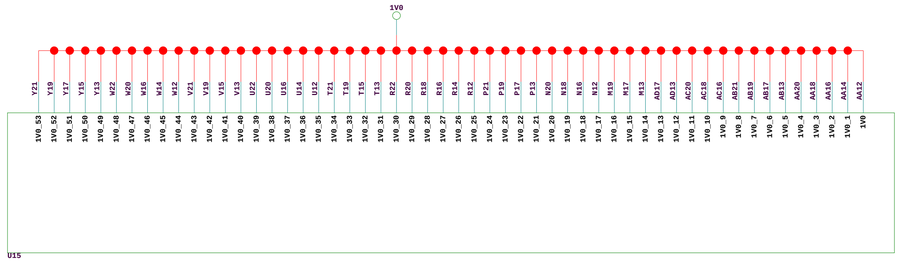

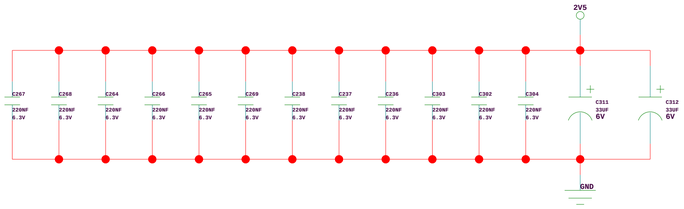

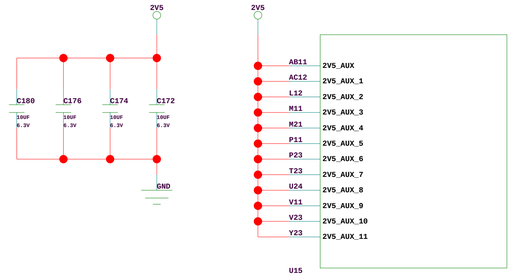

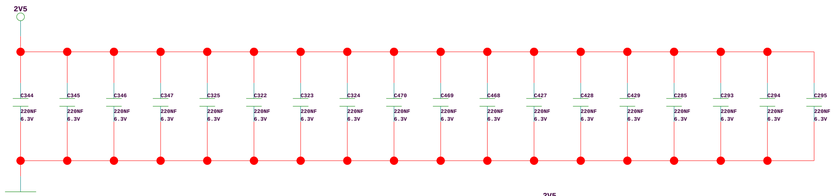

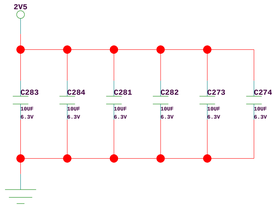

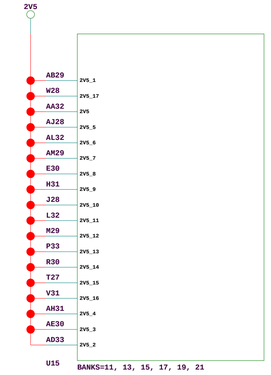

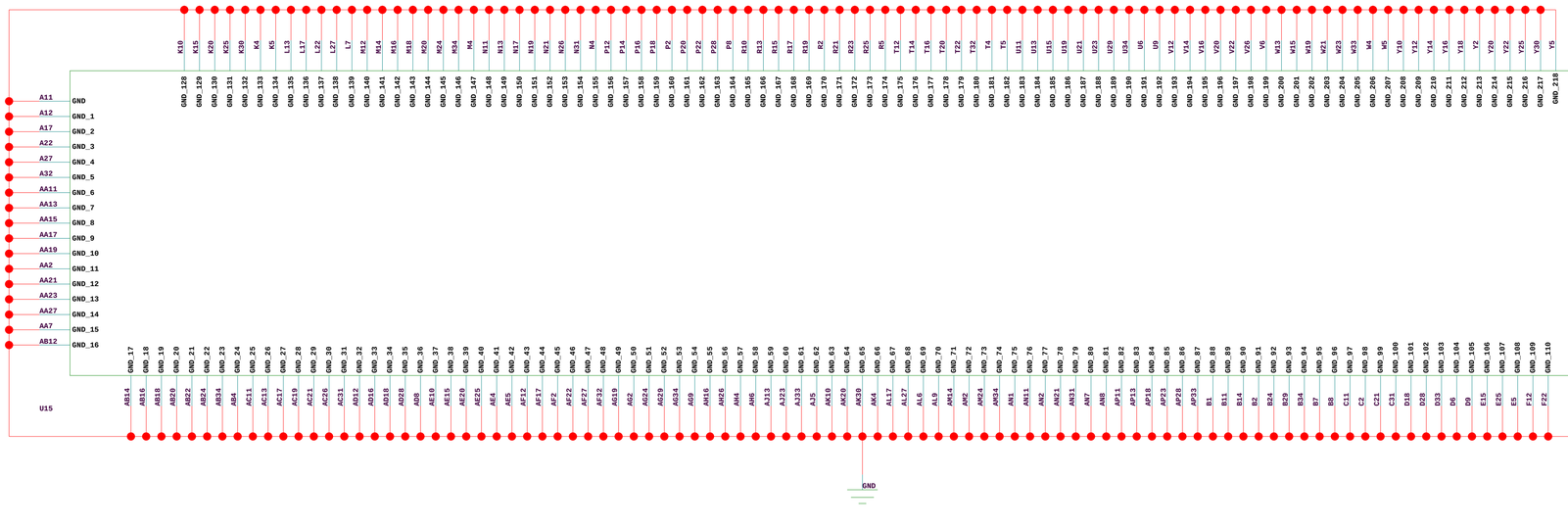

ROACH/iBOB2	**ROACH_5V_POWER**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 4 OF 25
6-10-2008_15:47 PATH PATH	

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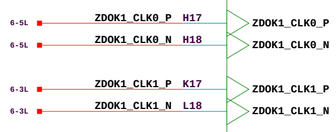
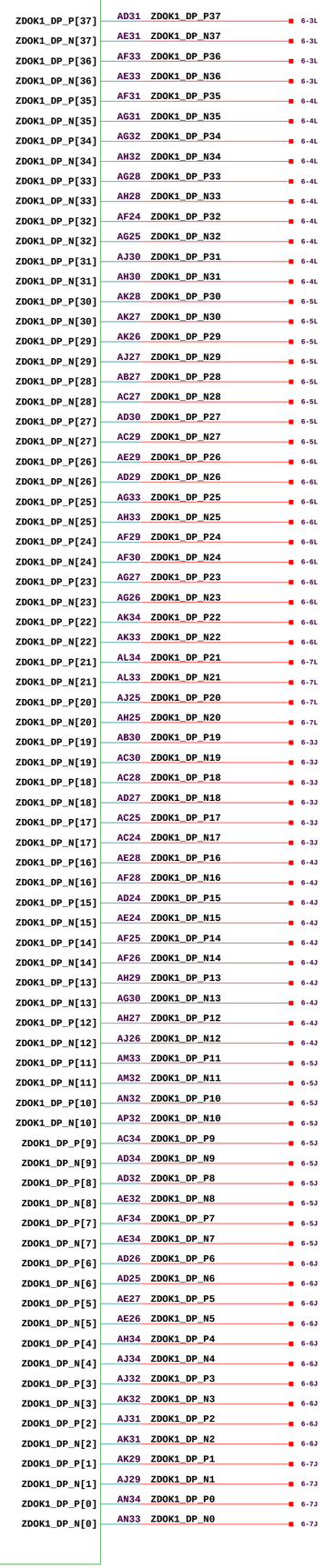
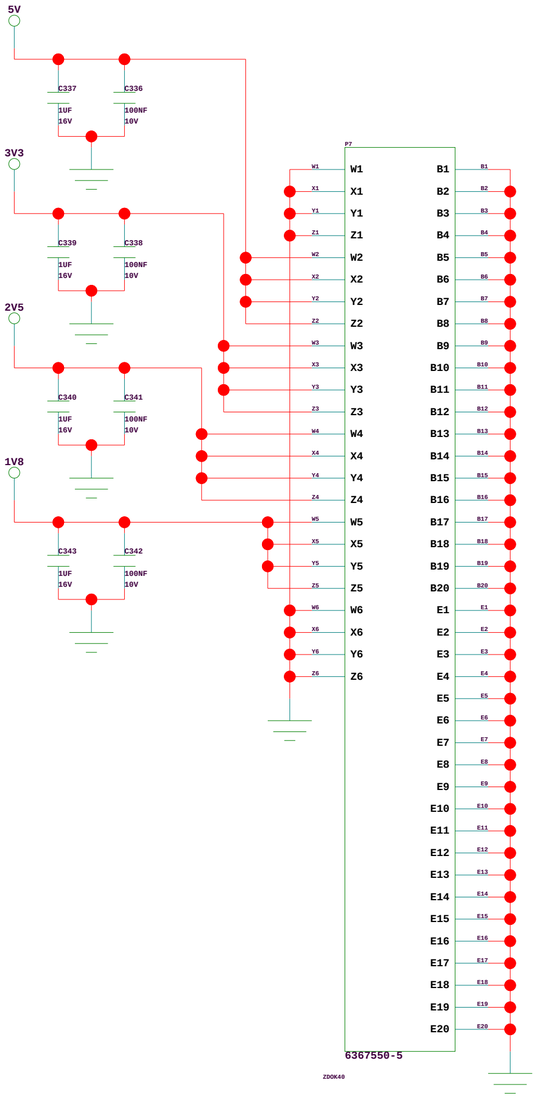
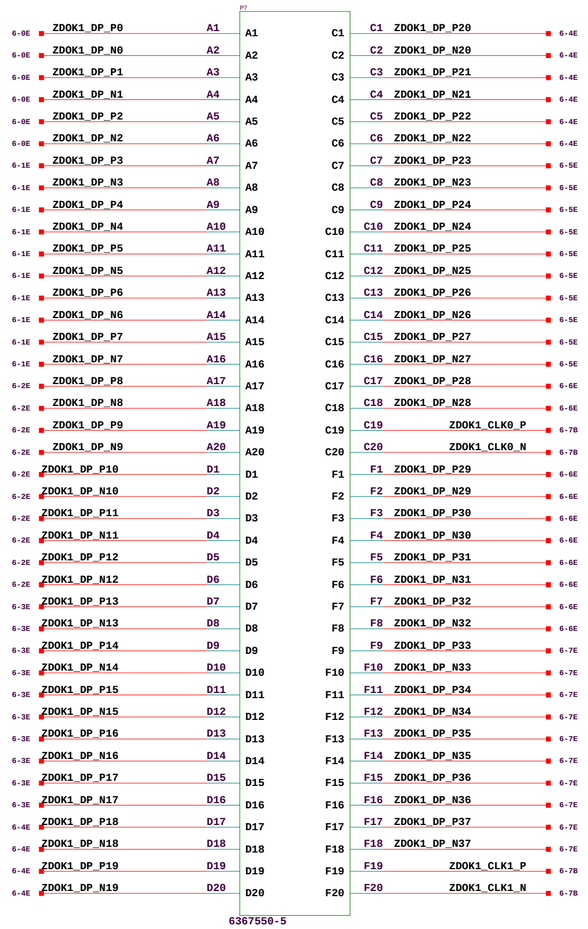




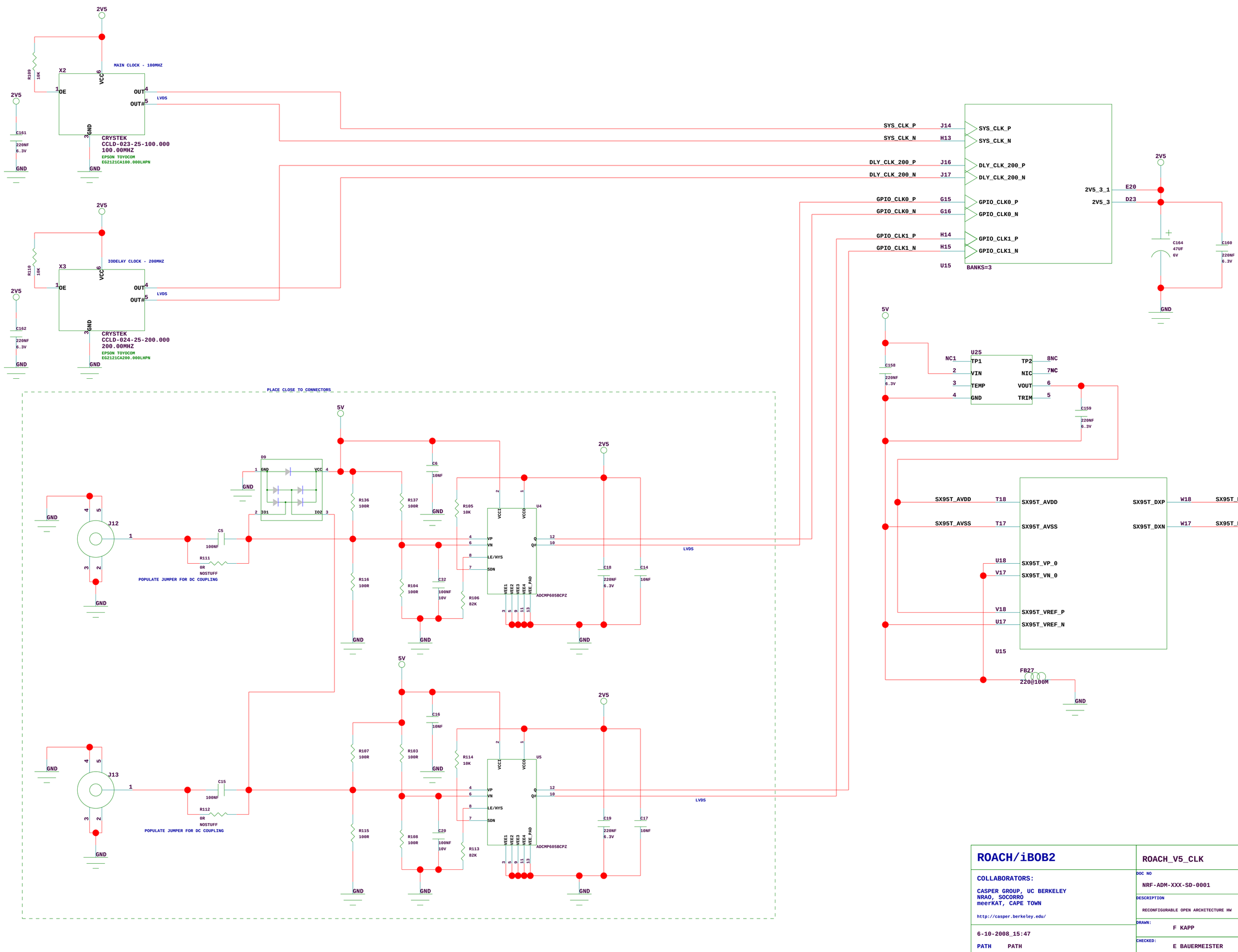
U15

BANKS=11, 13, 15, 17, 19, 21





ROACH/iBOB2	**ROACH_ADC_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 6 OF 25
6-10-2008_15:47 PATH PATH	



ROACH/iBOB2	**ROACH_V5_CLK**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 7 OF 25
6-10-2008_15:47 PATH PATH	

ROACH/iBOB2	**ROACH_TRANSCEIVERS0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001
	REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-10-2008_15:47	DRAWN: F KAPP
PATH	APPR:
	CHECKED: E BAUERMEISTER
	SHEET 8 OF 25

MGTRREF FOR ENTIRE DEVICE
SWAP MGTRREF CONNECTION TO
CLOSEST MGTVTTTX PIN DURING PLACEMENT

PLACEMENT: CLOSEST TO FPGA PIN

HIGH-SPEED DIFFERENTIAL VIAS

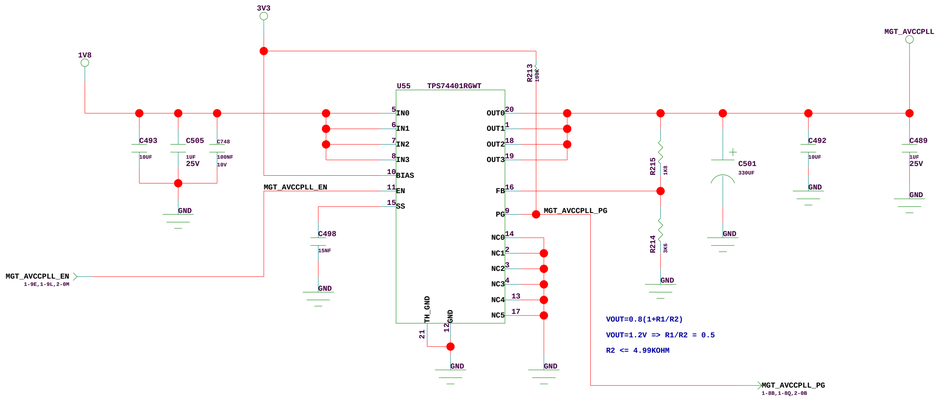
G4 AND G8 CONNECTED IN 2X2 MODULE

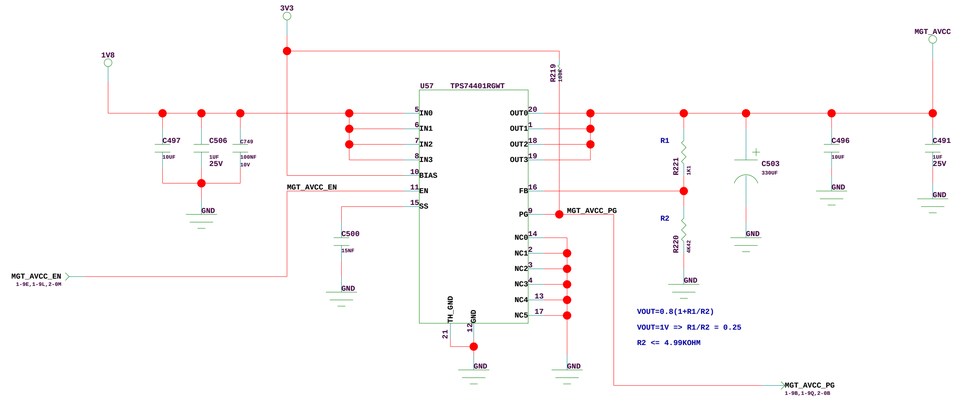
OPTICAL MODULE FAULT - RED LED

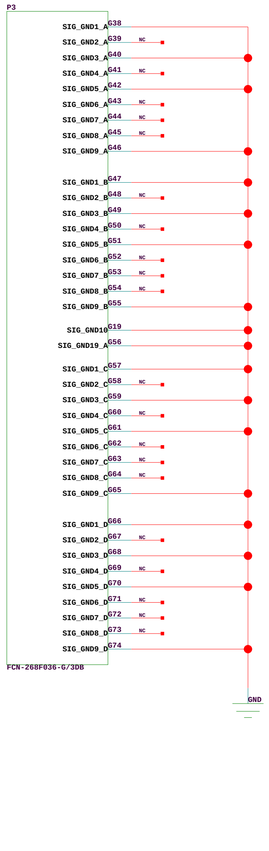
CCLD-023-25-156.250 156.25MHZ

FCN-268F036-G/3DB

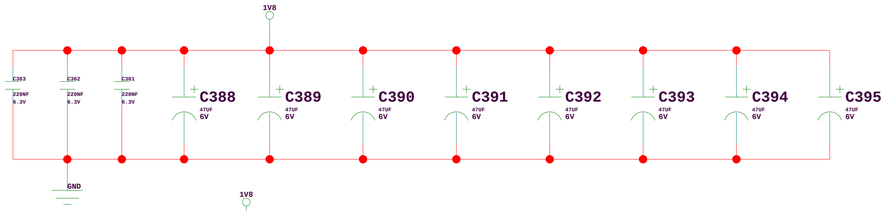
ROACH/iBOB2	ROACH_TRANSCEIVERS2_3
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-10-2008_15:47	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 9 OF 25

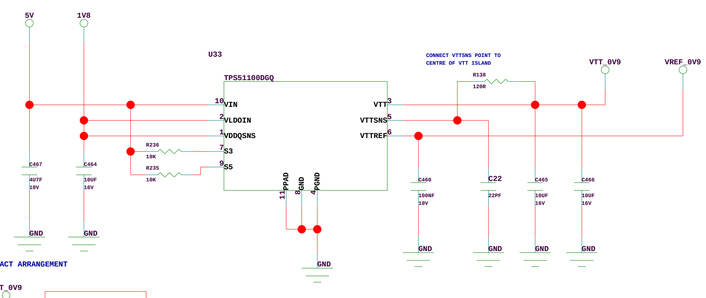




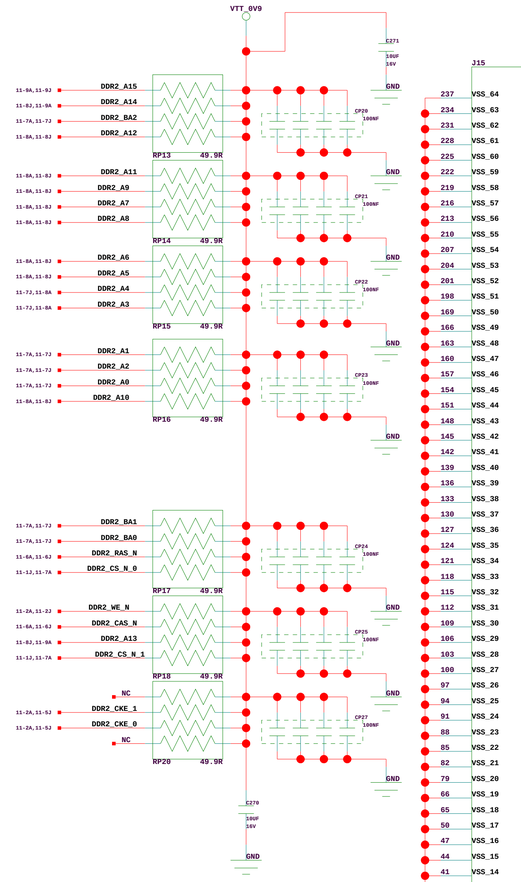


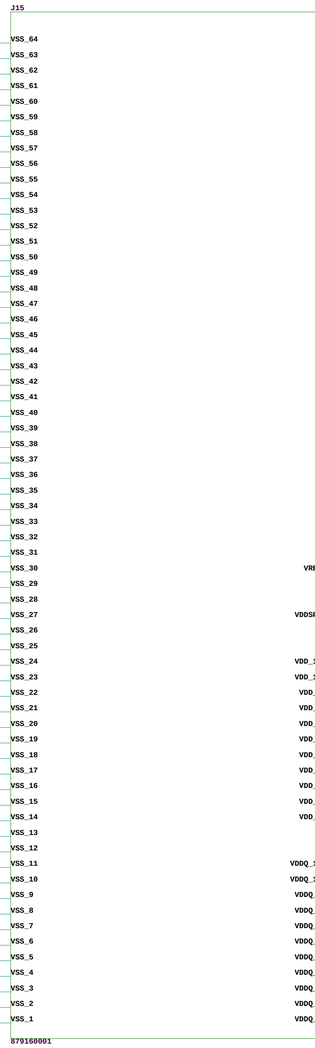
ROACH/iBOB2	ROACH_TRANSCEIVERS_PSU
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-10-2008_15:47	DRAWN: F KAPP · APPR:
PATH PATH	CHECKED: E BAUERMEISTER · SHEET 10 OF 25



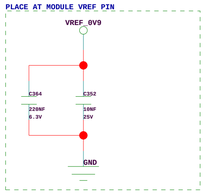


VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT
PLACE ONE 10uF CAPACITOR ON EITHER END OF ISLAND

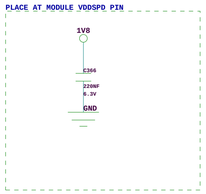




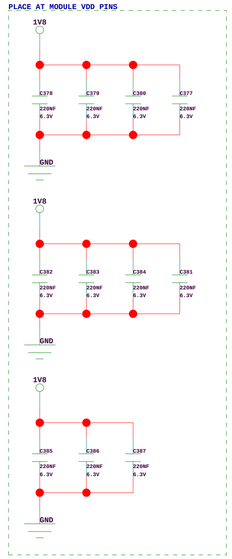
PLACE AT MODULE VREF PIN

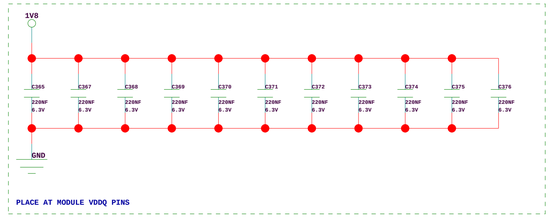


PLACE AT MODULE VDDSPD PIN

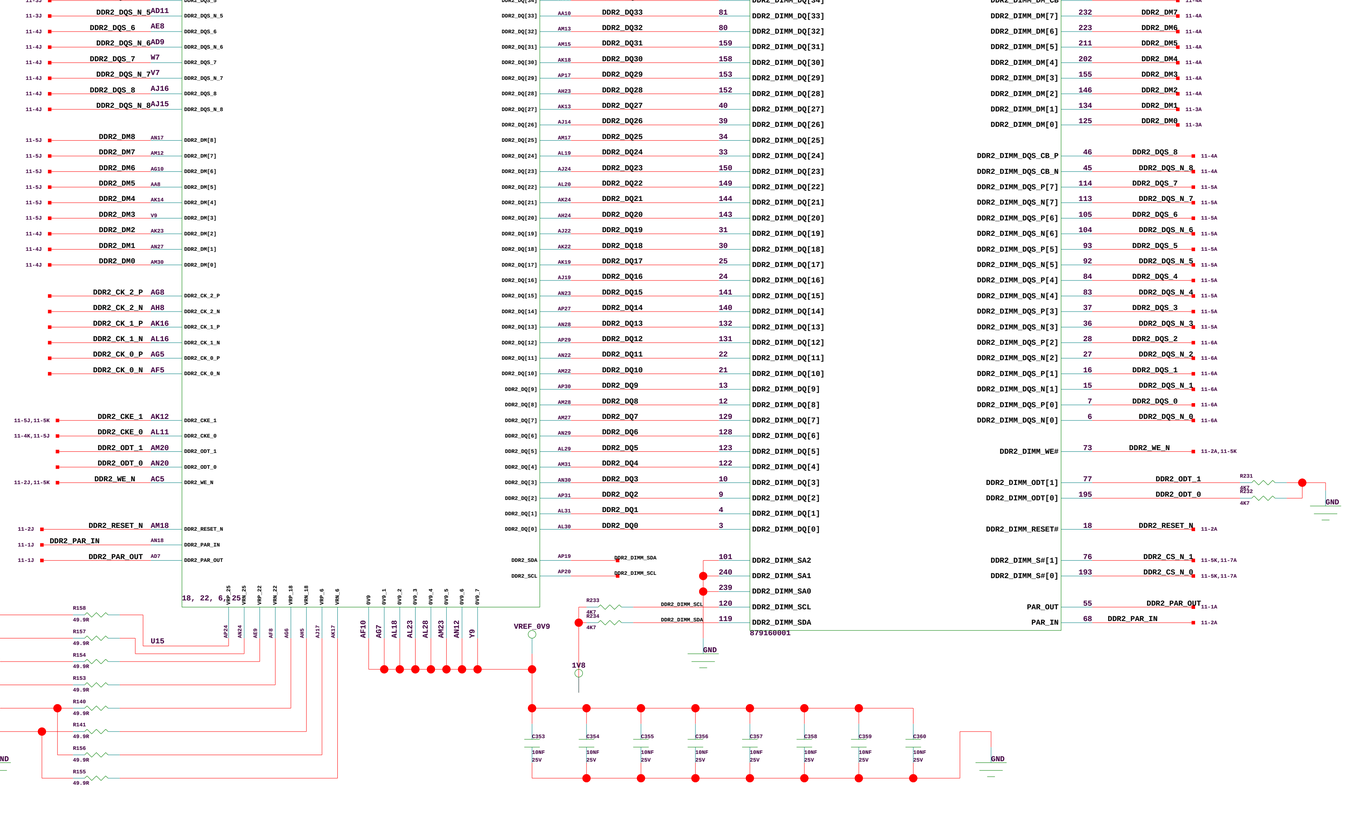


PLACE AT MODULE VDD PINS

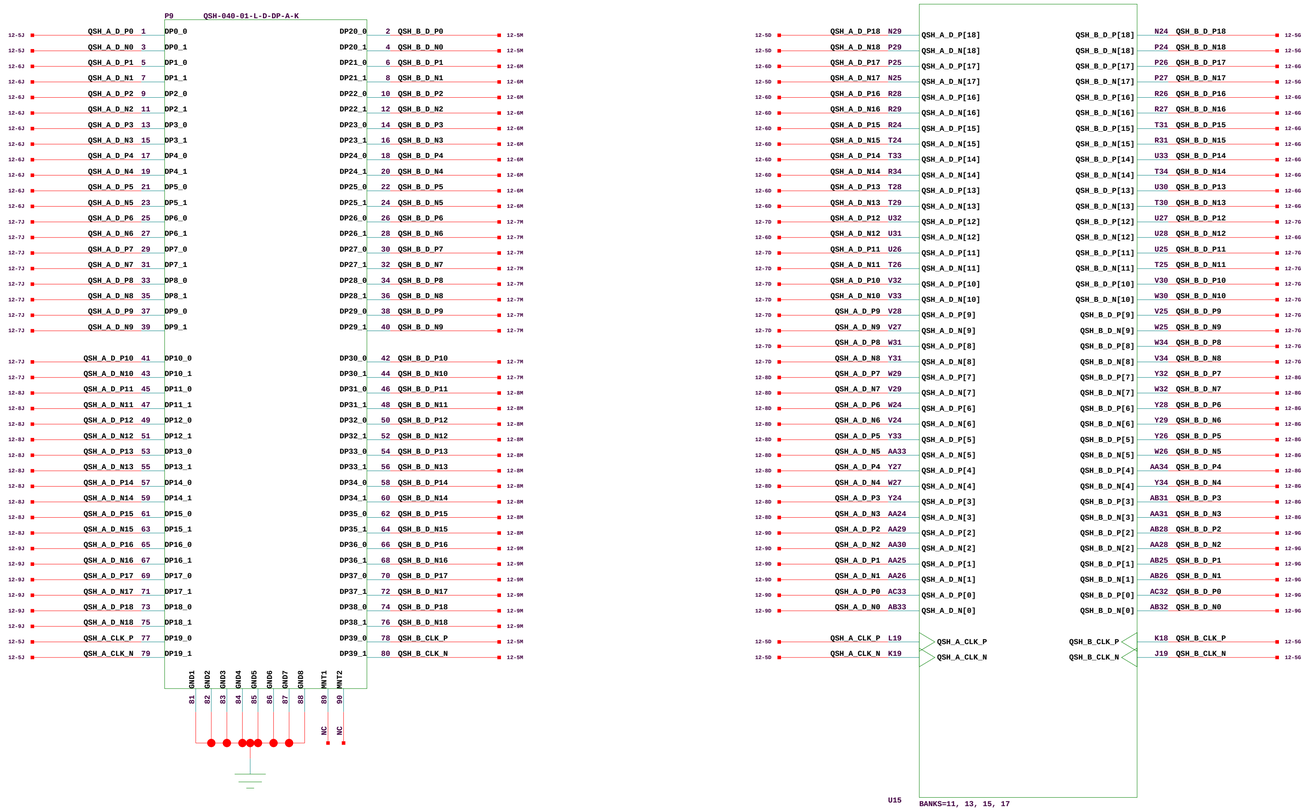




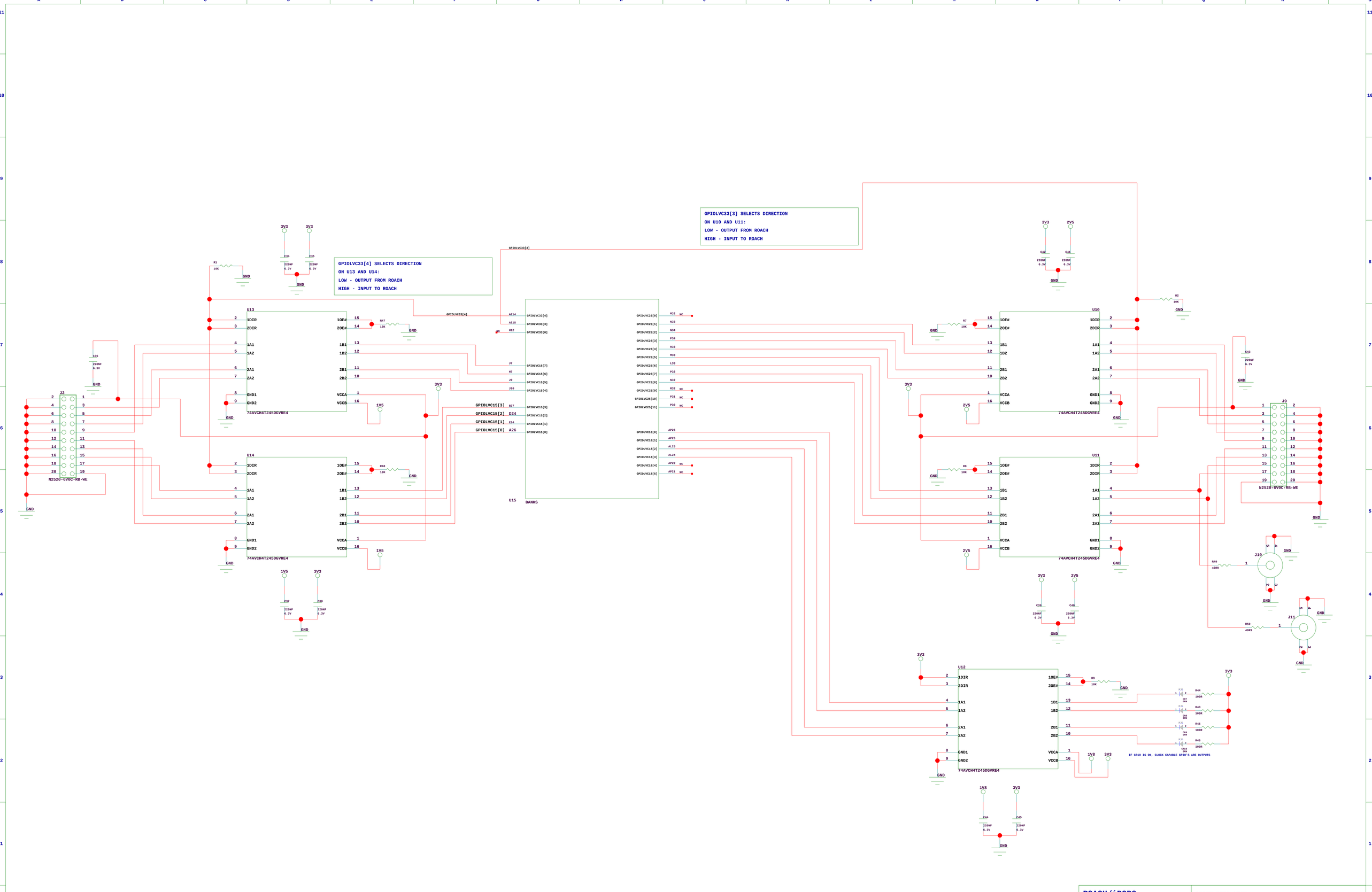
PLACE AT MODULE VDDQ PINS



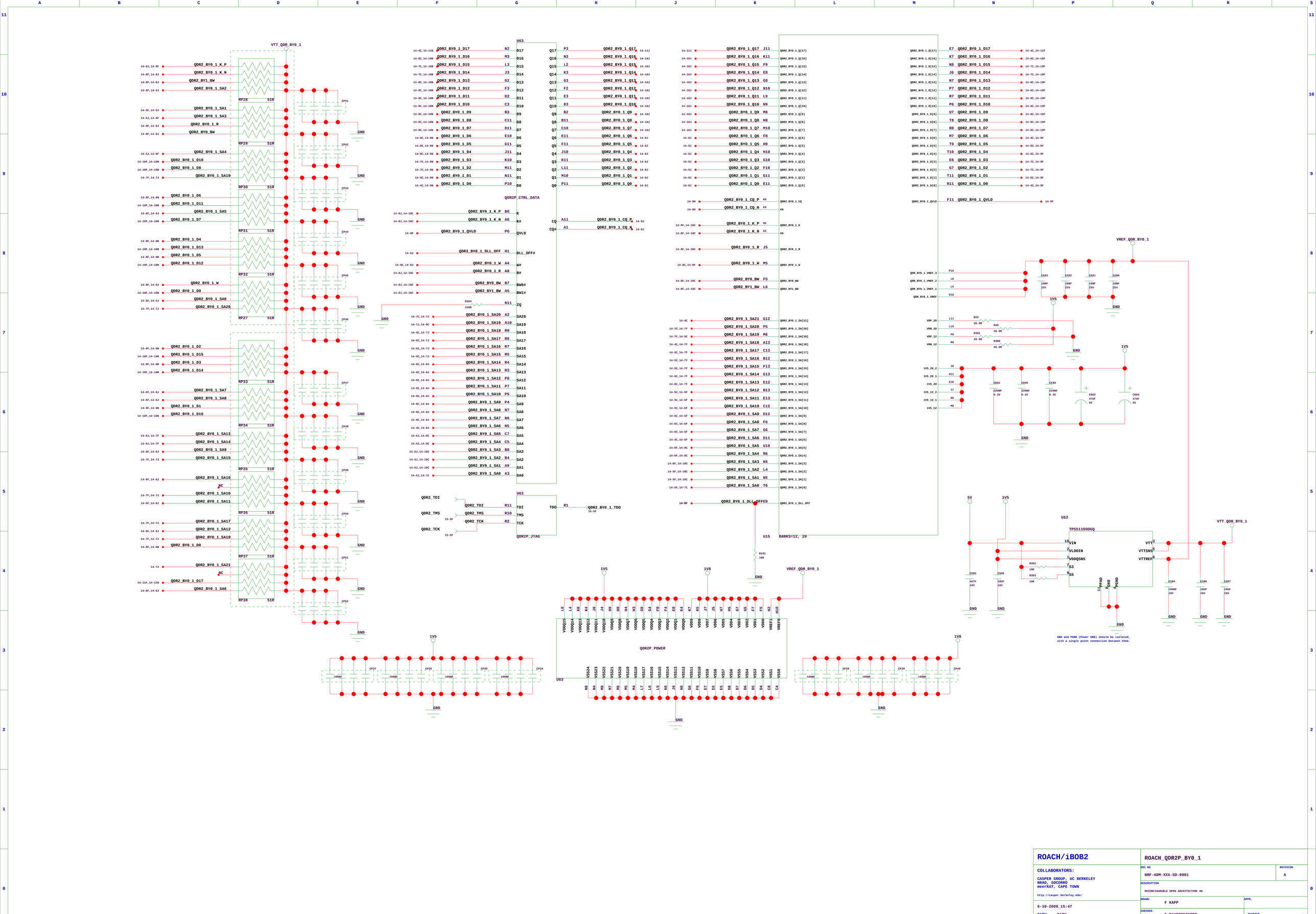
ROACH/iBOB2	**ROACH_DDR2_DIMM**
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE NW
6-10-2008_15:47	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 11 OF 25



ROACH/iBOB2	**ROACH_DIFF_GPIO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE MW
6-10-2008_15:47 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 12 OF 25



ROACH/iBOB2	**ROACH_GPIO_MISC**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-10-2008_15:47	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 13 OF 25



ROACH/iBOB2	**ROACH_QDR2P_BY0_1**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET: 14 OF 25
6-10-2008_15:47 PATH PATH	

VTT_QDR_BY2_3

RP1 51R
RP2 51R
RP3 51R
RP4 51R
RP5 51R
RP6 51R
RP7 51R
RP8 51R
RP9 51R
RP10 51R
RP11 51R
RP12 51R

15-8J,15-9F QDR2_BY2_3_K_P
15-8F,15-8J QDR2_BY2_3_K_N
15-8F,15-8J QDR3_BY3_BW
15-5F,15-5J QDR2_BY2_3_SA2
15-5F,15-5J QDR2_BY2_3_SA1
15-5J,15-6F QDR2_BY2_3_SA3
15-8F,15-8J QDR2_BY2_3_R
15-8F,15-8J QDR2_BY2_BW
15-6F,15-6J QDR2_BY2_3_SA5
15-10F,15-10N QDR2_BY2_3_D8
15-5J,15-6F QDR2_BY2_3_SA4
15-7F,15-7J QDR2_BY2_3_SA19
15-9F,15-9N QDR2_BY2_3_D6
15-10F,15-10N QDR2_BY2_3_D11
15-10F,15-10N QDR2_BY2_3_D7
15-10F,15-10N QDR2_BY2_3_D10
15-9F,15-9N QDR2_BY2_3_D4
15-10F,15-10N QDR2_BY2_3_D13
15-9F,15-9N QDR2_BY2_3_D5
15-10F,15-10N QDR2_BY2_3_D12
15-8F,15-8J QDR2_BY2_3_W
15-10F,15-10N QDR2_BY2_3_D9
15-5F,15-5J QDR2_BY2_3_SA0
15-7F,15-7J QDR2_BY2_3_SA20
15-10F,15-10N QDR2_BY2_3_D16
15-10F,15-10N QDR2_BY2_3_D15
15-9F,15-9N QDR2_BY2_3_D3
15-10F,15-10N QDR2_BY2_3_D14
15-7J QDR2_BY2_3_SA21
NC
15-11F,15-11N QDR2_BY2_3_D17
15-6F,15-6J QDR2_BY2_3_SA6
15-7F,15-7J QDR2_BY2_3_SA17
15-6F,15-6J QDR2_BY2_3_SA12
15-7F,15-7J QDR2_BY2_3_SA18
15-9F,15-9N QDR2_BY2_3_D0
15-6F,15-6J QDR2_BY2_3_SA10
NC
15-7F,15-7J QDR2_BY2_3_SA16
15-6F,15-6J QDR2_BY2_3_SA11
15-6J,15-7F QDR2_BY2_3_SA13
15-6J,15-7F QDR2_BY2_3_SA14
15-6F,15-6J QDR2_BY2_3_SA9
15-7F,15-7J QDR2_BY2_3_SA15
15-6F,15-6J QDR2_BY2_3_SA7
15-6F,15-6J QDR2_BY2_3_SA8
15-9F,15-9N QDR2_BY2_3_D1
15-9F,15-9N QDR2_BY2_3_D2

CP1 100NF
CP2 100NF
CP3 100NF
CP4 100NF
CP5 100NF
CP6 100NF
CP7 100NF
CP8
CP9
CP10
CP11
CP12
CP13
CP14
CP15
CP16
CP17
CP18
CP19

GND
1V5
1V8
5V
VREF_QDR_BY2_3

U17

15-6C,15-11N QDR2_BY2_3_D17 N2 D17
15-7C,15-10N QDR2_BY2_3_D16 M3 D16
15-7C,15-10N QDR2_BY2_3_D15 L3 D15
15-7C,15-10N QDR2_BY2_3_D14 J3 D14
15-8C,15-10N QDR2_BY2_3_D13 G2 D13
15-8C,15-10N QDR2_BY2_3_D12 F3 D12
15-9C,15-10N QDR2_BY2_3_D11 D2 D11
15-8C,15-10N QDR2_BY2_3_D10 C3 D10
15-8C,15-10N QDR2_BY2_3_D9 B3 D9
15-9C,15-10N QDR2_BY2_3_D8 C11 D8
15-9C,15-10N QDR2_BY2_3_D7 D11 D7
15-9C,15-9N QDR2_BY2_3_D6 E10 D6
15-8C,15-9N QDR2_BY2_3_D5 G11 D5
15-8C,15-9N QDR2_BY2_3_D4 J11 D4
15-7C,15-9N QDR2_BY2_3_D3 K10 D3
15-4C,15-9N QDR2_BY2_3_D2 M11 D2
15-4C,15-9N QDR2_BY2_3_D1 N11 D1
15-5C,15-9N QDR2_BY2_3_D0 P10 D0

Q17 P3 QDR2_BY2_3_Q17 D26 QDR2_BY2_3_Q[17]
Q16 N3 QDR2_BY2_3_Q16 C25 QDR2_BY2_3_Q[16]
Q15 L2 QDR2_BY2_3_Q15 B25 QDR2_BY2_3_Q[15]
Q14 K3 QDR2_BY2_3_Q14 C23 QDR2_BY2_3_Q[14]
Q13 G3 QDR2_BY2_3_Q13 C22 QDR2_BY2_3_Q[13]
Q12 F2 QDR2_BY2_3_Q12 A23 QDR2_BY2_3_Q[12]
Q11 E3 QDR2_BY2_3_Q11 C20 QDR2_BY2_3_Q[11]
Q10 D3 QDR2_BY2_3_Q10 B20 QDR2_BY2_3_Q[10]
Q9 B2 QDR2_BY2_3_Q9 C19 QDR2_BY2_3_Q[9]
Q8 B11 QDR2_BY2_3_Q8 B18 QDR2_BY2_3_Q[8]
Q7 C10 QDR2_BY2_3_Q7 A19 QDR2_BY2_3_Q[7]
Q6 E11 QDR2_BY2_3_Q6 C18 QDR2_BY2_3_Q[6]
Q5 F11 QDR2_BY2_3_Q5 A20 QDR2_BY2_3_Q[5]
Q4 J10 QDR2_BY2_3_Q4 A21 QDR2_BY2_3_Q[4]
Q3 K11 QDR2_BY2_3_Q3 B21 QDR2_BY2_3_Q[3]
Q2 L11 QDR2_BY2_3_Q2 B22 QDR2_BY2_3_Q[2]
Q1 M10 QDR2_BY2_3_Q1 B23 QDR2_BY2_3_Q[1]
Q0 P11 QDR2_BY2_3_Q0 A24 QDR2_BY2_3_Q[0]

QDR2P_CTRL_DATA

15-8J,15-10C QDR2_BY2_3_K_P B6 K
15-8J,15-10C QDR2_BY2_3_K_N A6 K#
15-9P QDR2_BY2_3_QVLD P6 QVLD
15-5J QDR2_BY2_3_DLL_OFF H1 DLL_OFF#
15-8C,15-8J QDR2_BY2_3_W A4 W#
15-8J,15-10C QDR2_BY2_3_R A8 R#
15-8J,15-10C QDR2_BY2_BW B7 BW0#
15-8J,15-10C QDR2_BY3_BW A5 BW1#
R55 240R
H11 ZQ
15-7C,15-7J GND
15-7J,15-9C QDR2_BY2_3_SA20 A2 SA20
15-6C,15-7J QDR2_BY2_3_SA19 A10 SA19
15-6C,15-7J QDR2_BY2_3_SA18 R9 SA18
15-6C,15-7J QDR2_BY2_3_SA17 R8 SA17
15-5C,15-7J QDR2_BY2_3_SA16 R7 SA16
15-4C,15-7J QDR2_BY2_3_SA15 R5 SA15
15-5C,15-6J QDR2_BY2_3_SA14 R4 SA14
15-5C,15-6J QDR2_BY2_3_SA13 R3 SA13
15-6C,15-6J QDR2_BY2_3_SA12 P8 SA12
15-5C,15-6J QDR2_BY2_3_SA11 P7 SA11
15-5C,15-6J QDR2_BY2_3_SA10 P5 SA10
15-4C,15-6J QDR2_BY2_3_SA9 P4 SA9
15-4C,15-6J QDR2_BY2_3_SA8 N7 SA8
15-4C,15-6J QDR2_BY2_3_SA7 N6 SA7
15-6C,15-6J QDR2_BY2_3_SA6 N5 SA6
15-6J,15-9C QDR2_BY2_3_SA5 C7 SA5
15-5J,15-9C QDR2_BY2_3_SA4 C5 SA4
15-5J,15-10C QDR2_BY2_3_SA3 B8 SA3
15-5J,15-10C QDR2_BY2_3_SA2 B4 SA2
15-5J,15-10C QDR2_BY2_3_SA1 A9 SA1
15-5J,15-7C QDR2_BY2_3_SA0 A3 SA0

CQ A11 QDR2_BY2_3_CQ_P 15-9J
CQ# A1 QDR2_BY2_3_CQ_N 15-9J

15-8N QDR2_BY2_3_CQ_P C24 QDR2_BY2_3_CQ
15-8N QDR2_BY2_3_CQ_N D25 D25
15-9F,15-10C QDR2_BY2_3_K_P D14 QDR2_BY2_3_K
15-8F,15-10C QDR2_BY2_3_K_N E14 E14
15-8F,15-10C QDR2_BY2_3_R C15 QDR2_BY2_3_R
15-8C,15-8F QDR2_BY2_3_W F15 QDR2_BY2_3_W
15-8F,15-10C QDR2_BY2_BW D15 QDR2_BY2_BW
15-8F,15-10C QDR3_BY3_BW D16 QDR3_BW

15-6C QDR2_BY2_3_SA21 D31 QDR2_BY2_3_SA[21]
15-7C,15-7F QDR2_BY2_3_SA20 F14 QDR2_BY2_3_SA[20]
15-7F,15-9C QDR2_BY2_3_SA19 A14 QDR2_BY2_3_SA[19]
15-6C,15-7F QDR2_BY2_3_SA18 D27 QDR2_BY2_3_SA[18]
15-6C,15-7F QDR2_BY2_3_SA17 A30 QDR2_BY2_3_SA[17]
15-5C,15-7F QDR2_BY2_3_SA16 B30 QDR2_BY2_3_SA[16]
15-4C,15-7F QDR2_BY2_3_SA15 C30 QDR2_BY2_3_SA[15]
15-5C,15-7F QDR2_BY2_3_SA14 B31 QDR2_BY2_3_SA[14]
15-5C,15-7F QDR2_BY2_3_SA13 D30 QDR2_BY2_3_SA[13]
15-6C,15-6F QDR2_BY2_3_SA12 B26 QDR2_BY2_3_SA[12]
15-5C,15-6F QDR2_BY2_3_SA11 A29 QDR2_BY2_3_SA[11]
15-5C,15-6F QDR2_BY2_3_SA10 D29 QDR2_BY2_3_SA[10]
15-4C,15-6F QDR2_BY2_3_SA9 A31 QDR2_BY2_3_SA[9]
15-4C,15-6F QDR2_BY2_3_SA8 G17 QDR2_BY2_3_SA[8]
15-4C,15-6F QDR2_BY2_3_SA7 C27 QDR2_BY2_3_SA[7]
15-6C,15-6F QDR2_BY2_3_SA6 C28 QDR2_BY2_3_SA[6]
15-6F,15-9C QDR2_BY2_3_SA5 E16 QDR2_BY2_3_SA[5]
15-6F,15-9C QDR2_BY2_3_SA4 E17 QDR2_BY2_3_SA[4]
15-6F,15-10C QDR2_BY2_3_SA3 A15 QDR2_BY2_3_SA[3]
15-5F,15-10C QDR2_BY2_3_SA2 B15 QDR2_BY2_3_SA[2]
15-5F,15-10C QDR2_BY2_3_SA1 C14 QDR2_BY2_3_SA[1]
15-5F,15-7C QDR2_BY2_3_SA0 B16 QDR2_BY2_3_SA[0]
15-8F QDR2_BY2_3_DLL_OFF D20 QDR2_BY2_3_DLL_OFF

BANKS=5, 23

U15
R102 10K

QDR2_BY0_1_TDO 14-5H QDR2_BY0_1_TDO R11 TDI
QDR2_TMS 14-5H QDR2_TMS R10 TMS
QDR2_TCK 14-5F QDR2_TCK R2 TCK
TDO R1 QDR2_BY2_3_TDO
QDR2P_JTAG

QDR2_BY2_3_D[17] F24 QDR2_BY2_3_D17 15-6C,15-11F
QDR2_BY2_3_D[16] F23 QDR2_BY2_3_D16 15-7C,15-10F
QDR2_BY2_3_D[15] E23 QDR2_BY2_3_D15 15-7C,15-10F
QDR2_BY2_3_D[14] E22 QDR2_BY2_3_D14 15-7C,15-10F
QDR2_BY2_3_D[13] D22 QDR2_BY2_3_D13 15-8C,15-10F
QDR2_BY2_3_D[12] E21 QDR2_BY2_3_D12 15-8C,15-10F
QDR2_BY2_3_D[11] D21 QDR2_BY2_3_D11 15-9C,15-10F
QDR2_BY2_3_D[10] F18 QDR2_BY2_3_D10 15-8C,15-10F
QDR2_BY2_3_D[9] A16 QDR2_BY2_3_D9 15-8C,15-10F
QDR2_BY2_3_D[8] B17 QDR2_BY2_3_D8 15-9C,15-10F
QDR2_BY2_3_D[7] C17 QDR2_BY2_3_D7 15-9C,15-10F
QDR2_BY2_3_D[6] D17 QDR2_BY2_3_D6 15-9C,15-9F
QDR2_BY2_3_D[5] F16 QDR2_BY2_3_D5 15-8C,15-9F
QDR2_BY2_3_D[4] E19 QDR2_BY2_3_D4 15-8C,15-9F
QDR2_BY2_3_D[3] F20 QDR2_BY2_3_D3 15-7C,15-9F
QDR2_BY2_3_D[2] G20 QDR2_BY2_3_D2 15-4C,15-9F
QDR2_BY2_3_D[1] F21 QDR2_BY2_3_D1 15-4C,15-9F
QDR2_BY2_3_D[0] G21 QDR2_BY2_3_D0 15-5C,15-9F

QDR2_BY2_3_QVLD A25 QDR2_BY2_3_QVLD 15-8F

VREF_QDR_BY2_3
QDR_BY2_3_VREF_3 G18
QDR_BY2_3_VREF_2 F19
QDR_BY2_3_VREF_1 A28
QDR_BY2_3_VREF A18
C56 10NF 25V
C55 10NF 25V
C59 10NF 25V
C46 10NF 25V

VRP_5 D19 RS1 49.9R
VRN_5 E18 RS2 49.9R
VRP_23 B28 R151 49.9R
VRN_23 C29 R152 49.9R

1V5_5_2 F17
1V5_5_1 C16
1V5_5 B19
1V5_23_2 G24
1V5_23_1 F27
1V5_23 C26
C85 220NF 6.3V
C86 220NF 6.3V
C87 220NF 6.3V
C88 470F 6V
C89 470F 6V

U16
VIN 10
VLDOIN 2
VDDQSNS 1
S3 7
S5 9
PPAD 11
GND 5
PGND 4
VTT 3
VTTSNS 5
VTTREF 6
R53 10K
R54 10K
C58 4U7F 10V
C59 10UF 16V
C57 100NF 10V
C84 10UF 16V
C69 10UF 16V

GND and PGND (Power GND) should be isolated, with a single point connection between them.

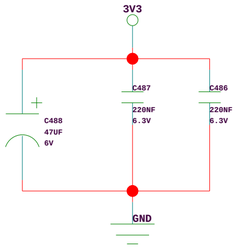
QDR2P_POWER

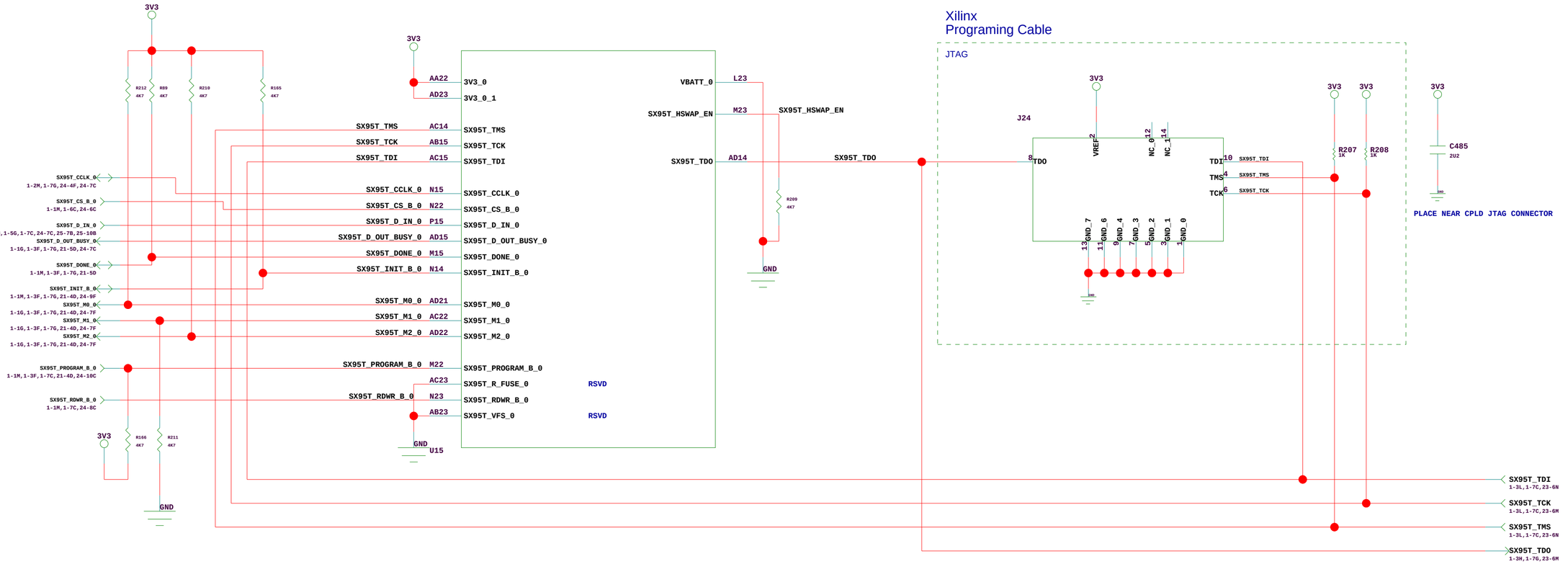
VDDQ15 L8
VDDQ14 L4
VDDQ13 K8
VDDQ12 K4
VDDQ11 J8
VDDQ10 J4
VDDQ9 H9
VDDQ8 H8
VDDQ7 H4
VDDQ6 H3
VDDQ5 G8
VDDQ4 G4
VDDQ3 F9
VDDQ2 F4
VDDQ1 E8
VDDQ0 E4
VDD9 K7
VDD8 J7
VDD7 J5
VDD6 H7
VDD5 H5
VDD4 G7
VDD3 G5
VDD2 F7
VDD1 F5
VDD0 H2
VREF1 H10
VREF0

VSS24 N8
VSS23 N4
VSS22 M8
VSS21 M7
VSS20 M6
VSS19 M5
VSS18 M4
VSS17 L7
VSS16 L6
VSS15 L5
VSS14 K6
VSS13 J6
VSS12 H6
VSS11 G6
VSS10 F8
VSS9 F6
VSS8 E7
VSS7 E6
VSS6 E5
VSS5 D8
VSS4 D7
VSS3 D6
VSS2 D5
VSS1 D4
VSS0 C8
C4

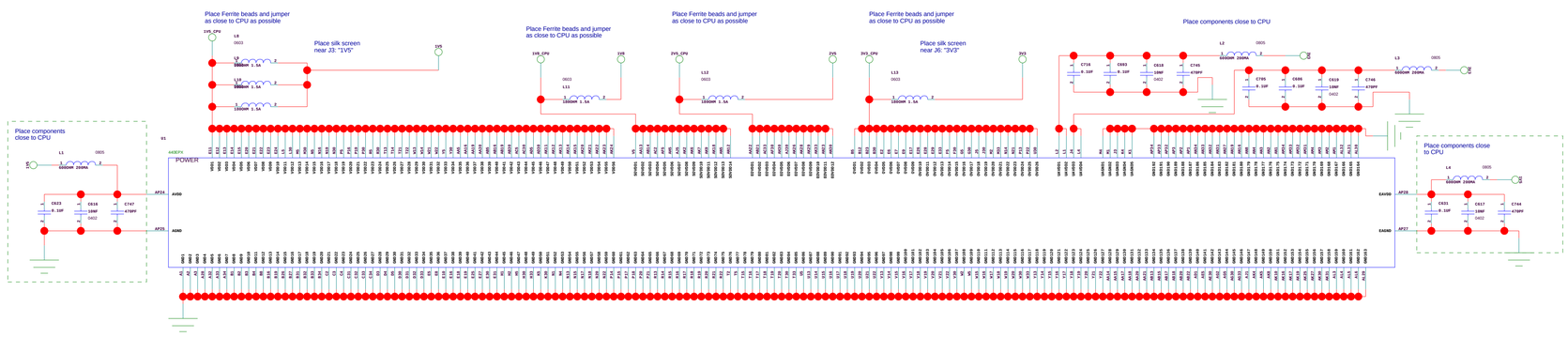
TBD

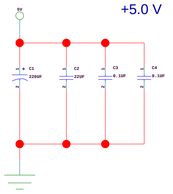
VALID CONFIGURATION MODES			
Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	1	Output
Master SPI	001	1	Output
Master BPI-Up	010	8, 16	Output
Master BPI-Down	011	8, 16	Output
Master SelectMAP	100	8, 16	Output
JTAG	101	1	Input (TCK)
Slave SelectMAP	110	8, 16, 32	Input
Slave Serial	111	1	Input

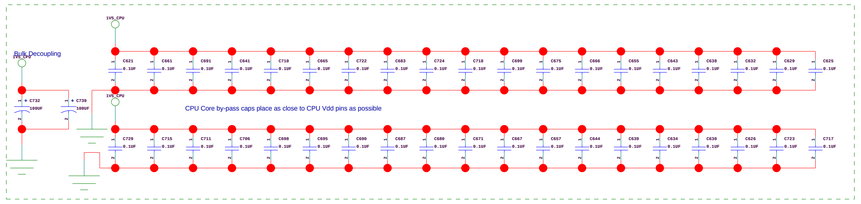


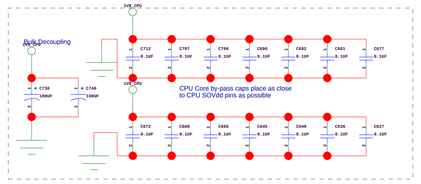


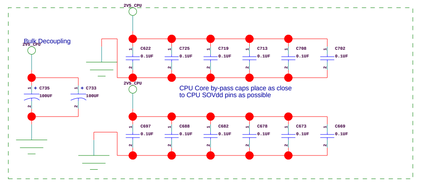
ROACH/iBOB2	**ROACH_CONFIG**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 16 OF 25
6-10-2008_15:47 PATH PATH	



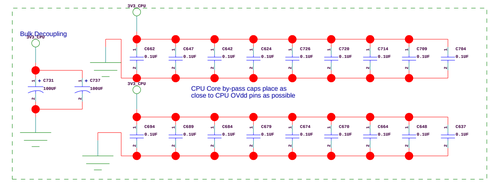


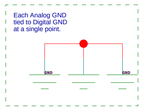






REMOVED 1.8V AND 1.5V REGULATORS, CONNECTED TO V5 RAILS

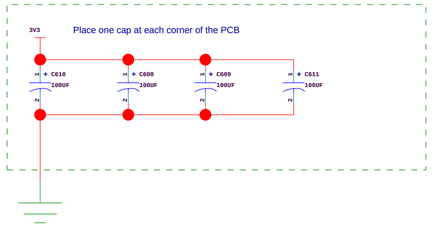




REMOVED VTT AND VREF - INCLUDED ON ROACH_PPC_DDR2

ROACH/iBOB2	**ROACH_PPC_POWER_1**
COLLABORATORS: **CASPER GROUP, UC BERKELEY** **NRAO, SOCORRO** **meerKAT, CAPE TOWN** http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-10-2008_15:47 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 17 OF 25

REMOVED 3V3 GENERATION



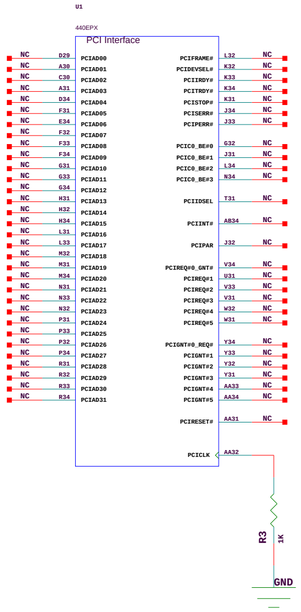
REMOVED +12V GENERATION

REMOVED -12V GENERATION

REMOVED +1V GENERATION

REMOVED +2V5 GENERATION

ROACH/iBOB2	ROACH_PPC_POWER_2
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 · REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW DRAWN: F KAPP · APPR: CHECKED: E BAUERMEISTER · SHEET 18 OF 25
6-10-2008_15:47 PATH PATH	



PCI BUS NOT IMPLEMENTED

ROACH/iBOB2	**ROACH_PPC_PCI**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-10-2008_15:47 PATH PATH	DRAWN: F KAPP APPR: CHECKED: E BAUERMEISTER SHEET 19 OF 25

Place nearest PHY pin 96

2V5
C533
10NF

Place nearest PHY pin 101

2V5
C534
10NF

Place nearest PHY pin 98

1V8
R233 1R
C536 22UF
C511 10NF

Place nearest PHY pin 100

1V8
R232 1R
C535 22UF
C512 10NF

Place as close to PHY CORE VDD power pins as possible

1V8
C526 10NF
C527 100NF
C525 10NF
C528 100NF
C530 10NF
C529 100NF
C531 10NF
C532 100NF

Place as close to PHY IO VDD power pins as possible

2V5
C513 10NF
C514 100NF
C515 10NF
C516 100NF
C517 10NF
C518 100NF
C519 10NF
C520 100NF
C521 10NF
C522 100NF
C523 10NF
C524 100NF

U3
440EPX
Gig-Ethernet RGMII1

GMC1_TXD0	AF26	NC
GMC1_TXD1	AL26	NC
GMC1_TXD2	AK26	NC
GMC1_TXD3	AK25	NC
GMC1_TXCTL	AK24	NC
GMC1_TXCLK	AK22	NC
GMC1_RXD0	AK29	NC
GMC1_RXD1	AF30	NC
GMC1_RXD2	AF31	NC
GMC1_RXD3	AK30	NC
GMC1_RXCTL	AL33	NC
GMC1_RXCLK	AJ32	NC

UNUSED SECOND ETHERNET MAC

U1
440EPX
Gig-Ethernet RGMII0

GMC0_TXD0	AL24	
GMC0_TXD1	AK23	
GMC0_TXD2	AK25	
GMC0_TXD3	AL25	
GMC0_TXCTL	AK24	
GMC0_TXCLK	AK27	
GMCTXCLK	AL27	
GMC0_RXD0	AL28	
GMC0_RXD1	AF29	
GMC0_RXD2	AK28	
GMC0_RXD3	AK29	
GMC0_RXCTL	AJ31	
GMC0_RXCLK	AK26	
GMCRXCLK	AL34	
GMCMDIO	AK34	
GMCREFCLK	AJ33	

Place resistors as close to CPU as possible and keep all traces lengths equal

R241 22R 4D10
R240 22R 4D11
R239 22R 4D12
R238 22R 4D13
R237 22R 4D14
R236 22R 4D15

GMCRXD0
GMCRXD1
GMCRXD2
GMCRXD3
GMCRXCTL
GMCRXCLK

R242 22R
R275 22R
R274 22R
R273 22R
R272 22R
R276 22R
22R

R219 0R
2V5
GMCMDCLK
GMCMDIO
GMCREFCLK_125MHZ
R277 22R
Place resistors close to PHY all trace lengths equal
R267 1K
GMCMDCLK 1-4E,20-3C
GMCMDIO 1-4E,20-3C

NC
NC NC
NC NC

GMCRXTXCTL
GMCRXD0
GMCRXD1
GMCRXD2
GMCRXD3
GMCRXCLK
GMCRXER
GMCRXDV
GMCCRS
GMCCOL
GMCTXCLK
GMCTXD0
GMCTXD1
GMCTXD2
GMCTXD3
GMCTXER
GMCTXEN

U50
DP83865DVH

RX_DV/RCK	125	GMCRXDV
RX_CLK	117	GMCRXCLK
RX_D0/SD	121	GMCRXD0
RX_D1/SD	120	GMCRXD1
RX_D2/SD	119	GMCRXD2
RX_D3/SD	118	GMCRXD3
RX_ER/MDIX_EN	116	GMCRXER
CRS_DV/MII_MODE	115	GMCRXDV
COL/RMII_MODE	114	GMCCOL
MDC	92	GMCMDCLK
MDIO	93	GMCMDIO
CLK_TO_MAC	95	GMCREFCLK_125MHZ
RESETn	33	GETH0_RST#
INTERRUPTn	3	GETH0_INT#
CLK_IN	96	CLK_25
CLK_OUT	97	NC
TDO	28	
TDI	31	
TCK	26	
TMS	27	
TRSTn	32	R178 2K2
TXD0/TX0	75	GMCTXD0
TXD1/TX1	74	GMCTXD1
TXD2/TX2	72	GMCTXD2
TXD3/TX3	71	GMCTXD3
TXD4	69	
TXD5	68	
TXD6	67	
TXD7	65	
TX_EN/TXEN_ER	63	GMCTXCTL
TX_ER	61	
TX_CLK/RGMII_SEL1	60	GMCTXCLK
GTX_CLK/TCK	79	NC
CRS/RGMII_SEL0	45	NC
COL	39	NC
RXD0/RX0	55	
RXD1/RX1	54	
RXD2/RX2	53	
RXD3/RX3	52	
RXD4	50	
RXD5	49	
RXD6	48	
RXD7	46	
RX_DV/RCK	44	
RX_ER/MDIX_EN	43	NC
RX_CLK	57	
MDC	91	
MDIO	90	
CLK_TO_MAC	85	
RESETn	33	
INTERRUPTn	3	
CLK_IN	86	
CLK_OUT	87	
TDO	28	
TDI	31	
TCK	26	
TMS	27	
TRSTn	32	
MDIA_P	108	MDI0_0P
MDIA_N	109	MDI0_0N
MDIB_P	114	MDI0_1P
MDIB_N	115	MDI0_1N
MDIC_P	120	MDI0_2P
MDIC_N	121	MDI0_2N
MDID_P	126	MDI0_3P
MDID_N	127	MDI0_3N
VDD_SEL_STRAP	34	
MAC_CLK_EN_STRAP	88	
MDIX_EN_STRAP	89	
MULTI_EN_STRAP	94	
L10_L100	10	LED0_L10/100
L100_L10	9	LED0_L100
L10_LED	8	LED0_L10
LED_ACT	7	
LED_DUPLEX	13	
PHYAD0	14	
PHYAD1	17	
PHYAD2	18	
PHYAD3	19	
PHYAD4	95	
BG_REF	102	R253 9K76
TX_TCLK		NC
NON_IEEE_STRAP		NC
RESERVED1		NC
RESERVED2		NC
RESERVED		NC

Place decoupling C close to termination R
All traces 50Ohm WRT GND or 2V5
Place corresponding as close to PHY as possible. Keep all trace lengths equal to each other and as short as possible.

R254 49.9R
R257 49.9R
R258 49.9R
R260 49.9R
C507 10NF
C508 10NF
C509 10NF
C510 10NF

R284 2K2
NOSTUFF
R265 2K2
NOSTUFF
R264 2K2
NOSTUFF

Ethernet LEDs
Top LED = SPEED/LINK
Green = 100
Off = 10/100
Bottom LED = ACTIVITY
Green/Toggle = ACTIVITY

J25
HFJ11-1G02E-L12
GRN
GRN_YEL
TRXP
TRXN
TDCP
TDCN
TDXP
TDXN
VCC
GND
MNT1
MNT2
CASE1
CASE2
NC
GND
C537 22UF

R269 49.9R
R270 49.9R
R271 49.9R
R272 49.9R
R273 49.9R
R274 49.9R
R275 49.9R
R276 49.9R
R277 49.9R
R278 49.9R
R279 49.9R
R280 49.9R
R281 49.9R
R282 49.9R
R283 49.9R
R284 49.9R
R285 49.9R
R286 49.9R
R287 49.9R
R288 49.9R
R289 49.9R
R290 49.9R
R291 49.9R
R292 49.9R
R293 49.9R
R294 49.9R
R295 49.9R
R296 49.9R
R297 49.9R
R298 49.9R
R299 49.9R
R300 49.9R
R301 49.9R
R302 49.9R
R303 49.9R
R304 49.9R
R305 49.9R
R306 49.9R
R307 49.9R
R308 49.9R
R309 49.9R
R310 49.9R
R311 49.9R
R312 49.9R
R313 49.9R
R314 49.9R
R315 49.9R
R316 49.9R
R317 49.9R
R318 49.9R
R319 49.9R
R320 49.9R
R321 49.9R
R322 49.9R
R323 49.9R
R324 49.9R
R325 49.9R
R326 49.9R
R327 49.9R
R328 49.9R
R329 49.9R
R330 49.9R
R331 49.9R
R332 49.9R
R333 49.9R
R334 49.9R
R335 49.9R
R336 49.9R
R337 49.9R
R338 49.9R
R339 49.9R
R340 49.9R
R341 49.9R

CONFIRMED NC'S ON PINS WITH AMCC TECH SUPPORT IN EMAIL DATED 2007/08/30
NC RDJECTPKT0
NC RDJECTPKT1

ETHERNET Mgt.
MDCLK
MDIO

The RGMII signaling is 125 MHz using both rising and falling edges of the clock.

The Tx and the RX side trace length should be matched within the signal group to minimize timing skew.
It is advised to match the trace length within 0.1 inch within the Tx and Rx signal groups. Minimize the number of via on the RGMII lines to minimize timing skew.
Since the signal rise and fall time are sub-nano second, transmission line design guidelines should be followed.

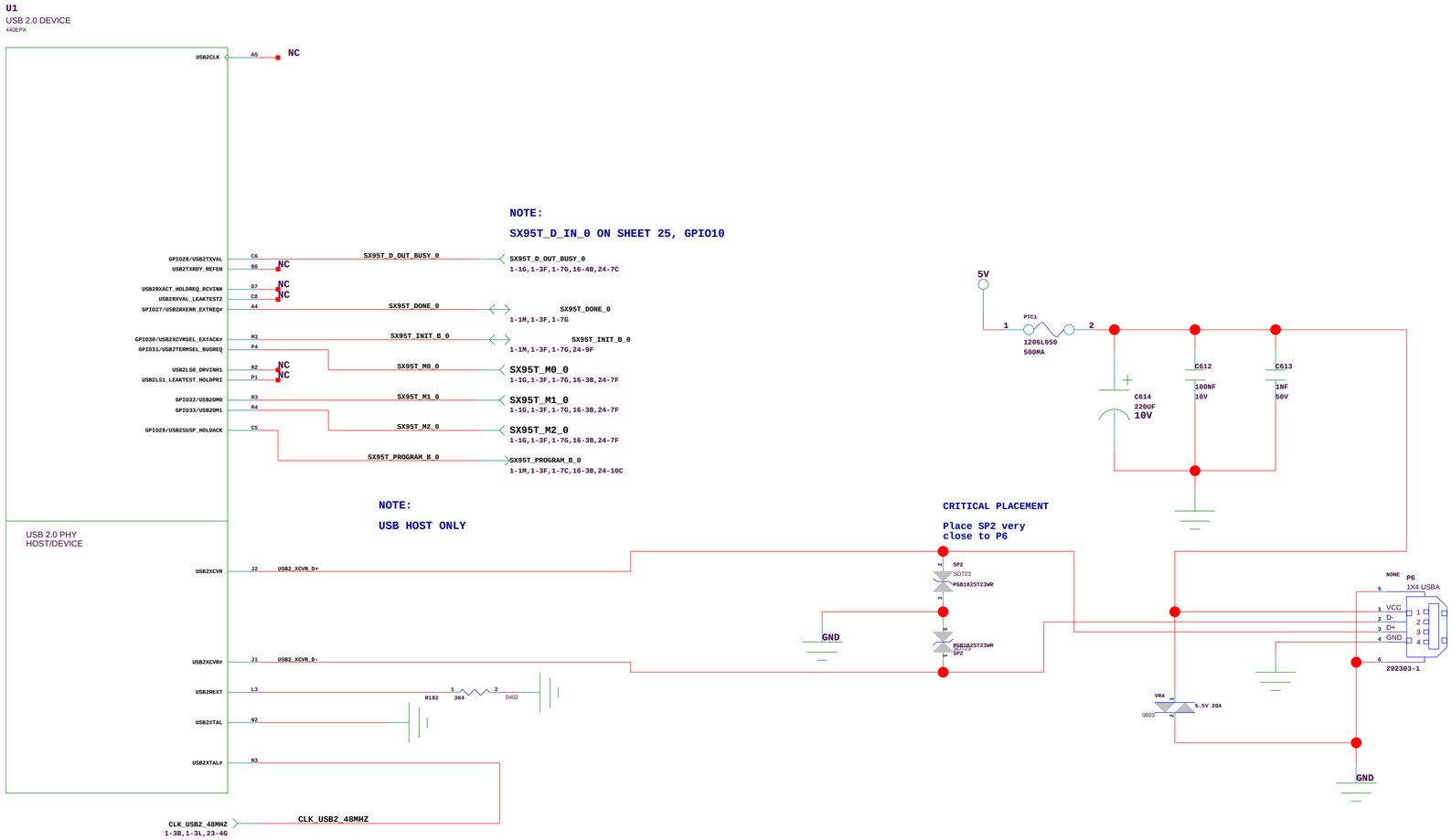
Place jumpers in line with signals
1-4E,29-4D GMCMDIO JP24
1-4E,29-4D GMCMDCLK JP25

2V5
NOSTUFF
R284 2K2
R309 2K2
R329 2K2
R271 2K2
JP20
JP21
JP22
JP23

STRAPPING OPTIONS FOR PHY - SEE DATA SHEET FOR DETAIL

JP11 R243 2K2 R244 330R DUPLEX LED D6
JP13 R245 2K2 R246 330R
JP15 R247 2K2 R248 330R L10 LED D7
JP17 R249 2K2 R250 330R L100 LED D8
JP18 R252 2K2 R251 330R
JP10
JP12
JP14
JP16
JP19

ROACH/iBOB2	ROACH_PPC_ETH1
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
6-10-2008_15:47 PATH PATH	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
	DRAWN: F KAPP; APPR:
	CHECKED: E BAUERMEISTER; SHEET 20 OF 25



ROACH/iBOB2	**ROACH_PPC_USB**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-10-2008_15:47 PATH PATH	DRAWN: F KAPP — APPR: CHECKED: E BAUERMEISTER — SHEET 21 OF 25

DDR_PA[15:0]

DDR_PD[63:0]

DDR SDRAM

U1

44GEPX

DDR_PD0	AB2	MEMDATA00	MEMADDR00	AM5	DDR_PA0
DDR_PD1	AP22	MEMDATA01	MEMADDR01	AP4	DDR_PA1
DDR_PD2	AM26	MEMDATA02	MEMADDR02	AM6	DDR_PA2
DDR_PD3	AL28	MEMDATA03	MEMADDR03	AM6	DDR_PA3
DDR_PD4	AL22	MEMDATA04	MEMADDR04	AP6	DDR_PA4
DDR_PD5	AM22	MEMDATA05	MEMADDR05	AN6	DDR_PA5
DDR_PD6	AR21	MEMDATA06	MEMADDR06	AL7	DDR_PA6
DDR_PD7	AP21	MEMDATA07	MEMADDR07	AN7	DDR_PA7
DDR_PD8	AP28	MEMDATA08	MEMADDR08	AM7	DDR_PA8
DDR_PD9	AL18	MEMDATA09	MEMADDR09	AP7	DDR_PA9
DDR_PD10	AR17	MEMDATA10	MEMADDR10	AL2	DDR_PA10
DDR_PD11	AP17	MEMDATA11	MEMADDR11	AL8	DDR_PA11
DDR_PD12	AN20	MEMDATA12	MEMADDR12	AP8	DDR_PA12
DDR_PD13	AP18	MEMDATA13	MEMADDR13	AN4	DDR_PA13
DDR_PD14	AN18	MEMDATA14			
DDR_PD15	AL15	MEMDATA15			
DDR_PD16	AM16	MEMDATA16			
DDR_PD17	AP16	MEMDATA17			
DDR_PD18	AL14	MEMDATA18			
DDR_PD19	AP14	MEMDATA19			
DDR_PD20	AL17	MEMDATA20			
DDR_PD21	AM17	MEMDATA21			
DDR_PD22	AN15	MEMDATA22			
DDR_PD23	AM15	MEMDATA23			
DDR_PD24	AP13	MEMDATA24			
DDR_PD25	AN13	MEMDATA25			
DDR_PD26	AP12	MEMDATA26			
DDR_PD27	AL12	MEMDATA27			
DDR_PD28	AM14	MEMDATA28			
DDR_PD29	AM13	MEMDATA29			
DDR_PD30	AL13	MEMDATA30			
DDR_PD31	AM12	MEMDATA31			
DDR_PD32	AF3	MEMDATA32			
DDR_PD33	AF1	MEMDATA33			
DDR_PD34	AD4	MEMDATA34			
DDR_PD35	AD3	MEMDATA35			
DDR_PD36	AD1	MEMDATA36			
DDR_PD37	AF2	MEMDATA37			
DDR_PD38	AE2	MEMDATA38			
DDR_PD39	AE1	MEMDATA39			
DDR_PD40	AC2	MEMDATA40			
DDR_PD41	AC1	MEMDATA41			
DDR_PD42	AA4	MEMDATA42			
DDR_PD43	AA3	MEMDATA43			
DDR_PD44	AD2	MEMDATA44			
DDR_PD45	AC4	MEMDATA45			
DDR_PD46	AB1	MEMDATA46			
DDR_PD47	AB2	MEMDATA47			
DDR_PD48	Y3	MEMDATA48			
DDR_PD49	Y2	MEMDATA49			
DDR_PD50	Y4	MEMDATA50			
DDR_PD51	V3	MEMDATA51			
DDR_PD52	AA2	MEMDATA52			
DDR_PD53	AA1	MEMDATA53			
DDR_PD54	W3	MEMDATA54			
DDR_PD55	W1	MEMDATA55			
DDR_PD56	V1	MEMDATA56			
DDR_PD57	U2	MEMDATA57			
DDR_PD58	T4	MEMDATA58			
DDR_PD59	R1	MEMDATA59			
DDR_PD60	V5	MEMDATA60			
DDR_PD61	V4	MEMDATA61			
DDR_PD62	T1	MEMDATA62			
DDR_PD63	T3	MEMDATA63			
		MEMDQS0		AN3	DDR_PDQS0
		MEMDQS1		AR1	DDR_PDQS1
				AN2	DDR_PDQS2
				AM3	DDR_PDQS3
				AM2	DDR_PDQS4
				AN1	DDR_PDQS5
				W4	DDR_PDQS6
				Y1	DDR_PDQS7
				AP10	DDR_PDQS8
		MEMDOT0		AN3	DDR_PDOT0
		MEMDOT1		AR1	DDR_PDOT1
				AN2	DDR_PCS0#
				AM1	DDR_PCS1#
		MEMCLKEN		AN9	DDR_PCKE
		MEMCLKOUT		AL1	DDR_CLKOUT
		MEMCLKOUT#		AM1	DDR_CLKOUT#
				AM11	PPC_ECC0
				AL11	PPC_ECC1
				AN9	PPC_ECC2
				AL9	PPC_ECC3
				AM11	PPC_ECC4
				AN11	PPC_ECC5
				AM10	PPC_ECC6
				AP9	PPC_ECC7

ECC0	AM11	PPC_ECC0
ECC1	AL11	PPC_ECC1
ECC2	AN9	PPC_ECC2
ECC3	AL9	PPC_ECC3
ECC4	AM11	PPC_ECC4
ECC5	AN11	PPC_ECC5
ECC6	AM10	PPC_ECC6
ECC7	AP9	PPC_ECC7

SVREF1A	Y4	
SVREF2A	AL19	
SVREF1B	AF4	
SVREF2B	AL19	

DDR_PBA0	AJ3	22-7L,22-8K
DDR_PBA1	AN3	22-8K,22-10L
DDR_PBA2	AP8	22-8K,22-8L
DDR_PRAS#	AJ4	22-7K,22-7L
DDR_PCAS#	AN4	22-7L,22-8K
DDR_PWE#	AJ2	22-3K,22-7L
DDR_PDM0	AL21	22-5K
DDR_PDM1	AP18	22-6K
DDR_PDM2	AP15	22-6K
DDR_PDM3	AL14	22-6K
DDR_PDM4	AD4	22-6K
DDR_PDM5	AB3	22-6K
DDR_PDM6	Y3	22-6K
DDR_PDM7	U3	22-6K
DDR_PDM8	AN18	22-6K

DDR_PDQS0	AM21	22-4K
DDR_PDQS1	AM19	22-4K
DDR_PDQS2	AL16	22-4K
DDR_PDQS3	AM13	22-4K
DDR_PDQS4	AB3	22-4K
DDR_PDQS5	AB4	22-5K
DDR_PDQS6	W4	22-5K
DDR_PDQS7	U4	22-5K
DDR_PDQS8	AP10	22-5K

DDR2 Clock line must be 500ps longer than Address/Command lines
To compensate for additional loading when using unbuffered DIMM's
See P84 of PPC440EPx for more information

DDR_VREF_0V9

DDR_VTT

5V

1V8

Place parts as close to CPU as possible

C158	0.1UF		
C149	0.1UF		
C151	0.1UF	0402	
C152	0.1UF	0402	
C148	10UF	0402	

U32

TPS51100DGQ

VIN	10		
VLDOIN	2		
VDDQSNS	1		
S3	7		
S5	9		
VTT	3		
VTTSNS	5		
VTTREF	6		
PAD	11		
GND	4		
PGND	8		

C459	H27F	10V
C456	10UF	10V
R230	10K	
R229	10K	
R6	120R	
C453	100NF	10V
C21	22PF	
C457	10UF	10V
C458	10UF	10V

GND

I2C0_SCLK	1-2B,1-5L,1-9B,2-2P,25-5A		
I2C0_SDATA	1-2B,1-5L,1-9C		

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DDR_PDQ63	236	DDR2_DIMM_DQ[63]	
DDR_PDQ62	235	DDR2_DIMM_DQ[62]	
DDR_PDQ61	230	DDR2_DIMM_DQ[61]	
DDR_PDQ60	229	DDR2_DIMM_DQ[60]	
DDR_PDQ59	117	DDR2_DIMM_DQ[59]	
DDR_PDQ58	116	DDR2_DIMM_DQ[58]	
DDR_PDQ57	111	DDR2_DIMM_DQ[57]	
DDR_PDQ56	110	DDR2_DIMM_DQ[56]	
DDR_PDQ55	227	DDR2_DIMM_DQ[55]	
DDR_PDQ54	226	DDR2_DIMM_DQ[54]	
DDR_PDQ53	218	DDR2_DIMM_DQ[53]	
DDR_PDQ52	217	DDR2_DIMM_DQ[52]	
DDR_PDQ51	108	DDR2_DIMM_DQ[51]	
DDR_PDQ50	107	DDR2_DIMM_DQ[50]	
DDR_PDQ49	99	DDR2_DIMM_DQ[49]	
DDR_PDQ48	98	DDR2_DIMM_DQ[48]	
DDR_PDQ47	215	DDR2_DIMM_DQ[47]	
DDR_PDQ46	214	DDR2_DIMM_DQ[46]	
DDR_PDQ45	209	DDR2_DIMM_DQ[45]	
DDR_PDQ44	208	DDR2_DIMM_DQ[44]	
DDR_PDQ43	96	DDR2_DIMM_DQ[43]	
DDR_PDQ42	95	DDR2_DIMM_DQ[42]	
DDR_PDQ41	90	DDR2_DIMM_DQ[41]	
DDR_PDQ40	89	DDR2_DIMM_DQ[40]	
DDR_PDQ39	206	DDR2_DIMM_DQ[39]	
DDR_PDQ38	205	DDR2_DIMM_DQ[38]	
DDR_PDQ37	200	DDR2_DIMM_DQ[37]	
DDR_PDQ36	199	DDR2_DIMM_DQ[36]	
DDR_PDQ35	87	DDR2_DIMM_DQ[35]	
DDR_PDQ34	86	DDR2_DIMM_DQ[34]	
DDR_PDQ33	81	DDR2_DIMM_DQ[33]	
DDR_PDQ32	80	DDR2_DIMM_DQ[32]	
DDR_PDQ31	159	DDR2_DIMM_DQ[31]	
DDR_PDQ30	158	DDR2_DIMM_DQ[30]	
DDR_PDQ29	153	DDR2_DIMM_DQ[29]	
DDR_PDQ28	152	DDR2_DIMM_DQ[28]	
DDR_PDQ27	40	DDR2_DIMM_DQ[27]	
DDR_PDQ26	39	DDR2_DIMM_DQ[26]	
DDR_PDQ25	34	DDR2_DIMM_DQ[25]	
DDR_PDQ24	33	DDR2_DIMM_DQ[24]	
DDR_PDQ23	150	DDR2_DIMM_DQ[23]	
DDR_PDQ22	149	DDR2_DIMM_DQ[22]	
DDR_PDQ21	144	DDR2_DIMM_DQ[21]	
DDR_PDQ20	143	DDR2_DIMM_DQ[20]	
DDR_PDQ19	31	DDR2_DIMM_DQ[19]	
DDR_PDQ18	30	DDR2_DIMM_DQ[18]	
DDR_PDQ17	25	DDR2_DIMM_DQ[17]	
DDR_PDQ16	24	DDR2_DIMM_DQ[16]	
DDR_PDQ15	141	DDR2_DIMM_DQ[15]	
DDR_PDQ14	140	DDR2_DIMM_DQ[14]	
DDR_PDQ13	132	DDR2_DIMM_DQ[13]	
DDR_PDQ12	131	DDR2_DIMM_DQ[12]	
DDR_PDQ11	22	DDR2_DIMM_DQ[11]	
DDR_PDQ10	21	DDR2_DIMM_DQ[10]	
DDR_PDQ9	13	DDR2_DIMM_DQ[9]	
DDR_PDQ8	12	DDR2_DIMM_DQ[8]	
DDR_PDQ7	129	DDR2_DIMM_DQ[7]	
DDR_PDQ6	128	DDR2_DIMM_DQ[6]	
DDR_PDQ5	123	DDR2_DIMM_DQ[5]	
DDR_PDQ4	122	DDR2_DIMM_DQ[4]	
DDR_PDQ3	10	DDR2_DIMM_DQ[3]	
DDR_PDQ2	9	DDR2_DIMM_DQ[2]	
DDR_PDQ1	4	DDR2_DIMM_DQ[1]	
DDR_PDQ0	3	DDR2_DIMM_DQ[0]	

PPC_ECC7	168	DDR2_DIMM_CB7	
PPC_ECC6	167	DDR2_DIMM_CB6	
PPC_ECC5	162	DDR2_DIMM_CB5	
PPC_ECC4	161	DDR2_DIMM_CB4	
PPC_ECC3	49	DDR2_DIMM_CB3	
PPC_ECC2	48	DDR2_DIMM_CB2	
PPC_ECC1	43	DDR2_DIMM_CB1	
PPC_ECC0	42	DDR2_DIMM_CB0	

DDR2_DIMM_SA2	101		
DDR2_DIMM_SA1	240		
DDR2_DIMM_SA0	239		
DDR2_DIMM_SCL	120		
DDR2_DIMM_SDA	119		

DDR2_DIMM_A[15]	173	DDR_PA15	
DDR2_DIMM_A[14]	174	DDR_PA14	
DDR2_DIMM_A[13]	196	DDR_PA13	
DDR2_DIMM_A[12]	176	DDR_PA12	
DDR2_DIMM_A[11]	57	DDR_PA11	
DDR2_DIMM_A[10]	70	DDR_PA10	
DDR2_DIMM_A[9]	177	DDR_PA9	
DDR2_DIMM_A[8]	179	DDR_PA8	
DDR2_DIMM_A[7]	58	DDR_PA7	
DDR2_DIMM_A[6]	180	DDR_PA6	
DDR2_DIMM_A[5]	60	DDR_PA5	
DDR2_DIMM_A[4]	61	DDR_PA4	
DDR2_DIMM_A[3]	182	DDR_PA3	
DDR2_DIMM_A[2]	63	DDR_PA2	
DDR2_DIMM_A[1]	183	DDR_PA1	
DDR2_DIMM_A[0]	188	DDR_PA0	

DDR2_DIMM_BA[2]	54	DDR_PBA2	22-8L,22-9D
DDR2_DIMM_BA[1]	190	DDR_PBA1	22-9D,22-10L
DDR2_DIMM_BA[0]	71	DDR_PBA0	22-7L,22-9D
DDR2_DIMM_CAS#	74	DDR_PCAS#	22-7L,22-9D
DDR2_DIMM_RAS#	192	DDR_PRAS#	22-7L,22-9D

DDR2_DIMM_CK_P[2]	220	NC	
DDR2_DIMM_CK_N[2]	221	NC	
DDR2_DIMM_CK_P[1]	137	NC	
DDR2_DIMM_CK_N[1]	138	NC	
DDR2_DIMM_CK_P[0]	185	DDR_CLKOUT	
DDR2_DIMM_CK_N[0]	186	DDR_CLKOUT#	
DDR2_DIMM_CKE[1]	171	NC	
DDR2_DIMM_CKE[0]	52	DDR_PCKE	22-8D,22-11L

C455 5PF 50V

DDR2_DIMM_DM_CB	164	DDR_PDM8	22-8D
DDR2_DIMM_DM[7]	232	DDR_PDM7	22-8D
DDR2_DIMM_DM[6]	223	DDR_PDM6	22-9D
DDR2_DIMM_DM[5]	211	DDR_PDM5	22-9D
DDR2_DIMM_DM[4]	202	DDR_PDM4	22-9D
DDR2_DIMM_DM[3]	155	DDR_PDM3	22-9D
DDR2_DIMM_DM[2]	146	DDR_PDM2	22-9D
DDR2_DIMM_DM[1]	134	DDR_PDM1	22-9D
DDR2_DIMM_DM[0]	125	DDR_PDM0	22-9D

DDR2_DIMM_DQS_CB_P	46	DDR_PDQS8	22-8D
DDR2_DIMM_DQS_CB_N	45	NC	
DDR2_DIMM_DQS_P[7]	114	DDR_PDQS7	22-8D
DDR2_DIMM_DQS_N[7]	113	NC	
DDR2_DIMM_DQS_P[6]	105	DDR_PDQS6	22-8D
DDR2_DIMM_DQS_N[6]	104	NC	
DDR2_DIMM_DQS_P[5]	93	DDR_PDQS5	22-8D
DDR2_DIMM_DQS_N[5]	92	NC	
DDR2_DIMM_DQS_P[4]	84	DDR_PDQS4	22-8D
DDR2_DIMM_DQS_N[4]	83	NC	
DDR2_DIMM_DQS_P[3]	37	DDR_PDQS3	22-8D
DDR2_DIMM_DQS_N[3]	36	NC	
DDR2_DIMM_DQS_P[2]	28	DDR_PDQS2	22-8D
DDR2_DIMM_DQS_N[2]	27	NC	
DDR2_DIMM_DQS_P[1]	16	DDR_PDQS1	22-8D
DDR2_DIMM_DQS_N[1]	15	NC	
DDR2_DIMM_DQS_P[0]	7	DDR_PDQS0	22-8D
DDR2_DIMM_DQS_N[0]	6	NC	

DDR2_DIMM_WE#	73	DDR_PWE#	22-7L,22-9D
DDR2_DIMM_ODT[1]	77	DDR_PODT1	
DDR2_DIMM_ODT[0]	195	DDR_PODT0	

R226 47R 4K7

DDR2_DIMM_RESET#	18	PPC_DDR2_RESET_N	PPC_DDR2_RESET_N 1-2B,1-2M,24-10F
DDR2_DIMM_S#[1]	76	DDR_PCS1#	22-7L,22-8D
DDR2_DIMM_S#[0]	193	DDR_PCS0#	22-7L,22-8D

PAR_OUT	55	PPC_DDR2_ERROR	1 TP4
PAR_IN	68	PAR_IN	1 TP5

VTT ISLAND WITH DECOUPLING AND TERMINATION IN COMPACT ARRANGEMENT

DDR_VTT

DDR_PCKE	22-6K,22-8D	RP24	CP26
DDR_PA15			
DDR_PA14			
DDR_PBA1	22-8K,22-9D		
DDR_PA12		RP23	CP28
DDR_PA11			
DDR_PA9			
NC			
DDR_PA7		RP22	CP29
DDR_PA8			
DDR_PA6			
DDR_PA5			
DDR_PA4		RP21	CP30
DDR_PA3			
DDR_PA1			
DDR_PA2			
DDR_PA0		RP25	CP32
DDR_PBA2	22-8K,22-9D		
DDR_PA10			
DDR_PBA0	22-8K,22-9D		
DDR_PRAS#	22-7K,22-9D	RP26	CP31
DDR_PWE#	22-3K,22-9D		
DDR_PCS0#	22-3K,22-9D		
DDR_PCAS#	22-8K,22-9D		
DDR_PCS1#	22-3K,22-8D	RP19	CP33
DDR_PODT0	22-9D		
DDR_PA13			
DDR_PODT1	22-8D		

GND

J8

VSS_64	237		
VSS_63	234		
VSS_62	231		
VSS_61	228		
VSS_60	225		
VSS_59	222		
VSS_58	219		
VSS_57	216		
VSS_56	213		
VSS_55	210		
VSS_54	207		
VSS_53	204		
VSS_52	201		
VSS_51	198		
VSS_50	169		
VSS_49	166		
VSS_48	163		
VSS_47	160		
VSS_46	157		
VSS_45	154		
VSS_44	151		
VSS_43	148		
VSS_42	145		
VSS_41	142		
VSS_40	139		
VSS_39	136		
VSS_38	133		
VSS_37	130		
VSS_36	127		
VSS_35	124		
VSS_34	121		
VSS_33	118		
VSS_32	115		
VSS_31	112		
VSS_30	109		
VSS_29	106		
VSS_28	103		
VSS_27	100		
VSS_26	97		
VSS_25	94		
VSS_24	91		
VSS_23	88		
VSS_22	85		
VSS_21	82		
VSS_20	79		
VSS_19	66		
VSS_18	65		
VSS_17	50		
VSS_16	47		
VSS_15	44		
VSS_14	41		
VSS_13	38		
VSS_12	35		
VSS_11	32		
VSS_10	29		
VSS_9	26		
VSS_8	23		
VSS_7	20		
VSS_6	17		
VSS_5	14		
VSS_4	11		
VSS_3	8		
VSS_2	5		
VSS_1	2		

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DDR_VREF_0V9

3V3

1V8

VREF	1		
VDDSPD	238		
VDD_11	197	VDDQ_11	194
VDD_10	189	VDDQ_10	191
VDD_9	187	VDDQ_9	181
VDD_8	184	VDDQ_8	175
VDD_7	178	VDDQ_7	170
VDD_6	172	VDDQ_6	78
VDD_5	69	VDDQ_5	75
VDD_4	67	VDDQ_4	72
VDD_3	64	VDDQ_3	62
VDD_2	59	VDDQ_2	56
VDD_1	53	VDDQ_1	51

GND

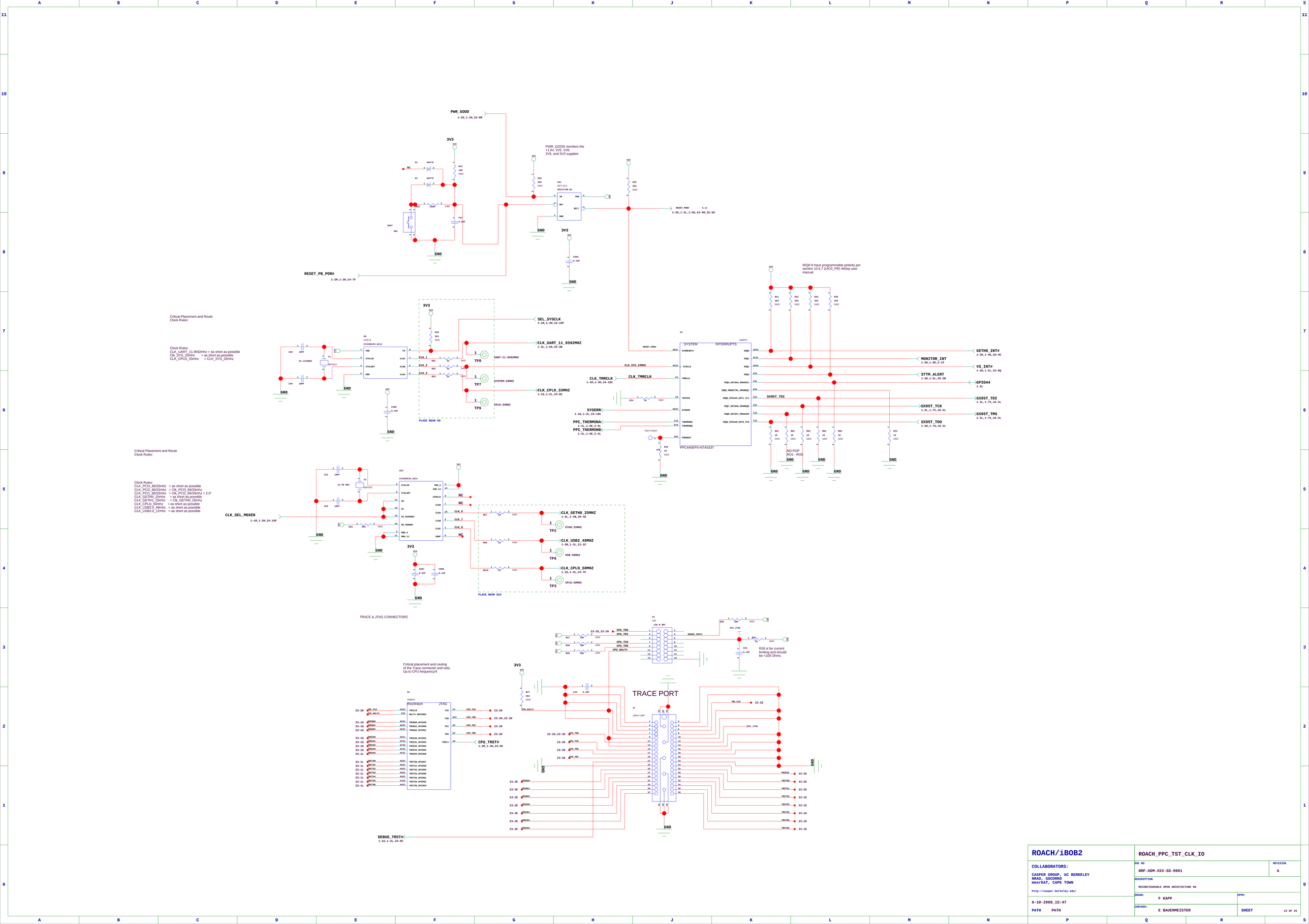
DDR_VREF_0V9

1V8

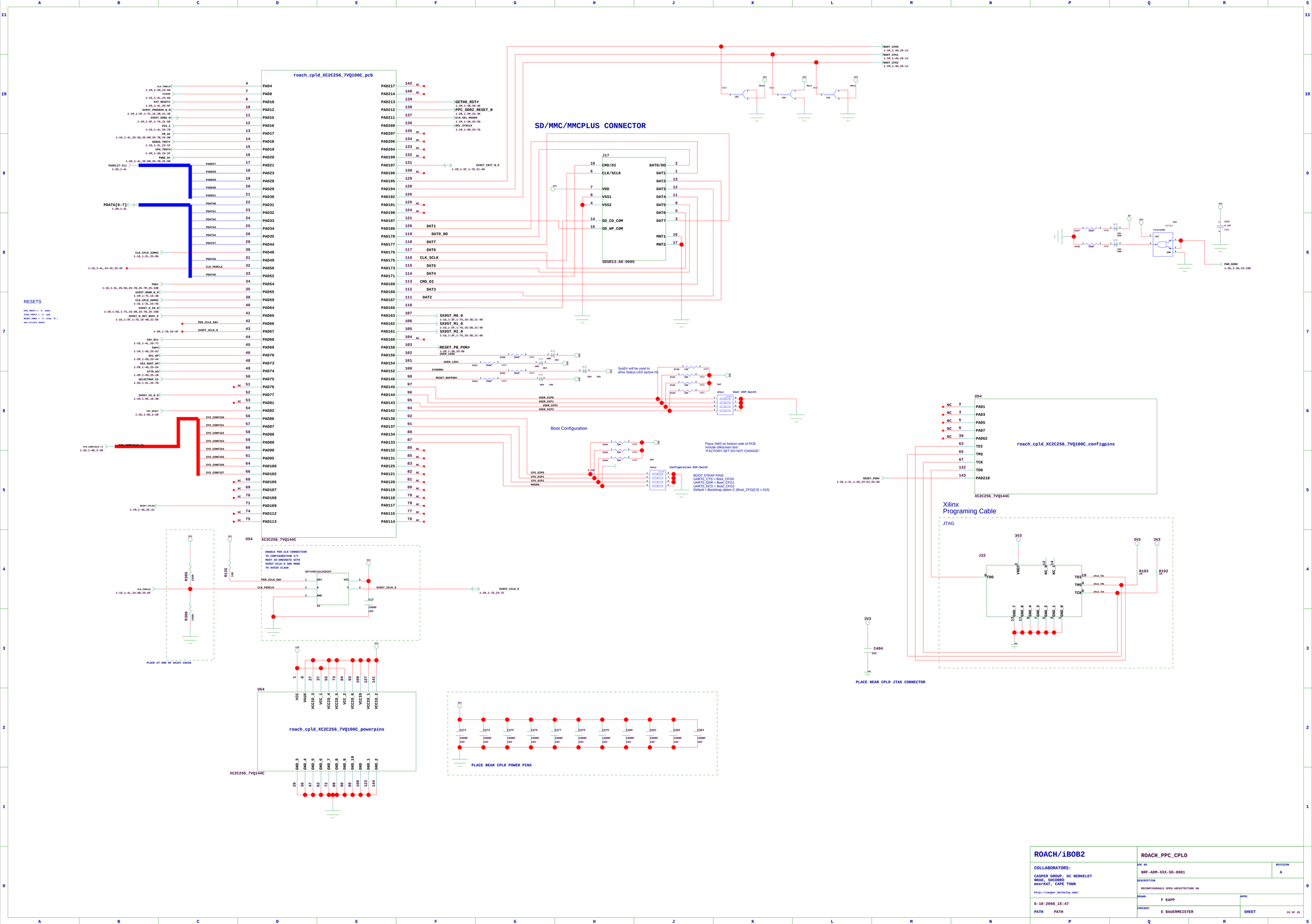
C432	100NF	10V	
C433	10NF	25V	
C454	100NF	10V	
C434	10NF	25V	
C430	100NF	10V	
C443	10NF	25V	
C431	100NF	10V	
C444	10NF	25V	
C436	100NF	10V	
C445	10NF	25V	
C435	100NF	10V	
C446	10NF	25V	
C438	100NF	10V	
C451	10NF	25V	
C437	100NF	10V	
C452	10NF	25V	
C439	100NF	10V	
C449	10NF	25V	
C440	100NF	10V	
C450	10NF	25V	
C441	100NF	10V	
C448	10NF	25V	
C442	100NF	10V	
C447	10NF	25V	

PLACE NEAREST DDR2 MODULE PINS

ROACH/iBOB2	ROACH_PPC_DDR2
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-10-2008_15:47	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 22 OF 25



ROACH/iBOB2	**ROACH_PPC_TST_CLK_IO**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-10-2008_15:47	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 23 OF 25



ROACH/iBOB2	**ROACH_PPC_CPLD**
COLLABORATORS: CASPER GROUP, UC BERKELEY NRAO, SOCORRO meerKAT, CAPE TOWN http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001 — REVISION: A
	DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-10-2008_15:47	DRAWN: F KAPP — APPR:
PATH PATH	CHECKED: E BAUERMEISTER — SHEET 24 OF 25

PADD30 IS THE LSB FOR 16 BIT
WIDE BUS TRANSFERS

NOTE:
DMA SIGNALS
IN GREEN TEXT

PADD2 IS THE MSB

PADD[2:31]

CHIP SELECTS CONFIG	
CS0	NOR FLASH - U42
CS1	FPGA - U15
CS2	CPLD - U54
CS3	FPGA - U15
CS4	SELECTMAP_CS
CS5	GPIO - SX95_D_IN

ROUTE AS DAISY CHAIN - U1 - U15 - U52 - TERMINATION
KEEP STUBS AS SHORT AS POSSIBLE

ROACH/iBOB2	ROACH_PPC_NVM_SERIAL
COLLABORATORS: CASPER GROUP, UC BERKELEY; NRAO, SOCORRO; meerKAT, CAPE TOWN; http://casper.berkeley.edu/	DOC NO: NRF-ADM-XXX-SD-0001; REVISION: A; DESCRIPTION: RECONFIGURABLE OPEN ARCHITECTURE HW
6-10-2008_15:47	DRAWN: F KAPP; APPR:
PATH PATH	CHECKED: E BAUERMEISTER; SHEET 25 OF 25