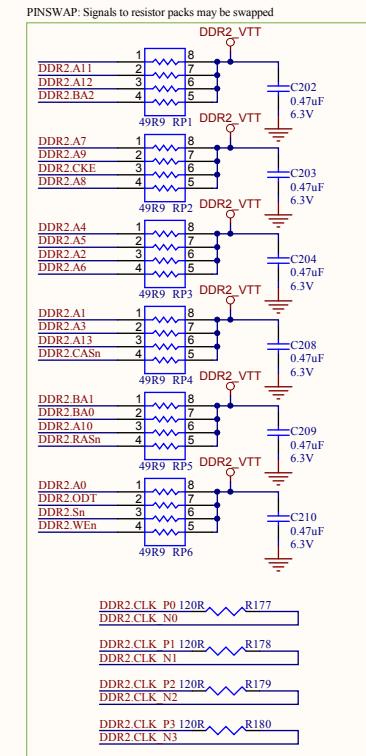
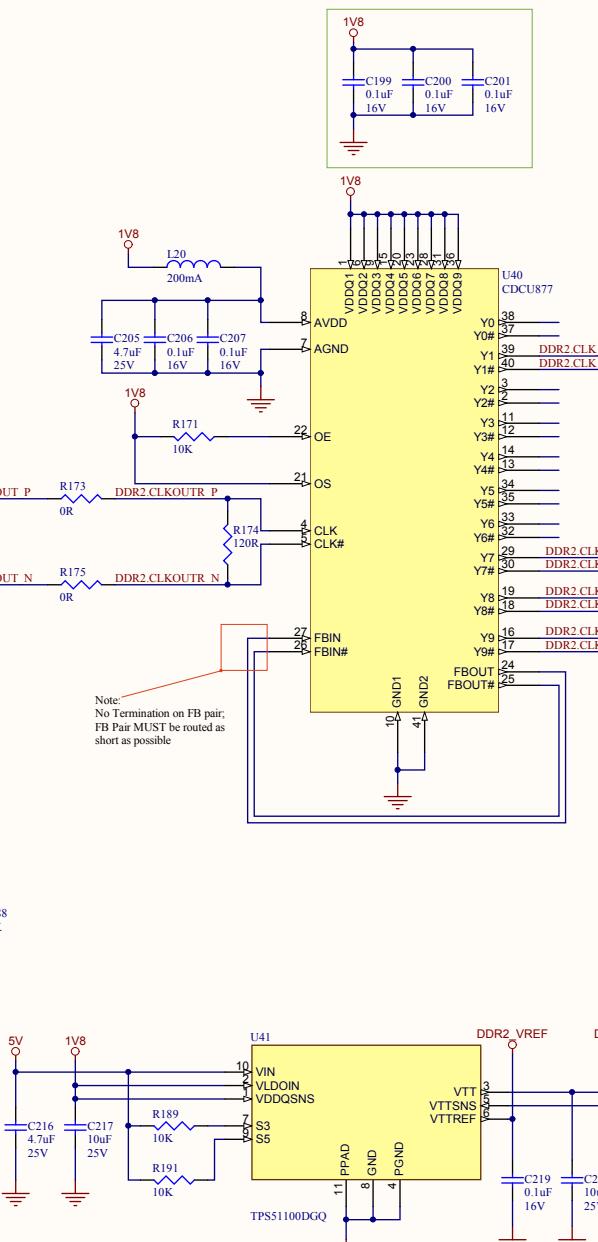
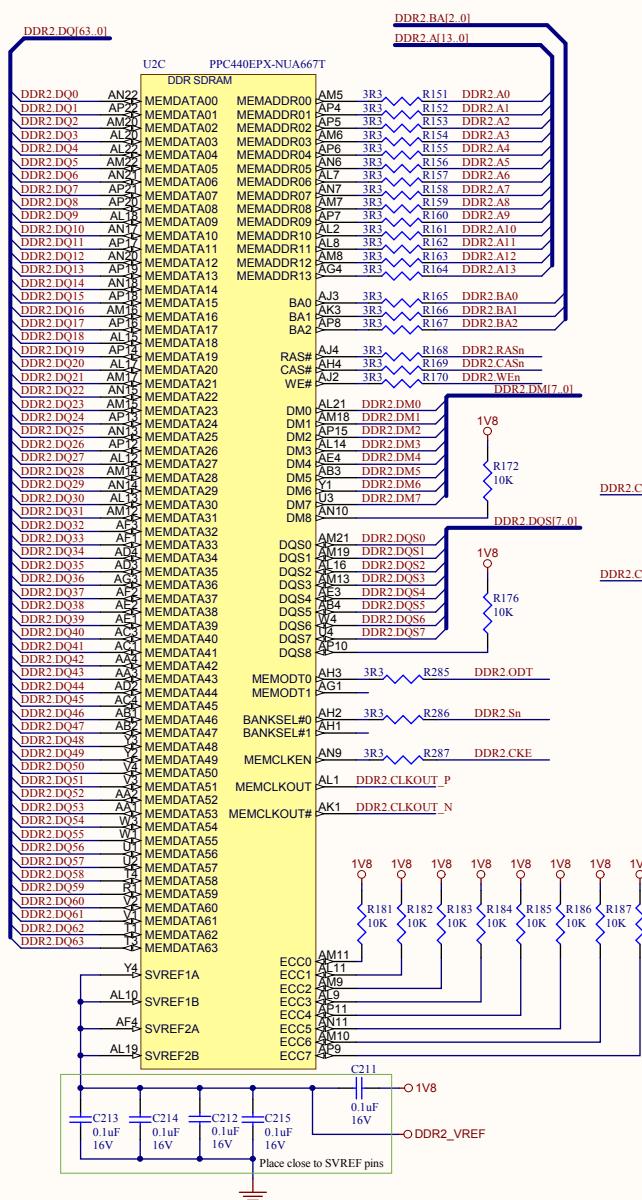
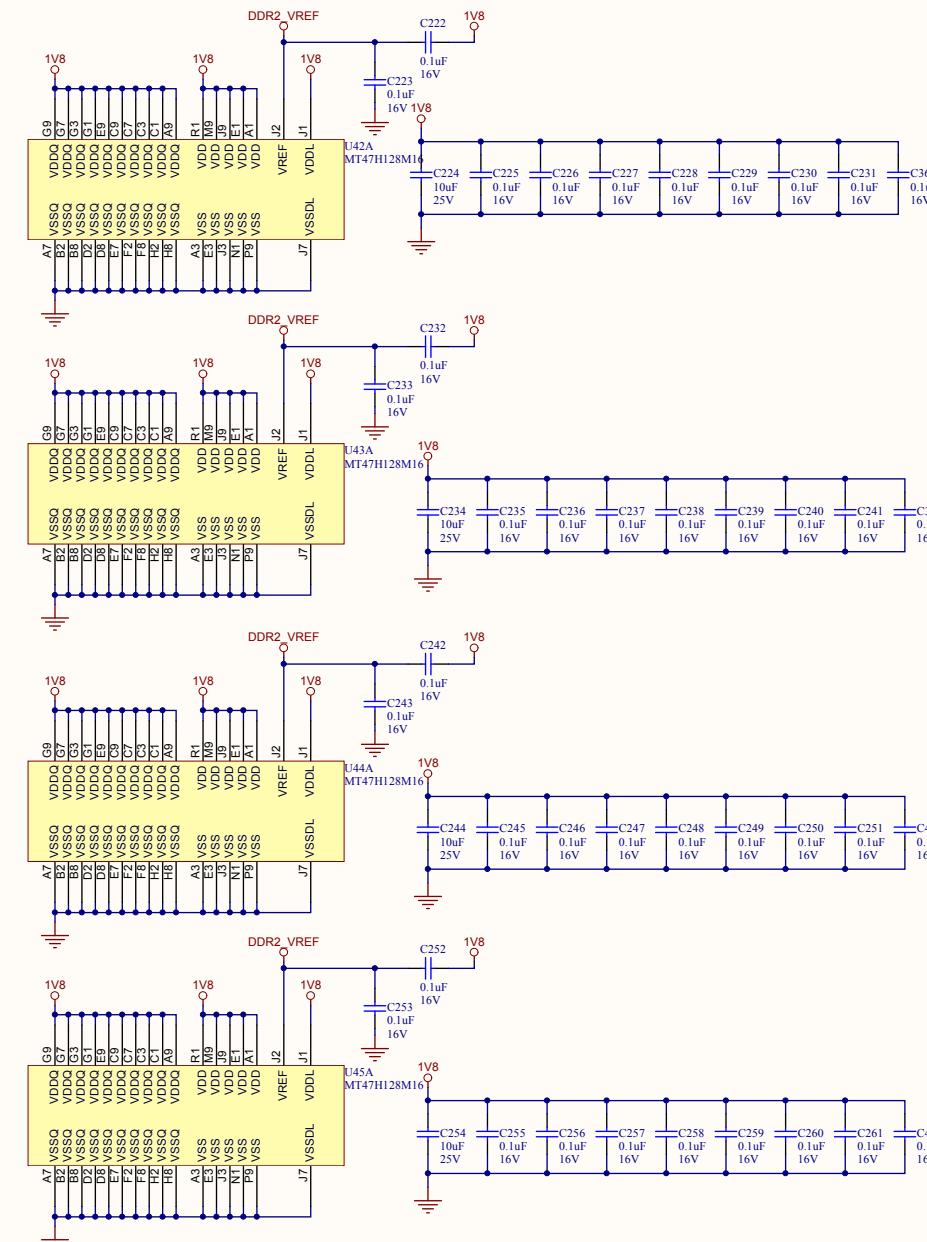
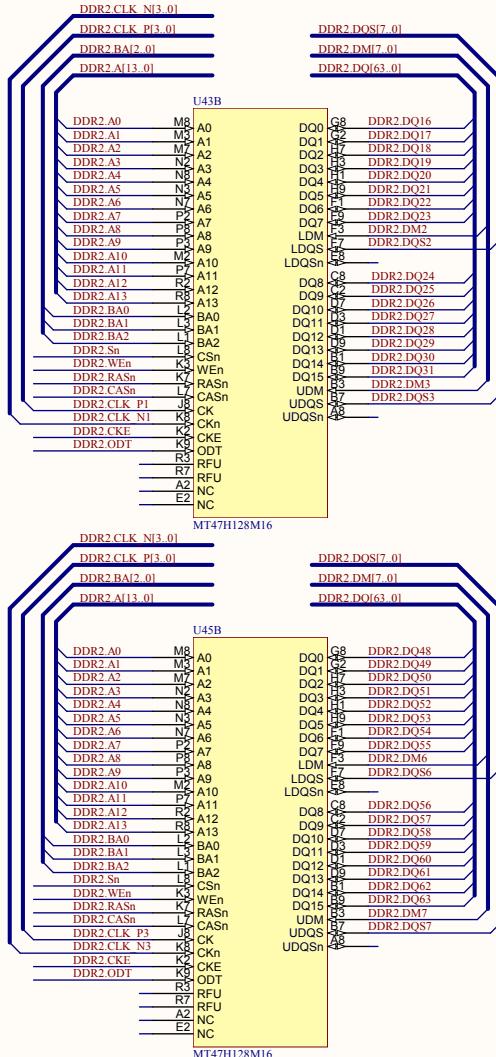
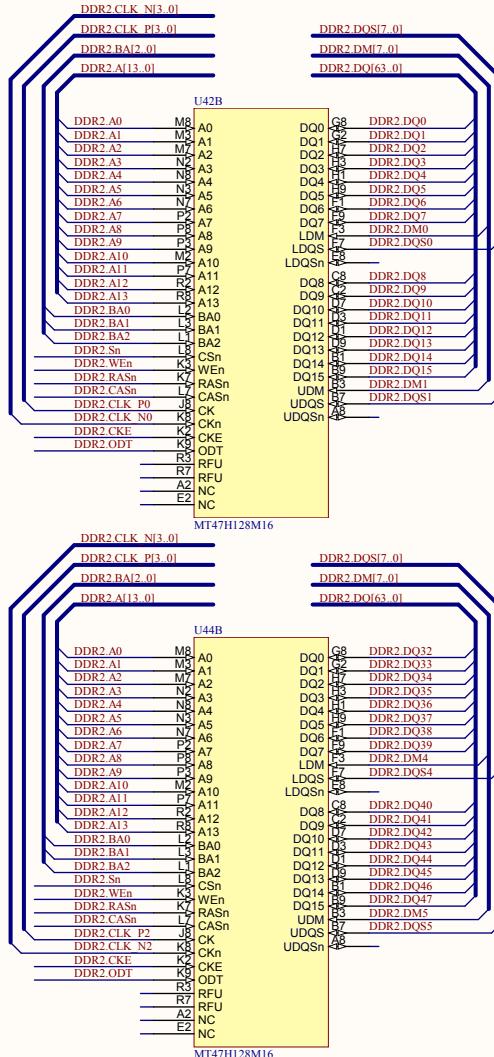


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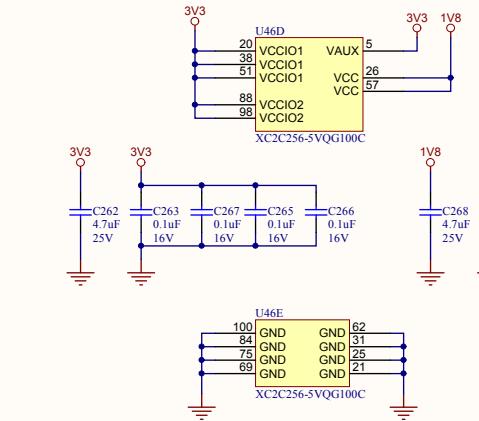
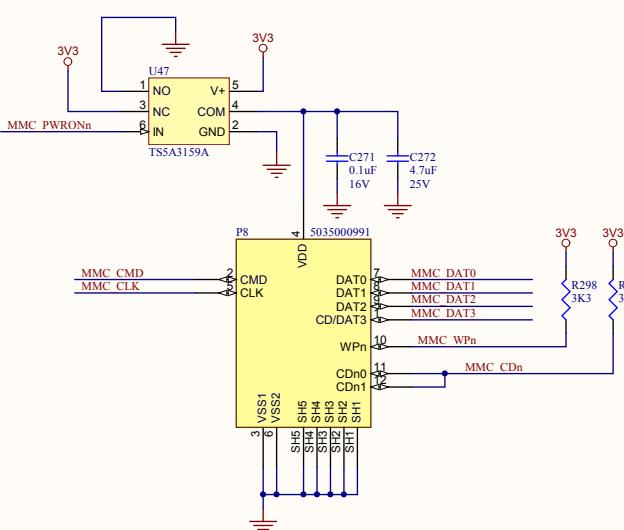
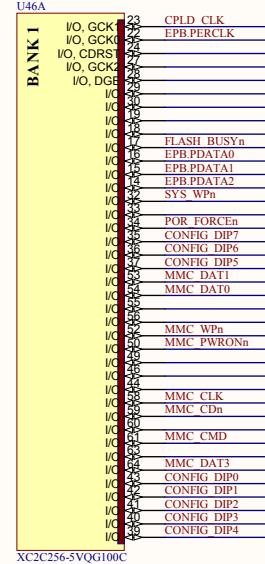
Note: No Termination on FB pair
FB Pair MUST be routed as short as possible

DDR2_D0[63..0]	DDR2
DDR2_DM[7..0]	DQ[63..0]
DDR2_DS[7..0]	DM[7..0]
DDR2_A1[3..0]	DQS[7..0]
DDR2_BA[2..0]	AI[3..0]
DDR2_Sn	BA[2..0]
DDR2_CSn	Sa
DDR2_WEn	CSn
DDR2_WEn	RASn
DDR2_ODT	WEn
DDR2_CKE	OT
DDR2_CLK_P1[3..0]	CKE
DDR2_CLK_N1[3..0]	PL[3..0]
DDR2_CLK_N1[3..0]	CLK_N[3..0]

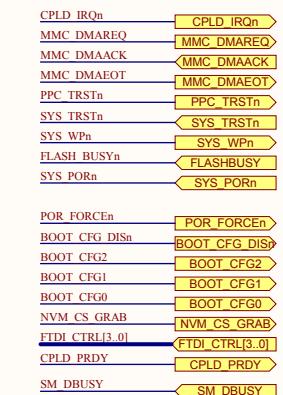
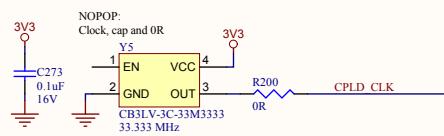
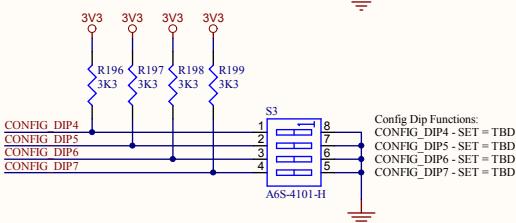
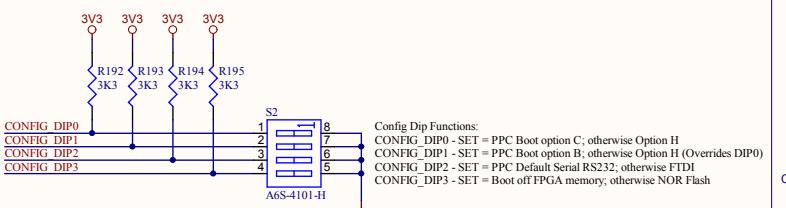
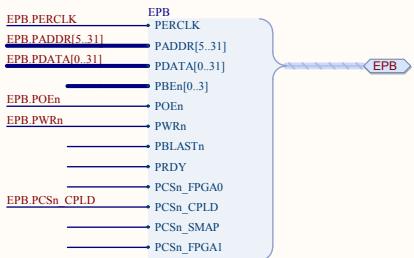
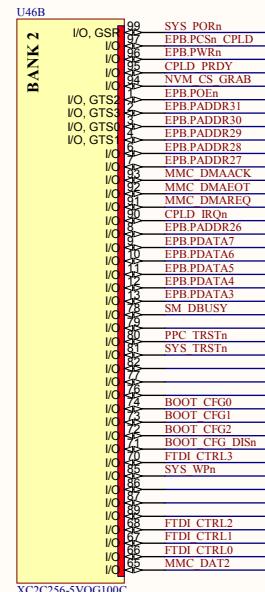
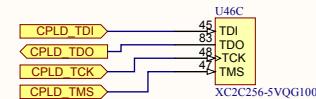


DDR2 Address	DDR2 Chip	Address Inputs
D63_0	DDR2_0	A13_0, A12_0, BA2_0, CSn
D62_0	DDR2_0	A13_0, A12_0, BA2_0, CSn
D61_0	DDR2_0	A13_0, A12_0, BA2_0, CSn
D60_0	DDR2_0	A13_0, A12_0, BA2_0, CSn
D59_0	DDR2_1	A13_0, A12_0, BA2_0, CSn
D58_0	DDR2_1	A13_0, A12_0, BA2_0, CSn
D57_0	DDR2_1	A13_0, A12_0, BA2_0, CSn
D56_0	DDR2_1	A13_0, A12_0, BA2_0, CSn
D55_0	DDR2_2	A13_0, A12_0, BA2_0, CSn
D54_0	DDR2_2	A13_0, A12_0, BA2_0, CSn
D53_0	DDR2_2	A13_0, A12_0, BA2_0, CSn
D52_0	DDR2_2	A13_0, A12_0, BA2_0, CSn
D51_0	DDR2_3	A13_0, A12_0, BA2_0, CSn
D50_0	DDR2_3	A13_0, A12_0, BA2_0, CSn
D49_0	DDR2_3	A13_0, A12_0, BA2_0, CSn

PINSWAP:
CPLD_CLK and EPB.PERCLK MUST go on GCK pins
SYS_PORn MUST go on GSR pin
EPB.POEn MUST go on GTS pin
Otherwise, swap away



SEQUENCING NOTE:
Xilinx recommends that the IO voltage (3v3) be applied after VCC(1v8).
Too bad.

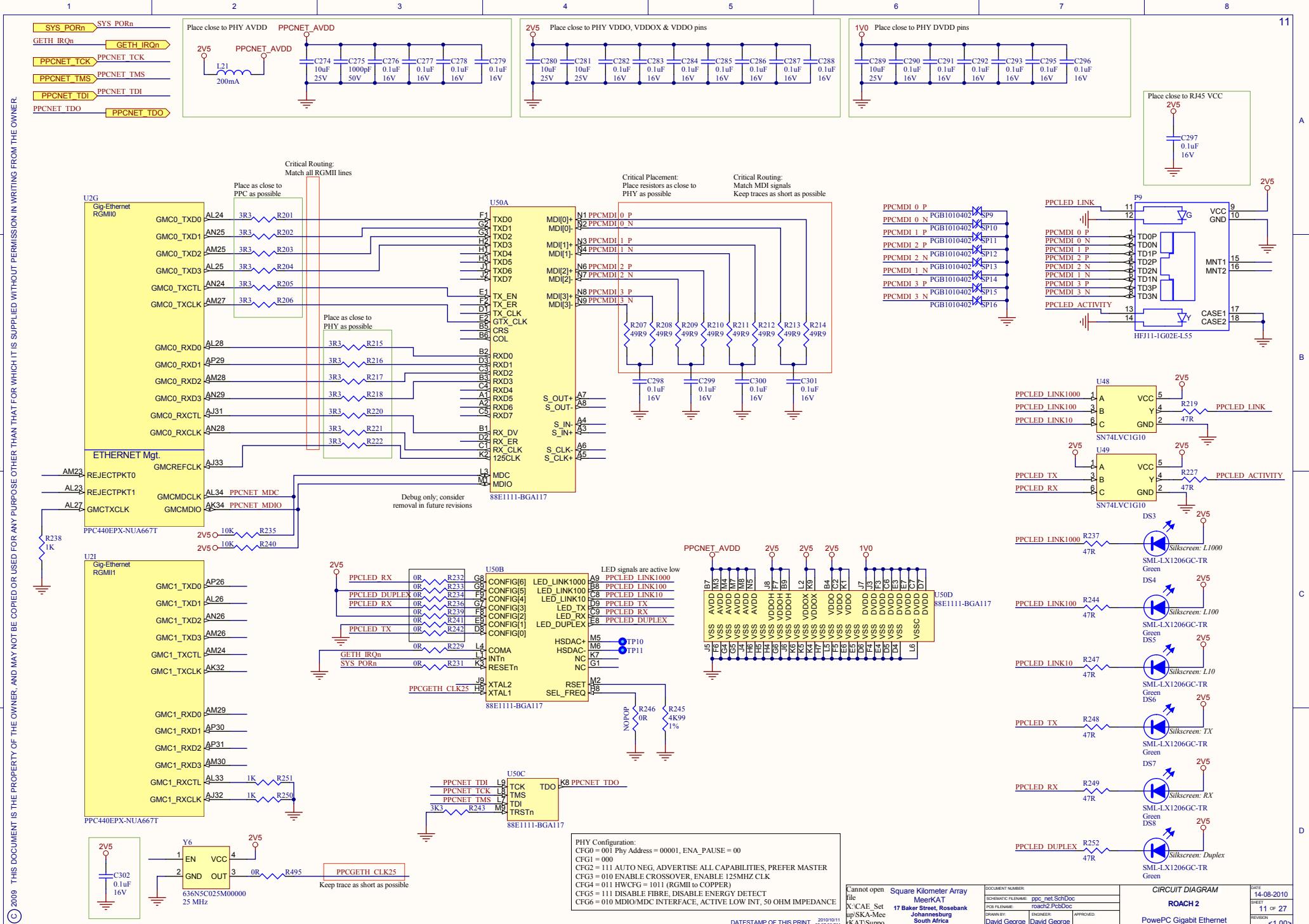


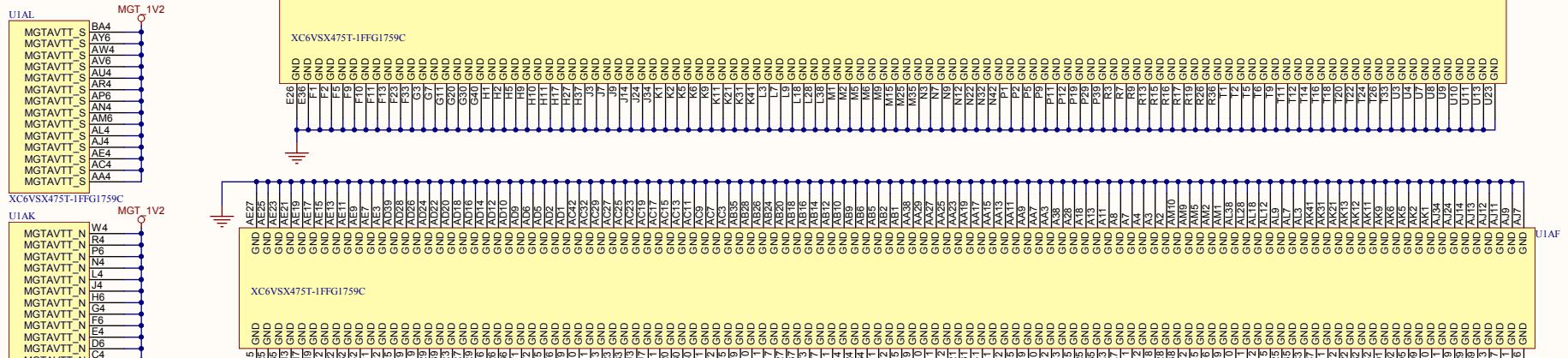
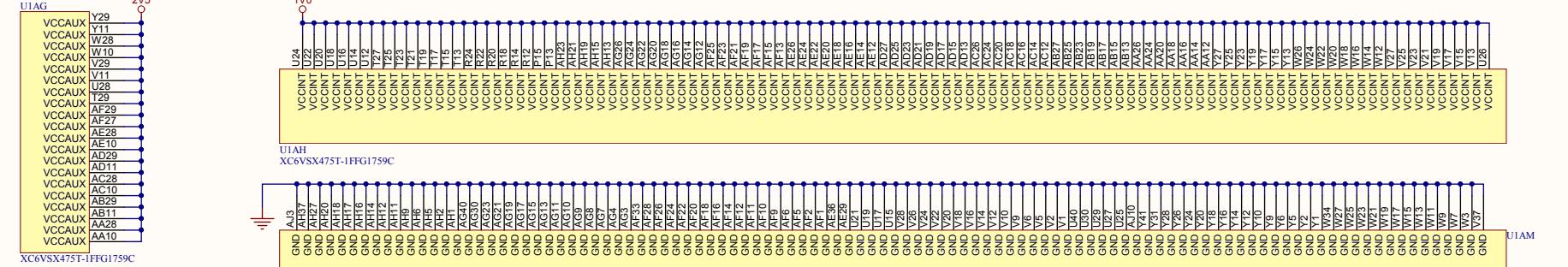
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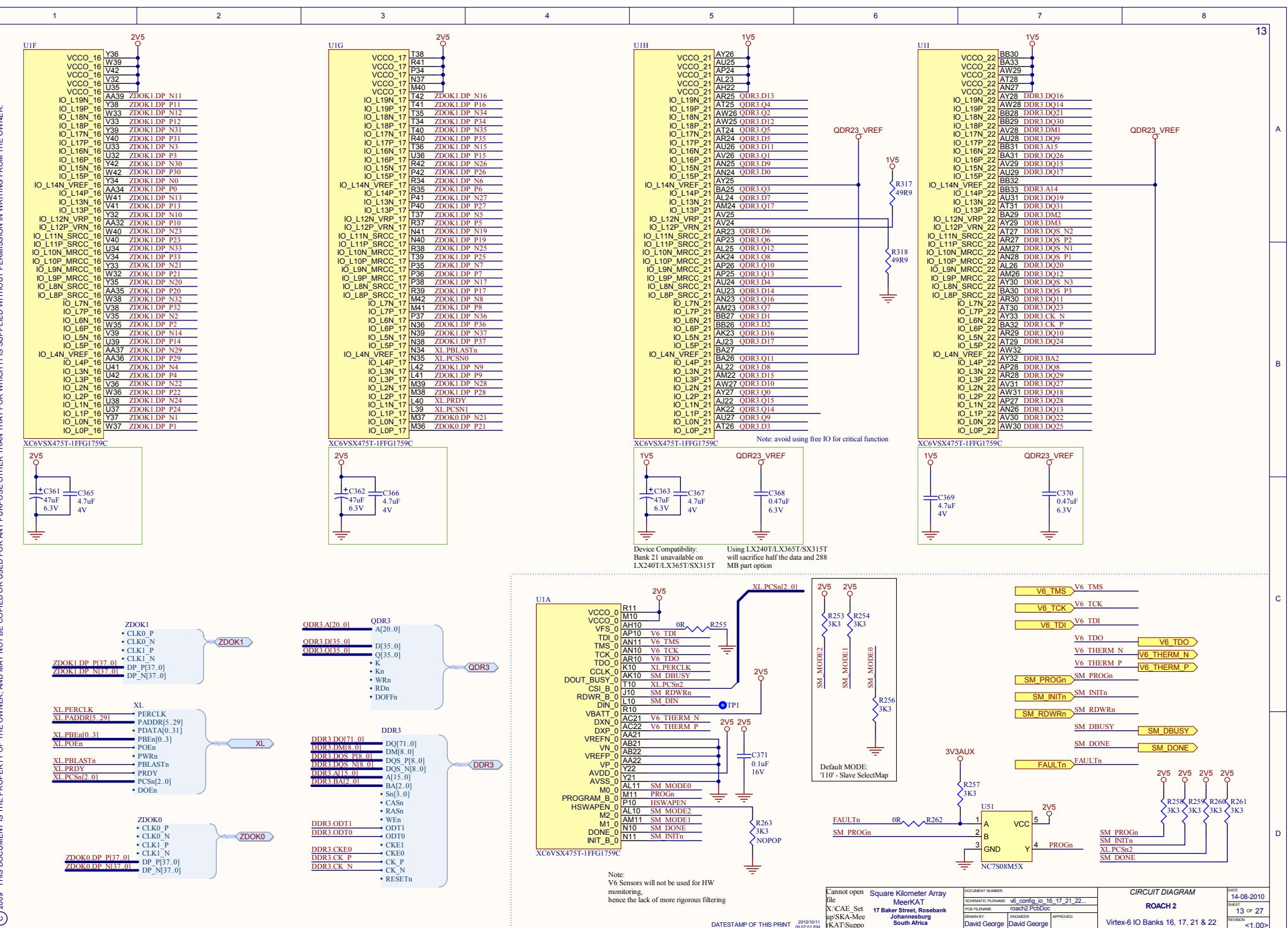
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osebank	SCHEMATIC FILENAME: ppc
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	ENCL: Dav

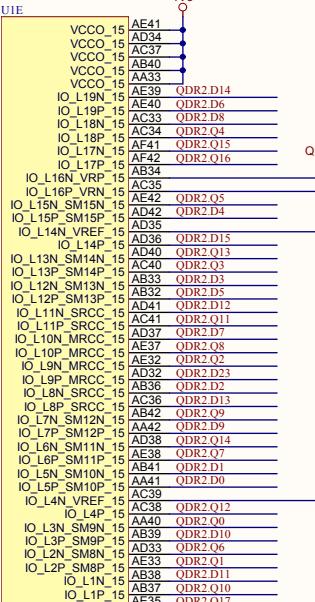
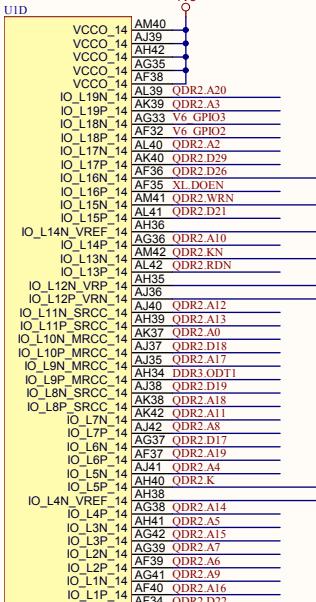
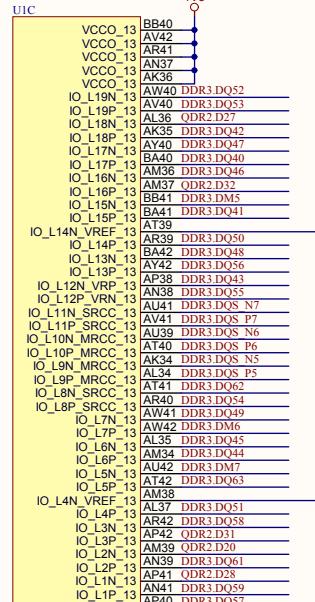
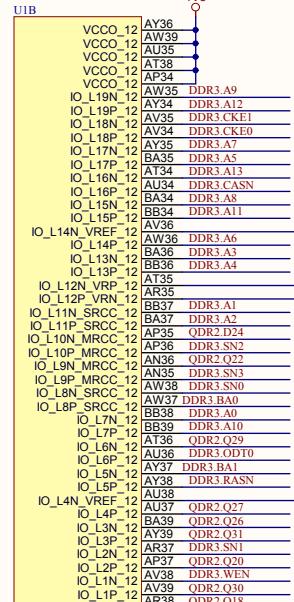
SchDoc		CIRCUIT DIAGRAM
cbDoc		ROACH 2
George	APPROVED:	PowerPC CPLD/MMC

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REVISION
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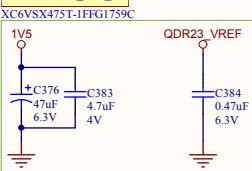
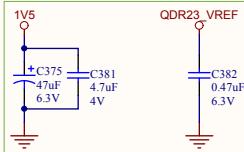
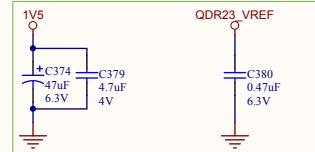
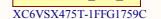
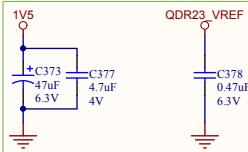








KC6VSX475T-1FFG1759C



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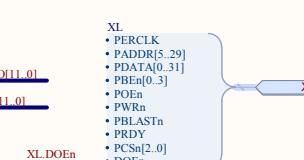
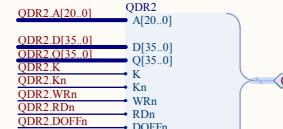
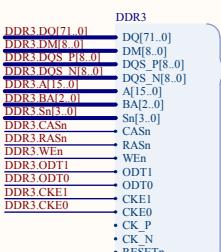
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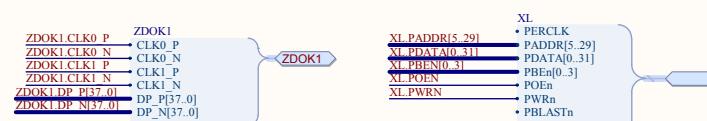
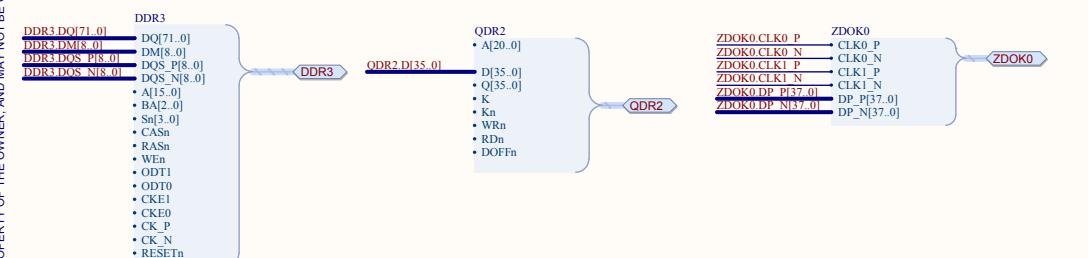
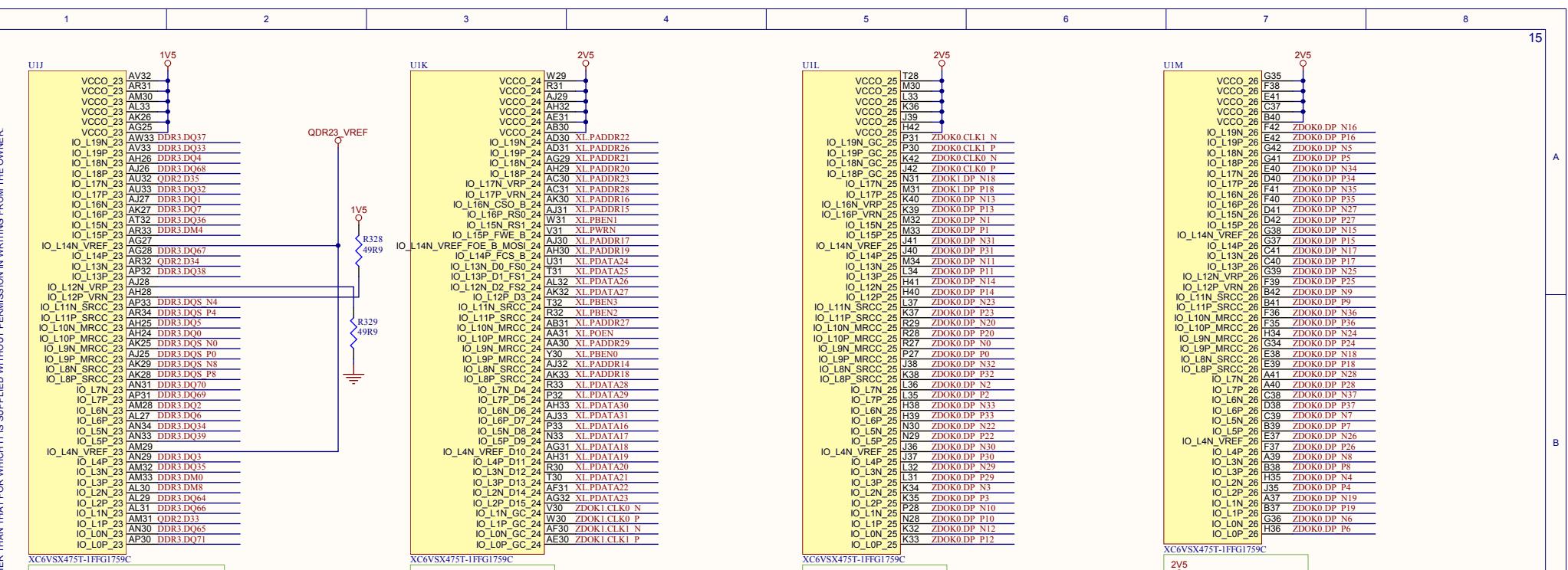
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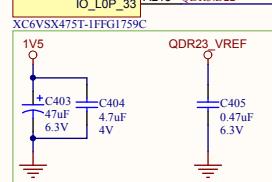
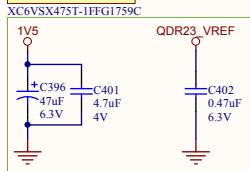
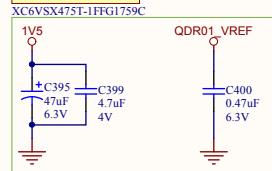
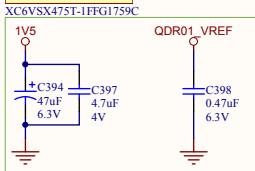
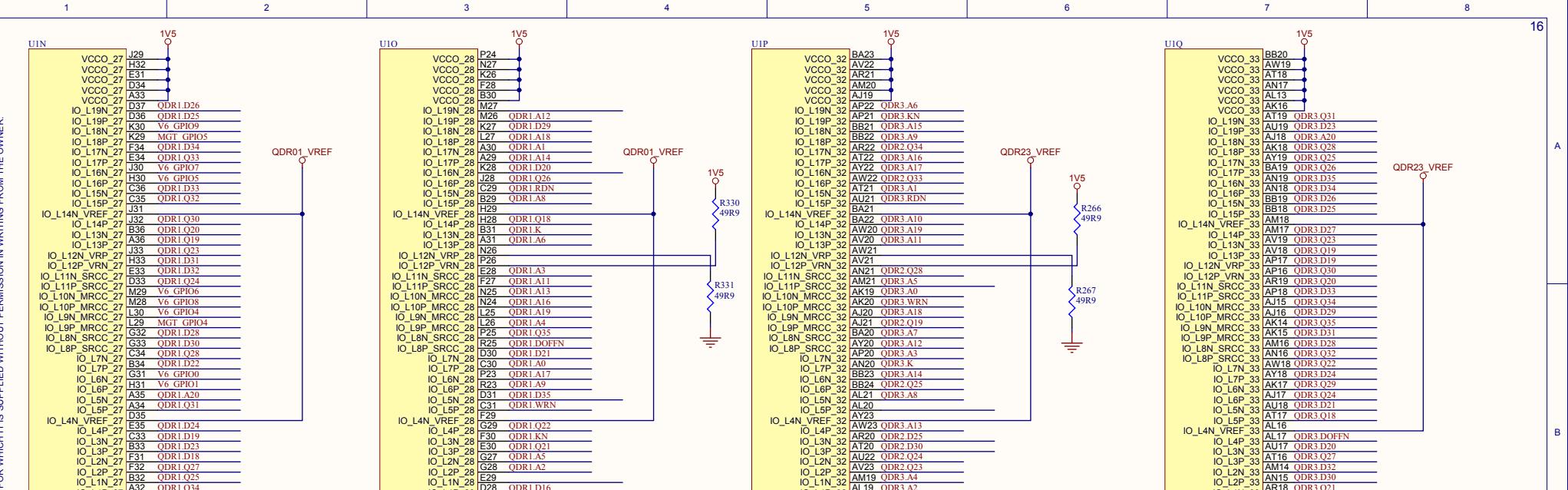
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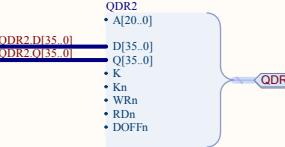
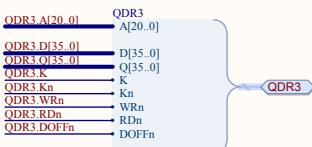
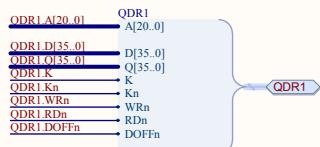
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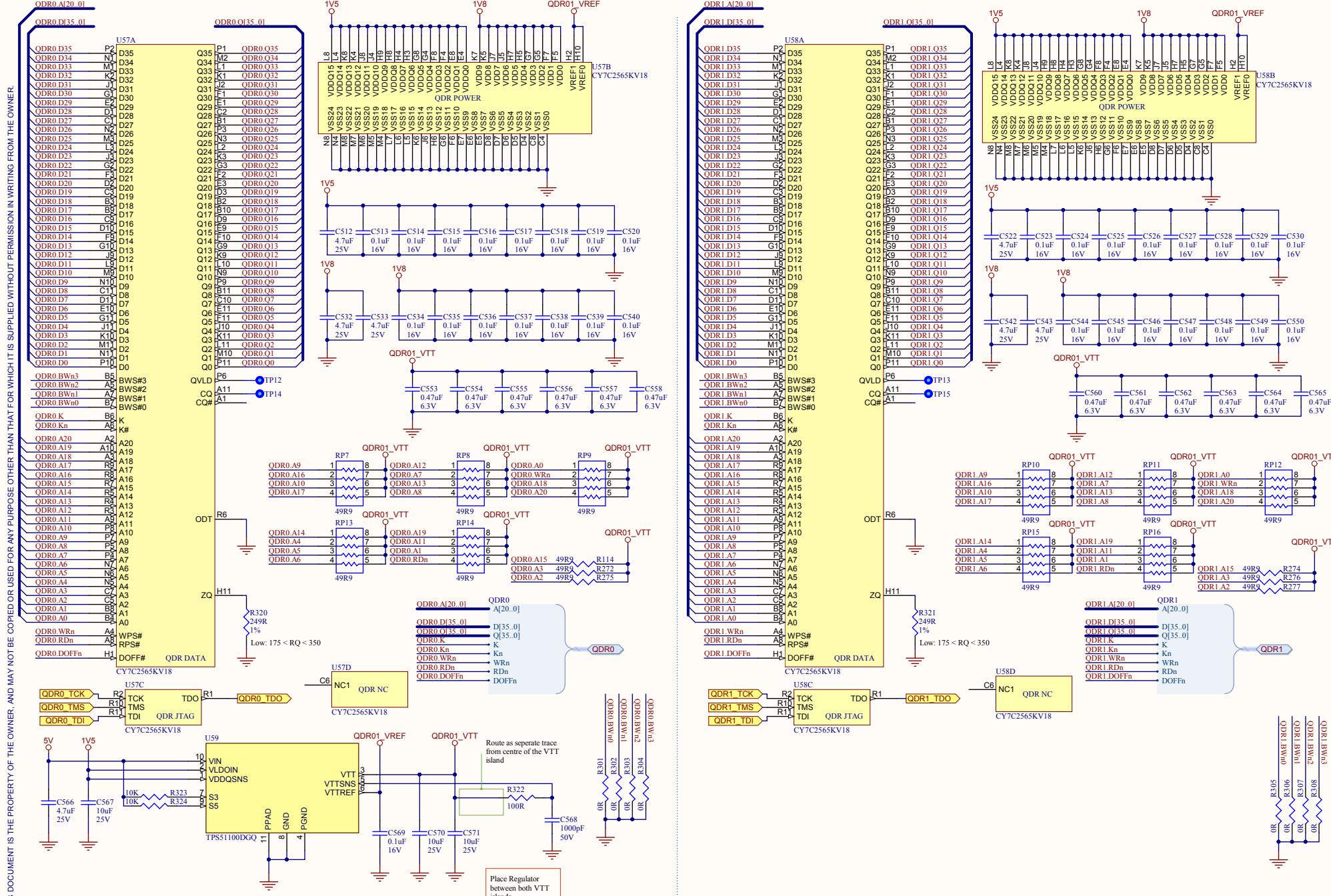


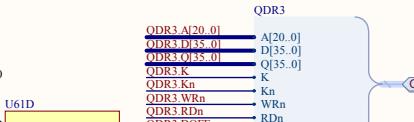
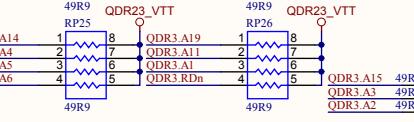
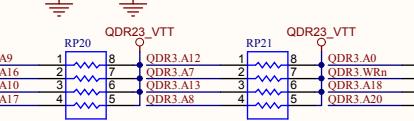
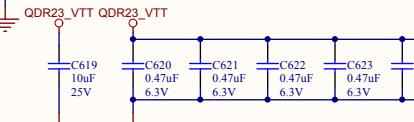
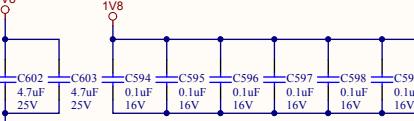
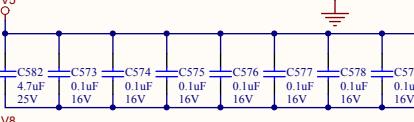
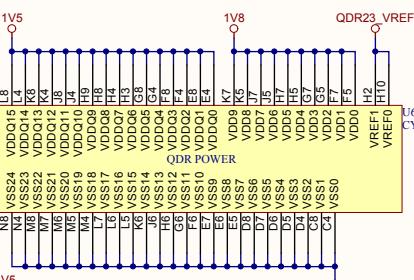
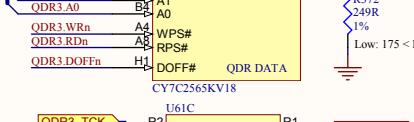
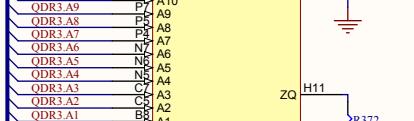
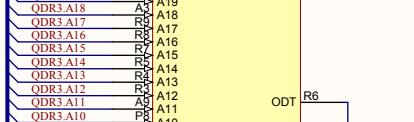
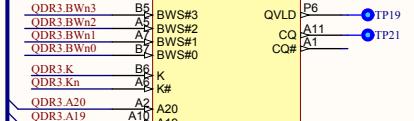
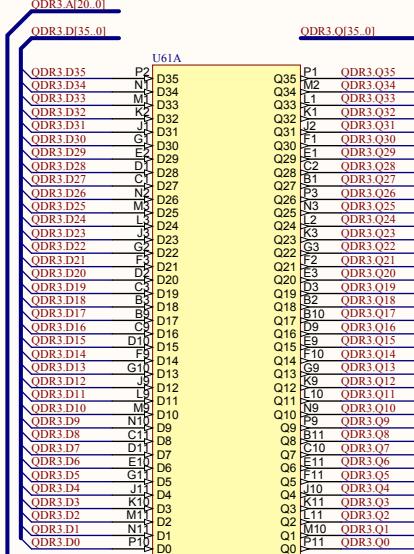
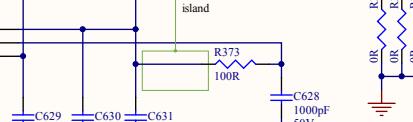
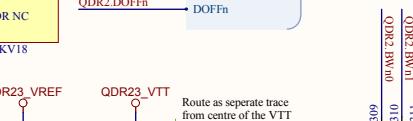
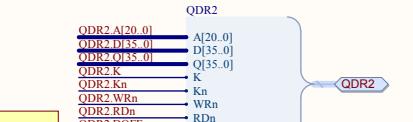
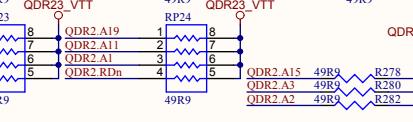
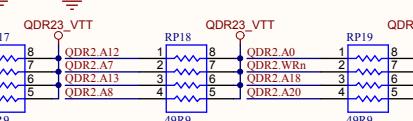
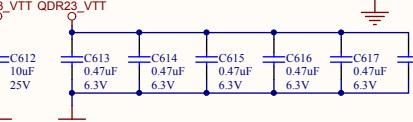
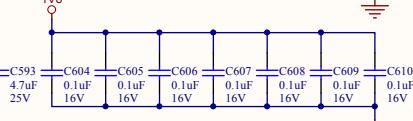
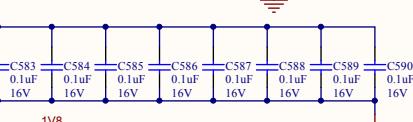
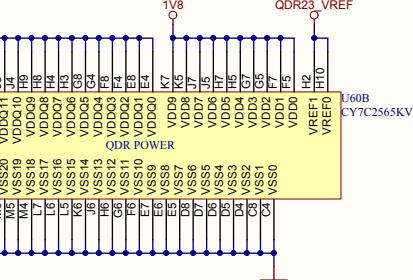
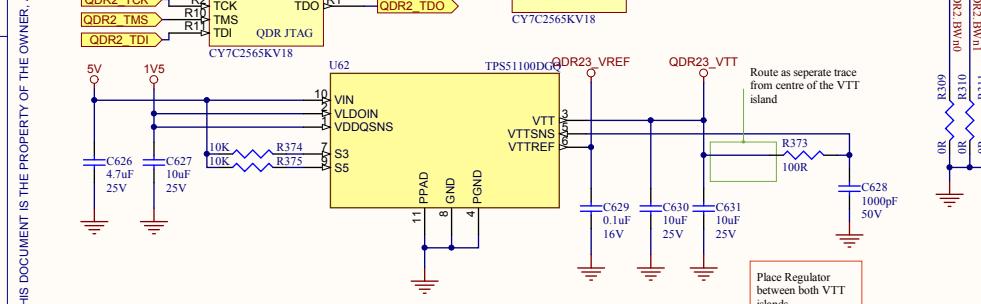
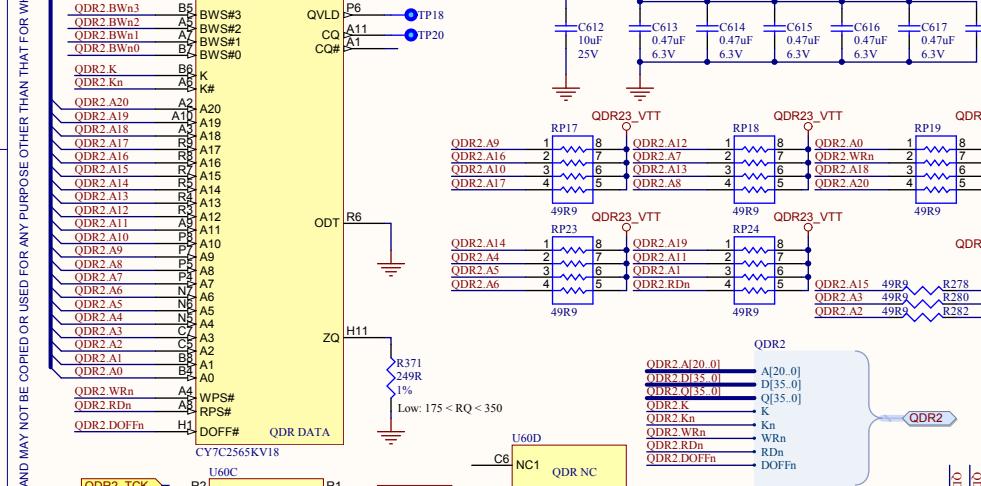
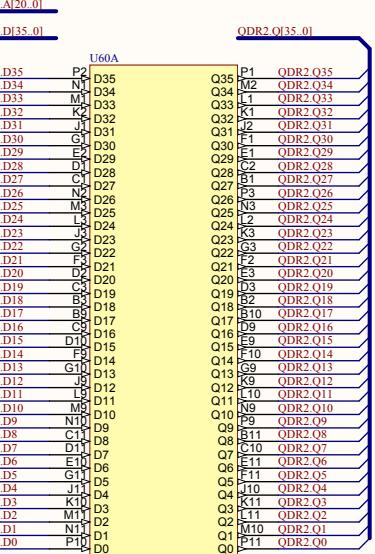




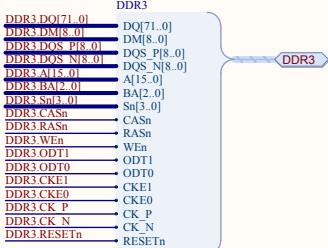
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LX240T/LX365T/SX315T



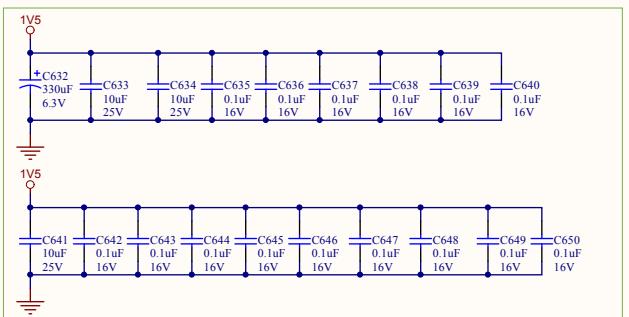




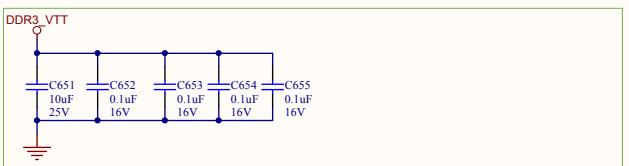
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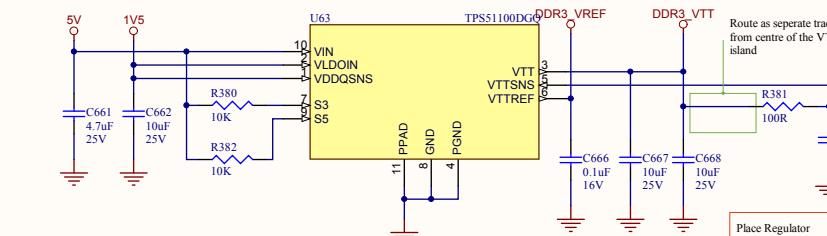
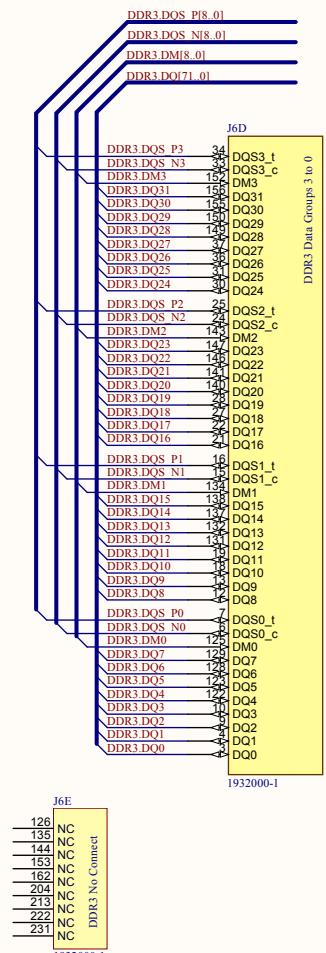
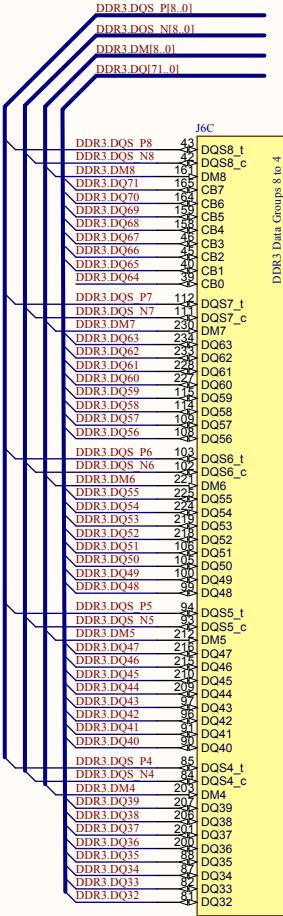
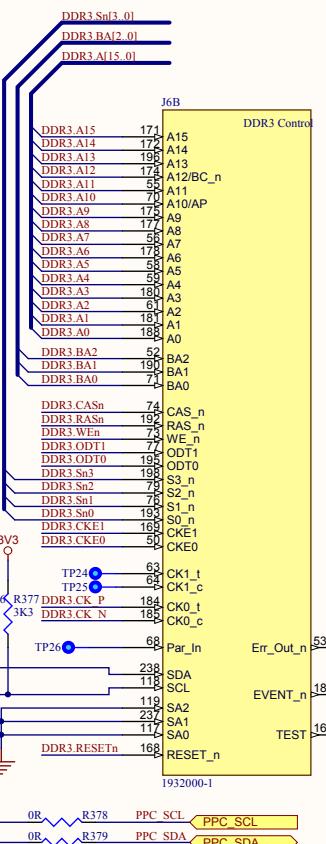
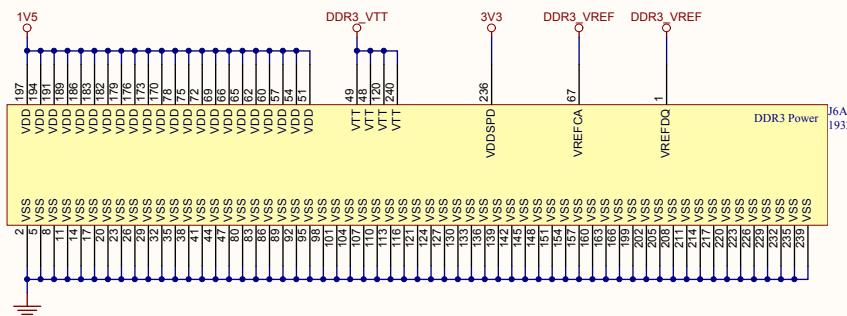
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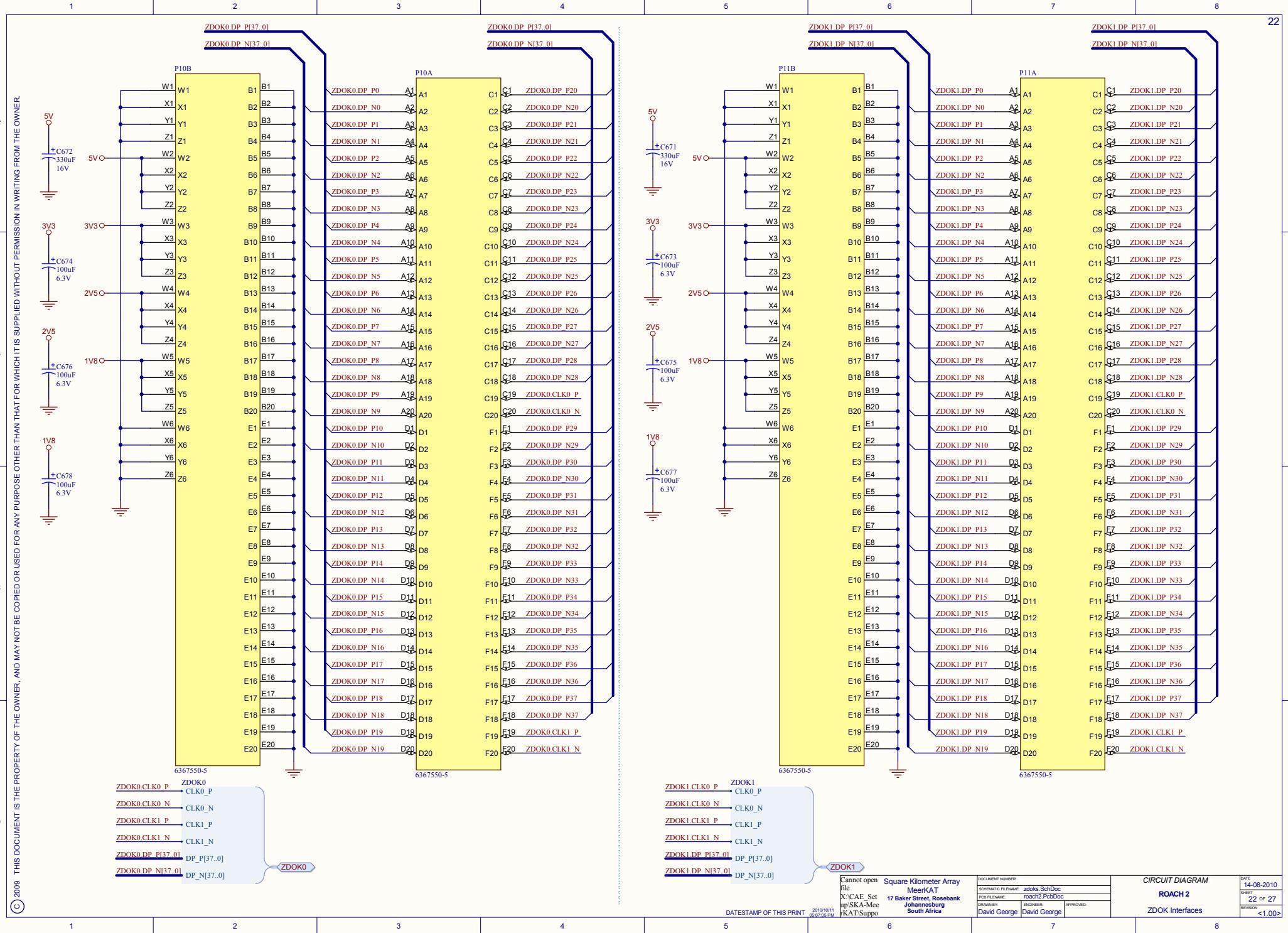
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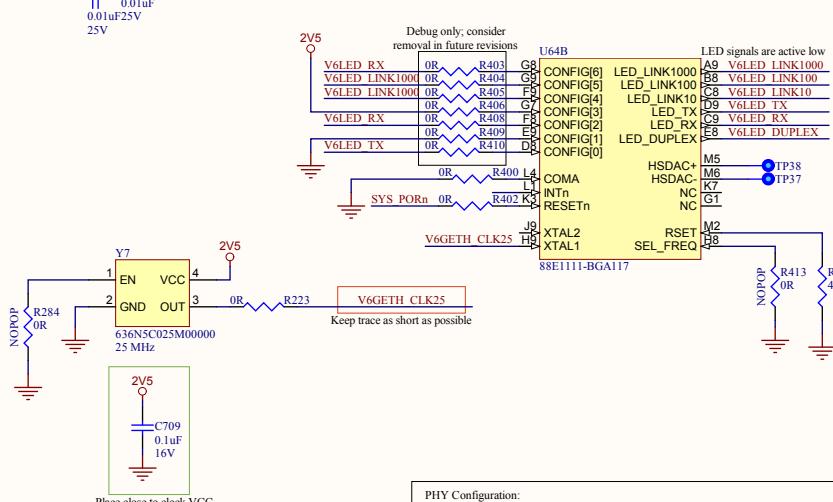
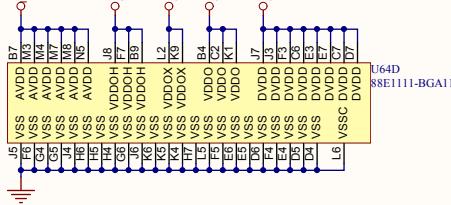
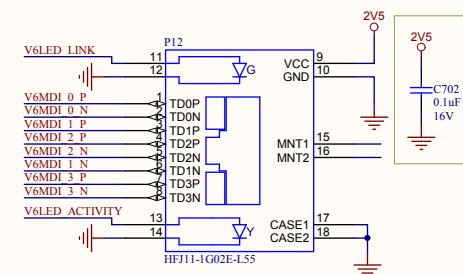
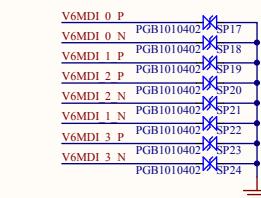
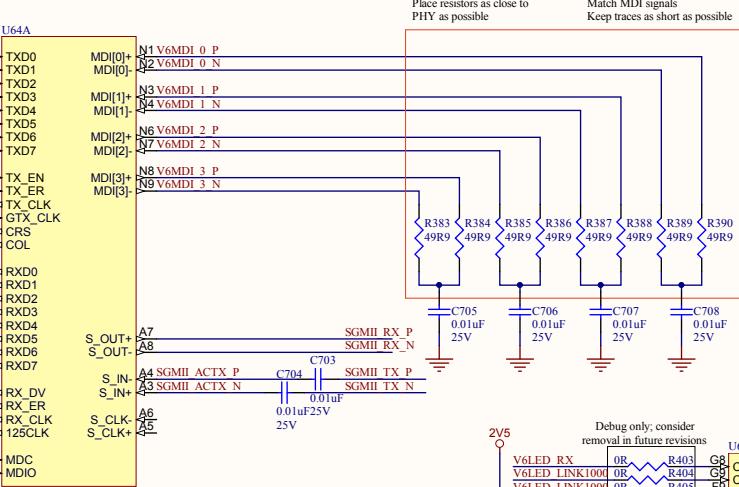
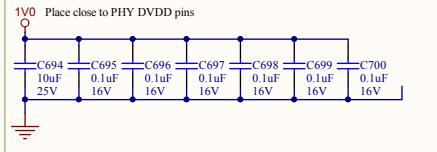
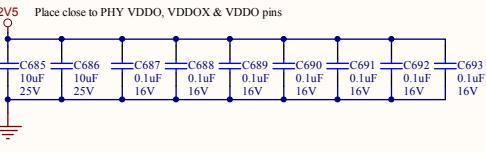
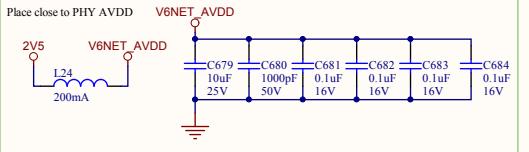
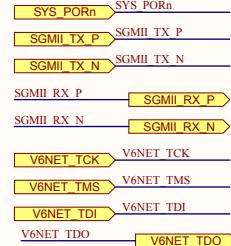


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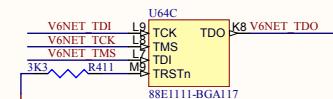


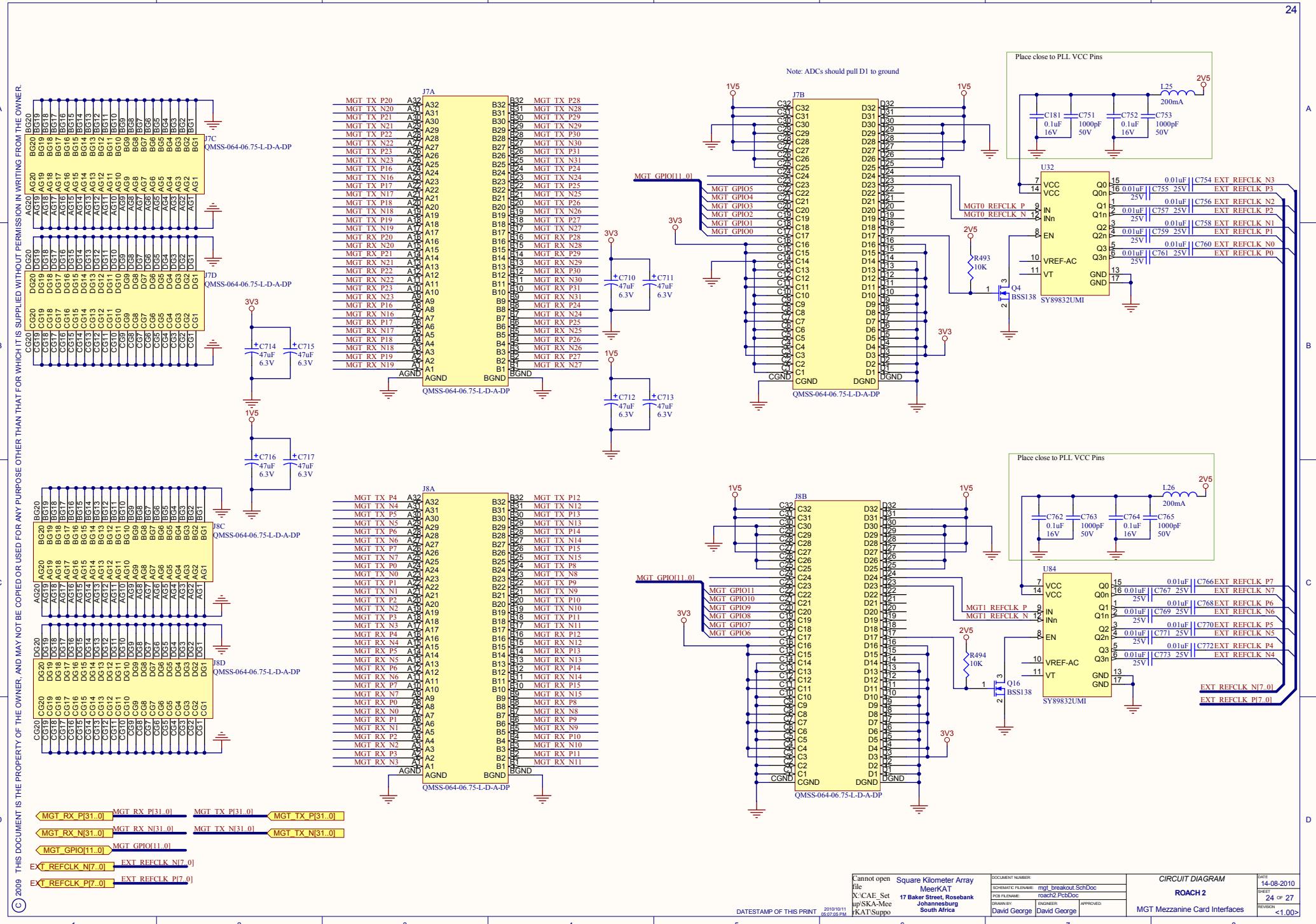
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ROACH 2		14-08-2010
Virtex-6 DDR3 DIMM		SP001
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PCB FILENAME:	roach2.PcbDoc	
DRAWN BY:	David George	
ENGINEER:	David George	
APPROVED:		
DATESTAMP OF THIS PRINT:	2010/08/11 05:07:04 PM	



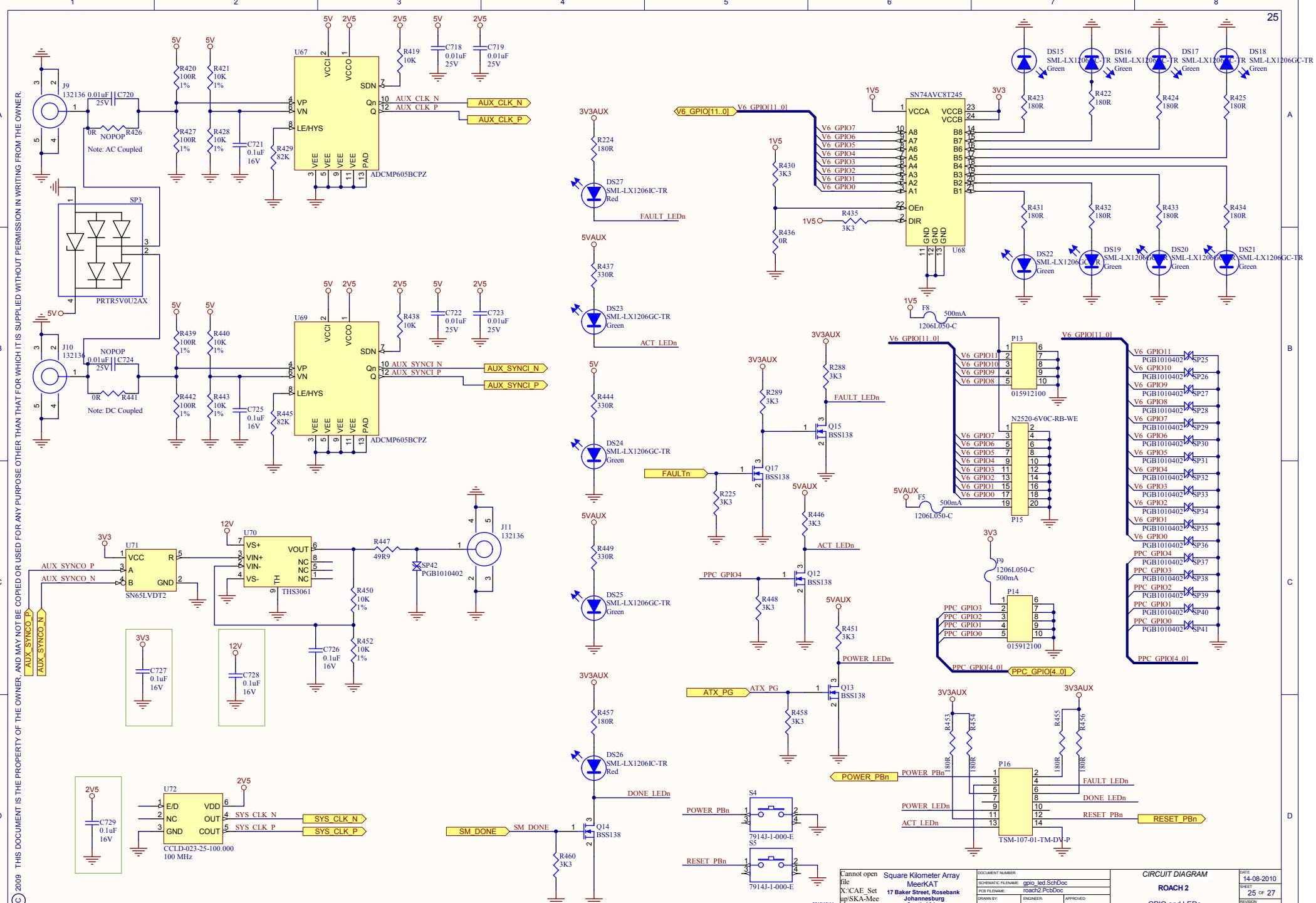


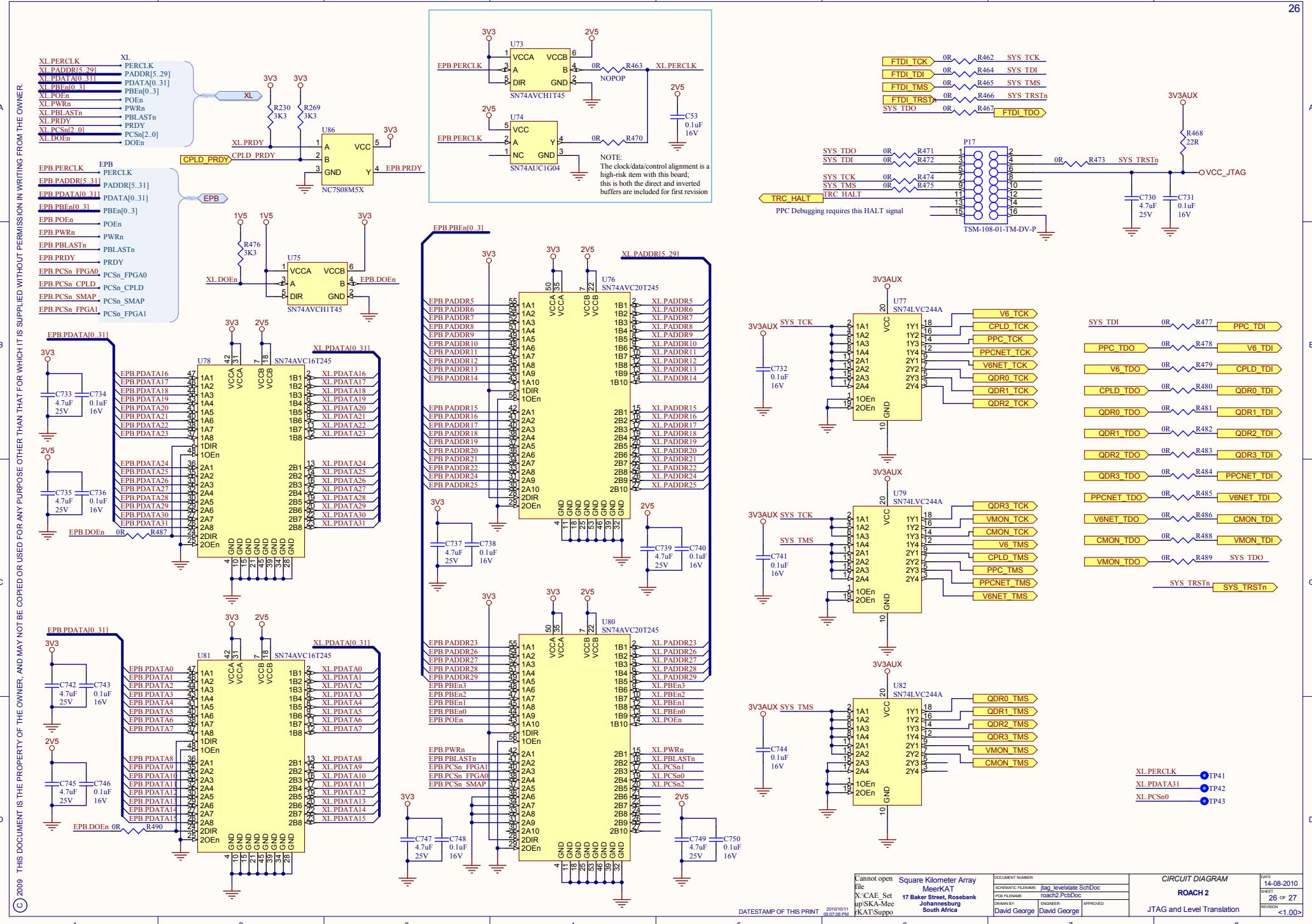
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PHY Configuration:  
CFG0 = 001 Phy Address = 00001, ENA_PAUSE = 00  
CFG1 = 000  
CFG2 = 111 AUTO NEG, ADVERTISE ALL CAPABILITIES, PREFER MASTER  
CFG3 = 010 ENABLE CROSSOVER, ENABLE 125MHZ CLK  
CFG4 = 100 HWCFG = 0100 (SMGII NO CLOCK, TO COPPER)  
CFG5 = 100 DISABLE FIBRE, ENABLE ENERGY DETECT  
CFG6 = 010 MDIO/MDTC INTERFACE, ACTIVE LOW LINE, 50 OHM IMPEDANCE
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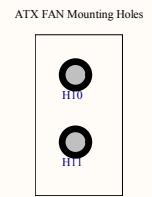
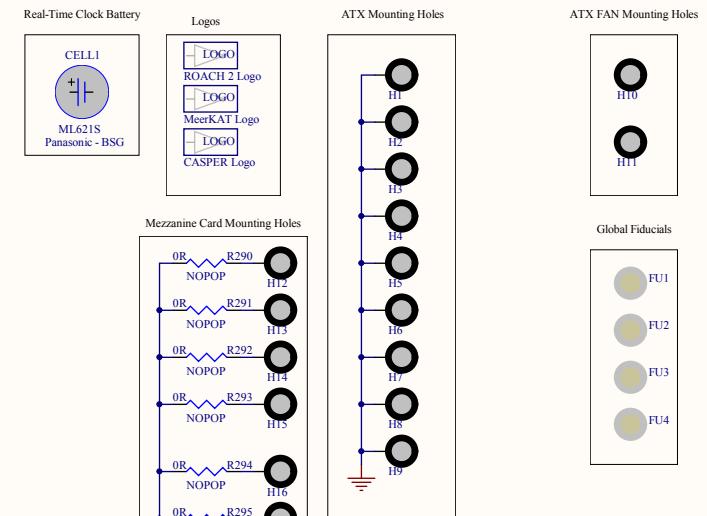
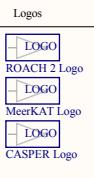
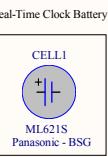


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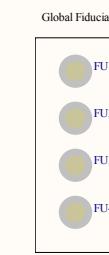
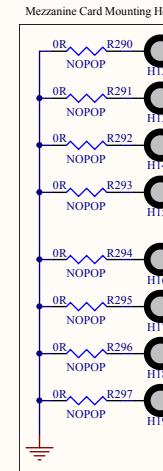




A



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D

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DATESTAMP OF THIS PRINT		DOCUMENT NUMBER		CIRCUIT DIAGRAM		DATE	
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DRAWN BY:		ENGINEER:		<1.00>		Miscellaneous Design Items	
REVISION		APPROVED:		27 OF 27		<1.00>	
DATE:		APPROVED:		REVISION		<1.00>	