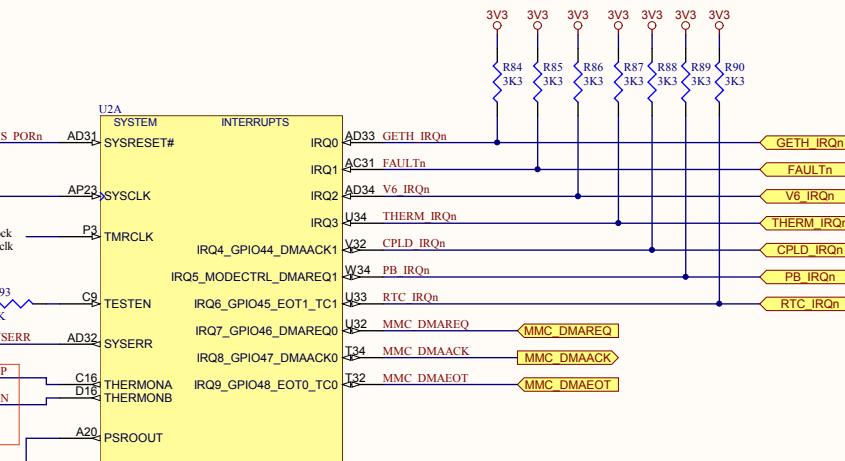
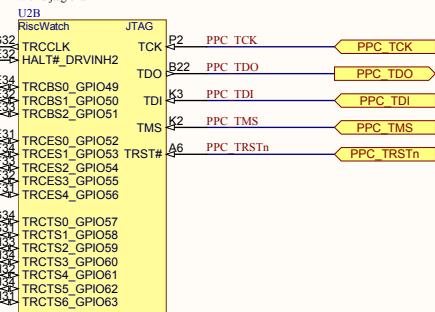


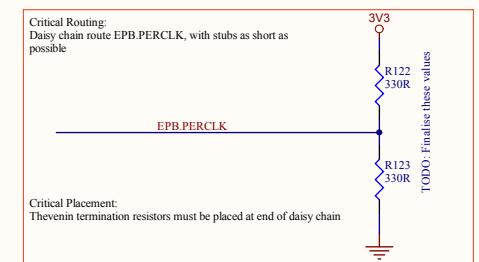
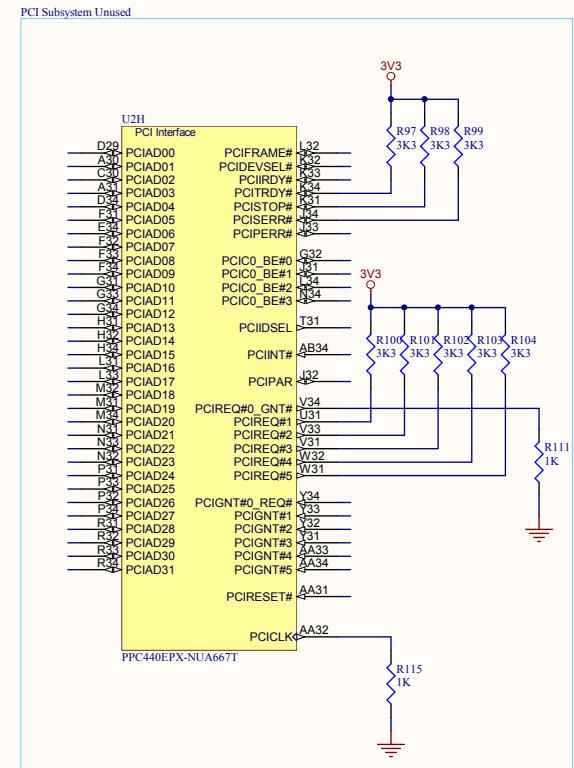
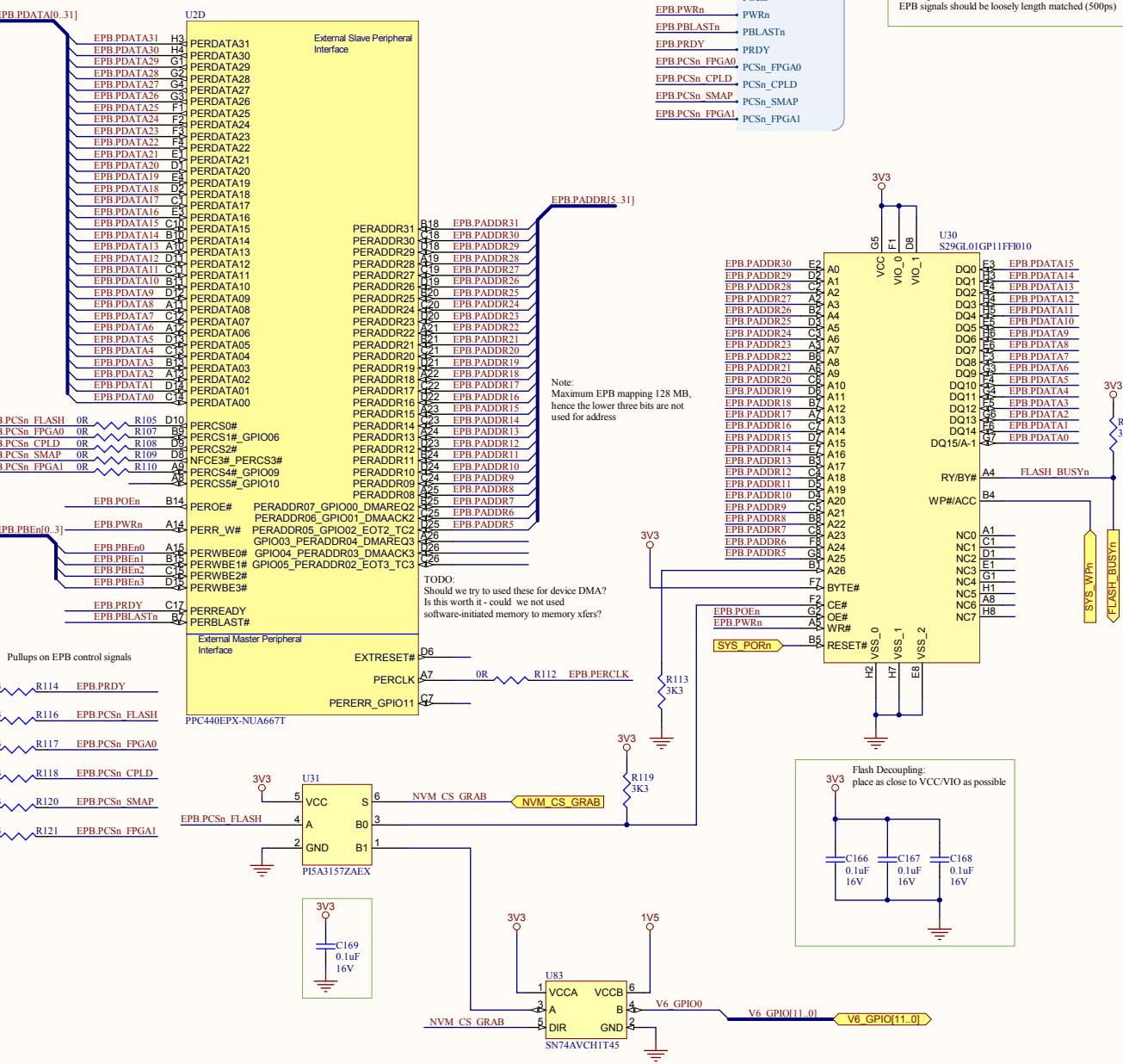
NOTE:
no JTAG on TRACE port,
use board JTAG instead

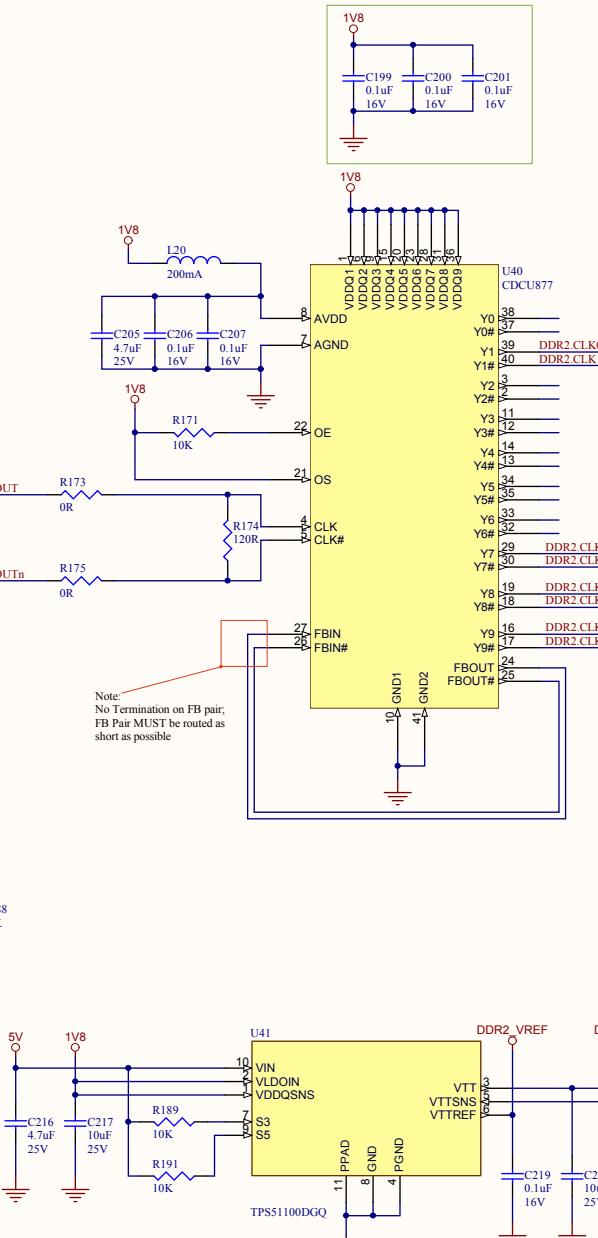
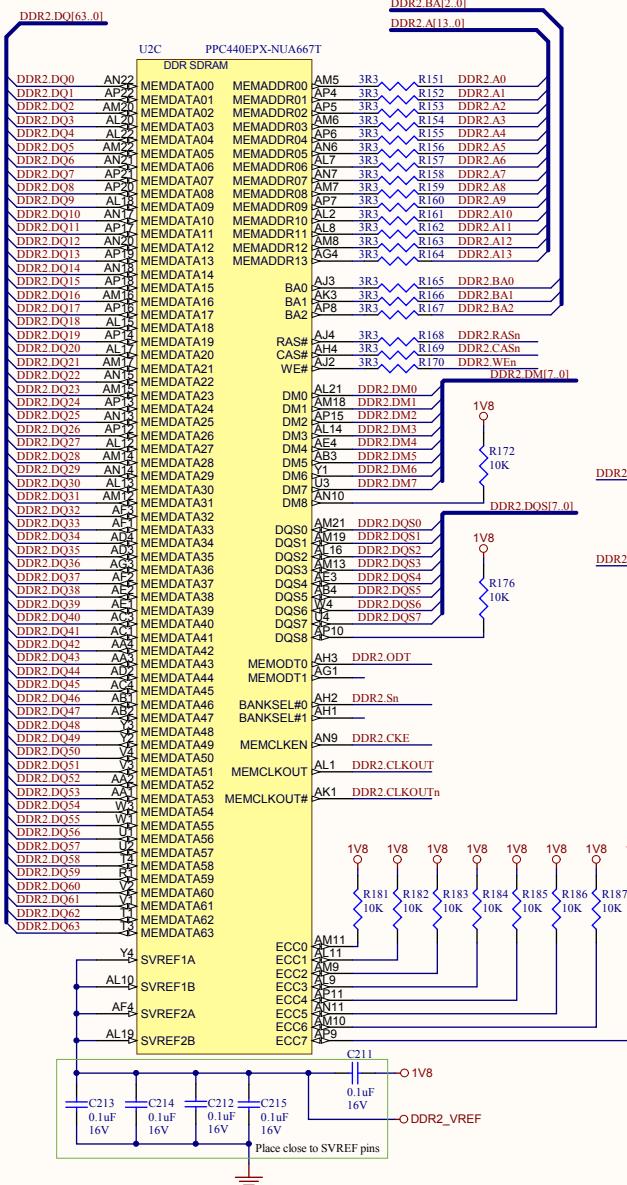


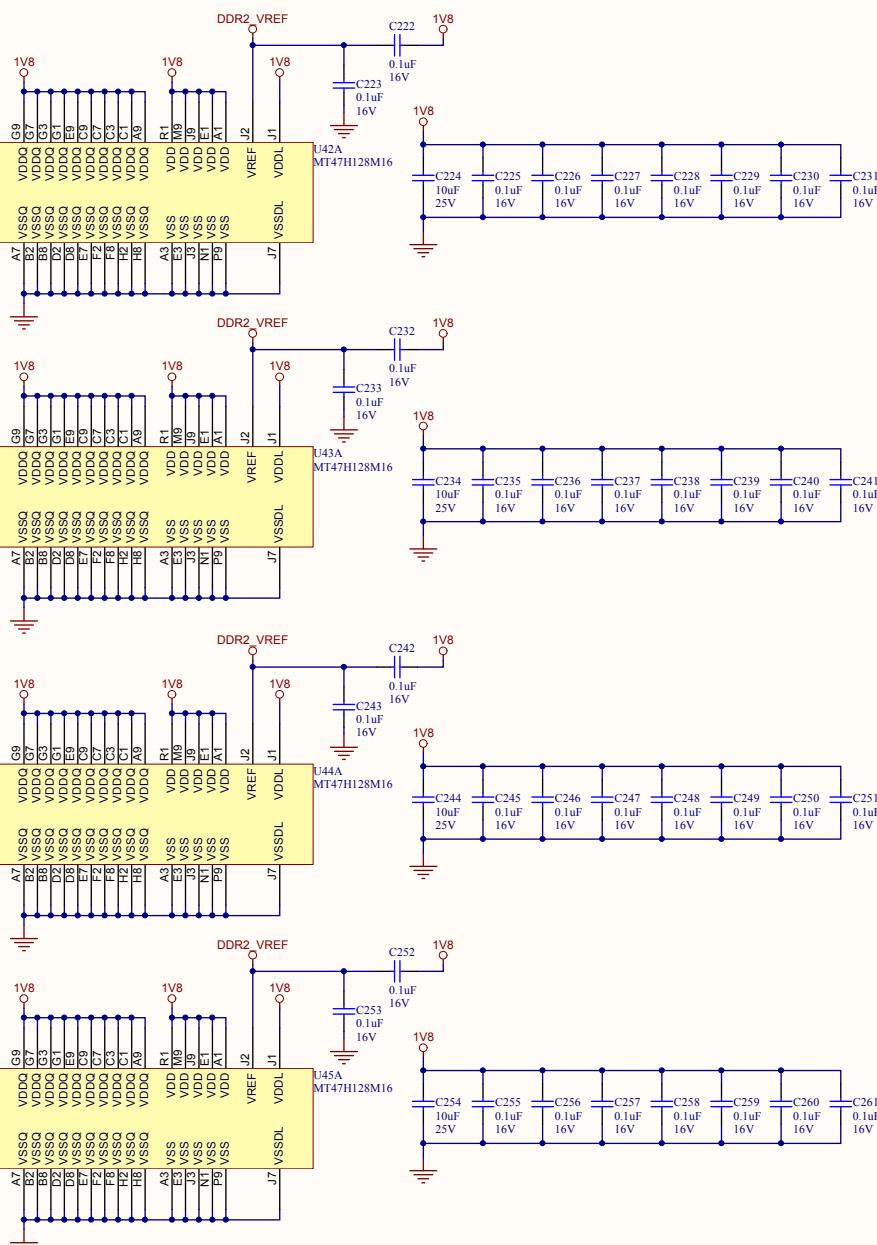
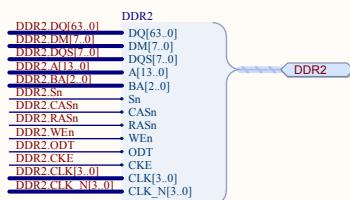
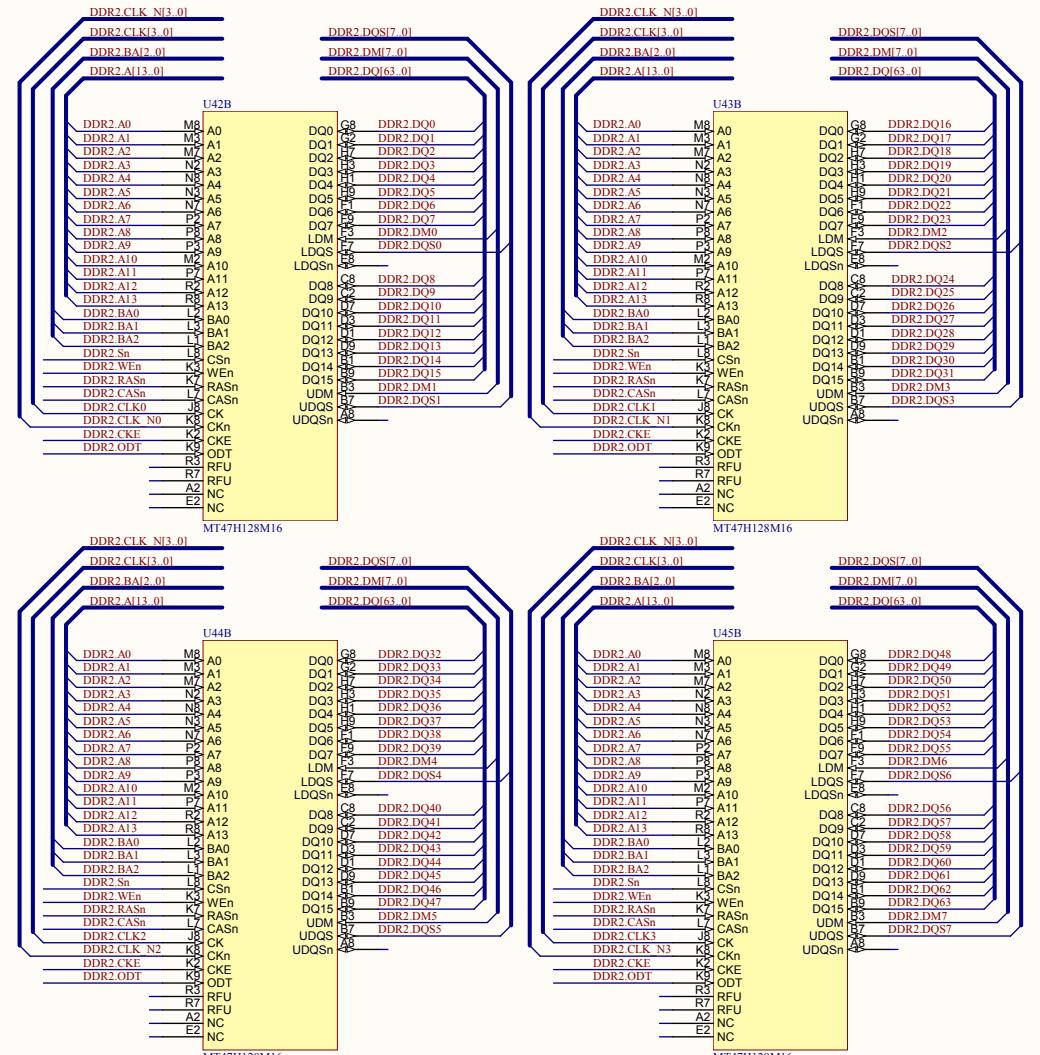
TODO: make absolutely sure that
the Macrigger software is happy
with a full chain



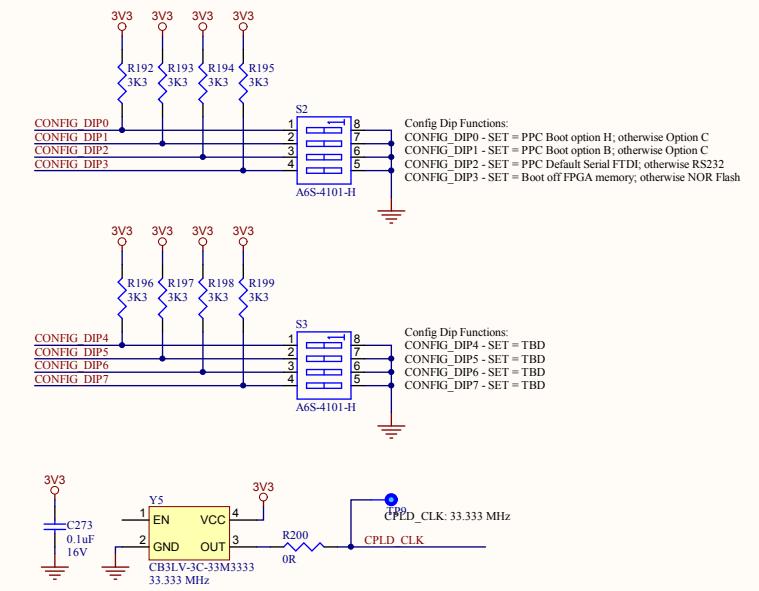
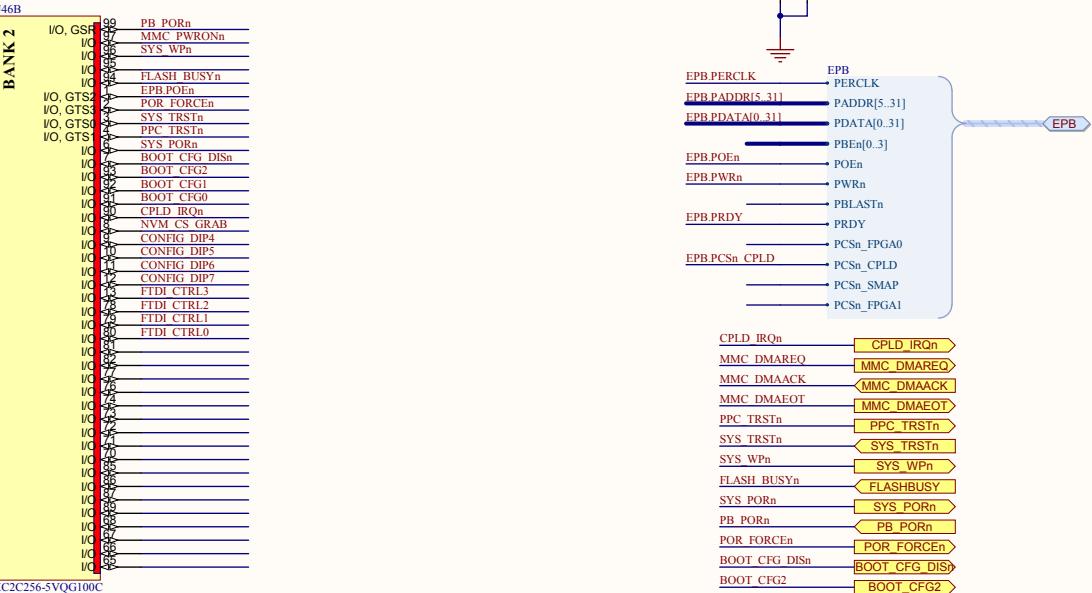
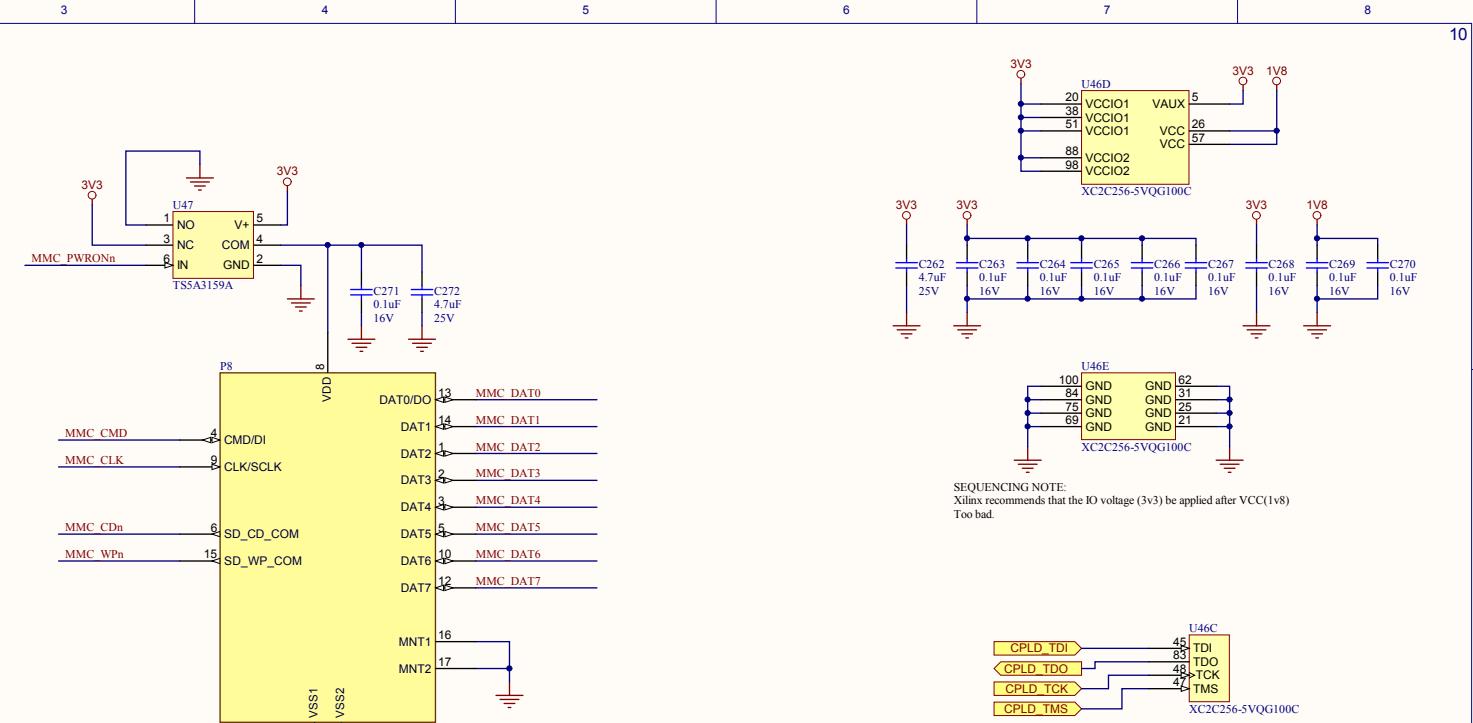
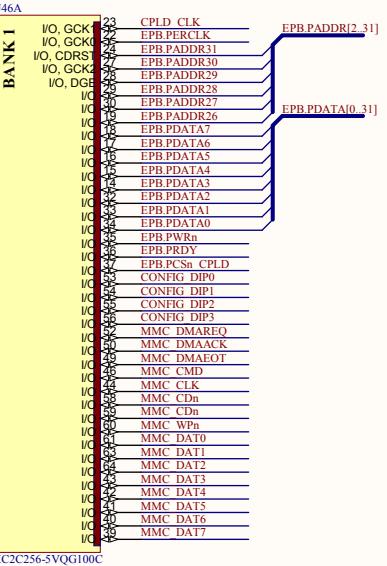
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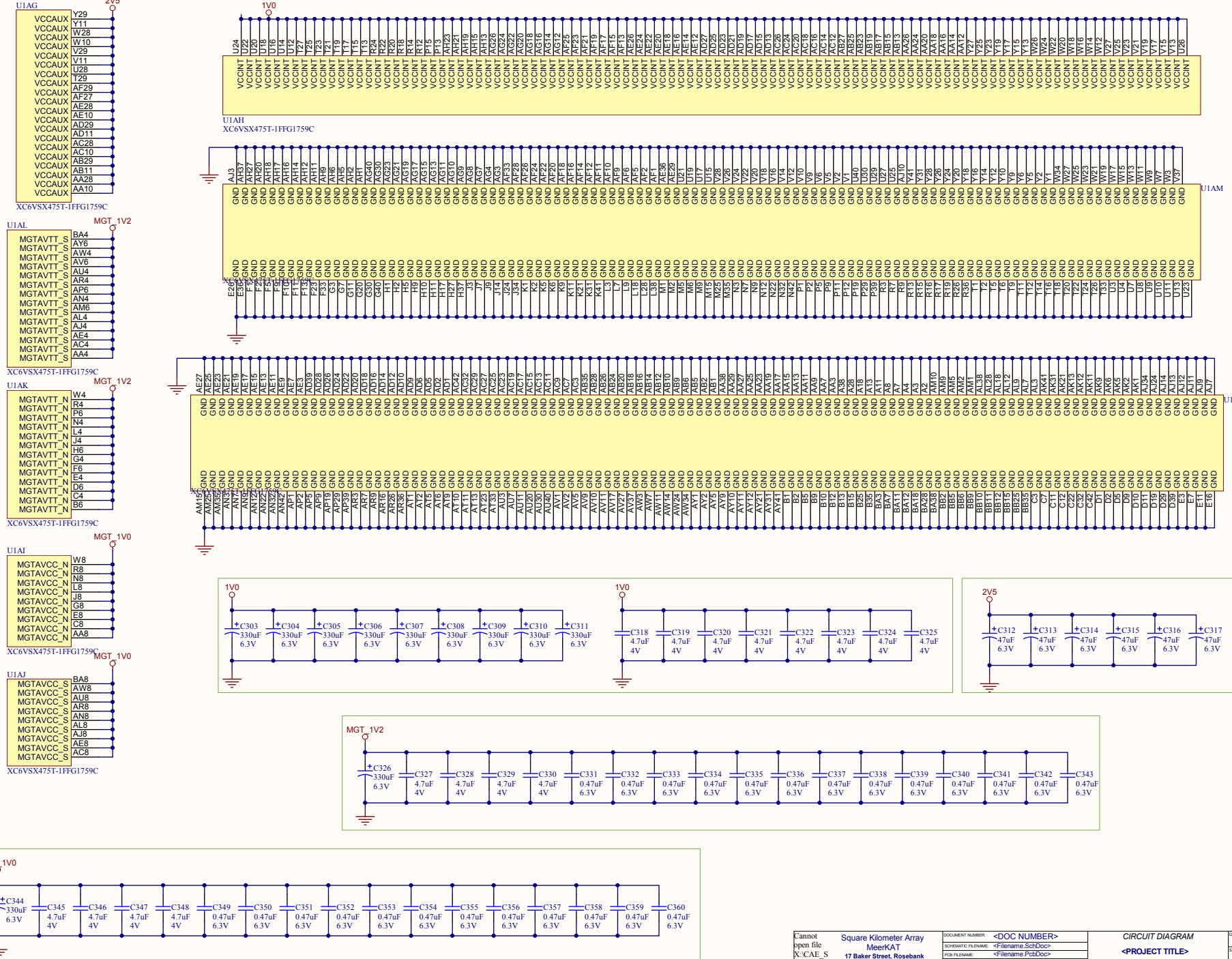


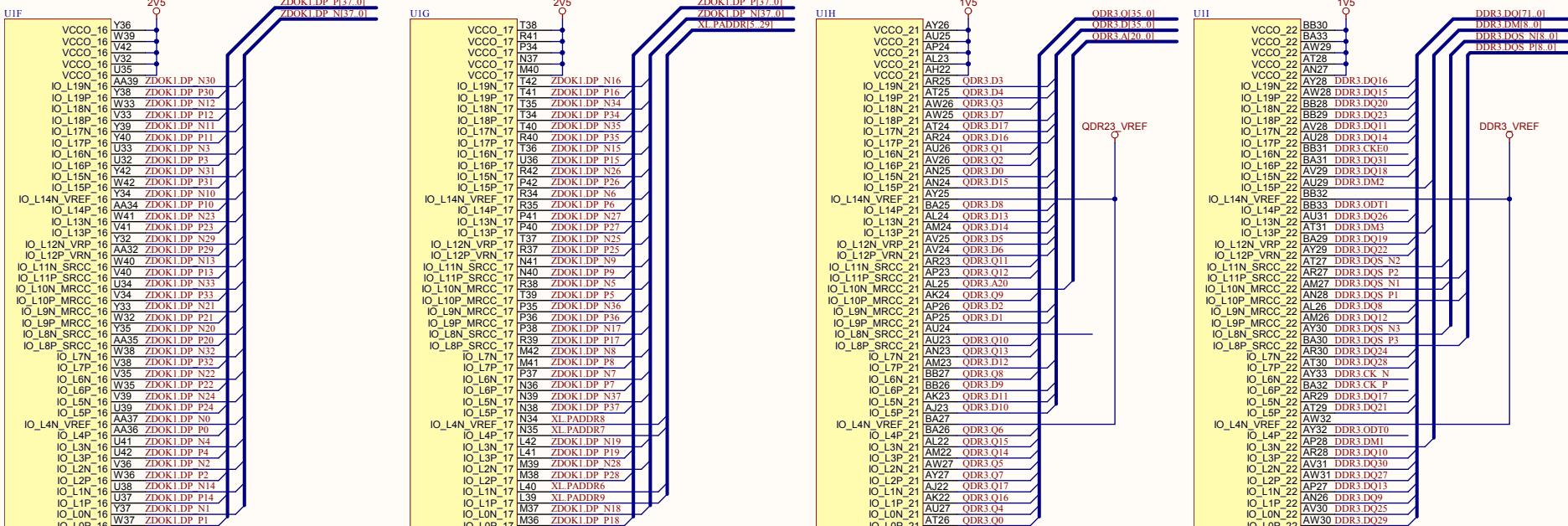




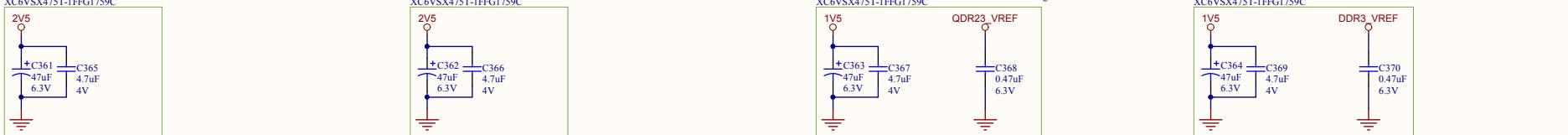
PINSWAP:
CPLD_CLK and EPB_PERCLK MUST go on GCK pins
SYS_PORn MUST go on GSR pin
EPB_POE_n MUST go on GTS pin
Otherwise, swap away



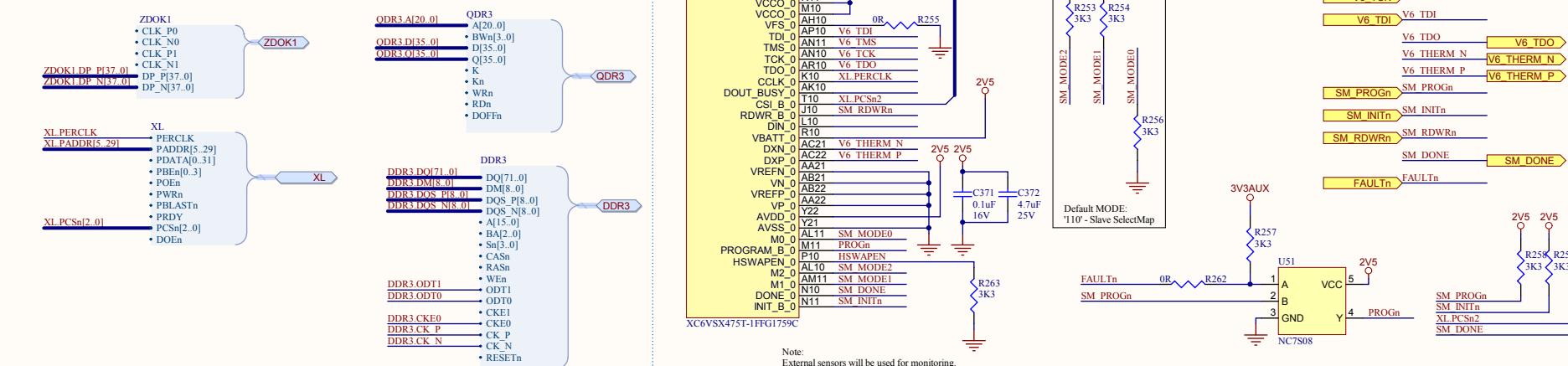




Note: avoid using free IO for critical function

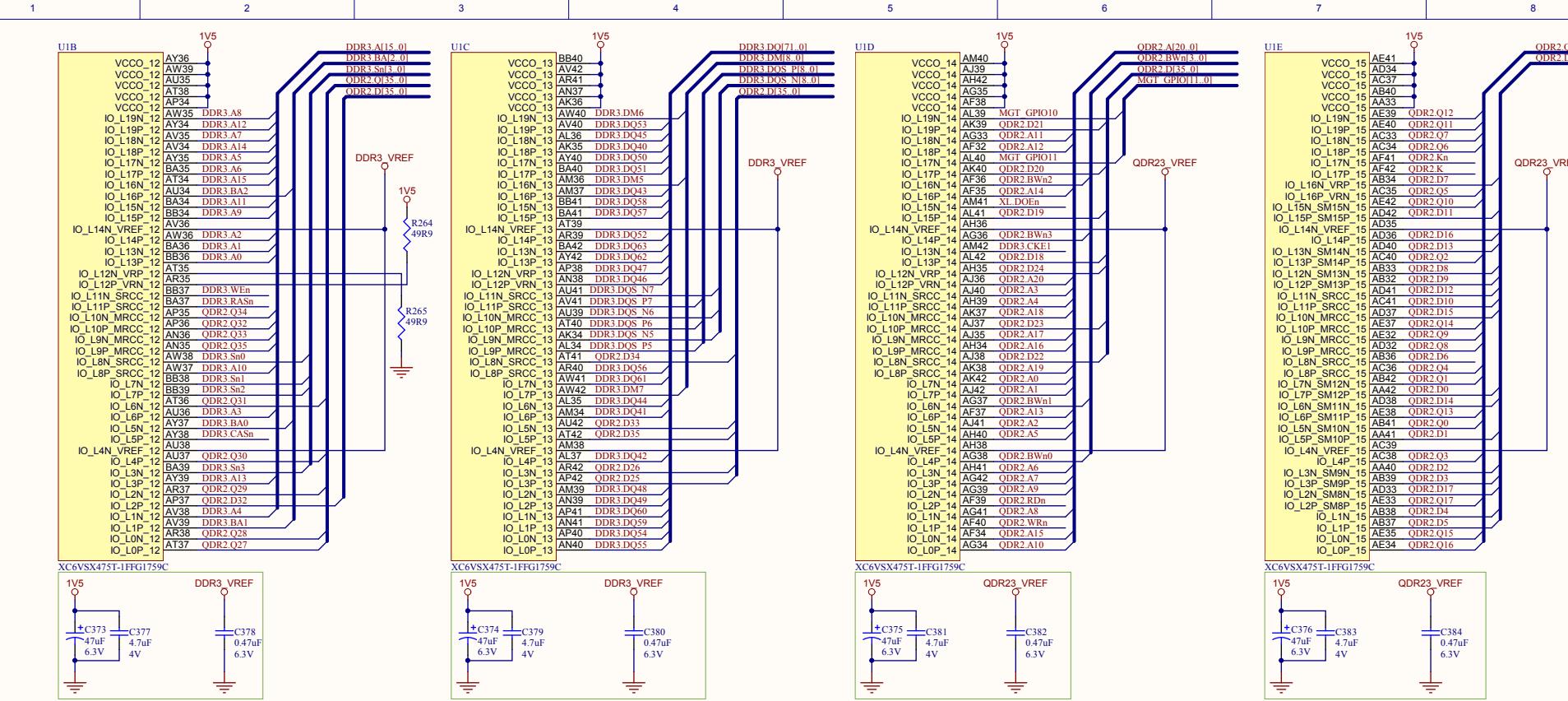


Device Compatibility:
Bank 21 unavailable on
LX240T/LS365T/SX315T



Note:
External sensors will be used for monitoring
hence the lack of more rigorous filtering

CIRCUIT DIAGRAM PROJECT TITLE SPECIFIC SHEET FUNCTION	DATE SHEET REVISION	
	DOCUMENT NUMBER SHEET NUMBER DRAWN BY	APPROVED FOR FILING BY
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DDR3

DDR3_DQ[7..0]	DQ[7..0]
DDR3_DM[8..0]	DM[8..0]
DDR3_P[8..0]	P[8..0]
DDR3_N[8..0]	N[8..0]
DDR3_A[15..0]	A[15..0]
DDR3_BA[2..0]	BA[2..0]
DDR3_Sn[3..0]	Sn[3..0]
DDR3_CASn	CASn
DDR3_RASn	RASn
DDR3_WEn	WE _n
DDR3_ODT1	ODT1
DDR3_ODT0	ODT0
DDR3_CKE1	CKE1
DDR3_CKE0	CKE0
CK_P	CK_P
CK_N	CK_N
RESETn	RESETn

DDR3

DDR3_DQ[7..0]	DQ[7..0]
DDR3_DM[8..0]	DM[8..0]
DDR3_P[8..0]	P[8..0]
DDR3_N[8..0]	N[8..0]
DDR3_A[15..0]	A[15..0]
DDR3_BA[2..0]	BA[2..0]
DDR3_Sn[3..0]	Sn[3..0]
DDR3_CASn	CASn
DDR3_RASn	RASn
DDR3_WEn	WE _n
DDR3_DQ[7..0]	DQ[7..0]
DDR3_DQ[8..0]	DQ[8..0]
DDR3_DQS[8..0]	DQS[8..0]
DDR3_DQS[8..0]	DQS[8..0]
DDR3_N[8..0]	N[8..0]
DDR3_BA[2..0]	BA[2..0]
DDR3_Sn[3..0]	Sn[3..0]
DDR3_CASn	CASn
DDR3_RASn	RASn
DDR3_WEn	WE _n
DDR3_DQ[7..0]	DQ[7..0]
DDR3_DQ[8..0]	DQ[8..0]
DDR3_DQS[8..0]	DQS[8..0]
DDR3_DQS[8..0]	DQS[8..0]
DDR3_N[8..0]	N[8..0]
DDR3_BA[2..0]	BA[2..0]
DDR3_Sn[3..0]	Sn[3..0]
DDR3_CASn	CASn
DDR3_RASn	RASn
DDR3_WEn	WE _n
DDR3_DQ[7..0]	DQ[7..0]
DDR3_DQ[8..0]	DQ[8..0]
DDR3_DQS[8..0]	DQS[8..0]
DDR3_DQS[8..0]	DQS[8..0]
DDR3_N[8..0]	N[8..0]
DDR3_BA[2..0]	BA[2..0]
DDR3_Sn[3..0]	Sn[3..0]
DDR3_CASn	CASn
DDR3_RASn	RASn
DDR3_WEn	WE _n

QDR2

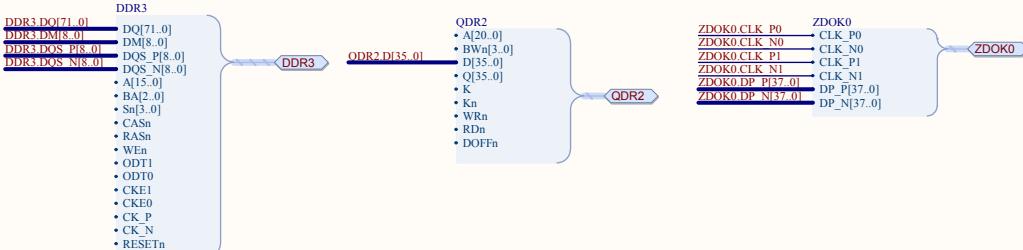
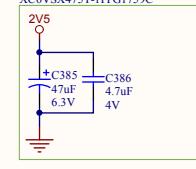
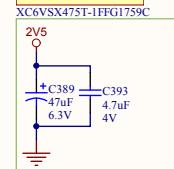
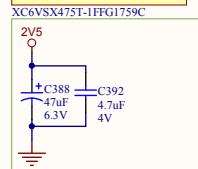
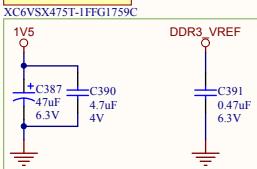
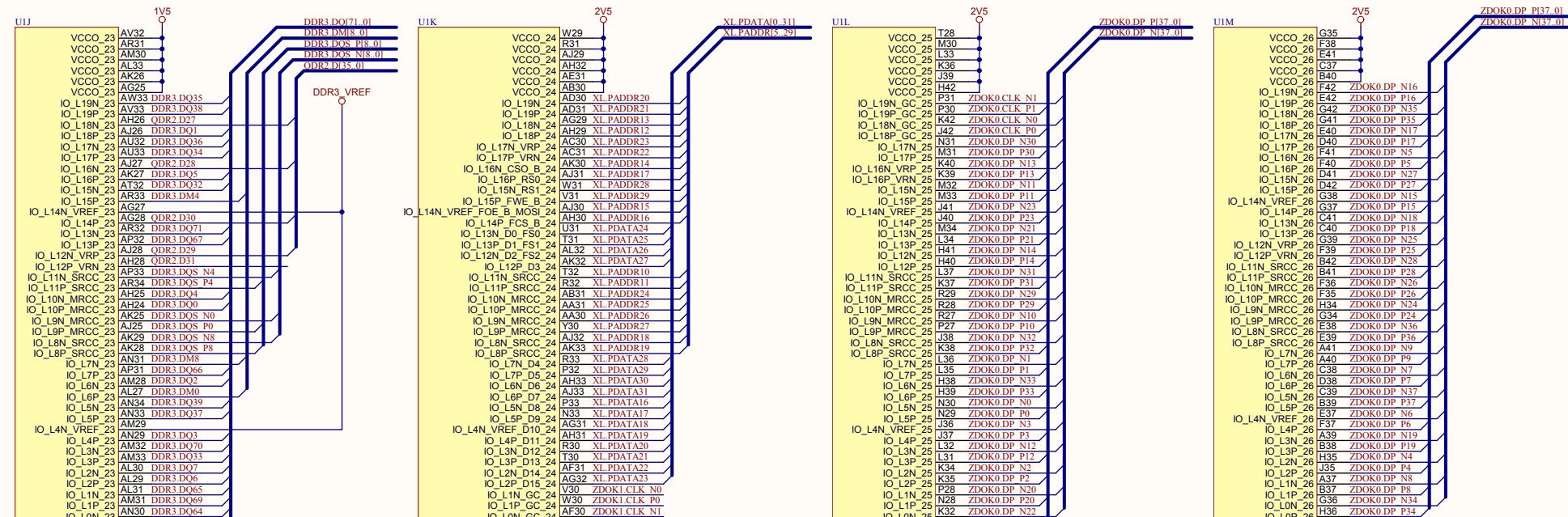
QDR2_A[20..0]	A[20..0]
QDR2_BWn[3..0]	BWn[3..0]
QDR2_D[35..0]	D[35..0]
QDR2_O[35..0]	O[35..0]
QDR2_Kn	Kn
QDR2_RDn	RDn
QDR2_DOFFn	DOFFn

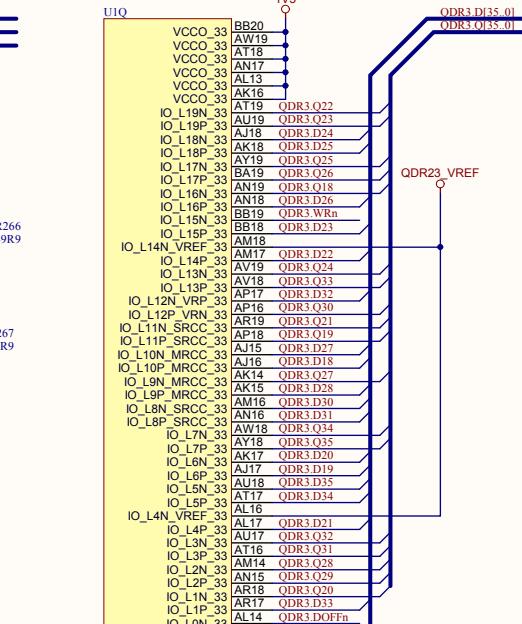
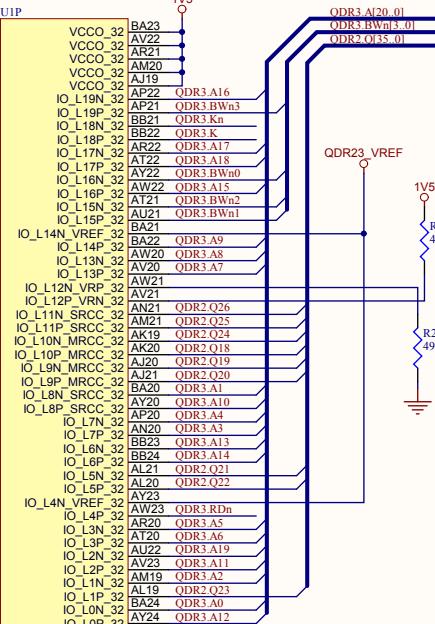
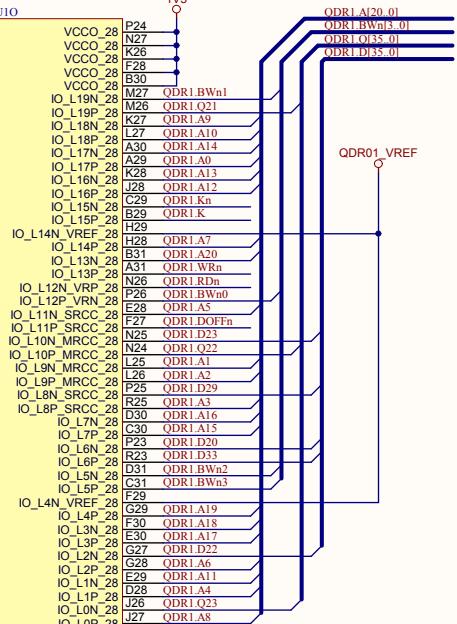
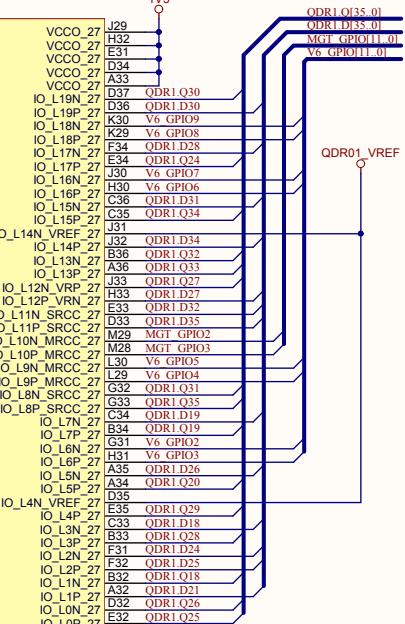
MGT

MGT_GPIO[11..0]	XL
XL_DOEn	XL

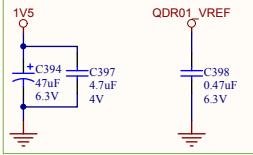
XL

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SCHMATIC FILENAME: <Filename.SchDoc>		PCB FILENAME: <Filename.PcbDoc>		SPS: 14 OF 26	
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DESIGNER: <DESIGNER>		ENGINEER: <ENGINEER>		APPROVED: <APPROVED>	
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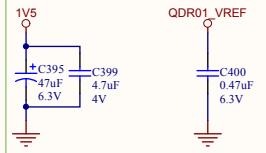




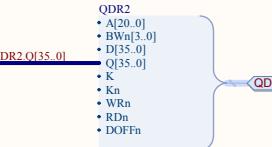
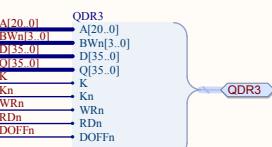
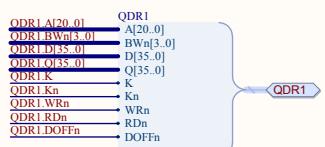
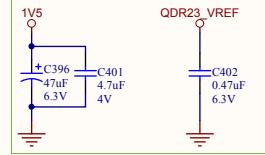
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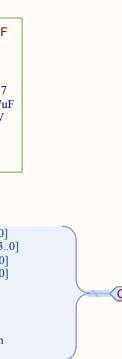
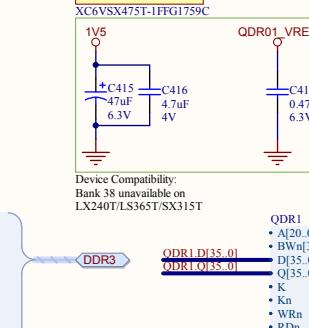
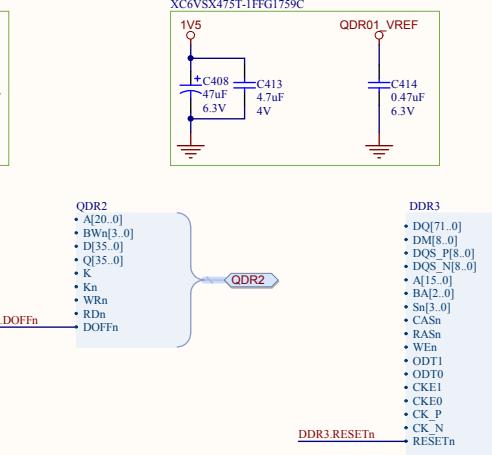
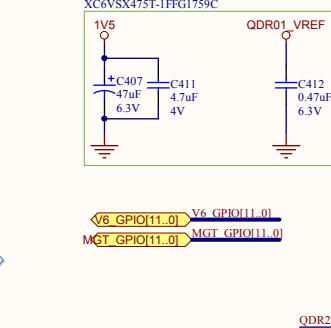
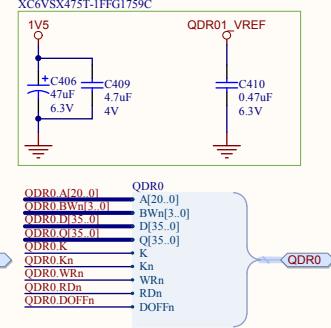
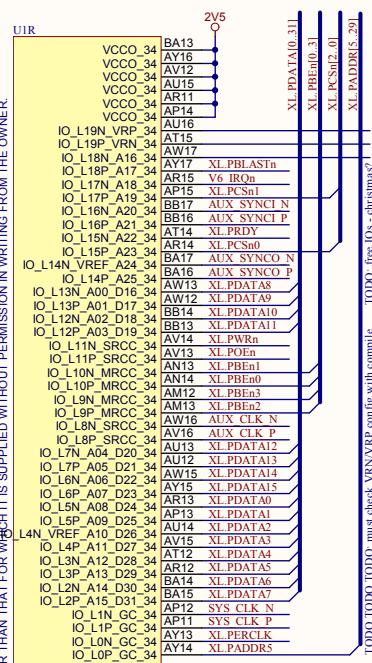


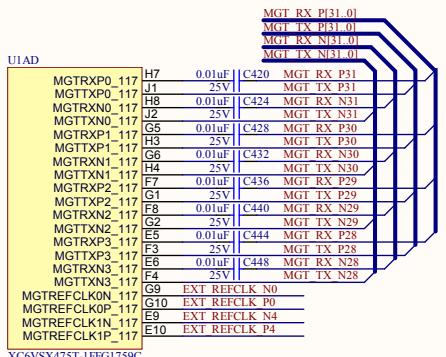
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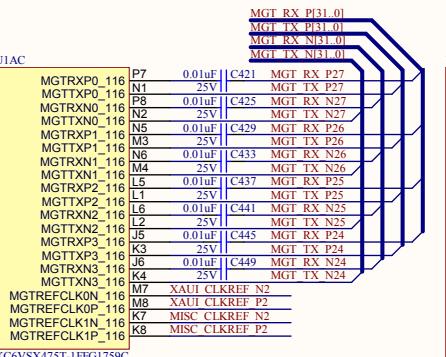
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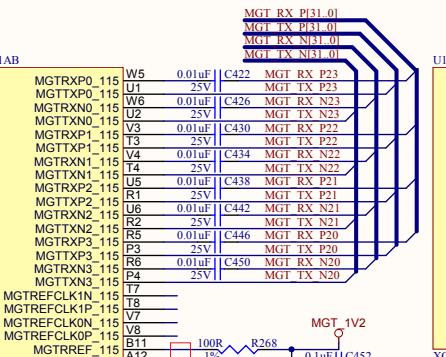




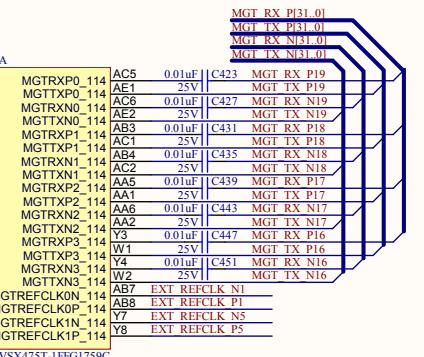
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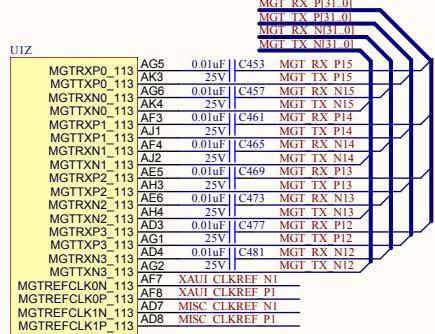
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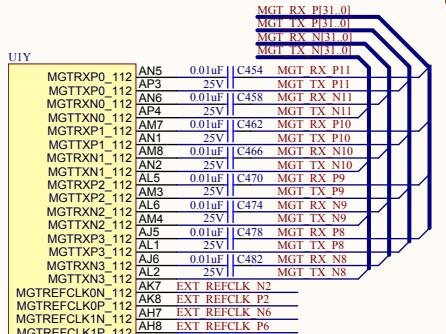
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MGTAVTBGA1_115 A1



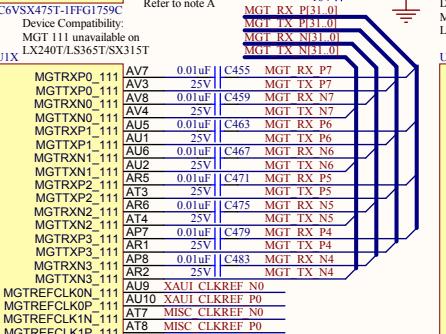
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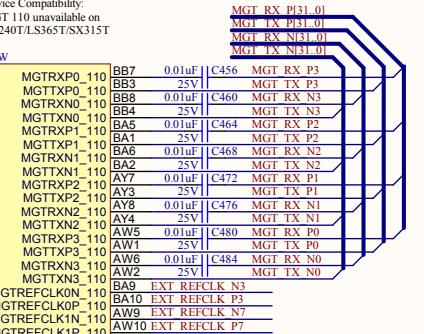
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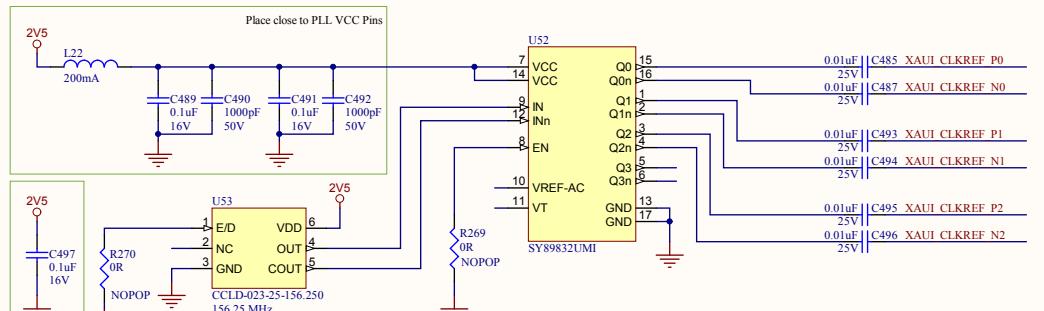
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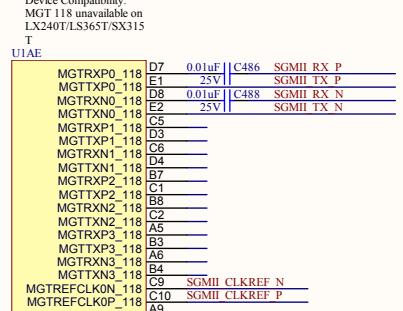
6VSX475T-1FFG1759C TODO: must check clock allocations with a compiler



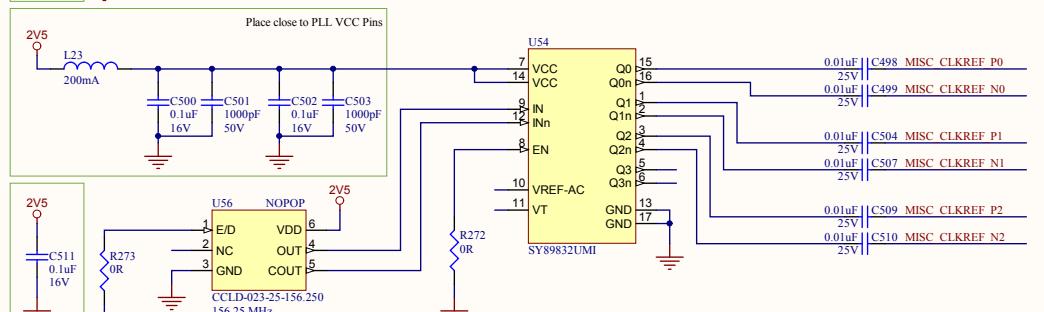
WSX475T-1EEG1759C



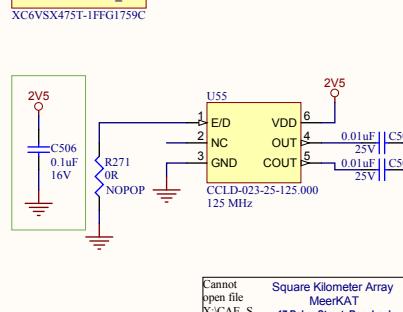
Place close to PLL_VCC Pins



MGT 118 unavailable on



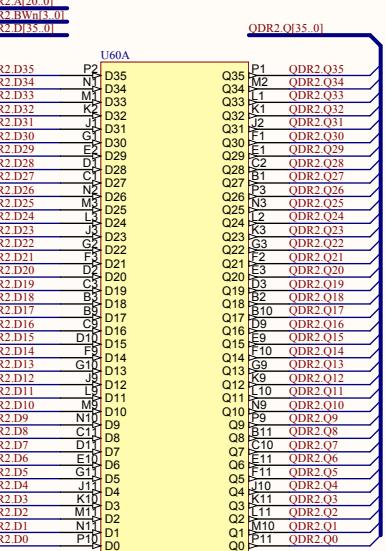
Close to PLL VCC Pins



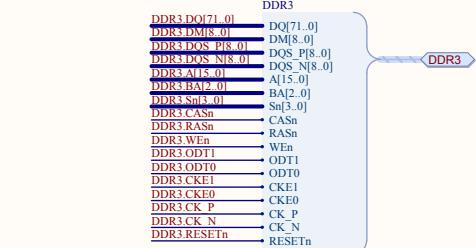
XC6VSX475T-1FFG1759C

This circuit makes provisions for a second MGT reference clock, which is not useful in most cases

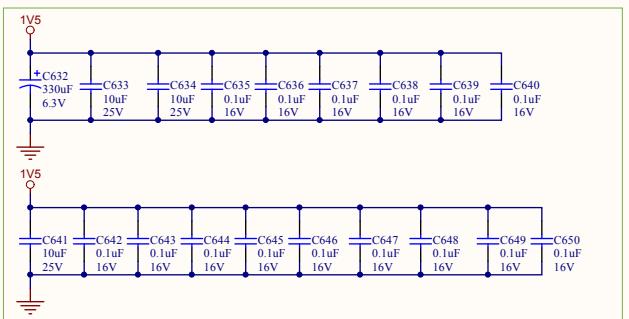
Note A:
Traces on either side of 100R resistor must have
same geometry



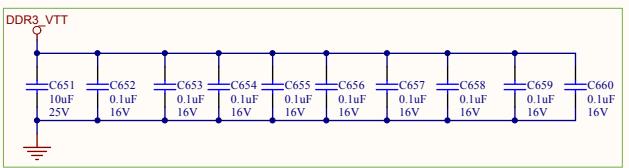
A



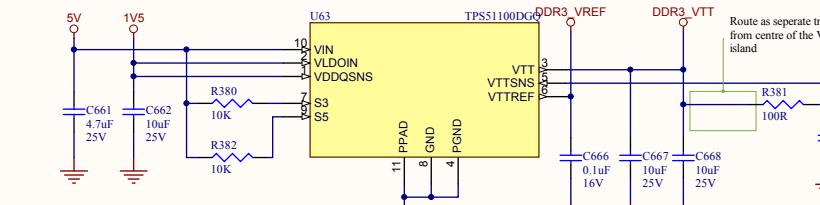
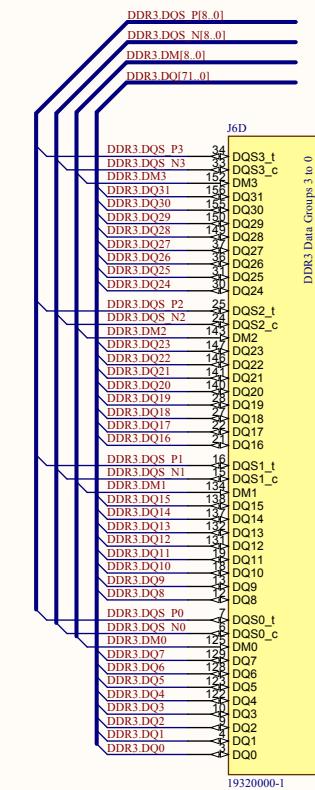
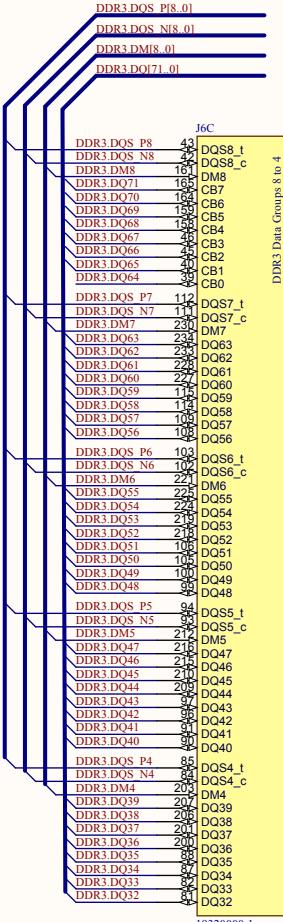
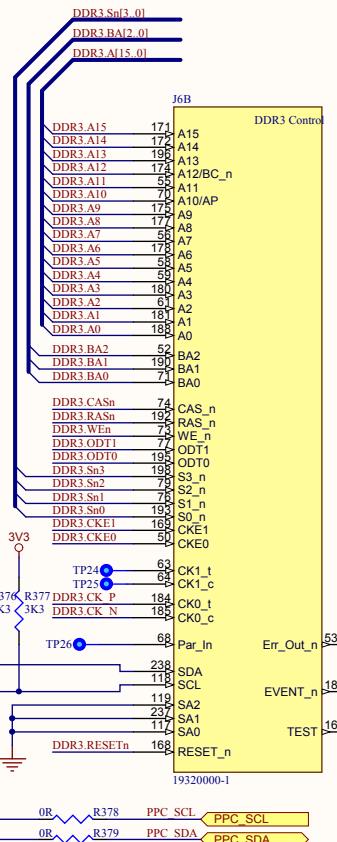
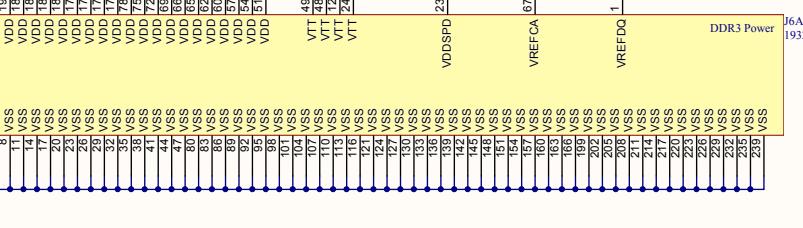
B



c



1



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A

B

C

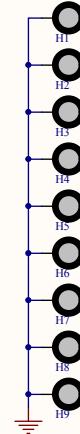
D

A

B

C

D



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			SCHEMATIC FILENAME: <filename_SchDoc>	<SPECIFIC SHEET FUNCTION>	SPR 22 OF 26
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DATESTAMP OF THIS PRINT	20100507 09:05:38 AM		MeerKAT 17 Baker Street, Rosebank Johannesburg South Africa	DRAWN BY: <DRAWN BY><ENGINEER>	
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				APPROVED: <APPROVED>	

A

B

C

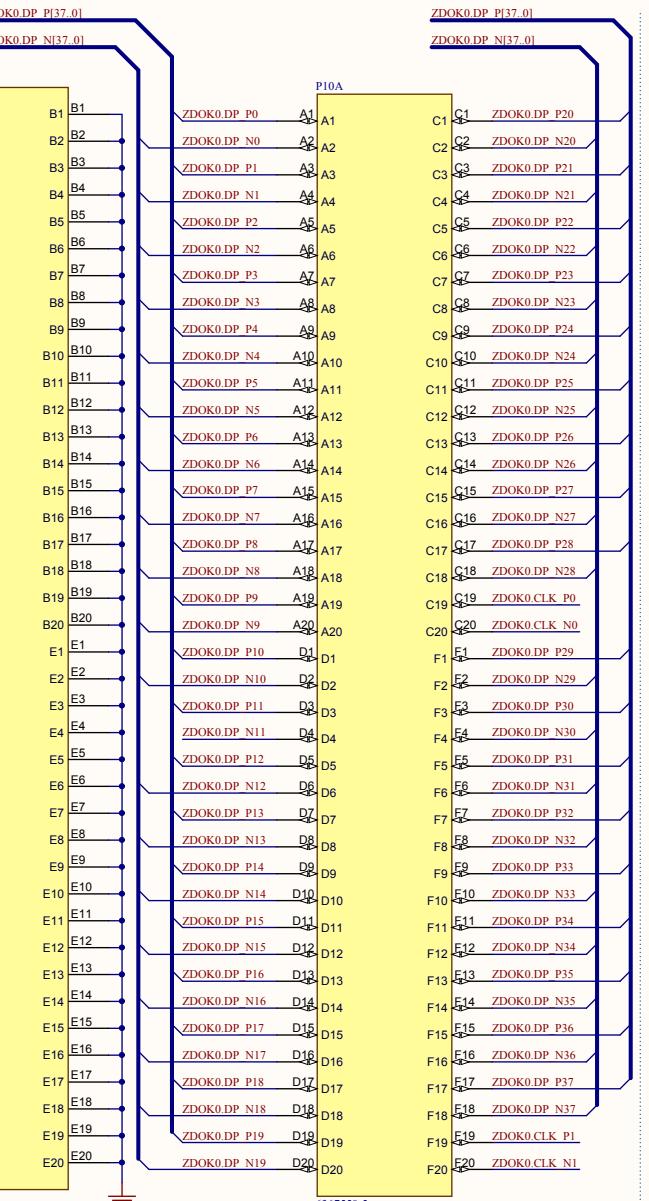
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A

B

C

D

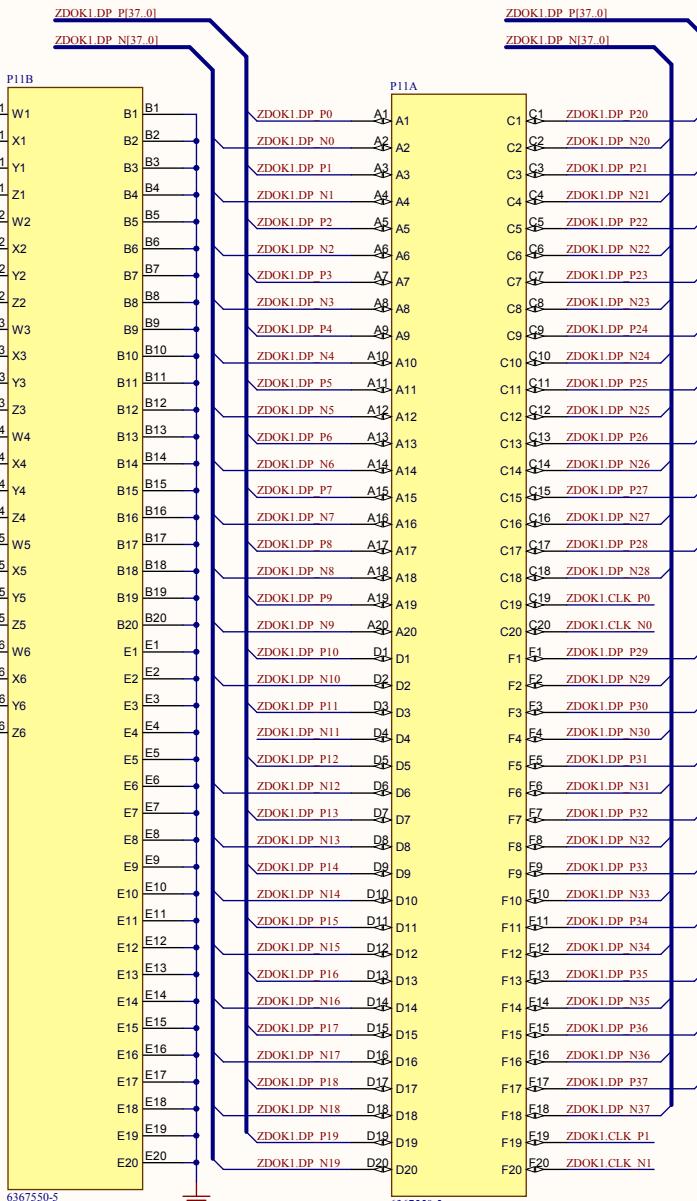


ZDOK0.CLK_P0 → ZDOK1.CLK_P0
 ZDOK0.CLK_N0 → CLK_N0
 ZDOK0.CLK_P1 → CLK_P1
 ZDOK0.CLK_N1 → CLK_N1
 ZDOK0.DP_P[37..0] → DP_P[37..0]
 ZDOK0.DP_N[37..0] → DP_N[37..0]

DATESTAMP OF THIS PRINT: 20100507 09:05:38 AM

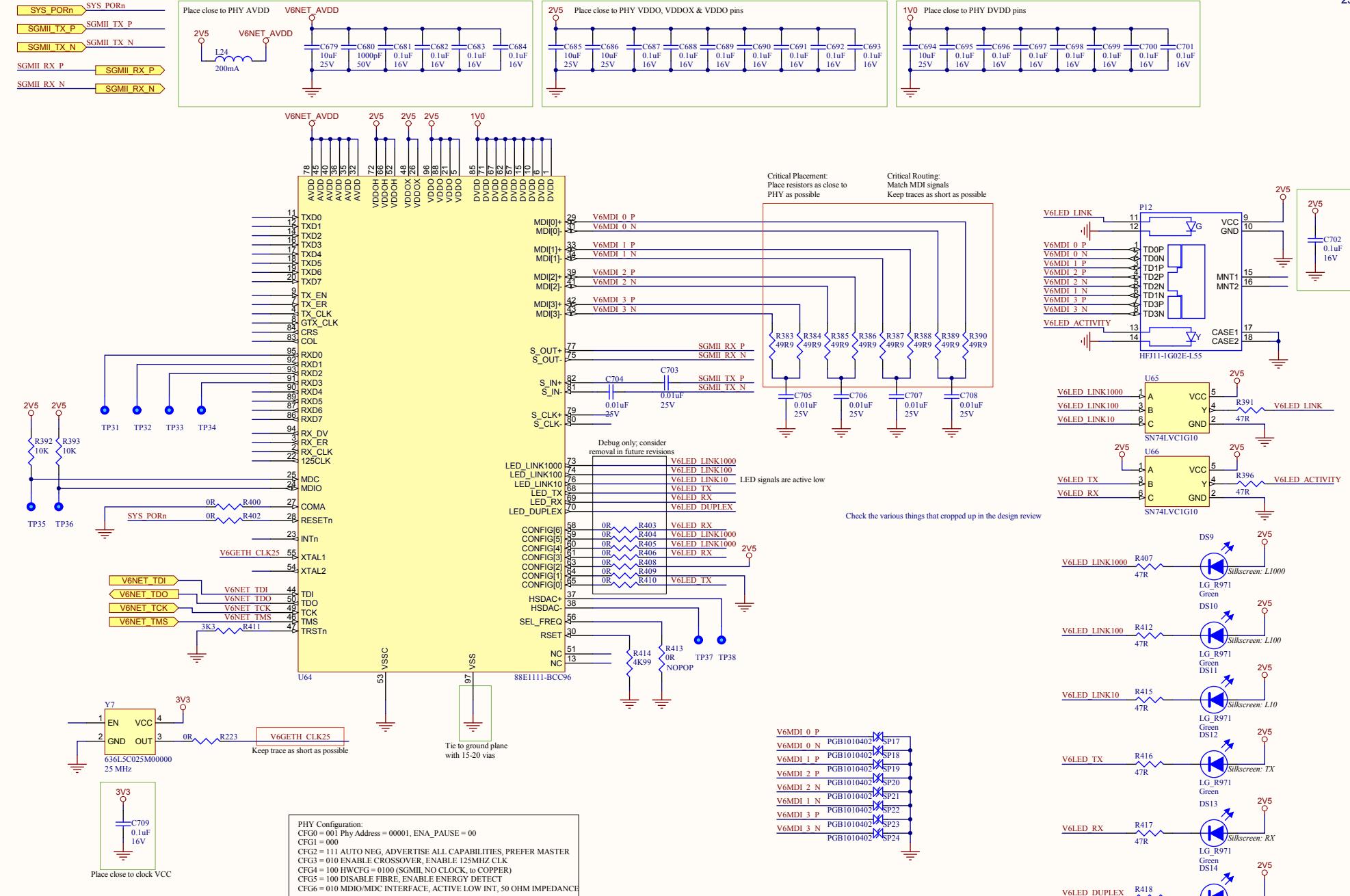
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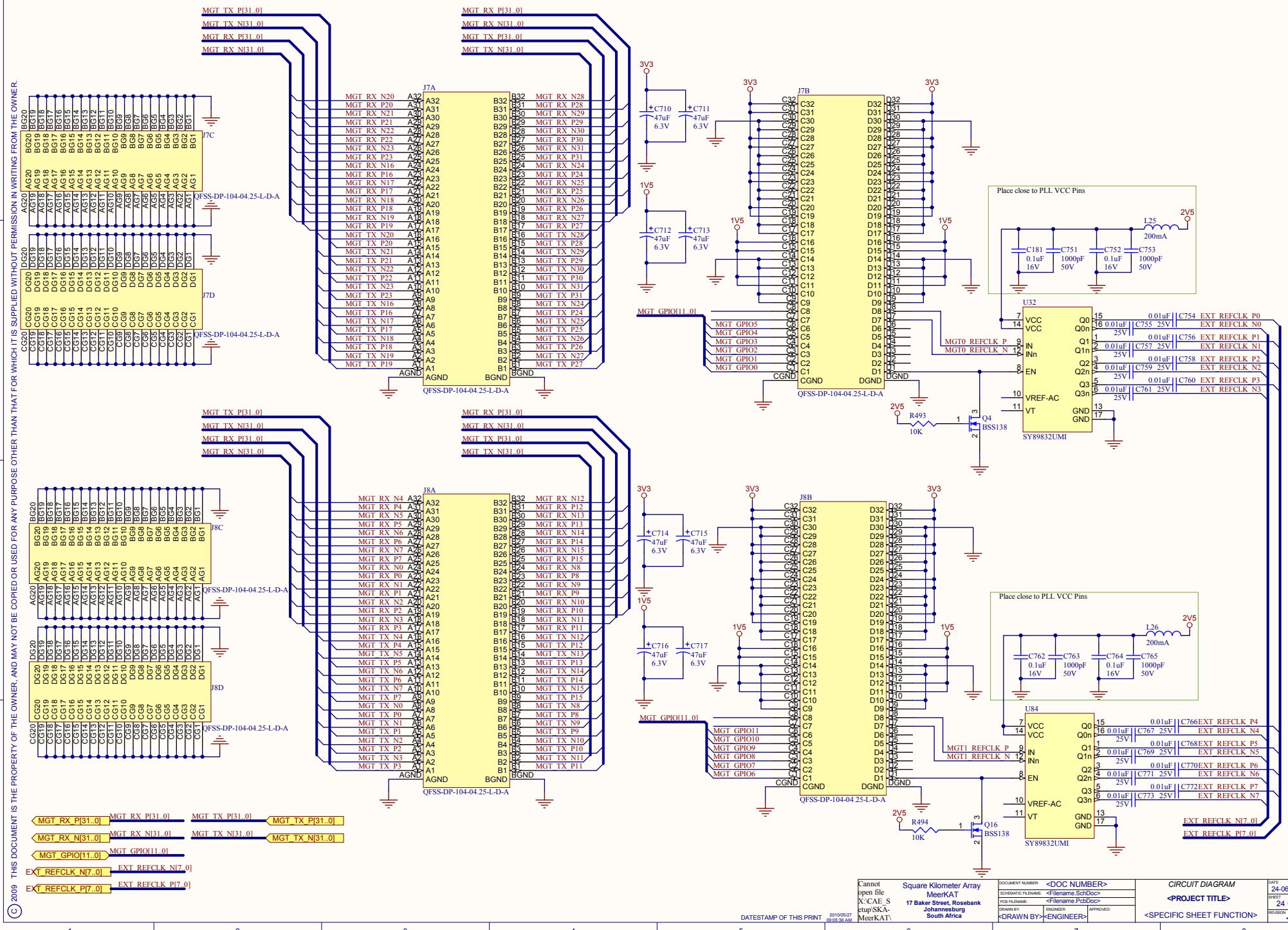
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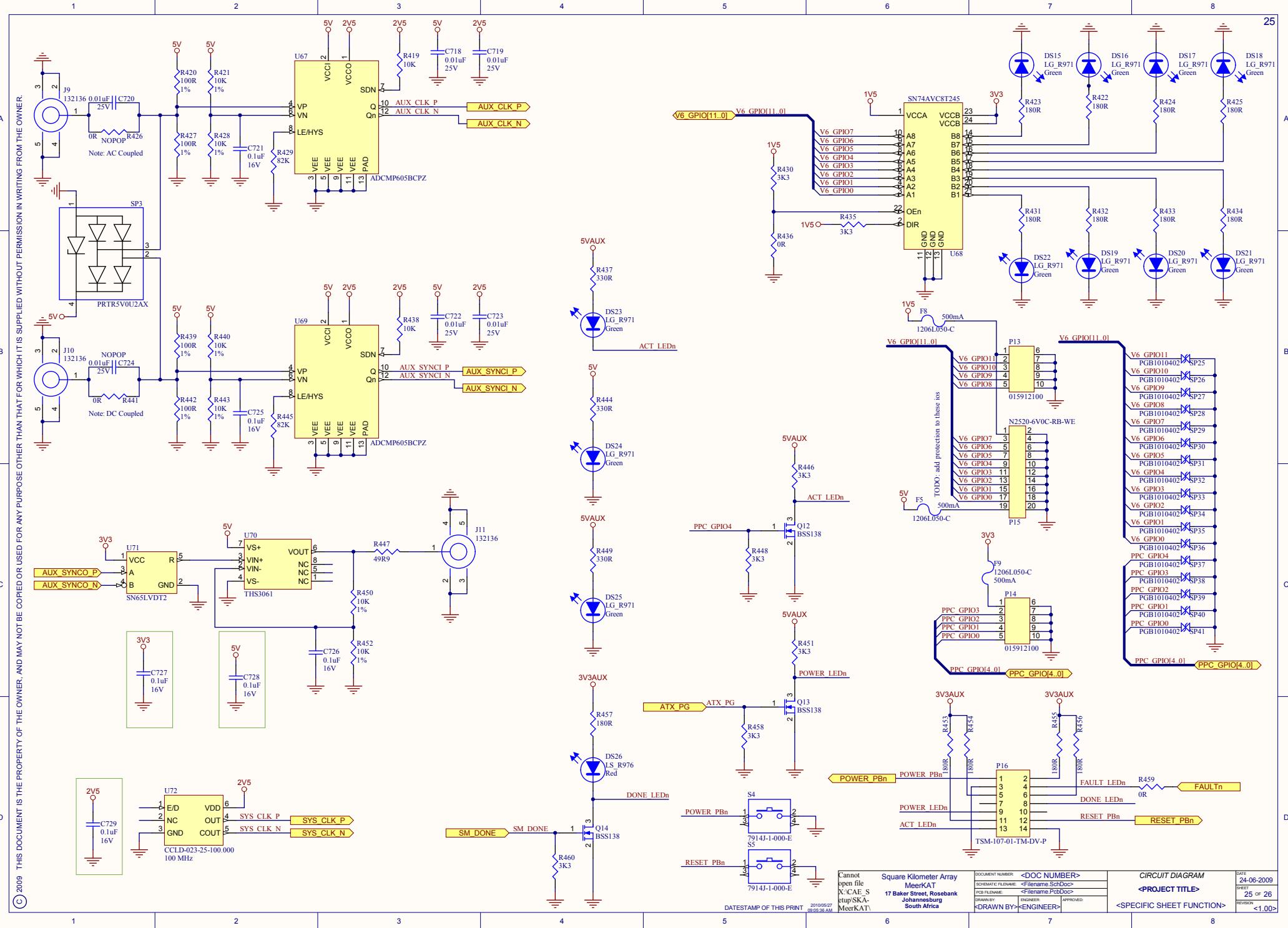


CIRCUIT DIAGRAM <PROJECT TITLE>		DATE 24-06-2009
<SPECIFIC SHEET FUNCTION>		SPR 22 OF 26
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DRAWN BY: <DRAWN BY>	ENGINEER: <ENGINEER>	APPROVED: <APPROVED>

A B C D ()







XL PERCLK
XL PADDR[5..29]
XL PDAT[0..31]
XL PBEn[0..31]
XL POEn
POEn
XL PWLn
XL PBASTn
XL PBASTn
XL PRD
XL PRDY
XL PCSn[2..0]
XL DOEn
DOEn

EPB PERCLK
EPB PADDR[5..31]
EPB PDAT[0..31]
EPB PBEn[0..31]
EPB POEn
EPB PWLn
EPB PBASTn
EPB PRD
EPB PCSn FPGA0
PCSn_FPGA0
EPB PCSn CPLD
PCSn_CPLD
EPB PCSn SMAP
PCSn_SMAP
EPB PCSn FPGA1
PCSn_FPGA1

EPB PDAT[0..31]

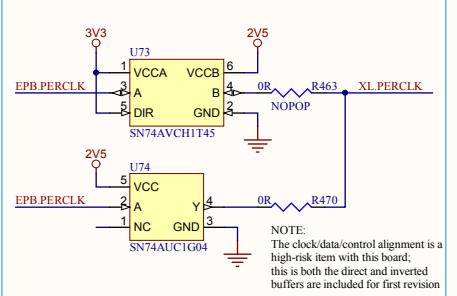
3V3
2V5
C733 4.7uF 0.1uF 25V 16V
C734 0.1uF 25V 16V
EPB DOEn OR R487 2OE

EPB PDAT[0..31]

3V3
2V5
C742 4.7uF 0.1uF 25V 16V
C743 0.1uF 25V 16V
EPB DOEn OR R490 2OE

Note:
Assuming Cds = 40 pF, Tr=10*40pF=4ns
Would load other PRDY driver by 44mA

XL
XL PRDY
Q15 BSS138
R469 3K3
3V3
R461 100R
EPB PRDY



NOTE:
The clock/data/control alignment is a high-risk item with this board;
this is both the direct and inverted buffers are included for first revision

FTDI TCK
FTDI TDI
FTDI TMS
FTDI TRST
SYS TDO

R462
R464
R465
R466
R467

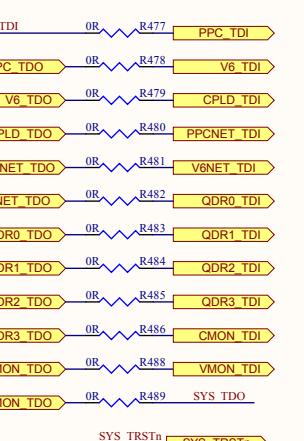
SYS TCK
SYS TDI
SYS TMS
SYS TRSTn

FTDI TDO

3V3AUX
R468 22R
OVC_JTAG

SYS TDO
SYS TDI
SYS TCK
SYS TMS
TSM-108-01-TM-DV-P

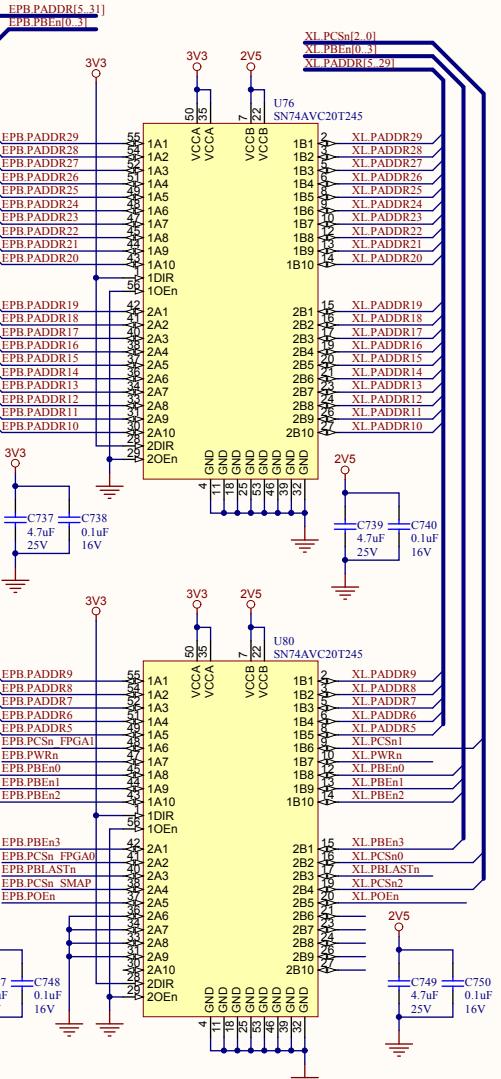
P17
R471
R472
R474
R475
R476
R477
R478
R479
R480
R481
R482
R483
R484
R485
R486
R488
R489
C730 4.7uF 0.1uF 25V 16V
C731 0.1uF 25V 16V



VCO
PPC TCK
PPCNET TCK
V6 NET TCK
QDR0 TCK
QDR1 TCK
QDR2 TCK

PPCNET TDO
V6NET TDO
QDR0 TDO
QDR1 TDO
QDR2 TDO
QDR3 TDO
CMON TCK
V6 TMS
CPLD TMS
PPC TMS
PPCNET TMS
V6NET TMS

QDR3 TMS
QDR1 TMS
QDR2 TMS
QDR3 TMS
CMON TMS



EPB PDATA[0..31]
3V3
2V5
R476 3K3
3V3
U75 SN74AVC16T245
VCCA VCCB
DIR GND
EPB DOEn

XL PDAT[0..31]
3V3
2V5
U76 SN74AVC20T245
VCCA VCCB
DIR GND
XL PADDR[2..0]
XL PBEn[0..31]
XL PADDR[5..29]

EPB PADDR[29]
EPB PADDR[28]
EPB PADDR[27]
EPB PADDR[26]
EPB PADDR[25]
EPB PADDR[24]
EPB PADDR[23]
EPB PADDR[22]
EPB PADDR[21]
EPB PADDR[20]
EPB PADDR[19]
EPB PADDR[18]
EPB PADDR[17]
EPB PADDR[16]
EPB PADDR[15]
EPB PADDR[14]
EPB PADDR[13]
EPB PADDR[12]
EPB PADDR[11]
EPB PADDR[10]
EPB PADDR[9]
EPB PADDR[8]
EPB PADDR[7]
EPB PADDR[6]
EPB PADDR[5]
EPB PADDR[4]
EPB PADDR[3]
EPB PADDR[2]
EPB PADDR[1]
EPB PADDR[0]
EPB PADDR[10E]

3V3
2V5
C737 4.7uF 0.1uF 25V 16V
C738 0.1uF 25V 16V
EPB PDATA[23]
EPB PDATA[22]
EPB PDATA[21]
EPB PDATA[20]
EPB PDATA[19]
EPB PDATA[18]
EPB PDATA[17]
EPB PDATA[16]
EPB PDATA[15]
EPB PDATA[14]
EPB PDATA[13]
EPB PDATA[12]
EPB PDATA[11]
EPB PDATA[10]
EPB PDATA[9]
EPB PDATA[8]
EPB PDATA[7]
EPB PDATA[6]
EPB PDATA[5]
EPB PDATA[4]
EPB PDATA[3]
EPB PDATA[2]
EPB PDATA[1]
EPB PDATA[0]
EPB PDATA[10E]

XL PDATA[23]
XL PDATA[22]
XL PDATA[21]
XL PDATA[20]
XL PDATA[19]
XL PDATA[18]
XL PDATA[17]
XL PDATA[16]
XL PDATA[15]
XL PDATA[14]
XL PDATA[13]
XL PDATA[12]
XL PDATA[11]
XL PDATA[10]
XL PDATA[9]
XL PDATA[8]
XL PDATA[7]
XL PDATA[6]
XL PDATA[5]
XL PDATA[4]
XL PDATA[3]
XL PDATA[2]
XL PDATA[1]
XL PDATA[0]
XL PDATA[10E]

3V3
2V5
C739 4.7uF 0.1uF 25V 16V
C740 0.1uF 25V 16V
EPB PDATA[23]
EPB PDATA[22]
EPB PDATA[21]
EPB PDATA[20]
EPB PDATA[19]
EPB PDATA[18]
EPB PDATA[17]
EPB PDATA[16]
EPB PDATA[15]
EPB PDATA[14]
EPB PDATA[13]
EPB PDATA[12]
EPB PDATA[11]
EPB PDATA[10]
EPB PDATA[9]
EPB PDATA[8]
EPB PDATA[7]
EPB PDATA[6]
EPB PDATA[5]
EPB PDATA[4]
EPB PDATA[3]
EPB PDATA[2]
EPB PDATA[1]
EPB PDATA[0]
EPB PDATA[10E]

XL PDATA[23]
XL PDATA[22]
XL PDATA[21]
XL PDATA[20]
XL PDATA[19]
XL PDATA[18]
XL PDATA[17]
XL PDATA[16]
XL PDATA[15]
XL PDATA[14]
XL PDATA[13]
XL PDATA[12]
XL PDATA[11]
XL PDATA[10]
XL PDATA[9]
XL PDATA[8]
XL PDATA[7]
XL PDATA[6]
XL PDATA[5]
XL PDATA[4]
XL PDATA[3]
XL PDATA[2]
XL PDATA[1]
XL PDATA[0]
XL PDATA[10E]

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Johannesburg
South Africa

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PCB FILENAME: <Filename.PcbDoc>

DRAWN BY: <DRAWN BY> APPROVED: <ENGINEER>

CIRCUIT DIAGRAM
<PROJECT TITLE>
<SPECIFIC SHEET FUNCTION>

DATE: 24-06-2009
SHEET: 26 OF 26
REVISION: <1.00>

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