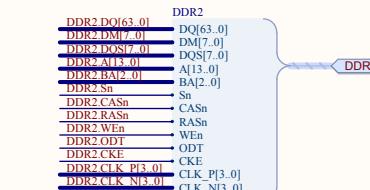
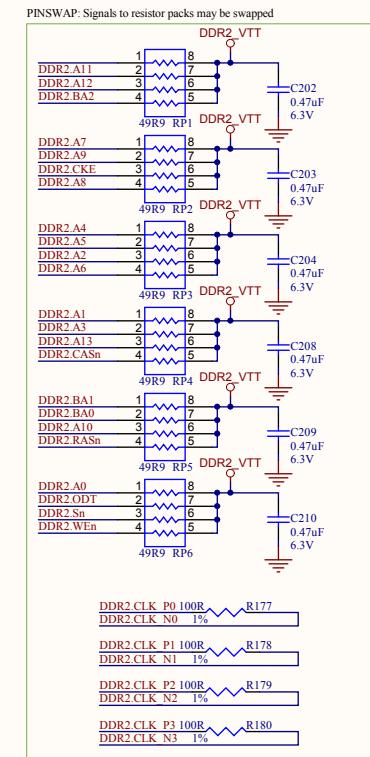
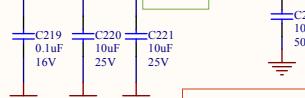
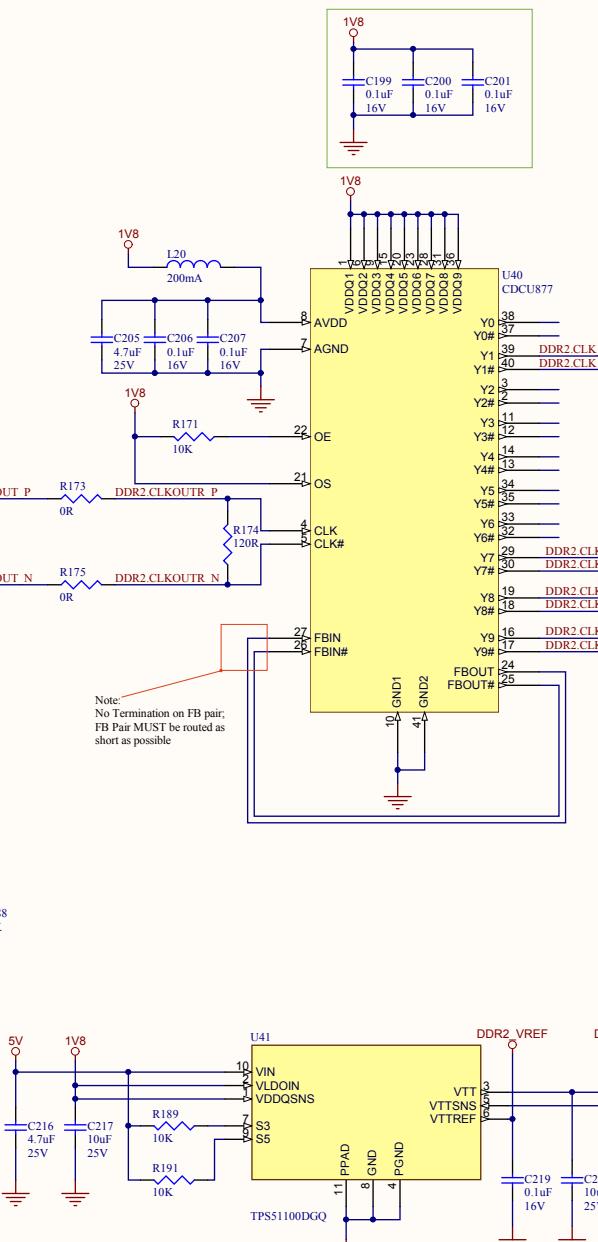
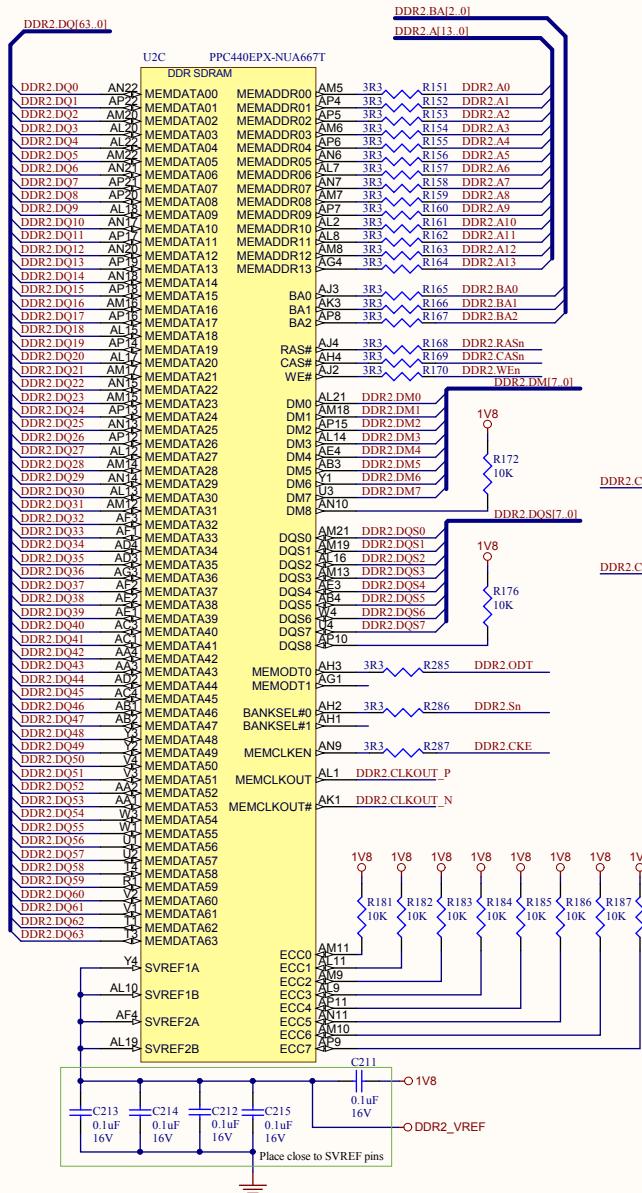
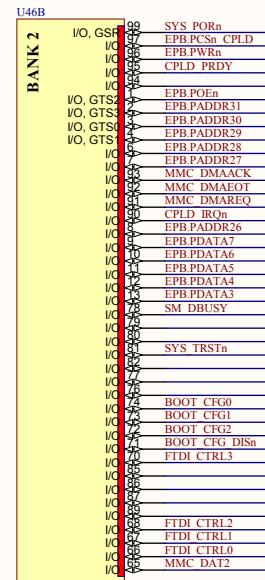
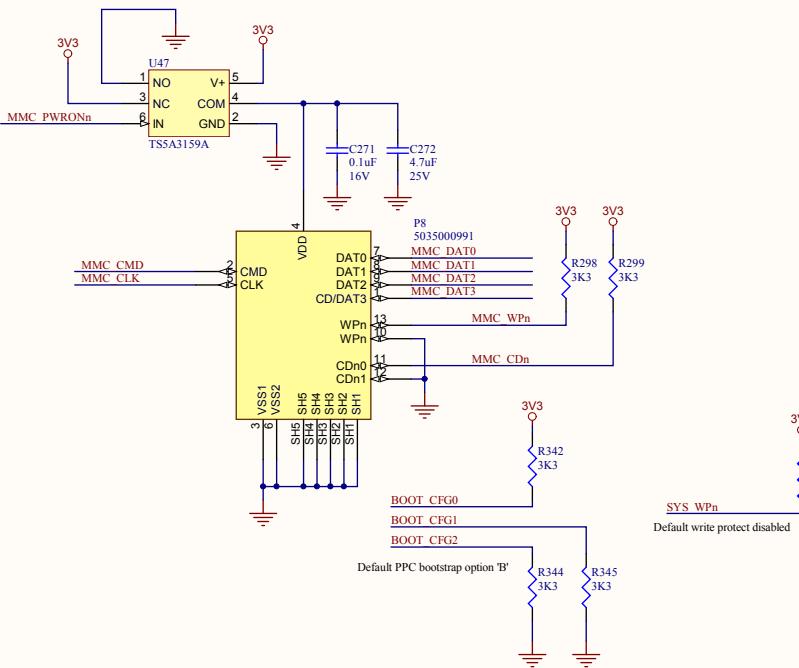
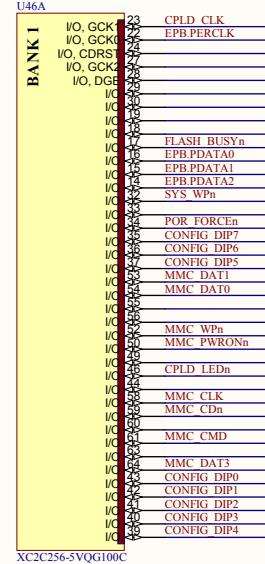


A



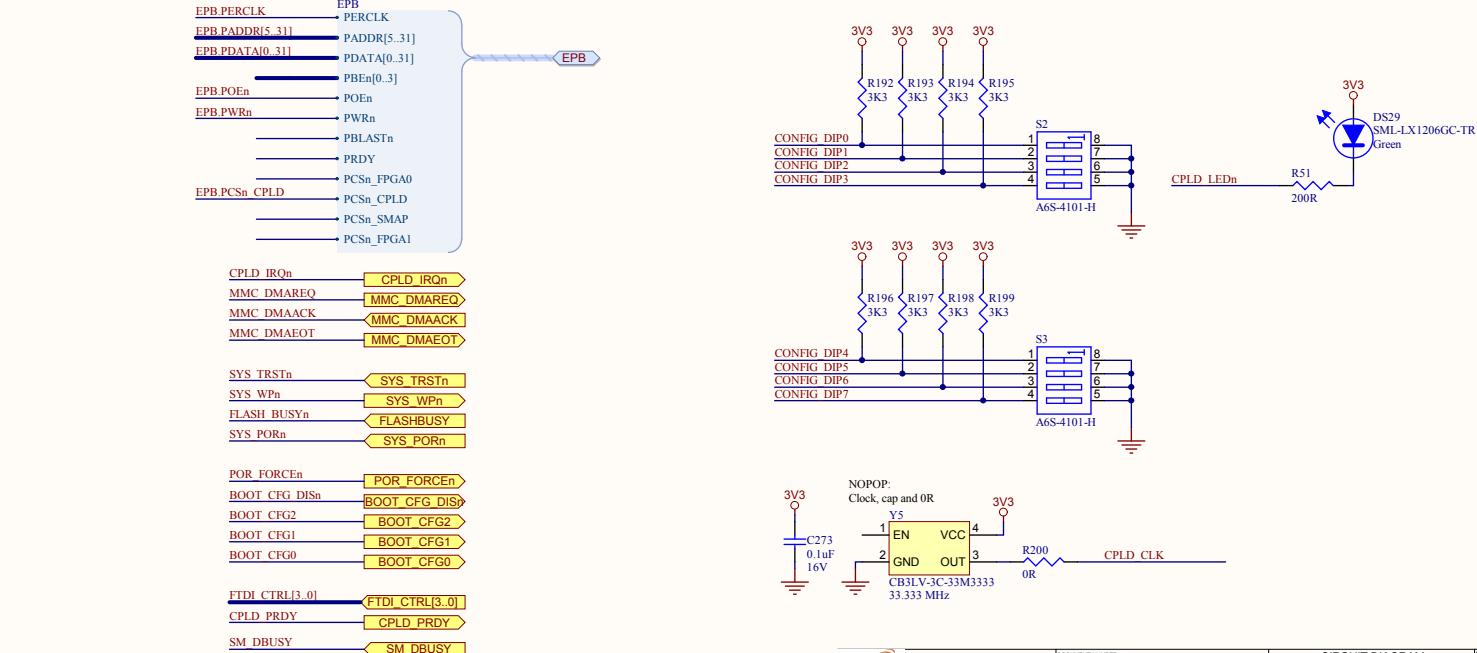


PINSWAP:  
 CPLD\_CLK and EPB\_PERCLK MUST go on GCK pins  
 SYS\_PORn MUST go on GSR pin  
 EPB\_POWEn MUST go on GTS pin  
 Otherwise, swap away

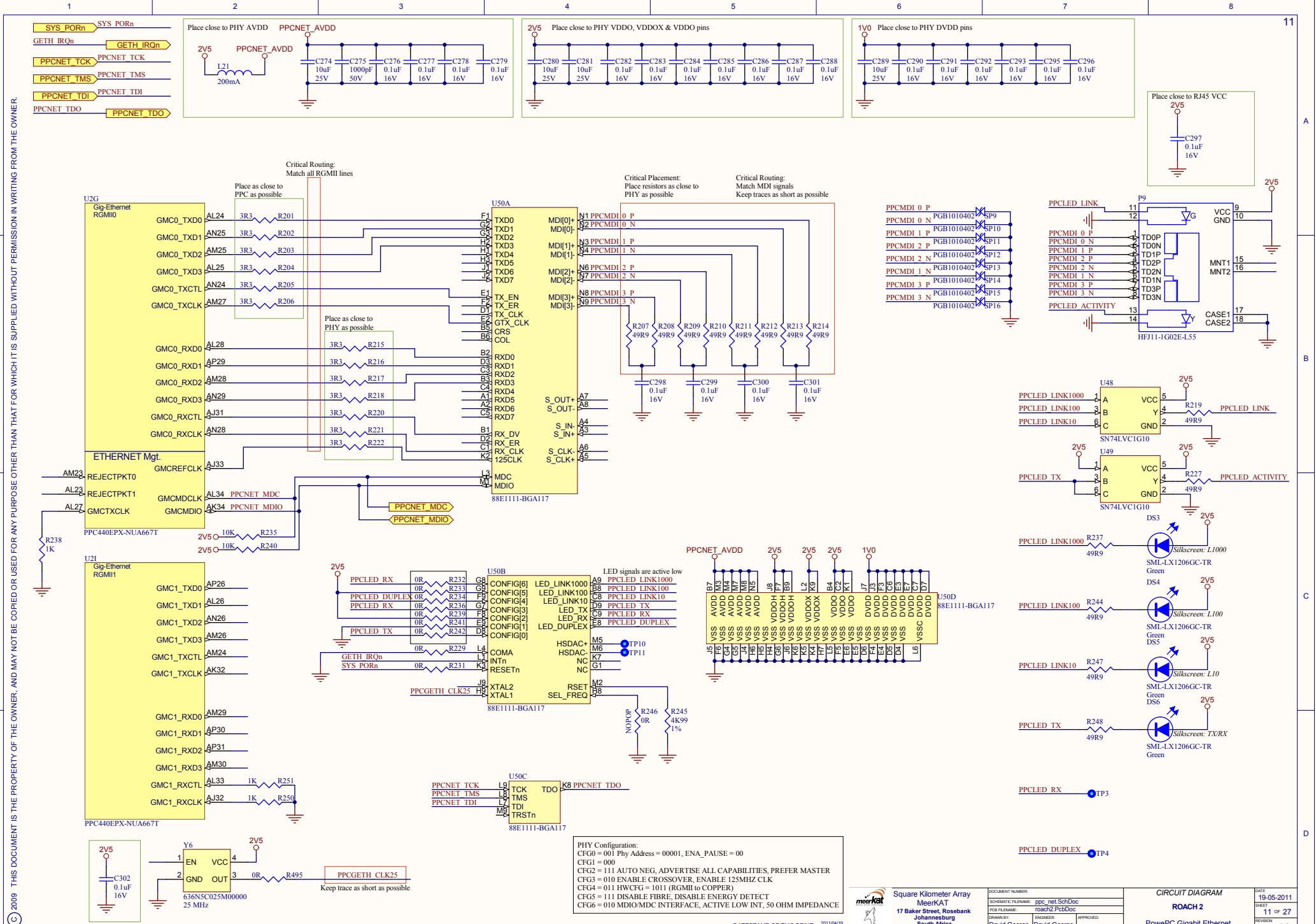


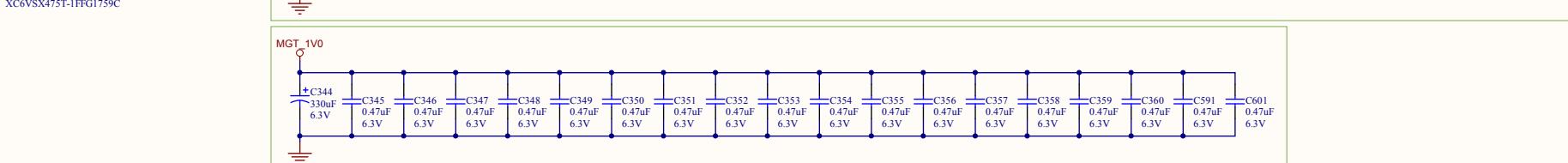
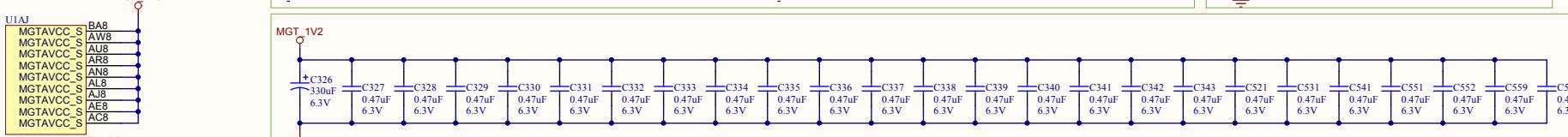
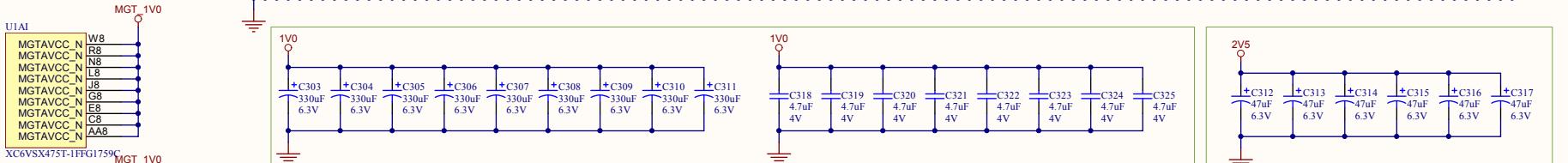
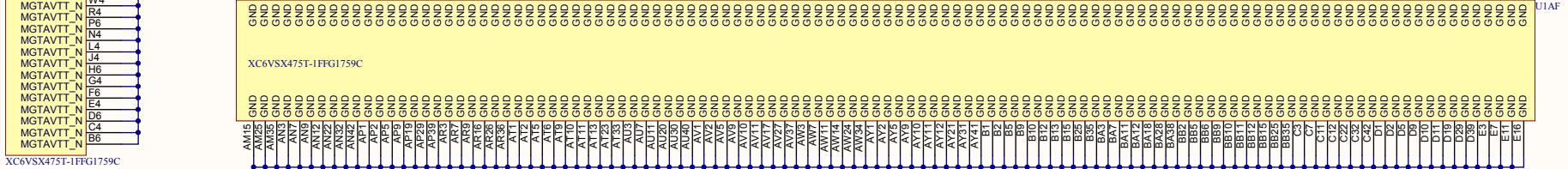
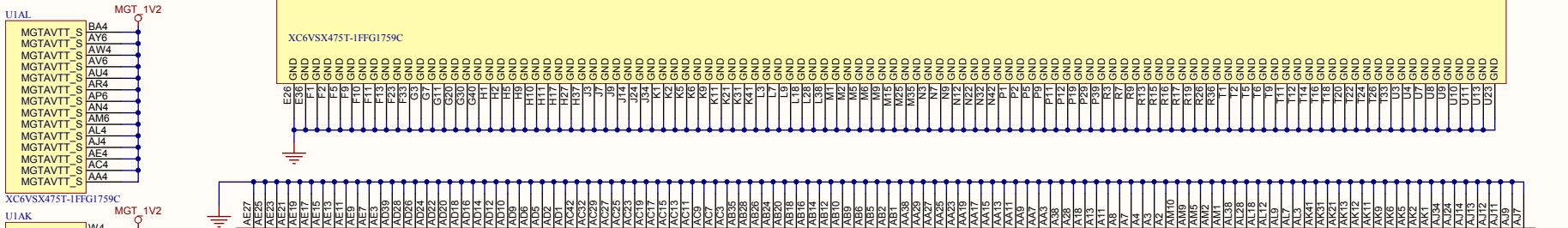
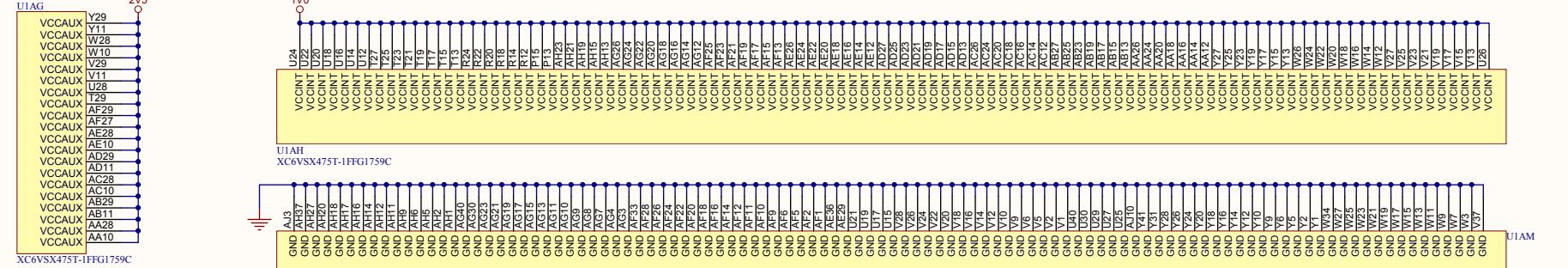
XC2C256-5VQG100C

XC2C256-5VQG100C

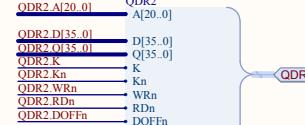
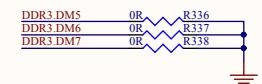
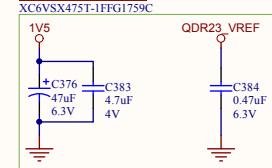
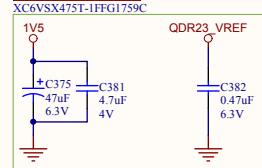
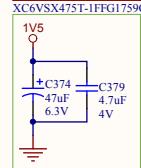
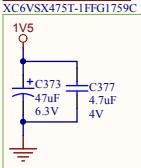
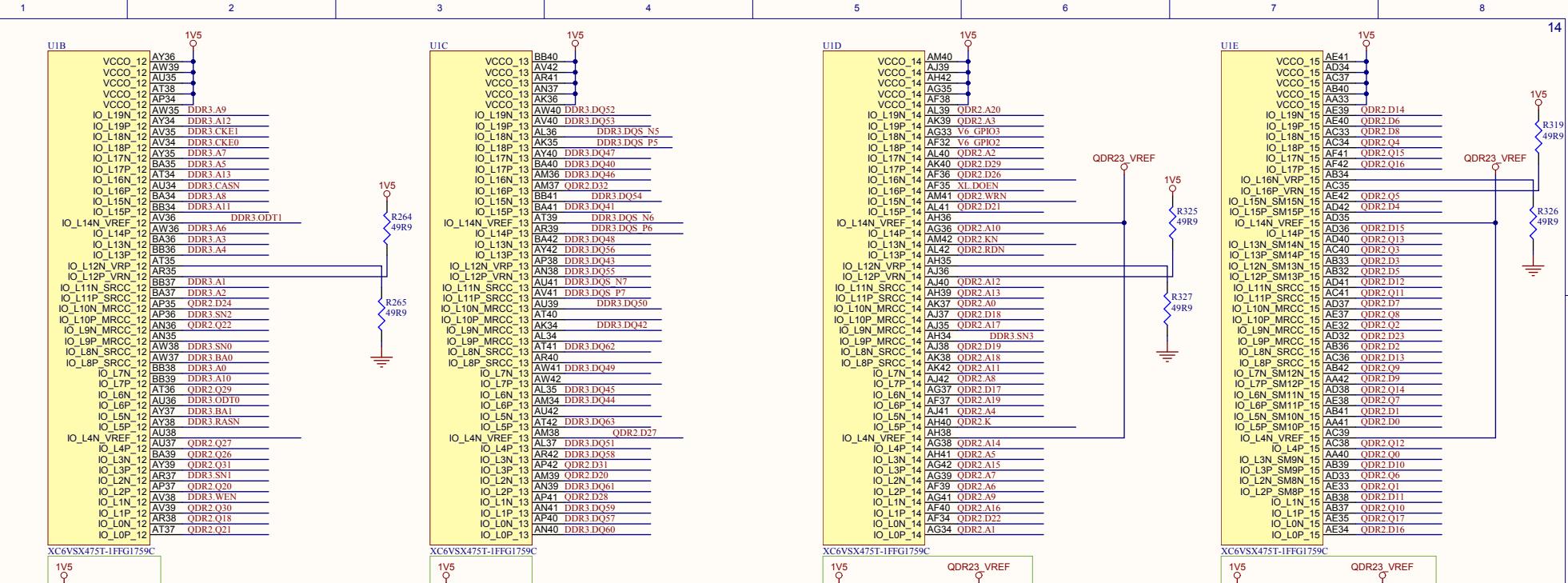


XC2C256-5VQG100C



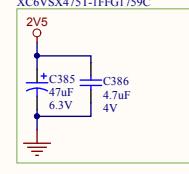
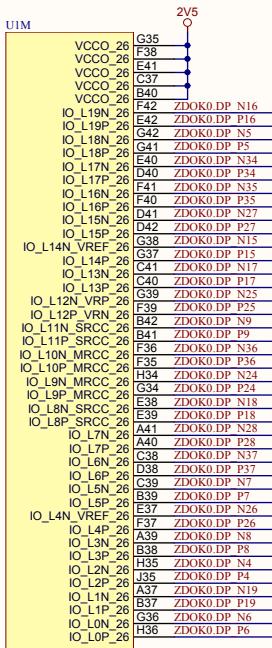
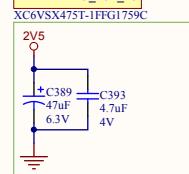
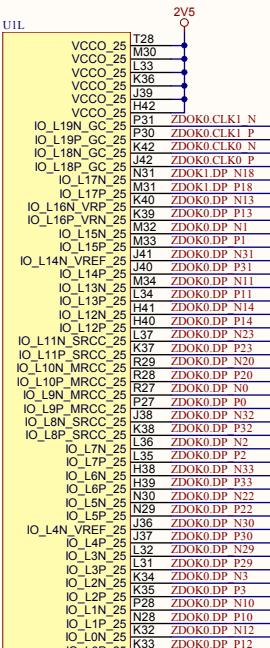
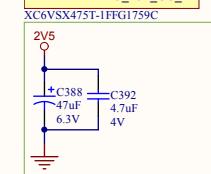
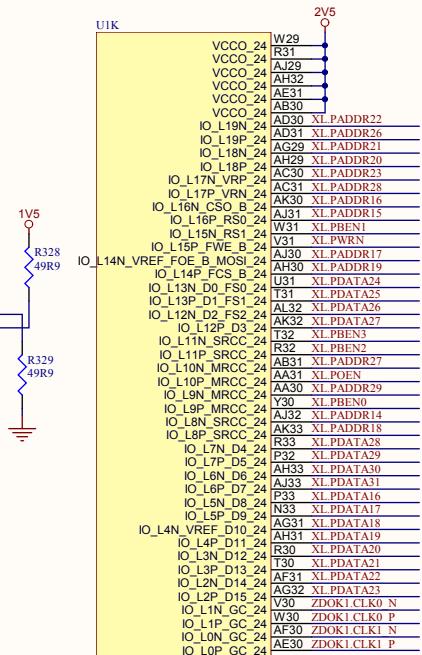
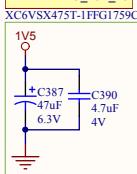
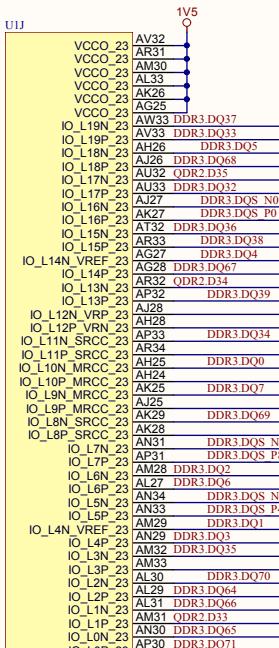




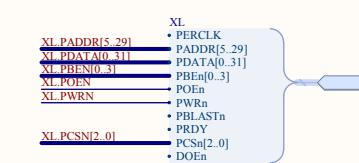
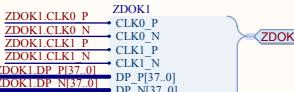
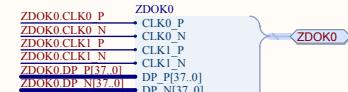
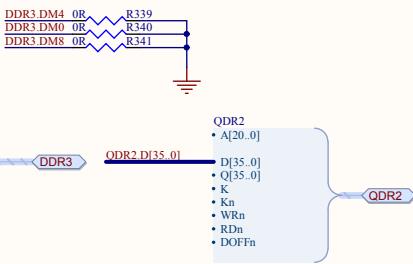


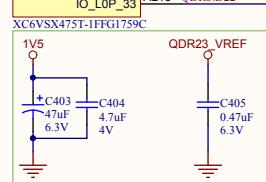
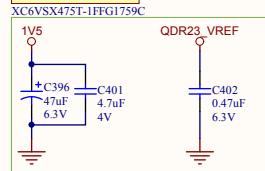
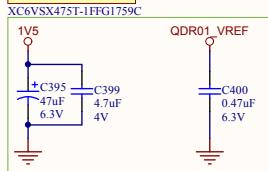
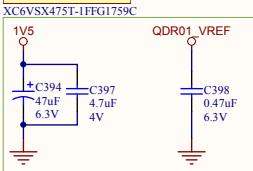
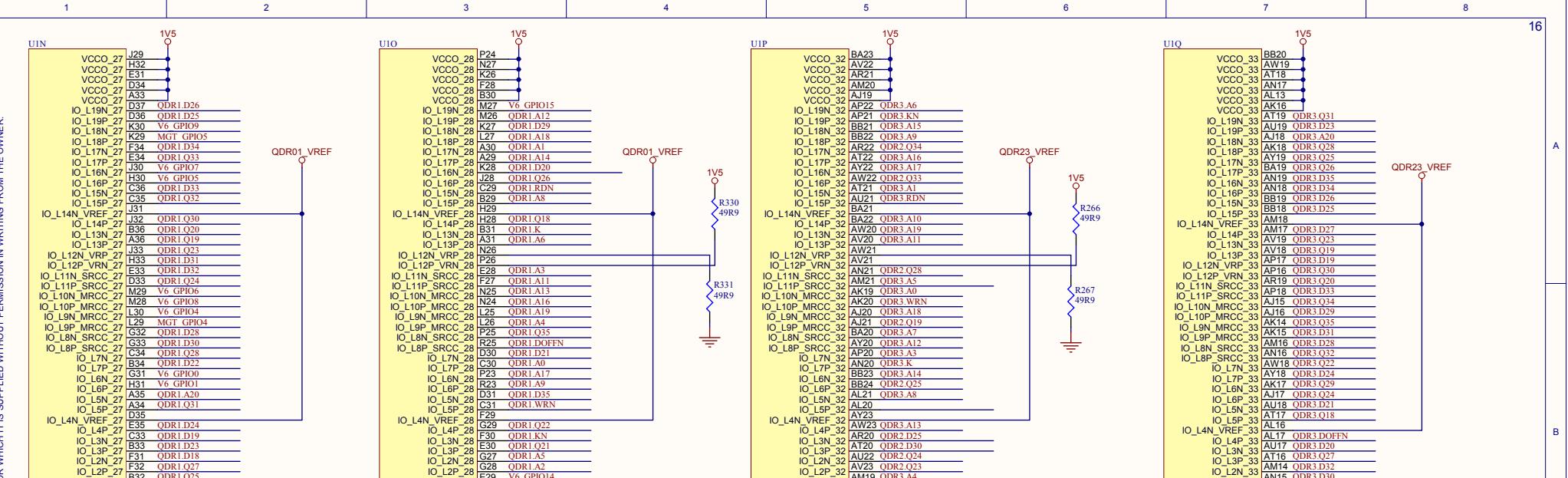
- PERCLK
- PAD9[5..29]
- PDATA[0..31]
- PDEN[0..3]
- POE
- PWRn
- PHLASTIn
- PRDY
- PCSEL[2..0]
- DOEn

A

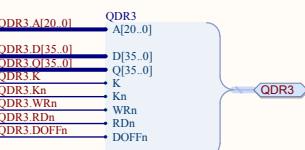
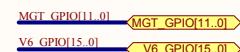
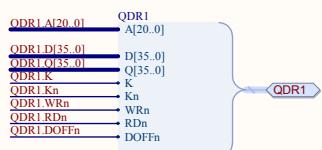


|                          |  |
|--------------------------|--|
| <b>DDR3 DQ[71..0]</b>    | DQ[71..0]  |
| <b>DDR3 DM[8..0]</b>     | DM[8..0]   |
| <b>DDR3 DQS P8[0..3]</b> | DQS P8[0..3]   |
| <b>DDR3 DQS N8[0..3]</b> | DQS N8[0..3]   |
|                          | <ul style="list-style-type: none"> <li>• A[15..0]</li> <li>• BA[2..0]</li> <li>• Sn[3..0]</li> <li>• CASN</li> <li>• RASn</li> <li>• WEn</li> <li>• ODT</li> <li>• ODT0</li> <li>• CKE1</li> <li>• CKE0</li> <li>• CK_P</li> <li>• CK_N</li> <li>• RESEtN</li> </ul> |

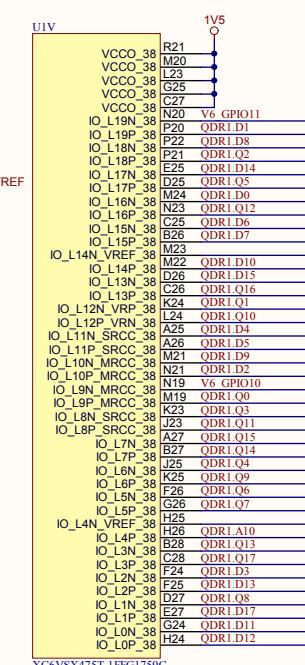
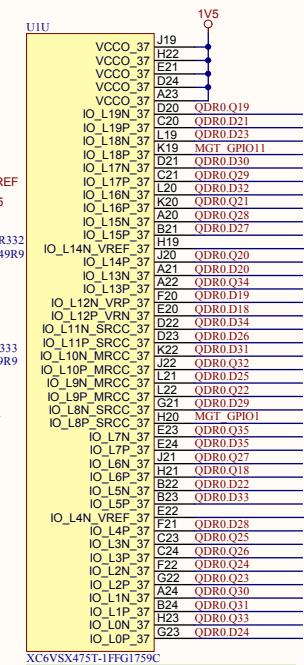
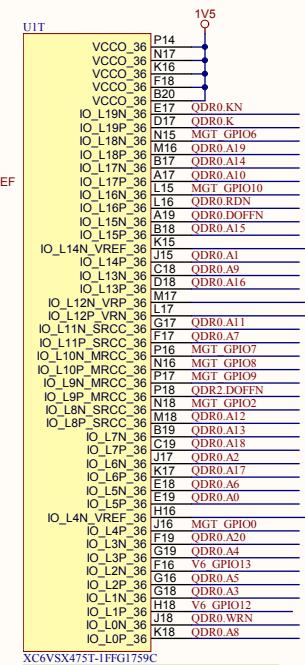
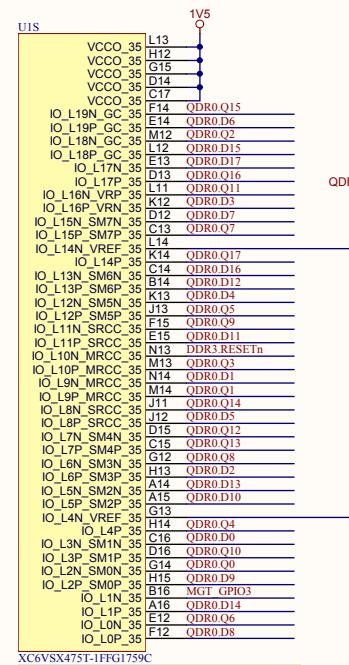
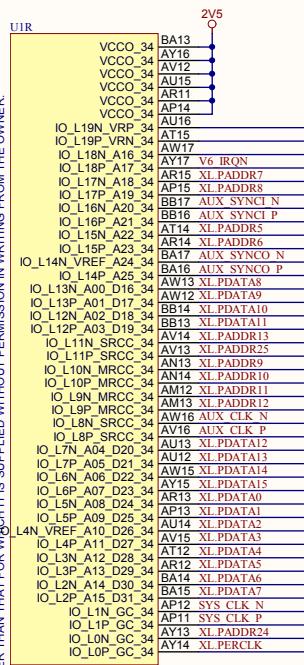




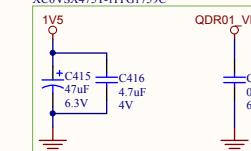
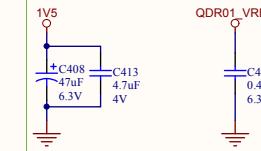
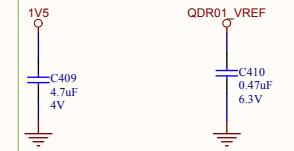
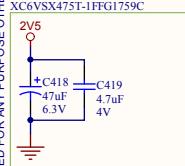
Device Compatibility:  
Bank 28 unavailable on  
LX240T/LX365T/SX315T



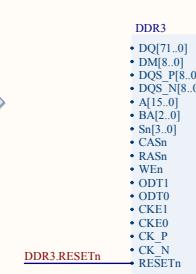
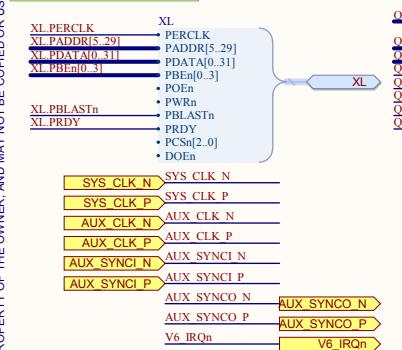
A  
B



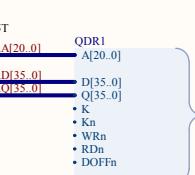
卷之三

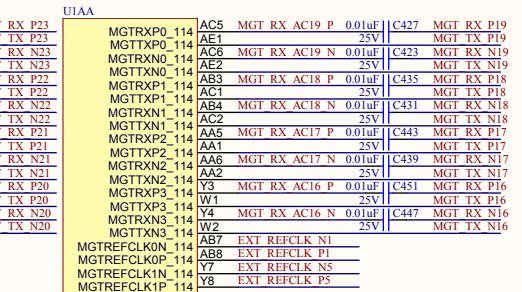
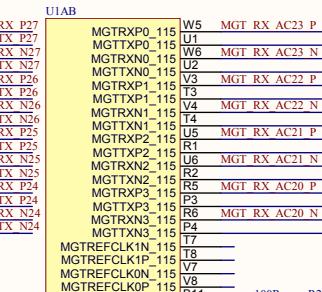
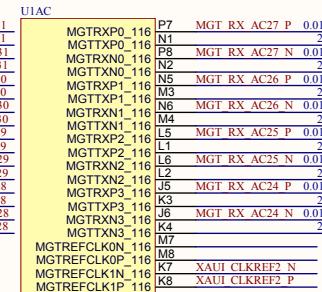
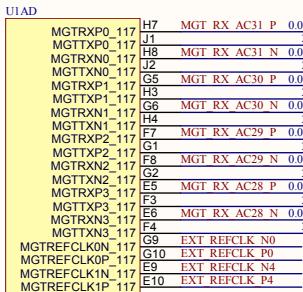


D

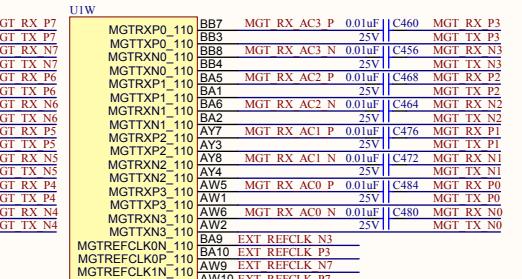
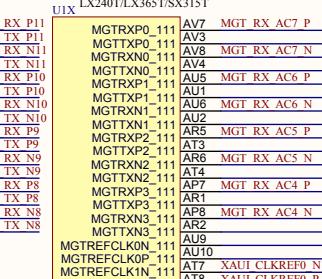
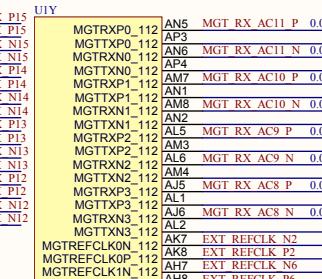
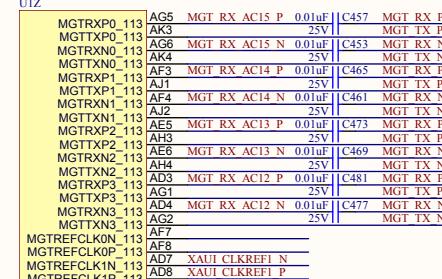


Device Compatibility:  
Bank 38 unavailable on  
LX240T/LX365T/SX315

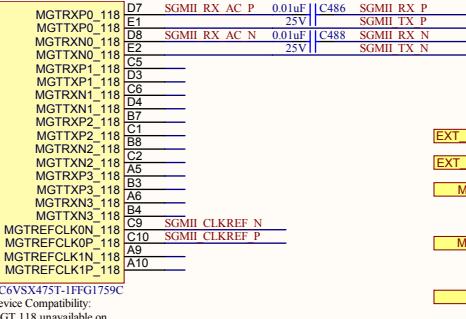
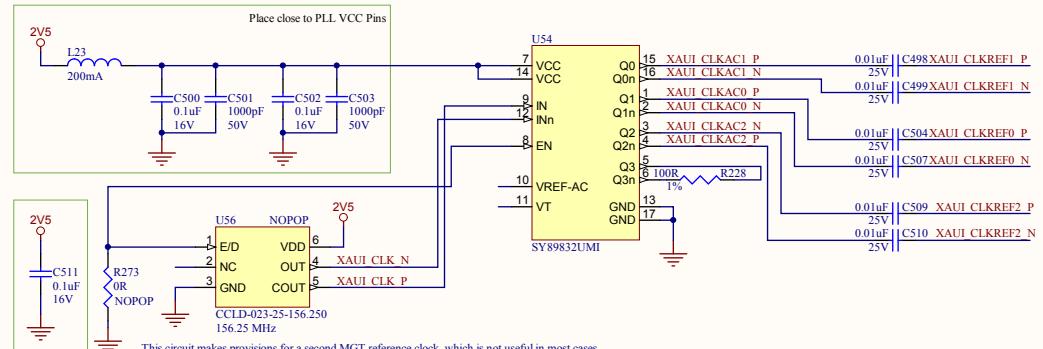




XC6VSX475T-1FFG1759C



XC6VSX475T-1FFG1759C

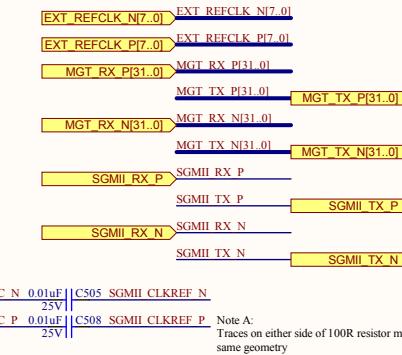


XC6VSX475T-1FFG1759C

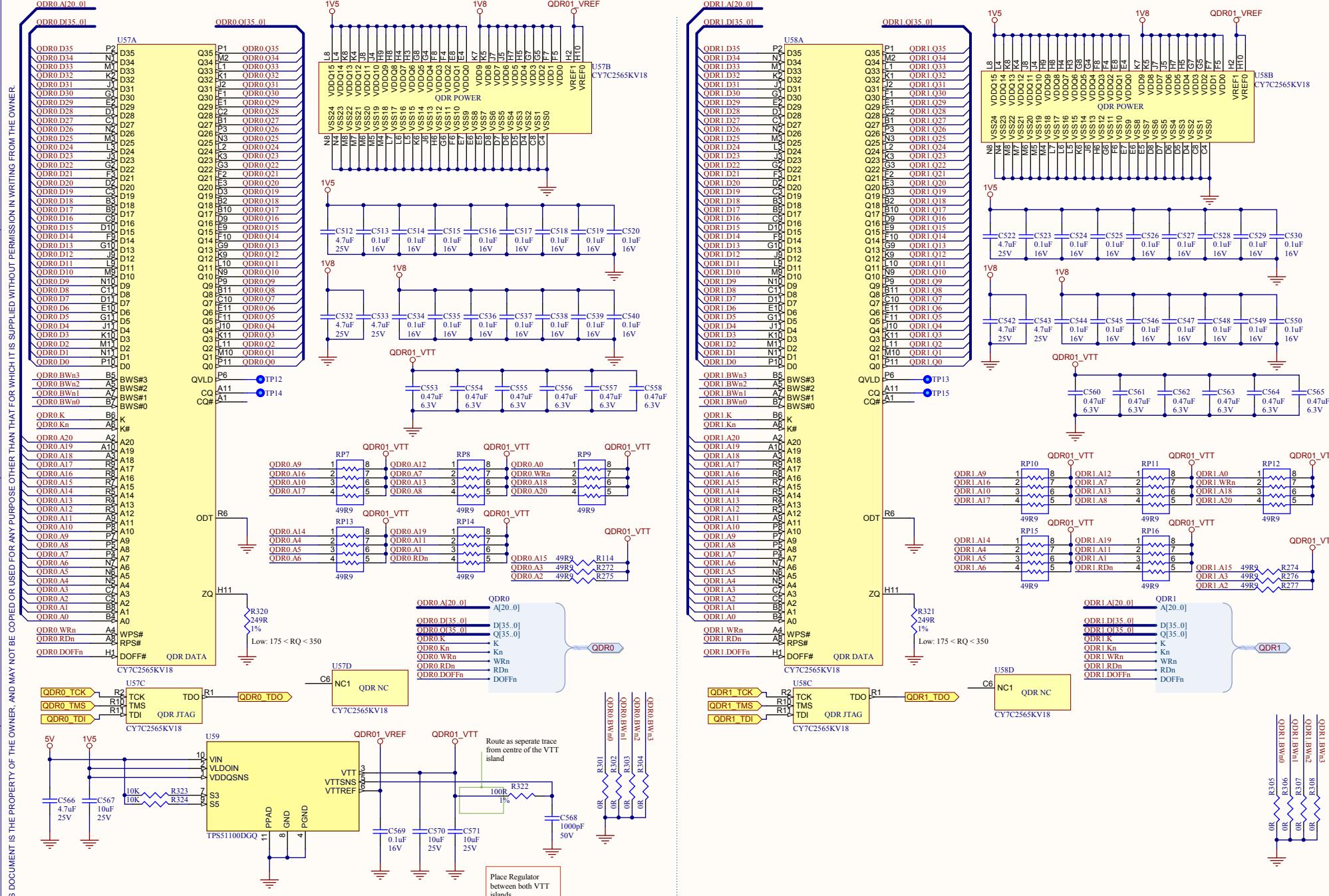
Device Compatibility:

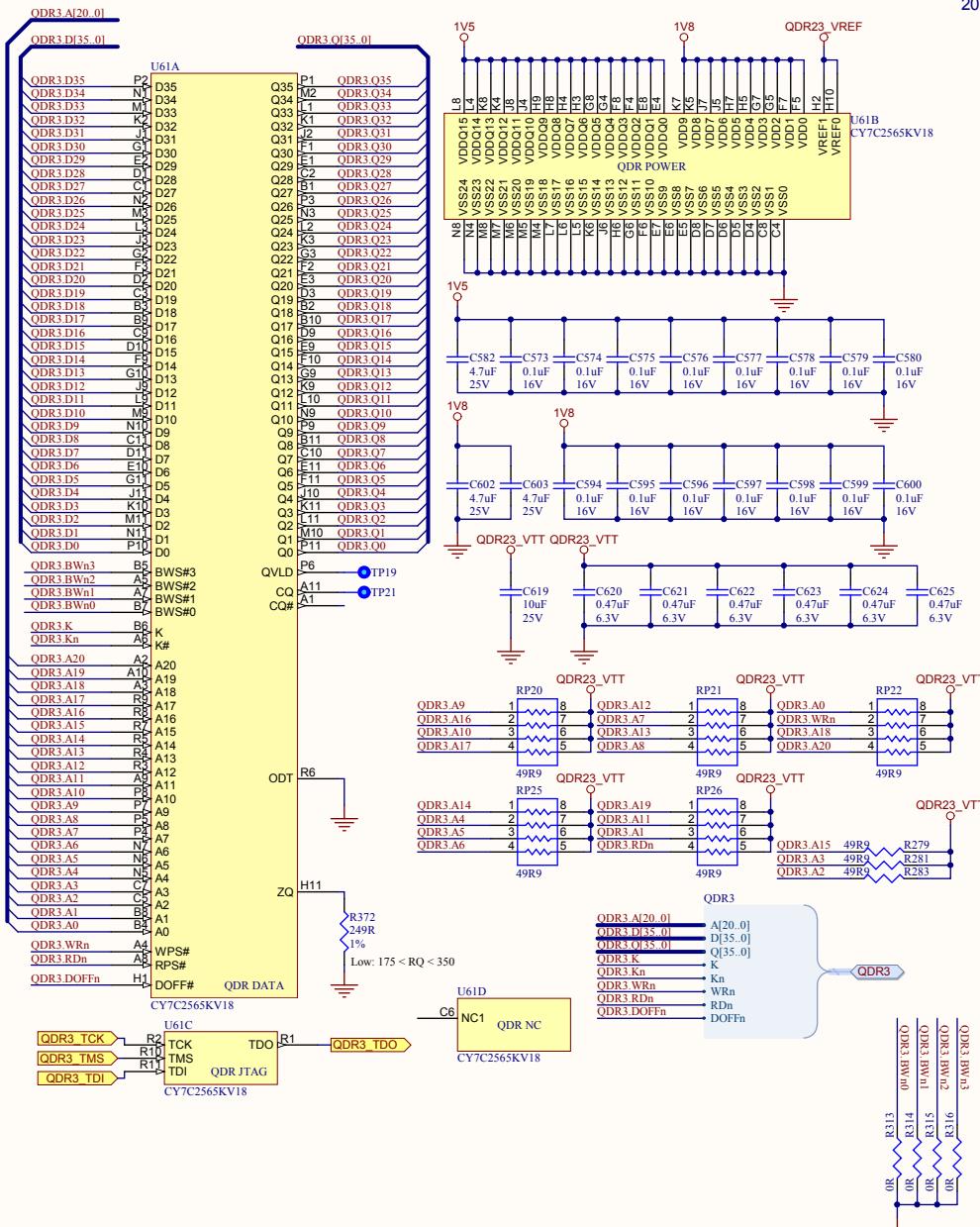
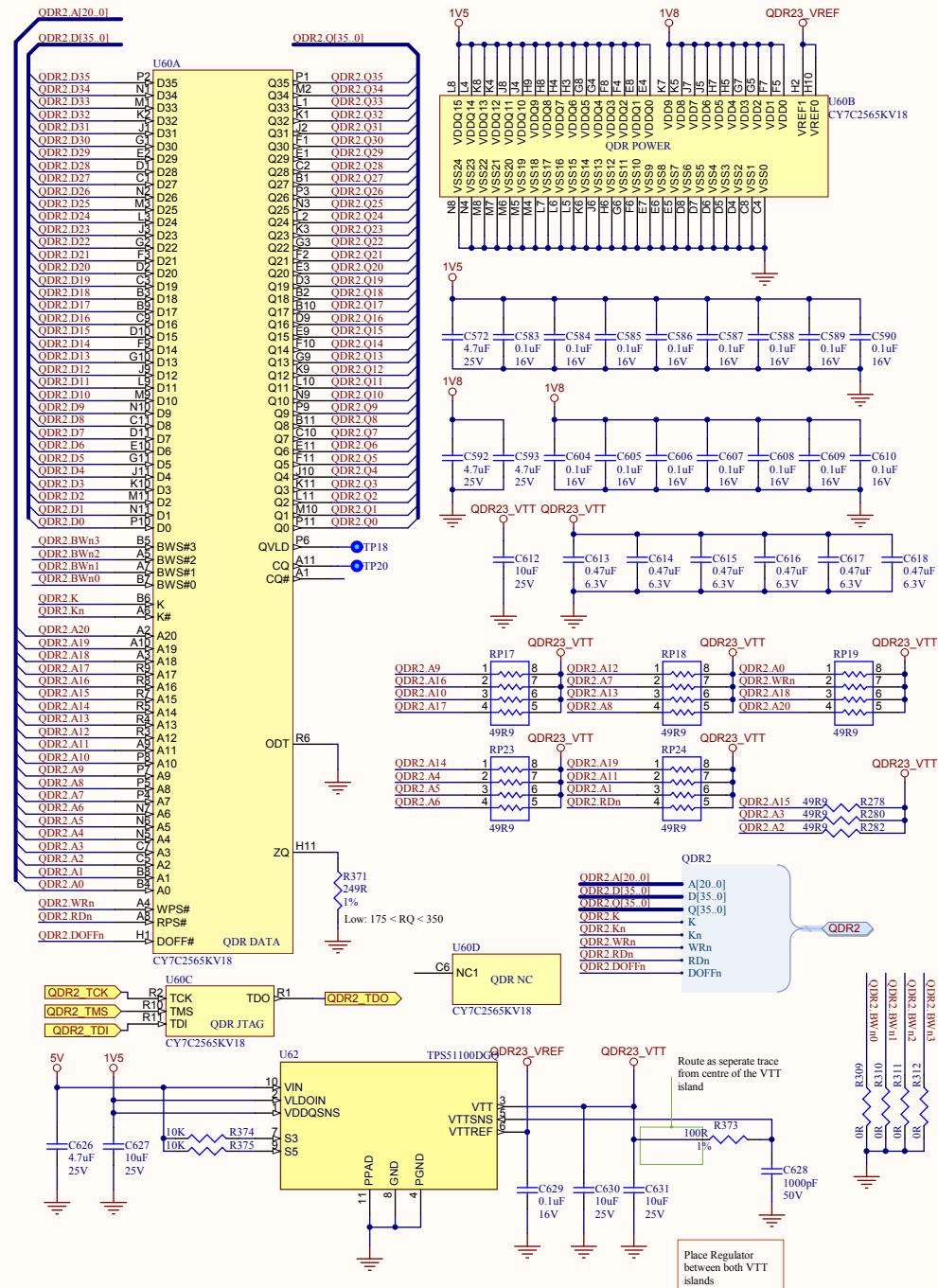
MGT 111 unavailable on

LX240T/LX365T/SX315T

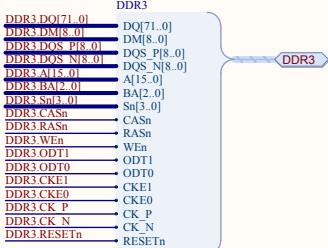


XC6VSX475T-1FFG1759C

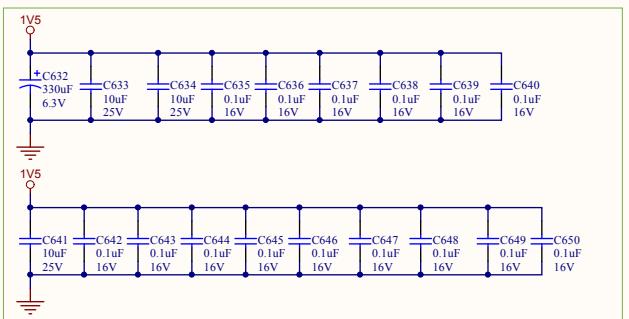




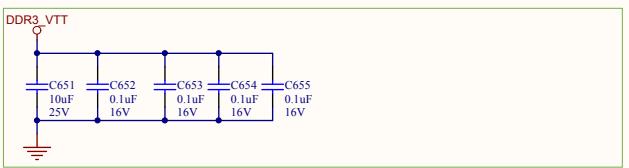
A



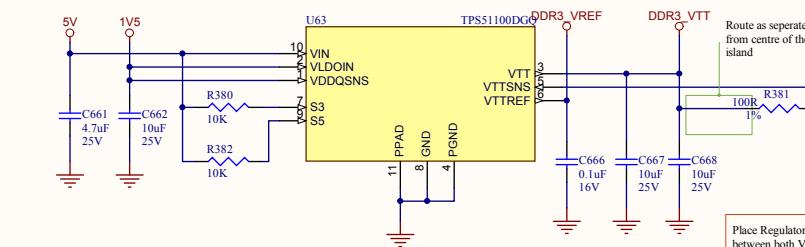
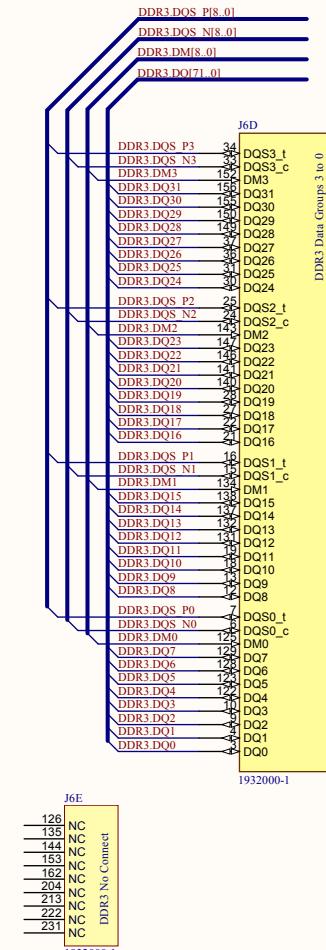
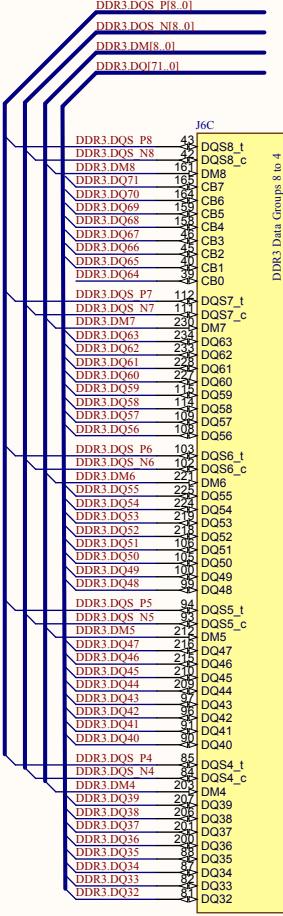
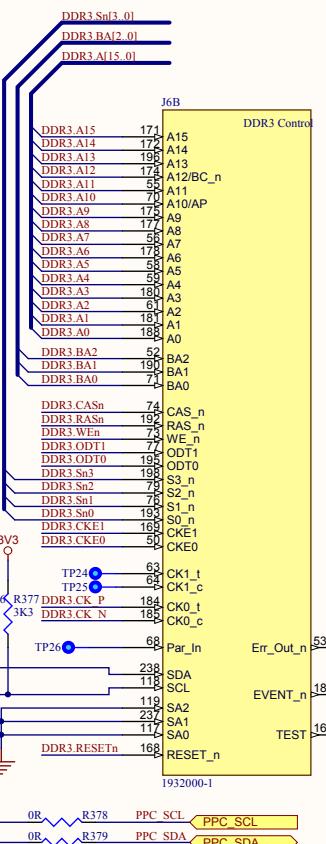
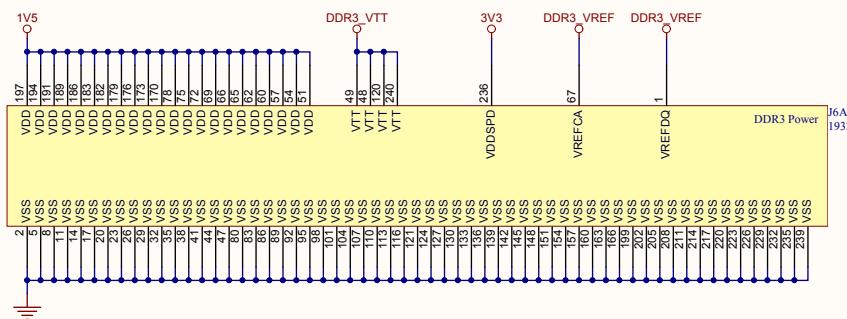
B

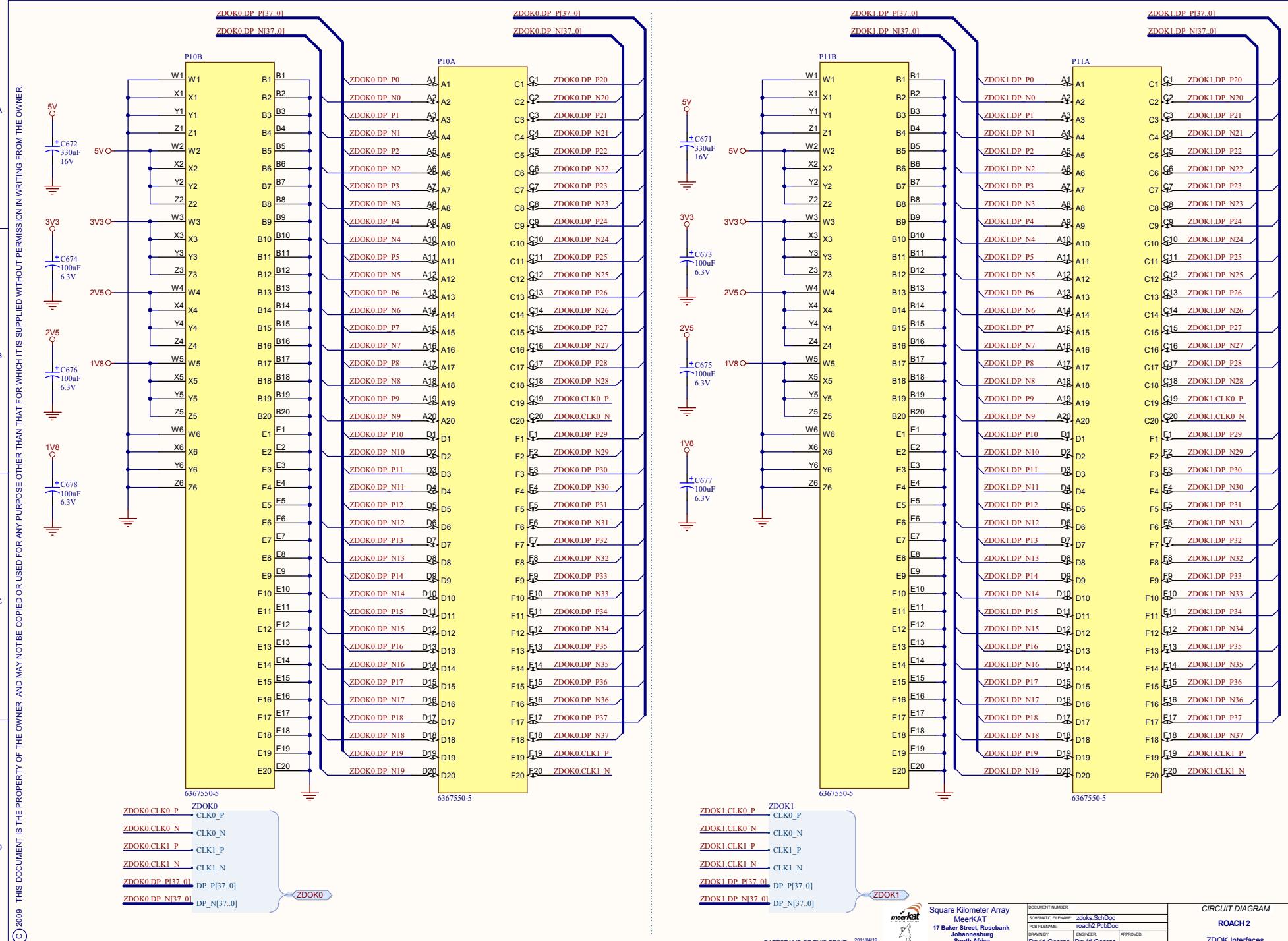


C

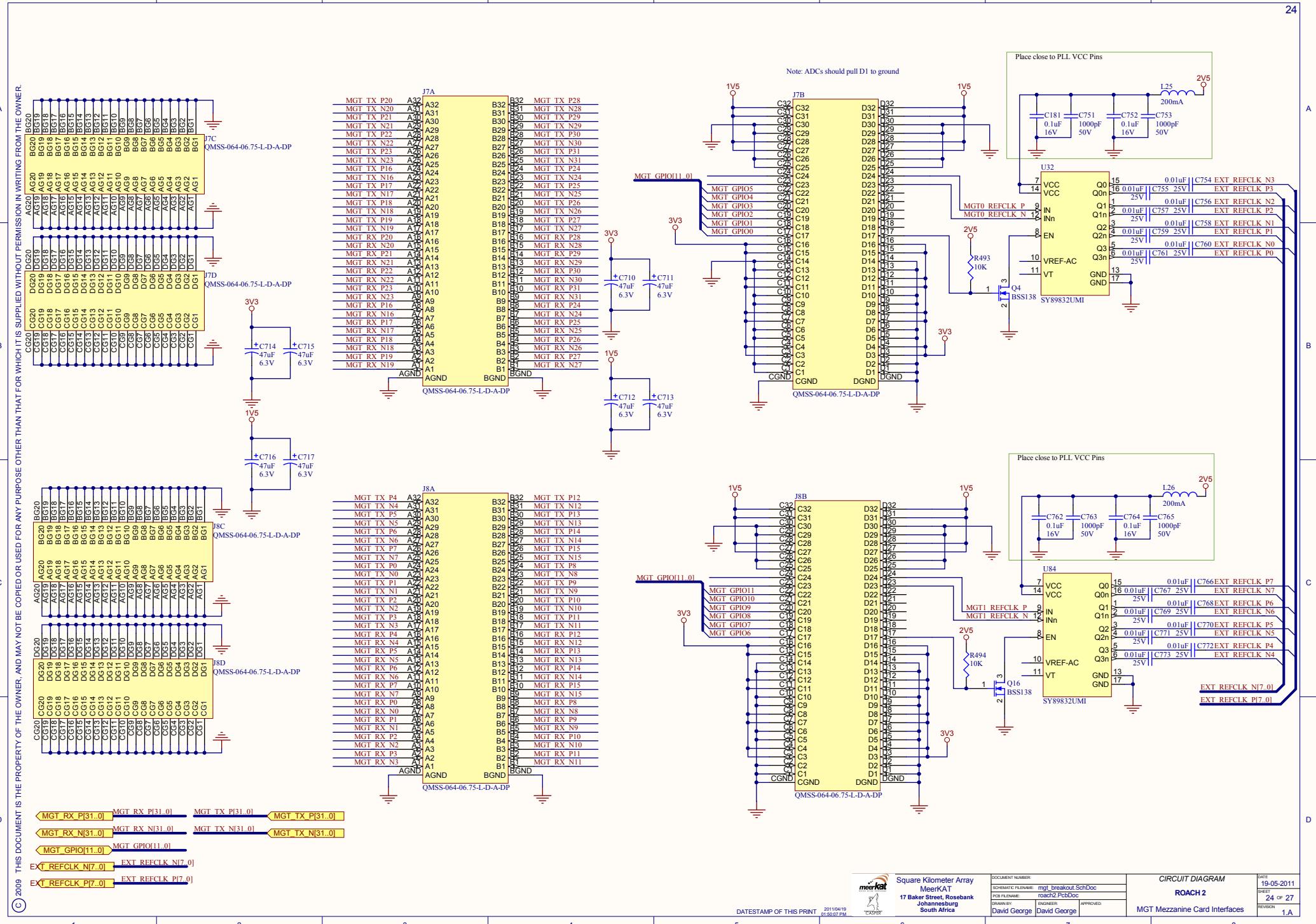


D

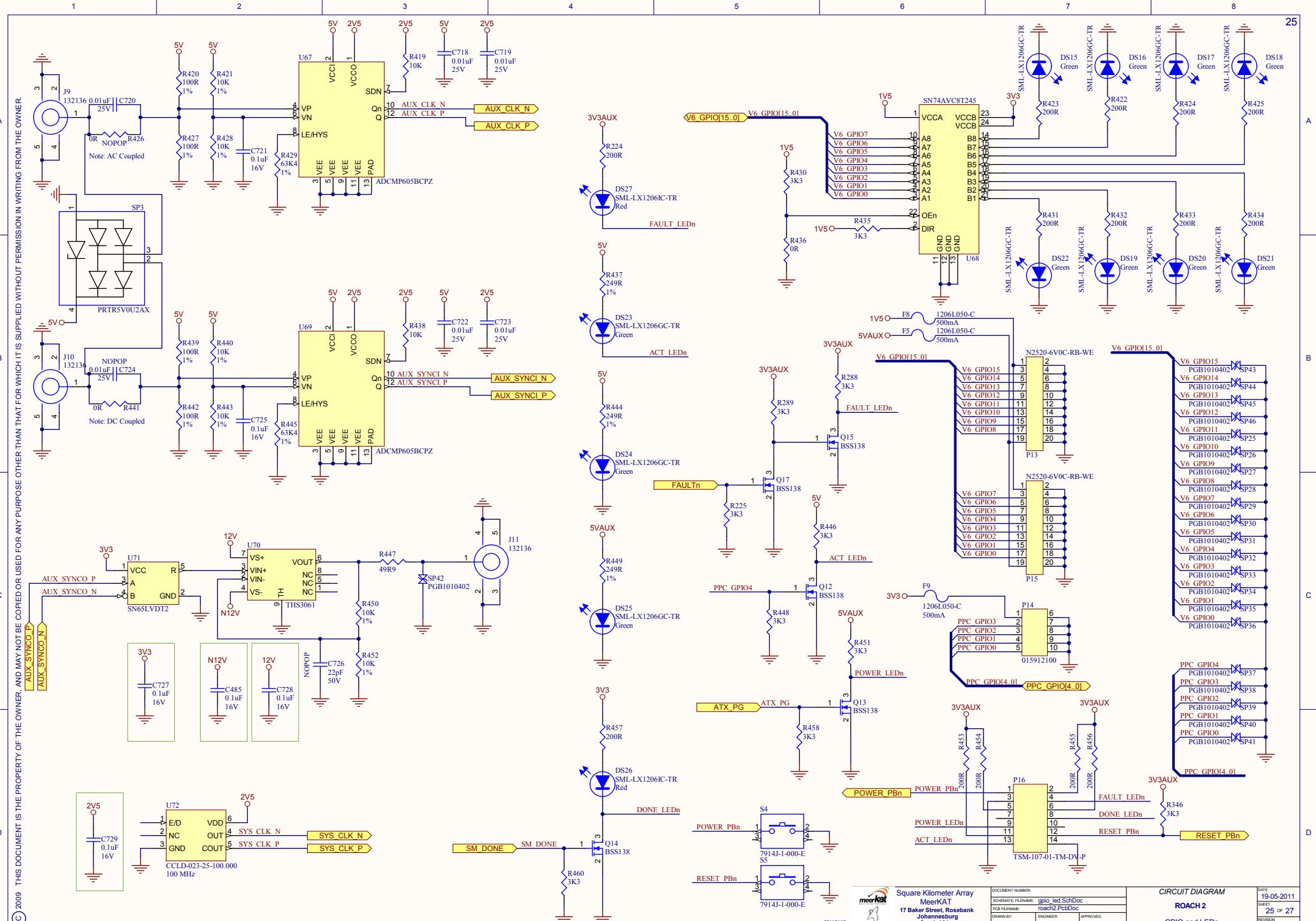


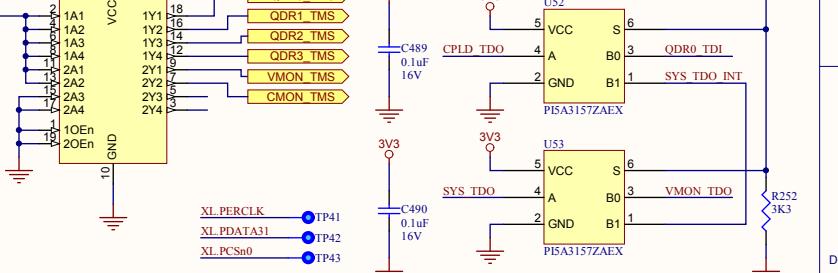
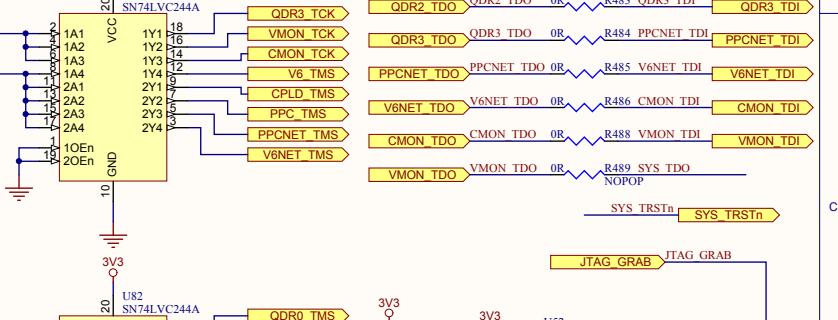
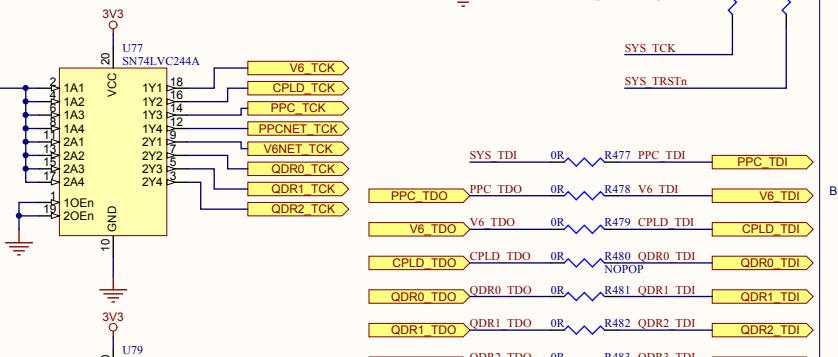
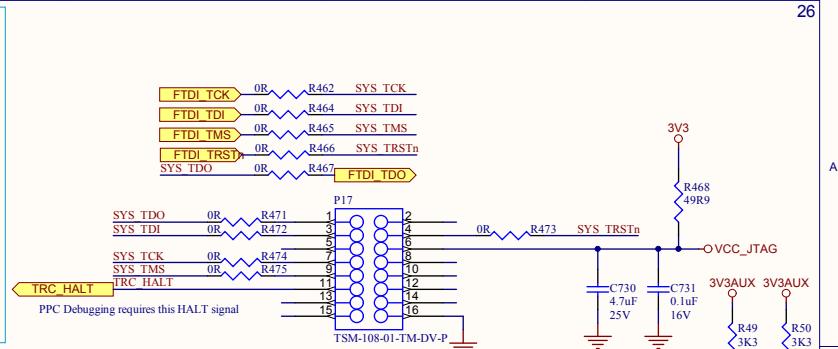
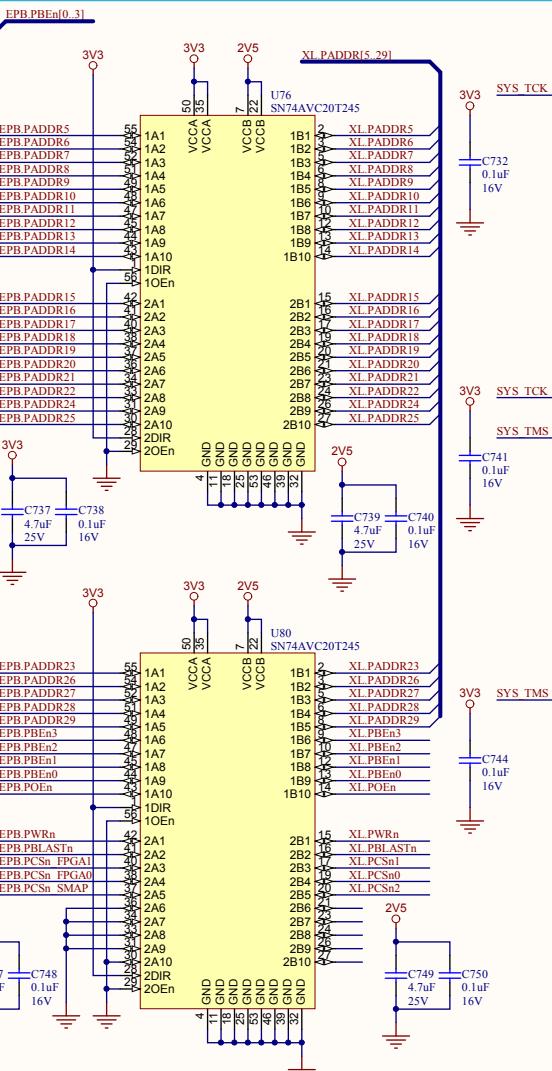
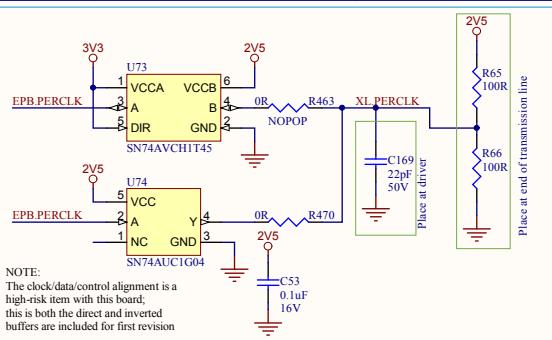
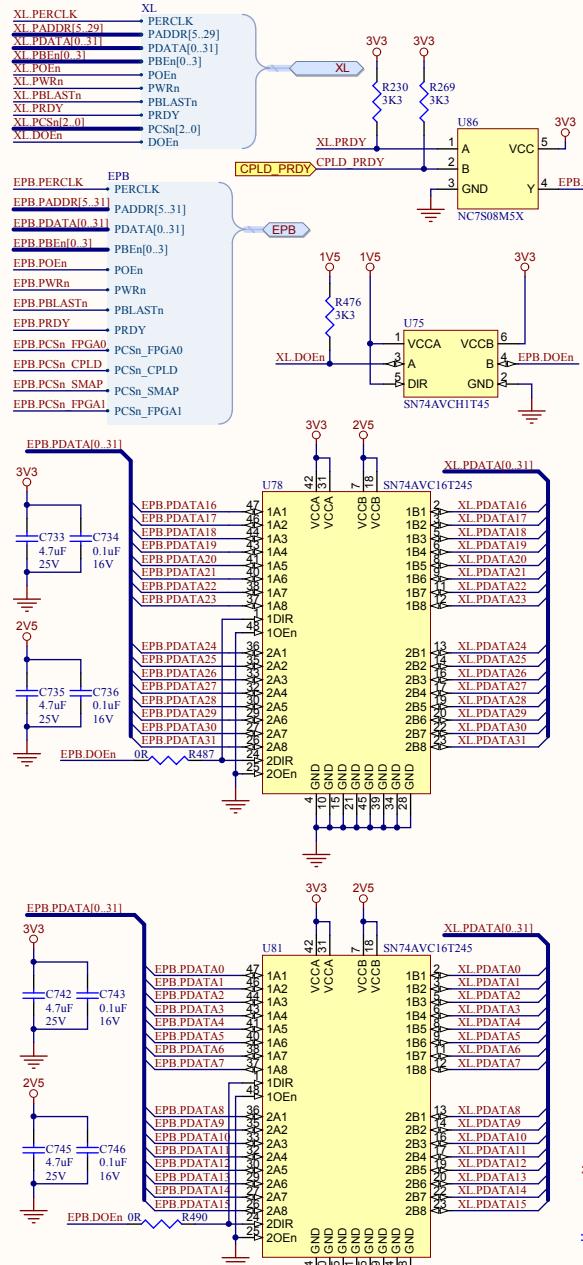






© 2000 THIS DOCUMENT IS THE PROPERTY OF THE OWNER AND MAY NOT BE COPIED OR USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH IT WAS PROVIDED. WITHOUT PERMISSION FROM THE OWNER





| DOCUMENT NUMBER:    |              | CIRCUIT DIAGRAM        |              | DATE:      |     |
|---------------------|--------------|------------------------|--------------|------------|-----|
| SCHEMATIC FILENAME: |              | ROACH 2                |              | 19-05-2011 |     |
| PCB FILENAME:       |              | JTAG_LevelTrans.SchDoc |              | SPEC:      |     |
| DRAWN BY:           | David George | ENGINEER:              | David George | APPROVED:  |     |
| TESTED BY:          |              | DATE:                  |              | REVISION:  | 1.A |
| SPEC:               | 26           | OF                     | 27           |            |     |
| DATE:               | 2011/04/19   | 01:50:08 PM            | CAPER        | TESTED:    |     |
| TESTED:             |              | BY:                    |              | REVISION:  | 1.A |

A

B

C

D

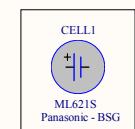
A

B

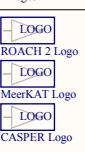
C

D

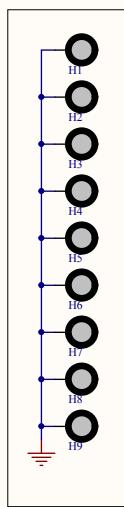
Real-Time Clock Battery



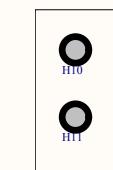
Logos



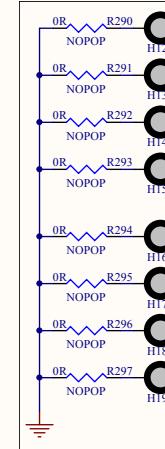
ATX Mounting Holes



ATX FAN Mounting Holes



Mezzanine Card Mounting Holes



Global Fiducials

