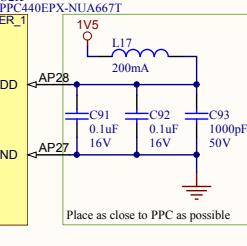
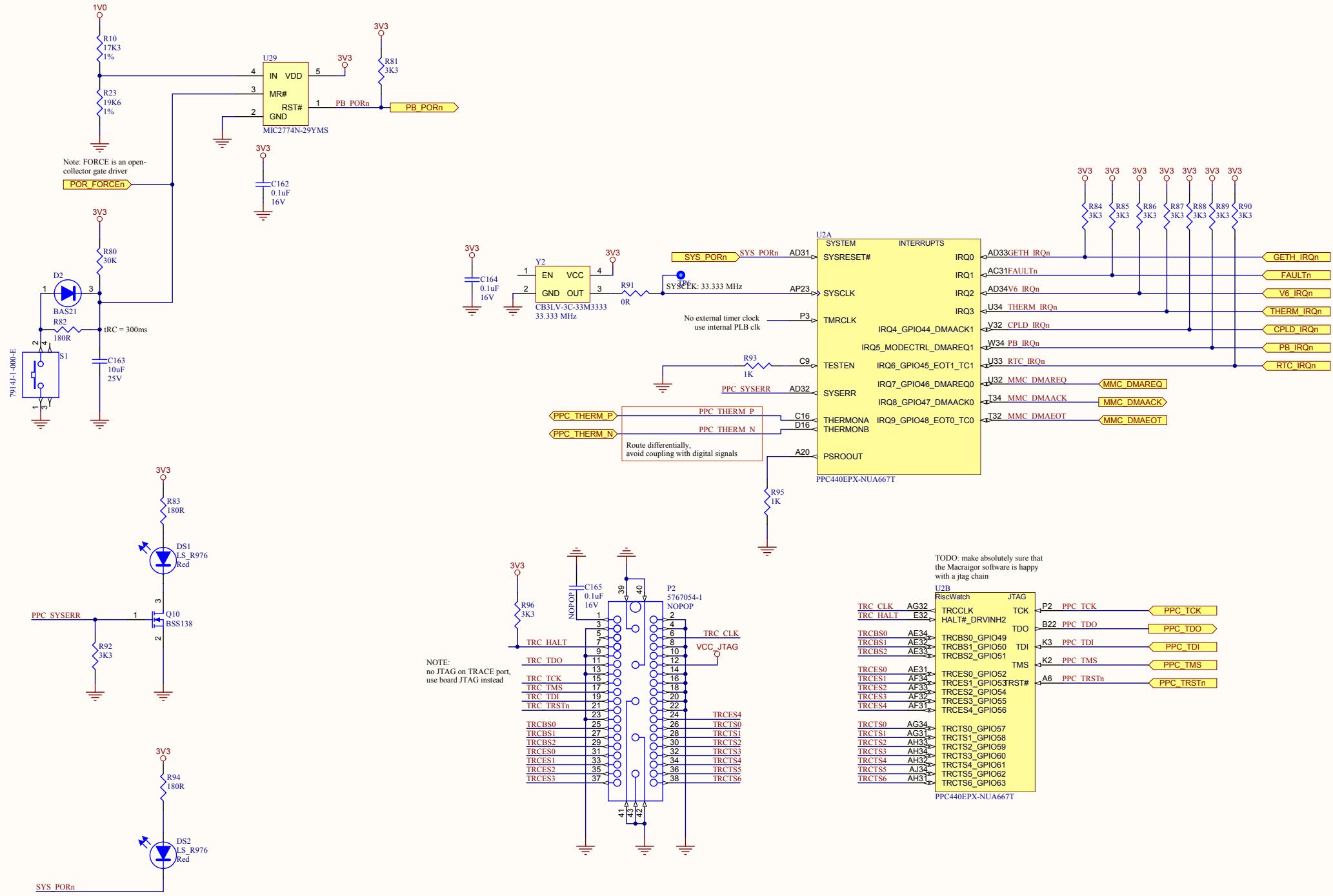


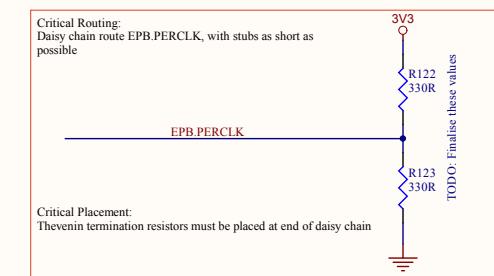
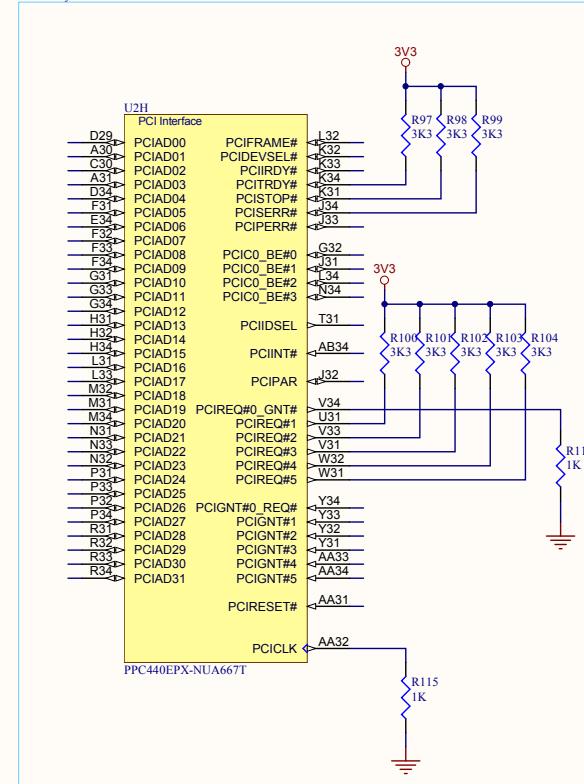
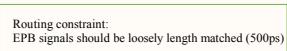
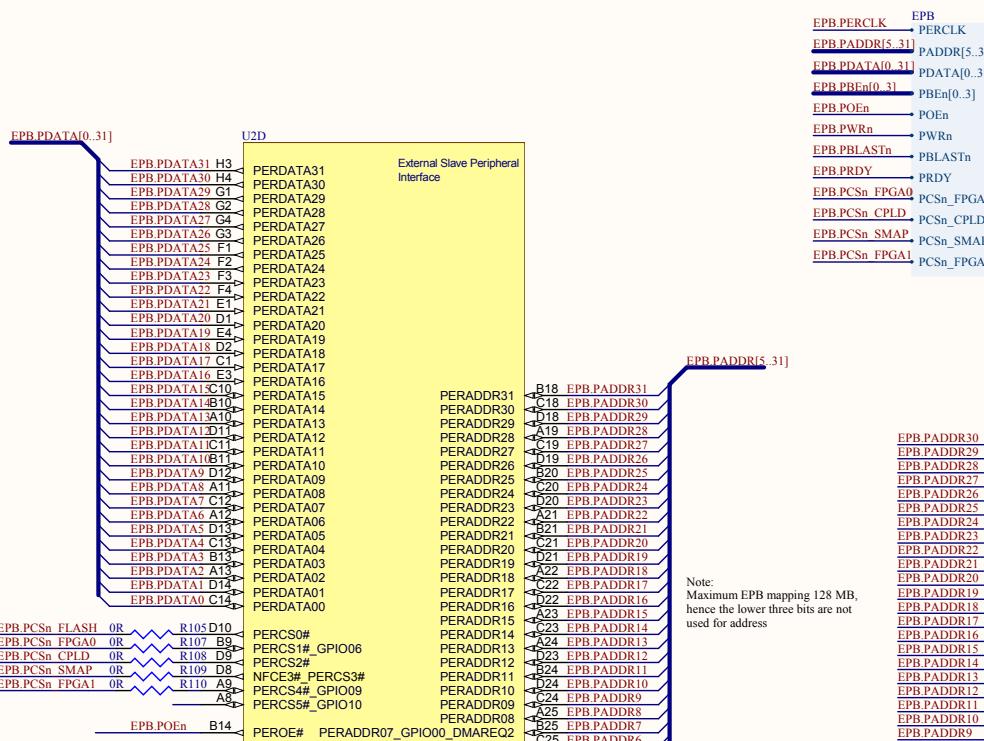
Note:
Analogue grounds EAGND, AGND
and UAGNDn to be routed to GND
pin of decoupling CAP



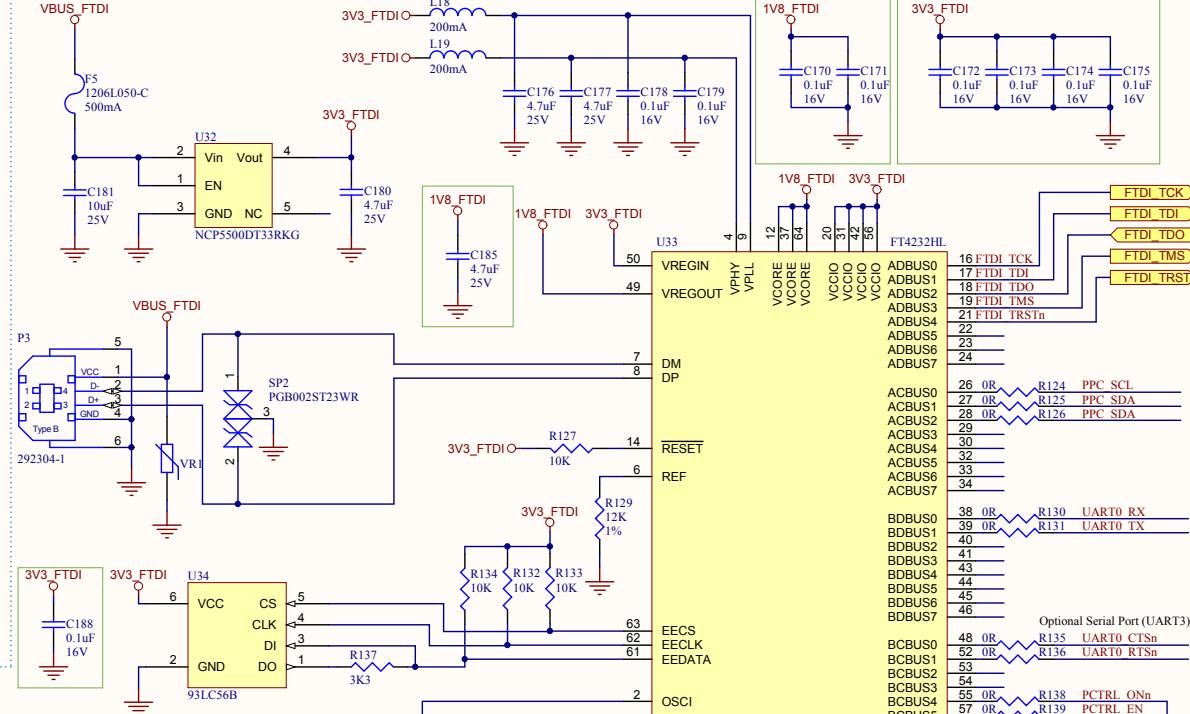
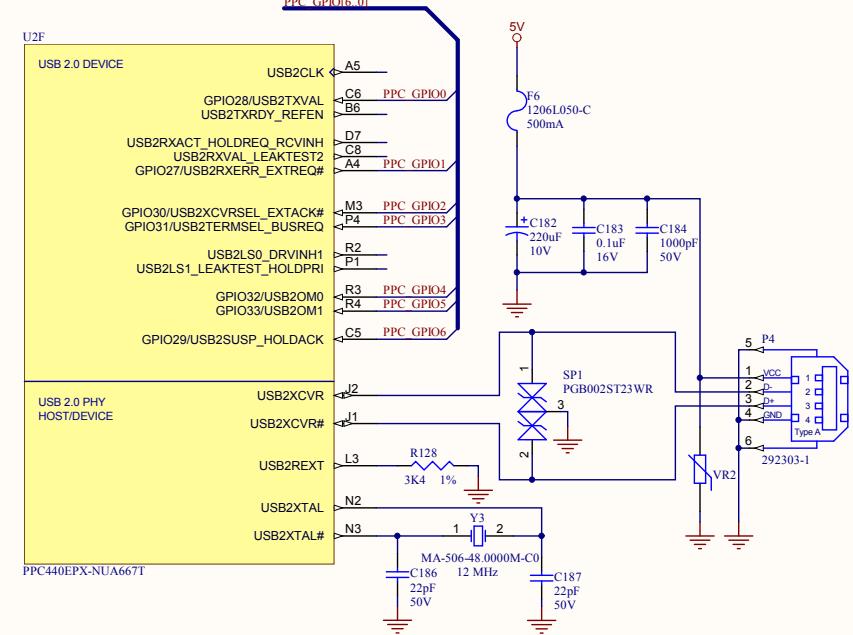
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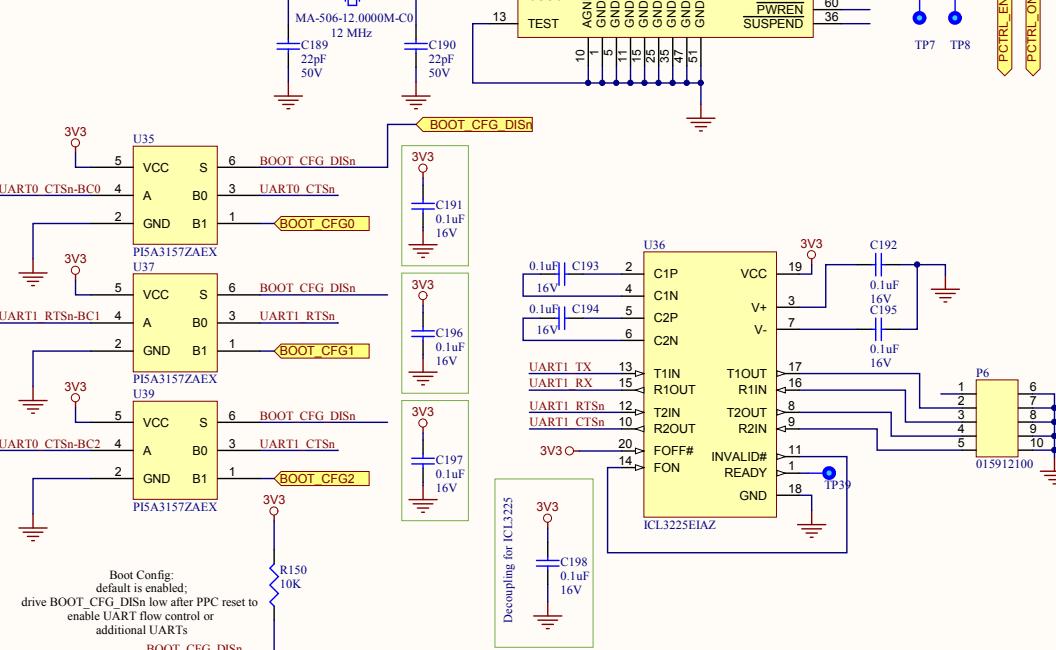
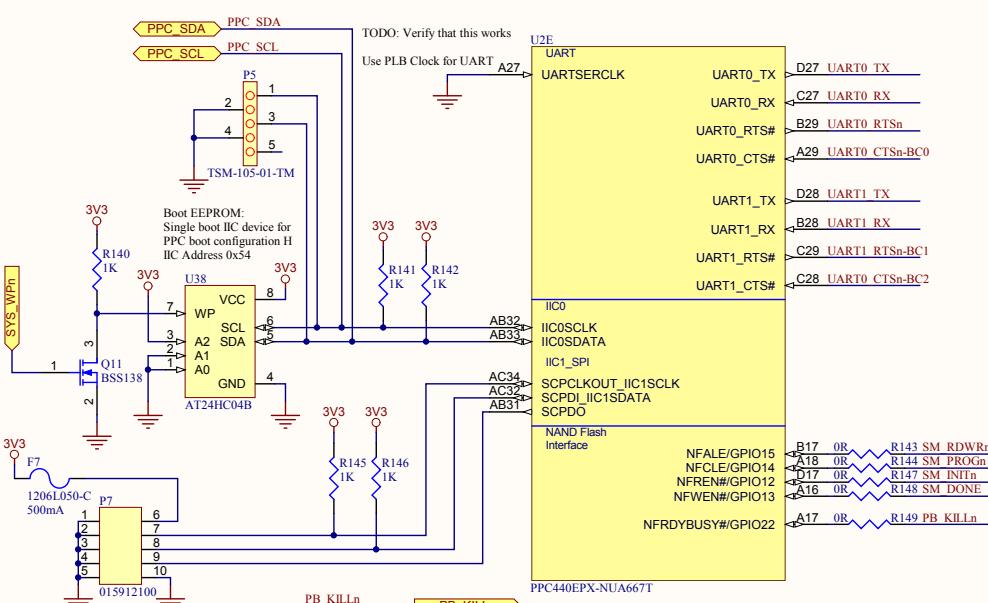


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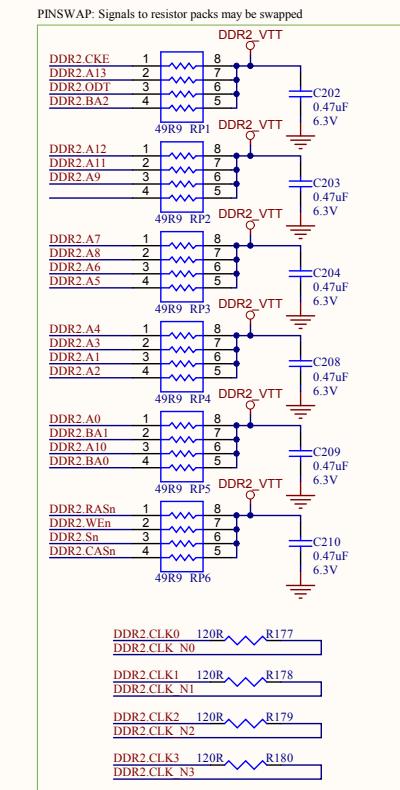
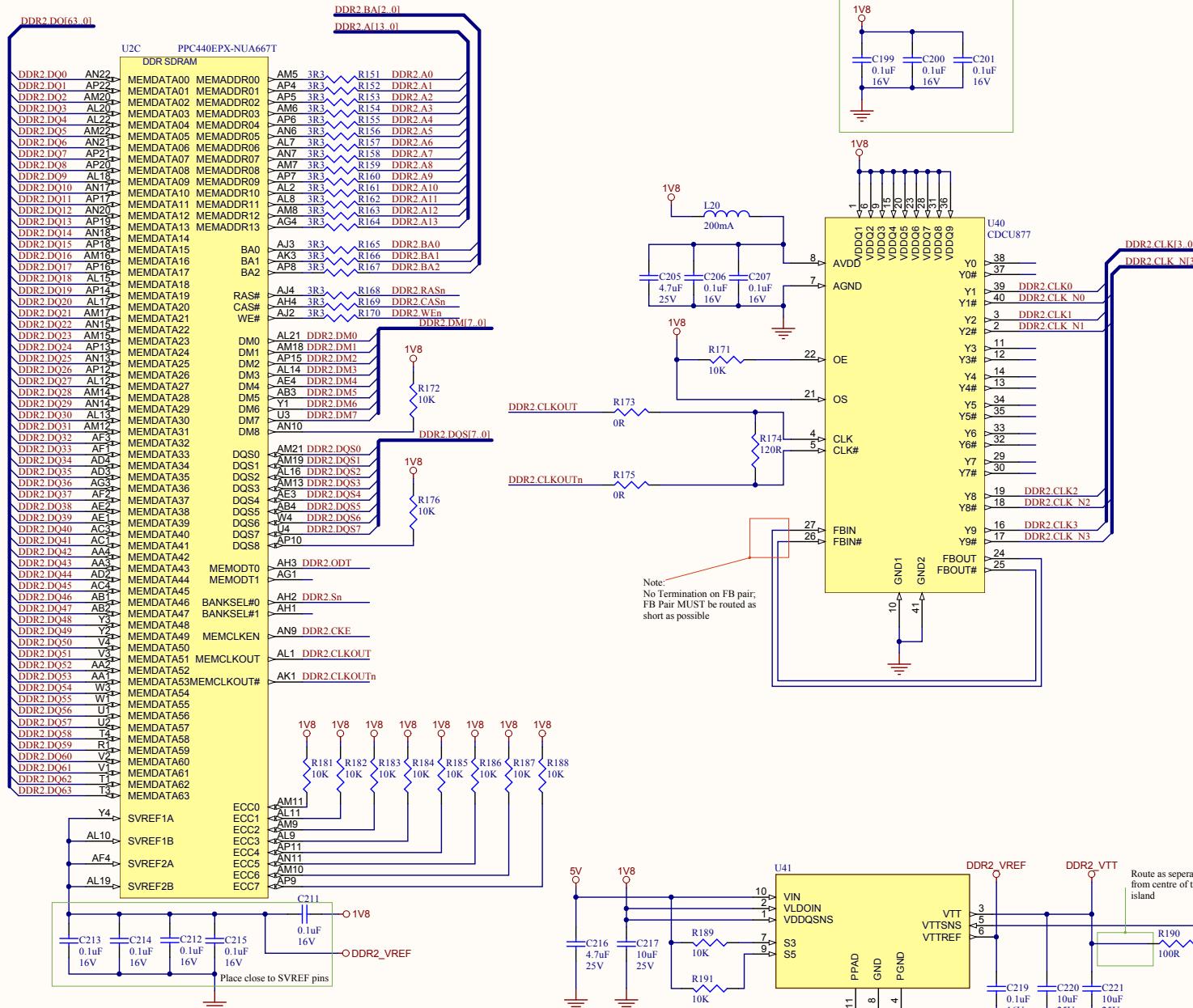
DO: Verify that this works

PLB Clock for UART



drive BOOT_CFG_D1S0 low after PPC reset
enable UART flow control or additional UARts

A 3 2 0



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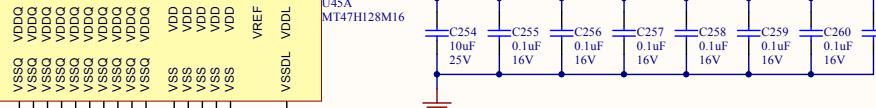
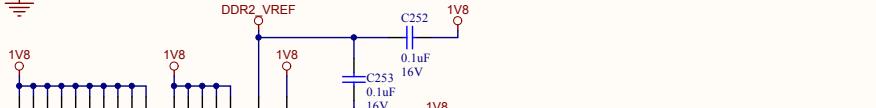
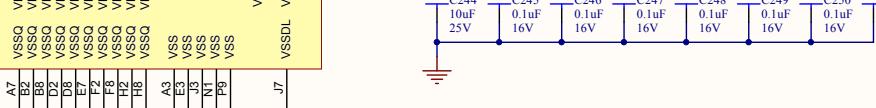
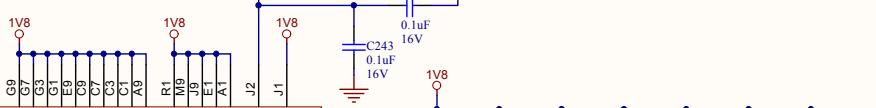
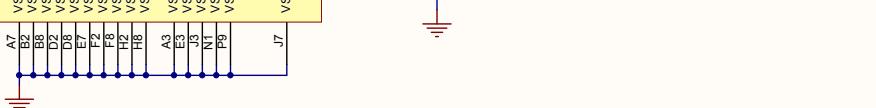
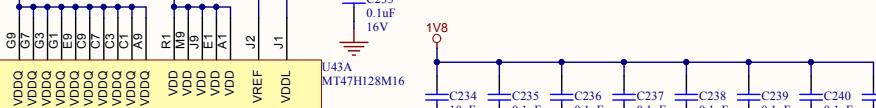
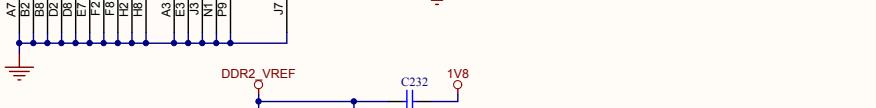
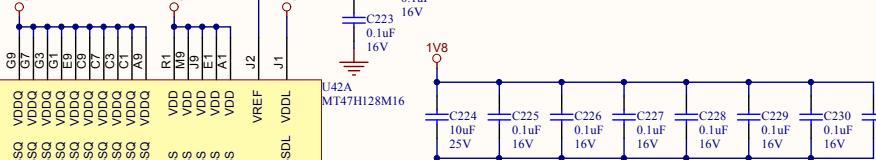
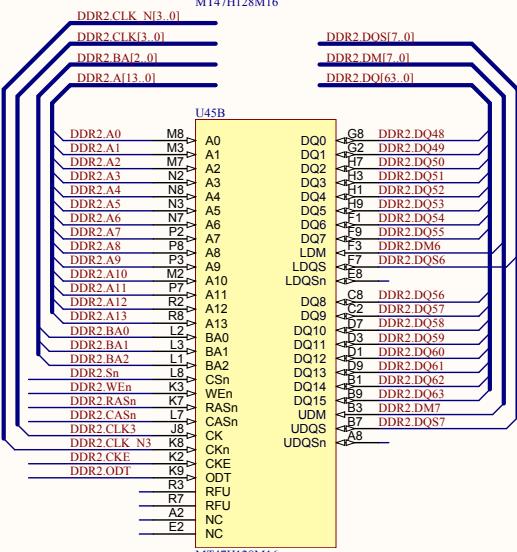
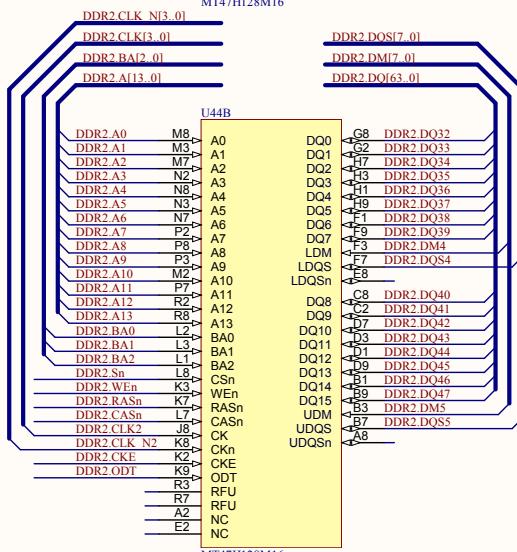
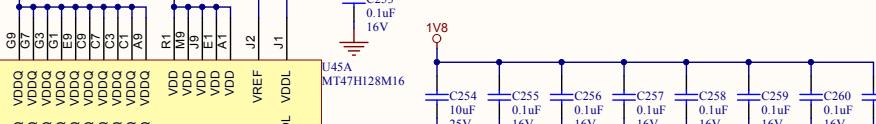
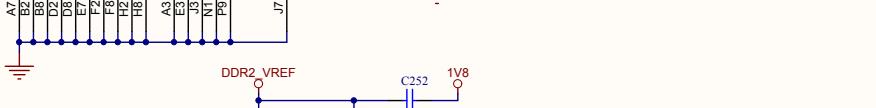
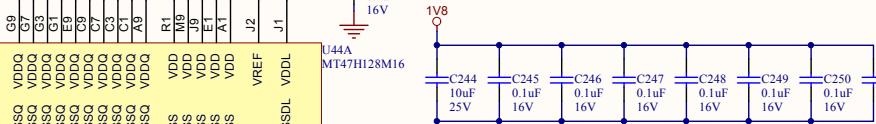
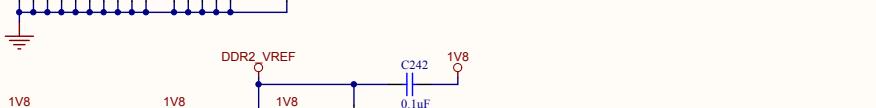
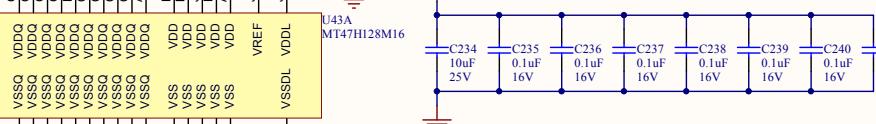
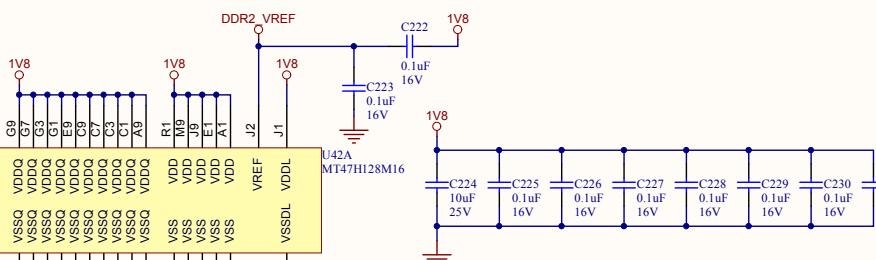
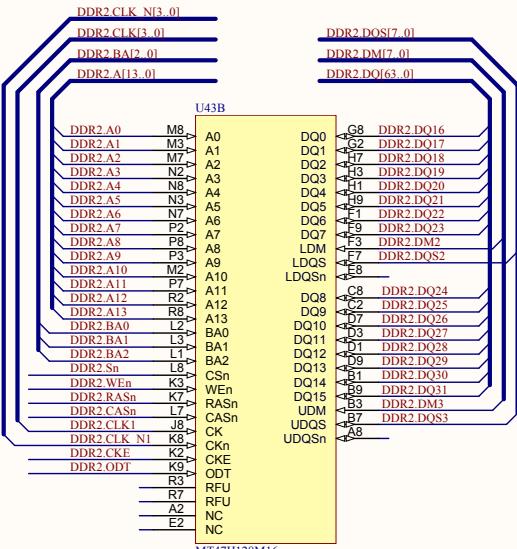
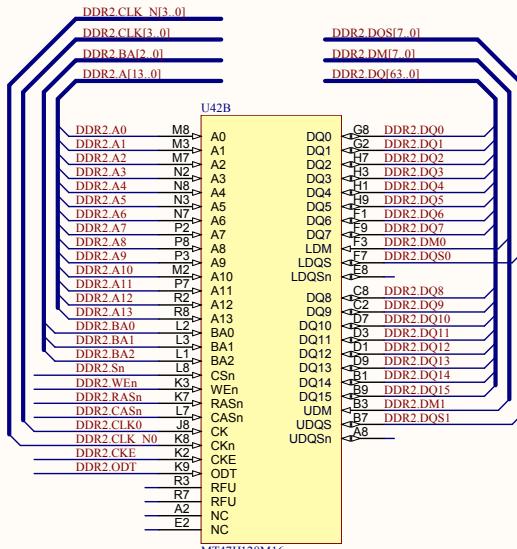
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SHEET
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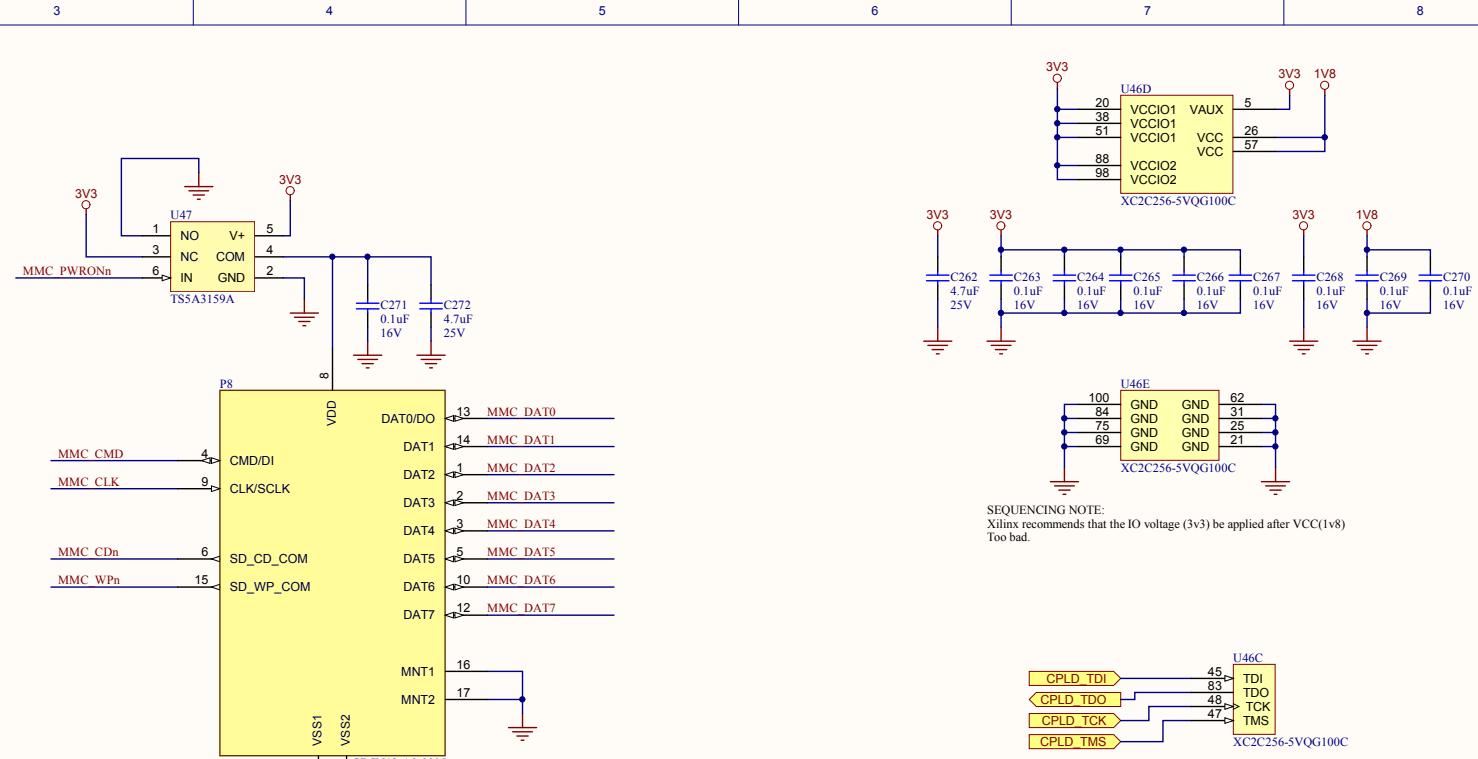
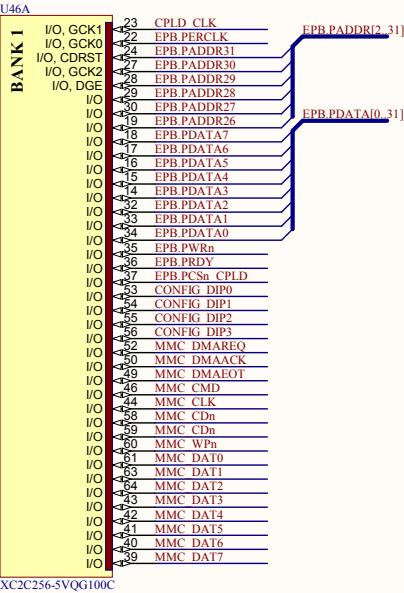


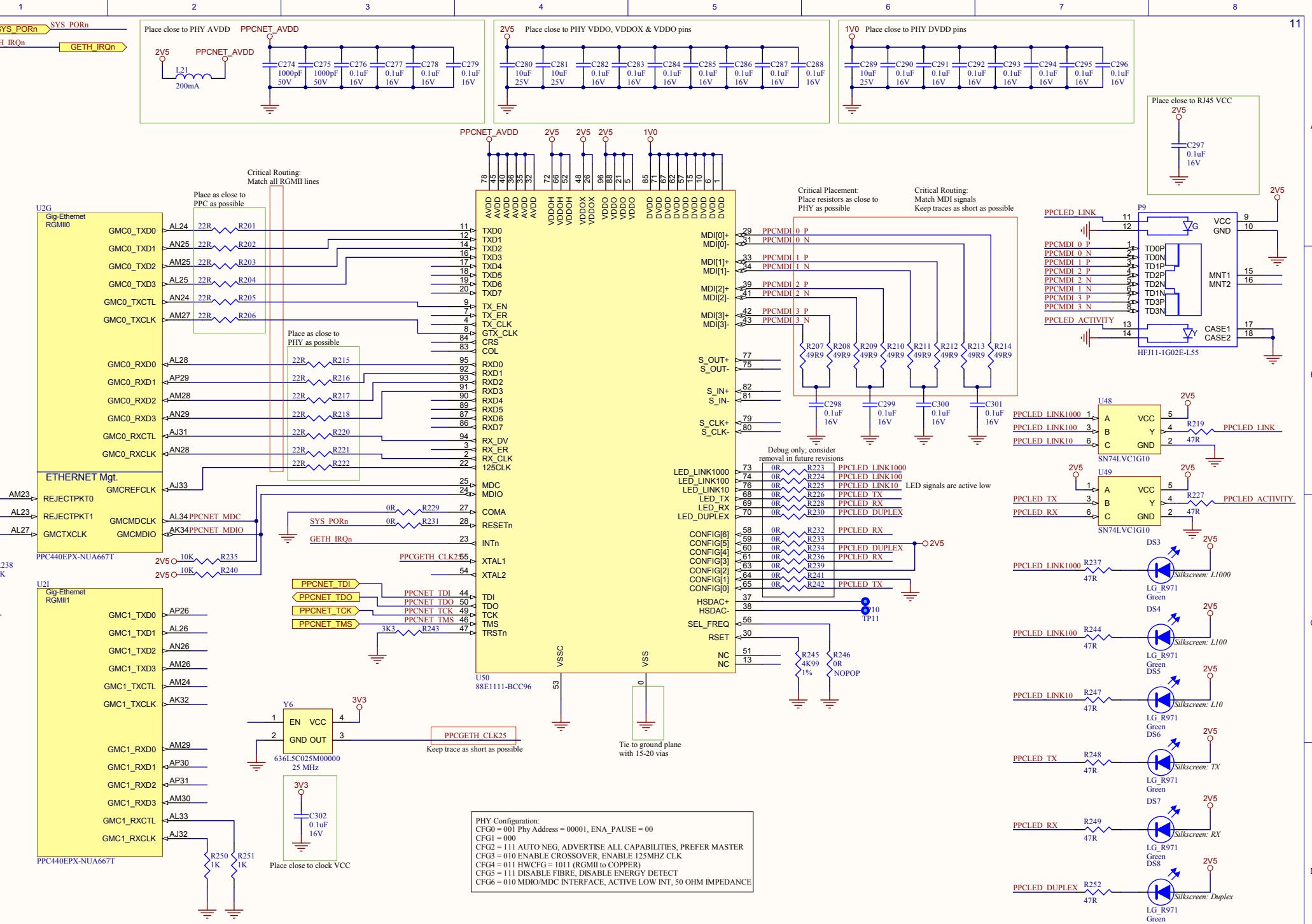
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graph TD
    DDR2[DDR2] --> DQ[DQ[63..0]]
    DDR2 --> DM[DM[7..0]]
    DDR2 --> DQS[DQS[7..0]]
    DDR2 --> A[A[13..0]]
    DQ --> DQn[DQ2_Sn]
    DM --> DMn[DM2_Sn]
    DQS --> DQSn[DQS2_RASn]
    A --> An[A2_CKE]

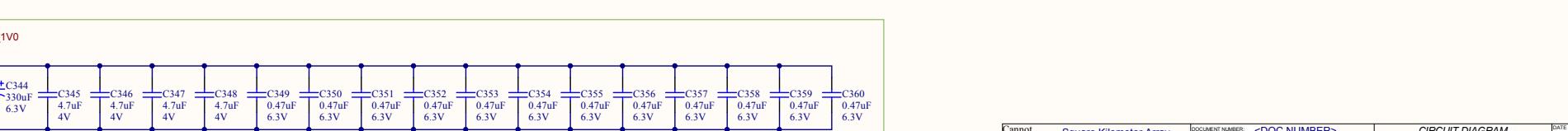
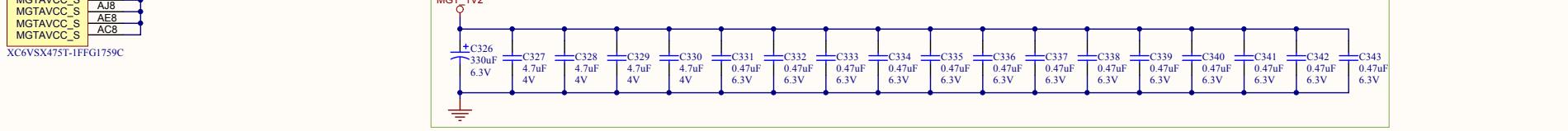
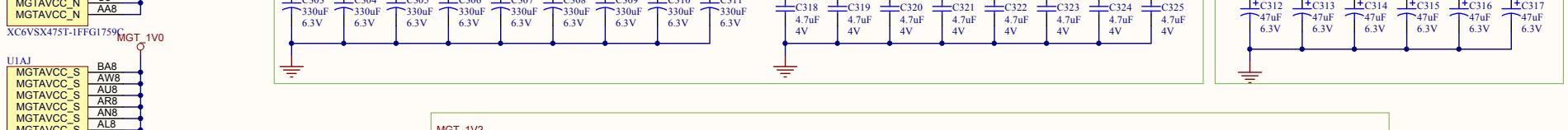
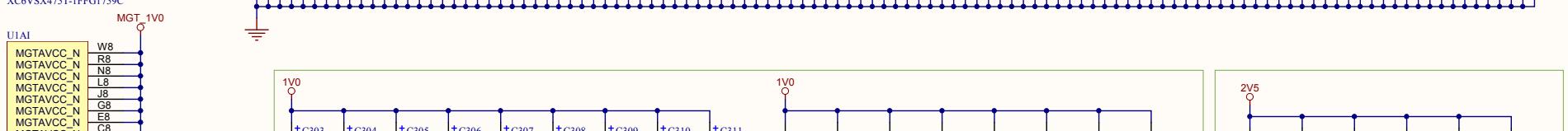
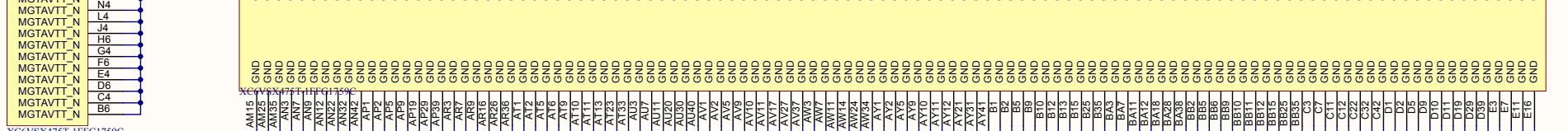
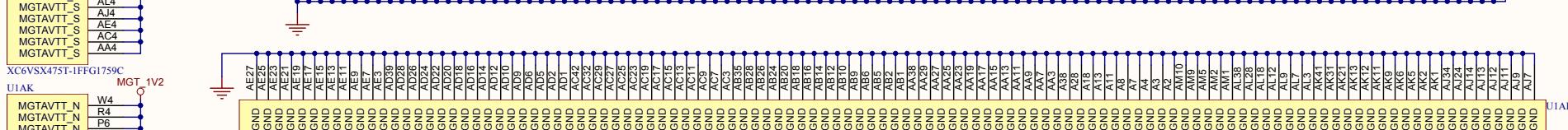
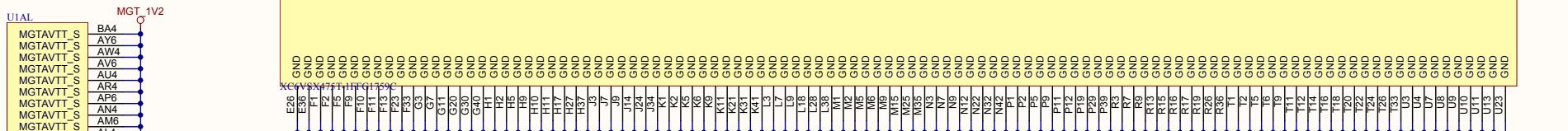
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PINSWAP:
 CPLD CLK and EPB.PERCLK MUST go on GCK pins
 SYS_PORn MUST go on GSR pin
 EPB.POEn MUST go on GTS pin
 Otherwise, swap away





1

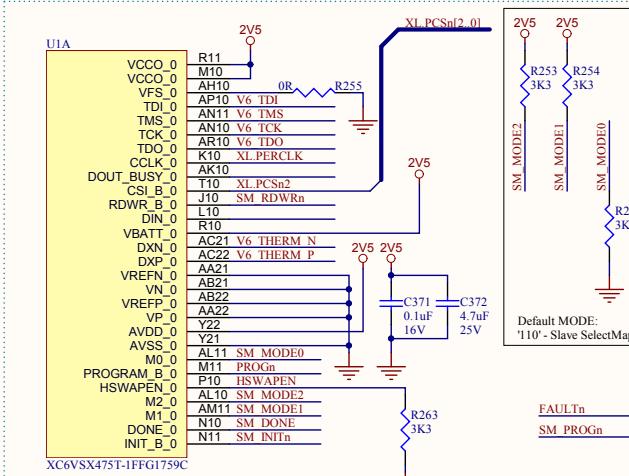
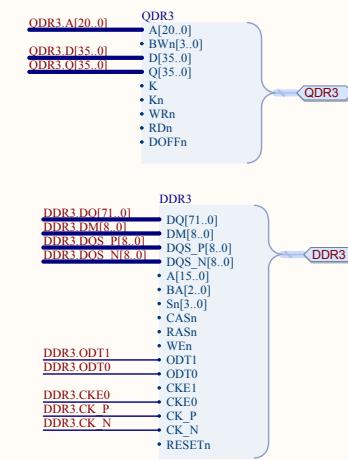
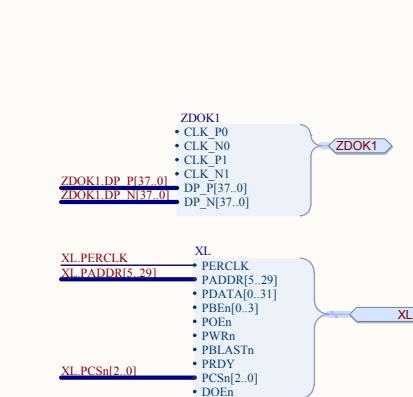
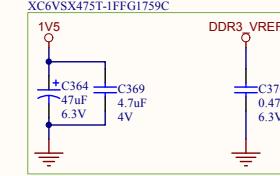
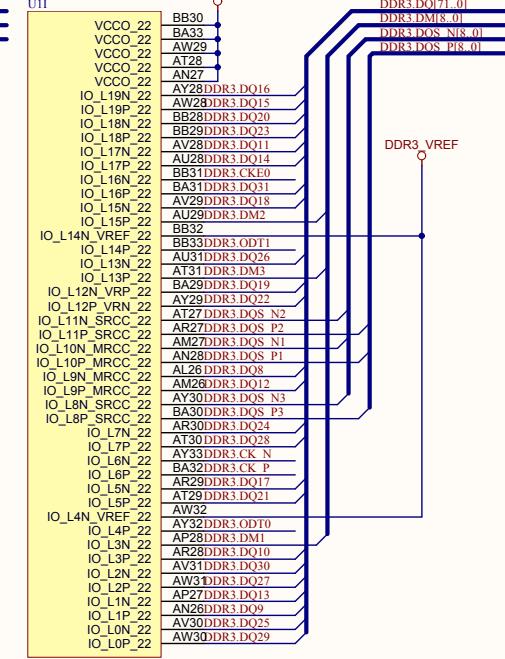
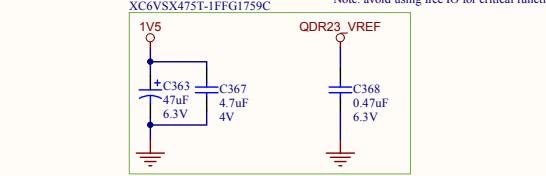
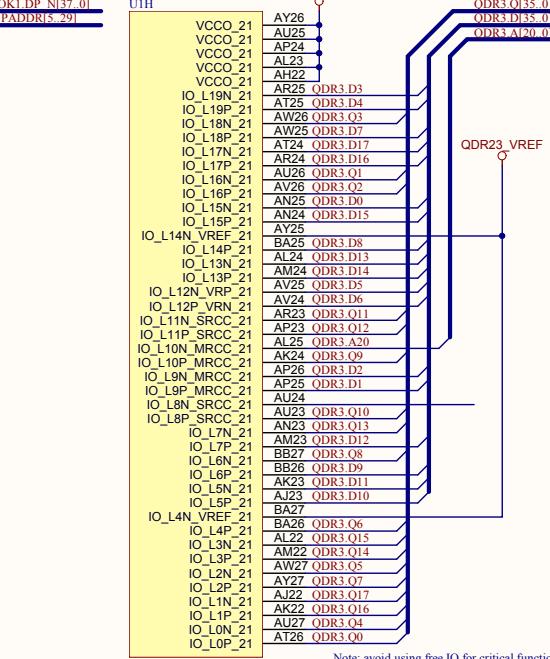
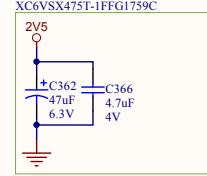
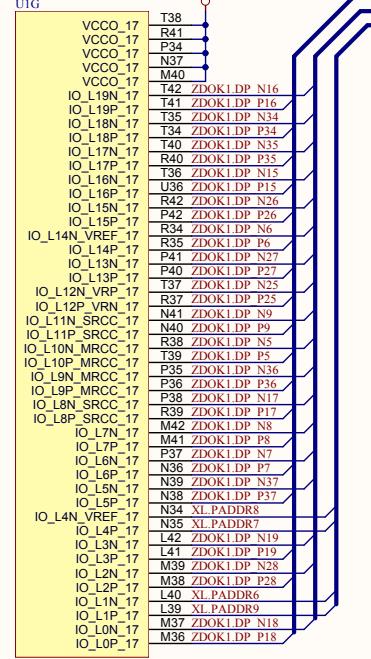
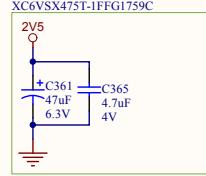
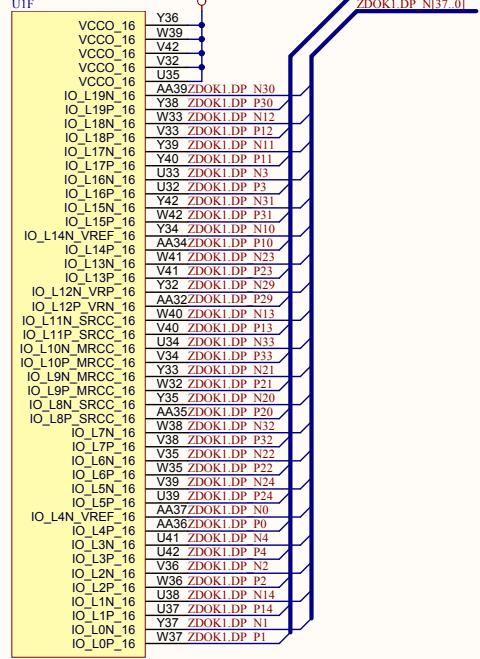


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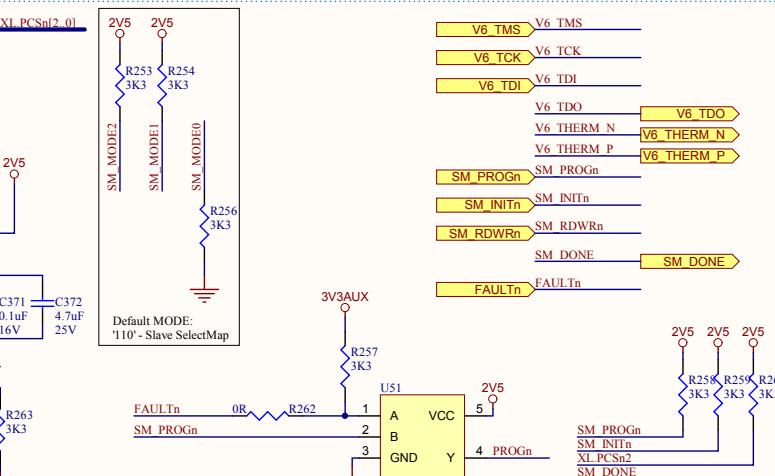
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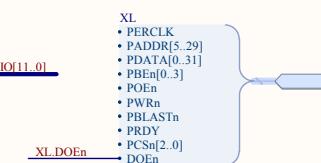
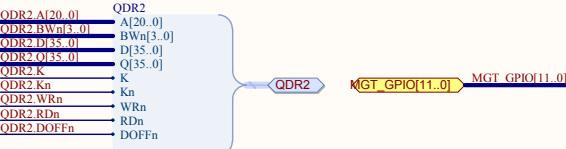
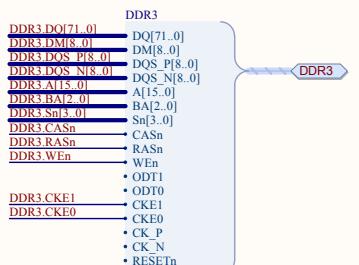
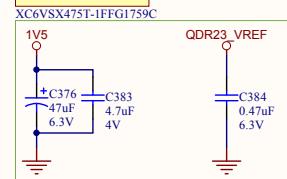
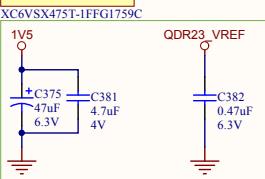
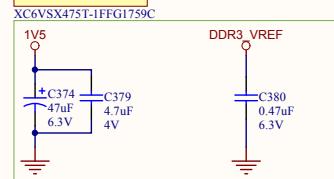
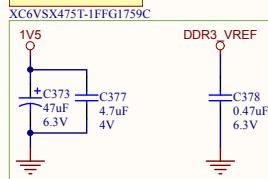
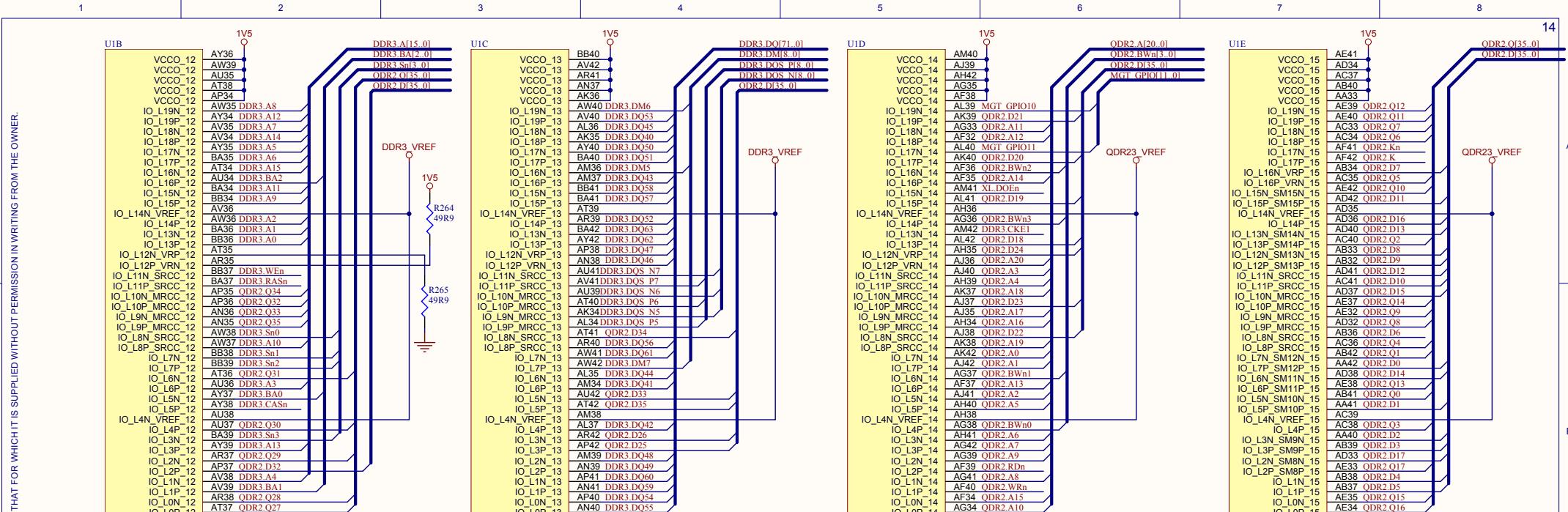
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Note:
External sensors will be used for monitoring,
hence the lack of more rigorous filtering



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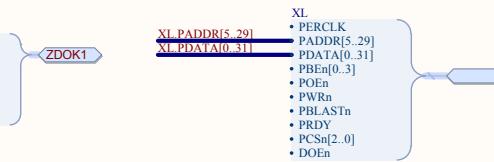
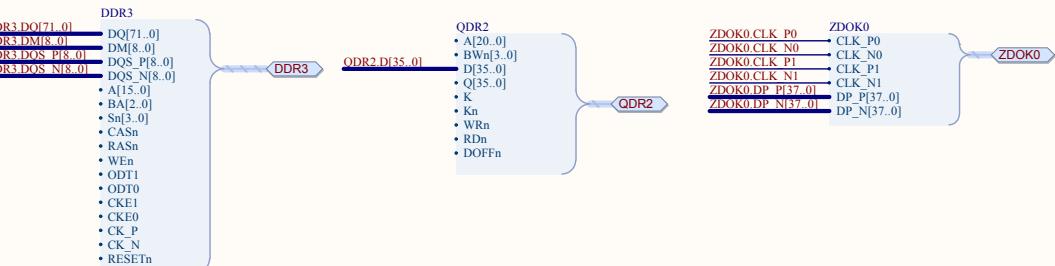
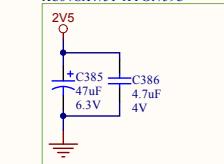
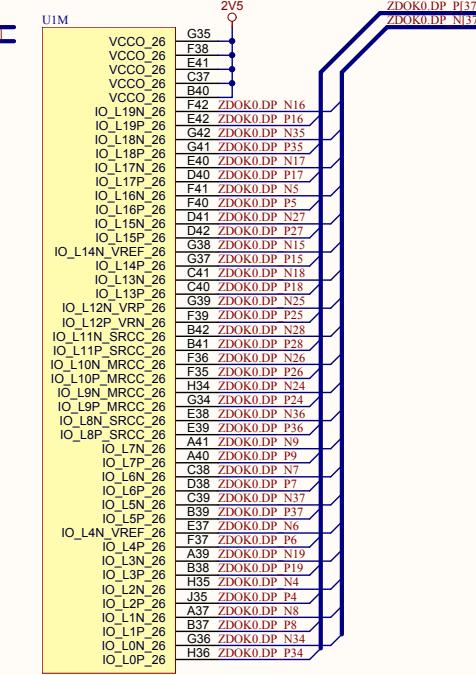
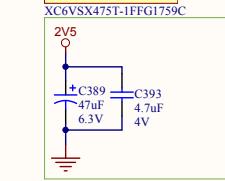
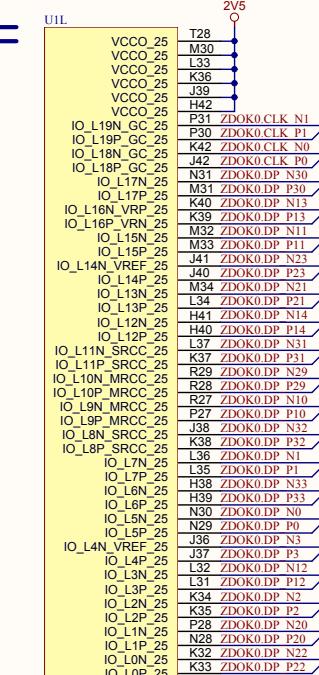
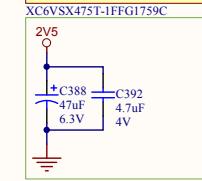
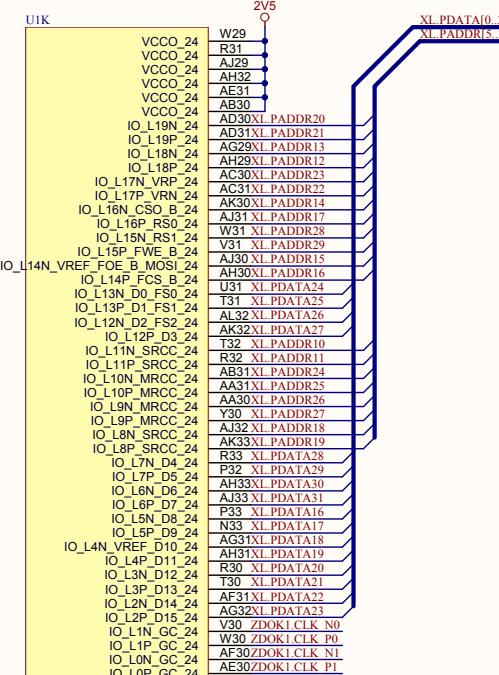
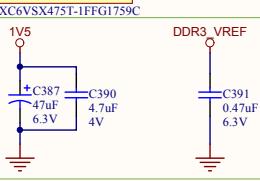
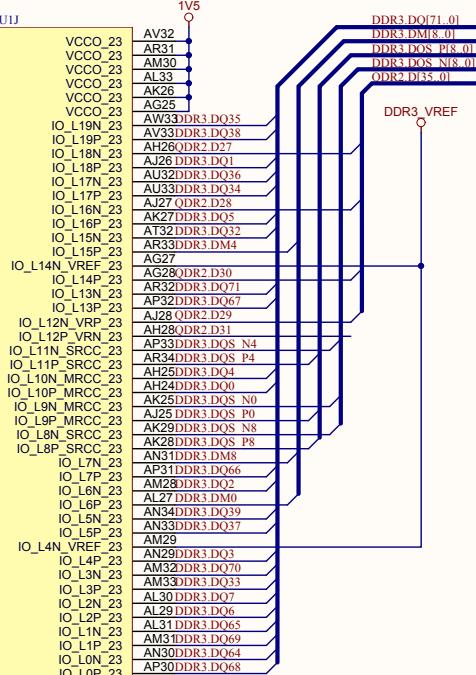
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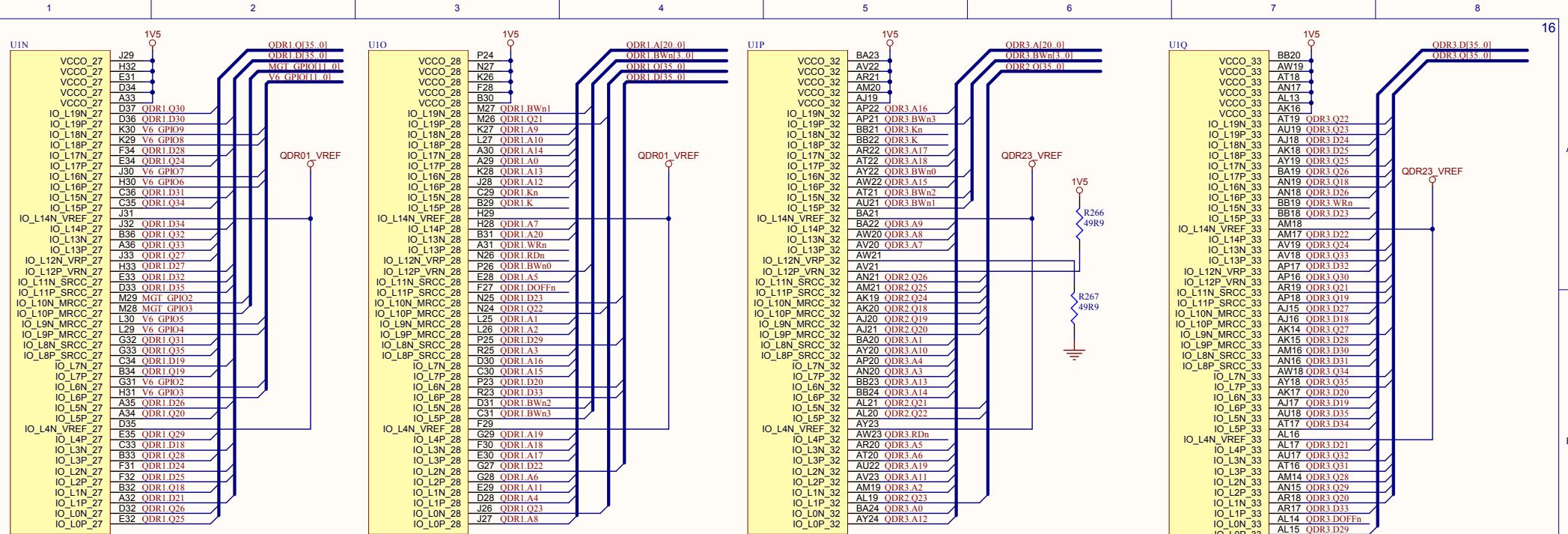
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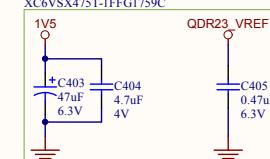
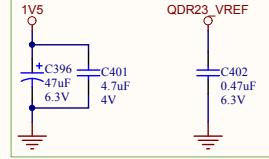
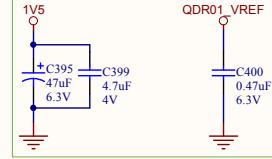
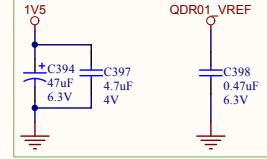
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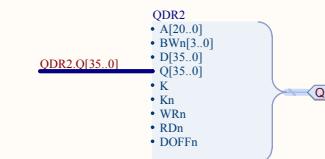
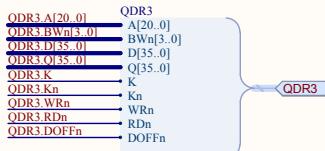
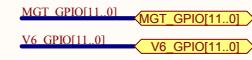
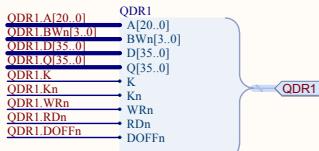




XC6VSX475T-1FFG1759C



Device Compatibility:
Bank 28 unavailable on
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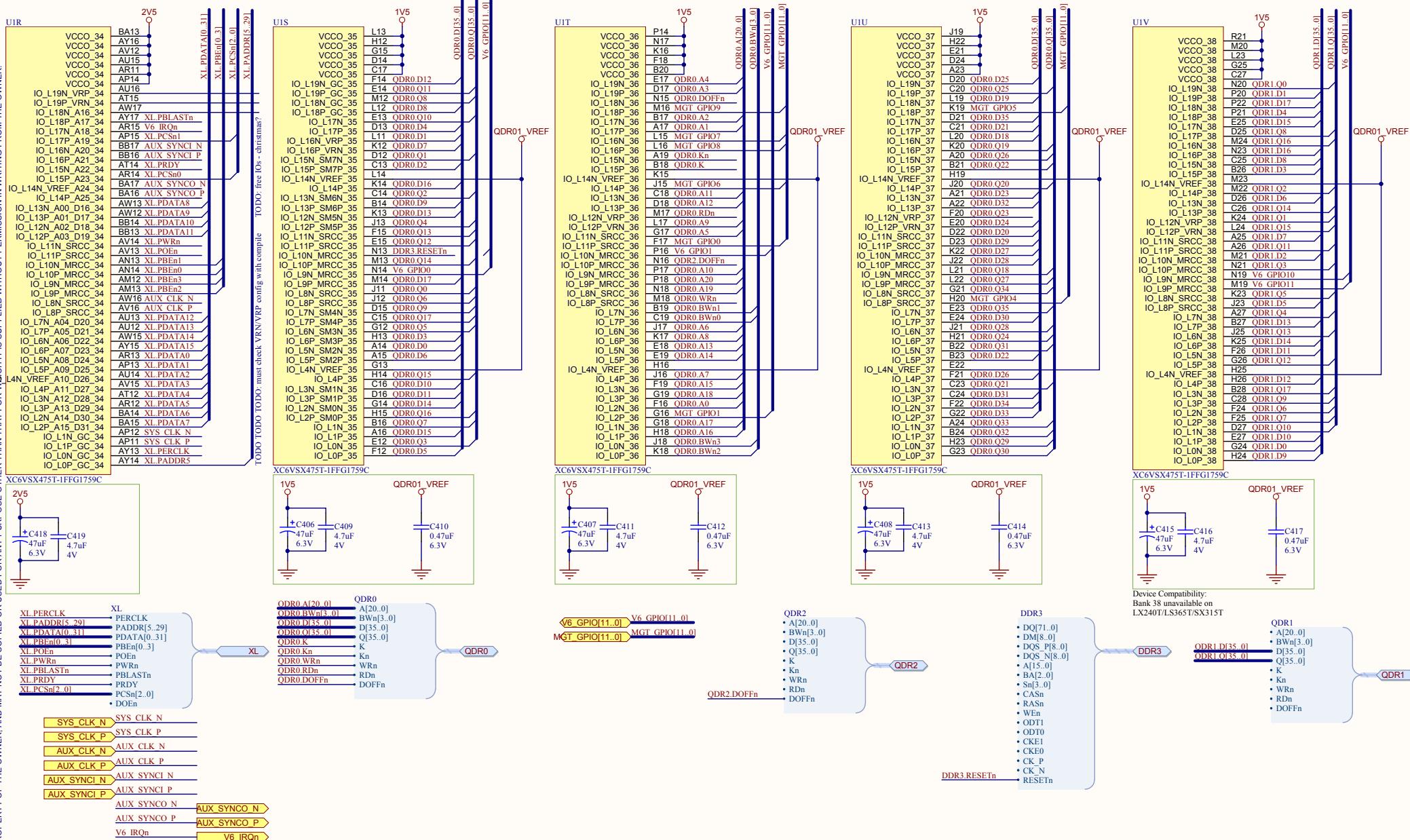
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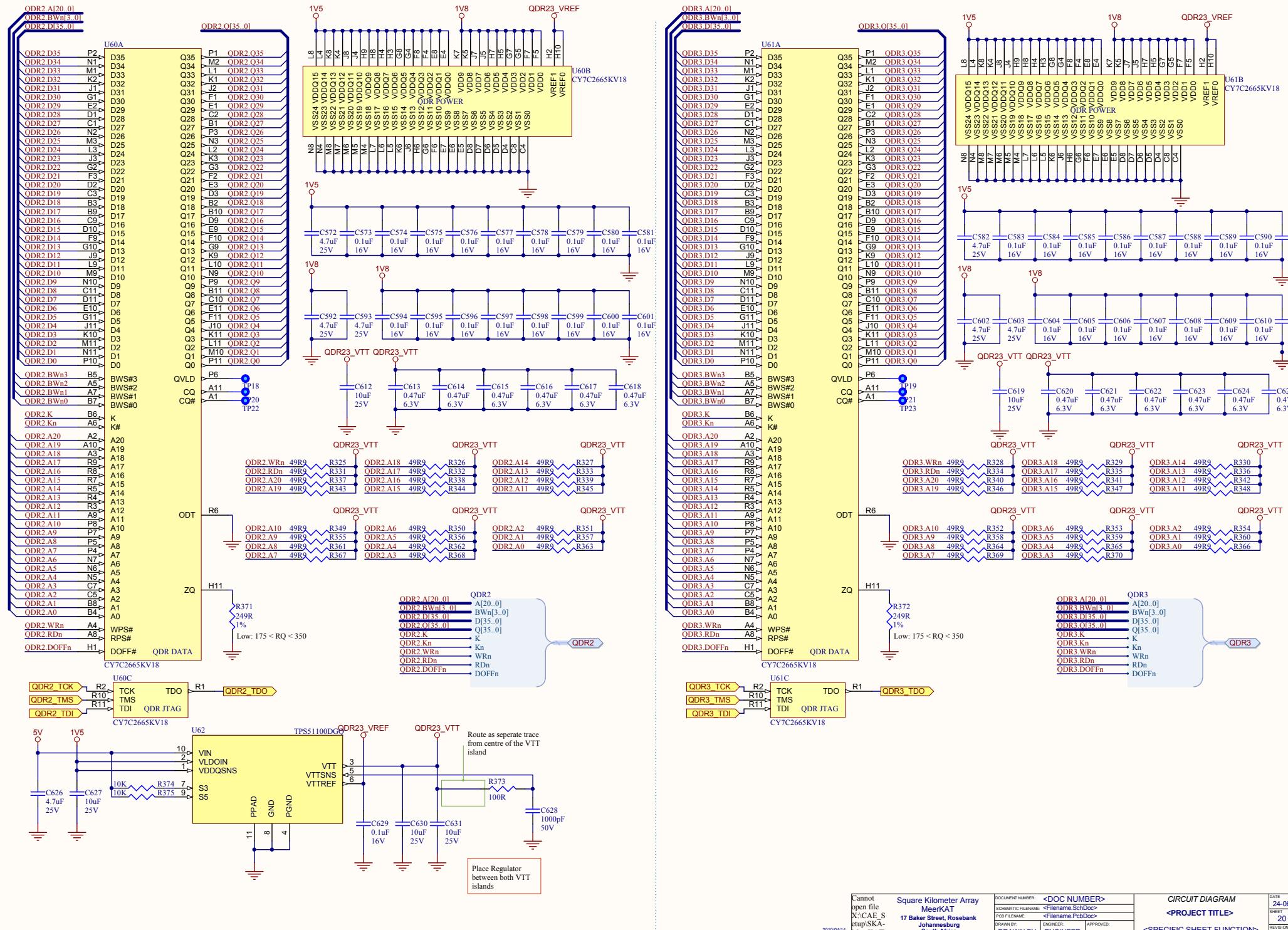
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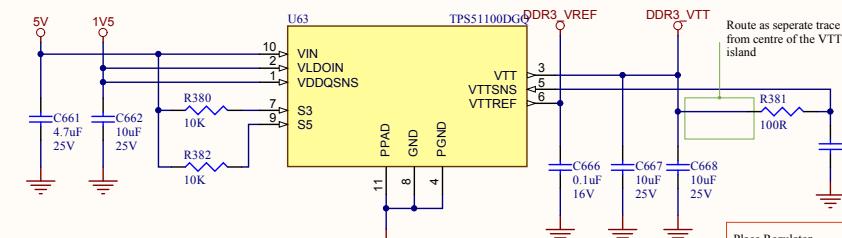
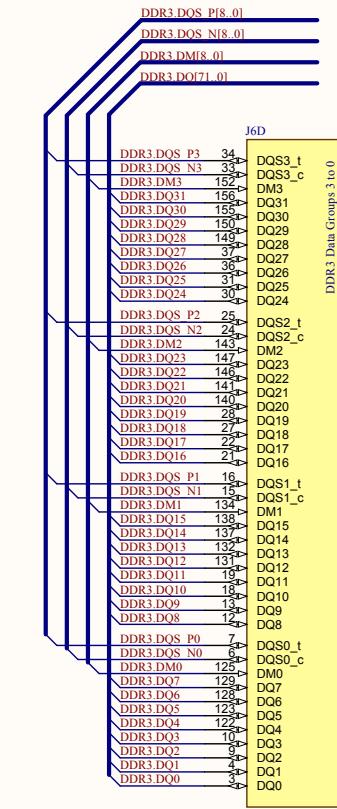
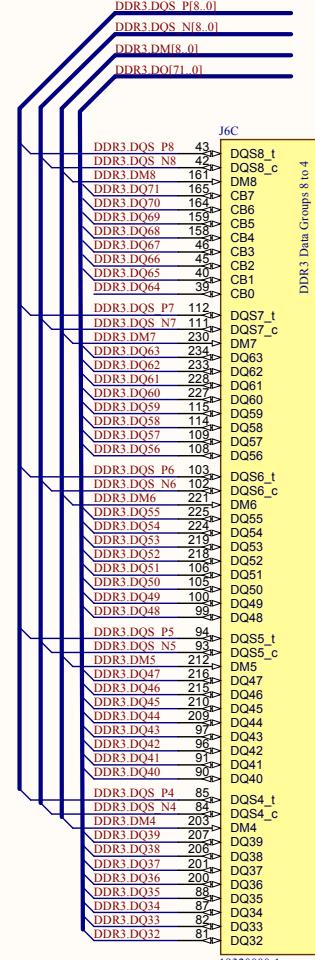
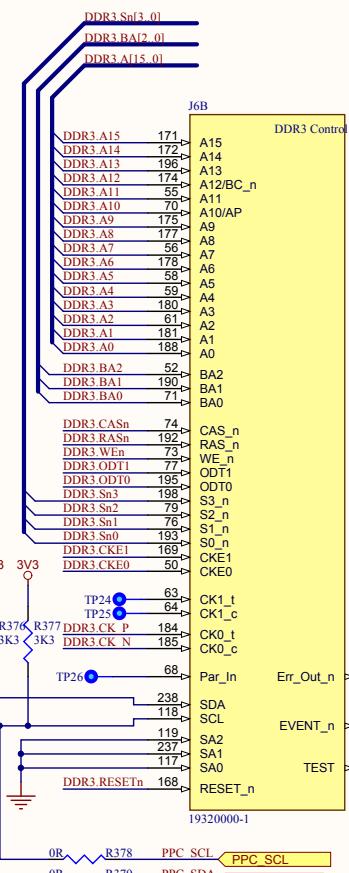
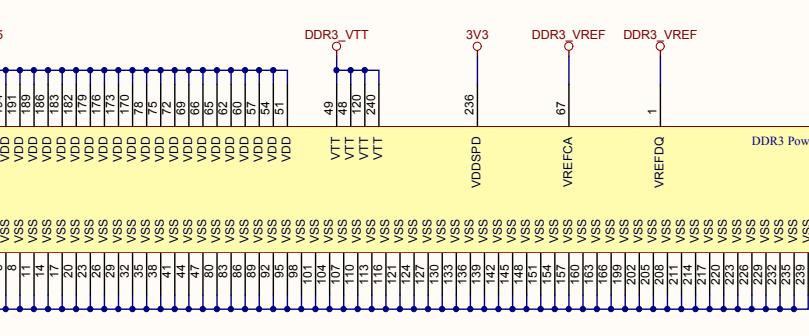
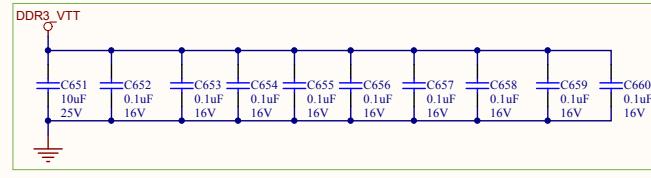
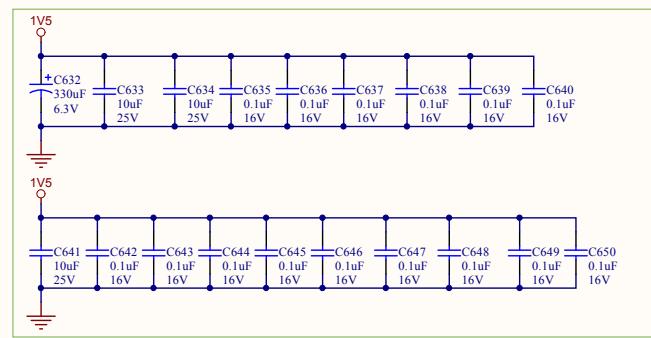
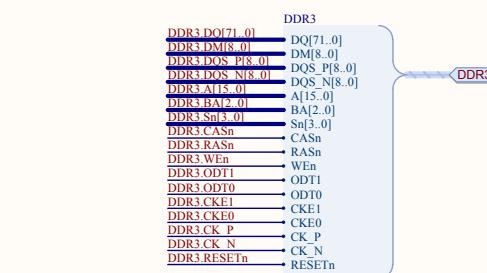
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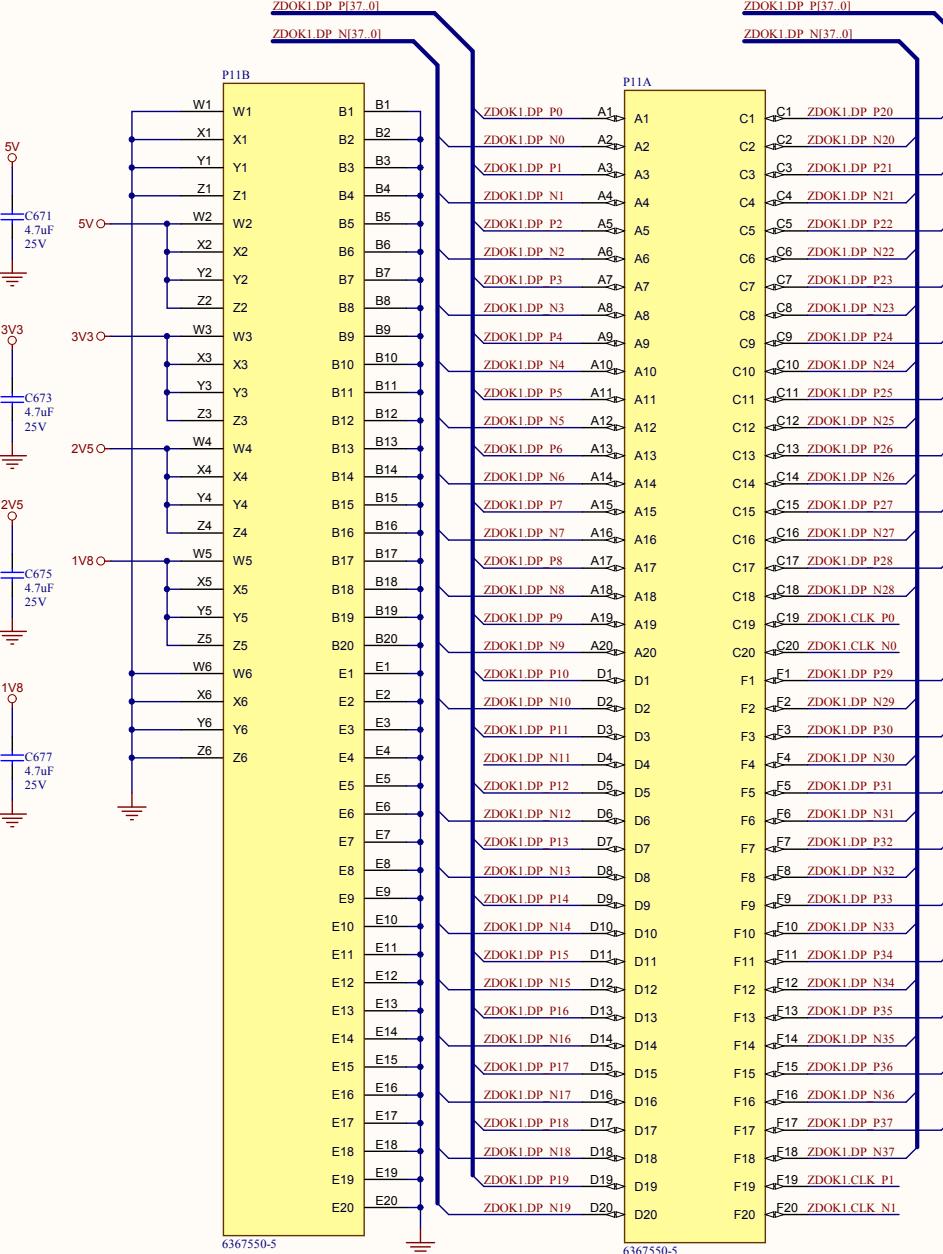
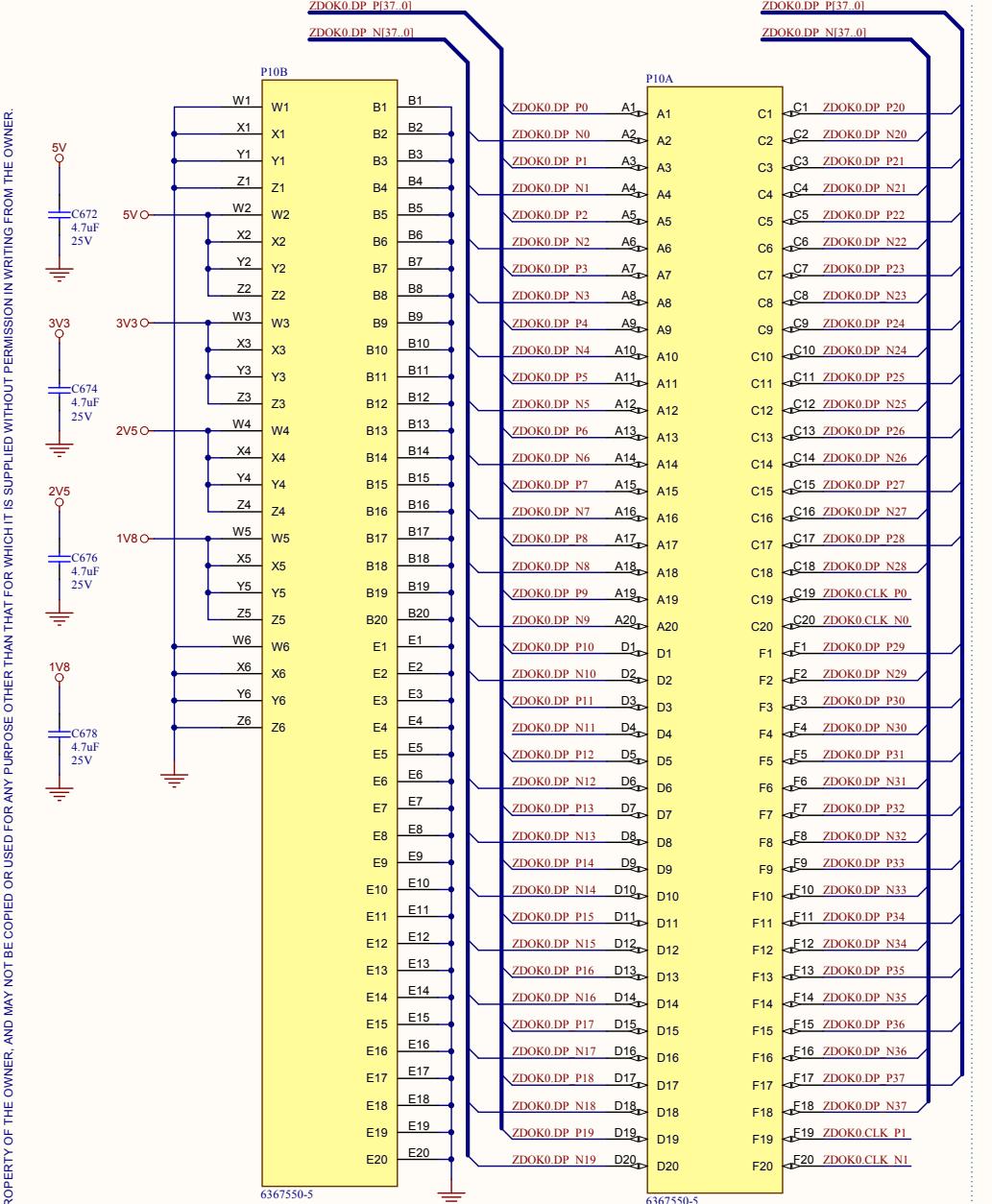
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D	THIS DOCUMENT IS THE ZDOK0 CLK P0	ZDOK0 CLK_P0
	ZDOK0 CLK N0	CLK_N0
	ZDOK0 CLK P1	CLK_P1
	ZDOK0 CLK N1	CLK_N1
	ZDOK0 DP_P[37..0]	DP_P[37..0]
	ZDOK0 DP_N[37..0]	DP_N[37..0]

The diagram illustrates the timing relationships between various digital signals. CKI_CLK_P0, CKI_CLK_N0, CKI_CLK_P1, and CKI_CLK_N1 are clock signals. CKI_DP_P[37..0] and CKI_DP_N[37..0] are data signals. ZDOK1_P and ZDOK1_N are outputs. Arrows indicate the flow from CKI_CLK_P0 to ZDOK1_P, CKI_CLK_N0 to ZDOK1_N, CKI_CLK_P1 to ZDOK1_P, CKI_CLK_N1 to ZDOK1_N, CKI_DP_P[37..0] to ZDOK1_P, and CKI_DP_N[37..0] to ZDOK1_N.

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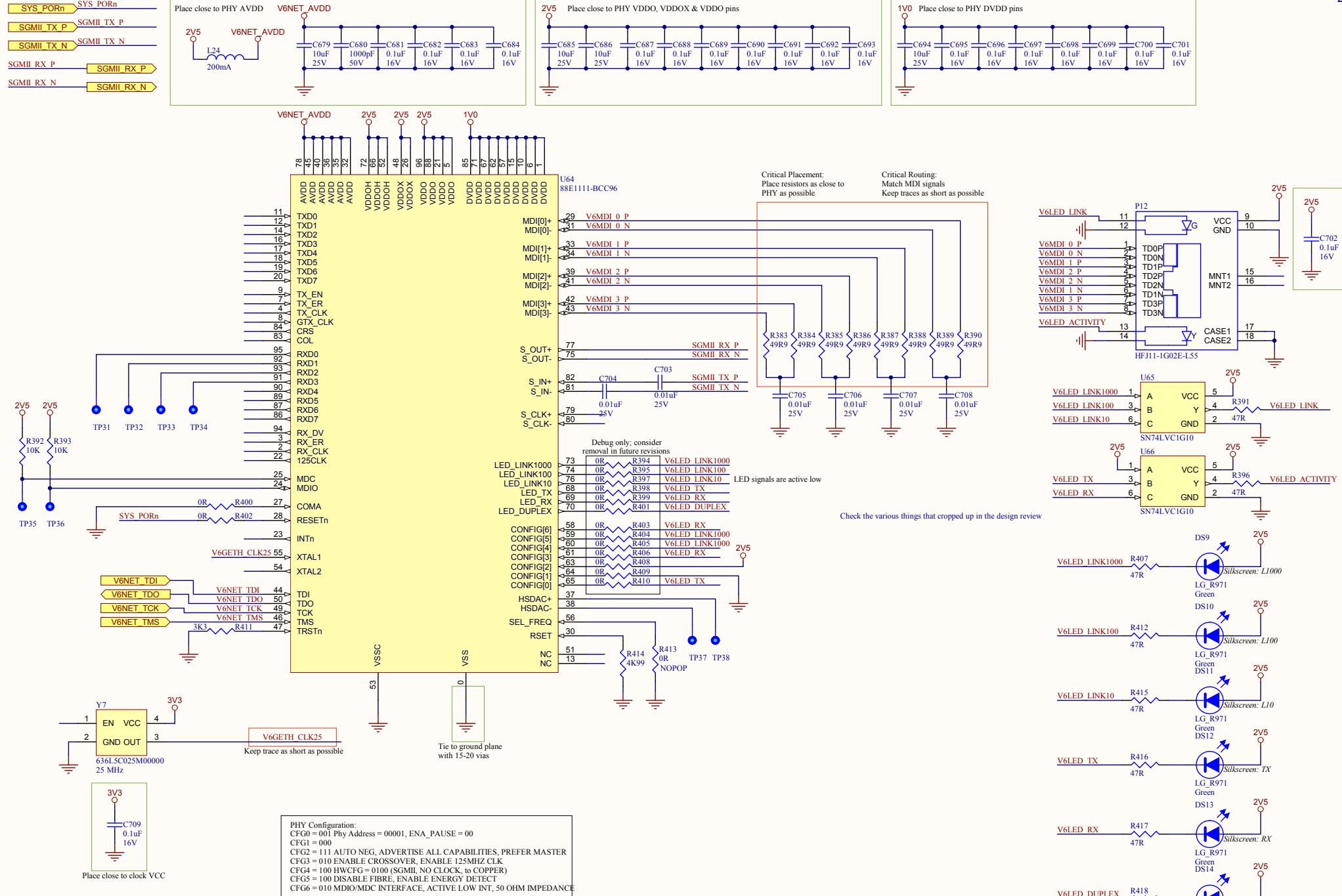
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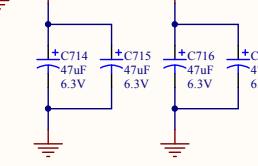
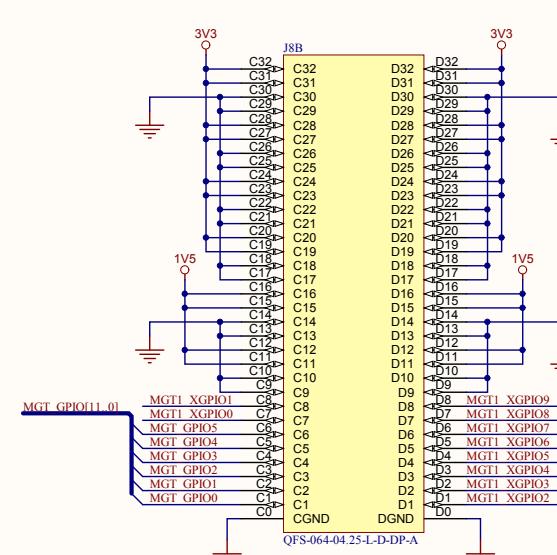
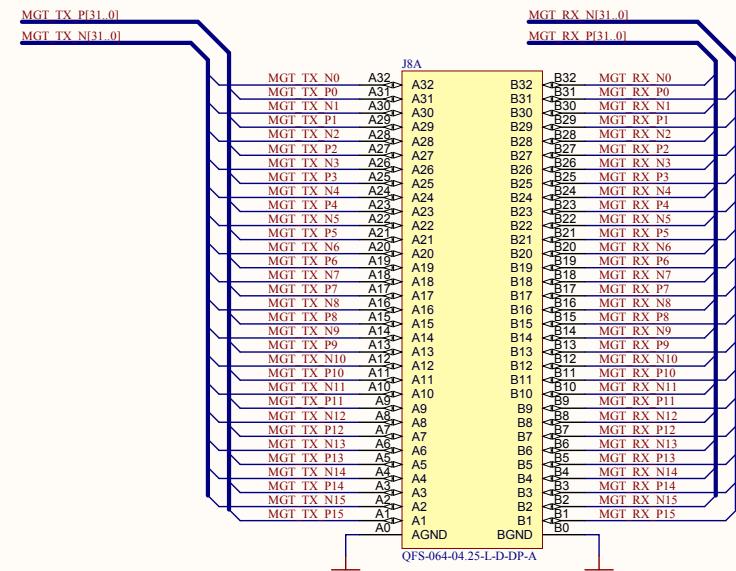
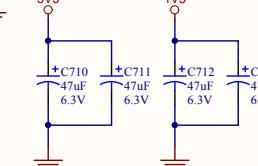
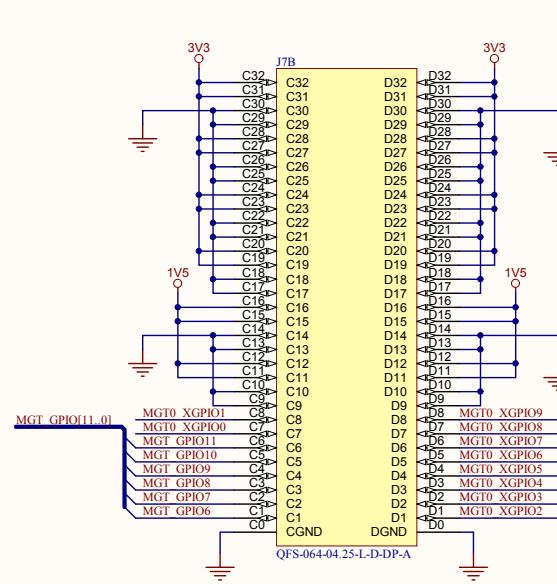
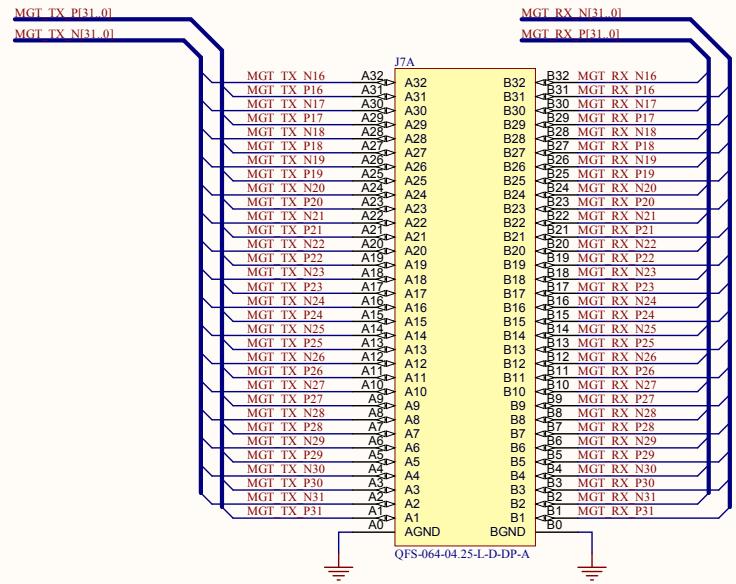
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MGT_RX_P[31..0] MGT_RX_N[31..0]
 MGT_TX_P[31..0] MGT_TX_N[31..0]
 MGT_GPIO[11..0]



TODO: add small form factor header for the extra gpio

MGT_RX_P[31..0] MGT_RX_P[31..0] MGT_RX_P[31..0]
 MGT_RX_N[31..0] MGT_RX_N[31..0] MGT_RX_N[31..0]
 MGT_GPIO[11..0] MGT_GPIO[11..0]

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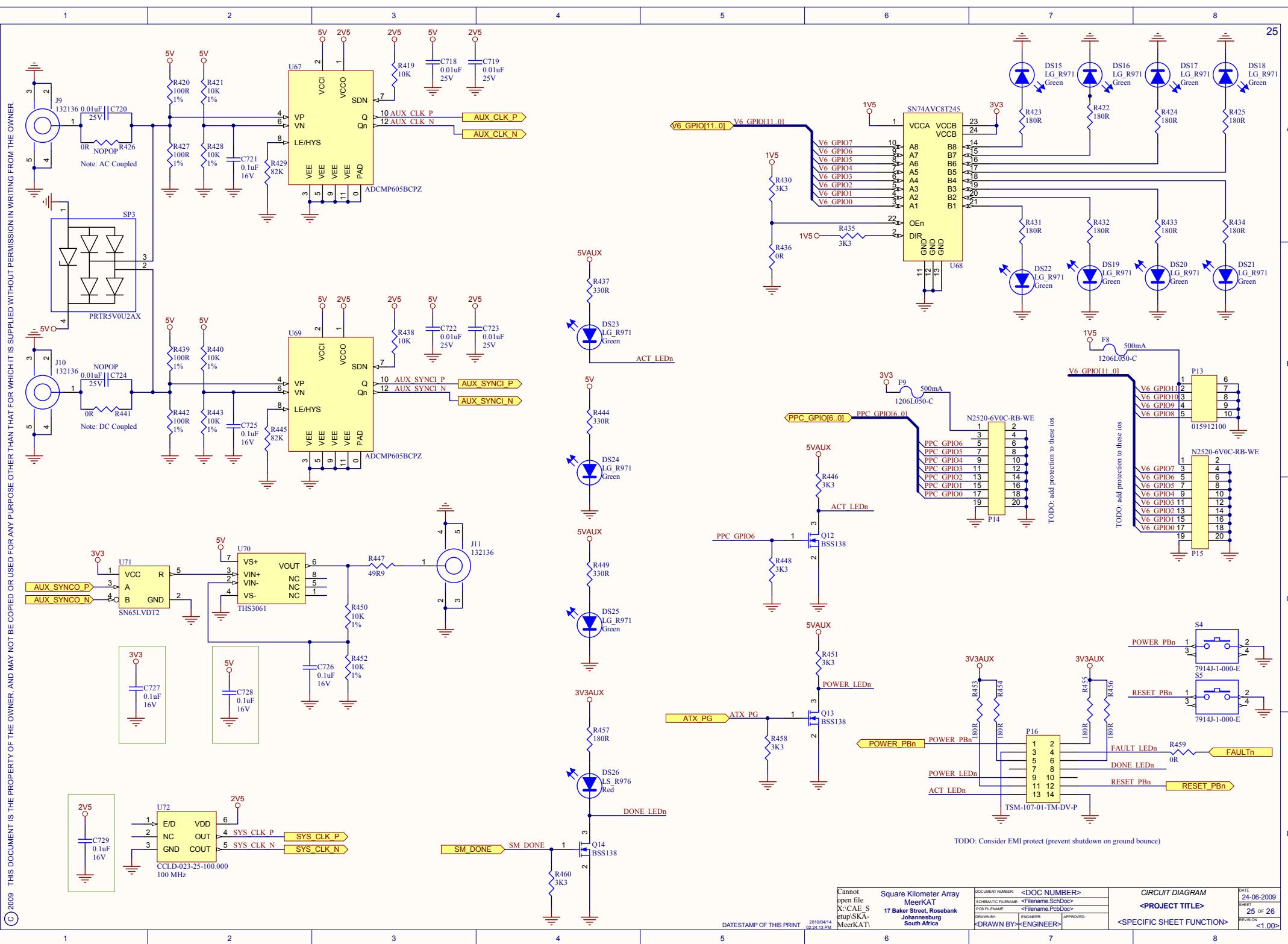
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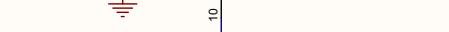
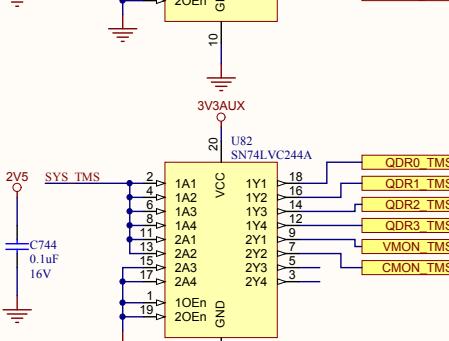
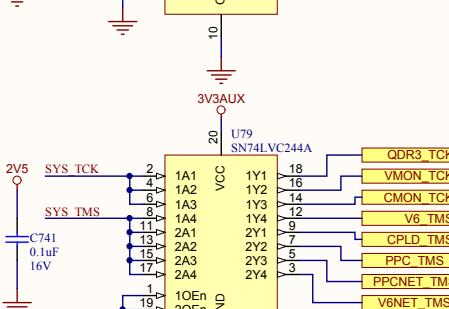
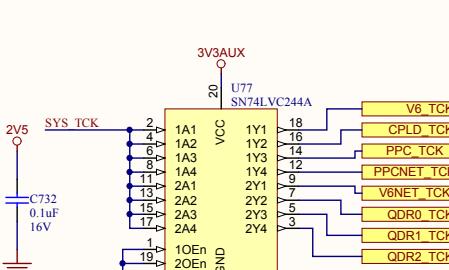
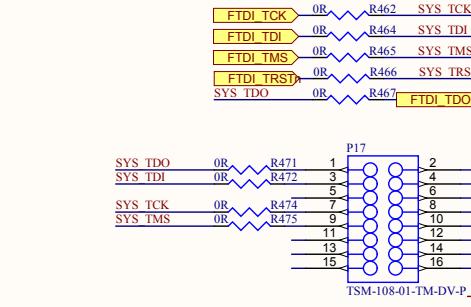
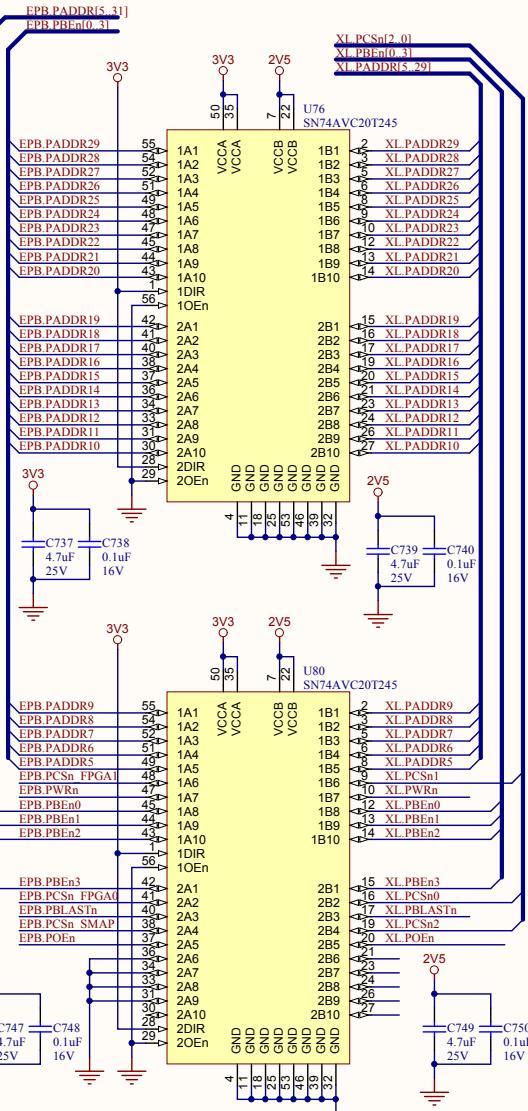
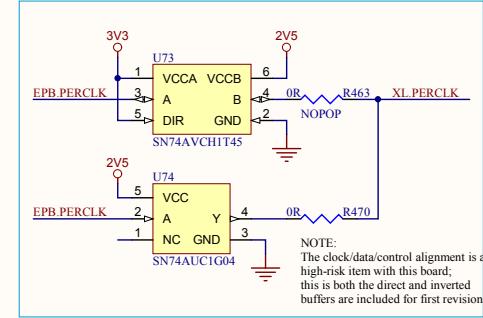
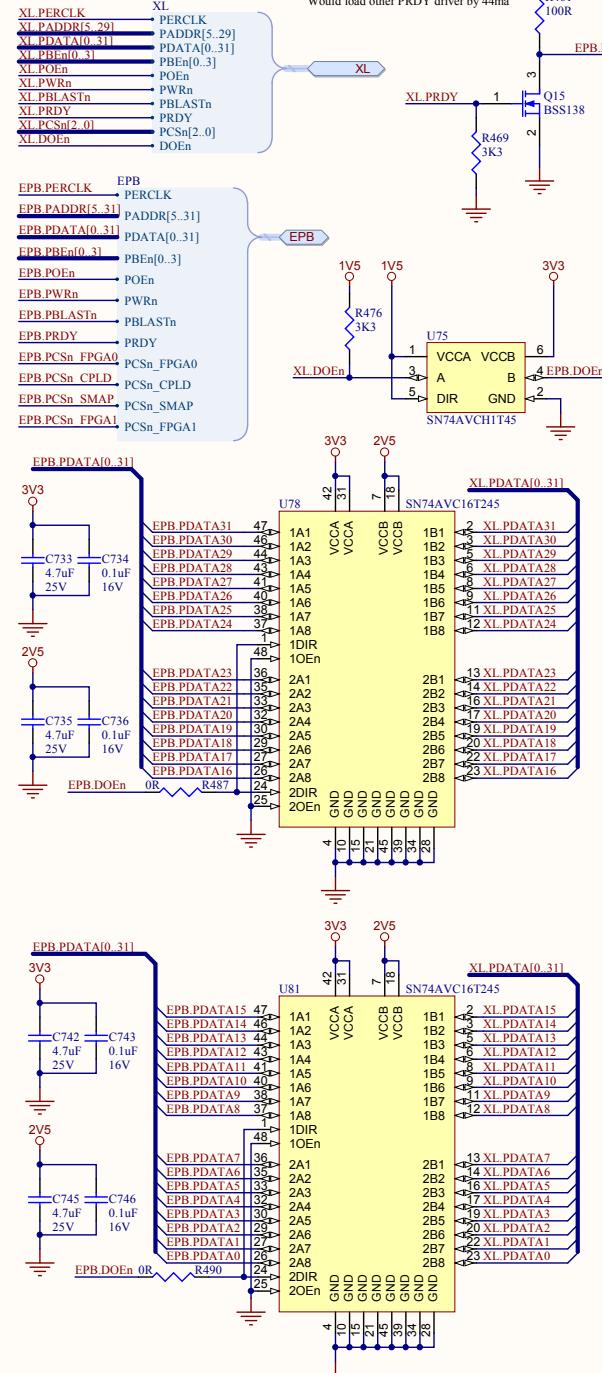
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