

**FDAS DDR CONTROLLER AND CALIBRATION BLOCK IN THE INTEL AGILEX F FPGA FAMILY**

FDAS\_DDR\_CONTROLLER\_DS Revision 3 Draft D

Classification: UNRESTRICTED

Document type: DTE

Date: 2023-02-05

Status:

© Copyright 2023 SKA Observatory.

  This work is licensed under a [Creative Commons Attribution 4.0 International License](http://creativecommons.org/licenses/by/4.0/)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| *Role* | *Name* | *Designation* | *Affiliation* | *Signature* | *Date* |
| Author | Martin Droog | FPGA Design Engineer | SKAO |  | 05/02/2023 |
| Owner | Ben Stappers | Head of SKA PSS Team | SKAO |  |  |
| Approver | Ben Stappers | Head of SKA PSS Team | SKAO |  |  |
| Released by | Lina Levin Preston | SKA PSS Team Scrum Master | SKAO |  |  |

|  |  |  |
| --- | --- | --- |
| Document History | | |
| Issue | Date | Comments |
| Issue 2 Draft A | 31/03/2022 | First Issue for review.  Comments from Prabu Thiagaraj and Atul Ghalame, and responses from Martin Droog:-  1) Pinouts for PCIe and DDR are given in the respective documents. It will be helpful to add the reference board schematics source (possibly a link to the intel schematics for the board or some file containing the pinouts). Once we have the board, we can perhaps upload relevant intel documents etc., with these details so that they will all be in one place.  **M. Droog Response: The Intel Agilex F Board schematics shall be referenced in this document.**  2) References to the DDR documentation etc. may be added to the document.  **M. Droog Response: The Intel Agilex DDR User Guide reference shall be added to this document as a table of references**  3) In the DDR interface document: page 8/25 says that the data lines could be selected from our sub bank and address from the inner sub bank. In our case, DDR side pinouts are fixed in the dev-kit. Could you please comment?  **M. Droog Response: The statement you are referring to is**  **“*If a DDR SDRAM memory interface spans more than one sub-bank then the control and address pins must be in the central sub-bank and the data pins can be assigned to outer sub-bank”.***  **This is a general Intel Agilex rule that must be adhered to when creating a DDR interface that needs to use more than one sub-bank. In the case of the Intel Agilex F Development Board Intel have defined the pinout for the DDR interfaces and they do abide by this rule, in that they support up to 72-data bit DDR interfaces and have ensured that the central sub-bank contains the Address/Control pins.**  4) Also, DDR clock considered is 1333.x MHz. If the design has to be ported for another speed DDR, I wonder how the clocks (333.x) scale fine?  **M. Droog Response: The maximum DDR interface clock speed that the Agilex FPGA family supports is 1333.33 MHz (using both clock edges with 64-bit data), which infers an internal clock speed of 333.33MHz (using just the rising clock edge with 512-bit data) to the DDRIF2 module within the FDAS FPGA. The DDRIF2 module contains phase buffers to cope with data transfer between the 333.33MHz DDR clock speed and the 350MHz internal core clock speeds. If the phase buffers are starting to get to full the signalling provided by the Avalon interface protocol used to connect the data paths allows data delivery to be paused. The CONV module which passes data to the DDRIF2 module to be written to DDR SDRAM therefore has to be designed to cope with back-pressure due to the DDRIF2 phase buffers starting to get too full.** |
| Issue 2 Draft B | 28/04/2022 | * Intel Agilex F Board schematics reference added. * Intel Agilex DDR User Guide reference added as a bookmark to a references table. |
| Issue 2 Draft C | 12/07/2022 | * Updated for the DDR SDRAM supplied with the Intel Agilex Development Kit DK-DEV-AGF014EA * Agilex FPGA AGFB014R24B2E2V * DDR4 SDRAM Modules: RDIMM DDR4 8GB K41197-001 MTA9ASF1G72PZ-2G9E1UI |
| Issue 2 Draft D | 18/07/2022 | * Typo correction |
| Issue 2 Draft E | 19/07/2022 | * Changed DDR4 PLL Clock Frequency to 33.333MHz to match the Development Board clock frequency. |
| Issue 2 Draft F | 22/07/2022 | * Added Appendix A to describe the FDAS DDR Controller design required for DDR Channel 1 which normally supports the HPS (Hard Processor Sub-System). |
| Issue 3 Draft A | 10/10/2022 | * DDR Controller and Calibration block designs to support all four DDR4 SDRAM interfaces of the Agilex FPGA. One DDR Controller and Calibration block design supports DDR channels 0 and 1, with channel 1 being repurposed from the HPS and the other DDR Controller and Calibration block design supports DDR channels 2 and 3. |
| Issue 3 Draft B | 19/10/2022 | * Renamed DDRIF2 instances to match DDR channel numbers. |
| Issue 3 Draft C | 2401/2023 | * Design changed to 1200MHz operation with ECC base on the parameters from the Intel Reference design as the 1333.333MHz presets in Intel Quartus Prime cause traffic errors in the DDR Controller. The intention is to eventually support 1333.333MHz, but until working parameters are available the design will use the Intel Reference design 1200MHz parameters with ECC enabled. |
| Issue 3 Draft D | 05/02/2023 | * The ECC seems to slow down the DDR SRDAM accesses by approx. 60%, Hence the ECC has been turned off on the FDAS\_DDR\_CONTROLLER to improve bandwidth. Quartus Prime does not allow the ECC to be turned off on the FDAS\_DDR\_CONTROLLER\_HPS |

**Table of Contents**

1 Introduction 6

2 Place in the System 8

3 Intel Agilex F DDR Controller and Calibration Block IP 10

3.1 Overview of External Memory Interfaces in Agilex F 10

3.2 FDAS Memory Bank Selection 13

3.3 DDR4 SDRAM Pinout 23

4 FDAS DDR Controller Simulation 35

4.1 Generation of DDR4 SDRAM Simulation Model 35

4.2 Creating Simulation Compile Script 35

5 FDAS\_DDR\_CONTROLLER\_CALIBRATION Architecture for DDR Channels 2 and 3 36

6 FDAS\_DDR\_CONTROLLER\_CALIBRATION\_HPS Architecture for DDR Channels 0 and 1 37

7 Design Requirement Tags 38

8 Interface Specifications 39

8.1 FDAS\_DDR\_CONTROLLER IP Component 39

8.2 FDAS\_DDR\_CONTROLLER\_HPS IP Component 43

8.3 FDAS\_EMIF\_CALIBRATION IP Component 47

9 MCI Memory Mapped Interface 48

10 Design Parameterisation 49

11 References 50

12 Abbreviations and Acronyms 51

# Introduction

This document captures the requirements for the DDR Controller used in the FDAS Intel Agilex F FPGA.

The Intel Agilex F Dev Kit DK-DEV-AGF014EA is fitted with the AGFB014R24B2E2V which supports up to four 72-bit DDR4 SDRAM Interfaces.

The supplied SDRAM modules are:-

DDR4 SDRAM Modules: RDIMM DDR4 8GB

K41197-001

MTA9ASF1G72PZ-2G9E1UI

For the FDAS version translated from Arria 10 to Agilex two DDR4 SDRAM Interfaces were required.

For the FDAS design in Agilex with improved processing times all four DDR SDRAM interfaces (including the DDR interface normally used by the on-board Hard Processor Sub-System) shall be used.

This document shall describe the DDR Controller and associated Calibration Blocks for the FDAS version with four DDR4 SDRAM interfaces, with each DDR4 SDRAM interface supported by a DDR Controller and with a Calibration block supporting each pair of DDR interfaces on the same side of the Agilex device.

DDR channels 0 and 1 are on one side of the Agilex device and DDR channels 2 and 3 are on the opposite side. On each side of the device is a single DDR Calibration block which serves all DDR Controllers in that side of the device.

DDR channel 1 is normally associated with an on-board Hard Processor System (HPS), however with appropriate settings in the Intel Quartus software design tool this DDR Controller can be re-purposed to be used by the FDAS function. Hence DDR Controller channel 1 requires different Intel Quartus software design tool settings compared to DDR Controller channels 0, 2 and 3.

The two DDR Controllers and associated DDR Calibration block for each side of the device are placed in a Wrapper to make instantiation in the FDAS Top Level structure more convenient. Since Channel 1 is different to the other channels this infers that two variants of the Wrapper are required. The one containing channels 2 and 3 shall be the “FDAS\_DDR\_CONTROLLER\_CALIBRATION” wrapper and the one containing channels 0 and 1 Wrapper shall be the “FDAS\_DDR\_CONTROLLER\_CALIBRATION\_HPS” wrapper to uniquely identify them.

The internal DDR Controller connection towards the core of the FDAS design shall be via a 512-bit data bus, operating at a maximum clock rate allowed by the Intel Agilex AGFB014R24B2E2V device. In the case of the AGFB014R24B2E2V Agilex F device the maximum DDR clock rate (to the external DDR SDRAMs) is 1333.333MHz, which infers a maximum internal clock of 333.333MHz to the core of the FDAS.

The intention is to use this clock frequency but currently the only DDR Controller parameters that support error free traffic are 1200MHz. These parameters have been obtained from the Intel Reference design.

The DDR Controller and associated Calibration Block shall be created using Intel IP via the Quartus Prime software version 22.2.

Note that the FDAS design only uses 4GByte of the DDR4 SDRAM

# Place in the System

The DDR Controller’s place in the FDAS FPGA is shown highlighted in the two figures below:-

**DDRIF2 #2**

**DDRIF2 #2**

PCIe

**CLD**

**CTRL**

FDAS Control

CLD\_DONE

**CONV**

data[63:0]

ready

**HSUM**

**FDAS**

CONV\_DONE CONV\_FFT\_REDAY

valid

**PCIE HARD IP MACRO (INTEL IP)**

**MCI\_TOP**

CLD\_DM\_TRIGGER

CLD\_ENABLE

CLD\_PAGE[31:0]

CONV\_DM\_TRIGGER

CONV\_ENABLE

CONV\_PAGE[31:0]

IFFT\_LOOP\_NUM[5:0]

HSUM\_DM\_TRIGGER

HSUM\_ENABLE

HSUM\_PAGE[31:0]

HSUM\_DONE

**PCIF**

ADDR

DATA[511:0]

**DDRIF2 #1**

**DDRIF2 #0, #2 and #34 acting in unison to provide a 1536-bit data interface to CONV and HSUM**

ADDR

3xDATA[5111:0]

3xDATA[511:0]

ADDR

ADDR

DATA[511:0]

*Note: The PCIe Hard Macro can read and write to allExternal DDR memories for diagnostic purposes. Not shown in this figure for clarity.*

*Note CLD, CONV and HSUM are designed with paging of the DDR memory for a future implementation. This allows different regions of the DDR SDRAM memory to be used to store data if desired.*

**FDAS\_DDR\_CONTROLLER\_CALIBRATION\_HPS (INTEL IP)**

**provides the DDR Controllers for DDRIF2#0 and DDRIF#1**

**FDAS\_DDR\_CONTROLLER\_CALIBRATION (INTEL IP)**

**provides the DDR Controllers for DDRIF2#2 and DDRIF#3**

DMA Transfer

**External 4 Gibi-Byte**

**DDR4 SDRAM Memory #1**

**External 4 Gibi-Byte**

**DDR4 SDRAM Memory #0. #2 and #3**

MC

Interface

Via

PCIe

*Note: In this implementation CLD\_PAGE, CONV\_PAGE and HSUM\_PAGE are fixed (static) in this implementation. However with a future implementation with more DDR Interfaces to CONV/HSUM a Paging technique shall enable increased processing performance.*

MC Bus

OVERLAP\_SIZE[9:0]

FOP\_SAMPLE\_NUM[22:0]

**MSIX**

MSI-X

Figure ‑ – DDR Controller Module Locations in FDAS

The figure below shows the detailed connectivity of the DDR Controller modules the FDAS design.

Figure ‑: Detailed DDR Controller Connectivity

PCIE

Hard IP

Macro

CLD

Module

CONV

Module

HSUM

Module

DDRIF2 #1 Module containing clock boundary FIFOs

DDR 4 SDRAM#1

**FDAS**

512-bit @ 350MHz access from PCIe to each DDRIF2

512-bit @ 350MHz

1536-bit @ 350MHz

1536-bit @ 350MHz

64-bit @ 1200MHz

C

A

L

DDR\_

CONT

HPS

Ch 1

FDAS\_DDR\_

CONTROLLER\_HPS

CALIBRATION

(INTEL IP) #1

DDR\_

CONT

Ch 0

DDRIF2 #0 Module containing clock boundary FIFOs

DDR 4 SDRAM#0

64-bit @ 1200MHz

DDRIF2 #2 Module containing clock boundary FIFOs

DDR 4 SDRAM#2

64-bit @ 1200MHz

C

A

L

DDR\_

CONT

Ch 2

FDAS\_DDR\_

CONTROLLER\_

CALIBRATION

(INTEL IP) #1

DDR\_

CONT

Ch 3

DDRIF2 #3 Module containing clock boundary FIFOs

DDR 4 SDRAM#3

64-bit @ 1200MHz

“FIFO\_READY”, “FIFO\_FULL” and “DATA\_AVAIL” signals transferred between DDRIF2 modules for CONV/ HSUM data paths

512 bits to/from each DDRIF2

# Intel Agilex F DDR Controller and Calibration Block IP

## Overview of External Memory Interfaces in Agilex F

The External Memory Interfaces are supported by blocks at the upper and lower edges of the Agilex F device.

An Intel document describes the External Memory Interface in Agilex [Ref: Agilex DDR User Guide].

Figure 3‑1 below shows the positions of the I/O banks in two rows (2 & 3) which support the external memory interfaces in the AGFB014R24B2E2V device. Each bank is sub-divided into sub-bank “top” and “bottom” with the outer sub-bank designated as “top”. The “HPS” is the Hard Processor Sub-System which can use Bank 3D to provide an external memory interface. The Zipper block performs routing adjustments where routing wires cross the Zipper.

Transceiver Block

Transceiver Block

3A

Top

3A

Bottom

3B

Top

3B

Bottom

3C

Top

3C

Bottom

3D

Top

3D

Bottom

2A

Bottom

2A

Top

2B

Bottom

2B

Top

2C

Bottom

2C

Top

2D

Bottom

2D

Top

HPS

Zipper

Row 3 External Memory Banks

Row 2 External Memory Banks

72-bitDDR I/F Channel 0

72-bit DDR I/F Channel 3

72-bit DDR I/F Channel 1

72-bit DDRI/F Channel 2

Figure 3‑1: External Memory Banks in Agilex AGFB014R24B2E2V

Each row includes one I/O subsystem manager which contains a NIOS II processor which is used to provide the calibration of the external memory interfaces of that row.

Each sub-bank contains:

* Hard Memory Controller
* Sequencer Components
* I/O PLL and PHY clock trees
* DLL
* Input DQS clock trees
* 48 pins, organised into for lanes each of 12 pins

Each sub-bank contains all the functions to build an external memory interface. A wider interface can be made by connecting multiple adjacent sub-banks together in the order shown below:-

The Top Row sub-bank ordering for the AGFB014R24B2E2V device is shown in Figure 3‑2 below:-

Figure 3‑2: Top Row Sub-Bank Ordering When Connecting Adjacent Sub-banks

Bank 3C

Top Sub-bank

Lane 0 (48-59

Lane 1 (60-71)

Lane 2 (72-83)

Lane 3 (84-95)

Bottom Sub-bank

Lane 0 (0-11)

Lane 1 (12-23)

Lane 2 (24-35)

Lane 3 (36-47)

Lane 0 (0-11)

Bank 3A

Top Sub-bank

Lane 3 (84-95)

Lane 2 (72-83)

Lane 1 (60-71)

Lane 0 (48-59)

Bottom Sub-bank

Lane 3 (36-47)

Lane 2 (24-35)

Lane 1 (12-23)

Lane 0 (0-11)

Bank 3B

Top Sub-bank

Lane 3 (84-95)

Lane 2 (72-83)

Lane 1 (60-71)

Lane 0 (48-59)

Bottom Sub-bank

Lane 3 (36-47)

Lane 2 (24-35)

Lane 1 (12-23)

Lane 0 (0-11)

Bank 3D

Top Sub-bank

Lane 0 (48-59)

Lane 1 (60-71)

Lane 2 (72-83)

Lane 3 (8495)

Bottom Sub-bank

Lane 0 (0-11)

Lane 1 (12-23)

Lane 2 (24-35)

Lane 3 (36-47)

Zipper

The Bottom Row sub-bank ordering for the AGFB014R24B2E2V device is shown in Figure 3‑3 below:-

Bank 2C

Bottom Sub-bank

Lane 0 (0-11)

Lane 1 (12-23)

Lane 2 (24-35

Lane 3 (36-47

Top Sub-bank

Lane 0 (48-59)

Lane 1 (60-71)

Lane 2 (72-83)

Lane 3 (84-95)

Lane 0 (0-11)

Bank 2A

Bottom Sub-bank

Lane 3 (36-47)

Lane 2 (24-35)

Lane 1 (12-23)

Lane 0 (0-11)

Top Sub-bank

Lane 3 (84-95)

Lane 2 (72-83)

Lane 1 (60-71)

Lane 0 (48-59)

Bank 2B

Bottom Sub-bank

Lane 3 (36-47)

Lane 2 (24-35)

Lane 1 (12-23)

Lane 0 (0-11)

Top Sub-bank

Lane 3 (84-95)

Lane 2 (72-83)

Lane 1 (60-71)

Lane 0 (48-59)

Bank2D

Bottom Sub-bank

Lane 0 (0-11)

Lane 1 (12-23)

Lane 2 (24-35)

Lane 3 (36-47)

Top Sub-bank

Lane 0 (48-59)

Lane 1 (60-71)

Lane 2 (72-83)

Lane 3 (74-95)

Zipper

Figure 3‑3: Bottom Row Sub-Bank Ordering When Connecting Adjacent Sub-banks

If a DDR SDRAM memory interface spans more than one sub-bank then the control and address pins must be in the central sub-bank and the data pins can be assigned to outer sub-banks.

**A sub-bank cannot be shared across different external memory interfaces.**

This effectively limits the Agilex device AGFB014R24B2E2V to four external 72-bit DDR4 SDRAM interfaces, since each interface uses three sub-banks.

## FDAS Memory Bank Selection

The FDAS FPGA requires four 64-bit DDR4 Interfaces to provide the maximum performance. Hence all DDR Interfaces of the Intel Agilex F device are used.

#### External Memory Controller IP for DDR Channels 0, 2 and 3

The External Memory Controller IP (i.e. DDR Controller”) is generated using the Intel Quartus Prime software version 22.2.0.

Quartus Prime software version 22.2 IP Catalog.

The “IP Catalog” shall be used with the following selected:-

Memory Interfaces and Controllers > External Memory Interfaces Intel Agilex FPGA IP

This launches “IP Platform Designer” which then asks for a name for the IP Variation which shall be entered as “FDAS\_DDR\_CONTROLLER”

The intention is to use the DDR Controller at its maximum declared frequency of 1333.333MHz. However, currently no parameters are available to support error free traffic operation.

Hence the 1200MHz parameters available in an Intel Reference design shall be used. **However with ECC enabled the DDR bandwidth seems to reduce by approximately 60%. Hence ECC shall be disabled.**

The full list of settings is:-

**General Tab**

=======

**Speed Grade:** E2V

**Configuration:** Hard PHY and Hard Controller

**Use Clamshell layout:** OFF

**Memory Clock Frequency:** 1200.0MHz

**Use recommended PLL reference clock frequency:** OFF

**PLL ref clock frequency:**  33.333MHz

**PLL ref clock jitter:** 10ps

**Clock rate of user logic:**  Quarter

**Specify additional core clocks based on existing PLL:** OFF

**Mimic HPS EMIF:** OFF

**Memory Tab**

======

**Memory Format:** RDIMM

**DQ Width:** 72

**DQ pins per DQS group:** 8

**Number of DQS groups:** 9

**Number of Clocks:** 1

**Number of DIMMs:** 1

**Chip ID width:** 0 (non-3DS)

**Number of Physical Ranks per DIMM:** 1

**Number of Chip Selects per DIMM:** 1

**Row Address Width:** 16

**Column Address Width:** 10

**Bank Address Width:** 2

**Bank Group Width:** 2

**Data Mask:** ON

**Write DBI:**  OFF

**Read DBI:** ON

**ALERT# Pin Placement:** Address/Command

Lane 3, Pin 8

**Memory CAS latency setting:** 21

**Memory Write CAS latency setting:** 16

**Memory additive CAS latency setting:** Disabled

**Addr/CMD parity latency:** Disabled

**Fine granularity refresh:** Fixed 1x

**Mem I/O Tab**

=======

**Use Default Memory I/O settings:** ON

**Output drive strength setting:** RZQ/7 (34 Ohm)

**Dynamic ODT (Rtt\_WR) value:** Dynamic ODT off

**ODT Rtt nominal value:** ODT Disabled

**RTT PARK:** RZQ/4 (60 Ohm)

**RCD CA Input Bus Termination:** 100 Ohm

**RDC DCS[3:0]\_n Input Bus Termination:** 100 Ohm

**RCD DCKE Input Bus Termination:** 100 Ohm

**RCD DODT Input Bus Termination:** 100 Ohm

**Use recommended initial VrefDQ value:** ON

**VrefDQ training value:** 70.0

**VrefDQ training range:** Range 1 - 60% to 92.5%

**SPD Byte 137 - RCD Drive Strength for Command/Address:** 0x65

**SPD Byte 138 - RCD Drive Strength for CK:** 0x05

**Use Default ODT Assertion Tables:** ON

**Derived ODT Matrix for Read Access** Rank 0 (Drive)

RZQ/7 (34 Ohm)

**Derived ODT Matrix for Write Access** Rank 0 (Park)

RZQ/4 (60 Ohm)

**FPGA I/O Tab**

========

**Voltage:** 1.2V

**Use Default I/O settings:** OFF

**Address/Command:**

**I/O standard:**  SSTL-12

**Output mode:** 40 Ohm with calibration

**Slew rate:** FAST

(unset in ref design)

**Deemphasis mode:** OFF

(unset in ref design)

**Memory Clock:**

**I/O standard:** SSTL-12

**Output mode:** 40 Ohm with calibration

**Slew rate:** FAST

(unset in ref design)

**Deemphasis mode:** OFF

(unset in ref design)

**Data Bus:**

**I/O standard**: 1.2V-POD

**Output mode:**  40 Ohm with calibration

**Slew rate:** FAST

(unset in ref design)

**Deemphasis mode:** HIGH

(unset in ref design)

**Input mode:** 60 Ohm with calibration

**Use recommended initial Vrefin** ON

**Initial Vrefin:** 68%

**PHY Inputs:**

**PLL reference clock I/O standard**: True Differential signalling

with On-Chip Termination

**RZQ I/O standard:** 1.2-V

**RZQ resistor:** 240 Ohm

**Mem Timing Tab**

===========

**Speed Bin:** -2666

**tlS (base):** 62 ps

**tlS (base) AC level:** 100mV

**tlH (base):** 87ps

**tlH (base) DC level:** 75mV

**TdivW\_total:** 0.2UI

**VdiVW\_total:** 130mV

**tDQSQ:** 0.14UI

**tQH:** 0.74UI

**tDVWp:** 0.72UI

**tDQSCK:** 175ps

**tDQSS:** 0.27 cycles

**tQSH:** 0.4 cycles

**tDSH:** 0.18 cycles

**tDSS:** 0.18 cycles

**tWLS:** 0.13 cycles

**tWLH:** 0.13 cycles

**tINIT:** 500us

**tRMD:** 8 cycles

**tRAS:** 32.0ns

**tRCD:** 14.16ns

**tRP:** 14.16ns

**tWR:** 15.0ns

**tRRD\_S:** 4 cycles

**tRRD\_L:** 6 cycles

**tFAW:** 21.0ns

**tCCD\_S:** 4 cycles

**tCCD\_L:** 6 cycles

**tWTR\_S:** 3 cycles

**tWTR\_L:** 9 cycles

**tRFC:** 350.0ns

**tREFI:** 7.8us

**Board Tab**

======

Refer to board layout guidelines in EMIF user

guide to design your board to the to the

given memory configuration.

**Controller Tab**

===========

**Enable Auto Power-Down:** OFF

**Auto Power-Down cycles:** 32 cycles

**Enable User Refresh Control:** OFF

**Enable Auto-Precharge Control:** OFF

**Address Ordering:** CS-CID-Row-Bank-Col-BG

**Enable Re-ordering:** ON

**Starvation Limit for each command:** 10

**Enable Command Priority Control:**  OFF

**Enable controller major mode:** OFF (not in Ref design)

**Enable controller post-pay refresh:** OFF (not in Ref design)

**Enable controller pre-pay refresh:** OFF (not in Ref design)

**Enable Memory-Mapped Configuration**

**and Status Register (MMR) Interface:** OFF

**Enable Error Detection and Error Correction Logic**

**with ECC:**  OFF

**Enable Auto correction to External Memory** OFF

**Enable ctrl\_ecc\_readdataerror signal to indicate**

**Uncorrectable data errors** OFF

**Export error-correction code (ECC) status ports:**  OFF

**Additional read-to-write turnaround time (same rank):** 0 cycles

**Additional write-to-read turnaround time (same rank):** 0 cycles

**Additional read-to-read turnaround time (different ranks):** 0 cycles

**Additional read-to-write turnaround time (different ranks):** 0 cycles

**Additional write-to-write turnaround time (different ranks):** 0 cycles

**Additional write-to-read turnaround time (different ranks)):** 0 cycles

This populates all the necessary External Memory settings. This can then be saved and the HDL can be generated (click “Generate HDL” button) ensuring that the selected language is VHDL.

#### External Memory Controller IP for DDR Channel 1

The External Memory Controller IP (i.e. DDR Controller”) is generated using the Intel Quartus Prime software version 22.2 IP Catalog.

The “IP Catalog” shall be used with the following selected:-

Memory Interfaces and Controllers > External Memory Interfaces Intel Agilex FPGA IP

This launches “IP Platform Designer” which then asks for a name for the IP Variation which shall be entered as “FDAS\_DDR\_CONTROLLER\_HPS”

The intention is to use the DDR Controller at its maximum declared frequency of 1333.333MHz. However, currently no parameters are available to support error free traffic operation.

Hence the 1200MHz parameters available in an Intel Reference design shall be used.

The full list of settings is:-

**General Tab**

=======

**Speed Grade:** E2V

**Configuration:** Hard PHY and Hard Controller

**Use Clamshell layout:** OFF

**Memory Clock Frequency:** 1200.0MHz

**Use recommended PLL reference clock frequency:** OFF

**PLL ref clock frequency:**  33.333MHz

**PLL ref clock jitter:** 10ps

**Clock rate of user logic:**  Quarter

**Specify additional core clocks based on existing PLL:** OFF

**Mimic HPS EMIF:** ON

**Memory Tab**

======

**Memory Format:** RDIMM

**DQ Width:** 72

**DQ pins per DQS group:** 8

**Number of DQS groups:** 9

**Number of Clocks:** 1

**Number of DIMMs:** 1

**Chip ID width:** 0 (non-3DS)

**Number of Physical Ranks per DIMM:** 1

**Number of Chip Selects per DIMM:** 1

**Row Address Width:** 16

**Column Address Width:** 10

**Bank Address Width:** 2

**Bank Group Width:** 2

**Data Mask:** ON

**Write DBI:**  OFF

**Read DBI:** ON

**ALERT# Pin Placement:** Address/Command

Lane 2, Pin 8

**Memory CAS latency setting:** 21

**Memory Write CAS latency setting:** 16

**Memory additive CAS latency setting:** Disabled

**Addr/CMD parity latency:** Disabled

**Fine granularity refresh:** Fixed 1x

**Mem I/O Tab**

=======

**Use Default Memory I/O settings:** ON

**Output drive strength setting:** RZQ/7 (34 Ohm)

**Dynamic ODT (Rtt\_WR) value:** Dynamic ODT off

**ODT Rtt nominal value:** ODT Disabled

**RTT PARK:** RZQ/4 (60 Ohm)

**RCD CA Input Bus Termination:** 100 Ohm

**RDC DCS[3:0]\_n Input Bus Termination:** 100 Ohm

**RCD DCKE Input Bus Termination:** 100 Ohm

**RCD DODT Input Bus Termination:** 100 Ohm

**Use recommended initial VrefDQ value:** ON

**VrefDQ training value:** 70.0

**VrefDQ training range:** Range 1 - 60% to 92.5%

**SPD Byte 137 - RCD Drive Strength for Command/Address:** 0x65

**SPD Byte 138 - RCD Drive Strength for CK:** 0x05

**Use Default ODT Assertion Tables:** ON

**Derived ODT Matrix for Read Access** Rank 0 (Drive)

RZQ/7 (34 Ohm)

**Derived ODT Matrix for Write Access** Rank 0 (Park)

RZQ/4 (60 Ohm)

**FPGA I/O Tab**

========

**Voltage:** 1.2V

**Use Default I/O settings:** OFF

**Address/Command:**

**I/O standard:**  SSTL-12

**Output mode:** 40 Ohm with calibration

**Slew rate:** FAST

(unset in ref design)

**Deemphasis mode:** OFF

(unset in ref design)

**Memory Clock:**

**I/O standard:** SSTL-12

**Output mode:** 40 Ohm with calibration

**Slew rate:** FAST

(unset in ref design)

**Deemphasis mode:** OFF

(unset in ref design)

**Data Bus:**

**I/O standard**: 1.2V-POD

**Output mode:**  40 Ohm with calibration

**Slew rate:** FAST

(unset in ref design)

**Deemphasis mode:** HIGH

(unset in ref design)

**Input mode:** 60 Ohm with calibration

**Use recommended initial Vrefin** ON

**Initial Vrefin:** 68%

**PHY Inputs:**

**PLL reference clock I/O standard**: True Differential signalling

with On-Chip Termination

**RZQ I/O standard:** 1.2-V

**RZQ resistor:** 240 Ohm

**Mem Timing Tab**

===========

**Speed Bin:** -2666

**tlS (base):** 62 ps

**tlS (base) AC level:** 100mV

**tlH (base):** 87ps

**tlH (base) DC level:** 75mV

**TdivW\_total:** 0.2UI

**VdiVW\_total:** 130mV

**tDQSQ:** 0.14UI

**tQH:** 0.74UI

**tDVWp:** 0.72UI

**tDQSCK:** 175ps

**tDQSS:** 0.27 cycles

**tQSH:** 0.4 cycles

**tDSH:** 0.18 cycles

**tDSS:** 0.18 cycles

**tWLS:** 0.13 cycles

**tWLH:** 0.13 cycles

**tINIT:** 500us

**tRMD:** 8 cycles

**tRAS:** 32.0ns

**tRCD:** 14.16ns

**tRP:** 14.16ns

**tWR:** 15.0ns

**tRRD\_S:** 4 cycles

**tRRD\_L:** 6 cycles

**tFAW:** 21.0ns

**tCCD\_S:** 4 cycles

**tCCD\_L:** 6 cycles

**tWTR\_S:** 3 cycles

**tWTR\_L:** 9 cycles

**tRFC:** 350.0ns

**tREFI:** 7.8us

**Board Tab**

======

Refer to board layout guidelines in EMIF user

guide to design your board to the to the

given memory configuration.

**Controller Tab**

===========

**Enable Auto Power-Down:** OFF

**Auto Power-Down cycles:** 32 cycles

**Enable User Refresh Control:** OFF

**Enable Auto-Precharge Control:** OFF

**Address Ordering:** CS-CID-Row-Bank-Col-BG

**Enable Re-ordering:** ON

**Starvation Limit for each command:** 10

**Enable Command Priority Control:**  OFF

**Enable controller major mode:** OFF (not in Ref design)

**Enable controller post-pay refresh:** OFF (not in Ref design)

**Enable controller pre-pay refresh:** OFF (not in Ref design)

**Enable Memory-Mapped Configuration**

**and Status Register (MMR) Interface:** OFF

**Enable Error Detection and Error Correction Logic**

**with ECC:**  ON

**Enable Auto correction to External Memory** OFF

**Enable ctrl\_ecc\_readdataerror signal to indicate**

**Uncorrectable data errors** OFF

**Export error-correction code (ECC) status ports:**  OFF

**Additional read-to-write turnaround time (same rank):** 0 cycles

**Additional write-to-read turnaround time (same rank):** 0 cycles

**Additional read-to-read turnaround time (different ranks):** 0 cycles

**Additional read-to-write turnaround time (different ranks):** 0 cycles

**Additional write-to-write turnaround time (different ranks):** 0 cycles

**Additional write-to-read turnaround time (different ranks)):** 0 cycles

This populates all the necessary External Memory settings. This can then be saved and the HDL can be generated (click “Generate HDL” button) ensuring that the selected language is VHDL.

#### External Memory Interface Calibration IP

The External Memory Interface Calibration IP (i.e. DDR Controller) is generated using the Intel Quartus Prime software version 22.2 IP Catalog.

The “IP Catalog” shall be used with the following selected:-

Memory Interfaces and Controllers > External Memory Interfaces Intel Calibration IP

This launches “IP Platform Designer” which then asks for a name for the IP Variation which shall be entered as “FDAS\_EMIF\_CALIBRATION”

Enter the following settings:-

**Number of Calibration Interfaces:** 2

**Quartus Prime RMIF Debug toolkit/On-chip Debug port:** Disabled

**Calibration for Simulation:** Skip Calibration

**Show verbose simulation debug messages:** OFF

This can then be saved and the HDL can be generated (click “Generate HDL” button) ensuring that the selected language is VHDL.

#### Instantiation of the External Memory Interface

The FDAS\_DDR\_CONTROLLER, FDAS\_DDR\_CONTROLLER\_HPS and associated FDAS\_EMIF\_CALIBRATION modules are combined in a VHDL Wrapper.

Two FDAS\_DDR\_CONTROLLER blocks and an FDAS\_EMIF\_CALIBRATION block are contained in an FDAS\_DDR\_CONTROLLER\_CALIBRATION VHDL Wrapper.

An FDAS\_DDR\_CONTROLLER block, an FDAS\_DDR\_CONTROLLER\_HPS block and an FDAS\_EMIF\_CALIBRATION block are contained in an FDAS\_DDR\_CONTROLLER\_CALIBRATION\_HPS VHDL Wrapper.

## DDR4 SDRAM Pinout

The DDR4 pinout in the .qsf file is consistent with the Intel Agilex F-Series Development Board which supports the AGFB014R24B2E2V Intel Agilex device [Ref: Agilex Development Board].

**FDAS External Memory Interface #1 for CLD :**

**Connected to Banks 3C/3D (DDR I/F Channel 1)**

PIN\_L10 -to PLL\_REF\_CLK\_1

PIN\_T17 -to MEM1\_A[0]

PIN\_V17 -to MEM1\_A[1]

PIN\_U16 -to MEM1\_A[2]

PIN\_W16 -to MEM1\_A[3]

PIN\_T15 -to MEM1\_A[4]

PIN\_V15 -to MEM1\_A[5]

PIN\_U14 -to MEM1\_A[6]

PIN\_W14 -to MEM1\_A[7]

PIN\_T13 -to MEM1\_A[8]

PIN\_V13 -to MEM1\_A[9]

PIN\_U12 -to MEM1\_A[10]

PIN\_W12 -to MEM1\_A[11]

PIN\_P9 -to MEM1\_A[12]

PIN\_L8 -to MEM1\_A[13]

PIN\_N8 -to MEM1\_A[14]

PIN\_M7 -to MEM1\_A[15]

PIN\_P7 -to MEM1\_A[16]

PIN\_N16 -to MEM1\_ACT\_N[0]

PIN\_L6 -to MEM1\_ALERT\_N[0]

PIN\_N6 -to MEM1\_BA[0]

PIN\_M5 -to MEM1\_BA[1]

PIN\_P5 -to MEM1\_BG[0]

PIN\_M17 -to MEM1\_BG[1]

PIN\_M13 -to MEM1\_CK[0]

PIN\_P13 -to MEM1\_CK\_N[0]

PIN\_L14 -to MEM1\_CKE[0]

PIN\_L16 -to MEM1\_CS\_N[0]

PIN\_M15 -to MEM1\_ODT[0]

PIN\_A10 -to MEM1\_DQ[0]

PIN\_C10 -to MEM1\_DQ[1]

PIN\_B9 -to MEM1\_DQ[2]

PIN\_D9 -to MEM1\_DQ[3]

PIN\_A6 -to MEM1\_DQ[4]

PIN\_B5 -to MEM1\_DQ[5]

PIN\_C6 -to MEM1\_DQ[6]

PIN\_D5 -to MEM1\_DQ[7]

PIN\_G10 -to MEM1\_DQ[8]

PIN\_J10 -to MEM1\_DQ[9]

PIN\_F9 -to MEM1\_DQ[10]

PIN\_H9 -to MEM1\_DQ[11]

PIN\_G6 -to MEM1\_DQ[12]

PIN\_J6 -to MEM1\_DQ[13]

PIN\_F5 -to MEM1\_DQ[14]

PIN\_H5 -to MEM1\_DQ[15]

PIN\_F17 -to MEM1\_DQ[16]

PIN\_H17 -to MEM1\_DQ[17]

PIN\_G16 -to MEM1\_DQ[18]

PIN\_J16 -to MEM1\_DQ[19]

PIN\_F13 -to MEM1\_DQ[20]

PIN\_J12 -to MEM1\_DQ[21]

PIN\_H13 -to MEM1\_DQ[22]

PIN\_G12 -to MEM1\_DQ[23]

PIN\_B17 -to MEM1\_DQ[24]

PIN\_D17 -to MEM1\_DQ[25]

PIN\_A16 -to MEM1\_DQ[26]

PIN\_C16 -to MEM1\_DQ[27]

PIN\_B13 -to MEM1\_DQ[28]

PIN\_D13 -to MEM1\_DQ[29]

PIN\_A12 -to MEM1\_DQ[30]

PIN\_C12 -to MEM1\_DQ[31]

PIN\_U24 -to MEM1\_DQ[32]

PIN\_W24 -to MEM1\_DQ[33]

PIN\_T23 -to MEM1\_DQ[34]

PIN\_V23 -to MEM1\_DQ[35]

PIN\_U20 -to MEM1\_DQ[36]

PIN\_W20 -to MEM1\_DQ[37]

PIN\_T19 -to MEM1\_DQ[38]

PIN\_V19 -to MEM1\_DQ[39]

PIN\_L24 -to MEM1\_DQ[40]

PIN\_N24 -to MEM1\_DQ[41]

PIN\_M23 -to MEM1\_DQ[42]

PIN\_P23 -to MEM1\_DQ[43]

PIN\_L20 -to MEM1\_DQ[44]

PIN\_P19 -to MEM1\_DQ[45]

PIN\_N20 -to MEM1\_DQ[46]

PIN\_M19 -to MEM1\_DQ[47]

PIN\_M31 -to MEM1\_DQ[48]

PIN\_P31 -to MEM1\_DQ[49]

PIN\_L30 -to MEM1\_DQ[50]

PIN\_N30 -to MEM1\_DQ[51]

PIN\_M27 -to MEM1\_DQ[52]

PIN\_P27 -to MEM1\_DQ[53]

PIN\_L26 -to MEM1\_DQ[54]

PIN\_N26 -to MEM1\_DQ[55]

PIN\_T31 -to MEM1\_DQ[56]

PIN\_V31 -to MEM1\_DQ[57]

PIN\_U30 -to MEM1\_DQ[58]

PIN\_W30 -to MEM1\_DQ[59]

PIN\_T27 -to MEM1\_DQ[60]

PIN\_W26 -to MEM1\_DQ[61]

PIN\_V27 -to MEM1\_DQ[62]

PIN\_U26 -to MEM1\_DQ[63]

PIN\_U10 -to MEM1\_DQ[64]

PIN\_W10 -to MEM1\_DQ[65]

PIN\_T9 -to MEM1\_DQ[66]

PIN\_V9 -to MEM1\_DQ[67]

PIN\_U6 -to MEM1\_DQ[68]

PIN\_W6 -to MEM1\_DQ[69]

PIN\_T5 -to MEM1\_DQ[70]

PIN\_V5 -to MEM1\_DQ[71]

PIN\_A8 -to MEM1\_DQS[0]

PIN\_C8 -to MEM1\_DQS\_N[0]

PIN\_G8 -to MEM1\_DQS[1]

PIN\_J8 -to MEM1\_DQS\_N[1]

PIN\_F15 -to MEM1\_DQS[2]

PIN\_H15 -to MEM1\_DQS\_N[2]

PIN\_B15 -to MEM1\_DQS[3]

PIN\_D15 -to MEM1\_DQS\_N[3]

PIN\_U22 -to MEM1\_DQS[4]

PIN\_W22 -to MEM1\_DQS\_N[4]

PIN\_L22 -to MEM1\_DQS[5]

PIN\_N22 -to MEM1\_DQS\_N[5]

PIN\_M29 -to MEM1\_DQS[6]

PIN\_P29 -to MEM1\_DQS\_N[6]

PIN\_T29 -to MEM1\_DQS[7]

PIN\_V29 -to MEM1\_DQS\_N[7]

PIN\_U8 -to MEM1\_DQS[8]

PIN\_W8 -to MEM1\_DQS\_N[8]

PIN\_B7 -to MEM1\_DBI\_N[0]

PIN\_F7 -to MEM1\_DBI\_N[1]

PIN\_G14 -to MEM1\_DBI\_N[2]

PIN\_A14 -to MEM1\_DBI\_N[3]

PIN\_T21 -to MEM1\_DBI\_N[4]

PIN\_M21 -to MEM1\_DBI\_N[5]

PIN\_L28 -to MEM1\_DBI\_N[6]

PIN\_U28 -to MEM1\_DBI\_N[7]

PIN\_T7 -to MEM1\_DBI\_N[8]

PIN\_N12 -to MEM1\_PAR[0]

PIN\_P17 -to MEM1\_RESET\_N[0]

PIN\_M9 -to OCT\_RZQIN1

**FDAS External Memory Interface #0 for CONV/HSUM :**

**Connected to Banks 3A/3B (DDR I/F Channel 0)**

PIN\_L40 -to PLL\_REF\_CLK\_0

PIN\_T33 -to MEM0\_A[0]

PIN\_V33 -to MEM0\_A[1]

PIN\_U34 -to MEM0\_A[2]

PIN\_W34 -to MEM0\_A[3]

PIN\_T35 -to MEM0\_A[4]

PIN\_V35 -to MEM0\_A[5]

PIN\_U36 -to MEM0\_A[6]

PIN\_W36 -to MEM0\_A[7]

PIN\_T37 -to MEM0\_A[8]

PIN\_V37 -to MEM0\_A[9]

PIN\_U38 -to MEM0\_A[10]

PIN\_W38 -to MEM0\_A[11]

PIN\_P41 -to MEM0\_A[12]

PIN\_L42 -to MEM0\_A[13]

PIN\_N42 -to MEM0\_A[14]

PIN\_M43 -to MEM0\_A[15]

PIN\_P43 -to MEM0\_A[16]

PIN\_N34 -to MEM0\_ACT\_N[0]

PIN\_U44 -to MEM0\_ALERT\_N[0]

PIN\_N44 -to MEM0\_BA[0]

PIN\_M45 -to MEM0\_BA[1]

PIN\_P45 -to MEM0\_BG[0]

PIN\_M33 -to MEM0\_BG[1]

PIN\_M37 -to MEM0\_CK[0]

PIN\_P37 -to MEM0\_CK\_N[0]

PIN\_L36 -to MEM0\_CKE[0]

PIN\_L34 -to MEM0\_CS\_N[0]

PIN\_M35 -to MEM0\_ODT[0]

PIN\_F33 -to MEM0\_DQ[0]

PIN\_H33 -to MEM0\_DQ[1]

PIN\_G34 -to MEM0\_DQ[2]

PIN\_J34 -to MEM0\_DQ[3]

PIN\_J38 -to MEM0\_DQ[4]

PIN\_G38 -to MEM0\_DQ[5]

PIN\_F37 -to MEM0\_DQ[6]

PIN\_H37 -to MEM0\_DQ[7]

PIN\_B33 -to MEM0\_DQ[8]

PIN\_D33 -to MEM0\_DQ[9]

PIN\_A34 -to MEM0\_DQ[10]

PIN\_C34 -to MEM0\_DQ[11]

PIN\_D37 -to MEM0\_DQ[12]

PIN\_A38 -to MEM0\_DQ[13]

PIN\_B37 -to MEM0\_DQ[14]

PIN\_C38 -to MEM0\_DQ[15]

PIN\_A40 -to MEM0\_DQ[16]

PIN\_C40 -to MEM0\_DQ[17]

PIN\_B41 -to MEM0\_DQ[18]

PIN\_D41 -to MEM0\_DQ[19]

PIN\_D45 -to MEM0\_DQ[20]

PIN\_B45 -to MEM0\_DQ[21]

PIN\_A44 -to MEM0\_DQ[22]

PIN\_C44 -to MEM0\_DQ[23]

PIN\_G40 -to MEM0\_DQ[24]

PIN\_J40 -to MEM0\_DQ[25]

PIN\_F41 -to MEM0\_DQ[26]

PIN\_H41 -to MEM0\_DQ[27]

PIN\_J44 -to MEM0\_DQ[28]

PIN\_H45 -to MEM0\_DQ[29]

PIN\_G44 -to MEM0\_DQ[30]

PIN\_F45 -to MEM0\_DQ[31]

PIN\_G48 -to MEM0\_DQ[32]

PIN\_F47 -to MEM0\_DQ[33]

PIN\_J48 -to MEM0\_DQ[34]

PIN\_H47 -to MEM0\_DQ[35]

PIN\_F51 -to MEM0\_DQ[36]

PIN\_H51 -to MEM0\_DQ[37]

PIN\_G52 -to MEM0\_DQ[38]

PIN\_J52 -to MEM0\_DQ[39]

PIN\_F55 -to MEM0\_DQ[40]

PIN\_G54 -to MEM0\_DQ[41]

PIN\_H55 -to MEM0\_DQ[42]

PIN\_J54 -to MEM0\_DQ[43]

PIN\_J58 -to MEM0\_DQ[44]

PIN\_F59 -to MEM0\_DQ[45]

PIN\_G58 -to MEM0\_DQ[46]

PIN\_H59 -to MEM0\_DQ[47]

PIN\_B55 -to MEM0\_DQ[48]

PIN\_A54 -to MEM0\_DQ[49]

PIN\_D55 -to MEM0\_DQ[50]

PIN\_C54 -to MEM0\_DQ[51]

PIN\_D59 -to MEM0\_DQ[52]

PIN\_C58 -to MEM0\_DQ[53]

PIN\_F61 -to MEM0\_DQ[54]

PIN\_H61 -to MEM0\_DQ[55]

PIN\_V55 -to MEM0\_DQ[56]

PIN\_T55 -to MEM0\_DQ[57]

PIN\_W54 -to MEM0\_DQ[58]

PIN\_U54 -to MEM0\_DQ[59]

PIN\_W58 -to MEM0\_DQ[60]

PIN\_T59 -to MEM0\_DQ[61]

PIN\_U58 -to MEM0\_DQ[62]

PIN\_V59 -to MEM0\_DQ[63]

PIN\_A48 -to MEM0\_DQ[64]

PIN\_B47 -to MEM0\_DQ[65]

PIN\_C48 -to MEM0\_DQ[66]

PIN\_D47 -to MEM0\_DQ[67]

PIN\_C52 -to MEM0\_DQ[68]

PIN\_D51 -to MEM0\_DQ[69]

PIN\_B51 -to MEM0\_DQ[70]

PIN\_A52 -to MEM0\_DQ[71]

PIN\_F35 -to MEM0\_DQS[0]

PIN\_H35 -to MEM0\_DQS\_N[0]

PIN\_B35 -to MEM0\_DQS[1]

PIN\_D35 -to MEM0\_DQS\_N[1]

PIN\_A42 -to MEM0\_DQS[2]

PIN\_C42 -to MEM0\_DQS\_N[2]

PIN\_G42 -to MEM0\_DQS[3]

PIN\_J42 -to MEM0\_DQS\_N[3]

PIN\_F49 -to MEM0\_DQS[4]

PIN\_H49 -to MEM0\_DQS\_N[4]

PIN\_G56 -to MEM0\_DQS[5]

PIN\_J56 -to MEM0\_DQS\_N[5]

PIN\_A56 -to MEM0\_DQS[6]

PIN\_C56 -to MEM0\_DQS\_N[6]

PIN\_U56 -to MEM0\_DQS[7]

PIN\_W56 -to MEM0\_DQS\_N[7]

PIN\_B49 -to MEM0\_DQS[8]

PIN\_D49 -to MEM0\_DQS\_N[8]

PIN\_G36 -to MEM0\_DBI\_N[0]

PIN\_A36 -to MEM0\_DBI\_N[1]

PIN\_B43 -to MEM0\_DBI\_N[2]

PIN\_F43 -to MEM0\_DBI\_N[3]

PIN\_G50 -to MEM0\_DBI\_N[4]

PIN\_F57 -to MEM0\_DBI\_N[5]

PIN\_B57 -to MEM0\_DBI\_N[6]

PIN\_T57 -to MEM0\_DBI\_N[7]

PIN\_A50 -to MEM0\_DBI\_N[8]

PIN\_N38 -to MEM0\_PAR[0]

PIN\_P33 -to MEM0\_RESET\_N[0]

PIN\_M41 -to OCT\_RZQIN0

**FDAS External Memory Interface #2 for CONV/HSUM :**

**Connected to Banks 2A/2B (DDR I/F Channel 2)**

PIN\_CN38 -to PLL\_REF\_CLK\_2

PIN\_CH31 -to MEM2\_A[0]

PIN\_CF31 -to MEM2\_A[1]

PIN\_CG32 -to MEM2\_A[2]

PIN\_CE32 -to MEM2\_A[3]

PIN\_CH33 -to MEM2\_A[4]

PIN\_CF33 -to MEM2\_A[5]

PIN\_CG34 -to MEM2\_A[6]

PIN\_CE34 -to MEM2\_A[7]

PIN\_CH35 -to MEM2\_A[8]

PIN\_CF35 -to MEM2\_A[9]

PIN\_CG36 -to MEM2\_A[10]

PIN\_CE36 -to MEM2\_A[11]

PIN\_CK39 -to MEM2\_A[12]

PIN\_CN40 -to MEM2\_A[13]

PIN\_CL40 -to MEM2\_A[14]

PIN\_CM41 -to MEM2\_A[15]

PIN\_CK41 -to MEM2\_A[16]

PIN\_CL32 -to MEM2\_ACT\_N[0]

PIN\_CG42 -to MEM2\_ALERT\_N[0]

PIN\_CL42 -to MEM2\_BA[0]

PIN\_CM43 -to MEM2\_BA[1]

PIN\_CK43 -to MEM2\_BG[0]

PIN\_CM31 -to MEM2\_BG[1]

PIN\_CM35 -to MEM2\_CK[0]

PIN\_CK35 -to MEM2\_CK\_N[0]

PIN\_CN34 -to MEM2\_CKE[0]

PIN\_CN32 -to MEM2\_CS\_N[0]

PIN\_CM33 -to MEM2\_ODT[0]

PIN\_CE52 -to MEM2\_DQ[0]

PIN\_CF53 -to MEM2\_DQ[1]

PIN\_CG52 -to MEM2\_DQ[2]

PIN\_CH53 -to MEM2\_DQ[3]

PIN\_CE56 -to MEM2\_DQ[4]

PIN\_CG56 -to MEM2\_DQ[5]

PIN\_CF57 -to MEM2\_DQ[6]

PIN\_CH57 -to MEM2\_DQ[7]

PIN\_CR52 -to MEM2\_DQ[8]

PIN\_CT53 -to MEM2\_DQ[9]

PIN\_CU52 -to MEM2\_DQ[10]

PIN\_CV53 -to MEM2\_DQ[11]

PIN\_CR56 -to MEM2\_DQ[12]

PIN\_CU56 -to MEM2\_DQ[13]

PIN\_CT57 -to MEM2\_DQ[14]

PIN\_CV57 -to MEM2\_DQ[15]

PIN\_DA52 -to MEM2\_DQ[16]

PIN\_CY53 -to MEM2\_DQ[17]

PIN\_DB53 -to MEM2\_DQ[18]

PIN\_DC52 -to MEM2\_DQ[19]

PIN\_CY57 -to MEM2\_DQ[20]

PIN\_DB57 -to MEM2\_DQ[21]

PIN\_DA56 -to MEM2\_DQ[22]

PIN\_DC56 -to MEM2\_DQ[23]

PIN\_DA46 -to MEM2\_DQ[24]

PIN\_DC46 -to MEM2\_DQ[25]

PIN\_DB45 -to MEM2\_DQ[26]

PIN\_CY45 -to MEM2\_DQ[27]

PIN\_DC50 -to MEM2\_DQ[28]

PIN\_DA50 -to MEM2\_DQ[29]

PIN\_DB49 -to MEM2\_DQ[30]

PIN\_CY49 -to MEM2\_DQ[31]

PIN\_CT39 -to MEM2\_DQ[32]

PIN\_CV39 -to MEM2\_DQ[33]

PIN\_CU38 -to MEM2\_DQ[34]

PIN\_CR38 -to MEM2\_DQ[35]

PIN\_CU42 -to MEM2\_DQ[36]

PIN\_CV43 -to MEM2\_DQ[37]

PIN\_CR42 -to MEM2\_DQ[38]

PIN\_CT43 -to MEM2\_DQ[39]

PIN\_CY39 -to MEM2\_DQ[40]

PIN\_DB39 -to MEM2\_DQ[41]

PIN\_DC38 -to MEM2\_DQ[42]

PIN\_DA38 -to MEM2\_DQ[43]

PIN\_DC42 -to MEM2\_DQ[44]

PIN\_DB43 -to MEM2\_DQ[45]

PIN\_DA42 -to MEM2\_DQ[46]

PIN\_CY43 -to MEM2\_DQ[47]

PIN\_DA32 -to MEM2\_DQ[48]

PIN\_DC32 -to MEM2\_DQ[49]

PIN\_DB31 -to MEM2\_DQ[50]

PIN\_CY31 -to MEM2\_DQ[51]

PIN\_DA36 -to MEM2\_DQ[52]

PIN\_DC36 -to MEM2\_DQ[53]

PIN\_DB35 -to MEM2\_DQ[54]

PIN\_CY35 -to MEM2\_DQ[55]

PIN\_CR32 -to MEM2\_DQ[56]

PIN\_CU32 -to MEM2\_DQ[57]

PIN\_CV31 -to MEM2\_DQ[58]

PIN\_CT31 -to MEM2\_DQ[59]

PIN\_CV35 -to MEM2\_DQ[60]

PIN\_CU36 -to MEM2\_DQ[61]

PIN\_CT35 -to MEM2\_DQ[62]

PIN\_CR36 -to MEM2\_DQ[63]

PIN\_CU46 -to MEM2\_DQ[64]

PIN\_CT45 -to MEM2\_DQ[65]

PIN\_CR46 -to MEM2\_DQ[66]

PIN\_CV45 -to MEM2\_DQ[67]

PIN\_CT49 -to MEM2\_DQ[68]

PIN\_CU50 -to MEM2\_DQ[69]

PIN\_CV49 -to MEM2\_DQ[70]

PIN\_CR50 -to MEM2\_DQ[71]

PIN\_CG54 -to MEM2\_DQS[0]

PIN\_CE54 -to MEM2\_DQS\_N[0]

PIN\_CU54 -to MEM2\_DQS[1]

PIN\_CR54 -to MEM2\_DQS\_N[1]

PIN\_DC54 -to MEM2\_DQS[2]

PIN\_DA54 -to MEM2\_DQS\_N[2]

PIN\_DB47 -to MEM2\_DQS[3]

PIN\_CY47 -to MEM2\_DQS\_N[3]

PIN\_CU40 -to MEM2\_DQS[4]

PIN\_CR40 -to MEM2\_DQS\_N[4]

PIN\_DC40 -to MEM2\_DQS[5]

PIN\_DA40 -to MEM2\_DQS\_N[5]

PIN\_DB33 -to MEM2\_DQS[6]

PIN\_CY33 -to MEM2\_DQS\_N[6]

PIN\_CV33 -to MEM2\_DQS[7]

PIN\_CT33 -to MEM2\_DQS\_N[7]

PIN\_CV47 -to MEM2\_DQS[8]

PIN\_CT47 -to MEM2\_DQS\_N[8]

PIN\_CH55 -to MEM2\_DBI\_N[0]

PIN\_CV55 -to MEM2\_DBI\_N[1]

PIN\_DB55 -to MEM2\_DBI\_N[2]

PIN\_DC48 -to MEM2\_DBI\_N[3]

PIN\_CV41 -to MEM2\_DBI\_N[4]

PIN\_DB41 -to MEM2\_DBI\_N[5]

PIN\_DC34 -to MEM2\_DBI\_N[6]

PIN\_CU34 -to MEM2\_DBI\_N[7]

PIN\_CU48 -to MEM2\_DBI\_N[8]

PIN\_CL36 -to MEM2\_PAR[0]

PIN\_CK31 -to MEM2\_RESET\_N[0]

PIN\_CM39 -to OCT\_RZQIN2

**FDAS External Memory Interface #3 for CONV/HSUM :**

**Connected to Banks 2C/2D (DDR I/F Channel 3)**

PIN\_DC8 -to PLL\_REF\_CLK\_3

PIN\_CV15 -to MEM3\_A[0]

PIN\_CT15 -to MEM3\_A[1]

PIN\_CU14 -to MEM3\_A[2]

PIN\_CR14 -to MEM3\_A[3]

PIN\_CV13 -to MEM3\_A[4]

PIN\_CT13 -to MEM3\_A[5]

PIN\_CU12 -to MEM3\_A[6]

PIN\_CR12 -to MEM3\_A[7]

PIN\_CV11 -to MEM3\_A[8]

PIN\_CT11 -to MEM3\_A[9]

PIN\_CU10 -to MEM3\_A[10]

PIN\_CR10 -to MEM3\_A[11]

PIN\_CY7 -to MEM3\_A[12]

PIN\_DC6 -to MEM3\_A[13]

PIN\_DA6 -to MEM3\_A[14]

PIN\_DB5 -to MEM3\_A[15]

PIN\_CY5 -to MEM3\_A[16]

PIN\_DA14 -to MEM3\_ACT\_N[0]

PIN\_CU4 -to MEM3\_ALERT\_N[0]

PIN\_CY3 -to MEM3\_BA[0]

PIN\_CV1 -to MEM3\_BA[1]

PIN\_CT1 -to MEM3\_BG[0]

PIN\_DB15 -to MEM3\_BG[1]

PIN\_DB11 -to MEM3\_CK[0]

PIN\_CY11 -to MEM3\_CK\_N[0]

PIN\_DC12 -to MEM3\_CKE[0]

PIN\_DC14 -to MEM3\_CS\_N[0]

PIN\_DB13 -to MEM3\_ODT[0]

PIN\_CN28 -to MEM3\_DQ[0]

PIN\_CL28 -to MEM3\_DQ[1]

PIN\_CK29 -to MEM3\_DQ[2]

PIN\_CM29 -to MEM3\_DQ[3]

PIN\_CK25 -to MEM3\_DQ[4]

PIN\_CM25 -to MEM3\_DQ[5]

PIN\_CN24 -to MEM3\_DQ[6]

PIN\_CL24 -to MEM3\_DQ[7]

PIN\_CG28 -to MEM3\_DQ[8]

PIN\_CH29 -to MEM3\_DQ[9]

PIN\_CE28 -to MEM3\_DQ[10]

PIN\_CF29 -to MEM3\_DQ[11]

PIN\_CE24 -to MEM3\_DQ[12]

PIN\_CH25 -to MEM3\_DQ[13]

PIN\_CF25 -to MEM3\_DQ[14]

PIN\_CG24 -to MEM3\_DQ[15]

PIN\_CH21 -to MEM3\_DQ[16]

PIN\_CF21 -to MEM3\_DQ[17]

PIN\_CE22 -to MEM3\_DQ[18]

PIN\_CG22 -to MEM3\_DQ[19]

PIN\_CE18 -to MEM3\_DQ[20]

PIN\_CG18 -to MEM3\_DQ[21]

PIN\_CH17 -to MEM3\_DQ[22]

PIN\_CF17 -to MEM3\_DQ[23]

PIN\_DC28 -to MEM3\_DQ[24]

PIN\_DA28 -to MEM3\_DQ[25]

PIN\_CY29 -to MEM3\_DQ[26]

PIN\_DB29 -to MEM3\_DQ[27]

PIN\_CY25 -to MEM3\_DQ[28]

PIN\_DB25 -to MEM3\_DQ[29]

PIN\_DC24 -to MEM3\_DQ[30]

PIN\_DA24 -to MEM3\_DQ[31]

PIN\_CN14 -to MEM3\_DQ[32]

PIN\_CL14 -to MEM3\_DQ[33]

PIN\_CK15 -to MEM3\_DQ[34]

PIN\_CM15 -to MEM3\_DQ[35]

PIN\_CK11 -to MEM3\_DQ[36]

PIN\_CM11 -to MEM3\_DQ[37]

PIN\_CN10 -to MEM3\_DQ[38]

PIN\_CL10 -to MEM3\_DQ[39]

PIN\_CG14 -to MEM3\_DQ[40]

PIN\_CH15 -to MEM3\_DQ[41]

PIN\_CE14 -to MEM3\_DQ[42]

PIN\_CF15 -to MEM3\_DQ[43]

PIN\_CE10 -to MEM3\_DQ[44]

PIN\_CH11 -to MEM3\_DQ[45]

PIN\_CF11 -to MEM3\_DQ[46]

PIN\_CG10 -to MEM3\_DQ[47]

PIN\_CM7 -to MEM3\_DQ[48]

PIN\_CN8 -to MEM3\_DQ[49]

PIN\_CK7 -to MEM3\_DQ[50]

PIN\_CL8 -to MEM3\_DQ[51]

PIN\_CK3 -to MEM3\_DQ[52]

PIN\_CN4 -to MEM3\_DQ[53]

PIN\_CL4 -to MEM3\_DQ[54]

PIN\_CM3 -to MEM3\_DQ[55]

PIN\_CH7 -to MEM3\_DQ[56]

PIN\_CF7 -to MEM3\_DQ[57]

PIN\_CE8 -to MEM3\_DQ[58]

PIN\_CG8 -to MEM3\_DQ[59]

PIN\_CE4 -to MEM3\_DQ[60]

PIN\_CG4 -to MEM3\_DQ[61]

PIN\_CH3 -to MEM3\_DQ[62]

PIN\_CF3 -to MEM3\_DQ[63]

PIN\_CM21 -to MEM3\_DQ[64]

PIN\_CN22 -to MEM3\_DQ[65]

PIN\_CK21 -to MEM3\_DQ[66]

PIN\_CL22 -to MEM3\_DQ[67]

PIN\_CK17 -to MEM3\_DQ[68]

PIN\_CL18 -to MEM3\_DQ[69]

PIN\_CN18 -to MEM3\_DQ[70]

PIN\_CM17 -to MEM3\_DQ[71]

PIN\_CM27 -to MEM3\_DQS[0]

PIN\_CK27 -to MEM3\_DQS\_N[0]

PIN\_CH27 -to MEM3\_DQS[1]

PIN\_CF27 -to MEM3\_DQS\_N[1]

PIN\_CG20 -to MEM3\_DQS[2]

PIN\_CE20 -to MEM3\_DQS\_N[2]

PIN\_DB27 -to MEM3\_DQS[3]

PIN\_CY27 -to MEM3\_DQS\_N[3]

PIN\_CM13 -to MEM3\_DQS[4]

PIN\_CK13 -to MEM3\_DQS\_N[4]

PIN\_CH13 -to MEM3\_DQS[5]

PIN\_CF13 -to MEM3\_DQS\_N[5]

PIN\_CN6 -to MEM3\_DQS[6]

PIN\_CL6 -to MEM3\_DQS\_N[6]

PIN\_CG6 -to MEM3\_DQS[7]

PIN\_CE6 -to MEM3\_DQS\_N[7]

PIN\_CN20 -to MEM3\_DQS[8]

PIN\_CL20 -to MEM3\_DQS\_N[8]

PIN\_CN26 -to MEM3\_DBI\_N[0]

PIN\_CG26 -to MEM3\_DBI\_N[1]

PIN\_CH19 -to MEM3\_DBI\_N[2]

PIN\_DC26 -to MEM3\_DBI\_N[3]

PIN\_CN12 -to MEM3\_DBI\_N[4]

PIN\_CG12 -to MEM3\_DBI\_N[5]

PIN\_CM5 -to MEM3\_DBI\_N[6]

PIN\_CH5 -to MEM3\_DBI\_N[7]

PIN\_CM19 -to MEM3\_DBI\_N[8]

PIN\_DA10 -to MEM3\_PAR[0]

PIN\_CY15 -to MEM3\_RESET\_N[0]

PIN\_DB7 -to OCT\_RZQIN3

# FDAS DDR Controller Simulation

## Generation of DDR4 SDRAM Simulation Model

In order to simulate the FDAS\_DDR\_CONTROLLER/ FDAS\_DDR\_CONTROLLER\_HPS it is necessary to have a realistic simulation model of the External DDR SDRAM.

This can be generated by using pressing the “Create Example Design” button in the Intel Quartus Prime Platform Designer window for the FDAS\_DDR\_CONTROLLER/ FDAS\_DDR\_CONTROLLER\_HPS, ensuring that in the “Example Designs” tab that the simulation HDL format is set to VHDL. (The name can left as emif\_0\_example\_design)

This shall generate a set of components that can aid simulation, one of them being the simulation model for the external memory.

The design is written to a directory “emif\_0\_example\_design” in the location chosen for the project.

## Creating Simulation Compile Script

This description assumes that relevant files are copied to a “simulation area”.

The steps are:-

1. Copy the complete directory containing the “FDAS\_DDR\_CONTROLLER” / “FDAS\_DDR\_CONTROLLER\_HPS” and “FDAS\_EMIF\_CALIBRATION” directories generated by Platform Designer to the “simulation area”.
2. Copy the “ed\_sim\_mem” directory residing in the “emif\_0\_example\_design/sim/ip/ed\_sim” directory generated by Platform Designer to the “simulation area”.
3. Use the “msim\_setup.tcl” file from the directory “sim/mentor” within the complete “FDAS\_DDR\_CONTROLLER” / “FDAS\_DDR\_CONTROLLER\_HPS” directory, and the “msim\_setup.tcl” file from the directory “sim/mentor” within the “ed\_sim\_mem”directory to create a compile script for the simulation, for example “modelsim\_script\_ddrif2\_ddr\_controller\_ddr\_memory.tcl”
4. Launch Modelsim Questa and change the directory to the “simulation area”.
5. In the GUI type “source modelsim\_script\_ddrif2\_ddr\_controller\_ddr\_memory.tcl” to run the compile script.
6. Once compiled run the test bench using normal methods

# FDAS\_DDR\_CONTROLLER\_CALIBRATION Architecture for DDR Channels 2 and 3

The FDAS\_DDR\_CONTROLLER\_CALIBRATION VHDL Wrapper contains the FDAS\_DDR\_CONTROLLER and FDAS\_EMIF\_CALIBRATION Intel Agilex IP Blocks.

**FDAS\_DDR\_**

**CONTROLLER**

**Intel**

**Agilex IP**

**Block**

PLL\_REF\_CLK\_2\_I

LOCAL\_RESET\_REQ\_2\_I

LOCAL\_RESET\_DONE\_2\_O

LOCAL\_CAL\_SUCCESS\_2\_O

LOCAL\_CAL\_FAIL\_2\_O

EMIF\_USR\_CLK\_2\_O

EMIF\_USER\_RESET\_N\_2\_O

AMM\_READY\_2\_O

AMM\_READ\_2\_I

AMM\_WRITE\_2\_I

AMM\_ADDRESS\_2\_I[25:0]

AMM\_READDATA\_2\_O[511:0]

AMM\_WRITEDATA\_2\_I[511:0]

AMM\_BURSTCOUNT\_2\_I[6:0]

AMM\_BYTEENABLE\_2\_I[63:0]

AMM\_READDATAVALID\_2\_O

**FDAS\_DDR\_CONTROLLER\_CALIBRATION**

External Reference Clock 33.333MHz

pll\_ref\_clk

local\_reset\_req

local\_reset\_done

local\_cal\_success

local\_cal\_fail

emif\_usr\_clk

emif\_usr\_reset\_n

amm\_ready\_0

amm\_read\_0

amm\_write\_0

amm\_address\_0[25:0]

amm\_readdata\_0[511:0]

amm\_writedata\_0[511:0]

amm\_burstcount\_0[6:0]

amm\_byteenable\_0[63:0]

amm\_readdatavalid\_0

amm\_readdata\_0[575:512]

amm\_address\_0[26]

amm\_writedata\_0[575:512]

amm\_byteenable\_0[71:64]

mem\_ck

mem\_ck\_n

mem\_a[16:0]

mem\_act\_n

mem\_ba[1:0]

mem\_bg[1:0]

mem\_cke

mem\_cs\_n

mem\_odt

mem\_reset\_n

mem\_par

mem\_alert\_n

mem\_dqs[8:0]

mem\_dqs\_n[8:0]

mem\_dq[71:0]

mem\_dbi\_n

oct\_rzqin

MEM2\_CK\_O

MEM2\_CK\_N\_O

MEM2\_A\_O[16:0]

MEM2\_ACT\_N\_O

MEM2\_BA\_O[1:0]

MEM2\_BG\_O[1:0]

MEM2\_CKE\_O

MEM2\_CS\_N\_O

MEM2\_ODT\_O

MEM2\_RESET\_N\_O

MEM2\_PAR\_O

MEM2\_ALERT\_N\_I

MEM2\_DQS\_IO[8:0]

MEM2\_DQS\_N\_IO[8:0]

MEM2\_DQ\_IO[71:0]

MEM2\_DBI\_N\_IO

OCT\_RZQIN2\_I

External DDR4 SDRAM Interface

Internal Interface to

DDRIF2 module

Internal Interface to

MCI\_TOP module

calbus\_read

calbus\_write

calbus\_address[19:0]

calbus\_wdata[31:0]

calbus\_rdata[31:0

calbus\_seq\_param\_tbl[4095:0]

calbus\_clk

‘0’

**FDAS\_DDR\_**

**CONTROLLER**

**Intel**

**Agilex IP**

**Block**

PLL\_REF\_CLK\_3\_I

LOCAL\_RESET\_REQ\_3\_I

LOCAL\_RESET\_DONE\_3\_O

LOCAL\_CAL\_SUCCESS\_3\_O

LOCAL\_CAL\_FAIL\_3\_O

EMIF\_USR\_CLK\_3\_O

EMIF\_USER\_RESET\_N\_3\_O

AMM\_READY\_3\_O

AMM\_READ\_3\_I

AMM\_WRITE\_3\_I

AMM\_ADDRESS\_3\_I[25:0]

AMM\_READDATA\_3\_O[511:0]

AMM\_WRITEDATA\_3\_I[511:0]

AMM\_BURSTCOUNT\_3\_I[6:0]

AMM\_BYTEENABLE\_3\_I[63:0]

AMM\_READDATAVALID\_3\_O

pll\_ref\_clk

local\_reset\_req

local\_reset\_done

local\_cal\_success

local\_cal\_fail

emif\_usr\_clk

emif\_usr\_reset\_n

amm\_ready\_0

amm\_read\_0

amm\_write\_0

amm\_address\_0[25:0]

amm\_readdata\_0[511:0]

amm\_writedata\_0[511:0]

amm\_burstcount\_0[6:0]

amm\_byteenable\_0[63:0]

amm\_readdatavalid\_0

 amm\_readdata\_0[575:512]

amm\_address\_0[26]

amm\_writedata\_0[575:512]

amm\_byteenable\_0[71:64]

mem\_ck

mem\_ck\_n

mem\_a[16:0]

mem\_act\_n

mem\_ba[1:0]

mem\_bg[1:0]

mem\_cke

mem\_cs\_n

mem\_odt

mem\_reset\_n

mem\_par

mem\_alert\_n

mem\_dqs[8:0]

mem\_dqs\_n[8:0]

mem\_dq[71:0]

mem\_dbi\_n

oct\_rzqin

MEM3\_CK\_O

MEM3\_CK\_N\_O

MEM3\_A\_O[16:0]

MEM3\_ACT\_N\_O

MEM3\_BA\_O[1:0]

MEM3\_BG\_O[1:0]

MEM3\_CKE\_O

MEM3\_CS\_N\_O

MEM3\_ODT\_O

MEM3\_RESET\_N\_O

MEM3\_PAR\_O

MEM3\_ALERT\_N\_I

MEM3\_DQS\_IO[8:0]

MEM3\_DQS\_N\_IO[8:0]

MEM3\_DQ\_IO[71:0]

MEM3\_DBI\_N\_IO

OCT\_RZQIN3\_I

Internal Interface to

DDRIF2 module

Internal Interface to

MCI\_TOP module

calbus\_clk

calbus\_read

calbus\_write

calbus\_address[19:0]

calbus\_wdata[31:0]

calbus\_rdata[31:0

calbus\_seq\_param\_tbl[4095:0]

External Reference Clock 33.333MHz

External DDR4 SDRAM Interface

**FDAS\_EMIF\_**

**CALIBRATION**

**Intel Agilex**

**IP Block**

calbus\_read\_0

calbus\_write\_0

calbus\_address\_0[19:0]

calbus\_wdata\_0[31:0]

calbus\_rdata\_0[31:0

calbus\_seq\_param\_tbl\_0[4095:0]

calbus\_clk

calbus\_read\_1

calbus\_write\_1

calbus\_address\_1[19:0]

calbus\_wdata\_1[31:0]

calbus\_rdata\_1[31:0

calbus\_seq\_param\_tbl\_1[4095:0]

calbus\_clk\_1

‘0’s

‘0’s

‘0’

‘0’s

‘0’s

Figure ‑: FDAS\_DDR\_CONTROLLER\_CALIBRATION Wrapper

# FDAS\_DDR\_CONTROLLER\_CALIBRATION\_HPS Architecture for DDR Channels 0 and 1

The FDAS\_DDR\_CONTROLLER\_CALIBRATION\_HPS VHDL Wrapper contains the FDAS\_DDR\_CONTROLLER, FDAS\_DDR\_CONTROLLER\_HPS and FDAS\_EMIF\_CALIBRATION Intel Agilex IP Blocks.

**FDAS\_EMIF\_**

**CALIBRATION**

**Intel Agilex**

**IP Block**

**FDAS\_DDR\_**

**CONTROLLER**

**Intel**

**Agilex IP**

**Block**

PLL\_REF\_CLK\_0\_I

LOCAL\_RESET\_REQ\_0\_I

LOCAL\_RESET\_DONE\_0\_O

LOCAL\_CAL\_SUCCESS\_0\_O

LOCAL\_CAL\_FAIL\_0\_O

EMIF\_USR\_CLK\_0\_O

EMIF\_USER\_RESET\_N\_0\_O

AMM\_READY\_0\_O

AMM\_READ\_0\_I

AMM\_WRITE\_0\_I

AMM\_ADDRESS\_0\_I[25:0]

AMM\_READDATA\_0\_O[511:0]

AMM\_WRITEDATA\_0\_I[511:0]

AMM\_BURSTCOUNT\_0\_I[6:0]

AMM\_BYTEENABLE\_0\_I[63:0]

AMM\_READDATAVALID\_0\_O

**FDAS\_DDR\_CONTROLLER\_CALIBRATION\_HPS**

External Reference Clock 33.333MHz

pll\_ref\_clk

local\_reset\_req

local\_reset\_done

local\_cal\_success

local\_cal\_fail

emif\_usr\_clk

emif\_usr\_reset\_n

amm\_ready\_0

amm\_read\_0

amm\_write\_0

amm\_address\_0[25:0]

amm\_readdata\_0[511:0]

amm\_writedata\_0[511:0]

amm\_burstcount\_0[6:0]

amm\_byteenable\_0[63:0]

amm\_readdatavalid\_0

amm\_readdata\_0[575:512]

amm\_address\_0[26]

amm\_writedata\_0[575:512]

amm\_byteenable\_0[71:64]

mem\_ck

mem\_ck\_n

mem\_a[16:0]

mem\_act\_n

mem\_ba[1:0]

mem\_bg[1:0]

mem\_cke

mem\_cs\_n

mem\_odt

mem\_reset\_n

mem\_par

mem\_alert\_n

mem\_dqs[8:0]

mem\_dqs\_n[8:0]

mem\_dq[71:0]

mem\_dbi\_n

oct\_rzqin

MEM0\_CK\_O

MEM0\_CK\_N\_O

MEM0\_A\_O[16:0]

MEM0\_ACT\_N\_O

MEM0\_BA\_O[1:0]

MEM0\_BG\_O[1:0]

MEM0\_CKE\_O

MEM0\_CS\_N\_O

MEM0\_ODT\_O

MEM0\_RESET\_N\_O

MEM0\_PAR\_O

MEM0\_ALERT\_N\_I

MEM0\_DQS\_IO[8:0]

MEM0\_DQS\_N\_IO[8:0]

MEM0\_DQ\_IO[71:0]

MEM0\_DBI\_N\_IO

OCT\_RZQIN0\_I

External DDR4 SDRAM Interface

Internal Interface to

DDRIF2 module

Internal Interface to

MCI\_TOP module

calbus\_read\_0

calbus\_write\_0

calbus\_address\_0[19:0]

calbus\_wdata\_0[31:0]

calbus\_rdata\_0[31:0

calbus\_seq\_param\_tbl\_0[4095:0]

calbus\_clk

calbus\_read

calbus\_write

calbus\_address[19:0]

calbus\_wdata[31:0]

calbus\_rdata[31:0

calbus\_seq\_param\_tbl[4095:0]

calbus\_clk

calbus\_read\_1

calbus\_write\_1

calbus\_address\_1[19:0]

calbus\_wdata\_1[31:0]

calbus\_rdata\_1[31:0

calbus\_seq\_param\_tbl\_1[4095:0]

calbus\_clk\_1

**FDAS\_DDR\_**

**CONTROLLER\_HPS**

**Intel**

**Agilex IP**

**Block**

PLL\_REF\_CLK\_1\_I

LOCAL\_RESET\_REQ\_1\_I

LOCAL\_RESET\_DONE\_1\_O

LOCAL\_CAL\_SUCCESS\_1\_O

LOCAL\_CAL\_FAIL\_1\_O

EMIF\_USR\_CLK\_1\_O

EMIF\_USER\_RESET\_N\_1\_O

AMM\_READY\_1\_O

AMM\_READ\_1\_I

AMM\_WRITE\_1\_I

AMM\_ADDRESS\_1\_I[25:0]

AMM\_READDATA\_1\_O[511:0]

AMM\_WRITEDATA\_1\_I[511:0]

AMM\_BURSTCOUNT\_1\_I[6:0]

AMM\_BYTEENABLE\_1\_I[63:0]

AMM\_READDATAVALID\_1\_O

pll\_ref\_clk

local\_reset\_req

local\_reset\_done

local\_cal\_success

local\_cal\_fail

emif\_usr\_clk

emif\_usr\_reset\_n

amm\_ready\_0

amm\_read\_0

amm\_write\_0

amm\_address\_0[25:0]

amm\_readdata\_0[511:0]

amm\_writedata\_0[511:0]

amm\_burstcount\_0[6:0]

amm\_byteenable\_0[63:0]

amm\_readdatavalid\_0

amm\_address\_0[26]

mem\_ck

mem\_ck\_n

mem\_a[16:0]

mem\_act\_n

mem\_ba[1:0]

mem\_bg[1:0]

mem\_cke

mem\_cs\_n

mem\_odt

mem\_reset\_n

mem\_par

mem\_alert\_n

mem\_dqs[8:0]

mem\_dqs\_n[8:0]

mem\_dq[71:0]

mem\_dbi\_n

oct\_rzqin

MEM1\_CK\_O

MEM1\_CK\_N\_O

MEM1\_A\_O[16:0]

MEM1\_ACT\_N\_O

MEM1\_BA\_O[1:0]

MEM1\_BG\_O[1:0]

MEM1\_CKE\_O

MEM1\_CS\_N\_O

MEM1\_ODT\_O

MEM1\_RESET\_N\_O

MEM1\_PAR\_O

MEM1\_ALERT\_N\_I

MEM1\_DQS\_IO[8:0]

MEM1\_DQS\_N\_IO[8:0]

MEM1\_DQ\_IO[71:0]

MEM1\_DBI\_N\_IO

OCT\_RZQIN1\_I

Internal Interface to

DDRIF2 module

Internal Interface to

MCI\_TOP module

calbus\_ckk

calbus\_read

calbus\_write

calbu\_address[19:0]

calbus\_wdata[31:0]

calbus\_rdata[31:0

calbus\_seq\_param\_tbl[4095:0]

External Reference Clock 33.333MHz

External DDR4 SDRAM Interface

‘0’

‘0’s

‘0’s

‘0’

Figure ‑: FDAS\_DDR\_CONTROLLER\_CALIBRATION\_HPS Wrapper

# Design Requirement Tags

The relevant design tags from the FDAS Design Specification Document for the DDR\_CONTROLLER module are listed below.

| **Design Requirement Tag** | **Description** | **Comment** |
| --- | --- | --- |
| FDAS.DATAIN:040/A | The FFT sequence shall be stored by FDAS in external DDR SDRAM memory, with all values static for a known period of time. | The freq-bin samples from the PC/Computer via the PCIe shall be stored in External DDR SDRAM memory. |
| FDAS.DATAIN:080/A | The input data to FDAS (i.e. the observed data) shall be stored in external DDR SDRAM memory with the information shared equally across the available SDRAM devices. The **internal** FDAS data bus width shall be dependent on the number of external DDR SDRAM memory interfaces. A generic “ddr\_g” shall indicate the number of external DDR interfaces. | In this implementation with reduced complexity DDR interface only one External DDR SDRAM device shall be used to store the freq-bin samples, with a separate External DDR SDRAM device being used to store the FOP. |

Table ‑ : DDR Controller Design Requirement Tags

# Interface Specifications

## FDAS\_DDR\_CONTROLLER IP Component

| Signal | Direction | Clock Domain | Description |
| --- | --- | --- | --- |
| **Interface to DDRIF2** |  |  |  |
| amm\_ready\_0 | OUT | emif\_usr\_clk | Indication that the DDR Controller is ready. This is inverted when it is passed to the DDRIF2 module which uses the Avalon MM Wait\_Request signal. |
| amm\_write\_0 | IN | emif\_usr\_clk | Write Request from the DDRIF2 module. |
| amm\_read\_0 | IN | emif\_usr\_clk | Read Request from the DDRIF2 module. |
| amm\_address\_0[26:0] | IN | emif\_usr\_clk | DDR SDRAM Memory address from the DDRIF2 module.  Since each DDR SDRAM memory location contains a 64-byte word in this case only bits [31:6] of the address from the DDRIF2 module map to amm\_address\_0[25:0] .  Note that within the wrapper bit[26] of the address to the DDR Controller is set to 0 This is because the DDR Controller supports the 8GB SDRAM but FDAS only uses 4GB. |
| amm\_writedata\_0[575:0] | IN | emif\_usr\_clk | Write Data from the DDRIF2 module. Only bits [511:0] are used, hence bits [575:512] are set to 0. |
| amm\_burstcount\_0[6:0] | IN | emif\_usr\_clk | This is set to “0000001” by DDRIF2 as the DDRIF2 module terminates the data bursts. |
| amm\_byteenable\_0[71:0] | IN | emif\_usr\_clk | Bits[63:0] are the Byte Enables for amm\_writedata\_0[511:0] .  Bits[71:64] are set to ‘0 as they are unused. |
| amm\_readdata\_0[575:0] | OUT | emif\_usr\_clk | Read Data to the DDRIF2 module. Only bits [511:0] are used. |
| amm\_readdatavalid\_0 | OUT | emif\_usr\_clk | Read Data Valid indication to the DDRIF2 module. |
|  |  |  |  |
| **Interface to External SDRAM** |  |  |  |
| mem\_ck | OUT | - | Clock (True) to External SDRAM. 1200.0MHz in this application. |
| mem\_ck\_n | OUT | - | Clock (Compliment) to External SDRAM. 1200.0MHz in this application. |
| mem\_a[16:0] | OUT | mem\_ck | Row Address for ACTIVATE commands/ Col Address for READ/WRITE Commands to External DDR4 SDRAM UDIMM.  Dual Use  A[10]: Auto Precharge  A[12]: Burst Chop  A[14]: WE Command  A[15]: CAS Command  A[16]: RAS Command |
| mem\_act\_n | OUT | mem\_ck | ACTIVATE Command to External DDR4 SDRAM UDIMM. |
| mem\_ba[1:0] | OUT | mem\_ck | Bank within the Bank Group to which REFRESH, ACTIVATE, READ or WRITE command is being applied. Connection to External DDR4 SDRAM UDIMM. |
| mem\_bg[1:0] | OUT | mem\_ck | Bank Group to which REFRESH, ACTIVATE, READ or WRITE command is being applied. Connection to External DDR4 SDRAM UDIMM. |
| mem\_cke | OUT | mem\_ck | Clock Enable to External DDR4 SDRAM UDIMM. |
| mem\_cs\_n | OUT | mem\_ck | Chip Select to External DDR4 SDRAM UDIMM. |
| mem\_odt | OUT | mem\_ck | On Die Termination. |
| mem\_reset\_n | OUT | mem\_ck | Reset (Active Low) to the External DDR4 SDRAM UDIMM. |
| mem\_par | OUT | mem\_ck | Parity for Command and Address to the External DDR4 SDRAM UDIMM. |
| mem\_alert\_n | IN | mem\_ck | ALERT from the DDR4 SDRAM UDIMM to the DDR Controller. |
| mem\_dqs[8:0] | IN/OUT | mem\_ck | Data Strobe (True) to External DDR4 SDRAM UDIMM. Output with READ data, Input with WRITE data.  Strobe per Byte, with a Byte per Micron Device. |
| mem\_dqs\_n[8:0] | IN/OUT | mem\_ck | Data Strobe (Compliment) to External DDR4 SDRAM UDIMM. Output with READ data, Input with WRITE data.  Strobe per Byte, with a Byte per Micron Device. |
| mem\_dq[71:0] | IN/OUT | mem\_ck | Data Input/Output to External DDR4 SDRAM UDIMM. |
| mem\_dbi\_n[8:0] | IN/OUT | mem\_ck | Data Bus Inversion to External DDR4 SDRAM UDIMM. |
| oct\_rzqin | IN | mem\_ck | Reference for ZQ calibration from External DDR4 SDRAM UDIMM. |
|  |  |  |  |
| **Indication Signals** |  |  |  |
| local\_cal\_success | IN | mem\_ck | External DDR4 SDRAM UDIMM is successful. |
| local\_cal\_fail | IN | mem\_ck | External DDR4 SDRAM UDIMM has failed. |
|  |  |  |  |
|  |  |  |  |
| **Global Clock/Resets** |  |  |  |
| emif\_usr\_clk | OUT | - | This is the CLK\_DDR generated by the DDR\_CONTROLLER to be used by the DDRIF2 module.  It shall be 333.333MHz in this application. |
| emif\_usr\_reset\_n | OUT | CLK\_DDR | Reset (active low) generated by the DDR\_CONTROLLER for the DDRIF2 module. |
| local\_reset\_req | IN | - | Signal from user logic to request the memory interface to be reset and recalibrated. Reset request is sent by transitioning the local\_reset\_req signal from low to high, then keeping the signal at the high state for a minimum of 2 EMIF core clock cycles, then transitioning the signal from high to low. local\_reset\_req is asynchronous in that there is no setup/hold timing to meet, but it must meet the minimum pulse width requirement of 2 EMIF core clock cycles. |
| local\_reset\_done | OUT | - | Signal from memory interface to indicate whether it has completed a reset sequence, is currently out of reset, and is ready for a new reset request. When local\_reset\_done is low, the memory interface is in reset. |
| pll\_ref\_clk | IN | - | PLL Reference Clock into the DDR\_CONTROLLER. (33.33MHz) |
|  |  |  |  |
| **Calibration Interface** |  |  |  |
| calbus\_read | IN | calbus\_clk | Calibration bus Read control from FDAS\_EMIF\_CALIBRATION IP Component |
| calbus\_write | IN | calbus\_clk | Calibration bus Write control from FDAS\_EMIF\_CALIBRATION IP Component |
| calbus\_address[19:0] | IN | calbus\_clk | Calibration bus Address from FDAS\_EMIF\_CALIBRATION IP Component |
| calbus\_wdata[31:0] | IN | calbus\_clk | Calibration bus Write Data from FDAS\_EMIF\_CALIBRATION IP Component |
| calbus\_rdata[31:0] | OUT | calbus\_clk | Calibration bus Read Data to FDAS\_EMIF\_CALIBRATION IP Component |
| calbus\_seq\_param\_tbl[4094:0] | OUT | calbus\_clk | Calibration bus Parameter Table to FDAS\_EMIF\_CALIBRATION IP Component |
| calbus\_clk | IN | - | Calibration bus clock |

Table ‑ : FDAS\_DDR\_CONTROLLER IP Component Pinout

## FDAS\_DDR\_CONTROLLER\_HPS IP Component

| Signal | Direction | Clock Domain | Description |
| --- | --- | --- | --- |
| **Interface to DDRIF2** |  |  |  |
| amm\_ready\_0 | OUT | emif\_usr\_clk | Indication that the DDR Controller is ready. This is inverted when it is passed to the DDRIF2 module which uses the Avalon MM Wait\_Request signal. |
| amm\_write\_0 | IN | emif\_usr\_clk | Write Request from the DDRIF2 module. |
| amm\_read\_0 | IN | emif\_usr\_clk | Read Request from the DDRIF2 module. |
| amm\_address\_0[26:0] | IN | emif\_usr\_clk | DDR SDRAM Memory address from the DDRIF2 module.  Since each DDR SDRAM memory location contains a 64-byte word in this case only bits [31:6] of the address from the DDRIF2 module map to amm\_address\_0[25:0] .  Note that within the wrapper bit[26] of the address to the DDR Controller is set to 0 This is because the DDR Controller supports the 8GB SDRAM but FDAS only uses 4GB. |
| amm\_writedata\_0[511:0] | IN | emif\_usr\_clk | Write Data from the DDRIF2 module. |
| amm\_burstcount\_0[6:0] | IN | emif\_usr\_clk | This is set to “0000001” by DDRIF2 as the DDRIF2 module terminates the data bursts. |
| amm\_byteenable\_0[63:0] | IN | emif\_usr\_clk | Bits[63:0] are the Byte Enables for amm\_writedata\_0[511:0]. |
| amm\_readdata\_0[511:0] | OUT | emif\_usr\_clk | Read Data to the DDRIF2 module. |
| amm\_readdatavalid\_0 | OUT | emif\_usr\_clk | Read Data Valid indication to the DDRIF2 module. |
|  |  |  |  |
| **Interface to External SDRAM** |  |  |  |
| mem\_ck | OUT | - | Clock (True) to External SDRAM. 1200.0MHz in this application. |
| mem\_ck\_n | OUT | - | Clock (Compliment) to External SDRAM. 1200.0MHz in this application. |
| mem\_a[16:0] | OUT | mem\_ck | Row Address for ACTIVATE commands/ Col Address for READ/WRITE Commands to External DDR4 SDRAM UDIMM.  Dual Use  A[10]: Auto Precharge  A[12]: Burst Chop  A[14]: WE Command  A[15]: CAS Command  A[16]: RAS Command |
| mem\_act\_n | OUT | mem\_ck | ACTIVATE Command to External DDR4 SDRAM UDIMM. |
| mem\_ba[1:0] | OUT | mem\_ck | Bank within the Bank Group to which REFRESH, ACTIVATE, READ or WRITE command is being applied. Connection to External DDR4 SDRAM UDIMM. |
| mem\_bg[1:0] | OUT | mem\_ck | Bank Group to which REFRESH, ACTIVATE, READ or WRITE command is being applied. Connection to External DDR4 SDRAM UDIMM. |
| mem\_cke | OUT | mem\_ck | Clock Enable to External DDR4 SDRAM UDIMM. |
| mem\_cs\_n | OUT | mem\_ck | Chip Select to External DDR4 SDRAM UDIMM. |
| mem\_odt | OUT | mem\_ck | On Die Termination. |
| mem\_reset\_n | OUT | mem\_ck | Reset (Active Low) to the External DDR4 SDRAM UDIMM. |
| mem\_par | OUT | mem\_ck | Parity for Command and Address to the External DDR4 SDRAM UDIMM. |
| mem\_alert\_n | IN | mem\_ck | ALERT from the DDR4 SDRAM UDIMM to the DDR Controller. |
| mem\_dqs[8:0] | IN/OUT | mem\_ck | Data Strobe (True) to External DDR4 SDRAM UDIMM. Output with READ data, Input with WRITE data.  Strobe per Byte, with a Byte per Micron Device. |
| mem\_dqs\_n[8:0] | IN/OUT | mem\_ck | Data Strobe (Compliment) to External DDR4 SDRAM UDIMM. Output with READ data, Input with WRITE data.  Strobe per Byte, with a Byte per Micron Device. |
| mem\_dq[71:0] | IN/OUT | mem\_ck | Data Input/Output to External DDR4 SDRAM UDIMM. |
| mem\_dbi\_n[8:0] | IN/OUT | mem\_ck | Data Bus Inversion to External DDR4 SDRAM UDIMM. |
| oct\_rzqin | IN | mem\_ck | Reference for ZQ calibration from External DDR4 SDRAM UDIMM. |
|  |  |  |  |
| **Indication Signals** |  |  |  |
| local\_cal\_success | IN | mem\_ck | External DDR4 SDRAM UDIMM is successful. |
| local\_cal\_fail | IN | mem\_ck | External DDR4 SDRAM UDIMM has failed. |
|  |  |  |  |
|  |  |  |  |
| **Global Clock/Resets** |  |  |  |
| emif\_usr\_clk | OUT | - | This is the CLK\_DDR generated by the DDR\_CONTROLLER to be used by the DDRIF2 module.  It shall be 333.333MHz in this application. |
| emif\_usr\_reset\_n | OUT | CLK\_DDR | Reset (active low) generated by the DDR\_CONTROLLER for the DDRIF2 module. |
| local\_reset\_req | IN | - | Signal from user logic to request the memory interface to be reset and recalibrated. Reset request is sent by transitioning the local\_reset\_req signal from low to high, then keeping the signal at the high state for a minimum of 2 EMIF core clock cycles, then transitioning the signal from high to low. local\_reset\_req is asynchronous in that there is no setup/hold timing to meet, but it must meet the minimum pulse width requirement of 2 EMIF core clock cycles. |
| local\_reset\_done | OUT | - | Signal from memory interface to indicate whether it has completed a reset sequence, is currently out of reset, and is ready for a new reset request. When local\_reset\_done is low, the memory interface is in reset. |
| pll\_ref\_clk | IN | - | PLL Reference Clock into the DDR\_CONTROLLER. (33.33MHz) |
|  |  |  |  |
| **Calibration Interface** |  |  |  |
| calbus\_read | IN | calbus\_clk | Calibration bus Read control from FDAS\_EMIF\_CALIBRATION IP Component |
| calbus\_write | IN | calbus\_clk | Calibration bus Write control from FDAS\_EMIF\_CALIBRATION IP Component |
| calbus\_address[19:0] | IN | calbus\_clk | Calibration bus Address from FDAS\_EMIF\_CALIBRATION IP Component |
| calbus\_wdata[31:0] | IN | calbus\_clk | Calibration bus Write Data from FDAS\_EMIF\_CALIBRATION IP Component |
| calbus\_rdata[31:0] | OUT | calbus\_clk | Calibration bus Read Data to FDAS\_EMIF\_CALIBRATION IP Component |
| calbus\_seq\_param\_tbl[4094:0] | OUT | calbus\_clk | Calibration bus Parameter Table to FDAS\_EMIF\_CALIBRATION IP Component |
| calbus\_clk | IN | - | Calibration bus clock |

Table ‑ : FDAS\_DDR\_CONTROLLER\_HPS IP Component Pinout

## FDAS\_EMIF\_CALIBRATION IP Component

| Signal | Direction | Clock Domain | Description |
| --- | --- | --- | --- |
| **Calibration Interface** |  |  |  |
| calbus\_read\_0 | OUT | calbus\_clk | Calibration bus Read control to FDAS\_DDR\_CONTROLLER IP Component |
| calbus\_write\_0 | OUT | calbus\_clk | Calibration bus Write control to FDAS\_DDR\_CONTROLLER IP Component |
| calbus\_address\_0[19:0] | OUT | calbus\_clk | Calibration bus Address to FDAS\_DDR\_CONTROLLER IP Component |
| calbus\_wdata\_0[31:0] | OUT | calbus\_clk | Calibration bus Write Data to FDAS\_DDR\_CONTROLLER IP Component |
| calbus\_rdata\_0[31:0] | IN | calbus\_clk | Calibration bus Read Data from FDAS\_DDR\_CONTROLLER IP Component |
| calbus\_seq\_param\_tbl\_0[4094:0] | IN | calbus\_clk | Calibration bus Parameter from FDAS\_DDR\_CONTROLLER IP Component |
| calbus\_clk\_0 | OUT | - | Calibration bus clock |

Table ‑ : FDAS\_EMIF\_CALIBRATION IP Component Pinout

# MCI Memory Mapped Interface

The FDAS\_DDR\_CONTROLLER\_CALIBRATION and FDAS\_DDR\_CONTROLLER\_CALIBRATION\_HPS modules do not have a memory mapped interface.

# Design Parameterisation

The FDAS\_DDR\_CONTROLLER\_CALIBRATION and FDAS\_DDR\_CONTROLLER\_CALIBRATION\_HPS modules do not have any generic parameterisation.

# References

|  |  |  |
| --- | --- | --- |
| **Bookmark** | **Reference** | **Description** |
| [Ref: Agilex DDR User Guide] | External Memory Interfaces Intel Agilex FPGA IP User Guide UG-20218 2021.07.09 | Intel DDR interface User Guide for the Agilex FPGA family. |
| [Ref: Agilex Development Board] | AgilexF\_FPGA\_DK\_2V\_ES.pdf containing:-  AgileX F-Series FPGA Dev Kit\_Enpirion schematics  Document Number: K57065-001-A  Date: Thursday, May 07, 2020 | Intel Agilex F Development Board schematics. This board is fitted with an Agilex AGFB014R24A2E2VR0 FPGA. The board supports a PCIe interface and four DDR4 SDRAM interfaces. |

# Abbreviations and Acronyms

|  |  |
| --- | --- |
| DMA | Direct Memory Access |
| DDR | Double Data Rate |
| FDAS | Fourier Domain Acceleration Search |
| FFT | Fast Fourier Transform |
| FOP | Filter Output Plane |
| FPGA | Field Programmable Gate Array |
| IEEE | Institute of Electrical Engineers |
| HPS | Hard Processor Sub-System |
| IP | Intellectual Property |
| MC | Micro Controller Interface |
| MSI-X | Extended Message Signalled Interrupt |
| PCIe | Peripheral Component Interconnect Express |
| SDRAM | Synchronous Dynamic RAM |
| TLP | Transaction Layer Packet |