# Design Exercise 1

IECE420/520/ICSI522: Introduction to VLSI

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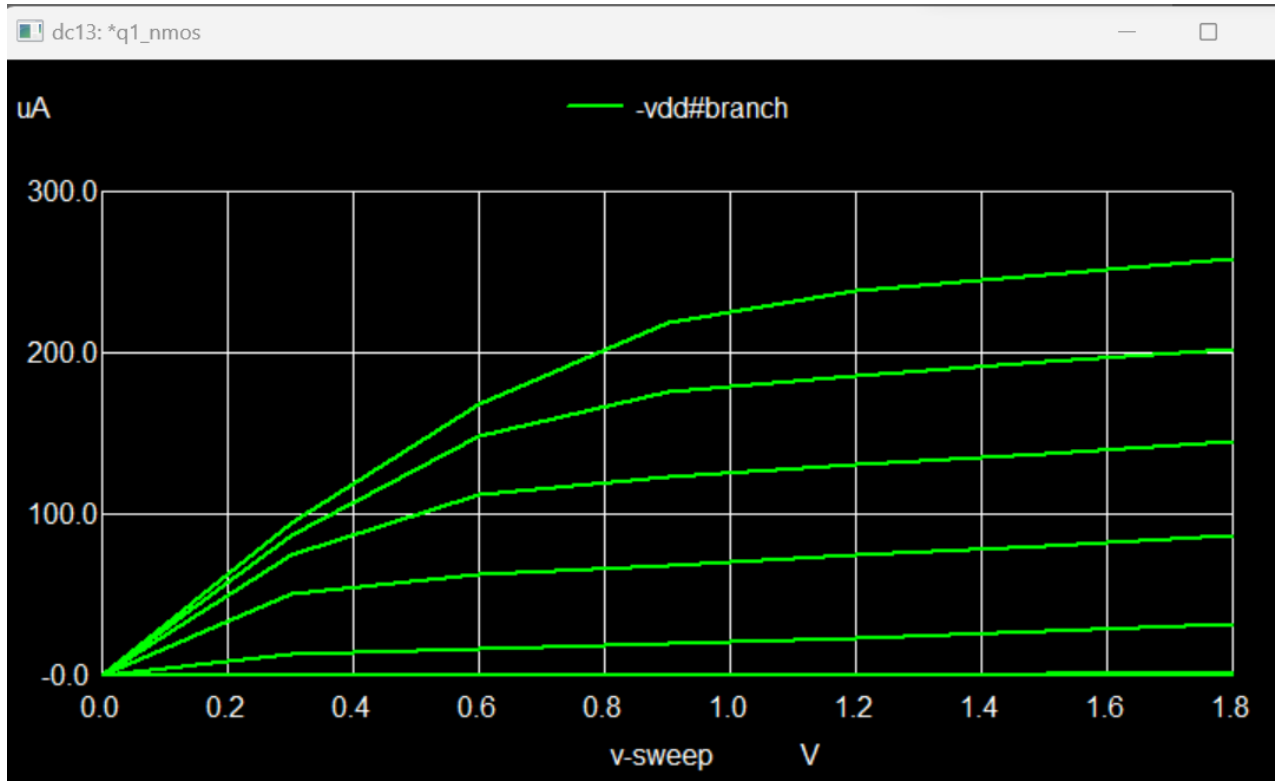
## Questions (1 hr 10 min)

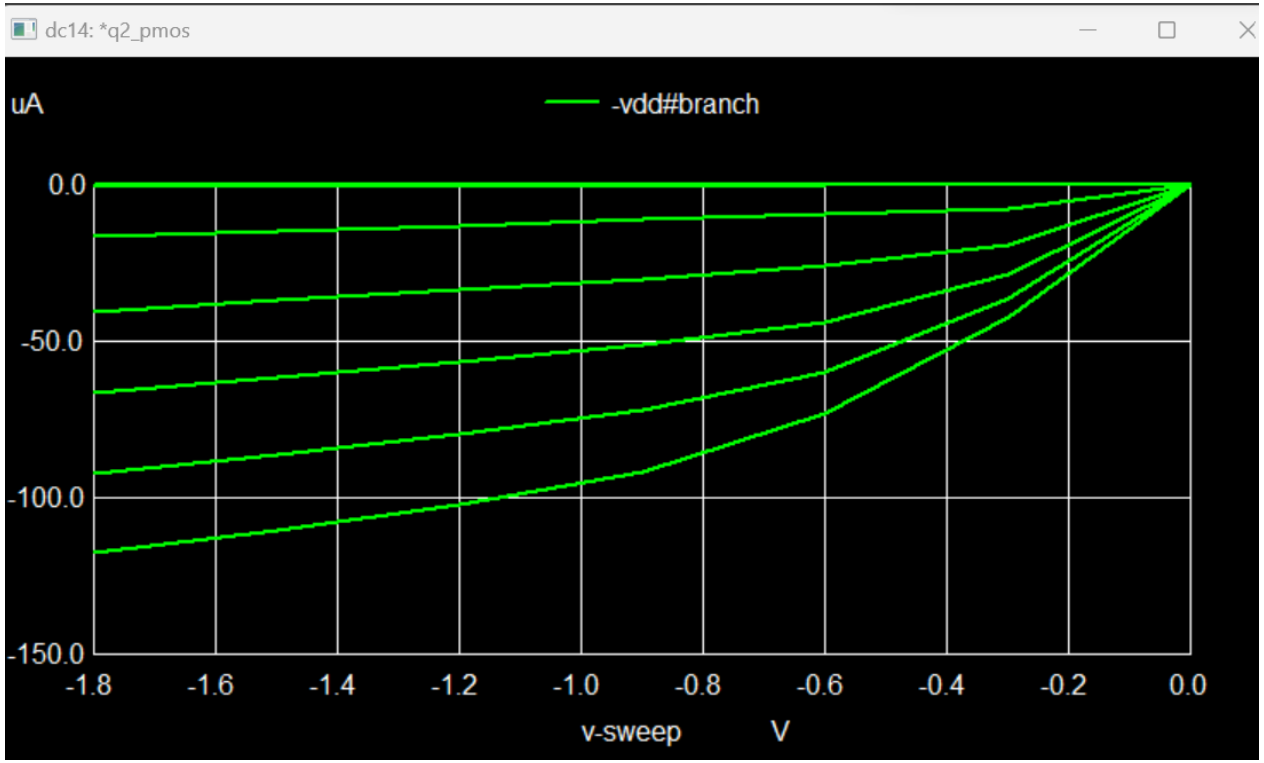
$2\lambda = 0.18\mu$, $L_{min} = 2\lambda$, $W_{min} = 4\lambda$

1. Simulate the I-V characteristics of a minimum sized NMOS transistor for $V_{GS}$ = 0 : *0.3V* : 1.8V (1 pt)



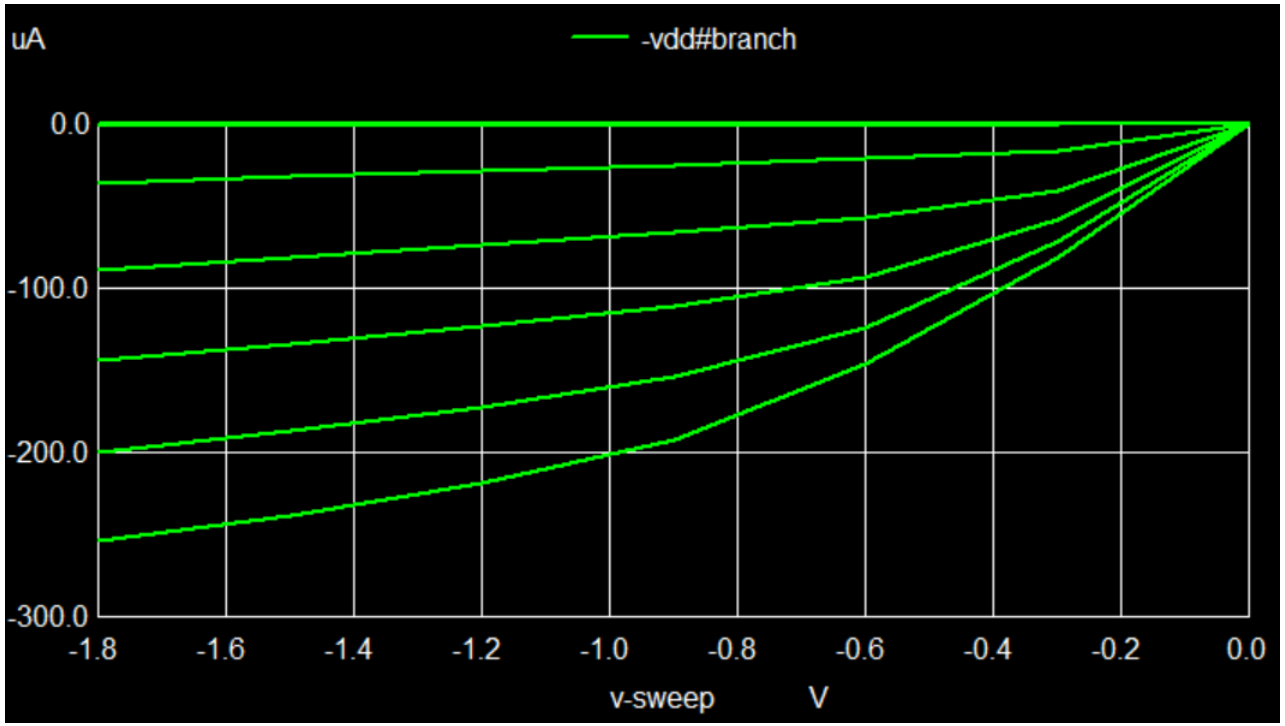

```
*Q1_NMOS
.include bsim.lib
VDD vd 0 DC 1.8
RD vd vout 1k
VG vin 0 DC 1.8
M1 vout vin 0 0 BSIM3_180nm_N W=0.36u L=0.18u

.dc VDD 0 1.8 0.3 VG 0 1.8 0.3
.control
run
plot -VDD#BRANCH
.endc
.end
```

2. Simulate the I-V characteristics of a minimum sized PMOS transistor for $V_{GS}$ = 0 : *0.3V* : 1.8V (1pt)



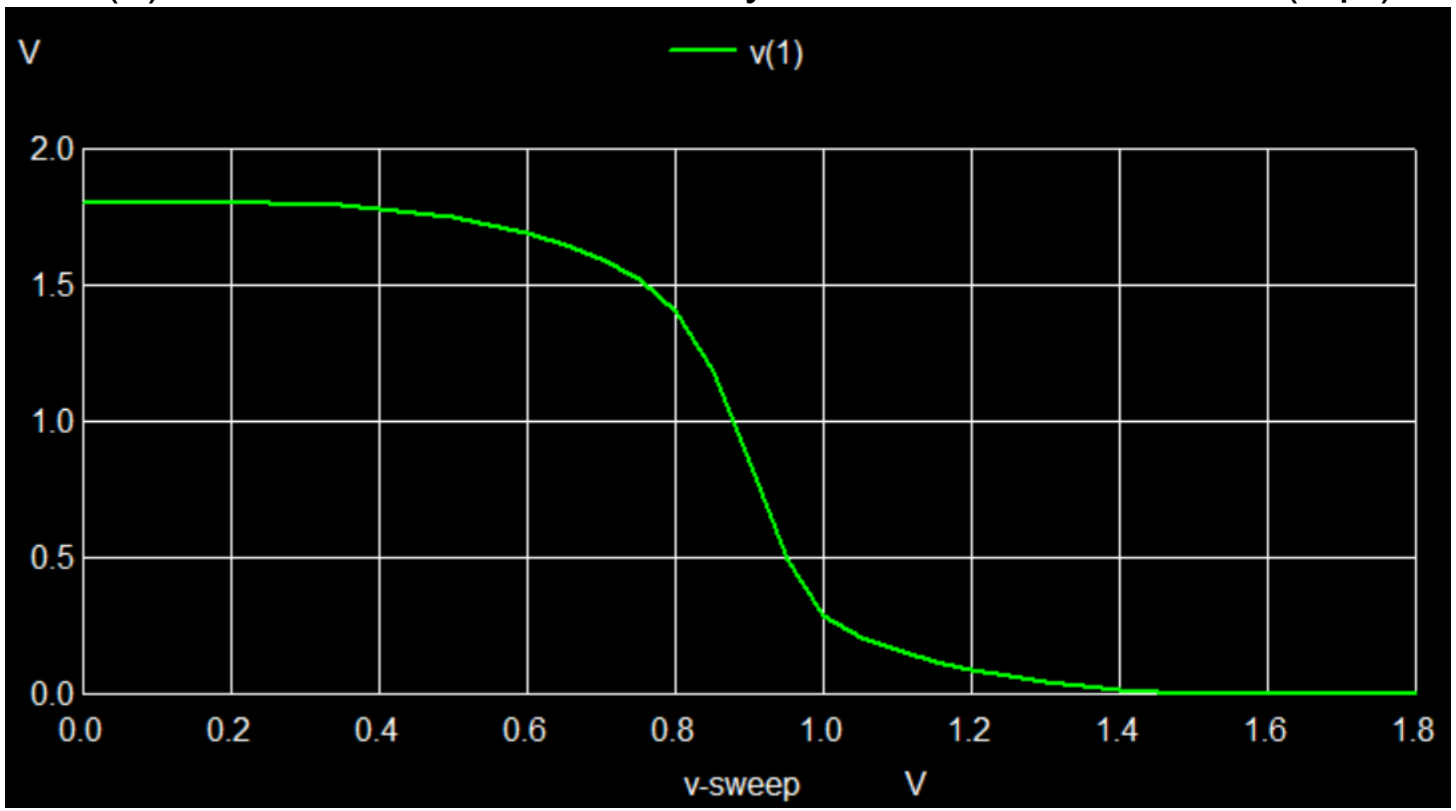

```
*Q2_PMOS
.include bsim.lib
VDD vd 0 DC -3
RD vd vout 1k
VG vin 0 DC -1.8
M1 vout vin 0 0 BSIM3_180nm_P W=0.36u L=0.18
.dc VDD -3 0 0.1 VG -1.8 0 0.3
.control
run
plot -VDD#BRANCH
.endc
.end
```

3. Size the PMOS so the I-V characteristics match that of minimum sized NMOS (1pt)



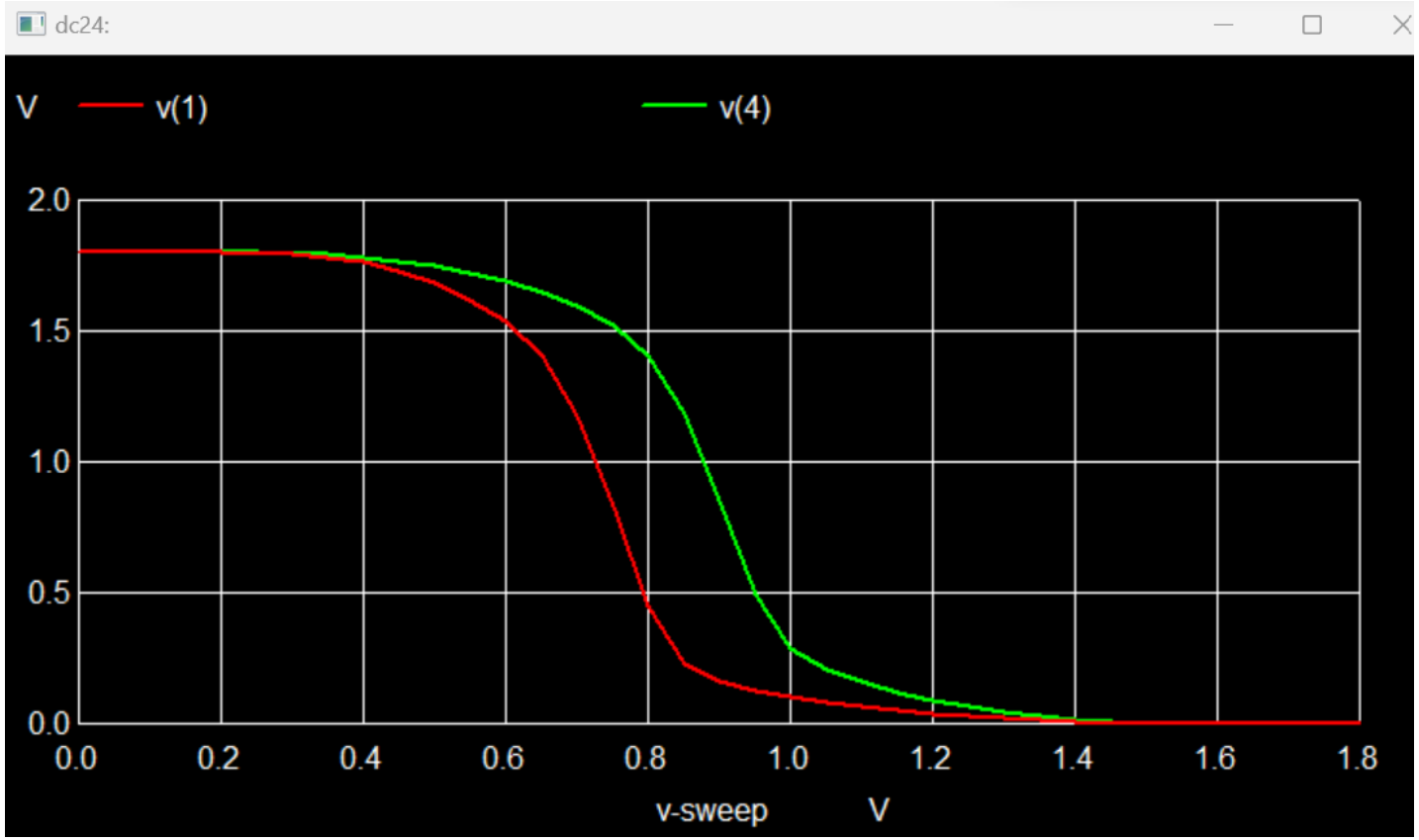

```
*Q3_PMOS
.include bsim.lib
VDD vd 0 DC -1.8
RD vd vout 1k
VG vin 0 DC -1.8
M1 vout vin 0 0 BSIM3_180nm_P W=0.8u L=0.18u
.dc VDD -1.8 0 0.3 VG -1.8 0 0.3
.control
run
plot -VDD#BRANCH
.endc
.end
```

4. Use (3) to simulate the VTC for a symmetric CMOS inverter (2 pt)




```
.include bsim.lib
vdd 3 0 DC 1.8
vin 2 0 DC 0
M1 1 2 3 3 BSIM3_180nm_P W=0.8u L=0.18u
M2 1 2 0 0 BSIM3_180nm_N W=0.36u L=0.18u
.dc vin 0 1.8 0.05
*vdd 0 1.8 0.6
.control
run
plot v(1)
.endc
.end
```

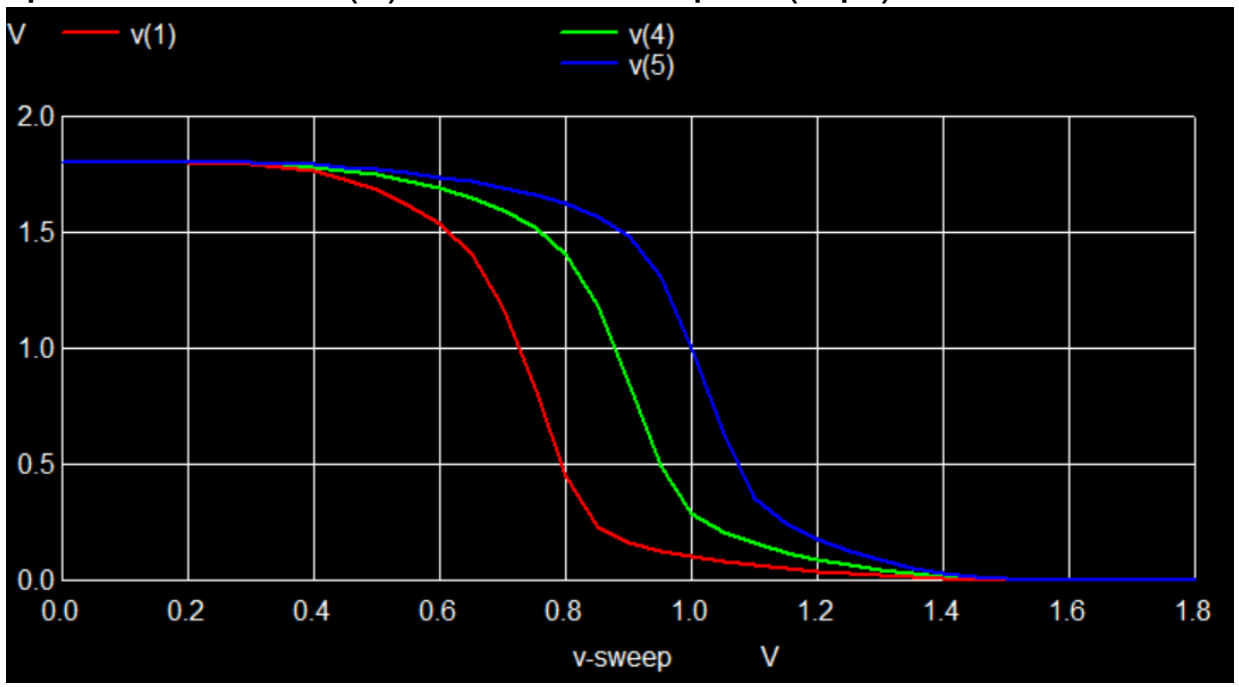
5. 5xx: Use minimum size for both NMOS and PMOS and compare VTC with (4) on the same plot (1 pt)




```
.include bsim.lib
vdd 3 0 DC 1.8
vin 2 0 DC 0
M1 1 2 3 3 BSIM3_180nm_P W=0.36u L=0.18u
M2 1 2 0 0 BSIM3_180nm_N W=0.36u L=0.18u

M3 4 2 3 3 BSIM3_180nm_P W=0.8u L=0.18u
M4 4 2 0 0 BSIM3_180nm_N W=0.36u L=0.18u


.dc vin 0 1.8 0.05
*vdd 0 1.8 0.6
.control
run
plot v(4) v(1)
.endc
.end
```

Green is Symmetric CMOS , Red is CMOS using Minimum size. Skewed towards the NMOS for minimum size

6. 5xx extra credit (not for 4xx): Use minimum size for NMOS and 4 times the minimum size for PMOS and compare VTC with (4) on the same plot (1 pt)




```
.include bsim.lib
vdd 3 0 DC 1.8
vin 2 0 DC 0
M1 1 2 3 3 BSIM3_180nm_P W=0.36u L=0.18u
M2 1 2 0 0 BSIM3_180nm_N W=0.36u L=0.18u

M3 4 2 3 3 BSIM3_180nm_P W=0.8u L=0.18u
M4 4 2 0 0 BSIM3_180nm_N W=0.36u L=0.18u

M5 5 2 3 3 BSIM3_180nm_P W=1.44u L=0.18u
M6 5 2 0 0 BSIM3_180nm_N W=0.36u L=0.18u


.dc vin 0 1.8 0.05
*vdd 0 1.8 0.6
.control
run
plot v(4) v(1) v(5)
.endc
.end
```

Red is minimum size
Green is symmetric CMOS
Blue is CMOS with PMOS sized six times. (skewed more towards the PMOS)