Design Exercise 2

IECE420/520/ICSI522: Introduction to VLSI

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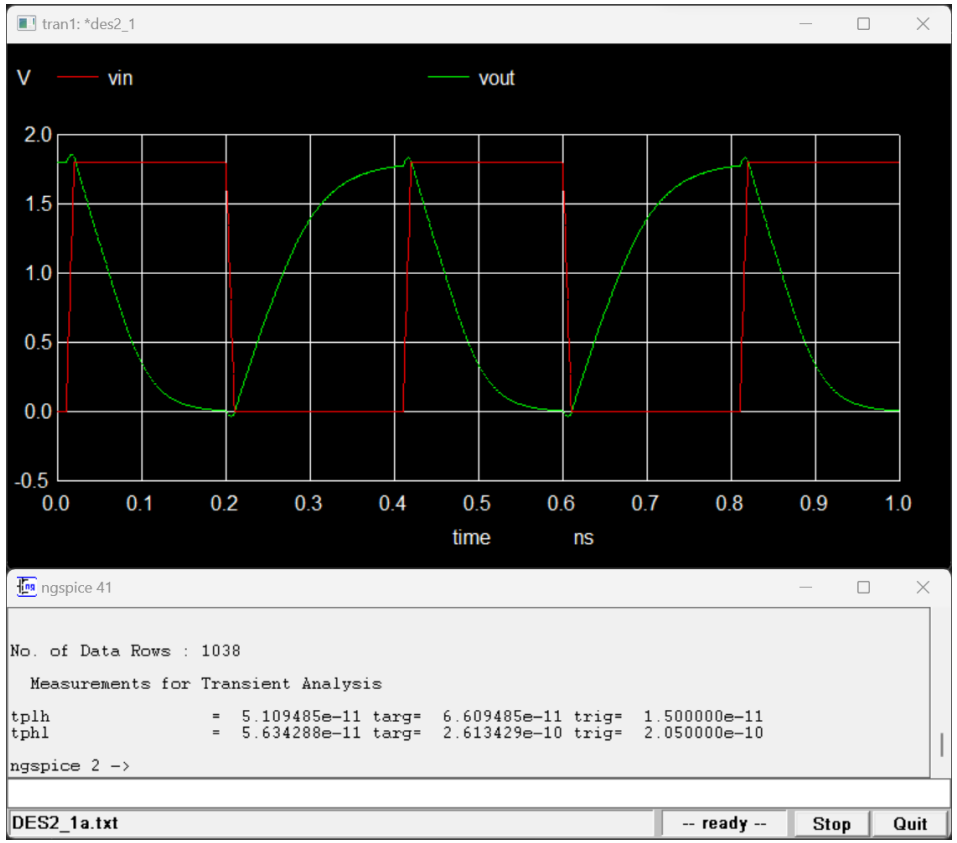
Questions (1 hr)

$2\lambda = 0.18\mu$, $L_{min} = 2\lambda$, $W_{min} = 4\lambda$

1. Let α be the upsizing factor on the unit inverter with a load of *15 fF*. Simulate and find α for

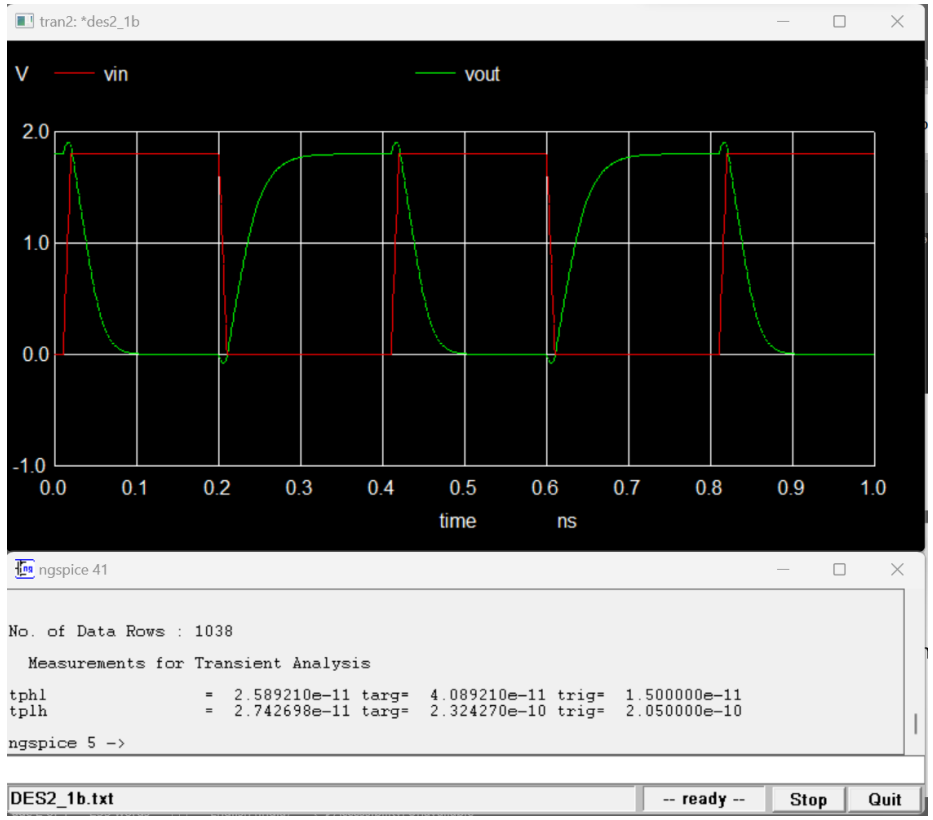
   a) $tp_{LH} = tp_{HL} = 50\ ps$ (1 point)




```
*DES2_1
.include bsim.lib

.param alpha = 1.4

VDD vd 0 DC 1.8
VG vin 0 pulse(0 1.8 10p 10p 10p 180p 400p)
Cload vout 0 15F

M1 vout vin 0 0 BSIM3_180nm_N W = '0.36u*alpha' L = 0.18u
M2 vout vin vd vd BSIM3_180nm_P W = '0.72u*alpha' L = 0.18u

.tran 1p 1000p

.measure tran tplh trig v(vin) val=0.9 rise=1 targ v(vout) val=0.9 fall=1
.measure tran tphl trig v(vin) val=0.9 fall=1 targ v(vout) val=0.9 rise=1

.control
run
plot vout vin
.endc

.end
```

α = 1.4

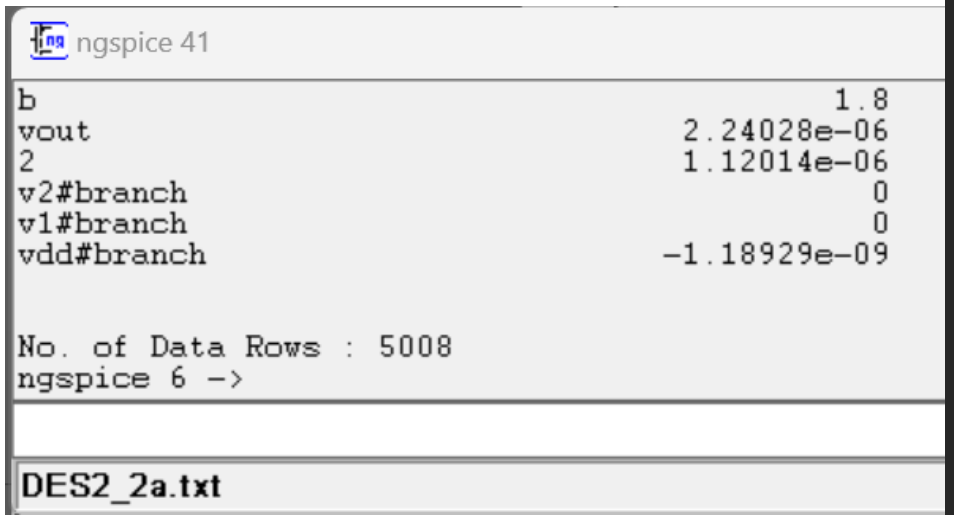
b) $tp_{LH} = tp_{HL} = 25\ ps$ (1 point)




```
*DES2_1b
.include bsim.lib

.param alpha = 4

VDD vd 0 DC 1.8
VG vin 0 pulse(0 1.8 10p 10p 10p 180p 400p)
Cload vout 0 15F

M1 vout vin 0 0 BSIM3_180nm_N W = '0.36u*alpha' L = 0.18u
M2 vout vin vd vd BSIM3_180nm_P W = '0.72u*alpha' L = 0.18u

.tran 1p 1000p

.measure tran tphl trig v(vin) val=0.9 rise=1 targ v(vout) val=0.9 fall=1
.measure tran tplh trig v(vin) val=0.9 fall=1 targ v(vout) val=0.9 rise=1

.control
run
plot vout vin
.endc

.end
```

$\alpha = 4$

2. Simulate and compute static current for a 2-input NAND gate with inputs A and B and with transistor widths chosen to achieve effective fall and rise resistance equal to that of a unit inverter for
   a) AB = 11 (1 point)




```
.include bsim.lib

Vdd Vcc 0 dc 1.8
V1 A 0 dc 1.8
V2 B 0 dc 1.8

M1 vout A Vcc Vcc BSIM3_180nm_P w=0.72u l=0.18u
M2 vout B Vcc Vcc BSIM3_180nm_P w=0.72u l=0.18u

M3 vout A 2 2 BSIM3_180nm_N w=0.72u l=0.18u
M4 2 B 0 0 BSIM3_180nm_N w=0.72u l=0.18u

Cl vout 0 15f

.tran 1p 5000p



.control
Run
Plot A B vout
.endc
.end
```

I = 1.18na

b) AB = 01 (1 point)

```
.include bsim.lib

Vdd Vcc 0 dc 1.8
V1 A 0 dc 1.8
V2 B 0 dc 0

M1 vout A Vcc Vcc BSIM3_180nm_P w=0.72u l=0.18u
M2 vout B Vcc Vcc BSIM3_180nm_P w=0.72u l=0.18u

M3 vout A 2 2 BSIM3_180nm_N w=0.72u l=0.18u
M4 2 B 0 0 BSIM3_180nm_N w=0.72u l=0.18u

Cl vout 0 15f
.tran 1p 5000p
.control
Run
Plot A B vout
.endc
.end
```

ngspice 41

b	0
vout	1.8
2	1.68947
v2#branch	0
v1#branch	0
vdd#branch	-5.51174e-10

No. of Data Rows : 5008
ngspice 7 ->

DES2_2b.txt

I = 0.551na

c) AB = 00 (1 point)

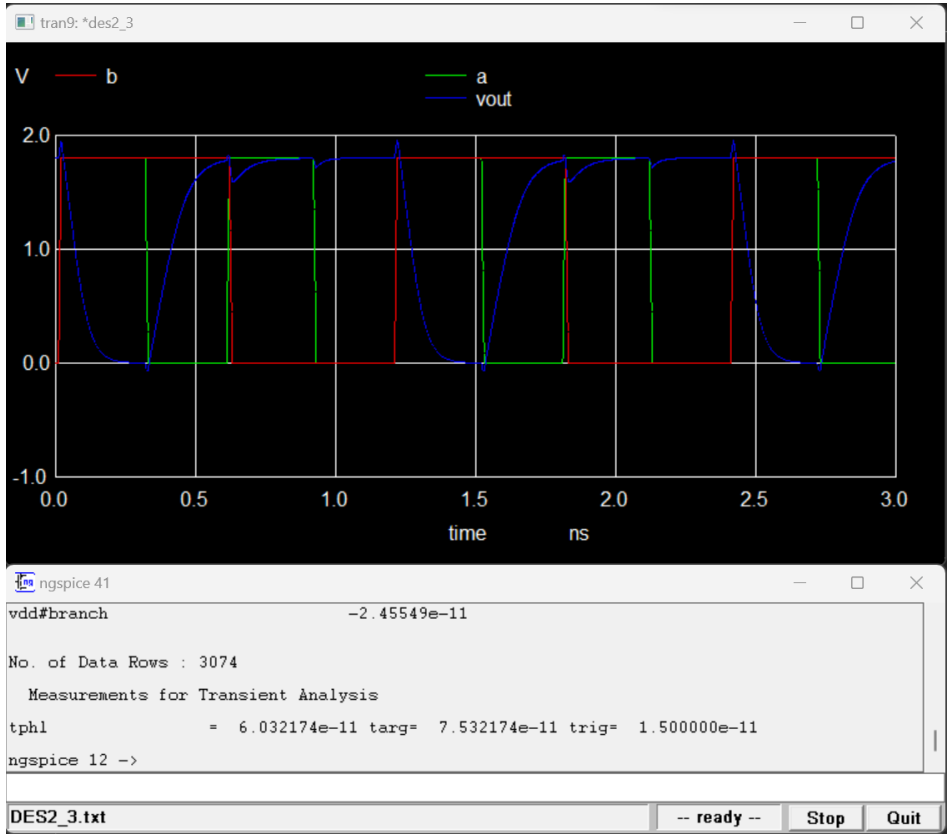
```
.include bsim.lib

Vdd Vcc 0 dc 1.8
V1 A 0 dc 0
V2 B 0 dc 0

M1 vout A Vcc Vcc BSIM3_180nm_P w=0.72u l=0.18u
M2 vout B Vcc Vcc BSIM3_180nm_P w=0.72u l=0.18u

M3 vout A 2 2 BSIM3_180nm_N w=0.72u l=0.18u
M4 2 B 0 0 BSIM3_180nm_N w=0.72u l=0.18u

Cl vout 0 15f
.tran 1p 5000p
.control
Run
Plot A B vout
.endc
.end
```

ngspice 41

```
b                                   0
vout                              1.8
2                            0.112102
v2#branch                           0
v1#branch                           0
vdd#branch                -2.45549e-11


No. of Data Rows : 5008
ngspice 8 ->
```

I = 0.024na

3. 5xx: For the NAND gate above, find tp_{HL} for AB = 00 -> 11 (1 point)

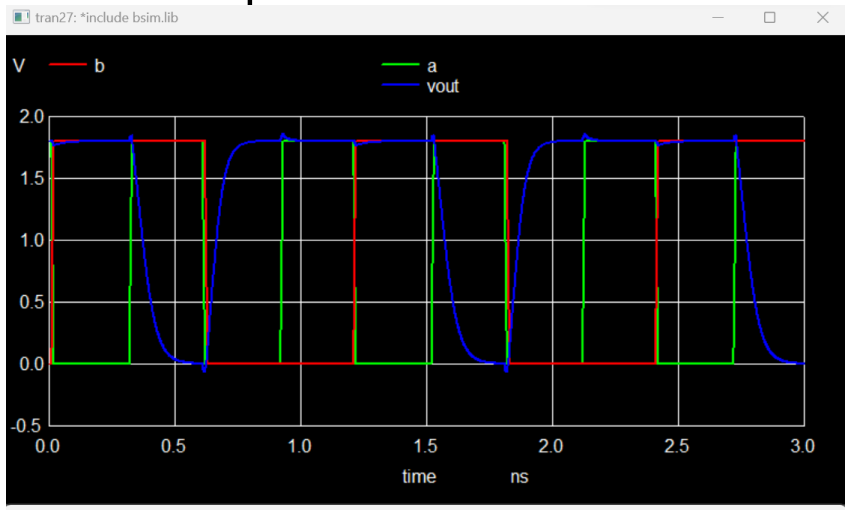


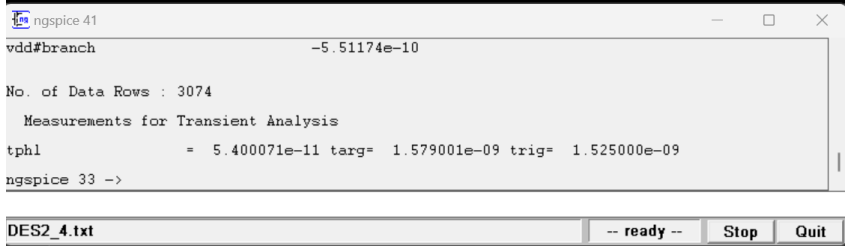

```
.include bsim.lib

Vdd Vcc 0 dc 1.8

VG1 A 0 pulse(0 1.8 10p 10p 10p 300p 600p)
VG2 B 0 pulse(0 1.8 10p 10p 10p 600p 1200p)

M1 vout A Vcc Vcc BSIM3_180nm_P w=0.72u l=0.18u
M2 vout B Vcc Vcc BSIM3_180nm_P w=0.72u l=0.18u

M3 vout A 2 2 BSIM3_180nm_N w=0.72u l=0.18u
M4 2 B 0 0 BSIM3_180nm_N w=0.72u l=0.18u

.measure tran tphl trig v(A) val=0.9 rise=1 targ v(vout) val=0.9 fall=1

Cl vout 0 15f
.tran 1p 3000p
.control
Run
Plot A B vout
.endc
.end
```

tp_{HL} = 60 psec

4. 5xx extra credit (not for 4xx): For the NAND gate above, compare tp_{HL} for AB = 00 -> 11 and AB = 01 ->11(1 point)

Below tphl for AB = 01 -> 11






```
.include bsim.lib

Vdd Vcc 0 dc 1.8

VG1 A 0 pulse(1.8 0 10p 10p 10p 300p 600p)
VG2 B 0 pulse(0 1.8 10p 10p 10p 600p 1200p)

M1 vout A Vcc Vcc BSIM3_180nm_P w=0.72u l=0.18u
M2 vout B Vcc Vcc BSIM3_180nm_P w=0.72u l=0.18u

M3 vout A 2 2 BSIM3_180nm_N w=0.72u l=0.18u
M4 2 B 0 0 BSIM3_180nm_N w=0.72u l=0.18u

.measure tran tphl trig v(A) val=0.9 rise=3 targ v(vout) val=0.9 fall=2

Cl vout 0 15f
.tran 1p 3000p
.control
Run
Plot A B vout
.endc
.end
```

Tphl = 54 psec(01 ->11) , Tphl = 60 psec(00->11)
Difference is 6psec slower for 00->11 transition