Intro to Processor Architecture

Project Mid-Evaluations

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Overview

The following module are implemented in the processor:
- (a) Fetch Stage: Contains instruction memory of 4096 memory locations, each 1-byte long.
- (b) Decode Stage: Contains 16 register files each 64-bit long.
- (c) Execute Stage: Contains a 64-bit ALU
- (d) Memory Stage: Contains a data memory of 4096 memory locations, each 64-bit long.
  (The code for showing status code is not written correctly yet)
- (e) PC Update Stage
- (f) Datapath Unit: Combines all the above stages. Contains a program counter register of 64-bit long.

All the registers except for the instruction memory gets updated at the positive edge of each clock cycle.

To compile the Processor run: `iverilog Datapath_Unit.v`

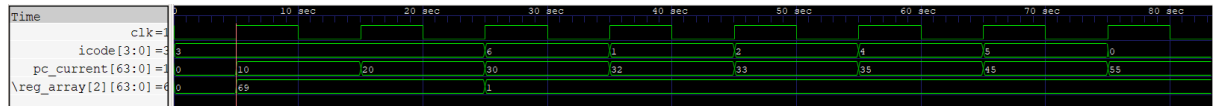To look at the waveforms run: `gtkwave dump.vcd`

Note: After running the code, nothing is seen on terminal as no monitor statement is included in the testbench. To monitor the data signals open gtkwave. Please ignore the warnings.

The following assembly code is being run in the processors:
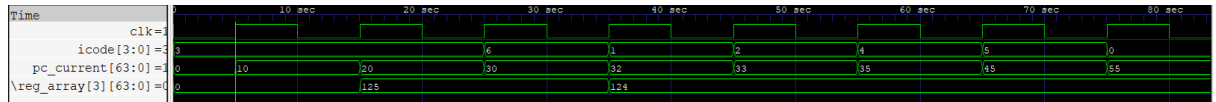
```
irmovq $69 %rdx

irmovq $125 %rbx

irmovq $1 %rdx

subq %rdx %rbx

nop

cmovne %rbx %rsp

rmmovq %rsp 2(%rdx)

mrmovq 2(%rdx) %rbp

halt
```
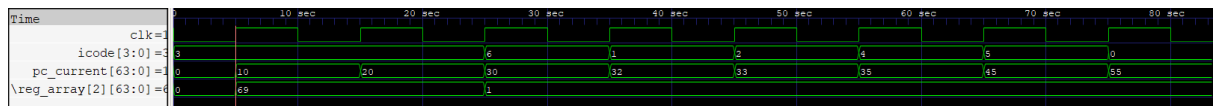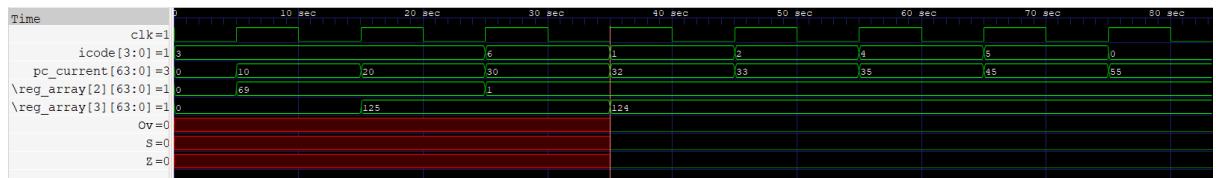
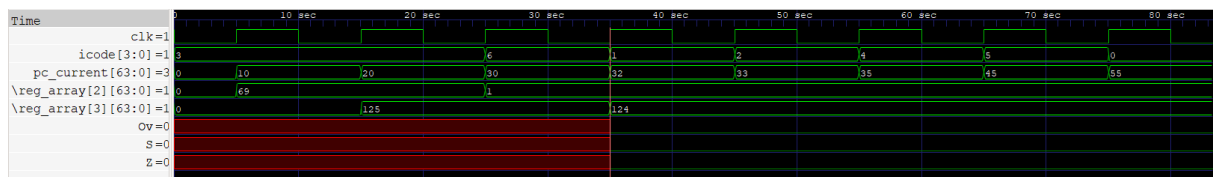# GTKwave waveforms

irmovq $69 %rdx

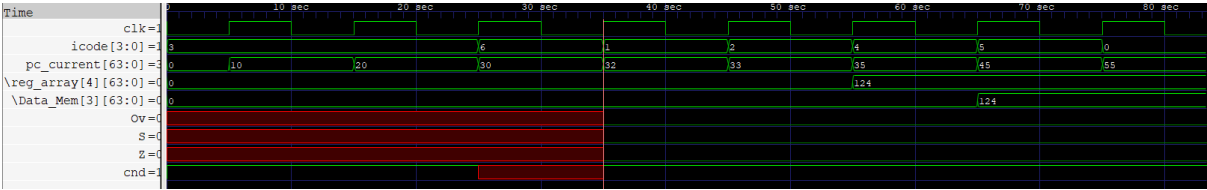## irmovq $125 %rbx

irmovq $1 %rdx

subq %rdx %rbx

nop

cmovne %rbx %rsp

rmmovq %rsp 2(%rdx)

mrmovq 2(%rdx) %rbp