```
· 15. b.4 addresses
                               · ELK & New instruction
                                                      · CLK IOW out of RST
    · 16 · bit date. 4 registers
                              * CLKT commit changes
    · 24-bit Instructions
                              · 74HC series preferred
    · Instruction formati
    TT TZ TI TA 14 18 17 16 15 14 13 15 11 10 1 7 7 6 6 4 3 2 1
    INSTR
                               co+a - 15 bits
    · 64 - pin backplane
        0-15 Adata
                               CLK
                           58
       16-31 Bdafa
                           59 RST
                           60 INTO
       32-55 Instruction
            A write/read
                           61 INT 1
            B write / rend
                          62 +3.3V
                                     63 GND
    · Instructions
    00000
01
    00001
                LD RAM@[dato] into A
                LDR RAME(B) into A
    0 0
       0 1 0
03
    00011
                MOV A into B
    00 1 00
                MOVD data into B
    00101
                ST data into RAME[B]
    00110
                STR A INO RAMELIS]
   00111
                STD A into RAMC[data]
                ALU instr A (4P) B - A OP = data
   01000
08
        001
                SR shift A right one bit
       010
                SL Shift A left one bit
03
        011
                IMP jump to [data]
06
       100
                JMPR jump to [A]
00
       1 0 1
                JMPZ jump to [date] if B=0
   01110
                IMPRZJUMP to [A] IF B=0
OF
   0 1
       1 1 1
               JAMANZ jump to Eduta] if B #0
   10000
               IMPRNE jump to [A] If B TO
11
   10001
12
   10010
1.3
   10
14
   10100
15
16
17
   10111
12
   1 10000
19
   11001
IA
   11010
18
16
10
       101
```

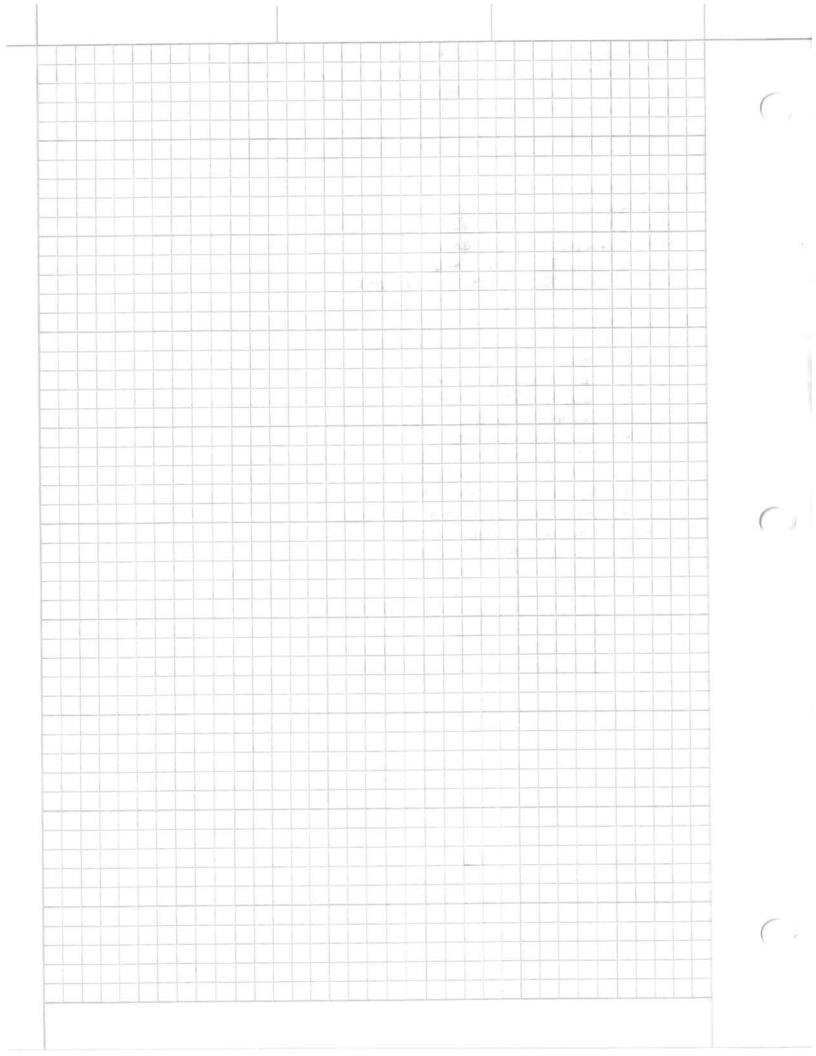
Instruction Architecture

18

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110

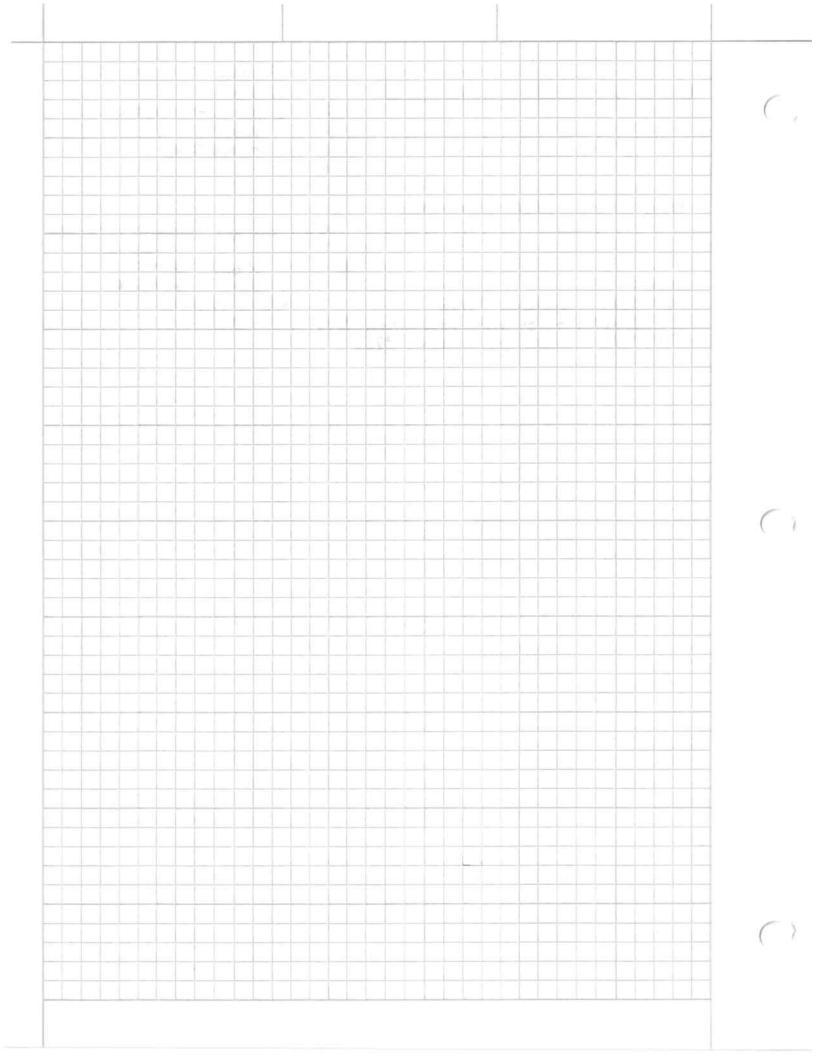
1 1 1 1 1



the same transfer to p 214 1 3 3 -200

A-data 15 14 13 12, 11 10 4 8 7 6 5 4,3 2 1 0 B-data ADD C. data -? -> ALU? SUB MASTE regador xo LOAD STORE Power + reset + clock + bus probes ALU: always answers into 00 abor Mus 12-bit Abus - 8 + 2+1 Mouser: B bus - 8 +2+1 854-803U - Bustoperd 4/1ea KST, GND, +Y, CLK, - 4 control - 6

571-5536385-5 - right engle 64 pin male 16 cq 571-5650861-5 - Vert 64 pin female 37 éq



ms13 15

B read/write

A read/write

CLK CLK2

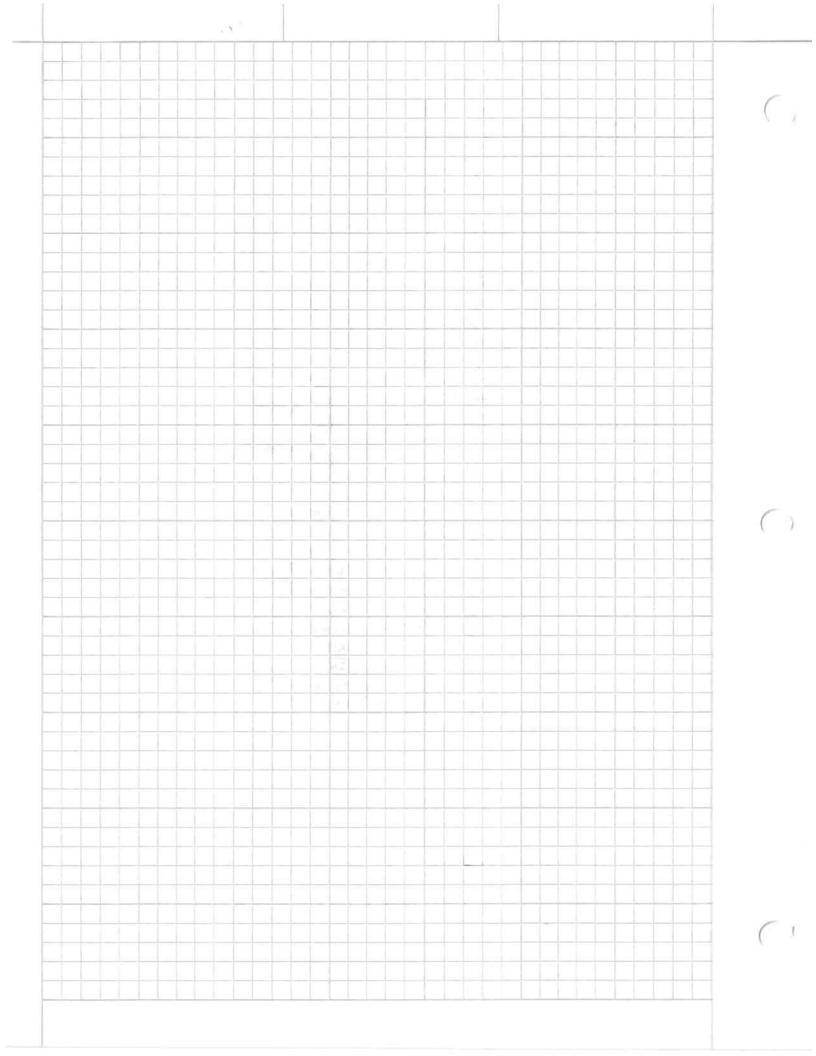
RST

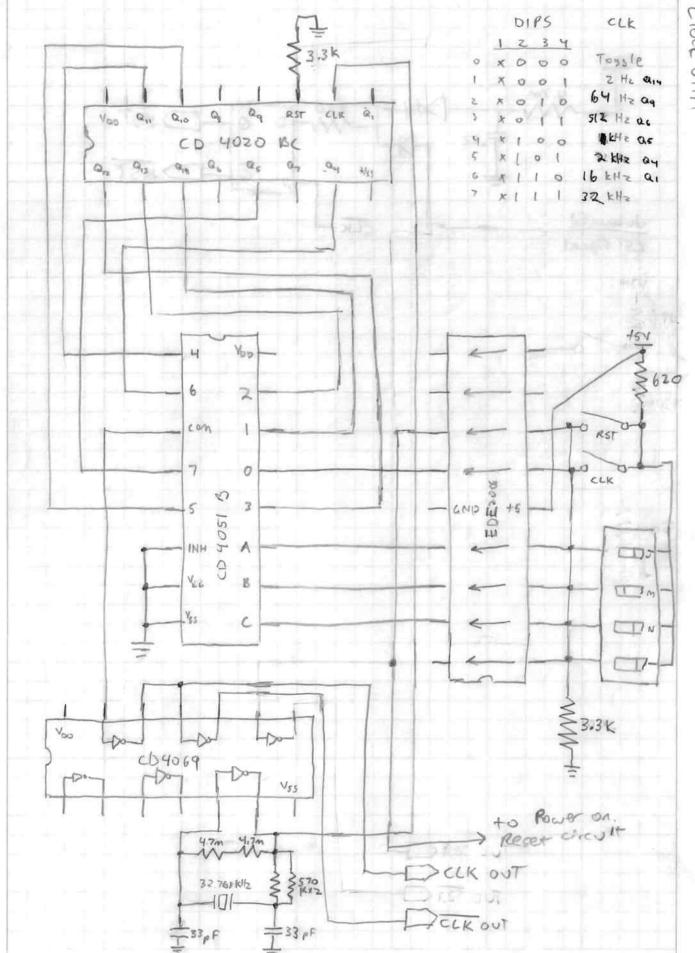
INT

+3,3V

GND

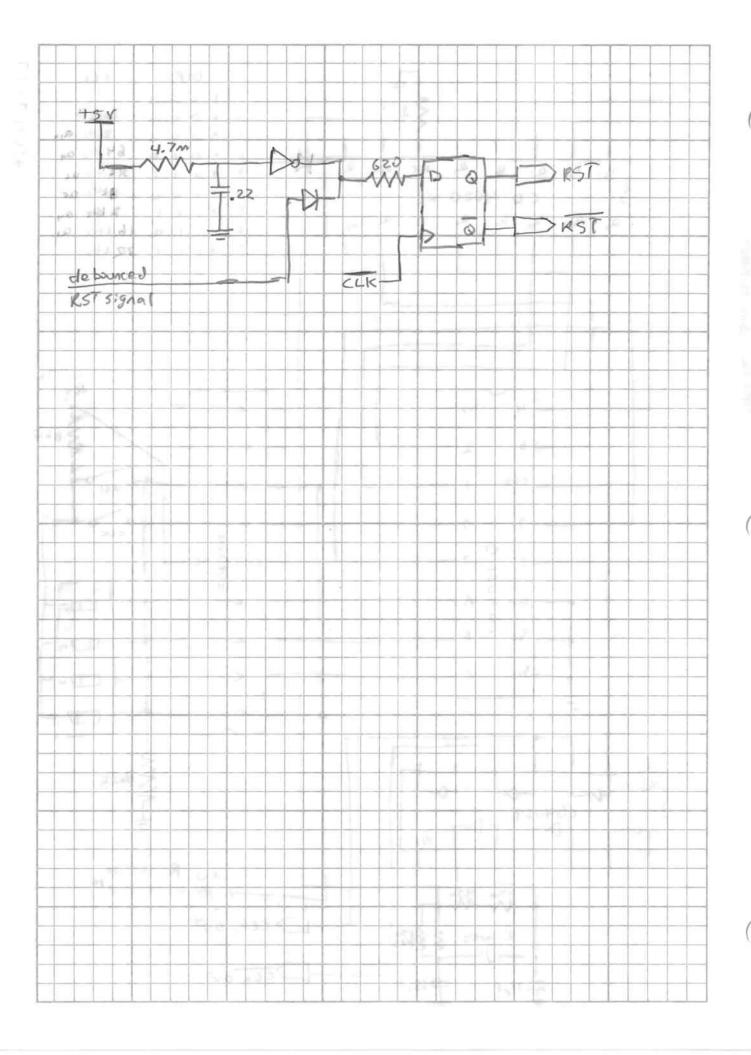
AMPAD"

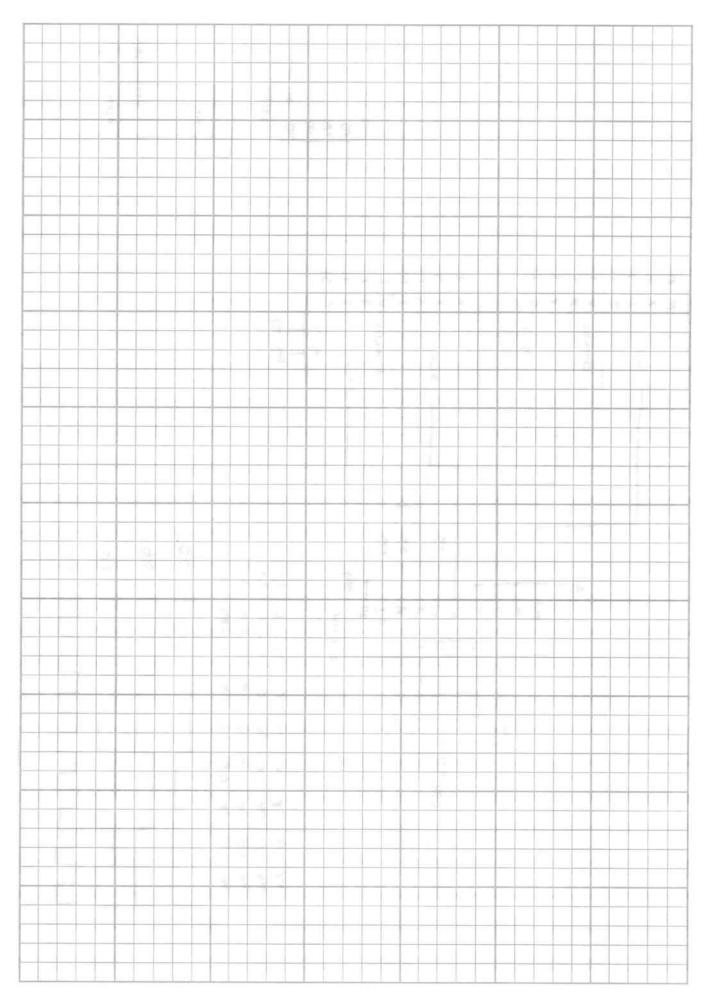


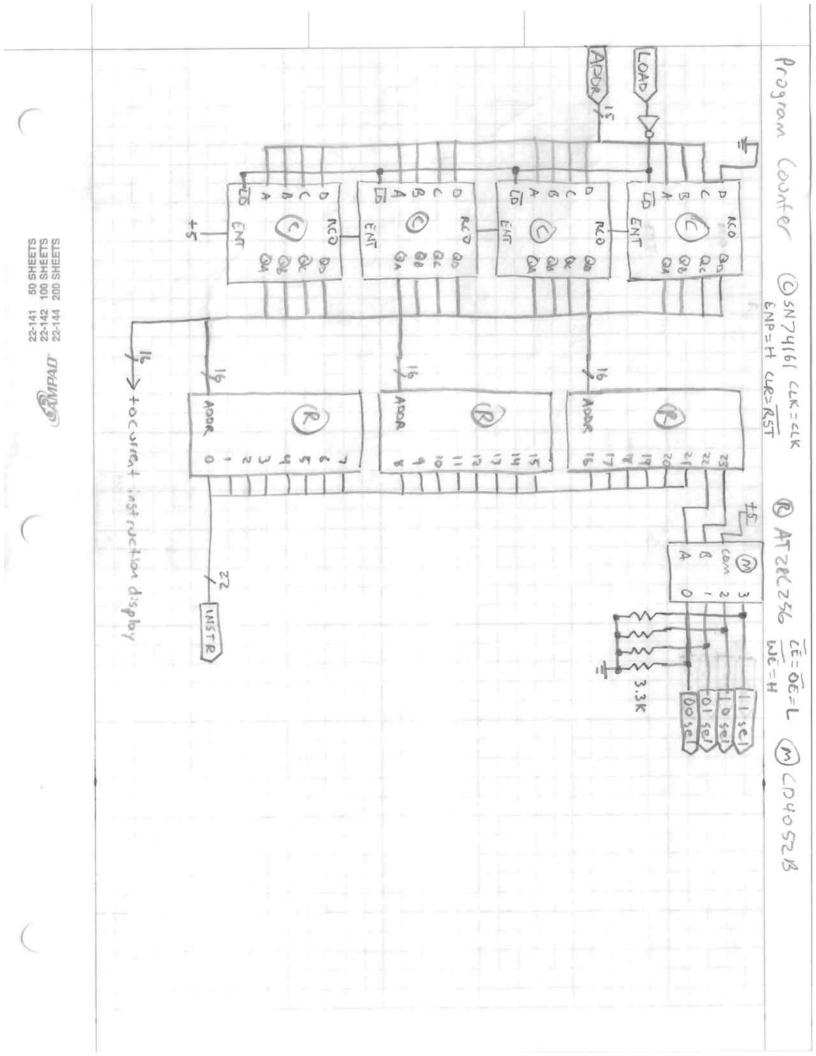


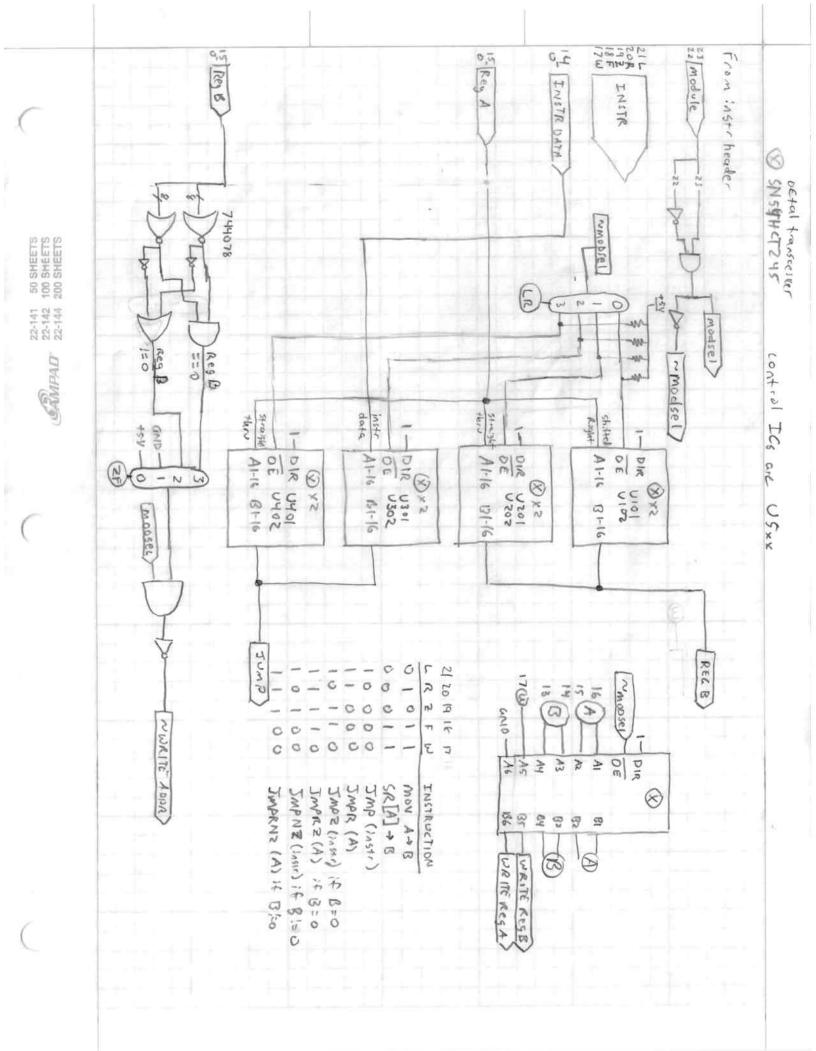
22-141 50 SHEETS 22-142 100 SHEETS 22-144 200 SHEETS

CANIFALT.









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