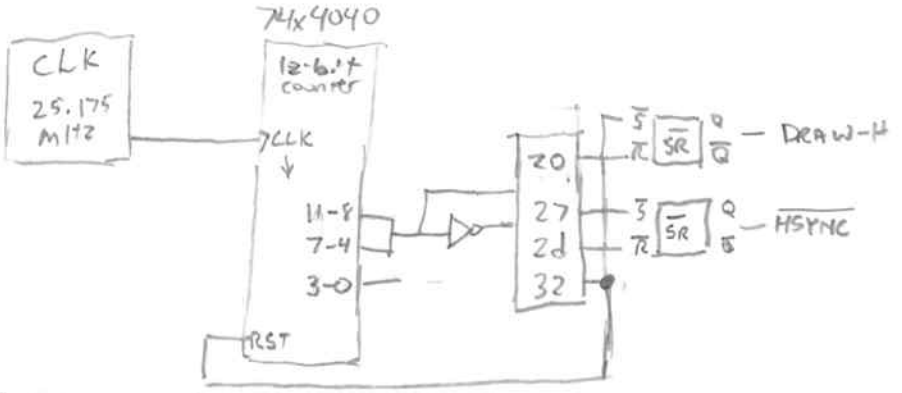
General timing

Screen refresh rate	60 Hz
Vertical refresh	31.46875 kHz
Pixel freq.	25.175 MHz

40ns

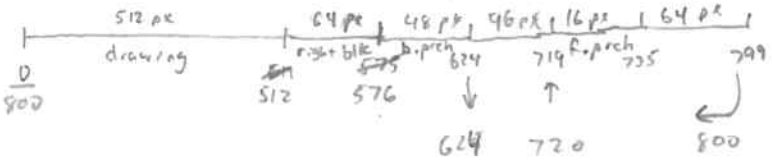


Horizontal timing (line)

Polarity of horizontal sync pulse is negative.

Scanline part	Pixels	Time [µs]
Visible area	640	25.422045680238
Front porch	16	0.63555114200596
Sync pulse	96	3.8133068520357
Back porch	48	1.9066534260179
Whole line	800	31.777557100298

0x000 (0) begin drawing ☆
0x200 (512) end drawing ☆
0x240 (576) end visible area/begin back porch
0x270 (624) end back porch/begin sync pulse ☆
0x2d0 (720) end sync pulse/begin front porch ☆
0x320 (800) end front porch/begin visible area/begin drawing ☆



Vertical timing (frame)

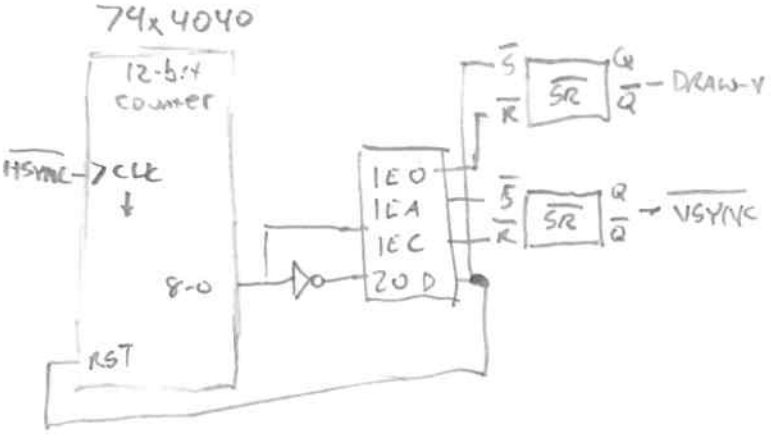
Polarity of vertical sync pulse is negative.

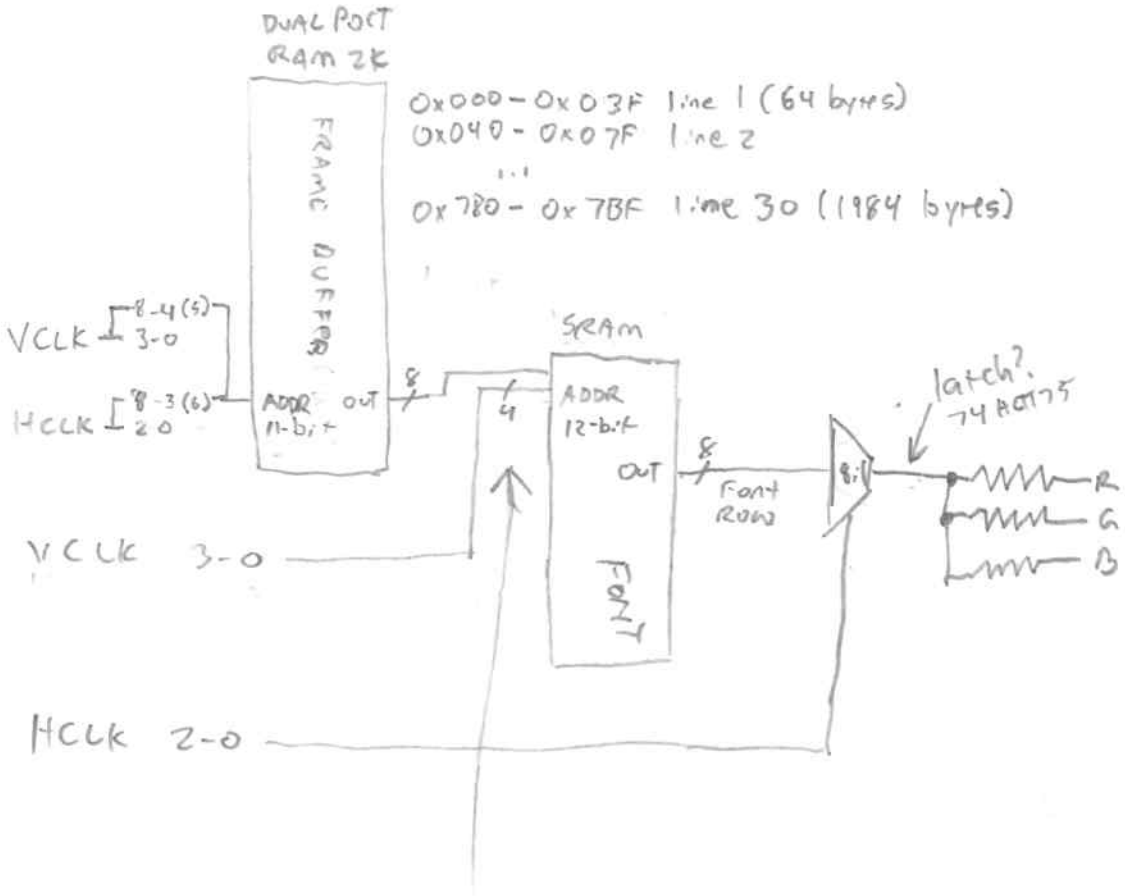
Frame part	Lines	Time [ms]
Visible area	480	15.253227408143
Front porch	10	0.31777557100298
Sync pulse	2	0.063555114200596
Back porch	33	1.0486593843098
Whole frame	525	16.683217477656

0x000 (0) begin drawing
0x1E0 (480) end drawing/begin front porch
0x1EA (490) begin sync pulse
0x1EC (492) end sync pulse/begin back porch
0x20D (525) end back porch/begin drawing

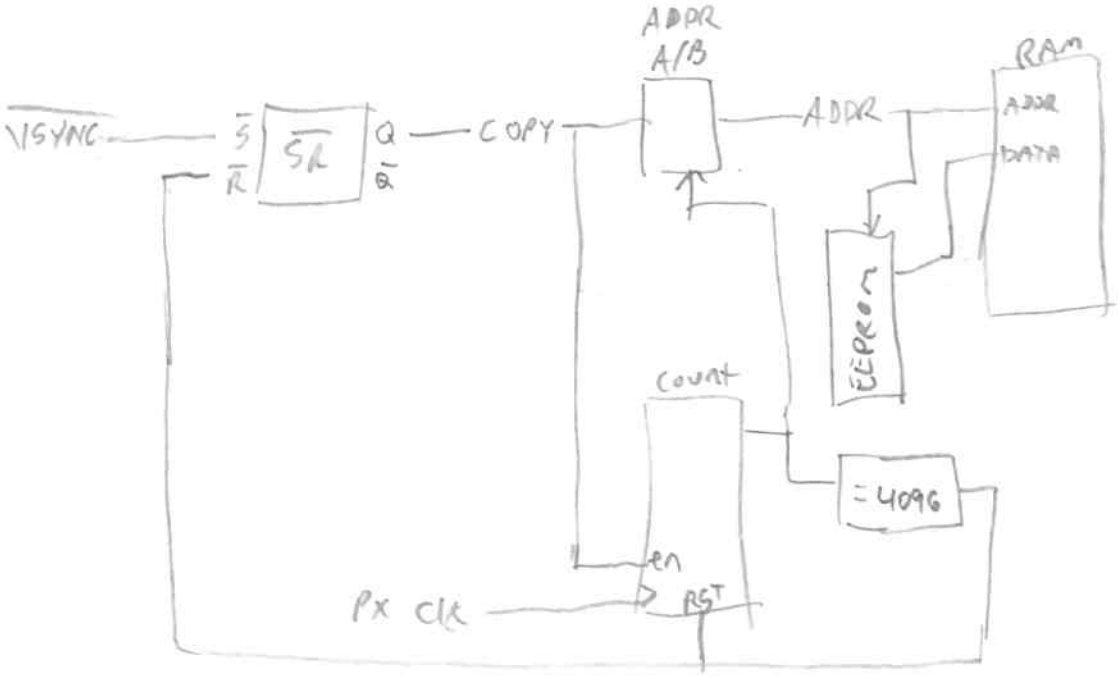
BOM

x1	25.175 MHz clock ✓ Mouser 774-MX045HS-3C-25.1	$2.07
x3	74HCT4040 14-bit counter ✓ Mouser 595-CD74HCT4040E	$0.68 ea.
x4	74HCT04 hex inverter ✓ Mouser 595-SN74HCT04N	$0.44 ea.
x10	74HCT30 8-input nand ✓ Mouser 595-CD74HCT30E	$0.41 ea.
x4	74HCT00 Quad nand ($\overline{SR}$ latch) ✓ Mouser 595-SN74HCT00N	$0.48 ea.
x1	74HCT151 8:1 mux ✓ Mouser 595-CD74HCT151E	$0.60 ea.
x1	32kx8 SRAM 12ns (Font) Mouser 972-71256SA12TPG ✓	$3.13 ea.
x1	2kx8 dual port SRAM 20ns (FB) Mouser 972-71421LA20JG8	$15.71 ea (Sample?)
x1	74HCT175 Quad D-FF ✓ Mouser 595-CD74HCT175E	
x3	74HCT157 Quad 4:1 demux ✓	

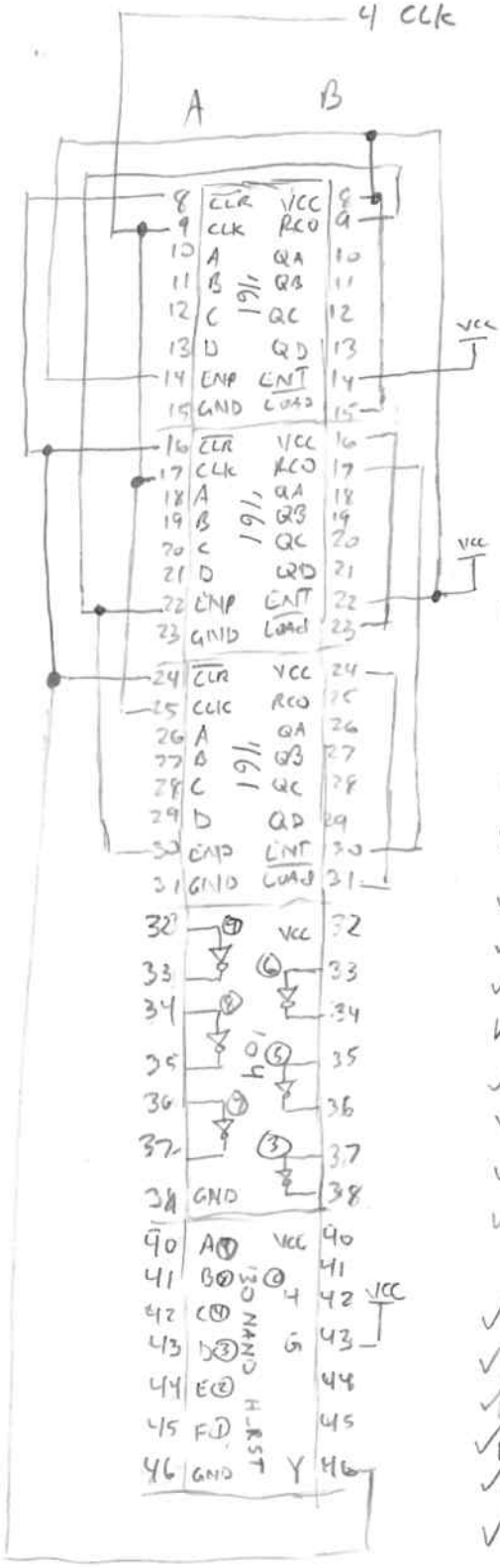




bus selector counter
SR latch eeprom
} load from eeprom during vertical porch



Horizontal Timing #1



- ✓A9 – A17
- ✓A17 – A25
- ✓E43 – A9 CLK
- ✓B8 – B15
- ✓B16 – B23
- ✓B24 – B31
- ✓A22 – A30
- ✓B9 – A22
- ✓B17 – B30
- ✓A14 – B22
- ✓B22 – VCC
- ✓A14 – VCC
- ✓A16 – A24
- ✓A8 – A16
- ✓A24 – B46 CLR

- ✓B27 – A40
- ✓B26 – A41
- ✓B14 – A42
- ✓B13 – A43
- ✓B12 – A44
- ✓B11 – A45
- ✓B10 – B42
- ✓B43 – VCC

RST

- ✓B32 – VCC
- ✓A38 – GND
- ✓B40 – VCC
- ✓A46 – GND

	inv bit
✓B27 – A32	9 → A33
✓B26 – A34	8 → A35
✓B21 – A36	7 → A37
✓B20 – B33	6 → B34
✓B19 – B35	5 → B36
✓B13 – B37	3 → B38

- ✓A15 – GND
- ✓A23 – GND
- ✓A31 – GND
- ✓B8 – VCC
- ✓B16 – VCC
- ✓B24 – VCC

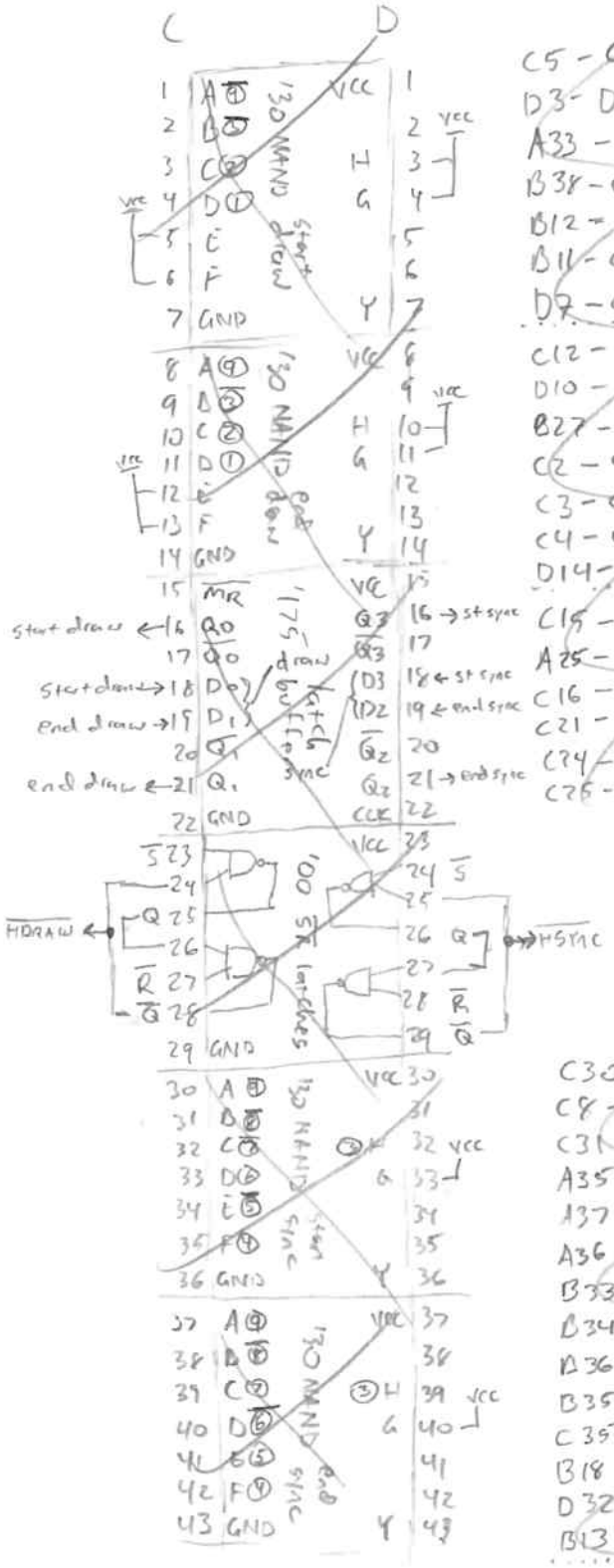
Horiz Pod D1

	B:t	
✓B10 – 21	0	HCNT
✓B11 – 81	1	HCNT
✓B12 – 20	2	HCNT
✓B13 – 80	3	HCNT
✓B18 – 19	4	HCNT
✓B19 – 79	5	HCNT
✓B20 – 18	6	HCNT
✓B21 – 78	7	HCNT
✓B26 – 17	8	HCNT
✓B27 – 77	9	HCNT
✓B46 – 16	10	HRST
✓L5 – 76	11	PIXEL C
✓D48 – 15	12	HSYNC
✓N4 – 75	13	PIXEL
✓C47 – 14	14	HDRAW
✓L6 – 74	15	PIXEL D
✓A9 – 13	–	CLK – CLK

	9 8 7 6 5 4 3 2 1 0	
reset counter	1 1 0 0 0 1 1 1 1 1	799
start drawing	0 0 0 0 0 0 0 1 1 1	7
end drawing	1 0 0 0 0 0 1 1 1 1	519
start sync	1 0 0 1 0 1 1 0 0 0	600
end sync	1 0 1 0 1 1 1 0 0 0	696

INV

Horizontal Timing #2



C5 - C6
D3 - D4
A33 - C1 bit $\overline{9}$
B38 - C2 bit $\overline{3}$
B12 - C3 bit 2
B11 - C4 bit 1
D7 - C18 start draw

C12 - C13
D10 - D11
B27 - C8 bit 9
C2 - C9 bit $\overline{3}$
C3 - C10 bit 2
C4 - C11 bit 1
D14 - C19 end draw

C15 - VCC
A25 - D22 CLK
C16 - C23 $\overline{S}$ draw
C21 - C27 $\overline{R}$ draw
C24 - 14 $\overline{\text{HDRAW}}$
C26 - 75 HDRAW

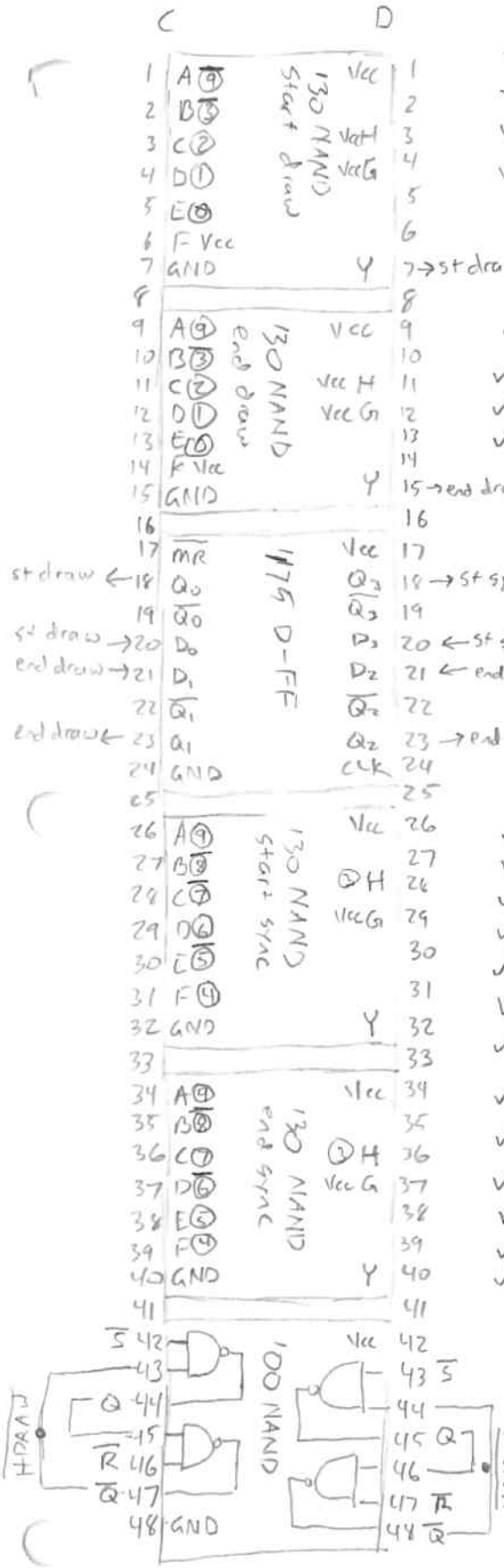
C7 - GND
D1 - VCC
C14 - GND
D8 - VCC
C22 - GND
D15 - VCC
C29 - GND
D23 - VCC
C36 - GND
D30 - VCC
C43 - GND
D37 - VCC

C24 - C28
C25 - C26
D25 - D29
D26 - D27
$\overline{SR}$ latch construction

C30 - C37
C8 - C30 (9)
C31 - C38
A35 - C31 (8)
A37 - C32 (7)
A36 - C39 (7)
B33 - C33 (6)
B34 - C40 (6)
D36 - C34 (5)
B35 - C41 (5)
C35 - C42 (4)
B18 - C35 (4)
D32 - D39 (3)
B13 - D32 (3)

D36 - D18 st sync unbuf
D43 - D19 end sync unbuf
D16 - D24 $\overline{S}$ sync
D21 - D28 $\overline{R}$ sync
D25 - 15 HSYNC
D26 - 76 HSYNC

Horizontal timing #2



✓D3 - D4 ✓A33 - C1 ⑨ ✓C7 - GND
✓C5 - C6 ✓B38 - C2 ③ ✓D1 - Vcc
✓C6 - D4 ✓A44 - C3 ②
✓D1 - D3 ✓A45 - C4 ①
✓B10 - C5 ⓪

✓D11 - D12 ✓A40 - C9 ⑨ ✓C15 - GND
✓C13 - C14 ✓C2 - C10 ③ ✓D9 - Vcc
✓C14 - D12 ✓C3 - C11 ②
✓D11 - D9 ✓C4 - C12 ①
C5 - C13 ⓪

✓D17 - C17 $\overline{MR}$ ✓C24 - GND
✓A25 - D24 CLK ✓D17 - Vcc
✓D7 - C20 st draw in
✓D15 - C21 end draw in
✓D32 - D20 st sync in
✓D40 - D21 end sync in

✓C26 - C34 ⑨ ✓A42 - C31 ④ ✓C32 - GND
✓C9 - C26 ⑨ ✓A43 - D28 ③ ✓D26 - Vcc
✓C27 - C35 ⑧ ✓D29 - D26 Vcc
✓A35 - C27 ⑧
✓A37 - C28 ⑦
✓B33 - C29 ⑥
✓B36 - C30 ⑤

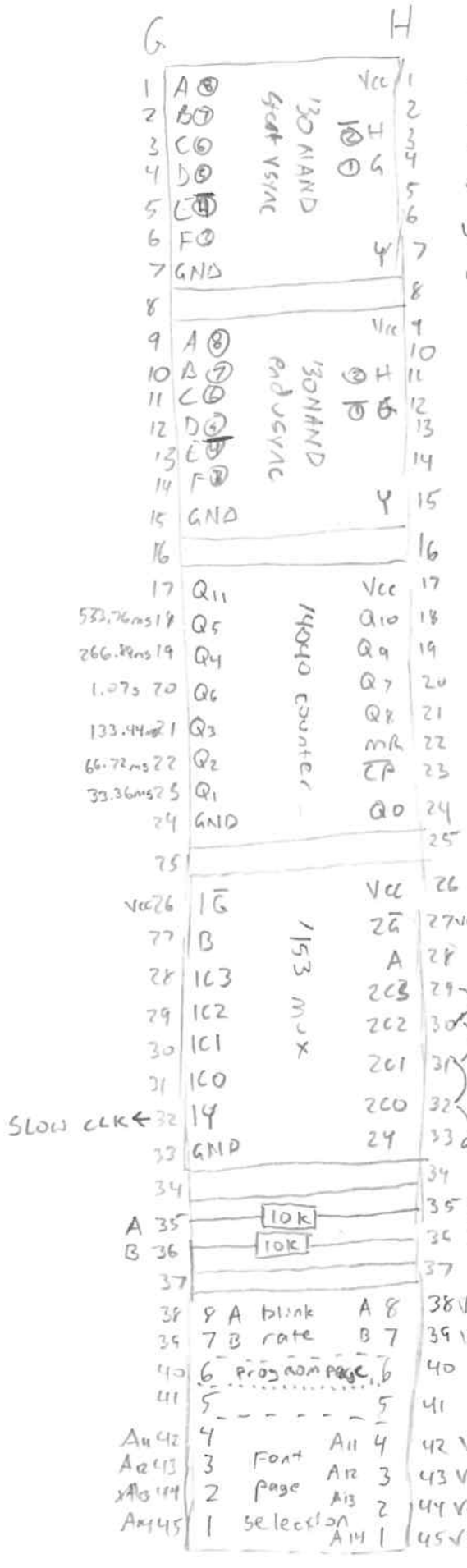
✓A36 - C36 ⑦ ✓C40 - GND
✓B34 - C37 ⑥ ✓D34 - Vcc
✓B35 - C38 ⑤
✓C39 - C31 ④
✓D36 - D28 ③
✓D37 - D34 Vcc

✓C44 - C45 ✓C48 - GND
✓C43 - C47 ✓D42 - Vcc
✓D45 - D46
✓D44 - D48

✓C18 - C42 ✓C47 - 14 H DRAW
✓C23 - C46 ✓C45 - 75 H DRAW
✓D18 - D43 ✓D48 - 15 HSYNC
✓D23 - D47 ✓D46 - 76 HSYNC

Vertical Timing #1

Vertical timing #2



✓G1 - G9 ✓G1 - F5 ✓H1 - Vcc
✓G2 - G10 ✓G2 - F4 ✓G7 - GND
✓G3 - G11 ✓G3 - E4
✓G4 - G12 ✓G4 - E2
✓G5 - G13 ✓G5 - E15
✓G6 - G14 ✓G6 - E5

✓H3 - E13 ✓H9 - Vcc
✓H11 - E12 ✓G15 - GND
✓H4 - E10
✓H12 - E11

Slow Clock Generation

✓G24 - GND
✓H17 - Vcc
✓H22 - GND
✓F30 - H23 VSYNC

✓G21 - G31 133ms 7↓ 8↓
✓G19 - G30 266ms 7↑ 8↑
✓G18 - G29 533ms 7↓ 8↓
✓G20 - G28 1067ms 7↑ 8↑

✓G33 - GND
✓H26 - Vcc
✓G26 - GND
✓H28 - G38 A DIP 8
✓G27 - G39 B DIP 7
✓G38 - G35 A pull down
✓G39 - G36 B pull down

✓H27 - Vcc
✓H29 - H30
✓H31 - H32
✓H30 - H31
✓H32 - GND

Feature selection

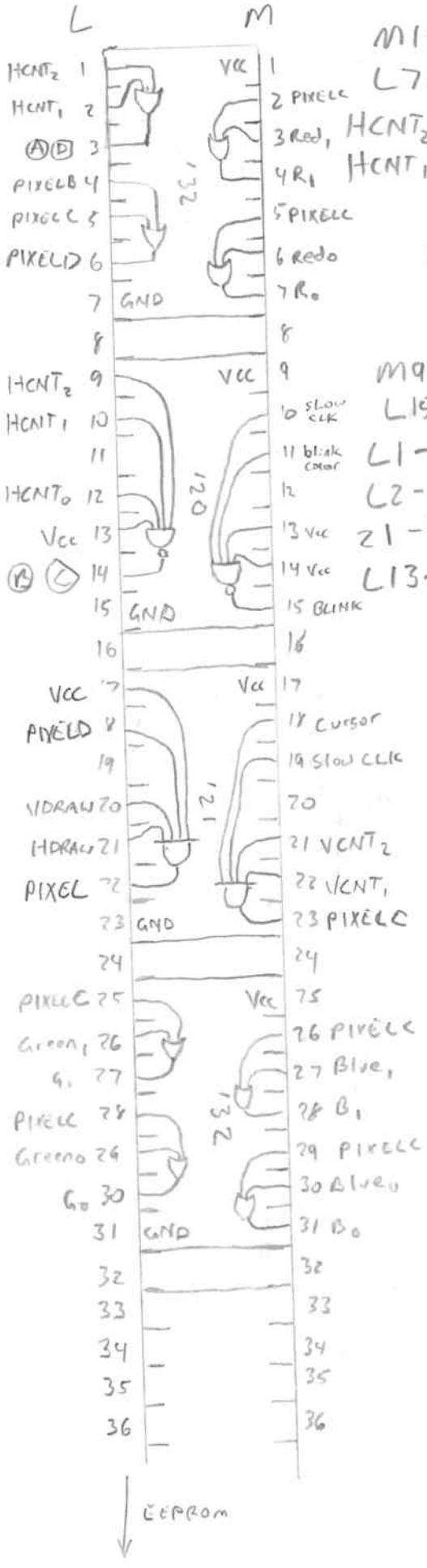
✓G42 - G47 A11 pull down
✓G43 - G48 A12 pull down
✓G44 - G49 A13 pull down
✓G45 - G50 A14 pull down

✓H35 - GND
✓H36 - GND

✓H38 - Vcc
✓H39 - Vcc

	G		H
✓	46		46
✓	47	10k	47 GND
✓	48	10k	48 GND
✓	49	10k	49 GND
	50	10k	50 GND

Character generation netlist #1



M1 - Vcc ✓
L7 - GND ✓
HCNT2 20 - L1 ✓
HCNT1 81 - L2 ✓
J1 - L3 ✓ A char. latch $\overline{CE}$
W2 - L3 ✓ D ADL RAM

L5 - M23 PIXELC ✓
L5 - M2 PIXELC ✓
M2 - M5 PIXELC ✓
K17 - M3 Red1 ✓
K20 - M6 Red0 ✓

M9 - Vcc ✓
L15 - GND ✓
L1 - L9 HCNT2 ✓
L2 - L10 HCNT1 ✓
21 - L12 HCNT0 ✓
L13 - Vcc ✓

J12 - L14 B color latch $\overline{CE}$ ✓
K24 - L14 C pixel shift SH/$\overline{LD}$ ✓
G32 - M10 slow CLK ✓
K13 - M11 blink color ✓
M13 - M14 - Vcc ✓

M17 - Vcc ✓
L23 - GND ✓

K16 - M18 cursor ✓
M10 - M19 slow CLK ✓
36 - M21 VCNT2 ✓
97 - M22 VCNT1 ✓

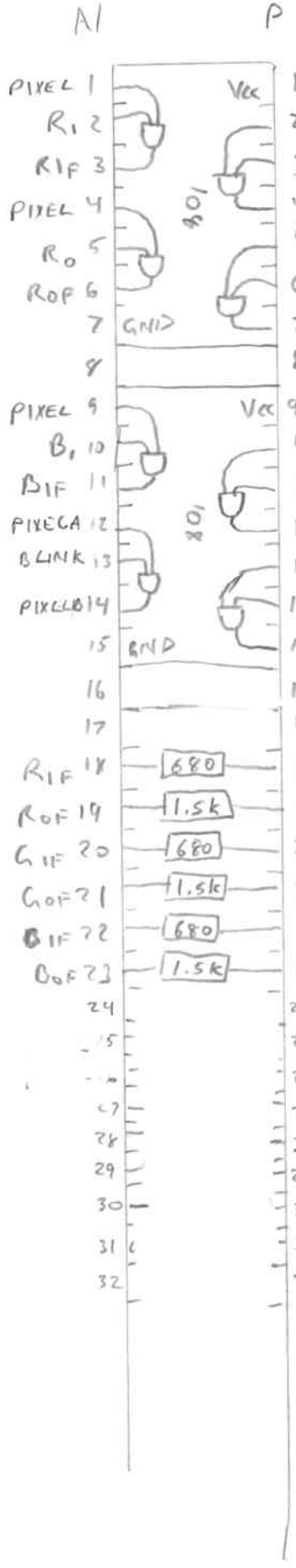
E28 - L20 VDRAW ✓
C45 - L21 HDRAW ✓

L18 - L6 PIXELD

M25 - Vcc ✓
L31 - GND ✓
L25 - L28 ✓
M26 - M29 ✓ PIXELC
L25 - M26 ✓
M23 - M26
→ break and change to L28 - GND for colored cursor

J20 - L26 Green1 ✓
J17 - L29 Green0 ✓
J16 - M27 Blue1 ✓
J13 - M30 Blue0 ✓

Color generation



P1-Vcc ✓
N7-GND ✓
P9-Vcc ✓
N15-GND ✓
✓N9-P10
✓N4-P5
✓N1-P2
✓N1-N4
✓P5-P10

L22-N4 PIXEL

✓M4-N2 R_1
✓M7-N5 R_0
✓L27-P3 G_1
✓L30-P6 G_0

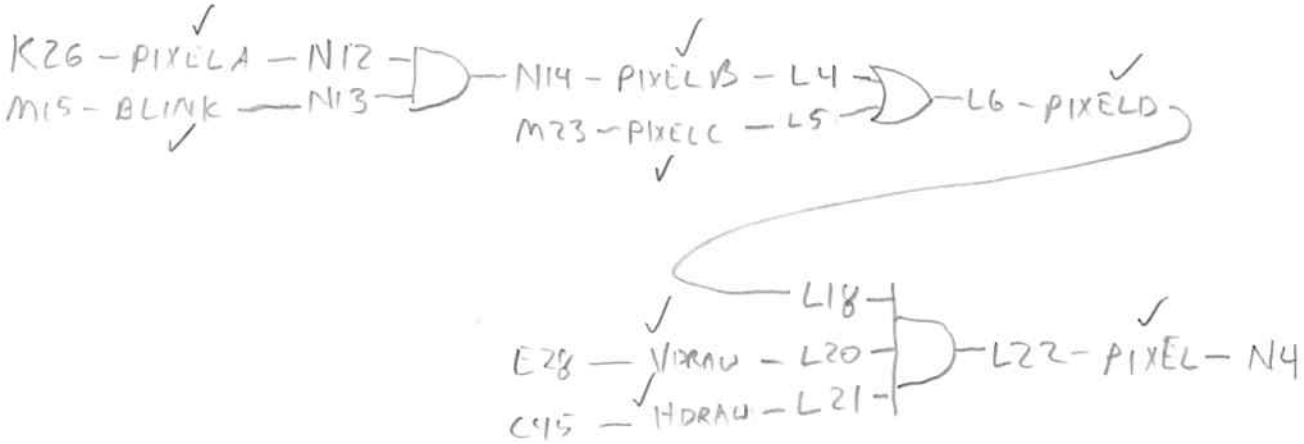
✓M28-N10 B_1
✓M31-P11 B_0
K26-N12 PIXEL A
M15-N13 BLINK
P25-Vcc N31-GND

✓N3-N18 ✓P18-P19 R ✓P18-25
✓N16-N19 ✓P20-P21 G ✓P20-24
✓P4-N20 ✓P22-P23 B ✓P22-26
✓P7-N21
✓N11-N22
✓P12-N23

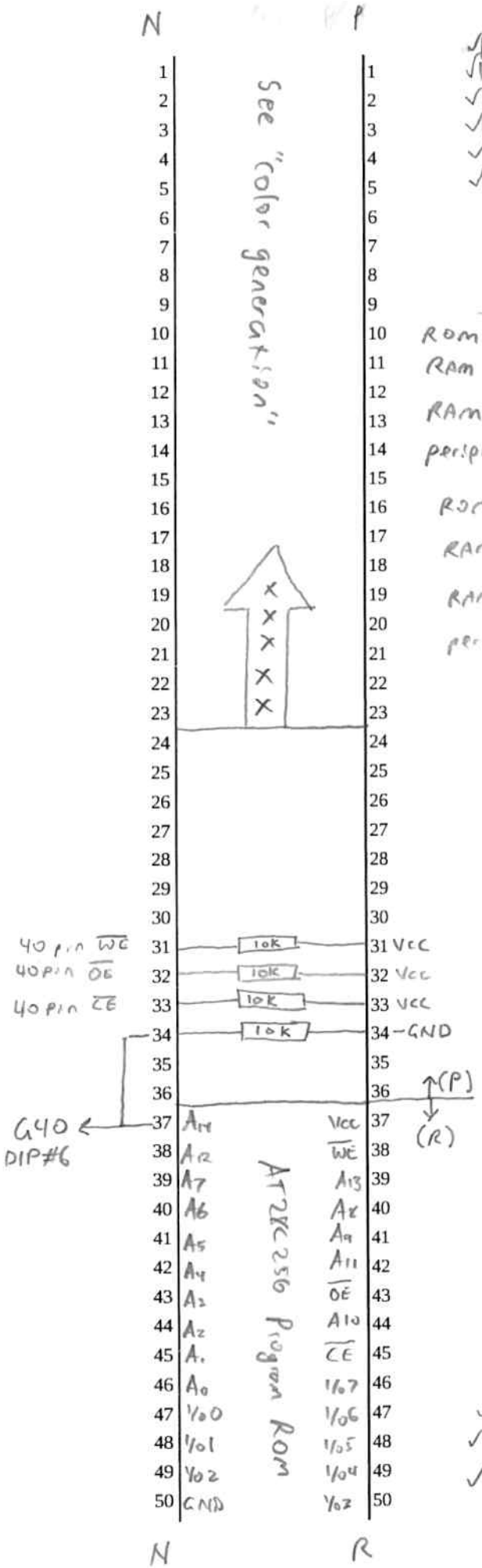
ROM/RAM pod E2

			Bit		Bit
V_{OOL}	V8	53	0 ✓	✓J47-49	8 I/O_0
	V9	113	1 ✓	✓J48-109	9
	V10	52	2 ✓	✓J49-48	10
	V11	112	3 ✓	✓L50-108	11 ROM
RAM	V12	51	4 ✓	✓L49-47	12
	V13	111	5 ✓	✓L48-107	13
	V15	50	6 ✓	✓L47-46	14
I/O_{7L}	V16	110	7 ✓	✓L46-106	15 I/O_7

(NC) 47 - CLK
J114 - ✓105 - GND



✓PIXELA - K26 - 92 - Vert pod
✓PIXELB - L4 - 91 - Vert pod
✓PIXELC - L5 - 76 - Horiz pod
✓PIXELD - L6 - 74 - Horiz pod
✓PIXEL - N4 - 75 - Horiz pod



Changes From V/W sheet

- ✓break V32 - (31) $\overline{CE}_R$
- ✓break V30 - (32) $R/\overline{W}_R$
- ✓break V29 - (33) $\overline{OE}_R$
- ✓break GND - (18) A15
- ✓break V33 - (16) $A14_R$
- ✓break GND - (30) CLK

$\overline{WE}$ = 32
A15 = 18
A14 = 16
CLK = 30
} 40-pin

mediated by CLK, see reverse

	From 40-pin $\overline{WE}$	A15	A14	ROM $\overline{OE}$	RAM $\overline{OE}$	RAM $\overline{WE}$
ROM	0	0	0	1	1	1
RAM	0	0	1	1	1	0
RAM	0	1	0	1	1	0
periph	0	1	1	1	1	1
ROM	1	0	0	0	1	1
RAM	1	0	1	1	0	1
RAM	1	1	0	1	0	1
periph	1	1	1	1	1	1

} while CLK is low

Program ROM hook-up

✓R37-Vcc ✓N50-GND ✓R45-Vcc $\overline{CE}$
✓R38-Vcc $\overline{WE}$ ✓P34-GND ✓N34-N37 A14
✓N37-G40 ✓H40-Vcc (A14 pull up)

✓R39-V34 A13 ✓N38-W33 A12
✓R42-W32 A11 ✓R44-W31 A10
✓R41-W30 A9 ✓R40-W29 A8
✓N39-W28 A7 ✓N40-W27 A6
✓N41-W26 A5 ✓N42-W25 A4
✓N43-W24 A3 ✓N44-W23 A2
✓N45-W22 A1 ✓N46-W21 A0

✓R46-V27 D7 ✓R47-V26 D6
✓R48-V25 D5 ✓R49-V24 D4
✓R50-V23 D3 ✓N49-V21 D2
✓N48-V20 D1 ✓N47-V19 D0

40-pin pull-ups

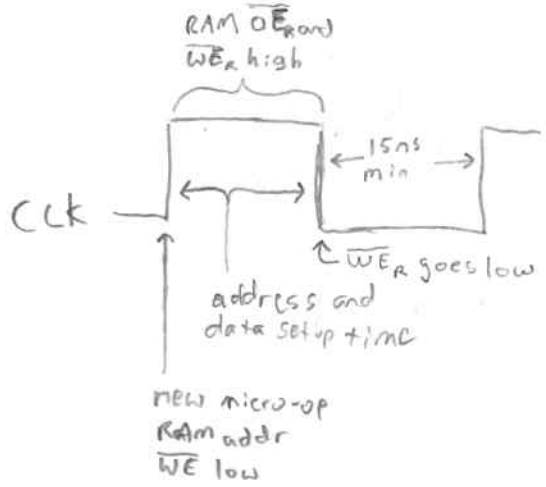
✓P32-P33-Vcc-P31 ✓N32-(33) $\overline{OE}$
✓N33-(31) $\overline{CE}$
✓P31-P32 ✓N31-(32) $\overline{WE}$

Addresses from 40-pin connector: 0000-3fff = ROM 0000-3fff (16K)
4000-bfff = RAM 0000-7fff (32K)
DIP#6 selects top(on) bot(off) of Program ROM

RAM writes on the rising edge of $\overline{WE}$

ROM A_{14} controlled by DIP
RAM A_{14} connects to 40-pin A_{15}, so:

40-pin		RAM	
A_{15}	A_{14}	A_{14}	
0	0	0	(ROM)
0	1	0	RAM, lower
1	0	1	RAM, upper
1	1	1	(peripherals)



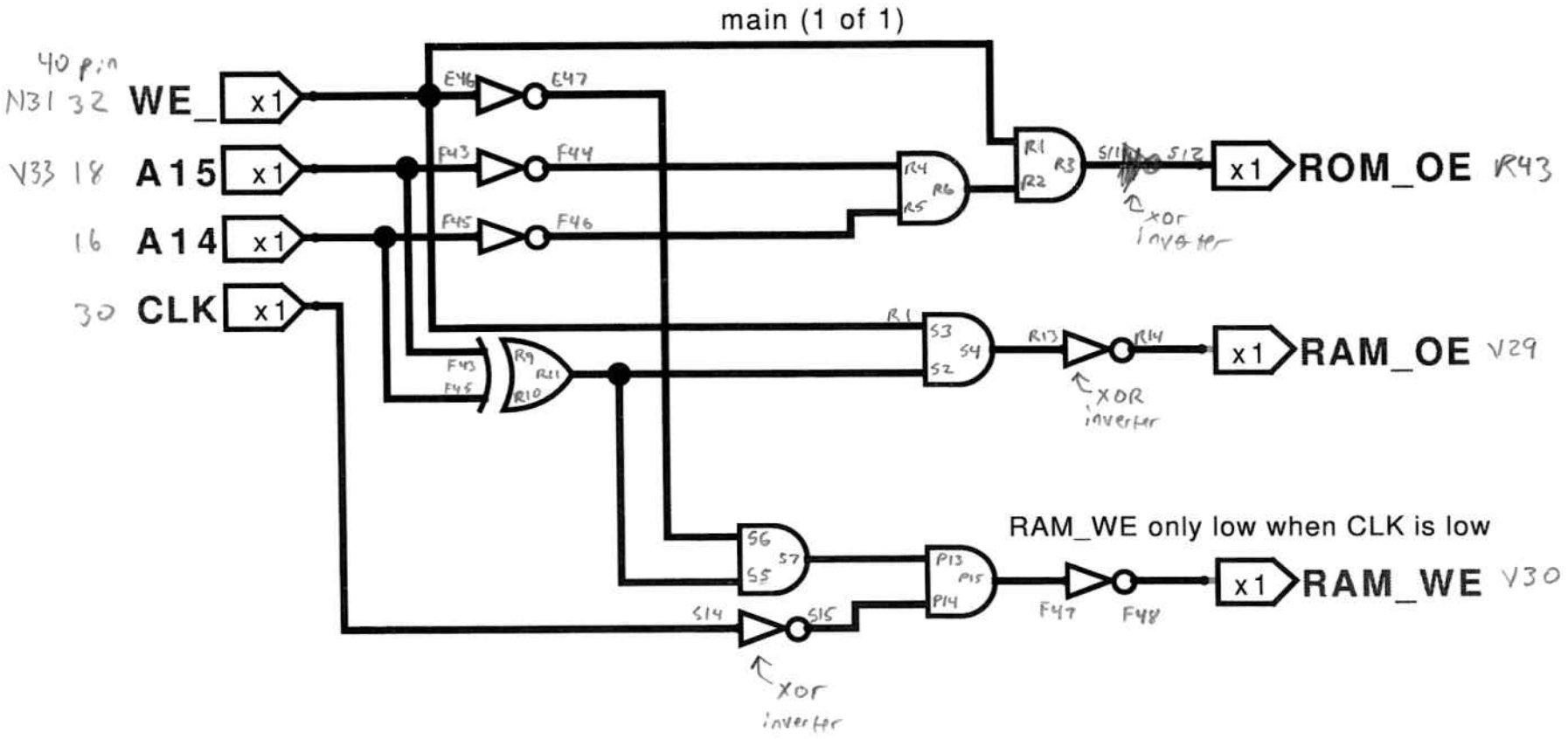
★ • $\overline{WE}_R$ must be high during address transition
• write occurs during overlap of low $\overline{CE}_R$ and low $\overline{WE}_R$

40-pin inputs

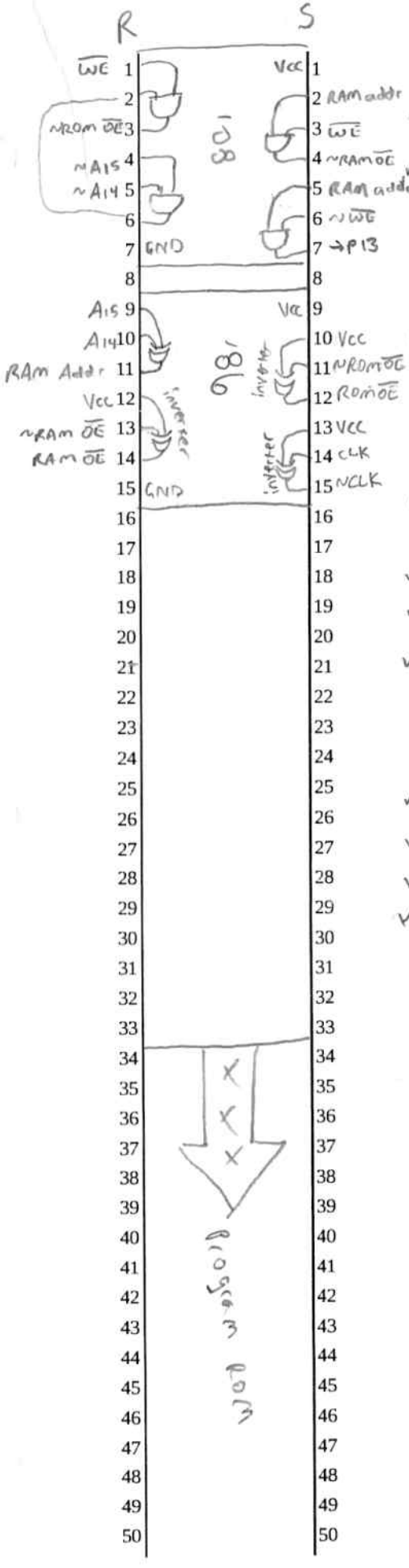
A_{15-0} 00x = ROM 01x = RAM 10x = RAM 11x = n/a
D_{7-0} data bus
$\overline{WE}$ high: ROM/RAM $\overline{OE}$ low for addresses starting with 00, 01, 10
low: ROM/RAM $\overline{OE}$ high, write pulse on falling clock edge
CLK see above

note: ROM & RAM $\overline{OE}$ high for all addresses starting with 11. If not performing a RAM/ROM operation, pull addr lines high to avoid data bus contention

RAM/ROM control 1 of 1



ROM / RAM control logic



RAM revised control signals

✓V32 - GND $\overline{CE}_R$

✓(18) - V33 $A14_R = A15_{Bus}$

✓(32) → N31 - E46 $\overline{WE}$ E47 = ~$\overline{WE}$

✓(18) → V33 - F43 $A15_{Bus}$ F44 = ~A15

✓(16) - F45 $A14_{Bus}$ F46 = ~A14

ROM_$\overline{OE}$ signal: $\overline{WE}$ + ~A15 + ~A14

✓N31 - R1 $\overline{WE}$ ✓F44 - R4 ~$A15_{Bus}$ ✓R6 - R2

✓F46 - R5 ~$A14_{Bus}$ ✓R3 - S11 ~ROM $\overline{OE}$ S10 - Vcc

✓S1 - Vcc ✓R7 - GND ✓S12 - R43 ROM $\overline{OE}$

RAM_$\overline{OE}$ signal: ~((A15 ⊗ A14) + ~$\overline{WE}$ + CLK)

✓S9 - Vcc ✓R15 - GND

✓F43 - R9 $A15_{Bus}$ ✓F45 - R10 $A14_{Bus}$

✓R11 - S2 ✓R1 - S3 $\overline{WE}$

✓S4 - R13 ✓R12 - Vcc

✓R14 - V29 RAM $\overline{OE}_R$

RAM_$\overline{WE}$ signal: ~(~$\overline{WE}$ + RAM addr + ~CLK)

✓R11 - S5 RAM addr ✓E47 - S6 ~$\overline{WE}$

✓S7 - P13 ✓S15 - P14 ~CLK

✓P15 - F47 ✓F48 - V30 $\overline{WE}_R$

✓(30) - S14 CLK ✓S13 - Vcc

← looking into male connector

1 Vcc	18 ~~GND~~ → A15	39 Vcc
2 GND	19 GND	40 GND
3 A7	20 KEY NC	
4	21 GND	
5 A6	22 D4	
6 A4	23 D3	
7 A5	24 D5	
8 A10	25 D2	
9 A11	26 D6	
10 A13	27 D1	
11 A3	28 D7	
12 A12	29 D0	
13 A2	30 ~~GND~~ → CLK	
14 A13	31 $\overline{CE}$ (NC) pulled up	
15 A1	32 R/$\overline{W}$ pulled up	
16 A14	33 $\overline{OE}$ (NC) pulled up	
17 A0	34 R/$\overline{W}$	

VGA connector

Black – GND – 85 – ✓
① Red – Red – 25 – P18
② Green – Green – 24 – P20
③ Blue – Blue – 26 – P22
⑬ HSYNC – Yellow – 87 – 15 ✓
⑭ VSYNC – White – 86 – 31 ✓

From CPU:
0x4000 – 0x4FFF characters
0x5000 – 0x5FFF colors

Memory range

0x0000 – 0x0FFF characters
0x1000 – 0x1FFF colors
13-bit address
8-bit data
Control:
$\overline{CE}_R$ 25 pins
R/$\overline{W}_R$
$\overline{OE}_R$
GND

Dual Port RAM L=GPU R=CPU

Power

V14 – GND ✓
V17 – Vcc ✓
V18 – GND ✓
V22 – Vcc ✓
W34 – GND ✓
W7 – GND ✓
W1 – Vcc ✓

Static Signals

$\overline{BUSY}_L$ – W16 – GND* ✓
A_{13L} – V1 – GND ✓
A_{14L} – V2 – GND ✓
$\overline{BUSY}_R$ – W19 – Vcc* ✓

m/$\overline{S}$ – W18 – GND* ✓
$\overline{CE}_L$ – V3 – GND ✓
R/$\overline{W}_L$ – V5 – Vcc ✓
$\overline{OE}_L$ – V6 – GND ✓
$\overline{SEM}_L$ – V4 – Vcc ✓
$\overline{SEM}_R$ – V31 – Vcc ✓

* Slave mode enabled to disable write to bit on BUSY. In slave mode, $\overline{BUSY}$ is a write inhibit pin (input): high = writes enabled, low = writes disabled.

1	A_{13L} GND	Vcc 68	1	
2	A_{14L} GND	L3-A_{12L} 67	2	
3	$\overline{CE}_L$ GND	V_{CNT8} A_{11L} 66	3	
4	$\overline{SEM}_L$ Vcc	V_{CNT7} A_{10L} 65	4	
5	R/$\overline{W}_L$ Vcc	V_{CNT6} A_{9L} 64	5	
6	$\overline{OE}_L$ GND	V_{CNT5} A_{8L} 63	6	
7	N/C	V_{CNT4} A_{7L} 62	7	
8	I/O_{0L}	V_{CNT3} A_{6L} 61	8	
9	I/O_{1L}	H_{CNT0} A_{5L} 60	9	
10	I/O_{2L}	H_{CNT7} A_{4L} 59	10	
11	I/O_{3L}	H_{CNT6} A_{3L} 58	11	
12	I/O_{4L} latches	H_{CNT5} A_{2L} 57	12	
13	I/O_{5L}	H_{CNT4} A_{1L} 56	13	
14	GND	H_{CNT3} A_{0L} 55	14	
15	I/O_{6L}	$\overline{INT}_L$ 54	15	
16	I/O_{7L}	GND $\overline{BUSY}_L$ 53	16	
17	Vcc	GND 52	17	
18	GND	GND m/$\overline{S}$ 51	18	
19	I/O_{0R}	Vcc $\overline{BUSY}_R$ 50	19	
20	I/O_{1R}	$\overline{INT}_R$ 49	20	
21	I/O_{2R}	A_{0R} 48	21	
22	Vcc	A_{1R} 47	22	
23	I/O_{3R} VGA video	A_{2R} 46	23	
24	I/O_{4R}	A_{3R} 45	24	
25	I/O_{5R}	A_{4R} 44	25	
26	I/O_{6R}	A_{5R} 43	26	
27	I/O_{7R}	A_{6R} 42	27	
28	N/C	A_{7R} 41	28	
29	$\overline{OE}_R$	A_{8R} 40	29	
30	R/$\overline{W}_R$	A_{9R} 39	30	
31	$\overline{SEM}_R$ Vcc	A_{10R} 38	31	
32	$\overline{CE}_R$	A_{11R} 37	32	
33	A_{14R}	A_{12R} 36	33	
34	A_{13R}	GND 35	34	

40-pin conn

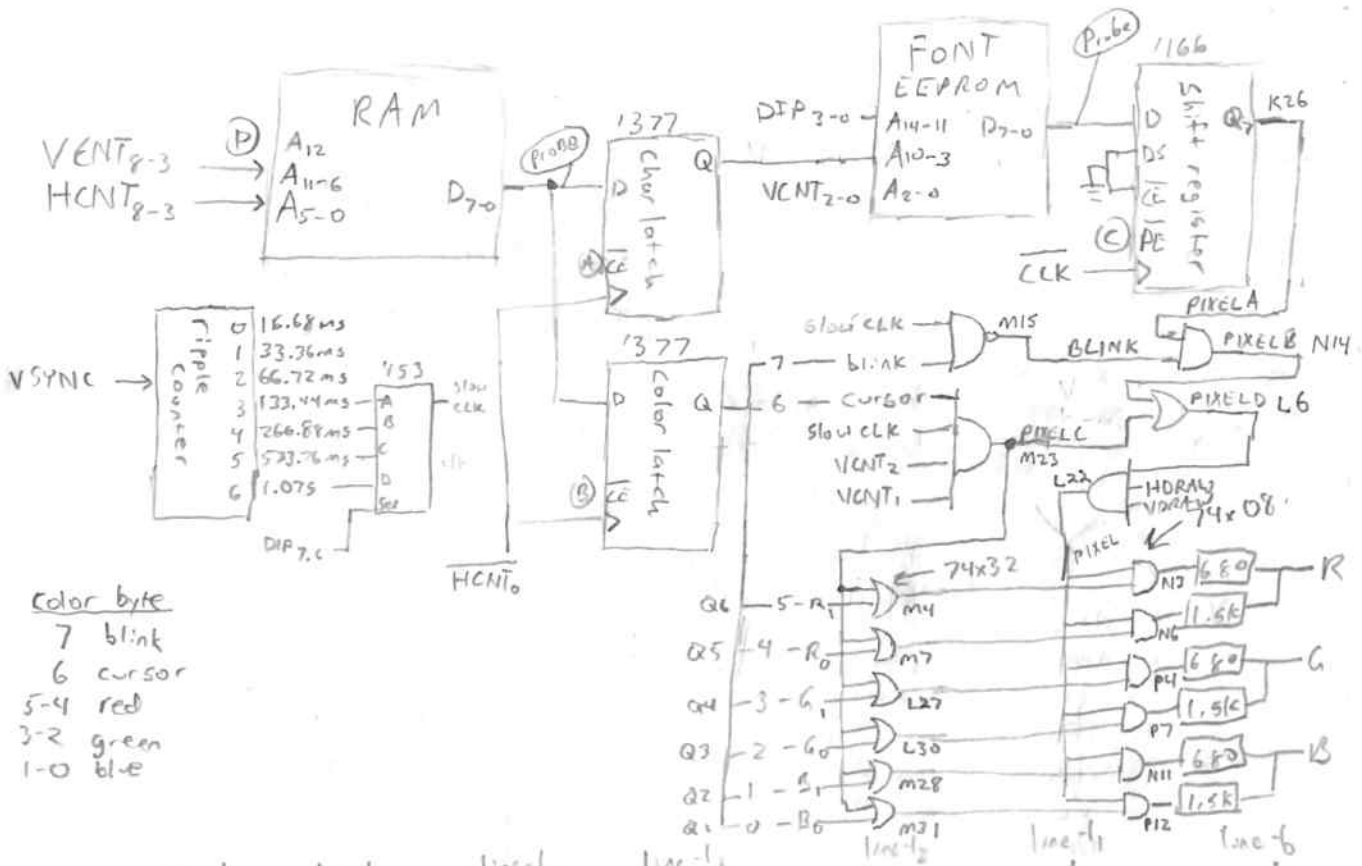
W
V_{CNT8} – 33 – W3 A_{11L} ✓
V_{CNT7} – 94 – W4 A_{10L} ✓
V_{CNT6} – 34 – W5 A_{9L} ✓
V_{CNT5} – 95 – W6 A_{8L} ✓
V_{CNT4} – 35 – W7 A_{7L} ✓
V_{CNT3} – 96 – W8 A_{6L} ✓
H_{CNT8} – 17 – W9 A_{5L} ✓
H_{CNT7} – 78 – W10 A_{4L} ✓
H_{CNT6} – 18 – W11 A_{3L} ✓
H_{CNT5} – 79 – W12 A_{2L} ✓
H_{CNT4} – 19 – W13 A_{1L} ✓
H_{CNT3} – 80 – W14 A_{0L} ✓

↷ edge connector
↓ 40-pin connector ↷

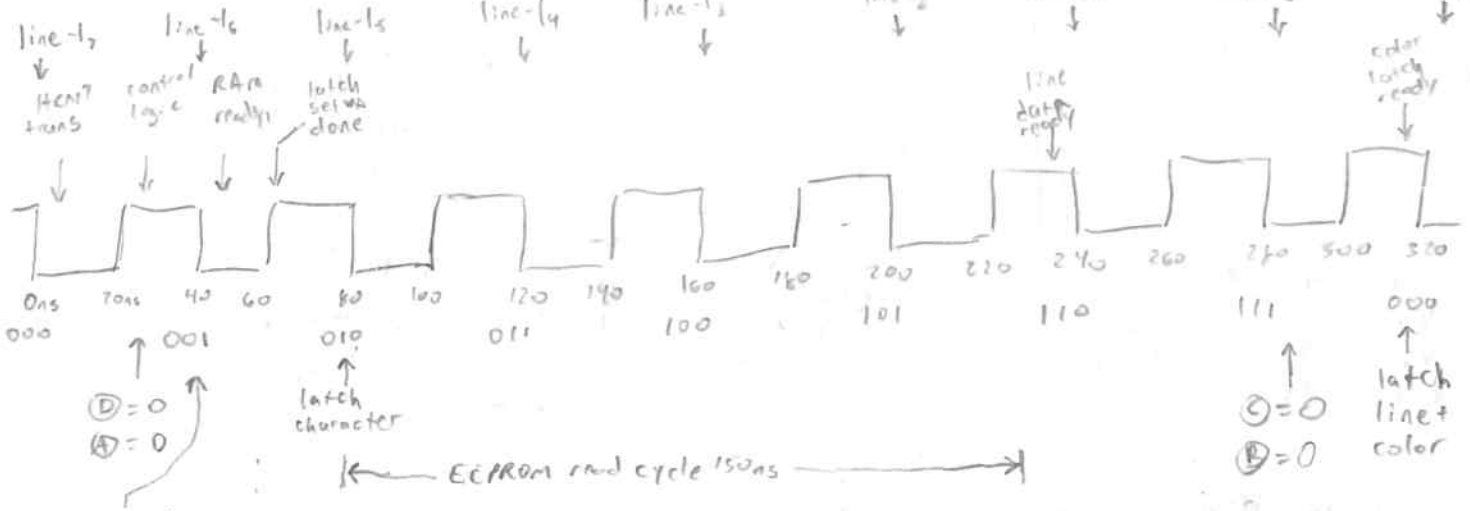
Vcc – 1 ✓
GND – 2 ✓
A_{7R} W28 – 3 ✓
A_{8R} W29 – 4 ✓
A_{6R} W27 – 5 ✓
A_{9R} W30 – 6 ✓
A_{5R} W26 – 7 ✓
A_{10R} W31 – 8 ✓
A_{4R} W25 – 9 ✓
A_{11R} W32 – 10 ✓
A_{3R} W24 – 11 ✓
A_{12R} W33 – 12 ✓
A_{2R} W23 – 13 ✓
A_{13R} V34 – 14 ✓
A_{1R} W22 – 15 ✓
A_{14R} V33 – 16 ✓
A_{0R} W21 – 17 ✓

~~GND~~ – 18 ✓ – A15
GND – 19 ✓
20
GND – 21 ✓
D_4 V24 – 22 ✓
D_3 V23 – 23 ✓
D_5 V25 – 24 ✓
D_2 V21 – 25 ✓
D_6 V26 – 26 ✓
D_1 V20 – 27 ✓
D_7 V27 – 28 ✓
D_0 V19 – 29
GND – 30 ✓
$\overline{CE}$ V32 – 31 ✓
R/$\overline{W}$ V30 – 32 ✓
$\overline{OE}$ V29 – 33 ✓

Character generation overview



Color byte
- 7 blink
- 6 cursor
- 5-4 red
- 3-2 green
- 1-0 blue



maybe false latch here, but should be ok

HCNT2-0	A	B	C	D	
0 0 0	0	1	1	0	latch char
0 0 1	0	1	1	0	present color addr
0 1 0	1	1	1	1	
0 1 1	1	1	1	1	
1 0 0	1	1	1	1	
1 0 1	1	1	1	1	
1 1 0	1	1	1	1	
1 1 1	1	0	0	1	latch char row

HCNT transition	t=0
control logic	+20ns
RAM data ready	+20ns
latch setup time	+15ns
pulse hold	+23ns