VLSI System Design (Graduate Level)

Fall 2025

HOMEWORK I

REPORT

Must do self-checking before submission:

◻ Compress all files described in the problem into one tar

◻ All SystemVerilog files can be compiled under SoC Lab environment

◻ All port declarations comply with I/O port specifications

◻ Organize files according to File Hierarchy Requirement

◻ No any waveform files in deliverables

Student name:

Student ID:

**Summary**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Hardware | | | | | | | | |
|  | | | | | RTL | | | synthesis |
| Top | CPU | | | |  | |  | |
| Synthesis result | | | | | | | | |
| Area | | | | Clock cycle(ns) | | | | |
|  | | | |  | | | | |
| Firmware & Software | | | | | | | | |
|  | | RTL pass | SYN pass | | | Execution time(ns) | | |
| Prog 0 | |  |  | | |  | | |
| Prog 1 | |  |  | | |  | | |
| Prog 2 | |  |  | | |  | | |
| Prog 3 | |  |  | | |  | | |
| Prog 4 | |  |  | | |  | | |
| Prog 5 | |  |  | | |  | | |
| Prog6 | |  |  | | |  | | |
| Superlint(number of inline messages) | | | | | | | | |
| Total lines | | Warning | Error | | | coverage(%) | | |
|  | |  |  | | |  | | |

Table1. Summary of HW1

Write Your Text Summary Here: