CSE315: Microprocessors, Microcontrollers, and Embedded Systems
Class Test – 2
Student #: **_1705002_____** ***Time: 20 minutes*** Mark: 20

[Instructions: 1) Type your answer in the place after "**Answer:**" below. 2) Then, make a pdf file of it (your answer) and submit that (pdf) in Moodle *in time*. 3) Check and confirm at your own that your submitted file is okay and not corrupted. Grading will be made based on what will be available in Moodle.]

Question:

A system designer is given a task to interface several memory units (DRAM, EPROM, and flash) with an advanced microprocessor. Here, all the memory units need to be organized in banks.

To develop such a design, the system designer has adopted the following –

1. He uses decoders to activate different banks through generating their (i.e., the banks') "Select" control signals by the decoders,
2. He produces separate "Write" signals for the banks, and
3. He produces separate "Read" signals for the banks.

Now, you need to judge the above mentioned points from the following perspectives with all necessary elaborations.

1. Does the design have any flaw from the perspective of accuracy? If so, clearly point that (those) out.
2. Does the design have any flaw from the perspective of efficiency? If so, clearly point that (those) out.

In case you think that there is no flaw (in either or both the perspectives) in the design, you need to explicitly mention that (those). Unless you explicitly mention anything, your answer will be treated as a blank answer in the corresponding part.

Answer:

Answer to Q-1:

Same read signals suffices different memory banks. However, if separate read signals are generated accurately, the design might work as well. Hence, it **cannot** be concluded that the design have any flaw from the perspective of accuracy.

Answer to Q-2:

It **can** be concluded that the design have flaws from the perspective of efficiency.

To interface memories with wider address buses, two techniques are commonly used:

1. Separate bank decoders: uses separate decoders and is costly, but can be energy efficient.

2. Separate write signals: uses PLD to generate write signals for different banks. This option is cheaper and thus, widely used.

In this given design, the designer combines the two methods, which is definitely redundant. Either option 1 or option 2 would suffice. The choice is dependent on priority. To be cost efficient, option 2 (separate write signals) has to be used and to be energy efficient, option 1 (separate bank decoders) might be used. However, since design efficiency is often sought, option 1 is the default choice.

It is not clear why separate read signals are needed, since microprocessors can read wider data and scrap the irrelevant part later. Typically, ~RD is used as the read signals across memory devices. Using so would also increase design efficiency.