Supplementary Online Material

Appendix A. Thermal Modeling and After-pulsing

Our model can include the effects of thermal relaxation in the superconducting state in certain circumstances, at least qualitatively. This physical process can result in after-pulsing of SNAP detectors. Because the critical current is suppressed by the elevated temperature in the superconducting state, current in the nanowire can exceed the critical current, resulting in a second switching event into the normal phase, occurring without a corresponding photon absorption event.[30]

In a one-dimensional electro-thermal model of superconducting nanowire, the time-space-dependent heat equation is:

$$J^2\rho + \kappa\frac{\partial^2 T}{\partial x^2} - \frac{h_\mathrm{c}}{d}\left(T - T_\mathrm{S}\right) = c\frac{\partial T}{\partial t} \tag{A.1}$$

where J is the current density. However, SPICE cannot integrate this partial differential equation directly. Here, we describe some assumptions and approximations that we used to simplify the equation into one that was easily solved in SPICE.

First, we assumed that the normal region of the resistive wire was uniform in temperature. This assumption was justified because the cooling along the length of the nanowire (the second term on the left hand side of the above equation) only affects the temperature significantly at the beginning of the heating process, when the resistive region is at its shortest and the current in the nanowire is at its highest. We were thus able to remove this term and instead include this effect phenomenologically as a reduction of Joule heating by a dividing scaling factor β. With this simplification, the temperature in equation (A.1) became only time dependent and can be written as:

$$\frac{J^2\rho}{\beta} - \frac{h_\mathrm{c}}{d}\left(T - T_\mathrm{S}\right) = c\frac{\partial T}{\partial t}. \tag{A.2}$$

First-order differential equations of this form can be integrated in SPICE by mapping them into the form of the time evolution of a first-order circuit, which we call the pseudo-circuit. In our case, we use an RC pseudo-circuit connected in parallel with a current source I. The circuit equation we used was:

$$I - \frac{v_\mathrm{c}}{R} = C\frac{dv_\mathrm{c}}{dt}, \tag{A.3}$$

where R is the resistance of a thermal pseudo-resistance and v_c is the pseudo-voltage across the thermal pseudo-capacitor with capacitance C.

Then, we changed the heat equation into a SPICE-calculable format, namely

$$\frac{J^2\rho}{\beta} + \frac{h_c}{d}T_S - \frac{T}{(d/h_c)} = c\frac{\partial T}{\partial t}. \tag{A.4}$$

Comparing equations (A.3) and (A.4), the heat equation can be represented in a circuit language by writing

$$I = \frac{J^2\rho}{\beta} + \frac{h_c}{d}T_S, \tag{A.5}$$

where $R = d/h_c$, and $C = c$. This model allowed us to estimate the hottest temperature in the nanowire after it has returned to the superconducting state. To determine whether I_{sw} is then exceeded, we need to use the phenomenological expression for I_{sw} presented in [8] of

$$I_{sw}(T) = I_{sw}(0)\left(1 - \left(\frac{T}{T_C}\right)^2\right)^2$$

where $I_{sw}(0)$ is the switching current of the nanowire at 0 K, and can be derived from the critical current of the nanowire measured at the bath temperature.

By using this approach, we were able to replicate in simulation the known after-pulsing effect[30]. However, we discovered that the behavior was somewhat sensitive to the choice of the β fitting parameter (which ranged from 2-5 for the test situations we examined). We have not made a rigorous comparison of this approach to experimental performance, and we believe a more thorough distributed treatment of heating effects may be worthwhile to accurately deal with such effects.

We studied a configuration that exhibited after-pulsing for two device configurations. When the kinetic inductance of the nanowire was set to 100 nH, a small peak appeared during the recovery. When the reset time of the nanowire was reduced by reducing its kinetic inductance to 20 nH, the slower thermal relaxation caused several trigger events after photon detection and finally pushed the nanowire into a latched state. Without including this thermal relaxation effect, the nanowire did not latch in this situation. However, we determined that this behavior was extremely sensitive to the choice of model parameters, and were not able to verify the parameters against experimental results. More work is thus needed in order to be able to rely on the models in this situation.

Appendix B. Removing Divergence in the Electrothermal Model

The phenomenological electrothermal model used throughout this paper and described in equation (3) is only valid when the denominator is real, i.e. when $\psi i^2/I_{sw}^2 > 1$. The expression thus cannot be used in SPICE, because continuity is broken at $i = i_{pole} = I_{sw}/\sqrt{\psi}$. This model also cannot accommodate currents less than i_{pole}, and thus we have to find a substitute expression that more realistically models the low-current behavior of the hot-spot.

To accommodate this practicality, we modified equation (3) by using an arbitrary small offset δ in the denominator and took the real part of the square root. The resulting alternative expression to (3) is

$$\frac{\mathrm{d}l_n}{\mathrm{d}t} = v_0 \frac{(\psi \frac{i^2}{I_{\mathrm{sw}}^2} - 2)}{\sqrt{((\psi \frac{i^2}{I_{\mathrm{sw}}^2} - 1) + |\psi \frac{i^2}{I_{\mathrm{sw}}^2} - 1|)/2 + \delta}}, \tag{B.1}$$

where δ is real and $\delta << 1$. This correction closely approximates equation (3) when $\psi i^2/I_{\mathrm{sw}}^2 > 1$, but is continuous and monotonically decreasing through $\psi i^2/I_{\mathrm{sw}}^2 \leq 1$.

From the electrothermal model, the hot-spot resistance $R_{\mathrm{hs}} = R_{\mathrm{SH}} l/w$ decreases rapidly when the current along the wire drops below I_{hs}. The typical temporal profile of $R_{\mathrm{hs}}(t)$, is asymmetric (faster on the falling edge than the rising edge). By choosing δ to be too large in equation (B.1), the collapse speed of the hot-spot can be reduced. If δ is chosen to be less than 0.01, the cooling rate converges to a sharp drop-off. The rapid cooling is essential to preventing the nanowire from latching, but it is important to realize that δ is purely a convenience necessary to ensure convergence of the model, and that it has no physical meaning within the context of the work presented here.

Appendix C. SNAP Simulations

SNAPs are parallel arrays of nanowires that can be used to provide similar performance to standard SNSPDs, but with larger signal voltages[44] and reduced reset times,[45] making readout easier and improving performance in certain applications. However, the devices must be appropriately biased and choked (with inductors) to realize ideal performance, and even then they can be subject to non-idealities. We replicated basic SNAP operation and observed some characteristic behavior of these systems.

A 4-SNAP consists of four parallel nanowires configured so that a photon arrival in one wire will, under the correct bias conditions, cause hot-spots to form across all four nanowires. The resulting increased diverted current to the load results in an increased signal level, which is one of the key advantages of the SNAP architecture.

Using these SPICE models, we confirmed the basic operation of a 4-SNAP circuit and the increased output signal with appropriate choke inductor and a simple 50 Ω load resistor.

The basic schematic and results for the simulation are shown below:

Figure C2 illustrates that the simulated SNAP showed amplitude scaling linearly with the number of SNAP components as expected.

We then investigated some more subtle effects associated with SNAPs. When the bias current was below the device avalanche current, we observed reduced-amplitude pulses that correspond to feed-through to the load from partial firing events. This undesirable behavior correctly reflects one of the key concerns in 4-SNAP design and testing.

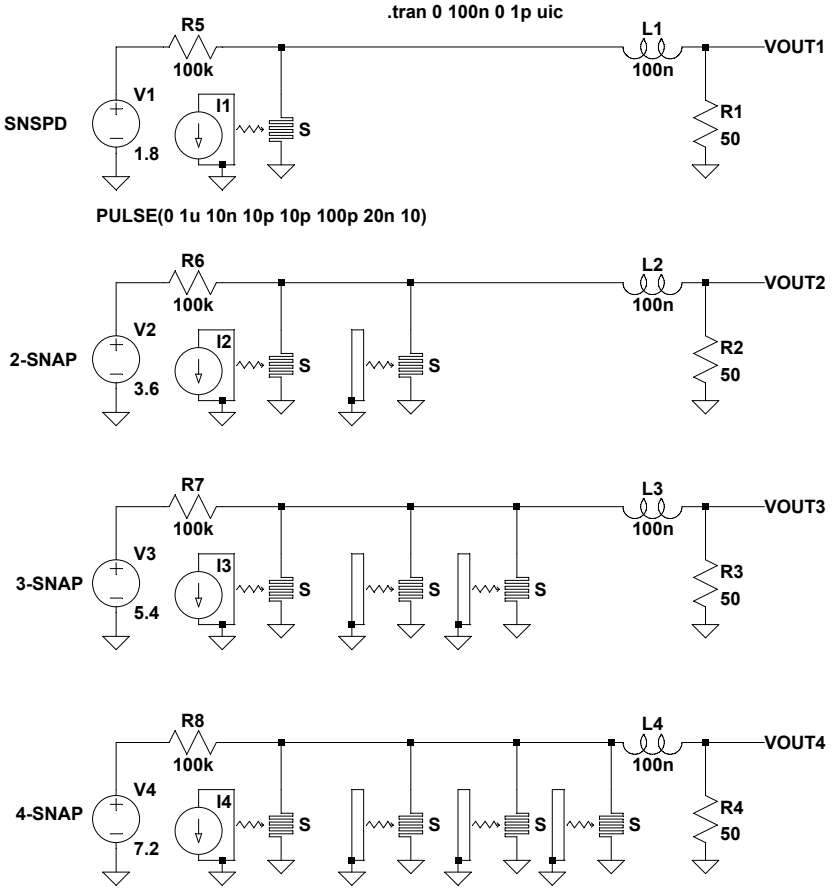

Figure C1. Schematic diagram showing basic SNSPD circuit and various SNAP configurations. 100 nH choke inductors and 50 Ω resistors were used on the output. The nanowires had 20 µA critical currents and the voltage sources included 100 kΩ series resistors in series, thus providing increasing bias currents in steps of 18 µA.

Appendix D. 4-Element Photon-Number-Resolving-Detector Test

In recent work, a variety of approaches for photon-number-resolving (PNR) detectors using SNSPDs that require complex circuit architectures have been proposed[46, 47]. In this section, we attempt to simulate one of these schemes [47], to show the utility of the model for exploration and discovery of novel applications. We suggest that the existence of this model could greatly simplify the search for such architectures in the future.

The circuit schematic for the desired scheme is shown below in fig. D1. It consists of a stack of SNSPDs, each of which has a resistor in parallel with it. When the device fires, a voltage pulse is generated which is observed at the output. Because the various

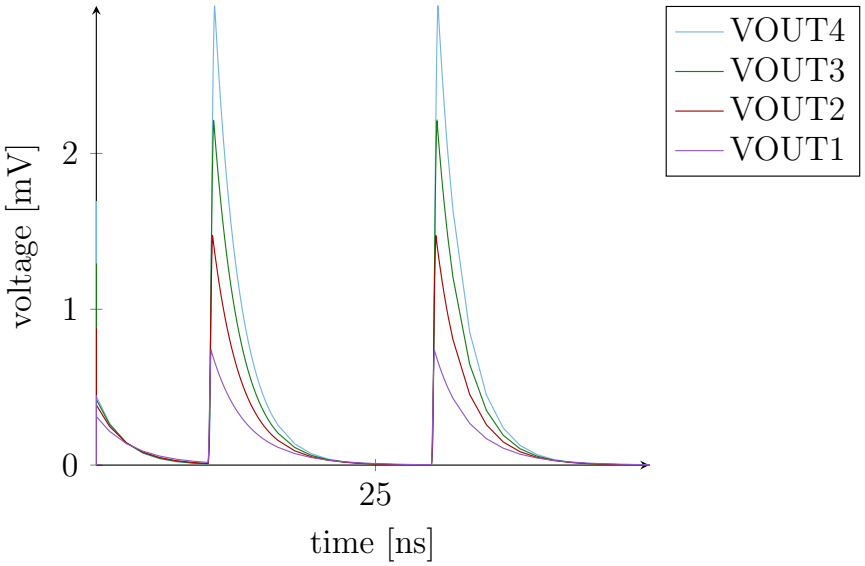

Figure C2. Voltage in 50 Ω output resistor for various SNAPs (2-, 3-, and 4-) relative to an SNSPD in a similar circuit environment. A 100 nH choke inductor was used to prevent latching. The full dynamic model was used with the following parameters for this simulation:$I_{sw} = 20\,\mu A$; bias current $i = 18\,\mu A$ via a 1.8 V voltage source in series with a 100 kΩ resistor. $L_\circ = 50\,nH$; $w = 100\,nm$; $d = 4\,nm$; $h_c = 50.000\,W/m^2K$, $\kappa = 0.108\,W/mK$; $c = 4400\,J/Km^3$; $R_{SH} = 400\,\Omega/\square$, $T_{sub} = 2\,K$; $T_C = 10.5\,K$.

detectors operate approximately independently, the voltage pulses will sum if multiple photons are incident simultaneously.

In fig. D2, we show the simulated output of the circuit. The pulse amplitude corresponds exactly to what is expected in terms of pulse amplitude, with pulse amplitude increasing linearly with number of detectors firing.

Appendix E. Effect of High Count Rates on Shifting Detector Bias Point

We have simulated the effect of back-bias current coming from discharge of a capacitive load, and observed that it lead to latching of the device, or at least a requirement to lower the DC bias current. This effect is discussed further in the main text. Here we provide the circuit model and the observed detector operation.

Appendix F. SPICE Material

We provide here the SPICE code containing the relevant models. Additional online files (including symbol files and examples) are available from `https://github.com/karlberggren/snspd-spice` as well as in the online-supplementary media files attached to this document.

```
** SNSPDLibrary **

* This library contains subckts and
```

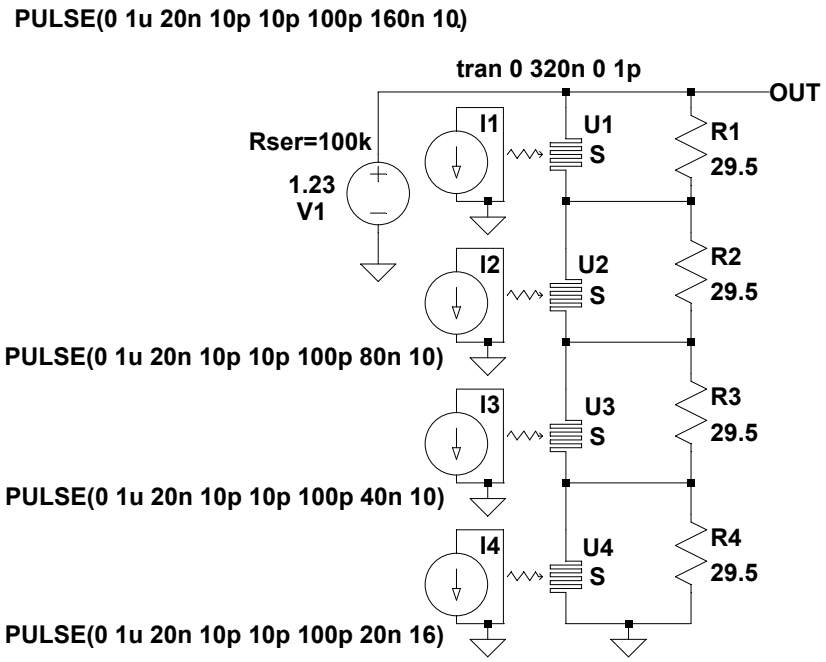

Figure D1. Electrical schematic showing architecture of a 4-element photon-number-resolving detector based on SNSPDs as described in [47]

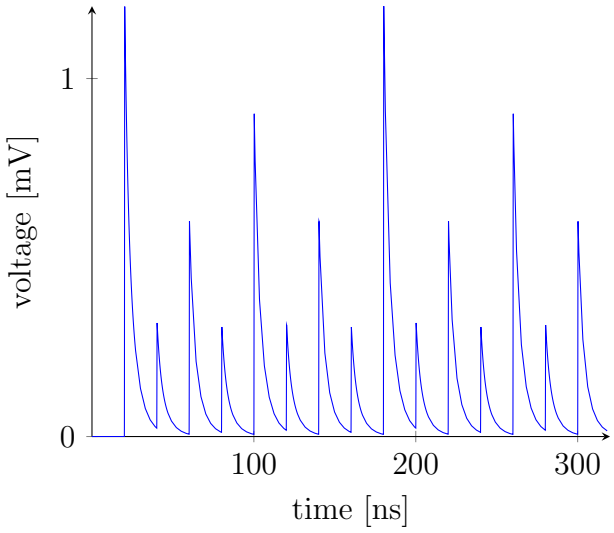

Figure D2. Plot of output voltage vs. time for photon sequence described above. Incident photon pattern was 4,1,2,1,3,1,2,1,4,1,2,1,3,1,2,1, as reflected in the pulse amplitudes.

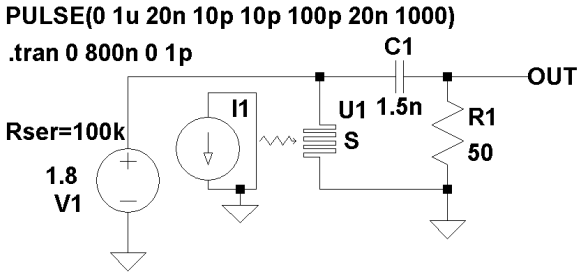

Figure E1. Schematic diagram showing the circuit used for simulating the effect of a capacitive load. The detector has a 100 nH inductance and a 20 µA critical current.

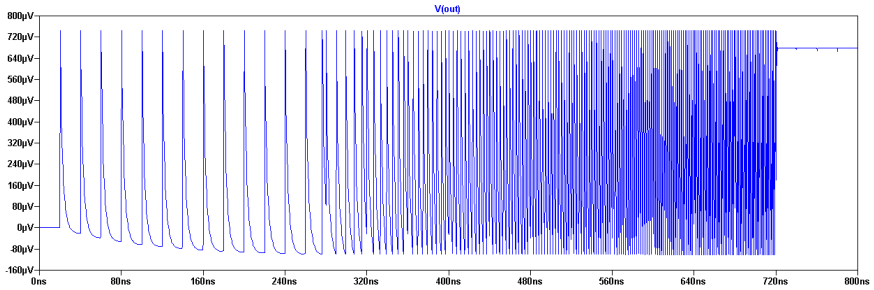

Figure E2. Plot of voltage at ouput as a function of time. Photons arrive every 20 ns, however soon after the start of photon arrival, the mean bias level shifts due to back-biasing from the capacitor. At that point the detector starts to become overbiased and relaxation oscillations begin. Eventually the device latches. This effect is routinely observe experimentally at high photon count rates in detectors.

```
* parameters needed to model an
* snspd. Specifically there are two
* nanowire models that simulate the
* superconducting nanowire's physical
* response to a photon.
*
* The nanowireBCF (Basic Curve Fit)
* model uses a group of switches
* parallel to a variable resistor
* to trace the i-v and pulse
* curves of a nanowire.
*
* The nanowireDynTherm (Dynamic Thermal)
* model uses sets of ancillary circuits to
* calculate and simulate the behavior
* of a nanowire. Each subcircuit is
* embedded into an snspd subcircuit that
* uses current pulses to simulate the
* arrivals of a photons.
```

```
************************************
* nanowireBCF                      *
*   basic curve-fitting-based model *
*   of a nanowire                  *
* gate: 1 uA in 2 ps pulse=photon  *
*   only connect to current source *
* drain: one terminal of channel   *
* source: other terminal of channel *
************************************

.subckt nanowireBCF gate gatereturn drain source
+Lind=100n Isw={Jc*width*thickness*C}
+width=100n thickness=4n sheetRes=400
+Tc=10.5 Tsub=2 Jc=50G C=1
  *Jc at T=Tsub in units of amps/m2
  *sheetRes has units of ohms/sq
  *Tc is critical temp and has units of K
  *Tsub is substrate temp and has units of K
  *C is constrition factor

*Dimensions
.PARAM length={width*Lind/inductivity}
.PARAM squares={length/width}

*Thermal Parameters
.PARAM kappa = 0.108
  * thermal conductivity
  * in W/m K
.PARAM heatCapacity = 4400
  * heat capacity per unit
  * volume in J/m^3 K
.PARAM hc = 50k
  * hc is the thermal conductivity
  * of the surface, units of W/m^2 K

*Electrical/Superconducting Parameters
.PARAM inductivity = {1.38p*sheetRes/Tc}
  * units of H/square
.PARAM  minSquares = 1
  * # of squares for min resistance
.PARAM maxSquares = 4
  * units of ohms/square
```

```
.PARAM psi={sheetRes*(Jc*thickness)**2
+/(hc*(Tc-Tsub))}
  * psi is the Stekly parameter.
.PARAM f={sqrt(2/psi)*.76}
  * quantify hysteresis of Ihs vs Isw
.PARAM Ihs={f*Isw}
  * hotspot current level

*Unitless Parameters
.PARAM gain={10}
  * factor photon signal gets multiplied by
.PARAM epsilon = {0.05}
  * provides margins for switching

** MAIN CIRCUIT **

* channel Inductor
L1 drain N1 Flux=({Lind}/(2.0*cos(0.67*
+asin(0.6*x/{Isw}))-1))*x Rser = 1e-100

* photodetection-event current sensor
V1 N1 N2 0

* photodetection current gain
B2 N2 N1 I=IF(I(V1)>0,10*I(R3),-10*I(R3))

* hotspot plateau current source
B1 N2 source I=IF(v(n2,source)>0,Ihs,-Ihs)

* hotspot limiting resistor
R2 N2 source {maxSquares*sheetRes}

* gate input resistor
R3 gate gatereturn 1

* current sense switch, detects photon arrival
W1 N2 N3 V1 currentSwitch OFF
W2 N3 N4 V1 negCurrentSwitch ON
  * starts in off state (short)
.PARAM hiIthresh = {Isw}
.PARAM loIthresh = {Isw*(f+epsilon)}
.model currentSwitch CSW(Ron=1e9 Roff=.01
```

```
 +It={(hiIthresh+loIthresh)/2}
 +Ih={(hiIthresh-loIthresh)/2})
.model negCurrentSwitch CSW(Ron=.01 Roff=1e9
 +It={-(hiIthresh+loIthresh)/2}
 +Ih={(hiIthresh-loIthresh)/2})

* voltage sense, prevents instant reset
S1 N4 N5 N2 source voltageSwitch OFF
S2 N5 source N2 source negVoltageSwitch ON

.PARAM Vthresh={minSquares*sheetRes*Ihs}
.model voltageSwitch SW(Ron=1e9 Roff=.01
+Vt={Vthresh} Vh=0)
.model negVoltageSwitch SW(Ron=.01 Roff=1e9
+Vt={-Vthresh} Vh=0)
.ends nanowireBCF

************************************
* nanowireDynamic                  *
*   full dynamic model of nanowire  *
* gate: 1 uA in 2 ps pulse=photon   *
*   only connect to current source  *
* drain: one terminal of channel    *
* source: other terminal of channel *
************************************

.subckt nanowireDynamic gate gatereturn drain
+ source params: Lind=100n Isw={Jc*
+width*thickness*C} width=100n thickness=4n
+ sheetRes=400 Tc=10.5 Tsub=2 Jc=50G C=1
  *Jc at T=Tsub in units of amps/m2
  *sheetRes has units of ohms/sq
  *Tc is critical temp and has units of K
  *Tsub is substrate temp and has units of K
  *C is constriction factor

*Dimensions
.PARAM length={width*Lind/inductivity}
.PARAM squares={length/width}

*Thermal Parameters
.PARAM kappa = 0.108
```

```
  * thermal conductivity W/m K
.PARAM heatCapacity = 4400
  * heat capacity J/m^3 K
.PARAM hc = 50k
  * thermal conductivity of surface W/m^2 K

*Electrical/Superconducting Parameters
.PARAM inductivity = {1.38p*sheetRes/Tc}
  * H/square
.PARAM  minSquares = {1/sheetRes}
  * # squares for minimum resistance
.PARAM Rnorm = {sheetRes*squares}
  * units of ohms/square
.PARAM psi={sheetRes*(Jc*thickness)**2/
+(hc*(Tc-Tsub))}
  * psi is the Stekly parameter.
.PARAM vo={sqrt(hc*kappa/thickness)/
+heatCapacity}
  * vo is characteristic velocity

.PARAM Ihs={sqrt(2/psi)*Isw}
.PARAM Vthresh={minSquares*sheetRes*Ihs}
.PARAM rho={sheetRes*thickness}

*Unitless Parameters
.PARAM gain={10}
  * factor photon signal gets multiplied by
.PARAM delta={0.005}
  * a small offset value for avoiding
  * singularity in hotspot velocity

** MAIN CIRCUIT **

*channel inductor
L1 drain N1 Flux=({Lind}/(2.0*cos(0.67*
+asin(0.6*x/{Isw}))-1))*x Rser = 1e-100

* hotspot resistor
B1 N1 source V=(v(N3)+abs(v(N3)))/2*i(L1)
  * v(N3) is resistance of hotspot

* hotspot limiter
```

```
R1 N1 source {Rnorm}
  * prevents channel resistance from
  * increasing without bound

*photon arrival sense resistor
R3 gate gatereturn 1e-100

** S/C SENSE SUBCIRCUIT **

**Superconducting to Resistive Transition

*dependent source used to store state
B2 N2 0 V=if((abs(i(L1))>Isw-gain*
+abs(i(R3)))|(abs(v(N1)-v(source))>{Vthresh}),1,0)
R2 N2 0 1
  * v(N2) is 0 if wire s/c, 1 if not

** HOTSPOT GROWTH INTEGRATOR SUBCIRCUIT **

*dependent current source that represents
*hotspot S-N boundary velocity
B3 0 N3 I=if(v(N2),(psi*(i(L1)/Isw)**2-2)
+/((sqrt(((psi*(i(L1)/Isw)**2-1)+abs(psi*
+(i(L1)/Isw)**2-1))/2)+delta)),0)

*capacitor that integrates hotspot velocity
C1 N3 0 {(width)/(2*sheetres*vo)}
  * hotspot resistance is v(N3)

*switch that shorts capacitor to ground when
*superconductivity is restored
S1 N3 0 N2 0 Srestore OFF
.model Srestore SW(Vt={0.5V} Roff=1m Ron=10G)

.ends nanowireDynamic
```

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