LOGIC FAMILY COMPATIBILITY ASSIGNMENT

The lecture on Wednesday February 4th covered digital logic levels as a function of signal voltage. We discussed input and output voltage levels that define HIGH and LOW discrete states. We also covered different logic families and their mutual compatibility. As part of the lecture, we examined the Electrical Characteristics of the 74LS04 Hex Inverter integrated circuit using it's datasheet.

In future lab exercises, we will build circuits using the breadboards and LS family logic devices. We will also be interfacing with those circuits using the LaunchPad GPIO ports. I made some reference to this problem in class on two occasions.

As an exercise, determine the LaunchPad GPIO port compatibility with the LS logic devices using the 74LS04 as a device that is representative of all LS devices we will be using. You will be comparing input and output voltage levels on both devices. Keep in mind that the LaunchPad GPIO ports and the LS logic devices will serve as both input and output devices to each other.

This exercise serves two purposes. First, it offers you an opportunity to practice your understanding of the material presented in Wednesday's lecture and section 1.7 of Digital Design and Computer Architecture. Second, it offers you the opportunity to develop the skill of researching technical material and finding the information you need.

I understand that the LaunchPad data sheet is 1,409 pages in length and the information you want is a needle in that haystack. Fear not! There is a table of contents and the document is searchable. Refer to Understanding and Interpreting Standard-Logic Data Sheets as needed. Your submission must show how you reached your conclusion.

What are the input and output logic levels of the LaunchPad GPIO ports and the LS logic devices? Calculate the input and output Noise Margins for both devices. Note that the LaunchPad GPIO ports min V_{IH} and max V_{IL} are specified as a function of V_{DD}. What assumptions does that require that you make in your compatibility determination.

Your assignment is to reach a determination of logic family compatibility that is either $TRUE$ or $FALSE$ based on information that you will include to support your determination.

Have a lot of fun!

From the 74LS04 datasheet, we can see that V_{OH} and V_{OL} are specified under test conditions of $V_{CC} = 4.75V$. The datasheet also specifies that the maximum V_{CC} is $5.5V$. Since $V_{CC} = 4.75V$ represents the test conditions for which V_{OH} and V_{OL} are valid, we will use $V_{CC} = 4.75V$.

From the datasheet, we can see that the LaunchPad tolerates a range of V_{DD} supply voltages from $3.15V$–$3.63V$. This will affect the input logic $HIGH$ and LOW levels. We do not need to consider either the Min or Max V_{DD} supply voltages since the LaunchPad nominal supply voltage is $V_{DD} = 3.3V$.

The data in Table 1 is taken from Table 24-6 in the LaunchPad datasheet on page 1360. The data in Table 2 is taken from the 74LS04 datasheet Electrical Characteristics table.

Parameter	Parameter Name	Min	Max
V_{IH}	GPIO high-level input voltage	0.65*V_{DD}	$5.5V$
V_{IL}	GPIO low-level input voltage	$0V$	0.35*V_{DD}
V_{OH}	GPIO high-level output voltage	$2.4V$	-
V_{OL}	GPIO low-level output voltage	-	$0.4V$

Table 1: LaunchPad Logic Levels

Parameter	Parameter Name	Min	Max
V_{IH}	High-level input voltage	$2.0V$	-
V_{IL}	Low-level input voltage	-	$0.8V$
V_{OH}	High-level output voltage	$2.7V$	-
V_{OL}	Low-level output voltage	-	$0.5V$

Table 2: 74LS04 Logic Levels

From here I will assume that $V_{DD} = 3.3V$ which is standard CMOS logic supply voltage. Using $V_{DD} = 3.3V$ we can compute the values of V_{IH} and V_{IL} for the LaunchPad as follows:

$$\begin{aligned} V_{IL} &= 0.65 \bullet 3.3V \\ V_{IL} &= 1.155V \end{aligned}$$

$$\begin{aligned} V_{IH} &= 0.65 \bullet 3.3V \\ V_{IH} &= 2.145V \end{aligned}$$

There are two cases to consider. First, the case of the LaunchPad output as input to the 74LS04 device. Second, the case of the 74LS04 output as input to the LaunchPad.

1– First consider the case of the LaunchPad output as input to the 74LS04. See Figure 1 for the logic level diagram for this case.

The noise margins may be computed for the LaunchPad acting as output to the 74LS04 as follows:

$$\begin{aligned} NM_L &= V_{IL} - V_{OL} \\ &= 0.8V - 0.4V \\ NM_L &= 0.4V \end{aligned}$$

$$\begin{aligned} NM_H &= V_{OH} - V_{IH} \\ &= 2.4V - 2.0V \\ NM_H &= 0.4V \end{aligned}$$

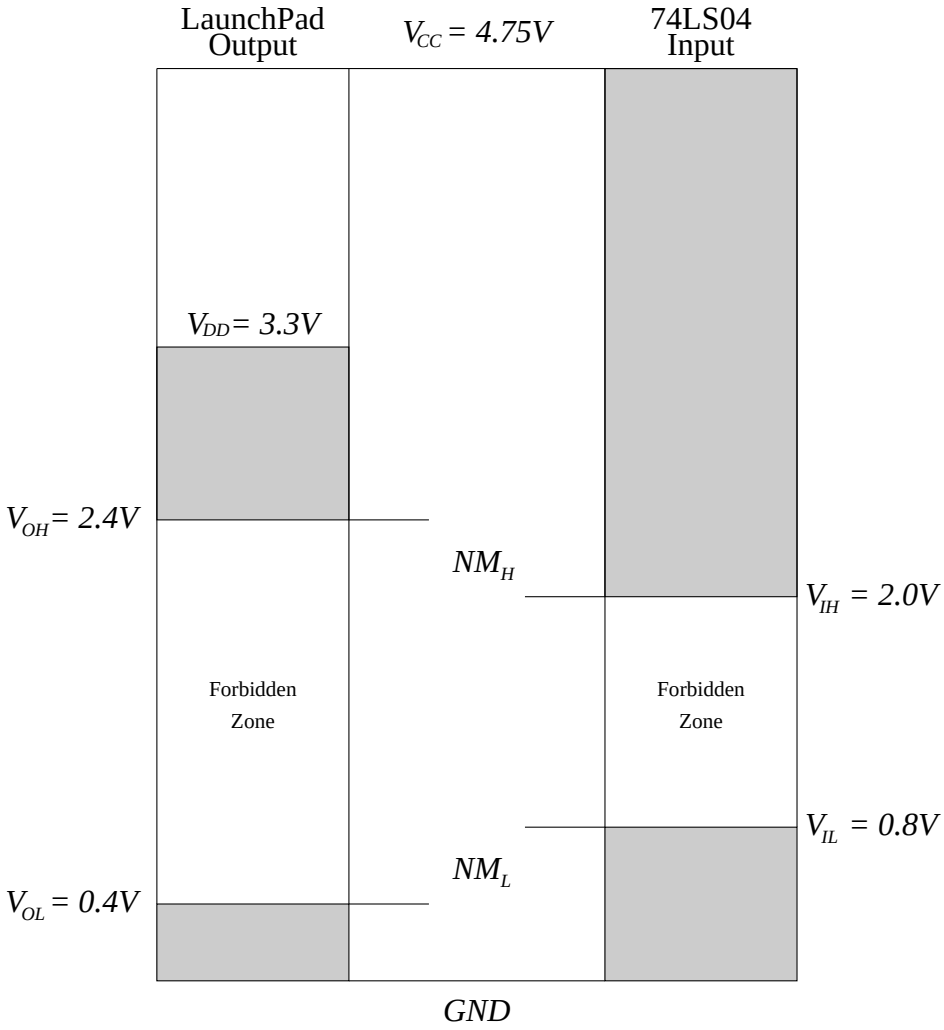


Figure 1: LaunchPad output to 74LS04 input.

Both NM_L and NM_H are positive so the LaunchPad output logic levels are compatible with the 74LS04 input logic levels.

2– Now consider the case of the 74LS04 output as input to the LaunchPad. See Figure 2 for the logic level diagram for this case. The 74LS04 specifies $V_{OL} = 0.4V$ and $V_{OL} = 0.5V$ depending on output current. This calculation will use $V_{OL} = 0.5V$ since that represents the worst case for compatibility.

The noise margins may be computed for the 74LS04 acting as output to the LaunchPad as follows:

$$\begin{aligned} NM_L &= V_{IL} - V_{OL} \\ &= 1.155V - 0.5V \\ NM_L &= 0.655V \end{aligned}$$

$$\begin{aligned} NM_H &= V_{OH} - V_{IH} \\ &= 2.7V - 2.145V \\ NM_H &= 0.555V \end{aligned}$$

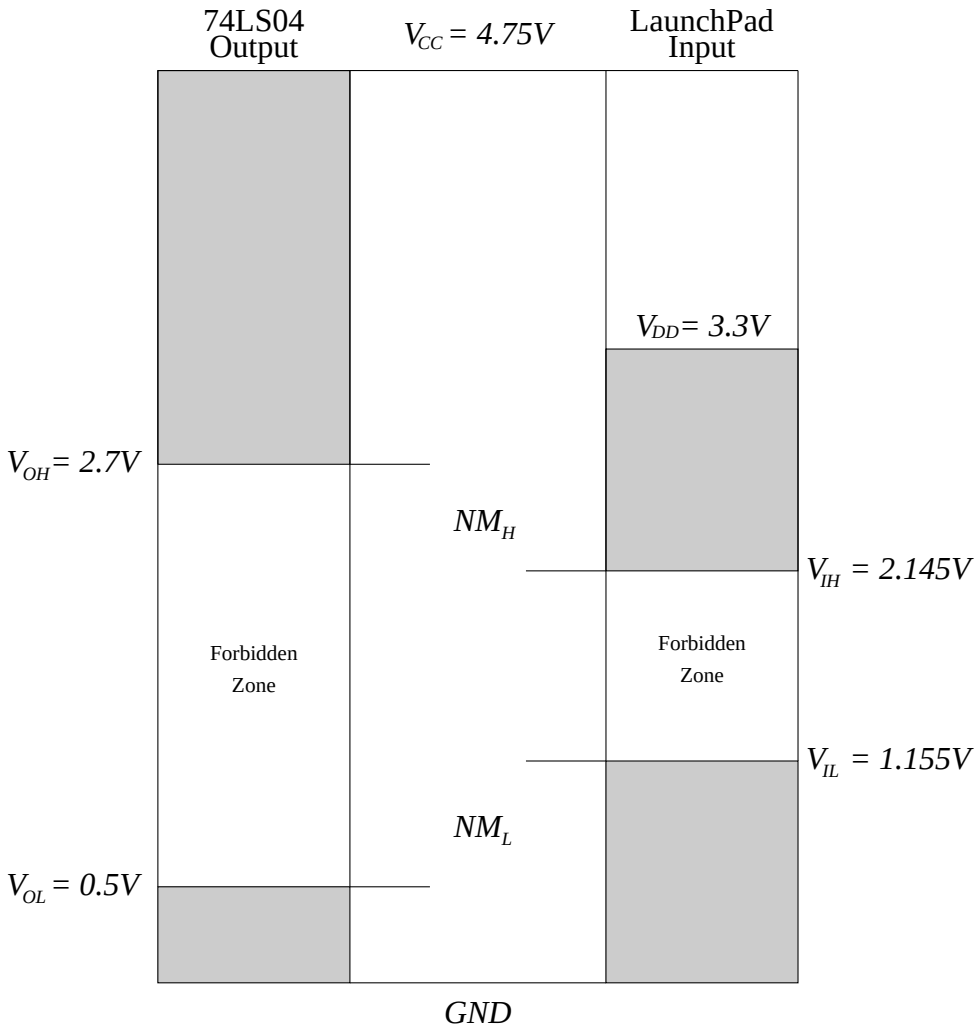


Figure 2: 74LS04 output to LaunchPad input.

Both NM_L and NM_H are positive so the 74LS04 output logic levels are compatible with the LaunchPad input logic levels.

In each case of the LaunchPad and 74LS04 acting as input or output to each other, the noise margins are positive. The input and output levels do not fall into the forbidden zone.

There is more explicit discussion that can take place with respect to whether or not the two logic families are compatible.

Consider case 1 with the LaunchPad as output to the 74LS04 input:

$$V_{OH} = 2.4V > V_{IH} = 2.0V$$
$$V_{OL} = 0.4V < V_{IL} = 0.8V$$

So the LaunchPad output represents valid $HIGH$ and LOW logic levels on the input of the 74LS04

Case 2 is the 74LS04 as output to the LaunchPad input:

$$V_{OH} = 2.7V > V_{IH} = 2.145V$$
$$V_{OL} = 0.5V < V_{IL} = 1.155V$$

Note that in this case, the 74LS04 $HIGH$ output exceeds V_{DD} of the LaunchPad. This is okay because the LaunchPad datasheet specifies that the GPIO pins are tolerant of $5.5V$.

So the 74LS04 output represents valid $HIGH$ and LOW logic levels on the input of the LaunchPad GPIO pins.

Since the LaunchPad and the 74LS04 outputs represent mutually valid logic levels, both logic families are compatible.

24.3 Recommended Operating Conditions

For special high-current applications, the GPIO output buffers may be used with the following restrictions. With the GPIO pins configured as 8-mA output drivers, a total of four GPIO outputs may be used to sink current loads up to 18 mA each. At 18-mA sink current loading, the V_{OL} value is specified as 1.2 V. The high-current GPIO package pins must be selected such that there are only a maximum of two per side of the physical package with the total number of high-current GPIO outputs not exceeding four for the entire package.

Table 24-5. Recommended DC Operating Conditions

Parameter	Parameter Name	Min	Nom	Max	Unit
V_{DD}	V_{DD} supply voltage	3.15	3.3	3.63	V
V_{DDA}	V_{DDA} supply voltage	2.97	3.3	3.63	V
V_{DDC}	V_{DDC} supply voltage	1.08	1.2	1.32	V
V_{DDCDS}[ab]	V_{DDC} supply voltage, Deep-sleep mode	1.08	-	1.32	V

a. These values are valid when LDO is in operation.

b. There are peripheral timing restrictions for SSI and LPC in Deep-sleep mode. Please refer to those peripheral characteristic sections for more information.

Table 24-6. Recommended GPIO Pad Operating Conditions

Parameter	Parameter Name	Min	Nom	Max	Unit
V_{IH}	GPIO high-level input voltage	0.65 * V_{DD}	-	5.5	V
V_{IL}	GPIO low-level input voltage	0	-	0.35 * V_{DD}	V
V_{HYS}	GPIO input hysteresis	0.2	-	-	V
V_{OH}	GPIO high-level output voltage	2.4	-	-	V
V_{OL}	GPIO low-level output voltage	-	-	0.4	V
I_{OH}	High-level source current, V_{OH}=2.4 V[a]				
	2-mA Drive	2.0	-	-	mA
	4-mA Drive	4.0	-	-	mA
	8-mA Drive	8.0	-	-	mA
I_{OL}	Low-level sink current, V_{OL}=0.4 V[a]				
	2-mA Drive	2.0	-	-	mA
	4-mA Drive	4.0	-	-	mA
	8-mA Drive	8.0	-	-	mA
	8-mA Drive, V_{OL}=1.2 V	18.0	-	-	mA

a. I_O specifications reflect the maximum current where the corresponding output voltage meets the V_{OH}/V_{OL} thresholds. I_O current can exceed these limits (subject to absolute maximum ratings).

Table 24-7. GPIO Current Restrictions[a]

Parameter	Parameter Name	Min	Nom	Max	Unit
I_{MAXL}	Cumulative maximum GPIO current per side, left[b]	-	-	30	mA
I_{MAXB}	Cumulative maximum GPIO current per side, bottom[b]	-	-	35	mA
I_{MAXR}	Cumulative maximum GPIO current per side, right[b]	-	-	40	mA
I_{MAXT}	Cumulative maximum GPIO current per side, top[b]	-	-	40	mA

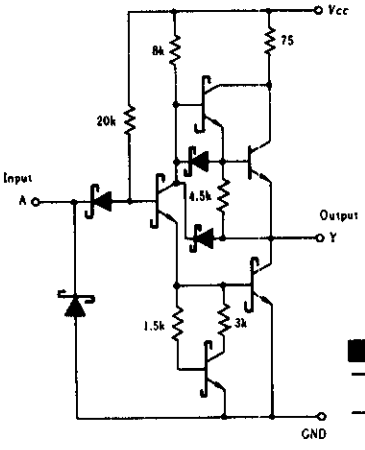
a. Based on design simulations, not tested in production.

b. Sum of sink and source current for GPIOs as shown in Table 24-8 on page 1361.

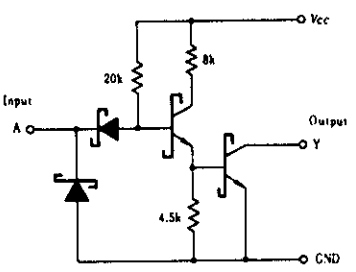
HD74LS04/HD74LS05 ●Hex Inverters ●Hex Inverters (with Open Collector Outputs)

■CIRCUIT SCHEMATIC(1/6)

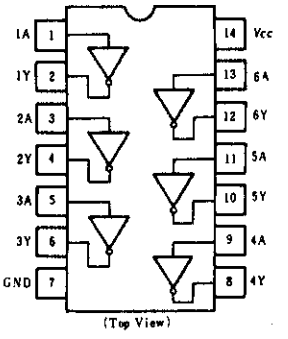
HD74LS04



HD74LS05



■PIN ARRANGEMENT



■HD74LS05 RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
High level output voltage	V_{OH}	–	–	5.5	V
Low level output current	I_{OL}	–	–	8	mA

■ELECTRICAL CHARACTERISTICS ($Ta=-20\sim+75°C$)

Item	Symbol	Test Conditions		HD74LS04			HD74LS05			Unit
				min	typ*	max	min	typ*	max	
Input voltage	V_{IH}			2.0	–	–	2.0	–	–	V
	V_{IL}			–	–	0.8	–	–	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	–	–	–	V
	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$	$I_{OL}=8mA$	–	–	0.5	–	–	0.5	V
			$I_{OL}=4mA$	–	–	0.4	–	–	0.4	
Output current	I_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$		–	–	–	–	–	100	μA
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	–	–	20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	–	–	−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	–	–	0.1	mA
Short-circuit output current	I_{OS}	$V_{CC}=5.25V$		−20	–	−100	–	–	–	mA
Supply current	I_{CCH}	$V_{CC}=5.25V$		–	1.2	2.4	–	1.2	2.4	mA
	I_{CCL}			–	3.6	6.6	–	3.6	6.6	
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	–	–	−1.5	V

* V_{CC}=5V, Ta=25°C

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

Item	Symbol	Test Conditions	HD74LS04			HD74LS05			Unit
			min	typ	max	min	typ	max	
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$	–	9	15	–	17	32	ns
	t_{PHL}		–	10	15	–	15	28	

Note) Refer to Test Circuit and Waveform of the Common Item