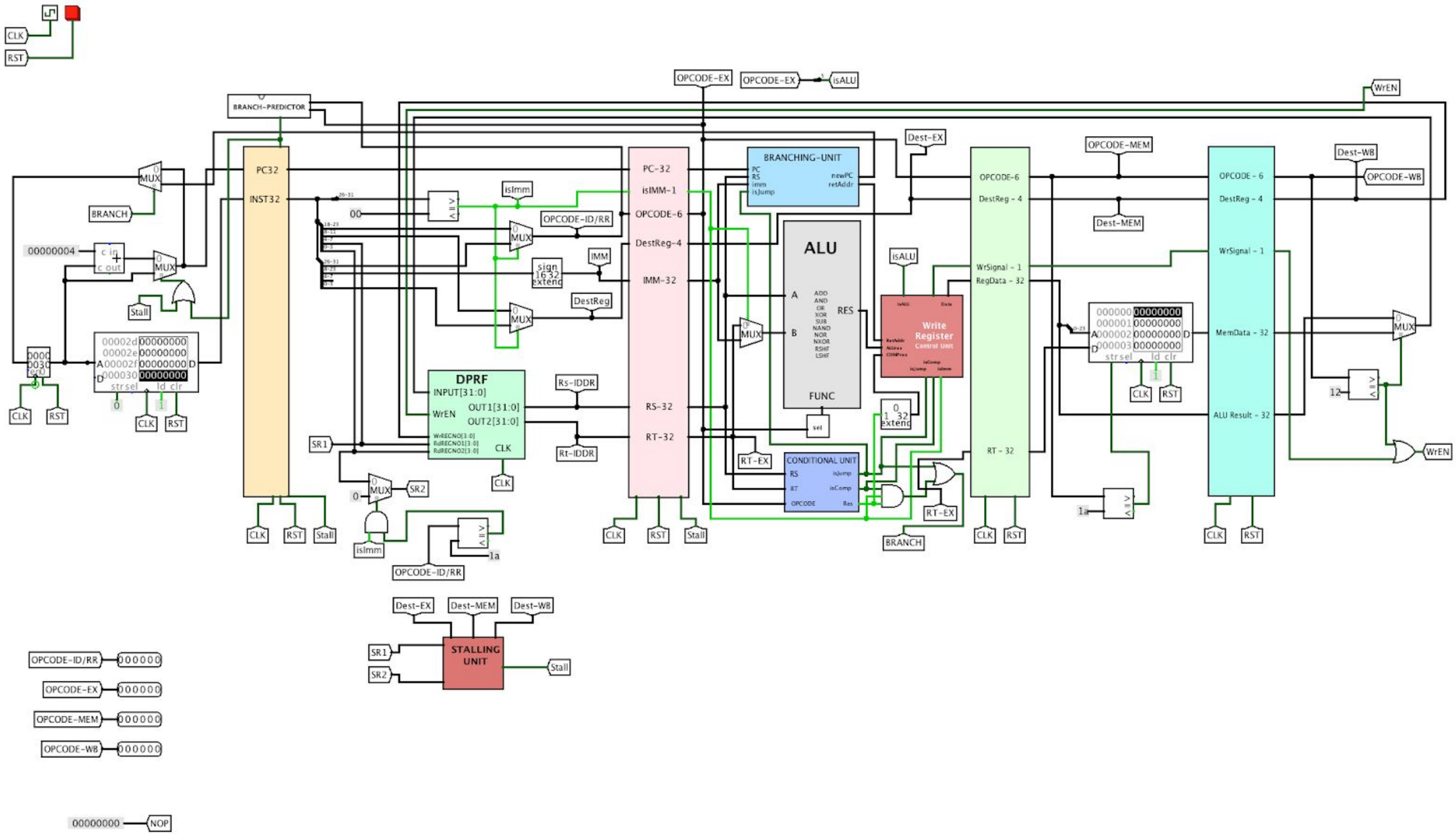
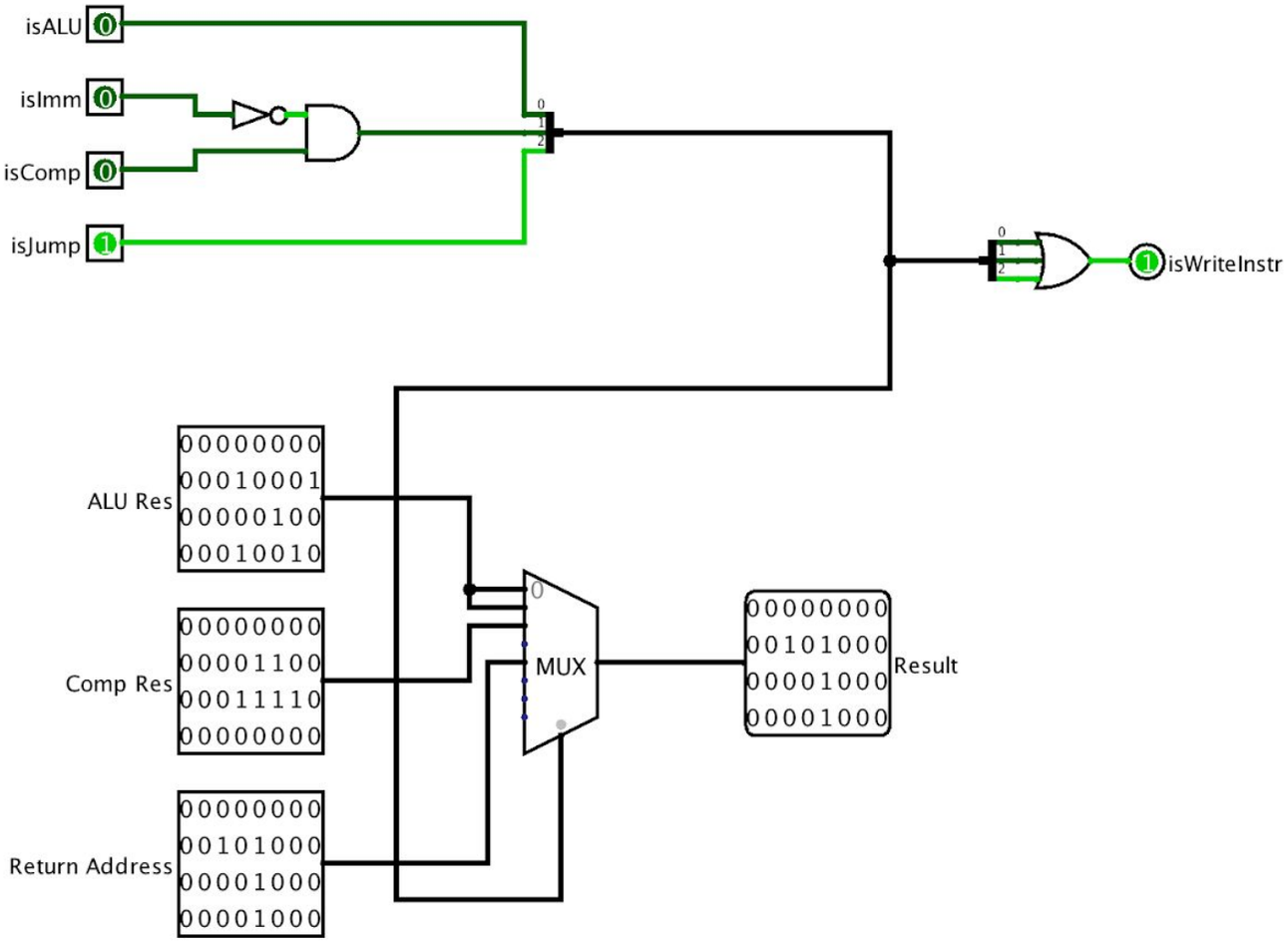
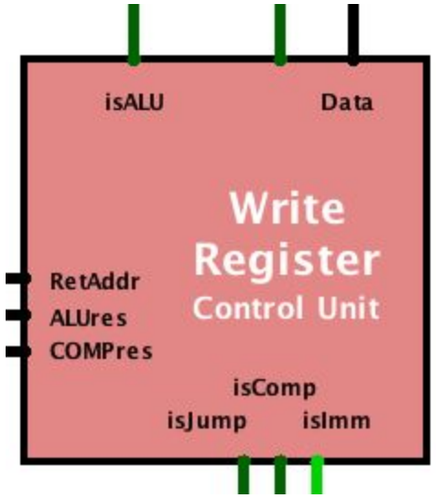

CLK
RST
BRANCH-PREDICTOR
PC32
INST32
BRANCH
00000004
Stall
00002d 00000000
00002e 00000000
A00002f 00000000 D
B000030 00000000
strsel ld clr
PC-32
isIMM-1
OPCODE-6
DestReg-4
IMM-32
RS-32
RT-32
isImm
OPCODE-ID/RR
IMM
DestReg
sign 16 32 extend
Rs-IDDR
Rt-IDDR
SR1
SR2
DPRF
INPUT[31:0]
WrEN
OUT1[31:0]
OUT2[31:0]
CLK
BRANCHING-UNIT
PC
RS
imm
isJump
newPC
retAddr
ALU
A
B
RES
FUNC
ADD
AND
OR
XOR
SUB
NAND
NOR
NXOR
RSHF
LSHF
sel
isALU
Write Register Control Unit
RT-EX
CONDITIONAL UNIT
RS
RT
OPCODE
isJump
isComp
Res
BRANCH
OPCODE-EX
Dest-EX
OPCODE-6
DestReg - 4
WrSignal - 1
RegData - 32
RT - 32
OPCODE-MEM
Dest-MEM
OPCODE - 6
DestReg - 4
WrSignal - 1
MemData - 32
ALU Result - 32
Dest-WB
OPCODE-WB
WrEN
STALLING UNIT
Dest-EX
Dest-MEM
Dest-WB
SR1
SR2
Stall
OPCODE-ID/RR
OPCODE-EX
OPCODE-MEM
OPCODE-WB
000000
NOP
00000000

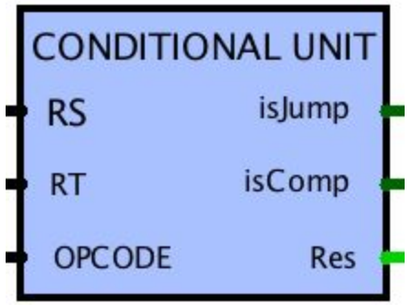
000: ALU | 001: ALU | 010: CompRes | 100: Return Address





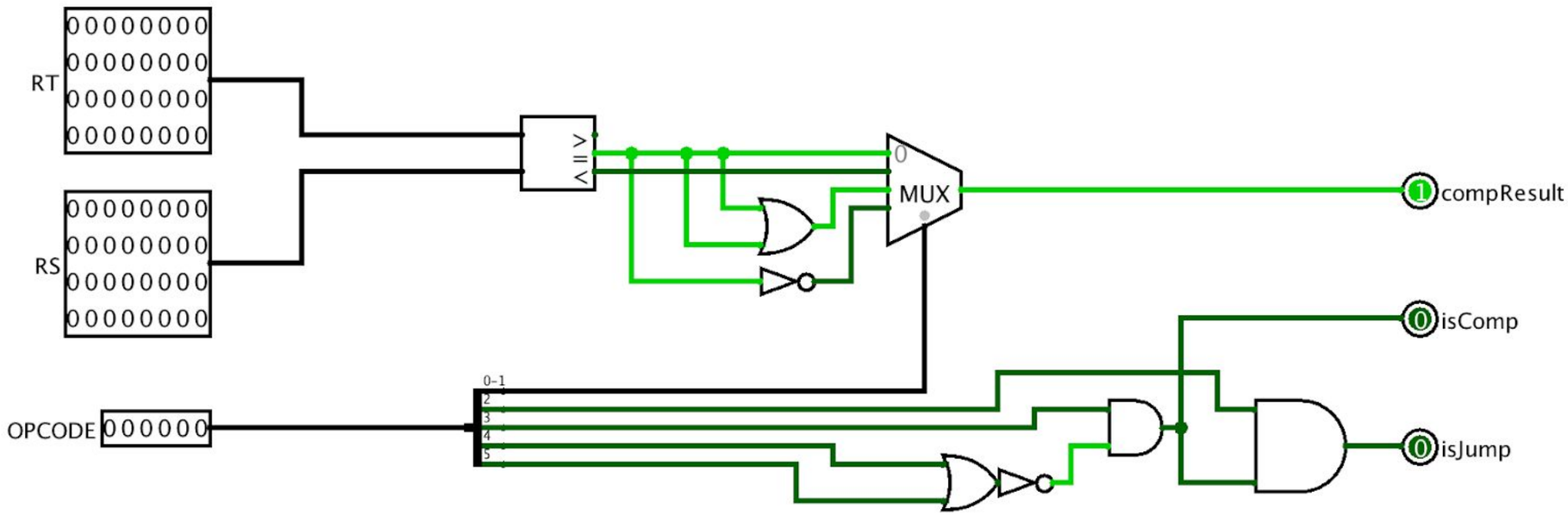
CONTROL UNIT - WRITE REG

Produce a signal when a value must be written to the register as well as the value that will be written depending on the signals isALU, isImm, isComp, isJump



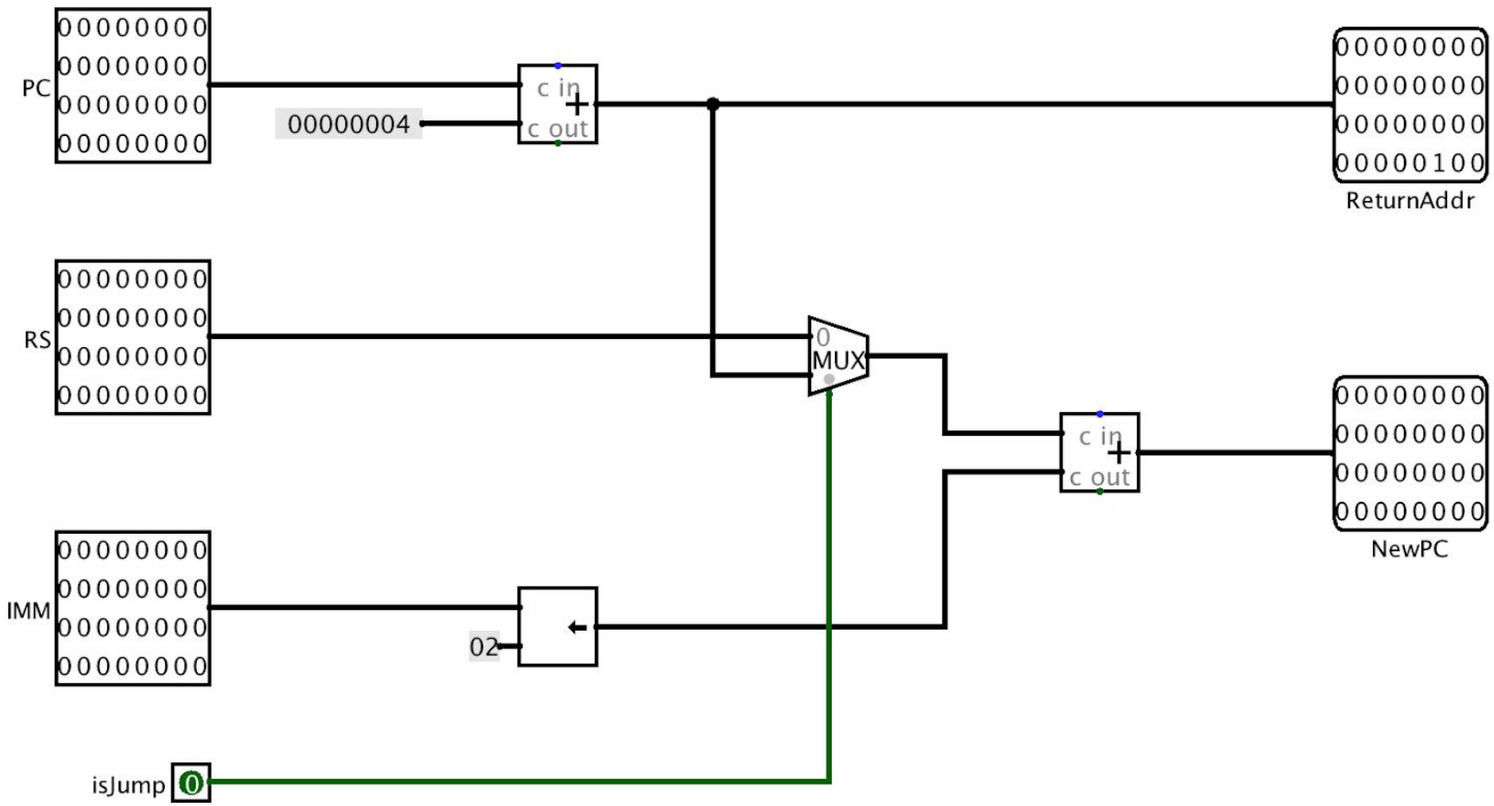
CONDITIONAL UNIT

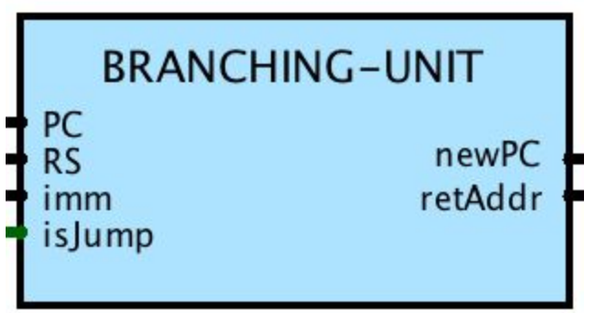
Compute comparison between two values and produce signals: isComp and isJump used in branching and register selection



BRANCHING-UNIT

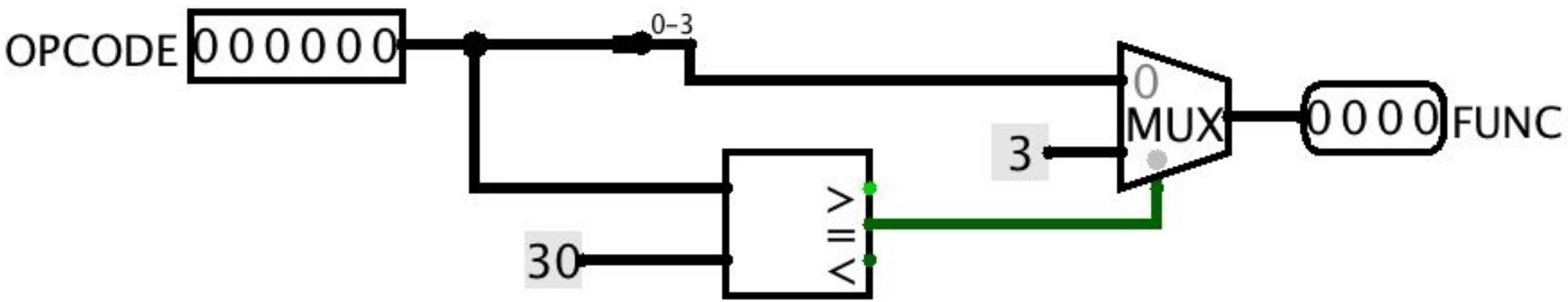
isJump is used to determine the new address of the PC

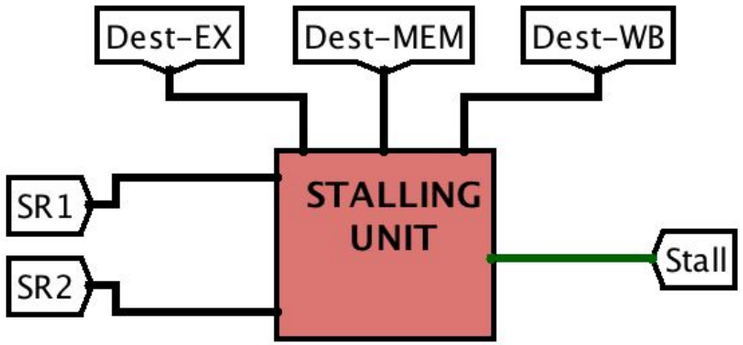


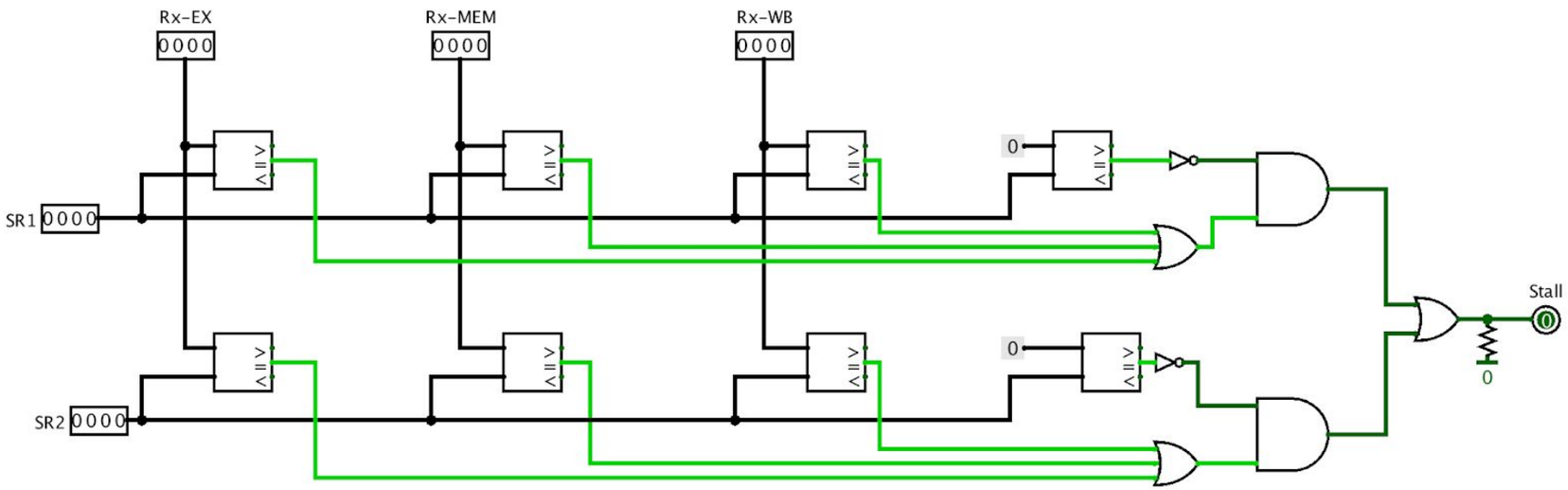


ALU Selector

OPCODE used to find the func of the ALU







STALLING UNIT

Determines if any of the registers needed is being used by any other stage to stall the pipeline