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# Multi-cycle MIPS Processor

In lieu of the final exam for Computer Architecture, a multi-cycle MIPS processor was created in Verilog and tested with a given program, which found the minimum and maximum values of an array. Building off of the components generated in the final project, additional modules were added to recognize and alleviate data hazards that may occur. These modules include a hazard detection unit and a data-forwarding unit along with pipeline registers between each stage.

## Simulation Results

The two figures below show the correct results of the multi-cycle processor including the 182 cycles, a CPI of 1.22, and the correct register values.

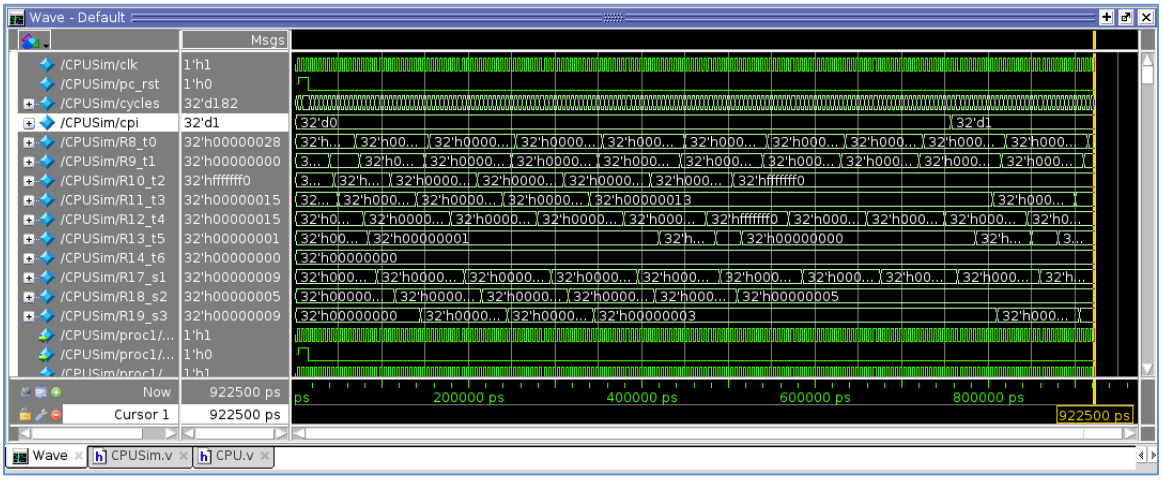


Figure 1 – Waveform screenshot showing 149 cycles and instructions, resulting in a CPI of 1.22. Also shown are the correct register output values at the end of the simulation.

```
// Stop the program if the halt instruction is hit
always@(instr)
begin
        if(instr == 32'hfc000000)
            $stop;
end
```

Figure 2 – Waveform screenshot showing the breakpoint inside of the CPU.v file that occurred when the halt instruction was hit.