Make CPU

Write testbench and simulate with provided program

Calculate CPI using Verilog simulator

Tell TA if we use another simulator

**Testbench**:  
Generator for in the input (reset and clock)

Instance of process defined in cpu.v

Instance of memory module defined in memory.v

Connections amongst them

**Loading the program:**

Image (hexdump) will be read by memory.v into array structure.

PC is 32-bit write-enabled register with asynchronous reset.

When reset is 1, output of PC is set to 0x00003000

**Instructions**:

Add, addi, slt

Beq, j

Lw, sw

Addi:

Modify 2-step ALU control

Add HLT with opcode 0x3f and machine instruction 0xfc000000.

**Other:**

Mux needs to go from 1 bit to 32 bit for inputs and outputs

ALU slt correctly? Signed, not unsigned. Use: reg signed [31:0]

**Submission**:

Zip file to COE server

README plaintext file to say which test bench to simulate and how long

2 page report with final waveform, development process, choice of data structures and implementation of modules, final simulation results (cycles, contents, instructions)

+10 for creating a different test program to load into memory

+? For performance optimizations