DOCUMENT NUMBER AND REVISION
VL-FS-MGLS320240-03 REV. B
(MGLS320240-SILVER)

DOCUMENT TITLE:
SPECIFICATION
OF
LCD MODULE TYPE

MODEL NUMBER: MGLS320240-03

DEPARTMENT	NAME	SIGNATURE	DATE
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DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM	TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
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A	B	2002.12.06	Items 1 to 3 were updated: 1.)(Page 1 & 4) "Preliminary Specification" was changed to "Specification". 2.)(Page 4, table 1) Weight was added. 3.) (Page 9, table 5) Supply voltage (LCD), Supply Current (Logic & LCD), and Supply Current (LCD) were updated.	PHILIP CHENG	Z.B.HE

CONTENTS

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Specification
of
LCD Module Type
Item No.: MGLS320240-03

1. General Description

- 320 x 240 dots STN Mode Positive Silver Reflective LCD Graphic Module.
- Viewing Angle: 6 O'clock direction
- Driving scheme: 1/240 Duty, 1/13.1 bias
- 'SAMSUNG' KS0086TQFP (Flat pack) 80-Channel Column / Segment Drivers or equivalent.
- 4-bit parallel interface mode.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	170.7(W) x 106.4(H) x 13.5 (D)	mm
Viewing area	122.0(W) x 92.0(H)	mm
Active area	115.17(W) x 86.37(H)	mm
Display format	320 (H) x 240 (V)	Dots
Dot size	0.33(W) x 0.33(H)	mm
Dot spacing	0.03(W) x 0.03(H)	mm
Dot pitch	0.36(W) x 0.36(H)	mm
Weight	Approx. 184	Grams

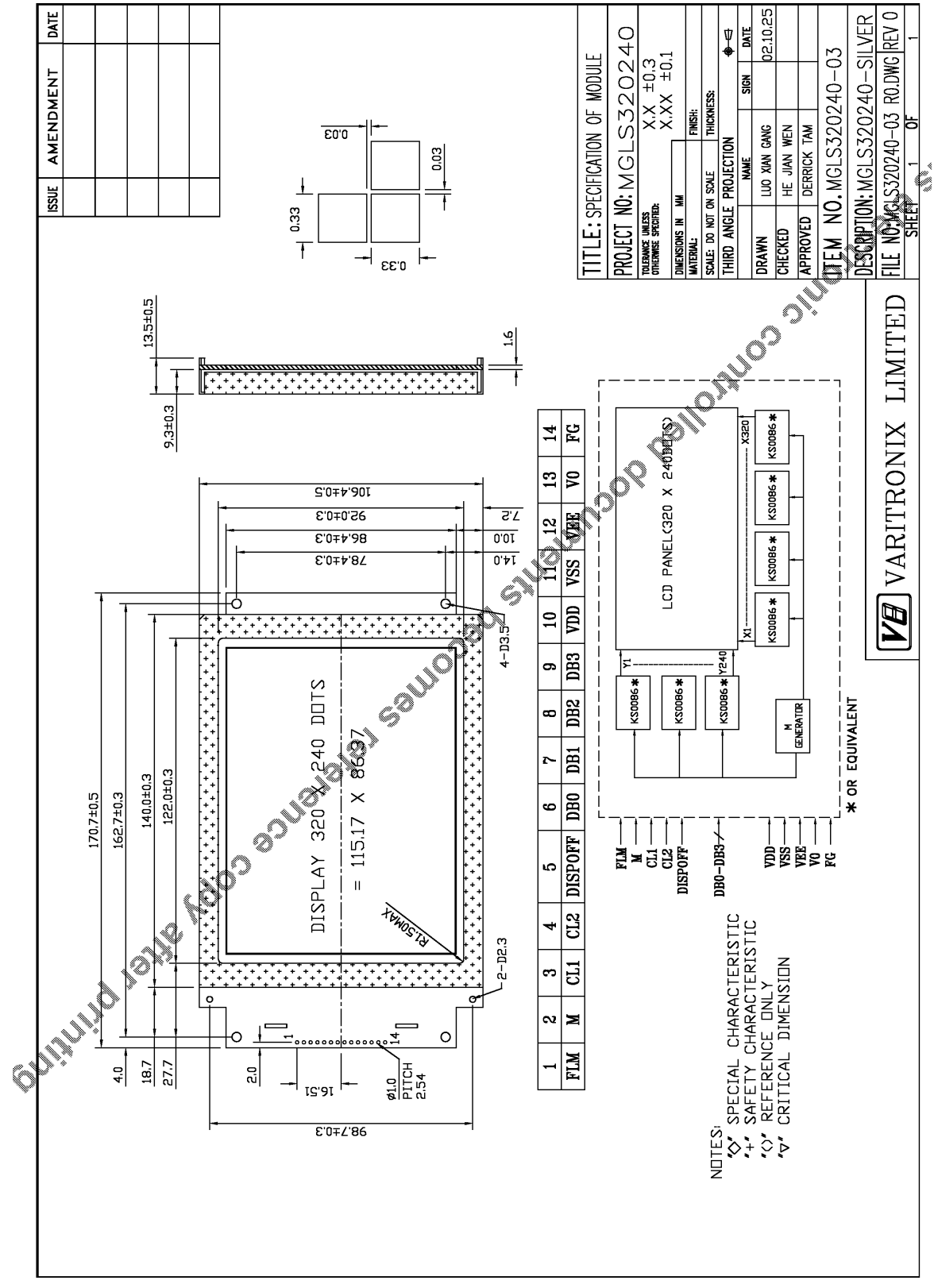


Figure 1: Module Specification

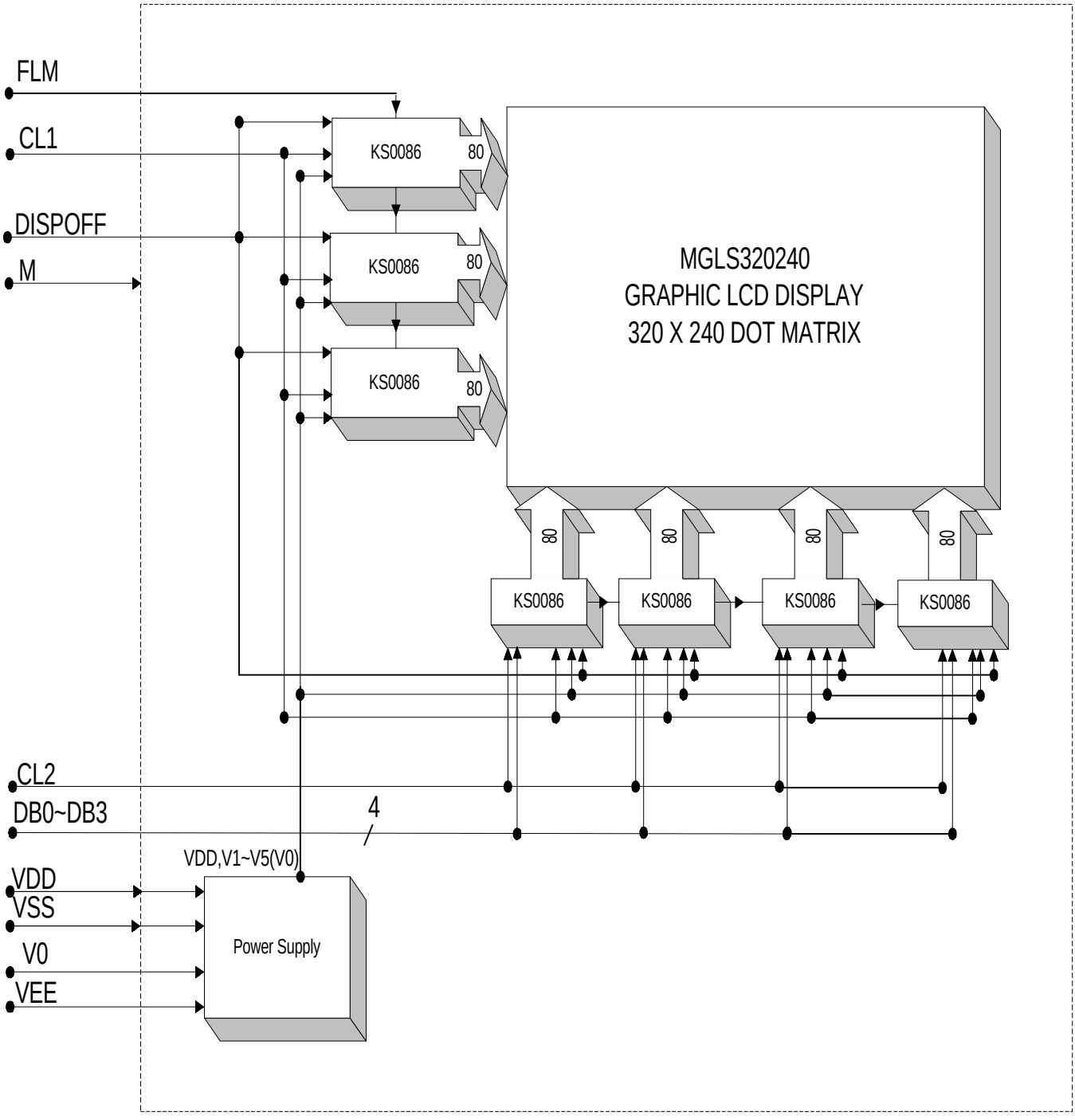


Figure 2: Block Diagram

3. Interface signals

Table 2

Pin No.	Symbol	Description
1	FLM	Inputs display data.
2	M	No Connection
3	CL1	Data Shift Signal. This signal is valid at its falling edge.
4	CL2	Data Latch Signal. Data is latched at the falling edge of this signal.
5	DISPOFF	Display ON (H), OFF(L)
6	DB0	Display Data input(LSB). 'High' for a selected level turns an LCD pixel on; 'Low' for a non-selected level turns an LCD pixel off
7	DB1	Display Data input. 'High' for a selected level turns an LCD pixel on; 'Low' for a non-selected level turns an LCD pixel off
8	DB2	Display Data input. 'High' for a selected level turns an LCD pixel on; 'Low' for a non-selected level turns an LCD pixel off
9	DB3	Display Data input (MSB) 'High' for a selected level turns an LCD pixel on; 'Low' for a non-selected level turns an LCD pixel off
10	VDD	Power supply for logic (+5V)
11	VSS	Ground (0V)
12	VEE	Negative power supply for the LCD drive circuits.
13	V0	Power supply for LCD contrast adjustment control.
14	FG	Frame Ground (see note 1)

Note 1: This pin is electrically connected to the metal bezel (frame) and is connected to Ground too.

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings(Ta = 25 ºC)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD - VSS	-0.3	+7.0	V
Power Supply voltage (LCD drive)	VLCD =VDD-V5 =VDD-V0	0	+30	V
Input voltage	Vin	-0.3	VDD +0.3	V
Input current	I	0	1	A

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 5V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		4.75	5.0	5.25	V
Supply voltage (LCD)	VLCD =VDD –V0	VDD = 5V, (Note 1).	22.0	23.0	24.0	V
Input signal voltage	V_{IN}	"High" level	0.8VDD	-	VDD	V
		"Low" level	0	-	0.2VDD	V
Supply Current (Logic & LCD)	I_{DD}	Character mode	-	5.5	8.5	mA
		Checker board mode	-	7.0	11.0	mA
Supply Current (LCD)	I_o	Character mode, V_{DD} = 5V, (Note 1).	-	4.0	6.0	mA
		Checker board mode V_{DD} = 5V, (Note 1).	-	5.5	8.5	mA

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

At Ta =0 °C to +50 °C , VDD = 5V±5%, VSS=0V.

Segment Driver Application Timing

Table 6

Characteristic	Symbol	Test Condition	MIN	TYP	MAX	Unit
Clock cycle time	t_{CY}	Duty=50%	125	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	
Clock rise/fall time	$t_{R/tF}$	-	-	-	-	
Data set-up time	t_{DS}	-	30	-	-	
Data hold time	t_{DH}	-	30	-	-	
Clock set-up time	t_{CS}	-	80	-	-	
Clock hold time	t_{CH}	-	80	-	-	
Propagation delay time	t_{PHL}	ELB Output	-	-	60	
		ERB Output			60	
ELB,ERB set-up time	t_{PSU}	ELB Input	30	-	-	
		ERB Input	30			
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	µs
DISPOFFB clear time	t_{CD}	-	100	-	-	ns
M - OUT propagation delay time	t_{PD1}	CL=15 pF	-	-	1.0	µs
CL1 - OUT propagation delay time	t_{PD2}		-	-	1.0	
DISPOFFB - OUT propagation delay time	t_{PD3}		-	-	1.0	

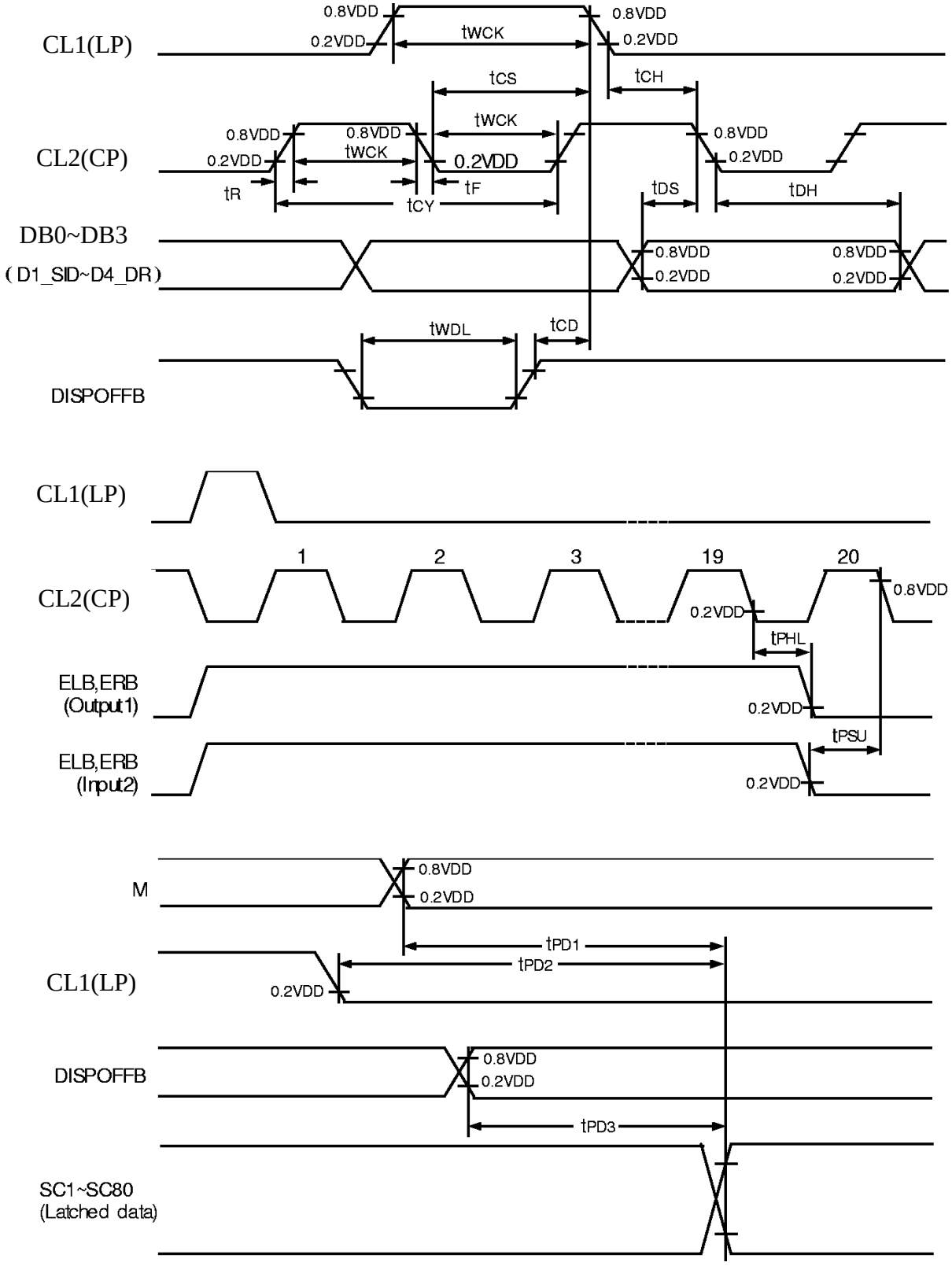


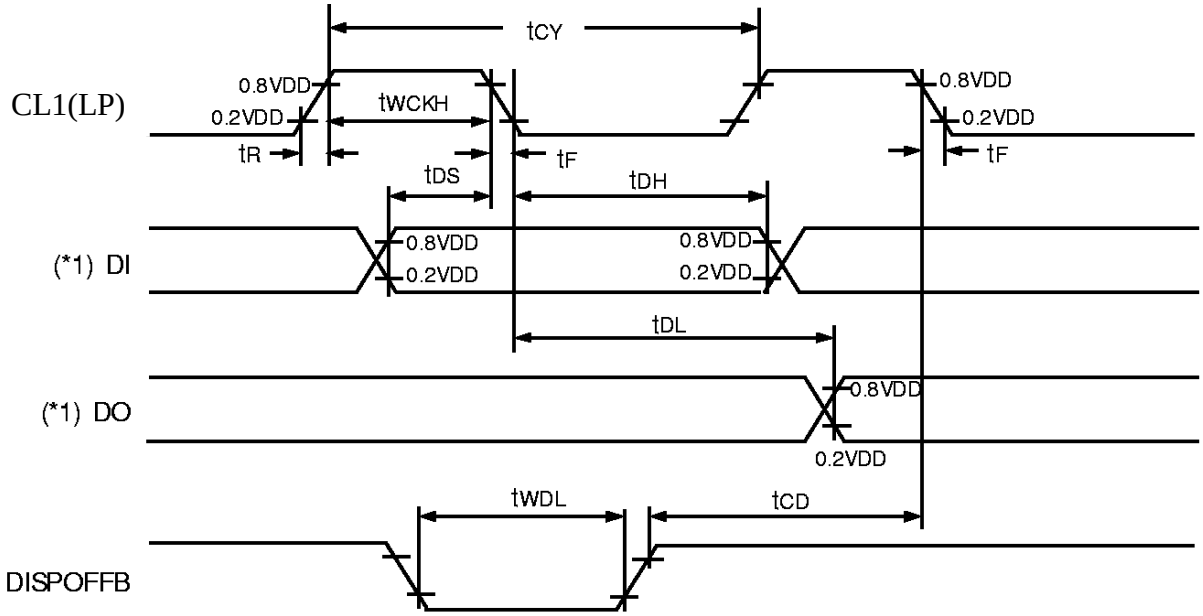
Figure 3: Diagram of Segment Driver Application Timing

At Ta = 0 °C to +50 °C , VDD = 5V±5%, VSS=0V.

Common Driver

Table 7

Characteristic	Symbol	Test Condition	MIN	TYP	MAX	Unit
Clock cycle time	t_{CY}	Duty=50%	250	-	-	ns
Clock pulse width	t_{WCK}	-	45	-	-	
Clock rise/fall time	$t_{R/tF}$	-	-	-	50	
Data set-up time	t_{DS}	-	30	-	-	
Data hold time	t_{DH}	-	30	-	-	
DISPOFFB low pulse width	t_{WDL}	-	1.2	-	-	µs
DISPOFFB clear time	t_{CD}	-	100	-	-	ns
Output delay time	t_{DL}	CL=15 pF	-	-	200	
M - OUT propagation delay time	t_{PD1}		-	-	1.0	µs
CL1 - OUT propagation delay time	t_{PD2}		-	-	1.0	
DISPOFFB - OUT propagation delay time	t_{PD3}		-	-	1.0	



(*1) When in single-type interface mode
DI ⇒ D2_DL(SHL="L"), D4_DR(SHL="H")
DO ⇒ D4_DR(SHL="L"), D2_DL(SHL="H")
When in dual-type interface mode
DI ⇒ D2_DL and D3_DM(SHL="L"), D4_DR and D3_DM(SHL="H")
DO ⇒ D4_DR(SHL="L"), D2_DL(SHL="H")

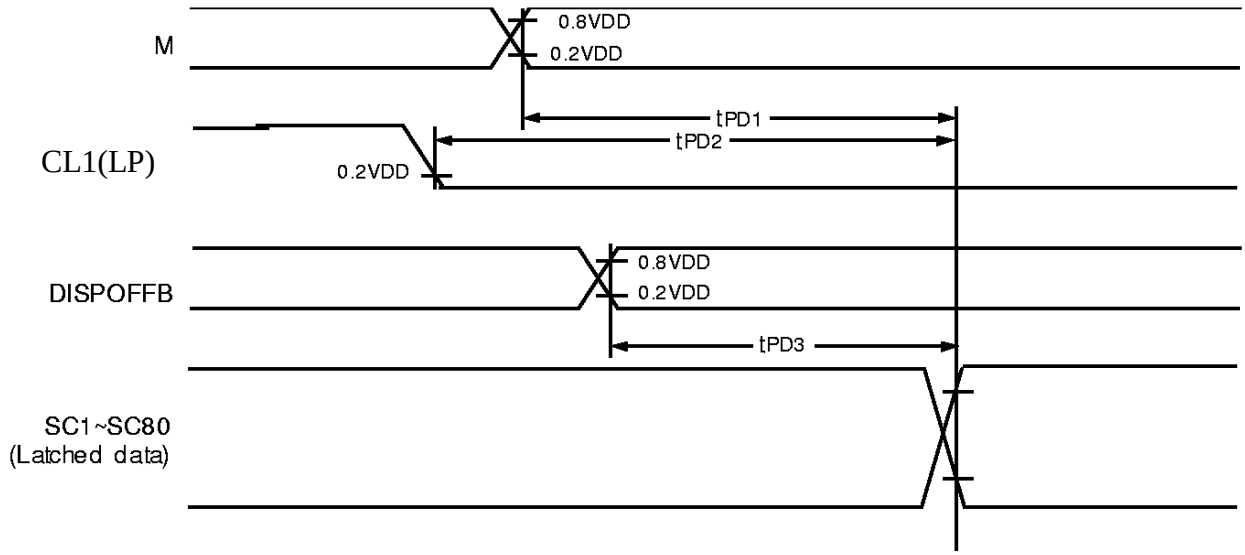


Figure 4: Diagram of Common Driver Application Timing

5.3 Timing Diagram of VDD against V0 and VEE.

Power on sequence shall meet the requirement of Figure 5, the timing diagram of VDD against V0 and VEE.

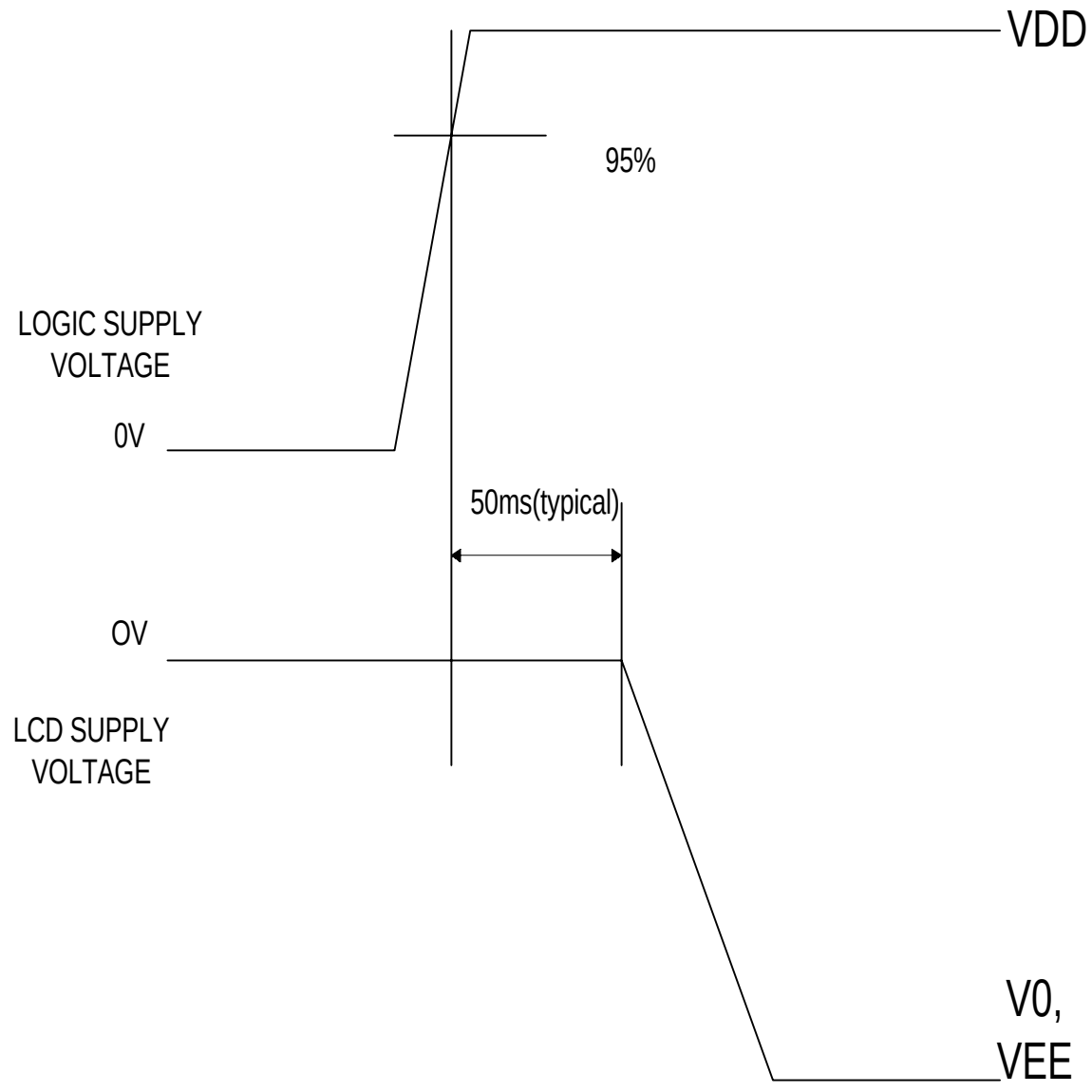


Figure 5: Timing diagram of VDD against V0 and VEE.

"Varitronix Limited reserves the right to change this specification."

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