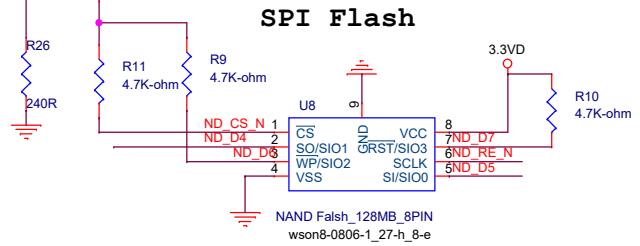
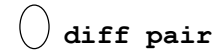
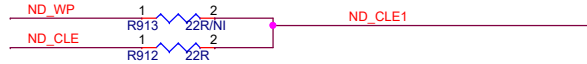
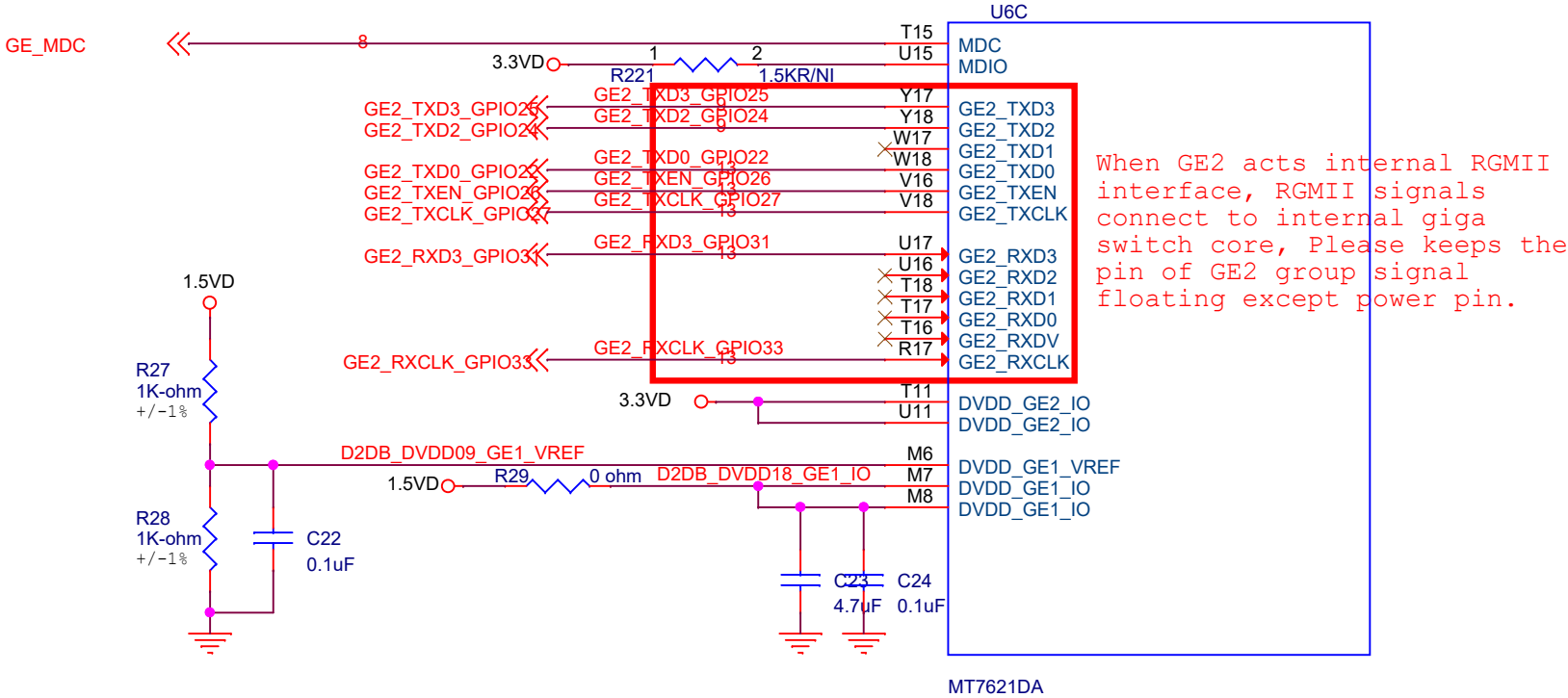


## U6B

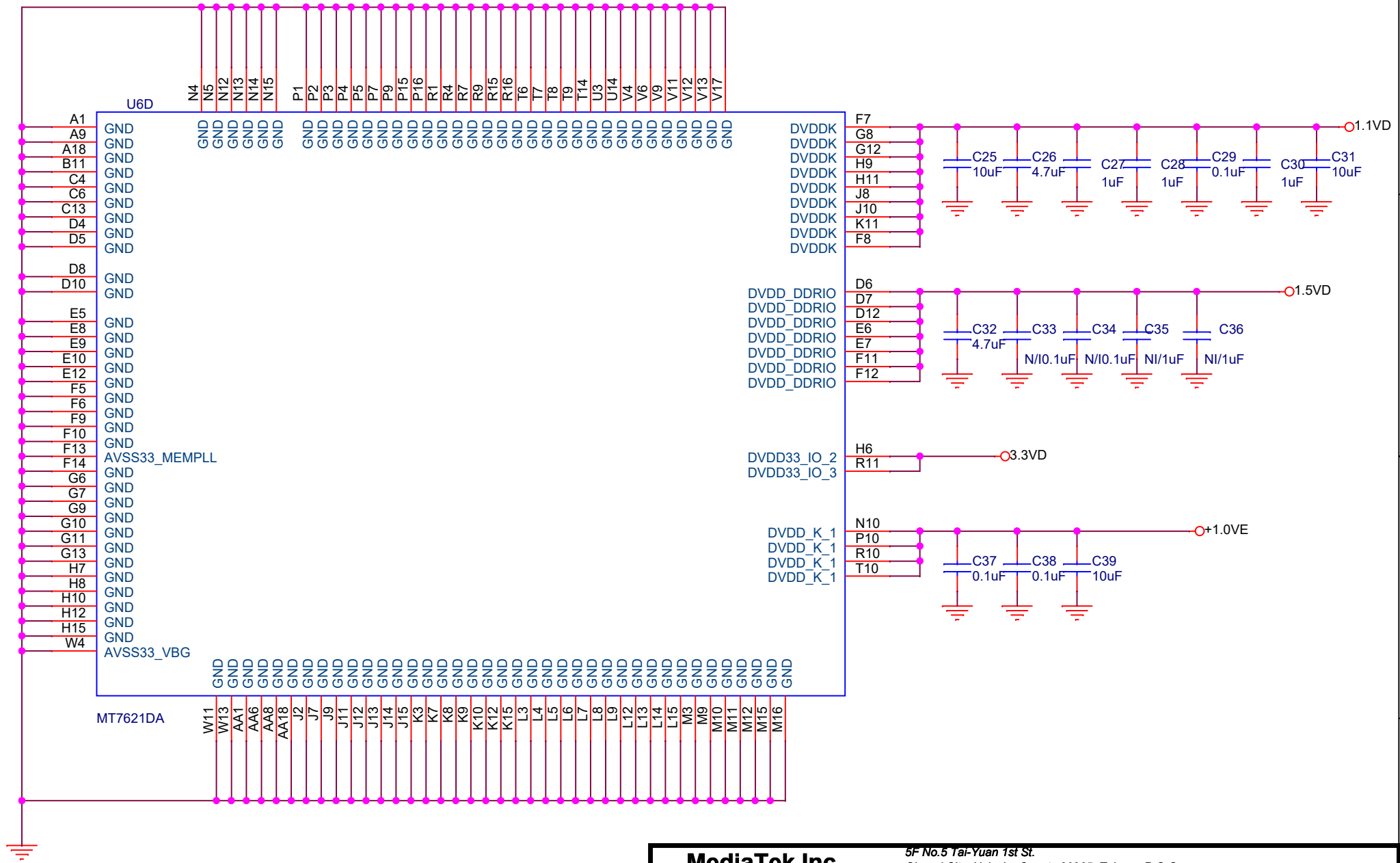


Nand Flash/ SD-XC/SPI Flash

RGMII Interface



# MT7621 Power

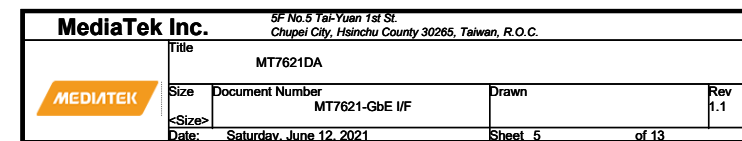


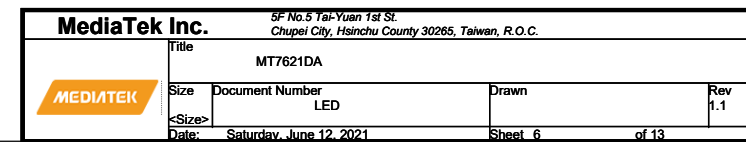
**MediaTek Inc.**

5F No.5 Tai-Yuan 1st St.  
Chupei City, Hsinchu County 30265, Taiwan, R.O.C.

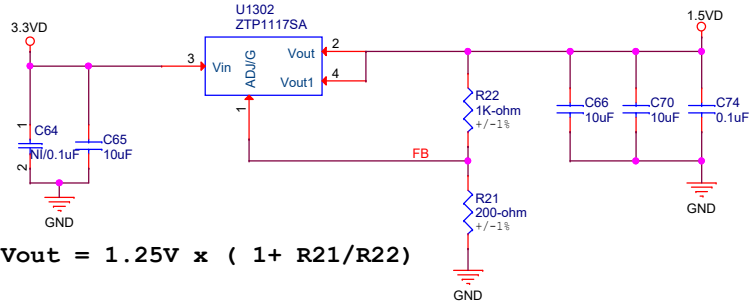


Title MT7621DA			
Size	Document Number	Drawn	Rev
<Size>	MT7621-Power		1.1
Date:	Saturday, June 12, 2021	Sheet 4	of 13



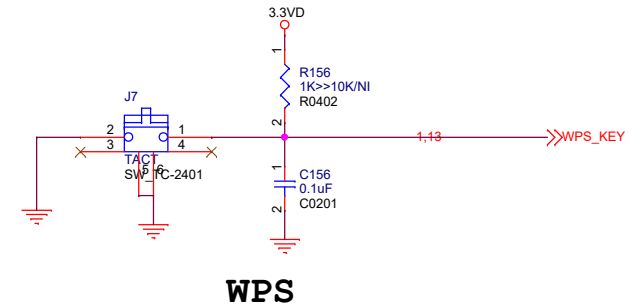
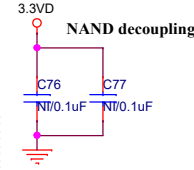
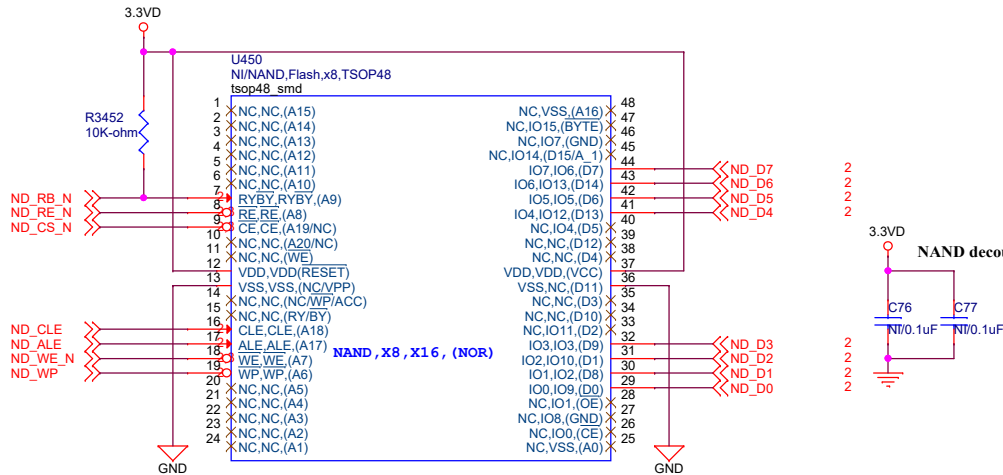
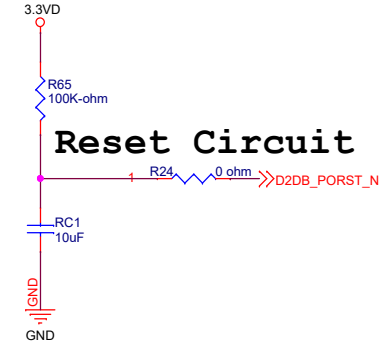
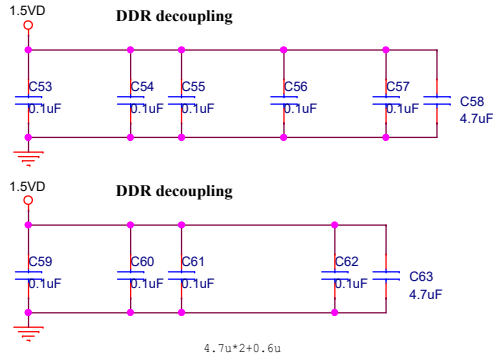


1.5V PMU MUST close MT7621DA for GE2 and DDR3



$$V_{out} = 1.25V \times (1 + R_{21}/R_{22})$$

Close to MT7621DA 1.5V power pin  
1.5V power trace should wider than MT7621A,  
2 Layer PCB can refer MT7621DA board design



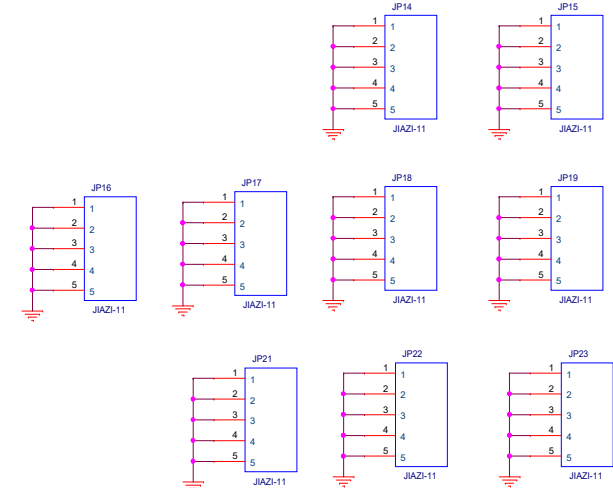
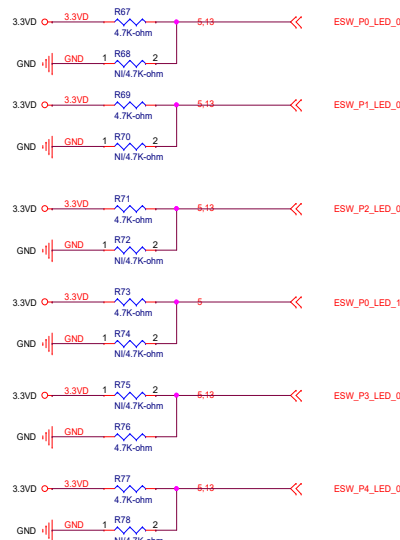
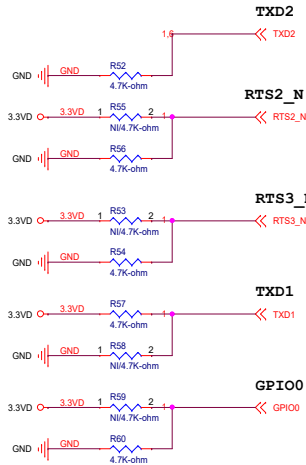
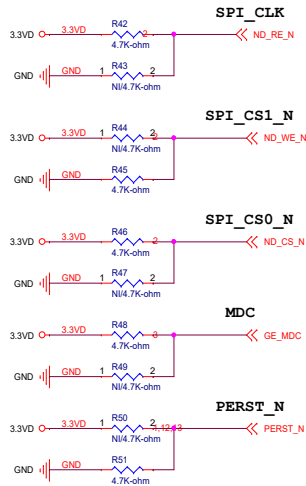
MediaTek Inc.		5F No.5 Tai-Yuan 1st St. Chupei City, Hsinchu County 30265, Taiwan, R.O.C.	
Title		MT7621DA	
Size	Document Number	MEM DDR3/NAND FLASH	
	<Size>		
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# Boot Strapping

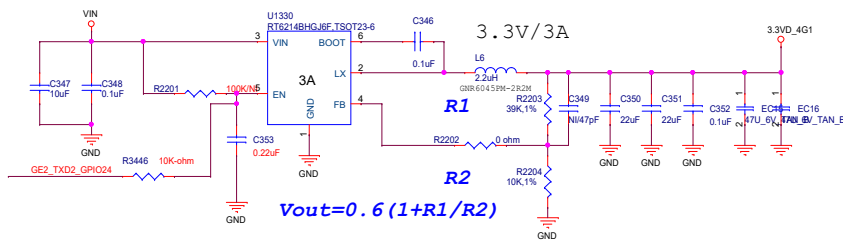
Pin Name	Description	Value	
SPI_CLK	DRAM_FROM_EE	For non scan mode: 0: DRAM/PLL configuration from EEPROM <b>1: DRAM configuration from Auto Detect</b>	For FT mode: 0: SUTIF 1: 3-wire SPI
{SPI_CS1_N, SPI_CS0_N, MDC}	XTAL_MODE	000: 20 MHz, Self Oscillation mode 001: 20 MHz, Single end input 110: 20 MHz, differential input <b>011: 40 MHz, Self Oscillation mode</b>	100: 40 MHz, Single end input 101: 40 MHz, differential input 110: 25 MHz, Self Oscillation mode 111: 25 MHz, Single end input
PERST_N	OCP_RATIO	0: 1:3 1: 1:4	
TXD2	DRAM_TYPE	0: DDR3 (MT7621DA w/DDR3 1Gb) 1: DDR2	
{RTS2_N, RTS3_N, TXD1, GPIO0}	CHIP_MODE[3:0]	0000: Normal / Boot from SPI 4-byte address and XTAL clock 0001: Normal / Boot from ROM (NAND page 2k+64 bytes) <b>0010: Normal / Boot from SPI 3-byte address</b> 0011: Normal / Boot from SPI 4-byte address 0100: iNIC RGMII / Boot from ROM 0101: iNIC MII / Boot from ROM 0110: iNIC RVMII / Boot from ROM 0111: iNIC PHY / Boot from ROM 1000: iNIC RGMII / Boot from ROM and XTAL clock 1001: Normal / Boot from internal SRAM 1010: Normal / Boot from ROM (NAND page 2k+128 bytes) 1011: Normal / Boot from ROM (NAND page 4k+128 bytes) 1100: Normal / Boot from ROM (NAND page 4k+224 bytes) 1101: Debug mode 1110: Scan mode 1111: Final Test	

# Giga Switch Hardware Trap

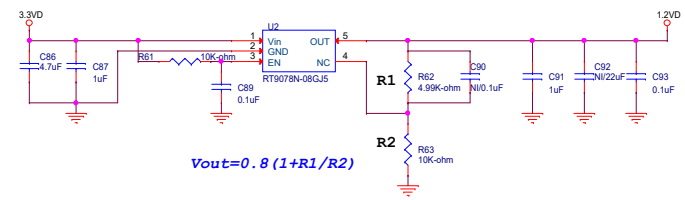
Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] 4'b0000: IDDO mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1000: AFE-OLT mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]		
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b01: 20MHz 2'b10: 40MHz 2'b11: 25MHz	2'b10
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		



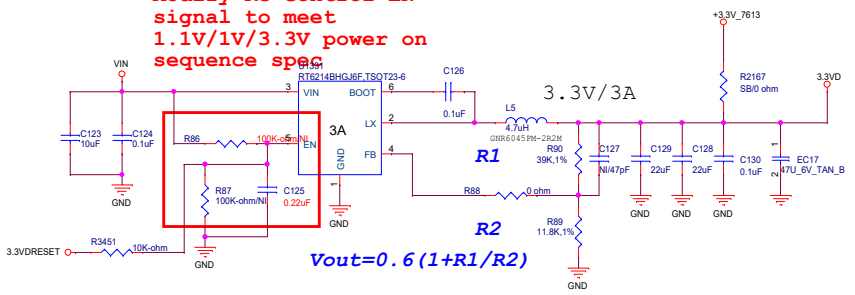




For USB/PCIe PHY Power (1.2V)  
Current= 300mA

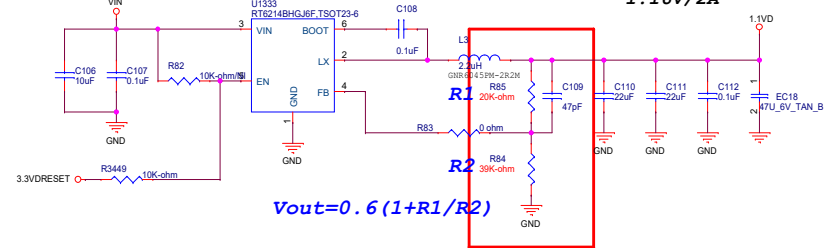


Modify RC control EN  
signal to meet  
1.1V/1V/3.3V power on  
sequence spec

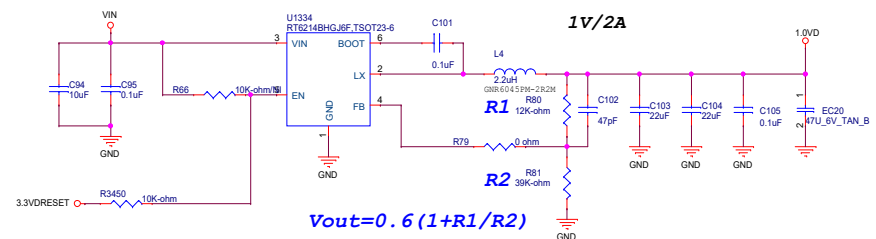
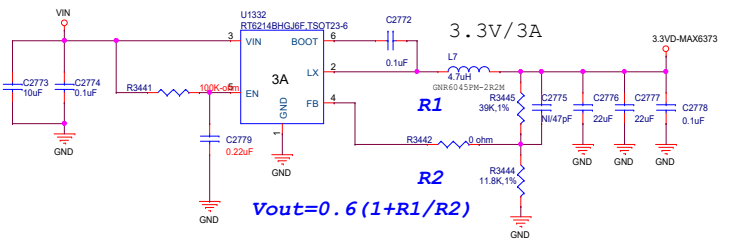
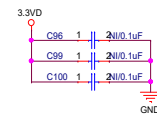


1. MT7621DA 2L PCB, Original Vcore 1.15V rising to 1.16V
2. 1.16V PMU MUST close MT7621DA.

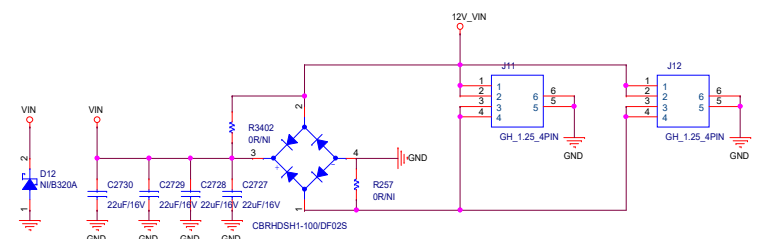
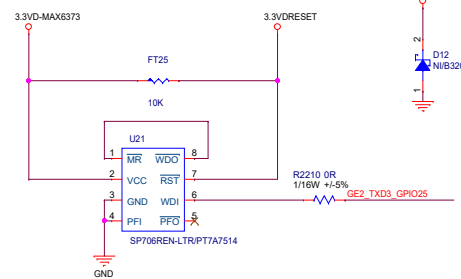
1.16V/2A

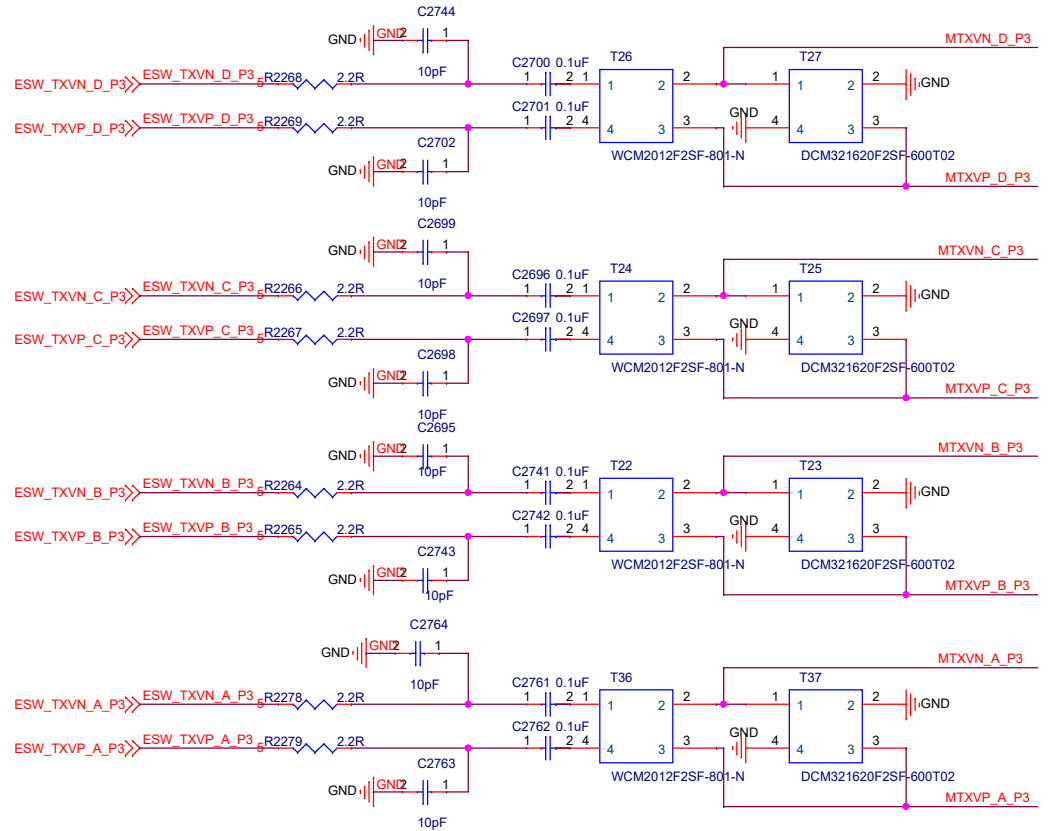
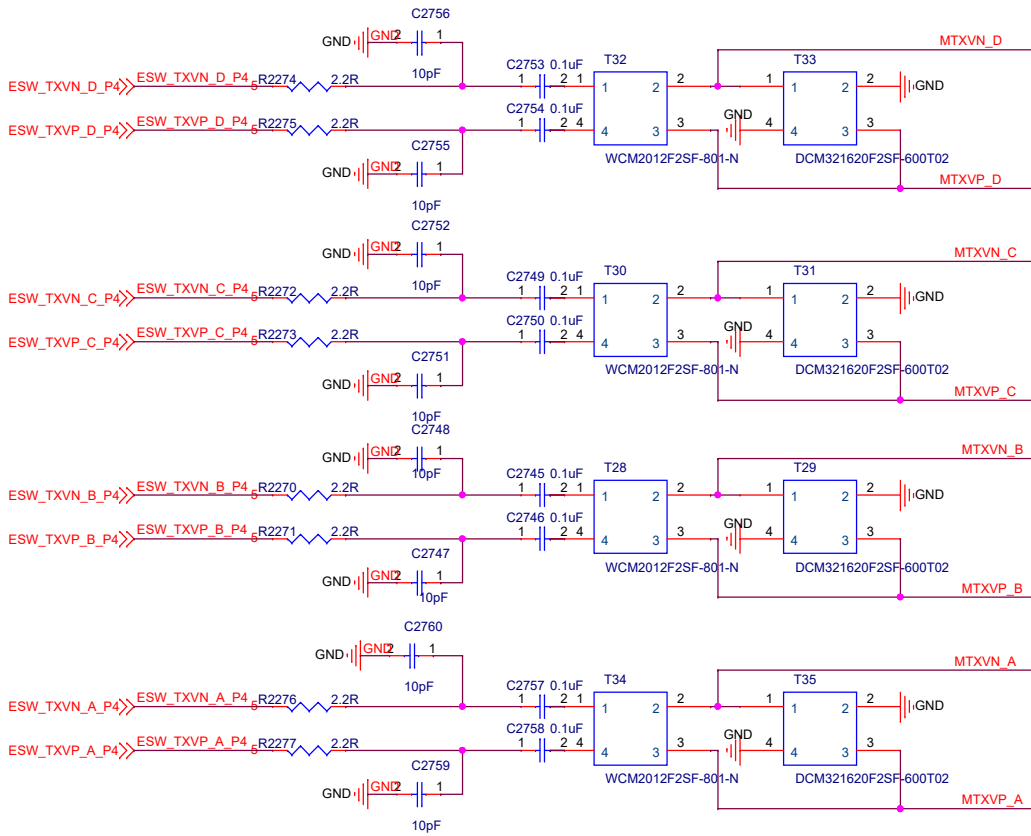


Reserve for EMI

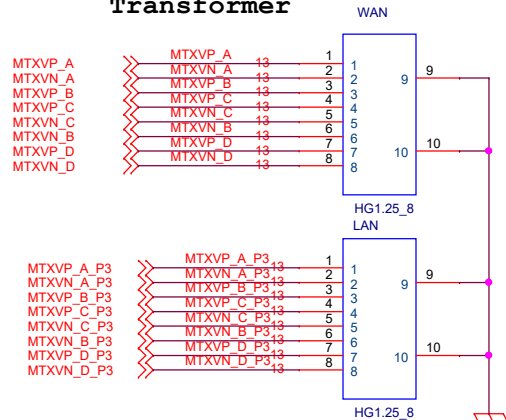



GE2\_TXD3\_GPIO25  
GE2\_TXD2\_GPIO24

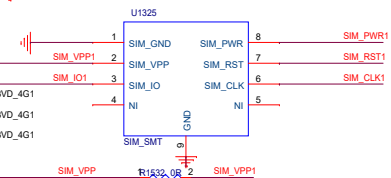
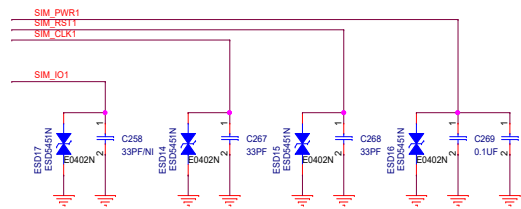
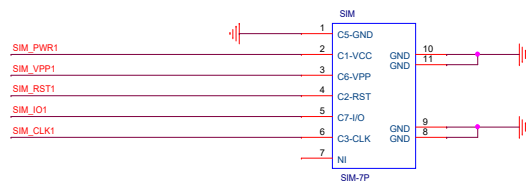




### Transformer



<b>MediaTek Inc.</b>		5F No.5 Tai-Yuan 1st St. Chupei City, Hsinchu County 30265, Taiwan, R.O.C.	
	Title	MT7621DA	
	Size	Document Number	TRANSFORMER/RJ45
	<Size>	Date:	Saturday, June 12, 2021
Date:		Sheet	10 of 13



复位信号

GE2\_RXD2\_GPIO3011



复位信号

GE2\_RXD2\_GPIO3011

SSUSB\_TXP 2:1R3 OR 1

SSUSB\_TXN 2:1R6 OR 1

SSUSB\_RXP 2:1R8 220M

SSUSB\_RXN 2:1R9 220M

USB\_DM 2:1X0 OR 1

USB\_DP 2:1X1 OR 1

开关机信号，默认高电平开机

