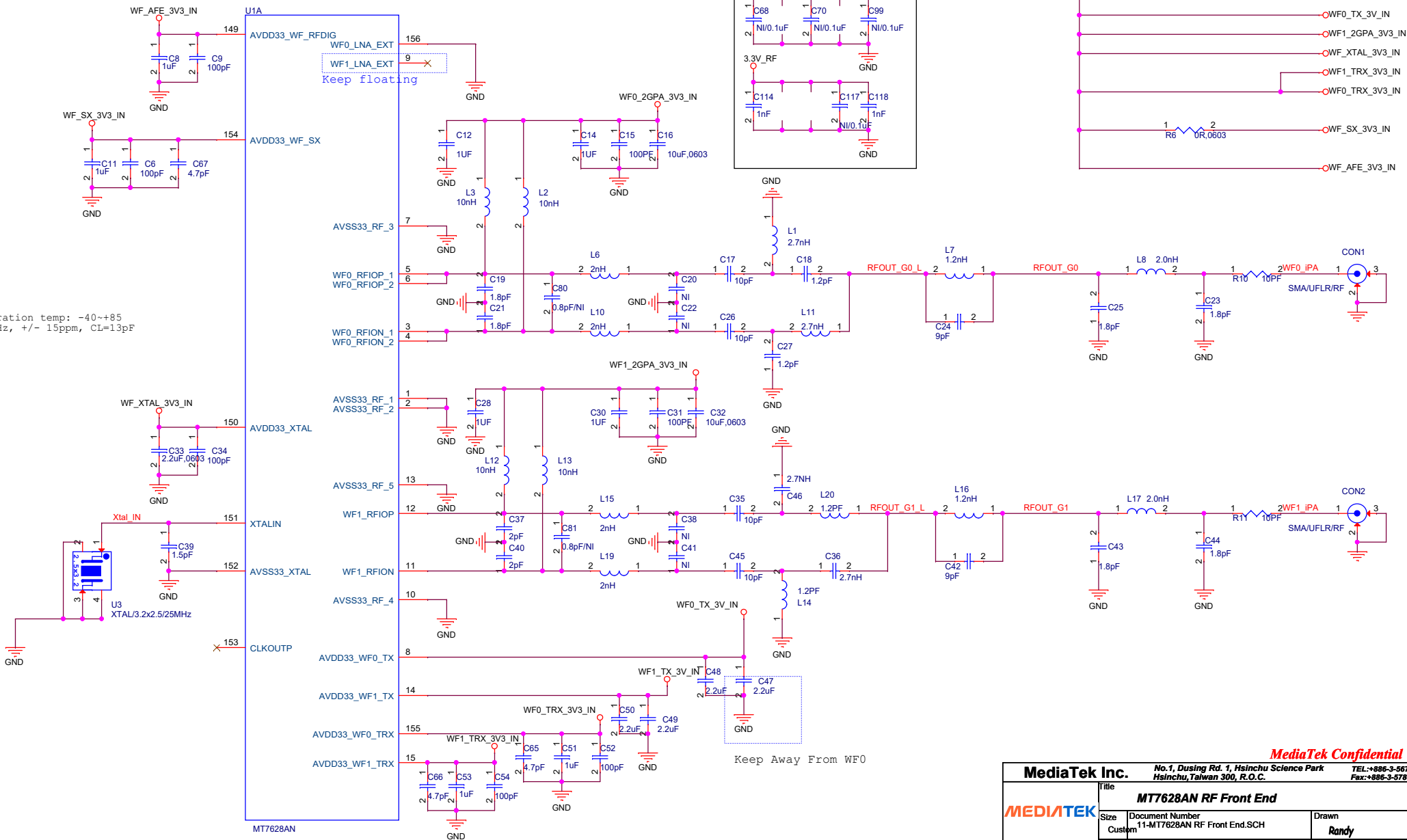

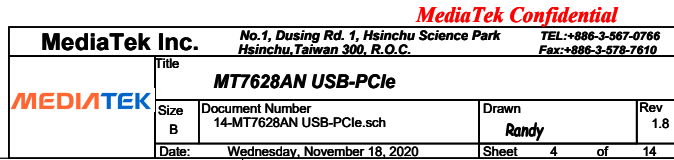


operation temp: -40~+85
25MHz, +/- 15ppm, CL=13pF

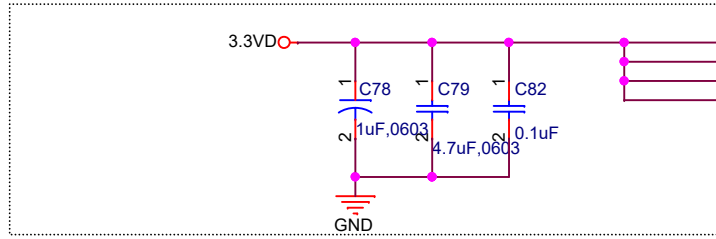


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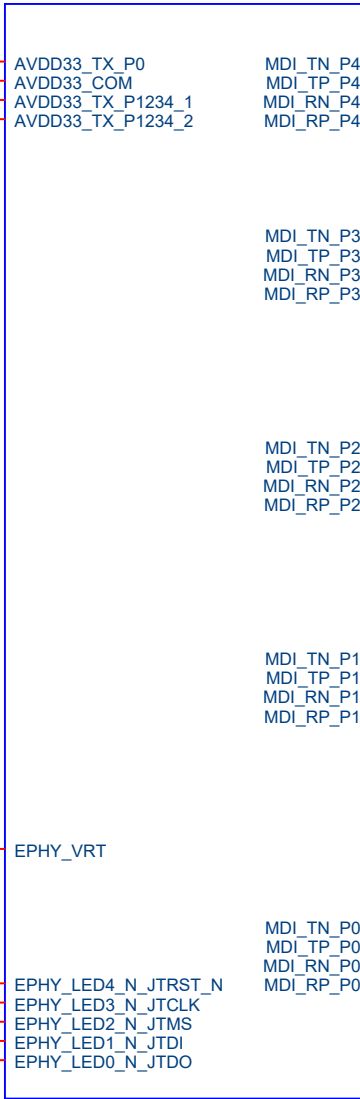
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		Title MT7628AN RF Front End			
		Size Document Number 11-MT7628AN RF Front End.SCH		Drawn Randy	
		Date Wednesday, November 18, 2020		Rev 1.8	
		Sheet 1		of 14	



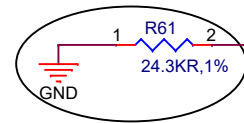
Close to MT7628



U1E




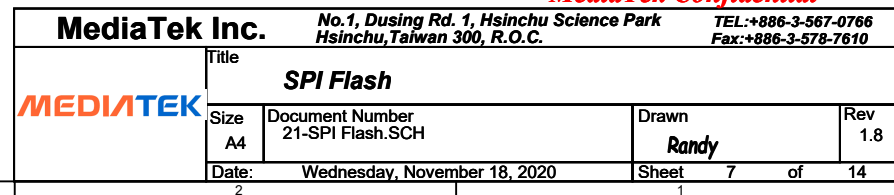
Close to MT7628N

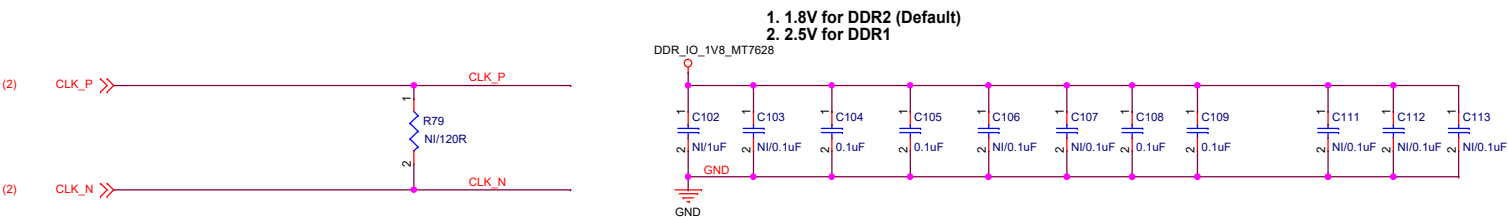
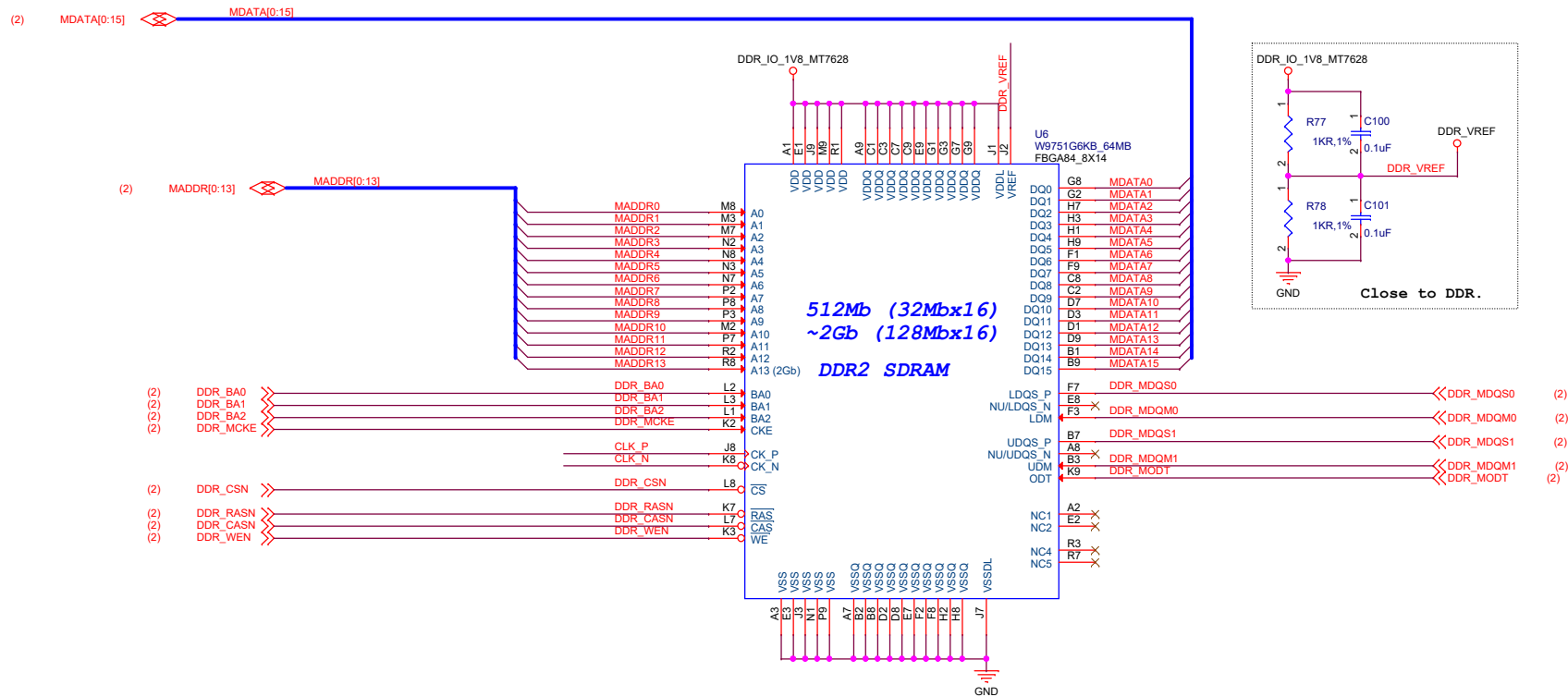


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	Size A4	Document Number 15-MT7628AN Ethernet-E.SCH		Drawn Randy	Rev 1.8
	Date:	Wednesday, November 18, 2020		Sheet 5 of 14	





I2S_DO >> I2S_DO (3)

SPI_MOSI >> SPI_MOSI (3,7)

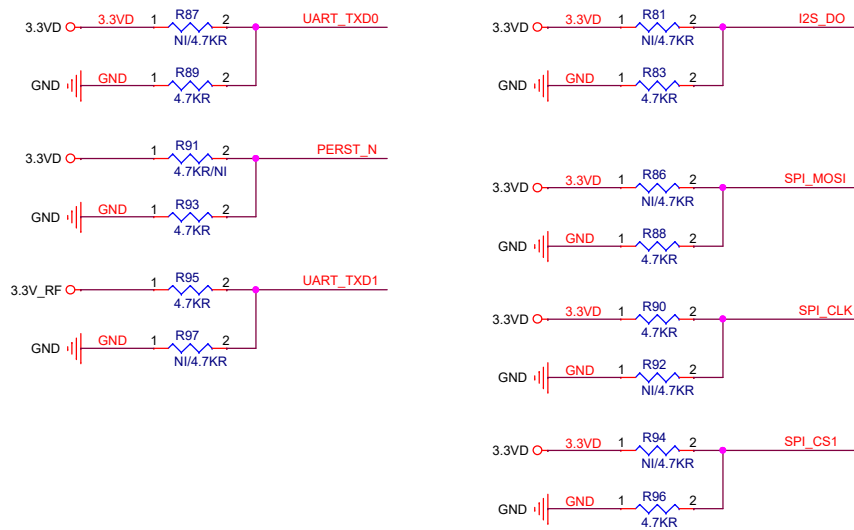
SPI_CLK >> SPI_CLK (3,7)

SPI_CS1 >> SPI_CS1 (3)

UART_TXD0 >> UART_TXD0 (3)

PERST_N >> PERST_N (10,3,4)


UART_TXD1 >> UART_TXD1 (3)



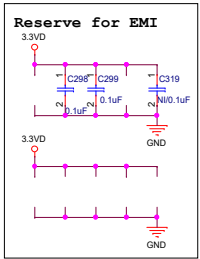
Bootstrapping Pins Description

Pin Name	Boot Strapping Signal Name	Description
UART_TXD1	DBG_JTAG_MODE	0: JTAG_MODE 1: EPHY_LED (default)
PERST_N	XTAL_FREQ_SEL	0: 25 MHz DIP 1: 40 MHz SMD
I2S_SDO	DRAM_TYPE	1: DDR1 0: DDR2 [note] This pin is valid for MT7628AN only. It needs to be pull-low for 7628KN which only supports DDR1.
{SPI_MOSI SPI_CLK, SPI_CS1}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. 000: Boot from PLL (boot from SPI 3-Byte Addr) 001: Boot from PLL (boot from SPI 4-Byte Addr) 010: Boot from XTAL (boot from SPI 3-Byte Addr) 011: Boot from XTAL (boot from SPI 4-Byte Addr)
PAD_TXD0	EXT_BGCK	1: Test Mode 0: Normal (default)



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File		M77612E-5G			
	Size	Document Number		Drawn	Rev
	Case	31-M77612E-5G SCH		Randy	1.8
Date:		Wednesday, November 18, 2020		Sheet	10 of 14

Option for 5G client Power



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file					
MEDIATEK		Power & Reset			
Size	Document Number	Drawn	Rev		
Customer	5-Power - Reset.SCH	Randy	1.8		
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