

Turbo Switches and Turbo LEDs

I/O write to 0x063, bits 6,7 write to J6, J5
A9=0; A8=0; A7=0; J6=1; A6=1; A5=0; A3=0; A2=0; A1=1; A0=1
Turbo LEDs?

I/O read from 0x073, returns J3 and J4 in bits 0,1
A9=0; A8=0; A7=0; A6=1; A5=1; A4=1; A3=0; A2=0; A1=1; A0=1
Turbo switches?

The diagram illustrates a complex digital logic circuit for reading turbo switches and LEDs. It features several 74LS152 and 74LS153 chips, which are 4-to-1 multiplexers. The circuit uses a series of AND gates to combine inputs from pins A0 through A9 and J3 through J6. The outputs of these gates are connected to the inputs of the multiplexers. The multiplexers are configured to output the state of the turbo switches (J3, J4) and LEDs (J5, J6) to the D0 and D1 pins. The circuit is powered by VCC and GND, with pull-up resistors (R4, R5, R9, R10) connected to the inputs of the multiplexers.

Logic ICs – Power Pins

The diagram illustrates the power pin connections for seven logic ICs. Each IC is shown as a yellow rectangle with pins on all four sides. The connections are as follows:

- U290 74LS150:** VCC to pins 1 and 14; GND to pins 4 and 5.
- U306 74LS100:** VCC to pins 1 and 14; GND to pins 4 and 5.
- U316 74LS104:** VCC to pins 1 and 14; GND to pins 4 and 5.
- U42D 74LS11:** VCC to pins 1 and 14; GND to pins 4 and 5.
- U43E 74LS102:** VCC to pins 1 and 14; GND to pins 4 and 5.
- U44E 74LS125:** VCC to pins 1 and 14; GND to pins 4 and 5.
- U47G 74LS109:** VCC to pins 1 and 14; GND to pins 4 and 5.

Logic ICs – Spare Gates

The diagram illustrates four spare logic gates within a 7400 IC package:

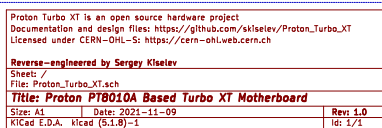
- U208 74LS10:** A 2-input AND gate with inputs x_1 and x_2 , and output x_6 .
- U300 74LS20:** A 3-input AND gate with inputs x_{11} , x_{12} , and x_{13} , and output x_3 .
- U404 74LS125:** A 2-input OR gate with inputs x_2 and x_7 , and output x_3 .
- U402 74LS125:** A 2-input OR gate with inputs x_{12} and x_{13} , and output x_4 .

Power and Decoupling Capacitors

The schematic shows a detailed layout of power and decoupling capacitors for the P2 module. The main horizontal line represents the power rail, with capacitors C3 through C52 connected to ground. The capacitors are arranged in a sequence that likely corresponds to the physical layout of the module. The values of the capacitors are specified as follows:

- C3: 100nF
- C4: 100nF
- C5: 100nF
- C6: 100nF
- C7: 100nF
- C8: 100nF
- C9: 100nF
- C10: 100nF
- C11: 100nF
- C12: 100nF
- C13: 100nF
- C14: 100nF
- C15: 100nF
- C16: 100nF
- C17: 100nF
- C18: 100nF
- C19: 100nF
- C20: 100nF
- C23: 100nF
- C24: 100nF
- C25: 100nF
- C26: 100nF
- C27: 100nF
- C28: 100nF
- C29: 100nF
- C30: 100nF
- C31: 100nF
- C32: 100nF
- C33: 100nF
- C34: 100nF
- C35: 100nF
- C36: 100nF
- C37: 100nF
- C38: 100nF
- C39: 100nF
- C40: 100nF
- C41: 100nF
- C42: 100nF
- C43: 100nF
- C44: 100nF
- C45: 100nF
- C46: 100nF
- C47: 100nF
- C48: 100nF
- C49: 100nF
- C50: 100nF
- C51: 100nF
- C52: 100nF

The diagram also shows connections for the +12V, -12V, and -5V rails, and a section for PWR_FLAG signals. A small inset shows the mounting holes for the module, labeled H1 through H6.



Proton Turbo XT is an open source hardware project
Documentation and design files: https://github.com/skileev/Proton_Turbo_XT
Licensed under CERN-OHL-S: <https://cern-ohlweb.cern.ch>

Reverse-engineered by Sergey Skileev

Sheet: /
File: Proton_Turbo_XT.sch

Title: Proton P18010A Based Turbo XT Motherboard

Size: A1	Date: 2021-11-09	Rev: 1.0
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