Processor

File: Processor.kicad_sch

Cache

File: Cache.kicad_sch

Local Bus IDE

File: VLB_IDE.kicad_sch

ISA

File: ISA.kicad_sch

Buffers

File: Buffers.kicad_sch

RTL8019AS Ethernet Controller

File: Ethernet.kicad_sch

Memory

File: Memory.kicad_sch

Keyboard and BIOS

File: Keyboard_BIOS.kicad_sch

AD1816 Audio Controller

File: Audio.kicad_sch

Chipset

File: Chipset.kicad_sch

TGUI9440 VGA Controller

File: TGUI9440_VGA.kicad_sch

Power

File: Power.kicad_sch

TGUI9440 VGA Memory

File: TGUI9440_Mem.kicad_sch

Pull-ups

File: Pull-ups.kicad_sch

Super I/O

File: Super_IO.kicad_sch

TODO:
- Add address decoder for DRAMS#
- Add DACK decoder
- Remove Ethernet boot ROM
- Add 3 pin header for CPU fan - switchable between 5V and 12V with a jumper

Check:
- MP0 strap option (chipset pin 50 function)
- MP1 strap option (chipser pins 192 and 193 function)
- MP2 strap option (chipset pins 108 and 47 function)
- Chipset power management signals, pins: 62, 156, 160
- Processor RESET and SRESET connections
- (82C602) XD7, XD6 and XD4 strap options
- (82C602) XD4 strap - add 2.2k pull-down to enable RTC
- (82C602) Load capacitors for RTC crystal?
- Reset circuit (button + PWRGD)

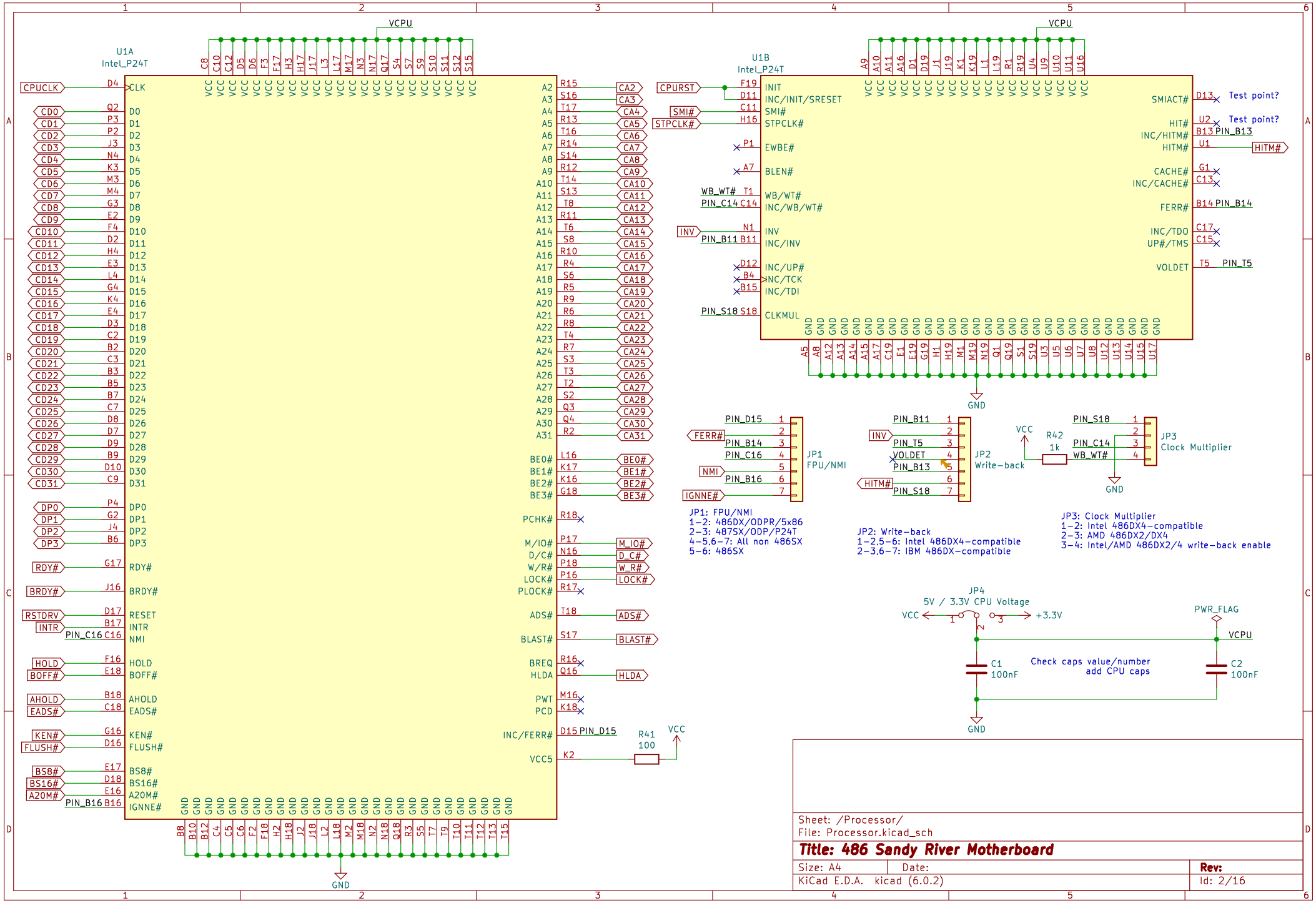
P24T Manual:
CPU EWBE# - NC or tied LOW (internall pull-down)
CPU BLEN# - NC or tied HIGH (internall pull-up)

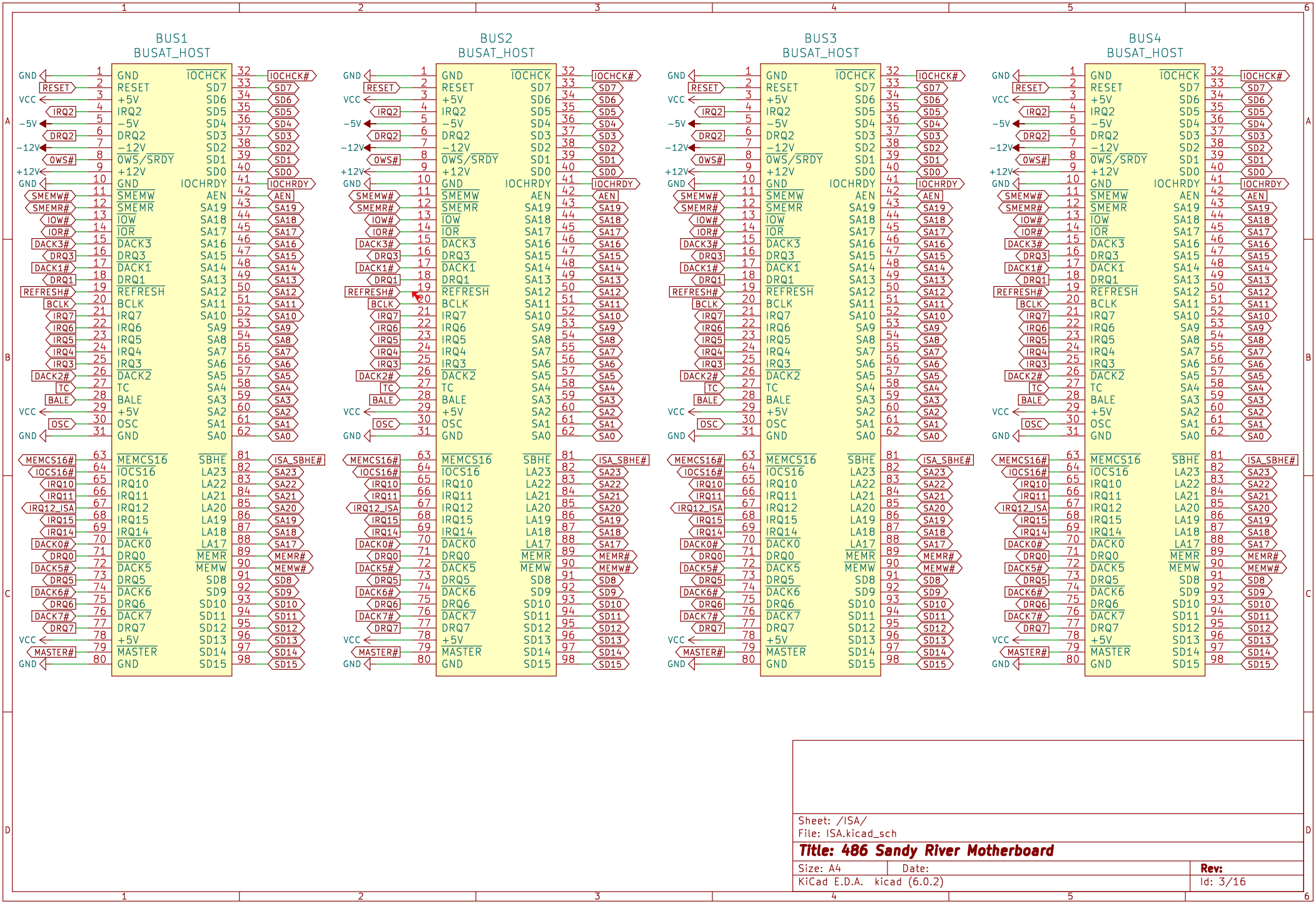
74xx Logic:
74F244 x 2 - DRAM address and control buffers?
74F138 - DACK decode?
74LS157 - Interrupt encode?
7407 - ?
74F08 - ?
74F245 - CA[23:16] - LA[23:17],SA[19:16]
Check ICs under keyboard controller

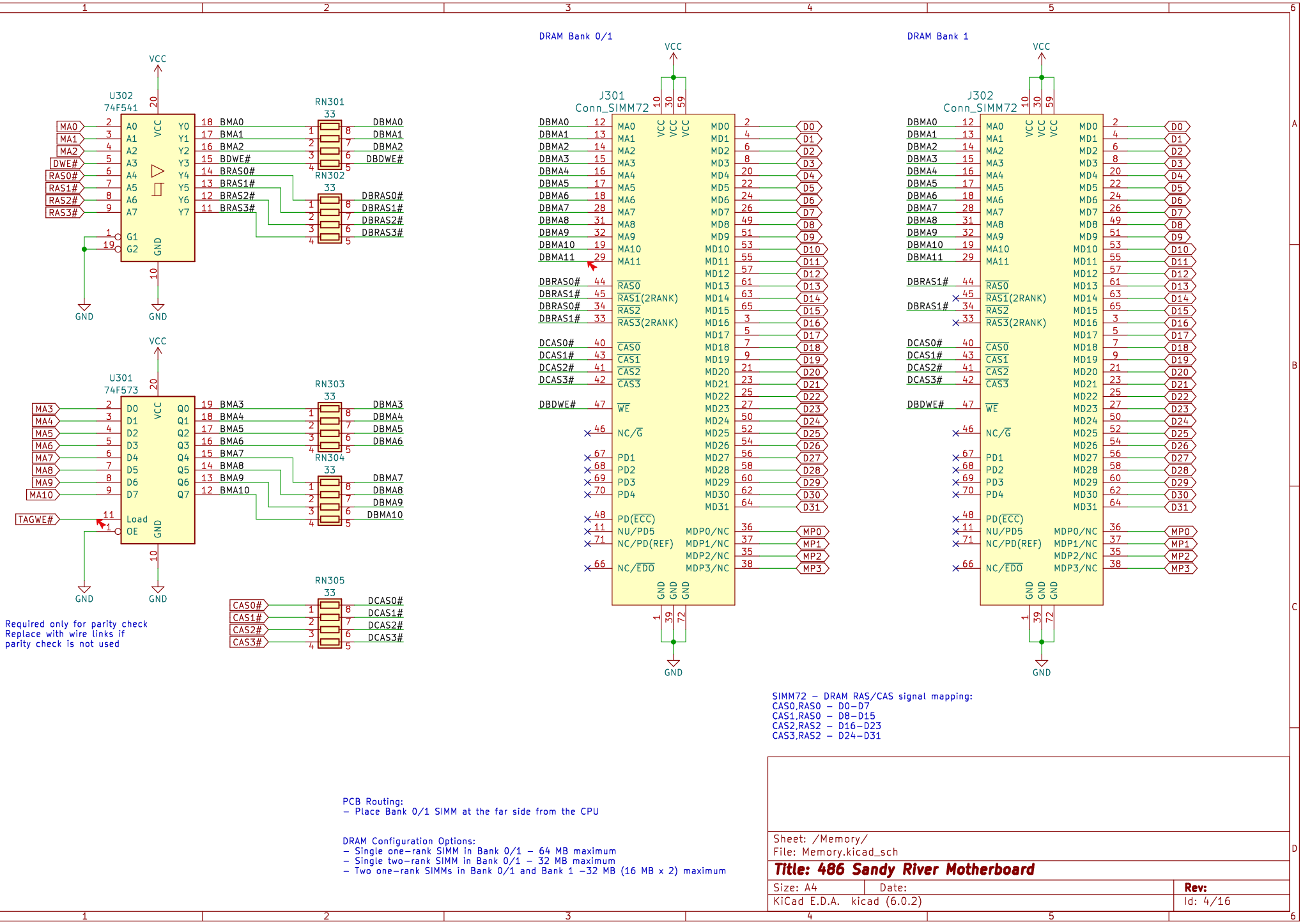
Sheet: /
File: mb486sr.kicad_sch

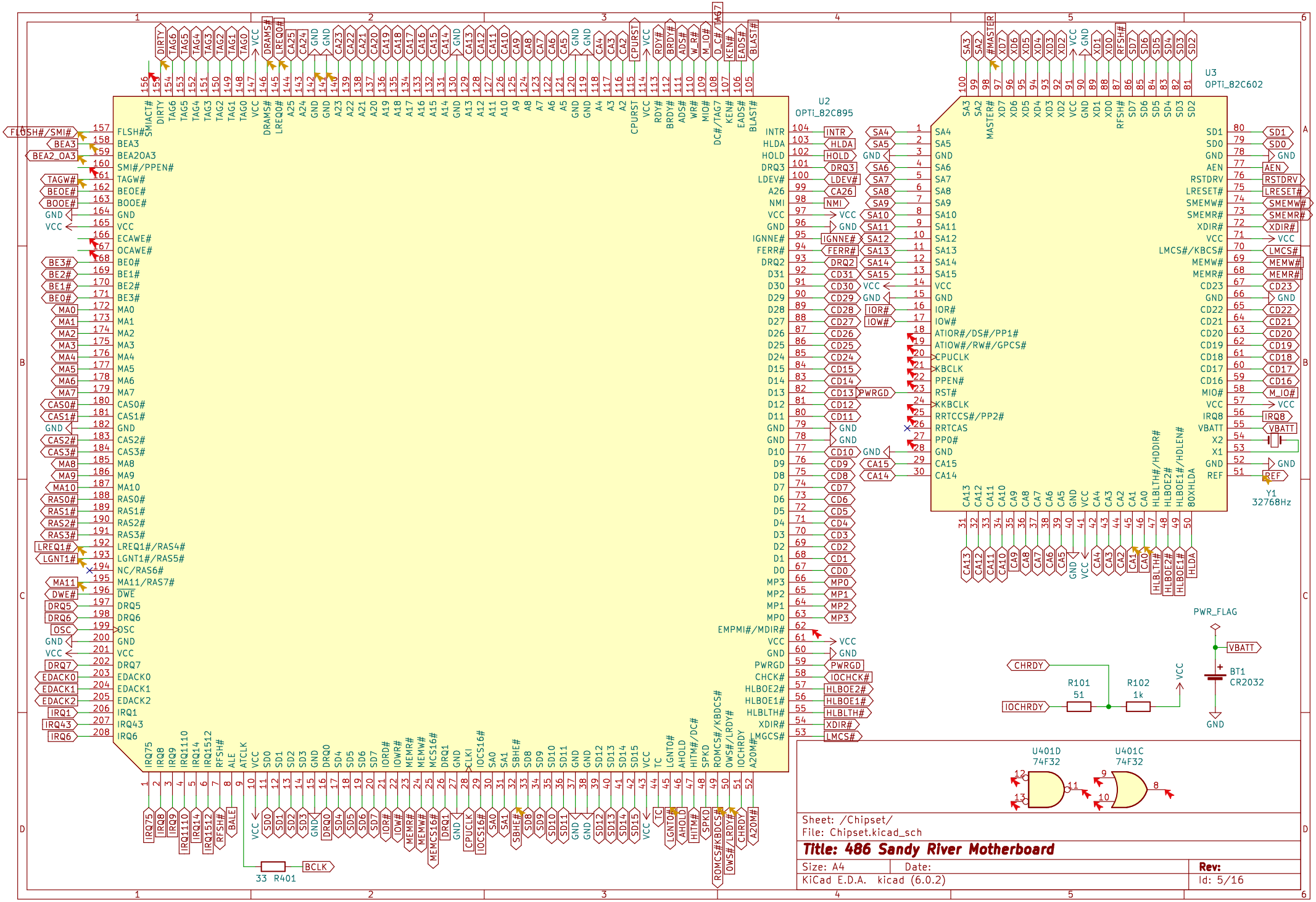
Title: 486 Sandy River Motherboard

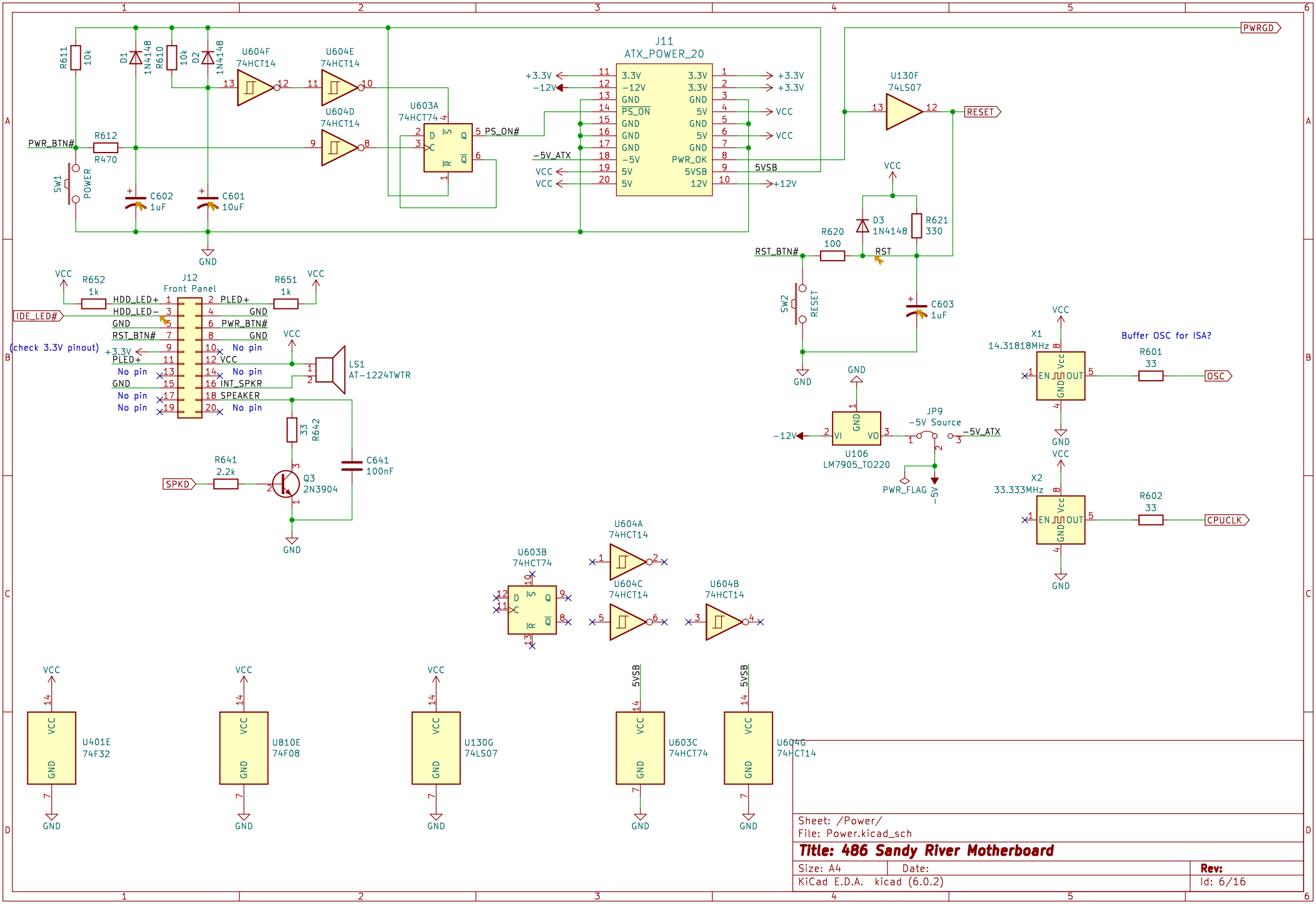
Size: A4	Date:	Rev:
KiCad E.D.A. kicad (6.0.2)		Id: 1/16

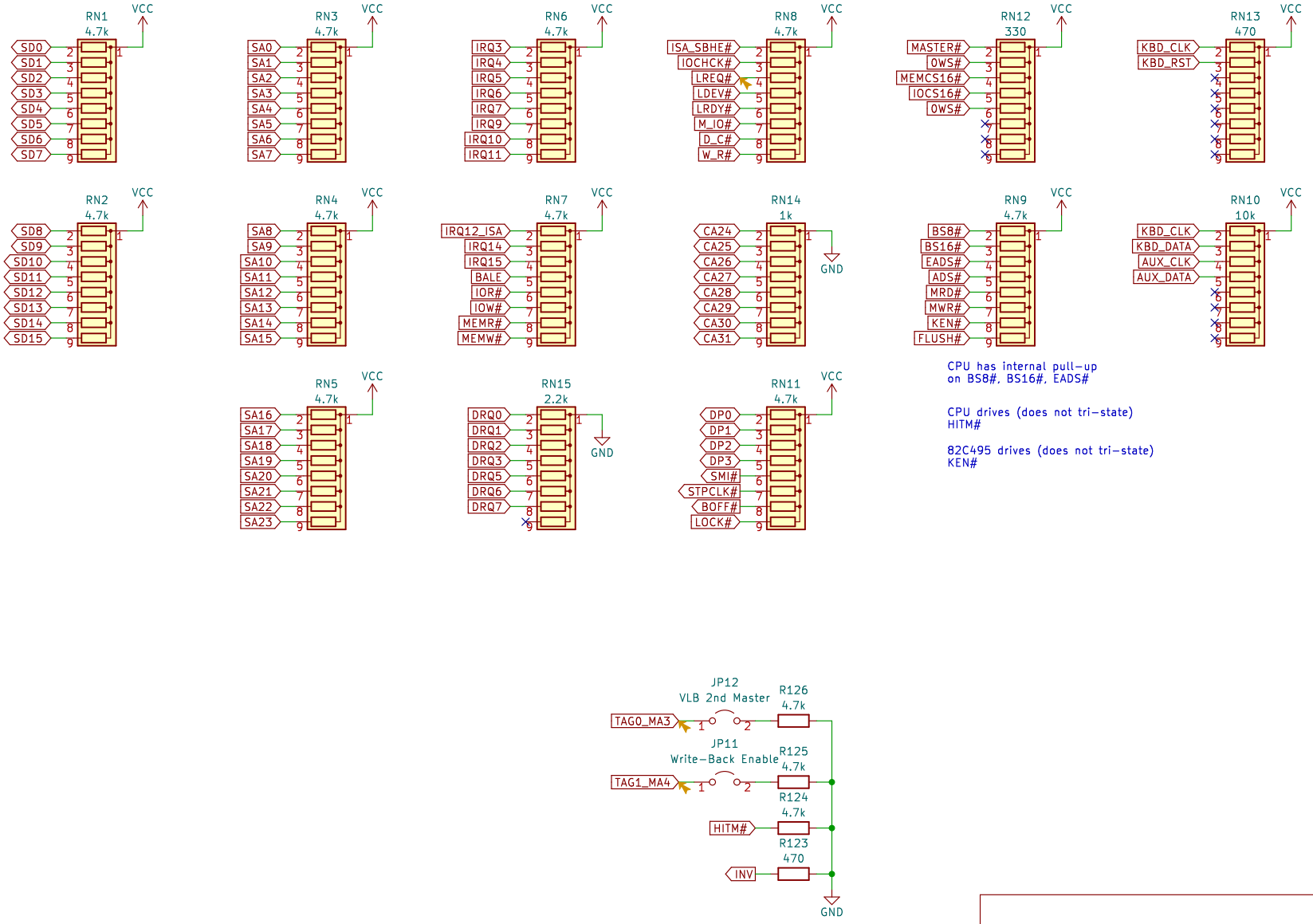

U1A
Intel_P24T
U1B
Intel_P24T
VCPU
CPUCLK
CD0
CD1
CD2
CD3
CD4
CD5
CD6
CD7
CD8
CD9
CD10
CD11
CD12
CD13
CD14
CD15
CD16
CD17
CD18
CD19
CD20
CD21
CD22
CD23
CD24
CD25
CD26
CD27
CD28
CD29
CD30
CD31
DP0
DP1
DP2
DP3
RDY#
BRDY#
RSTDRV
INTR
NMI
HOLD
BOFF#
AHOLD
EADS#
KEN#
FLUSH#
BS8#
BS16#
A20M#
IGNNE#
CLK
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
DP0
DP1
DP2
DP3
RDY#
BRDY#
RESET
INTR
NMI
HOLD
BOFF#
AHOLD
EADS#
KEN#
FLUSH#
BS8#
BS16#
A20M#
IGNNE#
CA2
CA3
CA4
CA5
CA6
CA7
CA8
CA9
CA10
CA11
CA12
CA13
CA14
CA15
CA16
CA17
CA18
CA19
CA20
CA21
CA22
CA23
CA24
CA25
CA26
CA27
CA28
CA29
CA30
CA31
BE0#
BE1#
BE2#
BE3#
PCHK#
M_IO#
D_C#
W_R#
LOCK#
PLOCK#
ADS#
BLAST#
BREQ
HLDA
PWT
PCD
INC/FERR#
VCC5
R41
100
VCC
GND
CPURST
SMI#
STPCLK#
EWBE#
BLEN#
WB_WT#
PIN_C14
INV
PIN_B11
CLKMUL
INIT
INC/INIT/SRESET
SMI#
STPCLK#
EWBE#
BLEN#
WB/WT#
INC/WB/WT#
INV
INC/INV
INC/UP#
INC/TCK
INC/TDI
CLKMUL
SMIACT#
HIT#
INC/HITM#
HITM#
CACHE#
INC/CACHE#
FERR#
INC/TDO
UP#/TMS
VOLDET
Test point?
PIN_B13
HITM#
PIN_B14
PIN_T5
JP1
FPU/NMI
PIN_D15
FERR#
PIN_B14
PIN_C16
NMI
PIN_B16
IGNNE#
JP1: FPU/NMI
1–2: 486DX/ODPR/5x86
2–3: 487SX/ODP/P24T
4–5,6–7: All non 486SX
5–6: 486SX
JP2
Write–back
PIN_B11
INV
PIN_T5
VOLDET
PIN_B13
HITM#
PIN_S18
JP2: Write–back
1–2,5–6: Intel 486DX4–compatible
2–3,6–7: IBM 486DX–compatible
R42
1k
JP3
Clock Multiplier
PIN_S18
PIN_C14
WB_WT#
JP3: Clock Multiplier
1–2: Intel 486DX4–compatible
2–3: AMD 486DX2/DX4
3–4: Intel/AMD 486DX2/4 write–back enable
JP4
5V / 3.3V CPU Voltage
+3.3V
PWR_FLAG
C1
100nF
C2
100nF
Check caps value/number
add CPU caps
Sheet: /Processor/
File: Processor.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 2/16


BUS1
BUSAT_HOST
BUS2
BUSAT_HOST
BUS3
BUSAT_HOST
BUS4
BUSAT_HOST
GND RESET +5V IRQ2 -5V DRQ2 -12V OWS# +12V GND SMEMW# SMEMR# IOW# IOR# DACK3# DRQ3 DACK1# DRQ1 REFRESH# BCLK IRQ7 IRQ6 IRQ5 IRQ4 IRQ3 DACK2# TC BALE +5V OSC GND
IOCHCK SD7 SD6 SD5 SD4 SD3 SD2 SD1 SD0 IOCHRDY AEN SA19 SA18 SA17 SA16 SA15 SA14 SA13 SA12 SA11 SA10 SA9 SA8 SA7 SA6 SA5 SA4 SA3 SA2 SA1 SA0
MEMCS16# IOCS16# IRQ10 IRQ11 IRQ12_ISA IRQ15 IRQ14 DACK0# DRQ0 DACK5# DRQ5 DACK6# DRQ6 DACK7# DRQ7 +5V MASTER# GND
MEMCS16 IOCS16 IRQ10 IRQ11 IRQ12 IRQ15 IRQ14 DACK0 DRQ0 DACK5 DRQ5 DACK6 DRQ6 DACK7 DRQ7 +5V MASTER GND
SBHE LA23 LA22 LA21 LA20 LA19 LA18 LA17 MEMR MEMW SD8 SD9 SD10 SD11 SD12 SD13 SD14 SD15
ISA_SBHE# SA23 SA22 SA21 SA20 SA19 SA18 SA17 MEMR# MEMW# SD8 SD9 SD10 SD11 SD12 SD13 SD14 SD15
Sheet: /ISA/
File: ISA.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 3/16


DRAM Bank 0/1
DRAM Bank 1
U302
74F541
U301
74F573
J301
Conn_SIMM72
J302
Conn_SIMM72
RN301
RN302
RN303
RN304
RN305
VCC
GND
Required only for parity check
Replace with wire links if
parity check is not used
SIMM72 – DRAM RAS/CAS signal mapping:
CAS0,RAS0 – D0–D7
CAS1,RAS0 – D8–D15
CAS2,RAS2 – D16–D23
CAS3,RAS2 – D24–D31
PCB Routing:
– Place Bank 0/1 SIMM at the far side from the CPU
DRAM Configuration Options:
– Single one–rank SIMM in Bank 0/1 – 64 MB maximum
– Single two–rank SIMM in Bank 0/1 – 32 MB maximum
– Two one–rank SIMMs in Bank 0/1 and Bank 1 –32 MB (16 MB x 2) maximum
Sheet: /Memory/
File: Memory.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 4/16


U2
OPTi_82C895
U3
OPTi_82C602
FLUSH#/SMI#
BEA3
BEA2_OA3
TAGW#
BEOE#
BOOE#
BE3#
BE2#
BE1#
BE0#
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
CAS0#
CAS1#
CAS2#
CAS3#
MA8
MA9
MA10
RAS0#
RAS1#
RAS2#
RAS3#
LREQ1#
LGNT1#
MA11
DWE#
DRQ5
DRQ6
OSC
DRQ7
EDACK0
EDACK1
EDACK2
IRQ1
IRQ43
IRQ6
SMIACT#
DIRTY
TAG6
TAG5
TAG4
TAG3
TAG2
TAG1
TAG0
VCC
DRAMS#
LREQ0#
A25
A24
GND
A23
A22
A21
A20
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
CPURST
RDY#
BRDY#
ADS#
W_R#
M_IO#
D_C#/TAG7
KEN#
EADS#
BLAST#
INTR
HLDA
HOLD
DRQ3
LDEV#
A26
NMI
IGNNE#
FERR#
DRQ2
D31
D30
D29
D28
D27
D26
D25
D24
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
MP3
MP2
MP1
MP0
EMPMI#/MDIR#
PWRGD
CHCK#
HLBOE2#
HLBOE1#
HLBLTH#
XDIR#
LMGCS#
A20M#
ROMCS#/KBDCS#
DWS#/LRDY#
IOCHRDY
SPKD
HITM#/DC#
AHOLD
LGNT0#
TC
SBHE#
MCS16#
IOCS16#
CLKI
MEMW#
MEMR#
IOW#
IOR#
SD15
SD14
SD13
SD12
SD11
SD10
SD9
SD8
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
IRQ75
IRQ8
IRQ9
IRQ1110
IRQ14
IRQ1512
RFSH#
ALE
ATCLK
BCLK
33 R401
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
IOR#
IOW#
PWRGD
CA26
CA25
CA24
CA23
CA22
CA21
CA20
CA19
CA18
CA17
CA16
CA15
CA14
CA13
CA12
CA11
CA10
CA9
CA8
CA7
CA6
CA5
CA4
CA3
CA2
CA1
CA0
#MASTER
XD7
XD6
XD5
XD4
XD3
XD2
XD1
XD0
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
AEN
RSTDRV
LRESET#
SMEMW#
SMEMR#
XDIR#
LMCS#/KBCS#
MEMW#
MEMR#
CD23
CD22
CD21
CD20
CD19
CD18
CD17
CD16
M_IO#
IRQ8
VBATT
X2
X1
REF
Y1
32768Hz
ATIOR#/DS#/PP1#
ATIOW#/RW#/GPCS#
CPUCLK
KBCLK
PPEN#
RST#
KKBCLK
RRTCCS#/PP2#
RRTCAS
PP0#
80XHLDA
HLBLTH#/HDDIR#
HLBOE2#
HLBOE1#/HDLEN#
HLDA
PWR_FLAG
BT1
CR2032
CHRDY
IOCHRDY
R101
51
R102
1k
U401D
74F32
U401C
74F32
Sheet: /Chipset/
File: Chipset.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 5/16

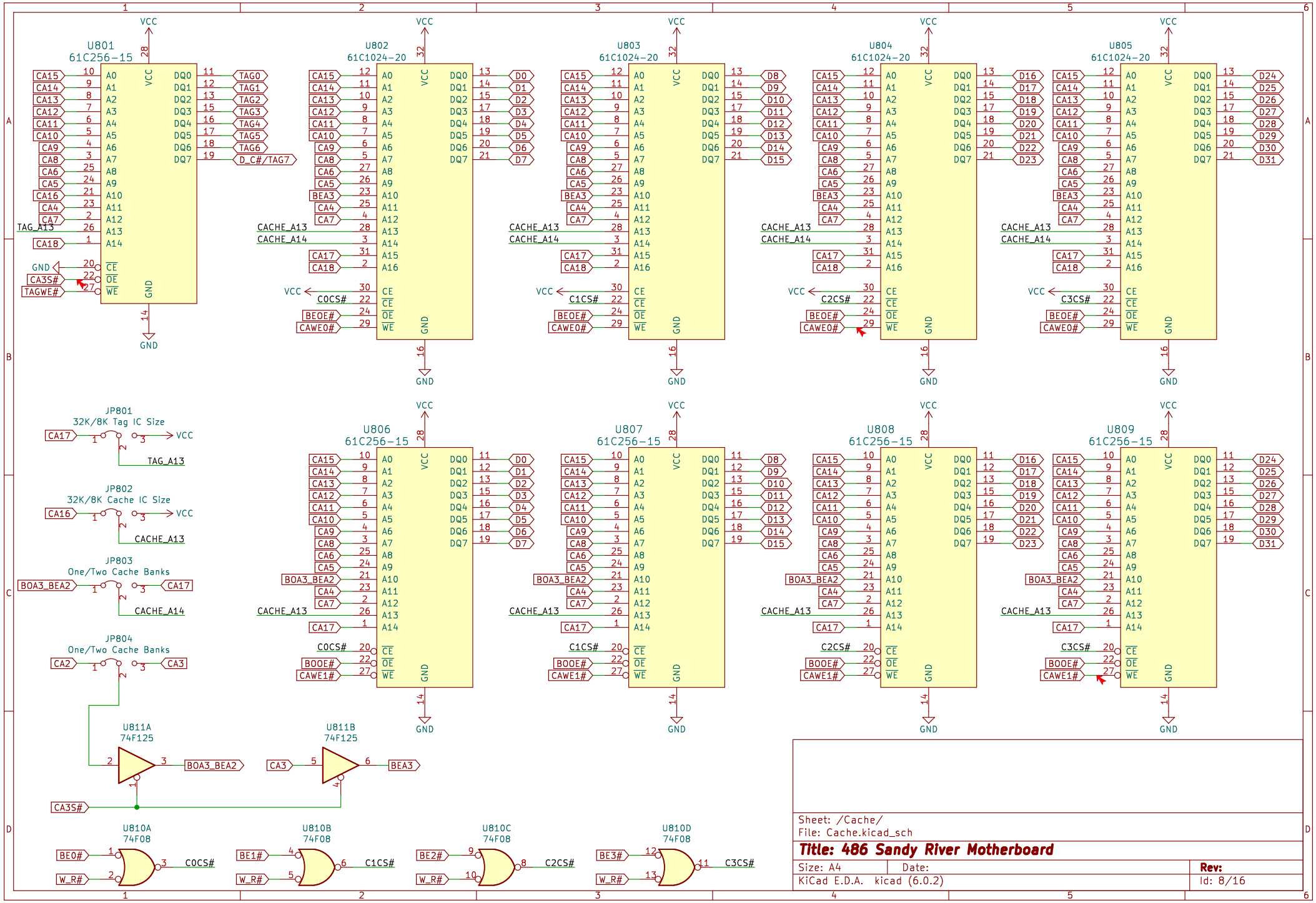

R611 10k
D1 1N4148
R610 10k
D2 1N4148
U604F 74HCT14
U604E 74HCT14
U604D 74HCT14
U603A 74HCT74
PWR_BTN#
R612
R470
SW1 POWER
C602 1uF
C601 10uF
GND
PS_ON#
J11 ATX_POWER_20
3.3V
−12V
GND
PS_ON
GND
GND
GND
−5V
VCC
VCC
3.3V
3.3V
GND
5V
GND
5V
GND
PWR_OK
5VSB
12V
+3.3V
+3.3V
VCC
VCC
+12V
−5V_ATX
5VSB
PWRGD
U130F 74LS07
RESET
VCC
D3 1N4148
R621 330
R620 100
RST_BTN#
RST
SW2 RESET
C603 1uF
GND
VCC
R652 1k
J12 Front Panel
R651 1k
VCC
IDE_LED#
HDD_LED+
HDD_LED−
GND
RST_BTN#
+3.3V
PLED+
No pin
GND
No pin
No pin
PLED+
GND
PWR_BTN#
GND
No pin
VCC
No pin
INT_SPKR
SPEAKER
No pin
(check 3.3V pinout)
VCC
LS1 AT−1224TWTR
R642 33
R641 2.2k
SPKD
Q3 2N3904
C641 100nF
GND
GND
JP9 −5V Source
−12V
GND
VI
VO
−5V_ATX
U106 LM7905_TO220
PWR_FLAG
−5V
VCC
X1 14.31818MHz
Buffer OSC for ISA?
R601 33
OSC
GND
VCC
X2 33.333MHz
R602 33
CPUCLK
GND
U604A 74HCT14
U603B 74HCT74
U604C 74HCT14
U604B 74HCT14
U401E 74F32
U810E 74F08
U130G 74LS07
U603C 74HCT74
U604G 74HCT14
Sheet: /Power/
File: Power.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 6/16



Sheet: /Pull-ups/
File: Pull-ups.kicad_sch

Title: 486 Sandy River Motherboard

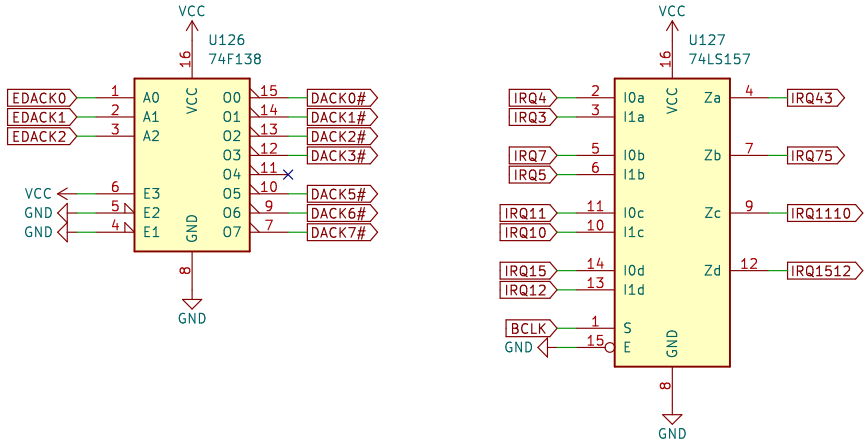
Size: A4	Date:	Rev:
KiCad E.D.A. kicad (6.0.2)		Id: 7/16

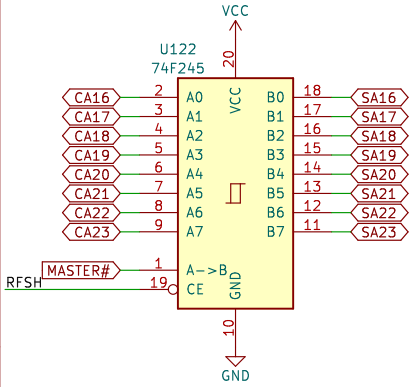


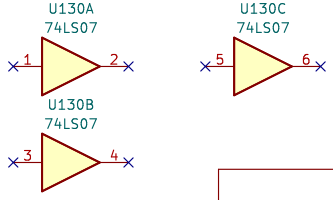
Sheet: /Cache/
File: Cache.kicad_sch

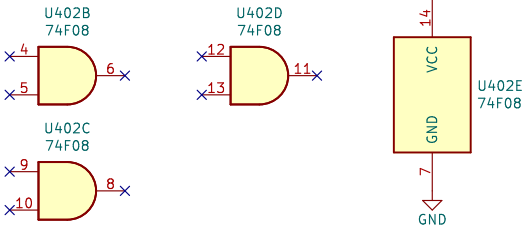
Title: 486 Sandy River Motherboard

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (6.0.2)		Id: 8/16





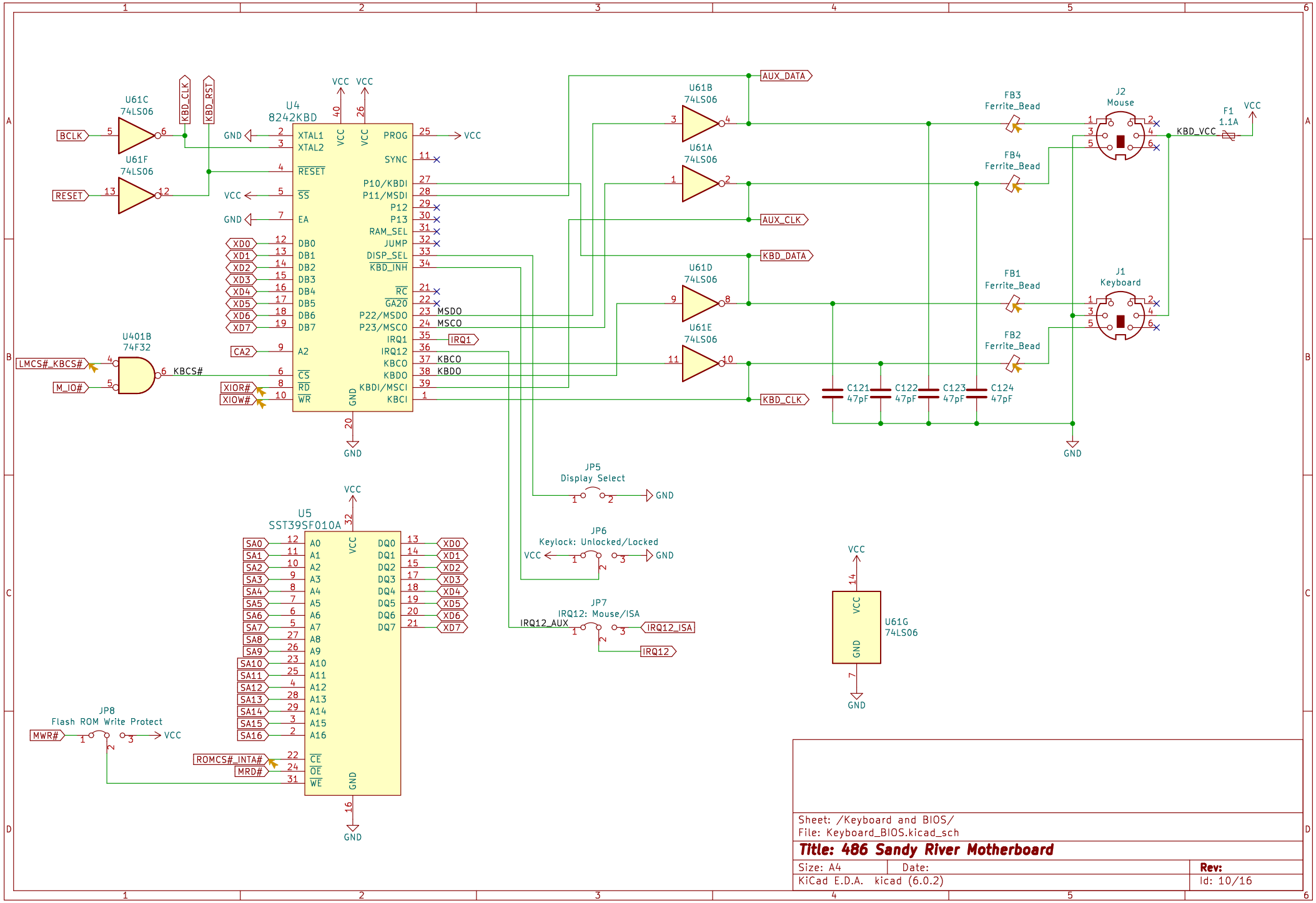


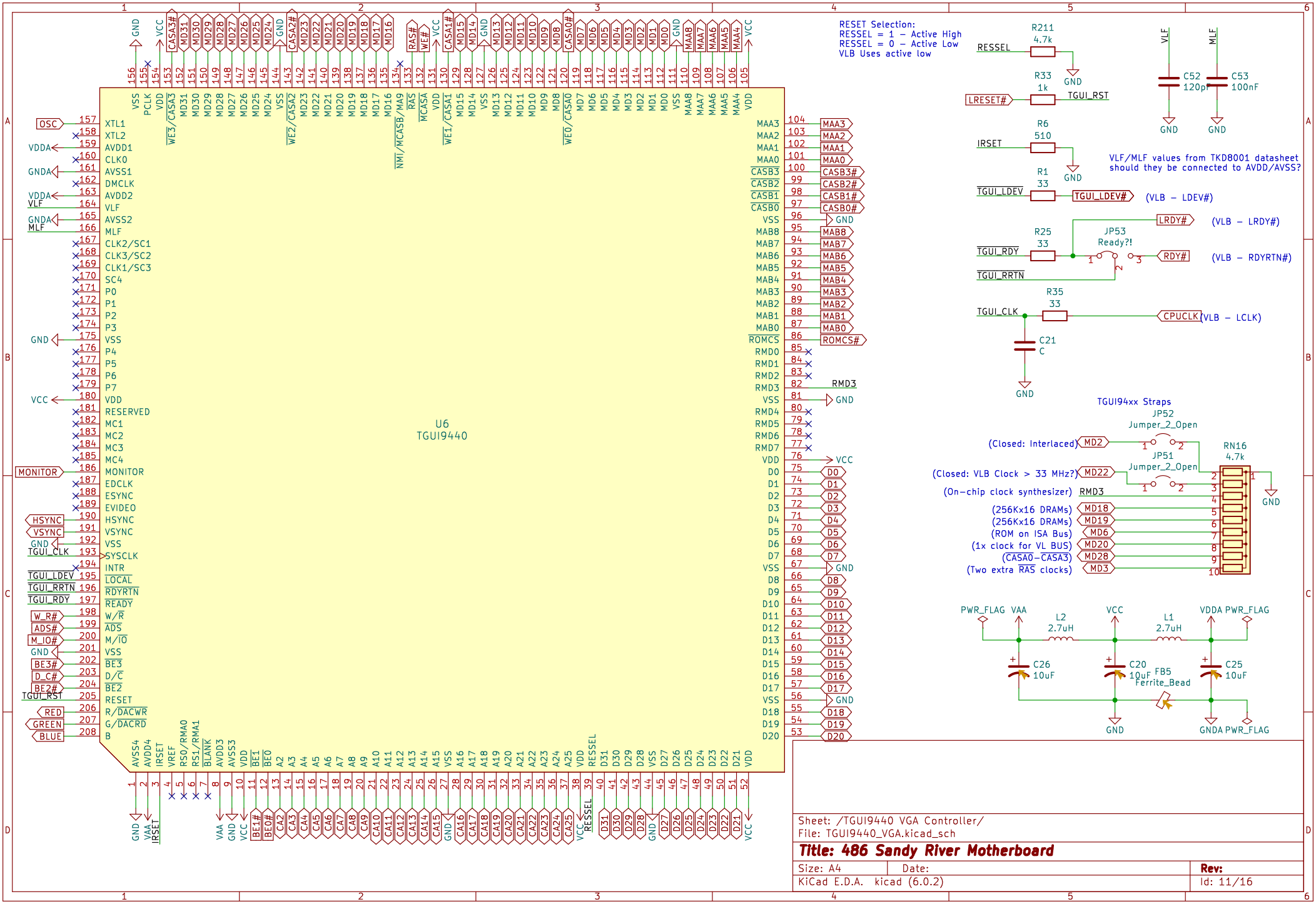


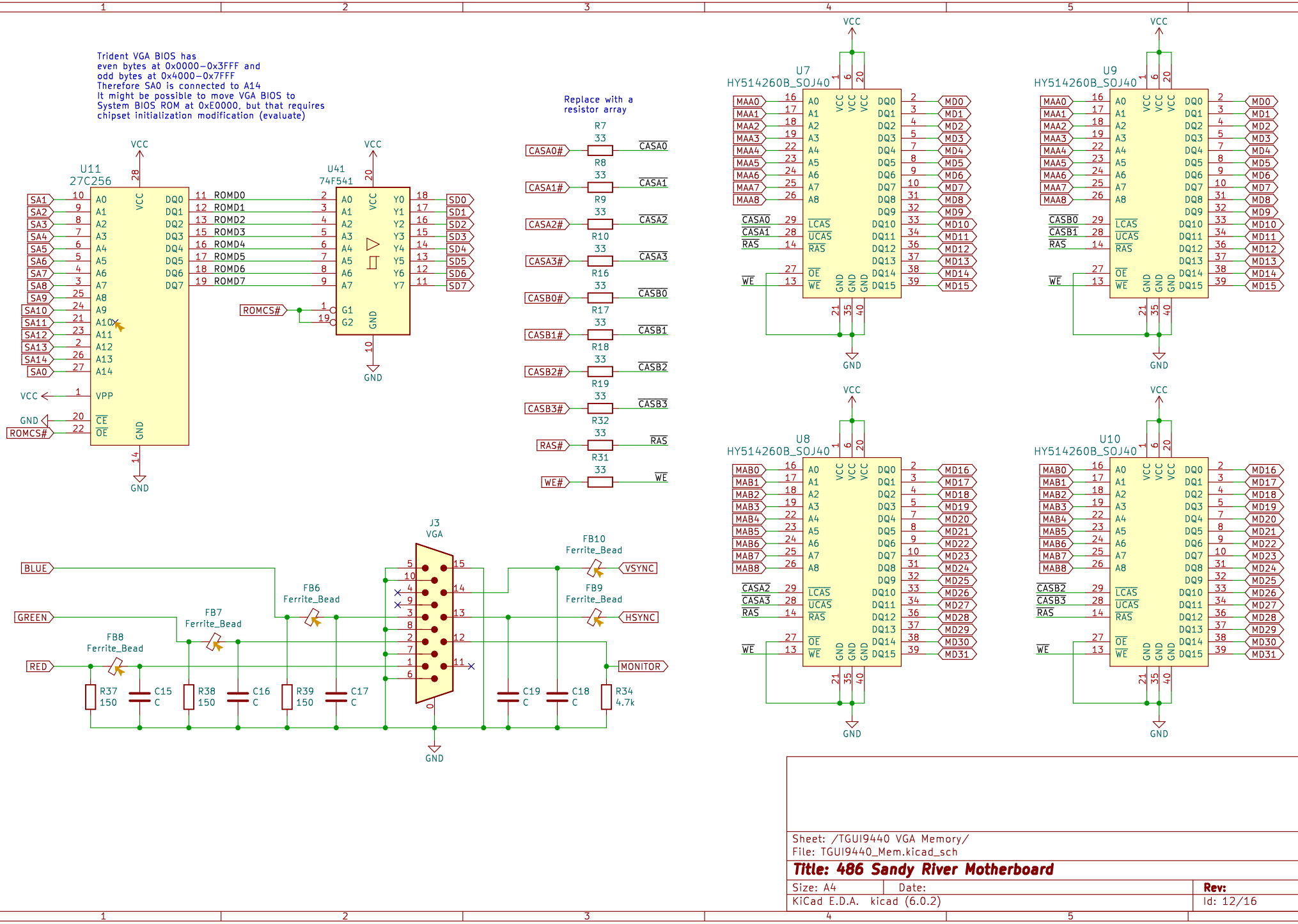
Sheet: /Buffers/
File: Buffers.kicad_sch

Title: 486 Sandy River Motherboard

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.2)		Id: 9/16


U61C
74LS06
U61F
74LS06
U4
8242KBD
U401B
74F32
U5
SST39SF010A
U61B
74LS06
U61A
74LS06
U61D
74LS06
U61E
74LS06
U61G
74LS06
FB3
Ferrite_Bead
FB4
Ferrite_Bead
FB1
Ferrite_Bead
FB2
Ferrite_Bead
J2
Mouse
J1
Keyboard
F1
1.1A
C121
47pF
C122
47pF
C123
47pF
C124
47pF
JP5
Display Select
JP6
Keylock: Unlocked/Locked
JP7
IRQ12: Mouse/ISA
JP8
Flash ROM Write Protect
BCLK
RESET
KBD_CLK
KBD_RST
LMCS#_KBCS#
M_IO#
KBCS#
XIOR#
XIOW#
CA2
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
MSDO
MSCO
IRQ1
KBCO
KBDO
KBDI/MSCI
KBCI
AUX_DATA
AUX_CLK
KBD_DATA
KBD_CLK
KBD_VCC
IRQ12_AUX
IRQ12_ISA
IRQ12
MWR#
ROMCS#_INTA#
MRD#
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
SA16
VCC
GND
Sheet: /Keyboard and BIOS/
File: Keyboard_BIOS.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 10/16

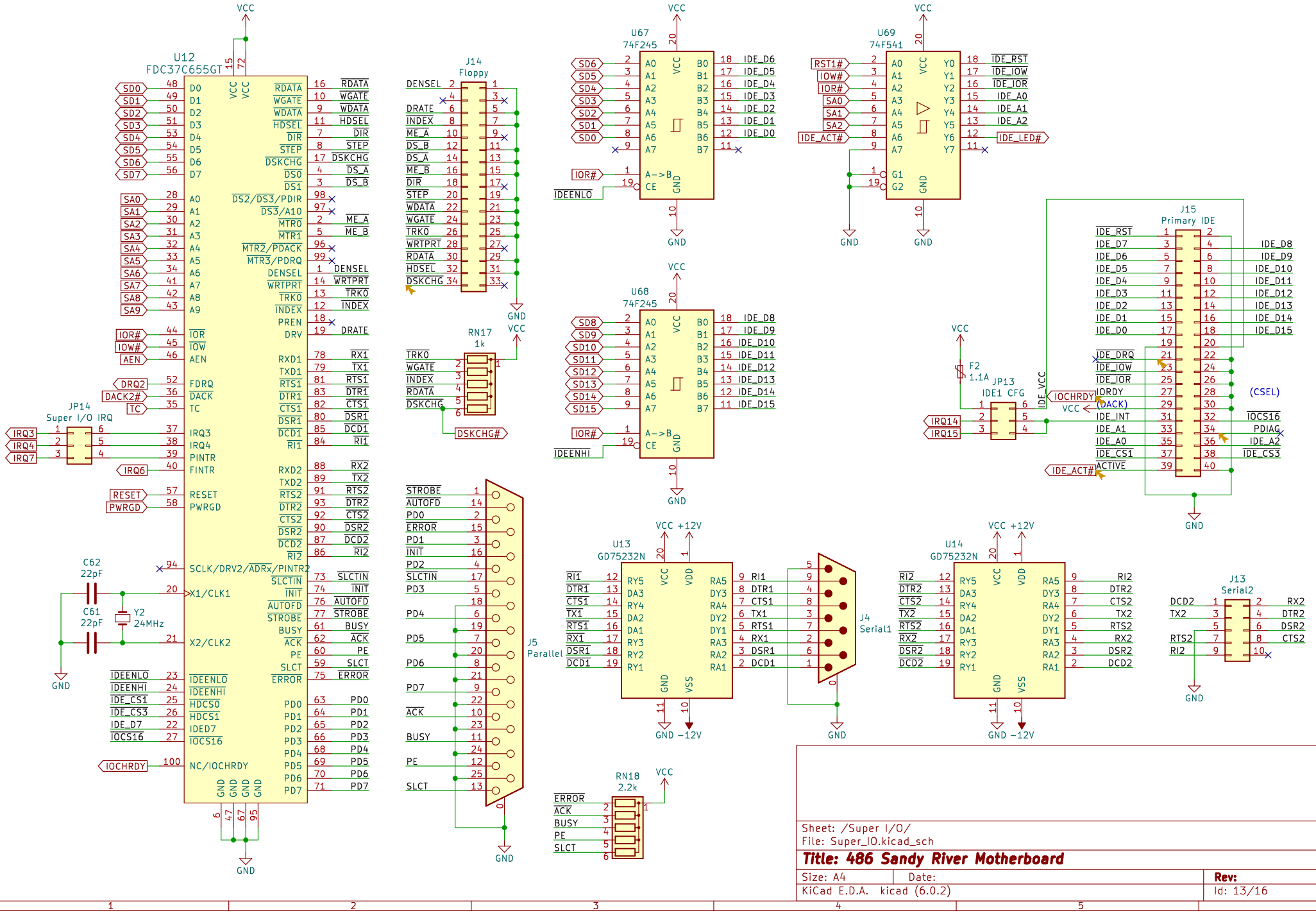

U6
TGUI9440
RESET Selection:
RESSEL = 1 – Active High
RESSEL = 0 – Active Low
VLB Uses active low
R211 4.7k
R33 1k
R6 510
R1 33
R25 33
R35 33
C52 120pF
C53 100nF
C21 C
JP53 Ready?!
VLF/MLF values from TKD8001 datasheet should they be connected to AVDD/AVSS?
(VLB – LDEV#)
(VLB – LRDY#)
(VLB – RDYRTN#)
(VLB – LCLK)
TGUI94xx Straps
JP52 Jumper_2_Open
JP51 Jumper_2_Open
RN16 4.7k
(Closed: Interlaced)
(Closed: VLB Clock > 33 MHz?)
(On–chip clock synthesizer)
(256Kx16 DRAMs)
(256Kx16 DRAMs)
(ROM on ISA Bus)
(1x clock for VL BUS)
(CASA0–CASA3)
(Two extra RAS clocks)
L2 2.7uH
L1 2.7uH
C26 10uF
C20 10uF
C25 10uF
FB5 Ferrite_Bead
Sheet: /TGUI9440 VGA Controller/
File: TGUI9440_VGA.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 11/16

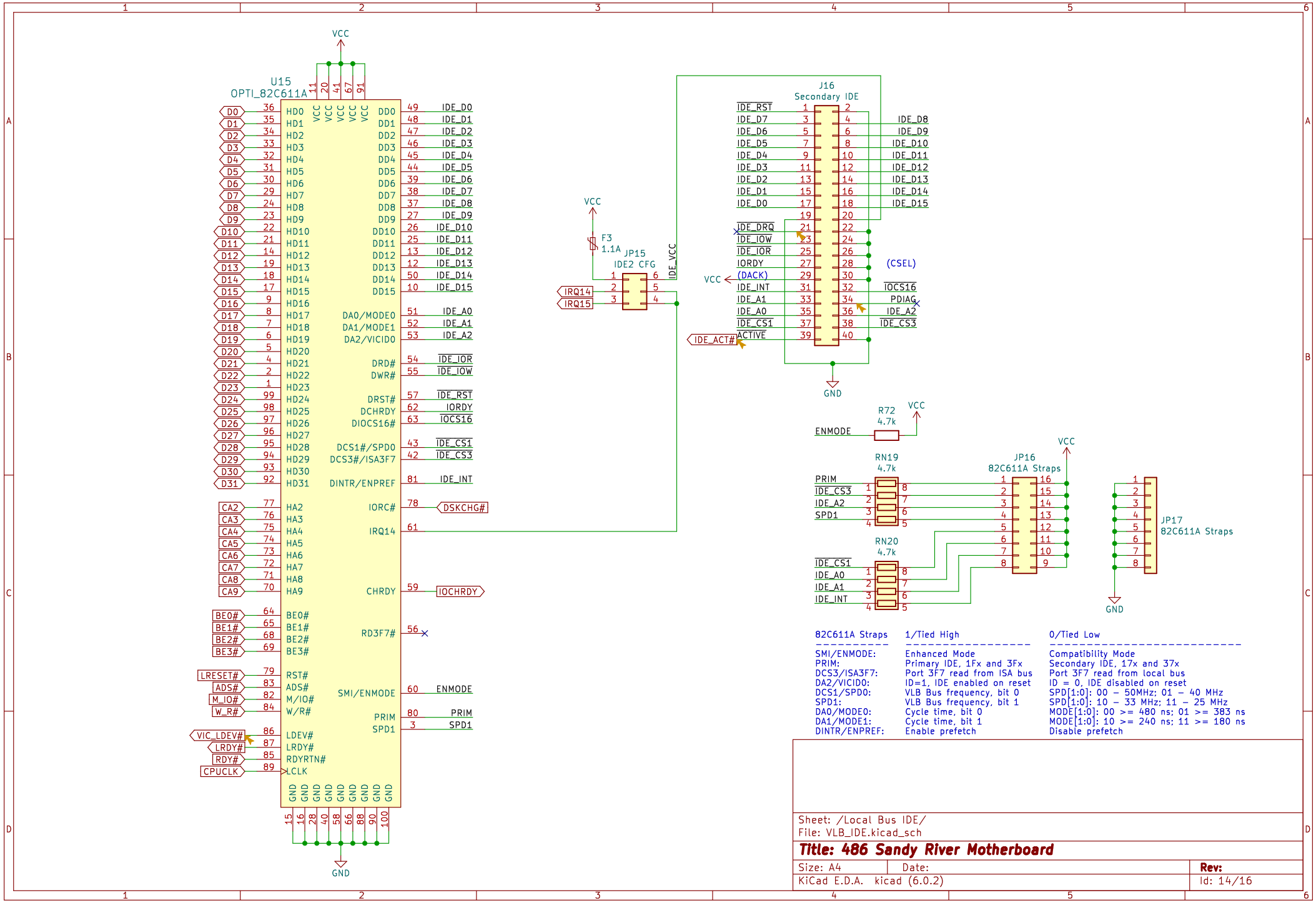


Sheet: /TGUI9440 VGA Memory/
File: TGUI9440_Mem.kicad_sch

Title: 486 Sandy River Motherboard

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (6.0.2)		Id: 12/16


U12
FDC37C655GT
U67
74F245
U68
74F245
U69
74F541
J14
Floppy
RN17
1k
RN18
2.2k
JP14
Super I/O IRQ
JP13
IDE1 CFG
F2
1.1A
J15
Primary IDE
C62
22pF
C61
22pF
Y2
24MHz
J5
Parallel
U13
GD75232N
U14
GD75232N
J4
Serial1
J13
Serial2
VCC
GND
VCC +12V
GND −12V
(CSEL)
Sheet: /Super I/O/
File: Super_IO.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 13/16

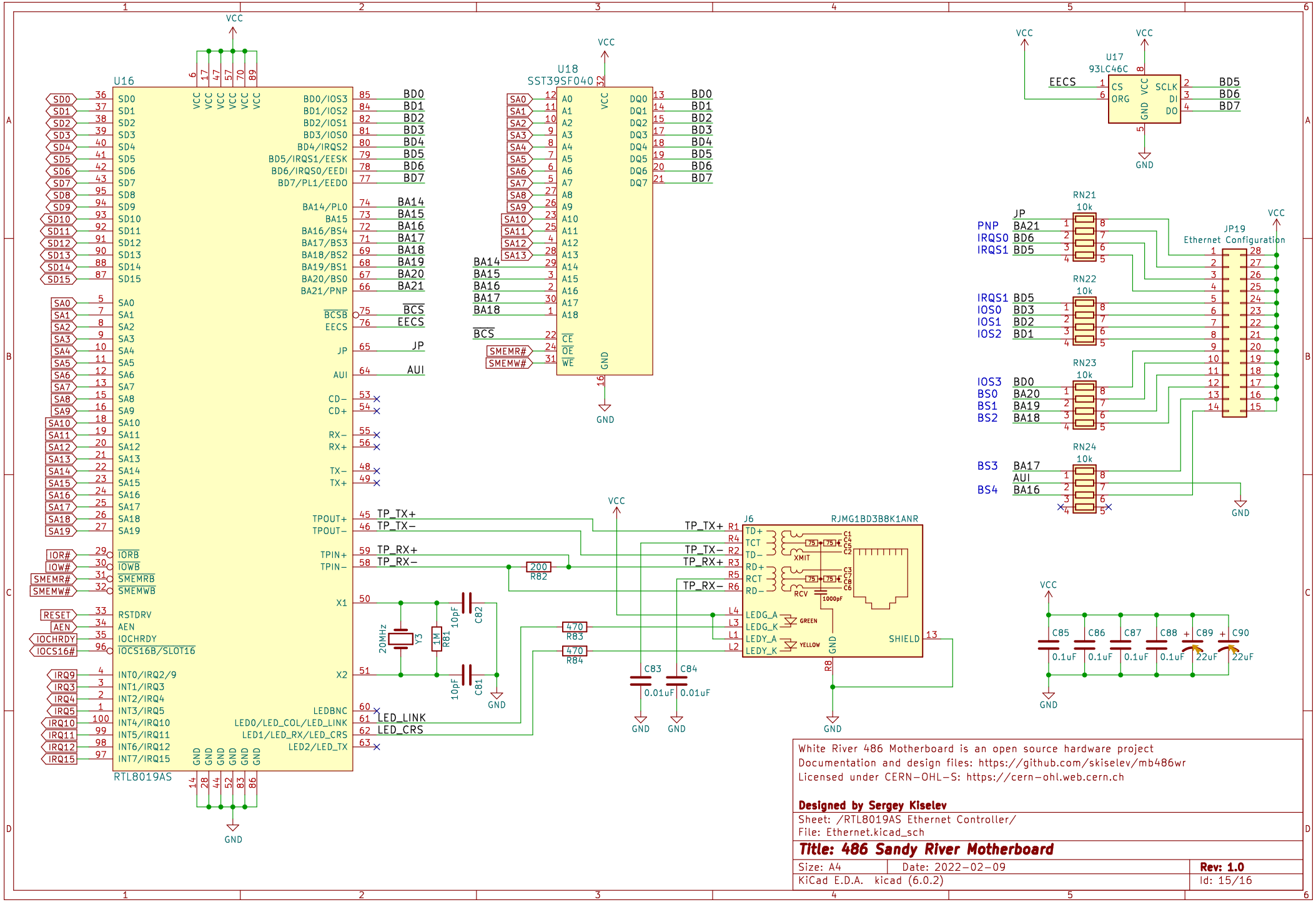


82C611A Straps	1/Tied High	0/Tied Low
SMI/ENMODE:	Enhanced Mode	Compatibility Mode
PRIM:	Primary IDE, 1Fx and 3Fx	Secondary IDE, 17x and 37x
DCS3/ISA3F7:	Port 3F7 read from ISA bus	Port 3F7 read from local bus
DA2/VICID0:	ID=1, IDE enabled on reset	ID = 0, IDE disabled on reset
DCS1/SPD0:	VLB Bus frequency, bit 0	SPD[1:0]: 00 – 50MHz; 01 – 40 MHz
SPD1:	VLB Bus frequency, bit 1	SPD[1:0]: 10 – 33 MHz; 11 – 25 MHz
DA0/MODE0:	Cycle time, bit 0	MODE[1:0]: 00 >= 480 ns; 01 >= 383 ns
DA1/MODE1:	Cycle time, bit 1	MODE[1:0]: 10 >= 240 ns; 11 >= 180 ns
DINTR/ENPREF:	Enable prefetch	Disable prefetch

Sheet: /Local Bus IDE/
File: VLB_IDE.kicad_sch

Title: 486 Sandy River Motherboard

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (6.0.2)		Id: 14/16



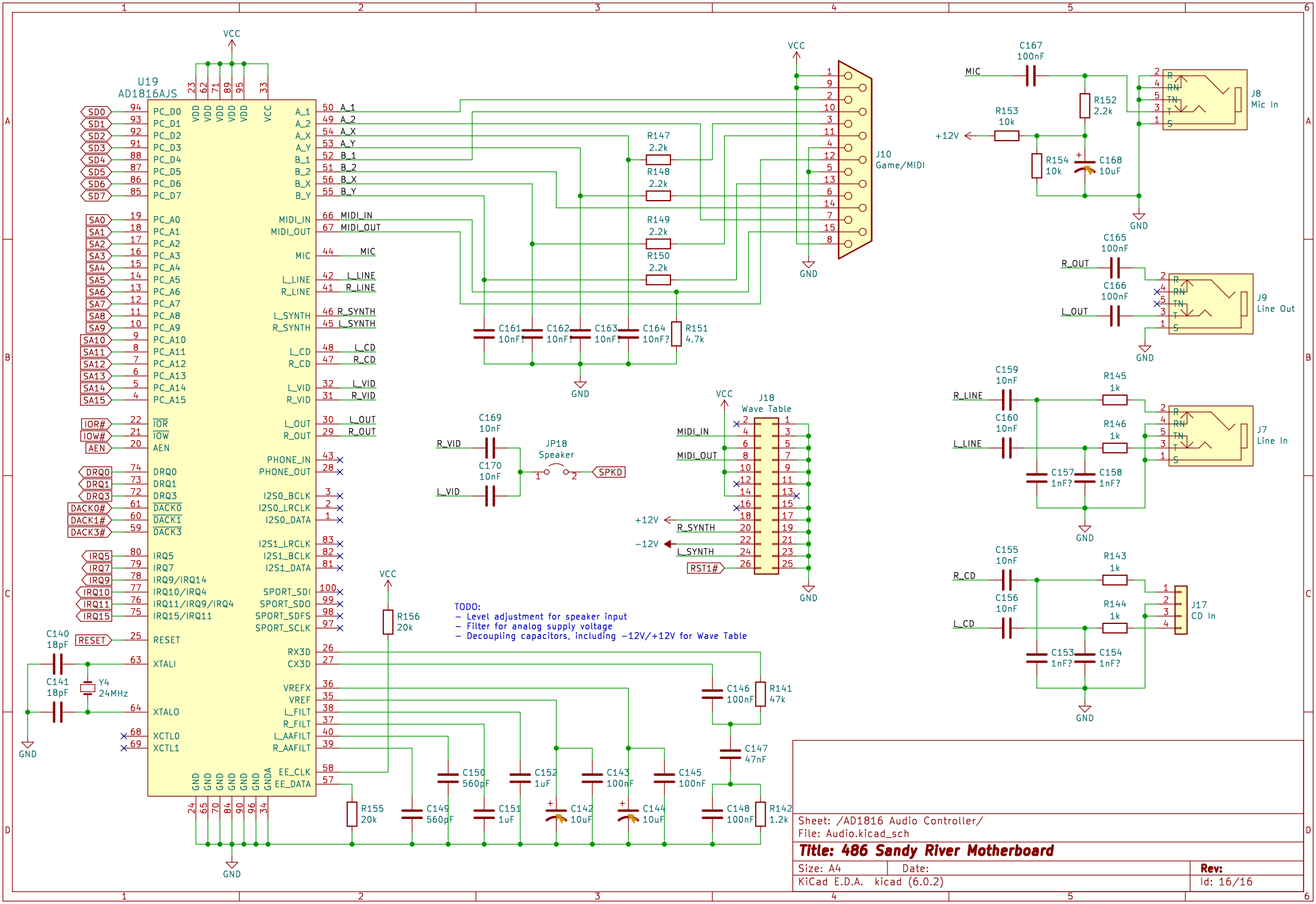
White River 486 Motherboard is an open source hardware project
Documentation and design files: https://github.com/skiselev/mb486wr
Licensed under CERN-OHL-S: https://cern-ohl.web.cern.ch

Designed by Sergey Kiselev

Sheet: /RTL8019AS Ethernet Controller/
File: Ethernet.kicad_sch

Title: 486 Sandy River Motherboard

Size: A4	Date: 2022-02-09	**Rev: 1.0**
KiCad E.D.A. kicad (6.0.2)		Id: 15/16


U19
AD1816AJS
VCC
GND
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
IOR#
IOW#
AEN
DRQ0
DRQ1
DRQ3
DACK0#
DACK1#
DACK3#
IRQ5
IRQ7
IRQ9
IRQ10
IRQ11
IRQ15
RESET
XTALI
XTALO
XCTL0
XCTL1
A_1
A_2
A_X
A_Y
B_1
B_2
B_X
B_Y
MIDI_IN
MIDI_OUT
MIC
L_LINE
R_LINE
R_SYNTH
L_SYNTH
L_CD
R_CD
L_VID
R_VID
L_OUT
R_OUT
PHONE_IN
PHONE_OUT
I2S0_BCLK
I2S0_LRCLK
I2S0_DATA
I2S1_LRCLK
I2S1_BCLK
I2S1_DATA
SPORT_SDI
SPORT_SDO
SPORT_SDFS
SPORT_SCLK
RX3D
CX3D
VREFX
VREF
L_FILT
R_FILT
L_AAFILT
R_AAFILT
EE_CLK
EE_DATA
J10
Game/MIDI
J8
Mic In
J9
Line Out
J7
Line In
J17
CD In
J18
Wave Table
JP18
Speaker
SPKD
RST1#
+12V
-12V
R147 2.2k
R148 2.2k
R149 2.2k
R150 2.2k
R151 4.7k
R152 2.2k
R153 10k
R154 10k
R155 20k
R156 20k
C140 18pF
C141 18pF
Y4 24MHz
C142 10uF
C144 10uF
C146 100nF
C147 47nF
C148 100nF
C149 560pF
C150 560pF
C151 1uF
C152 1uF
C153 1nF?
C154 1nF?
C155 10nF
C156 10nF
C157 1nF?
C158 1nF?
C159 10nF
C160 10nF
C161 10nF?
C162 10nF?
C163 10nF?
C164 10nF?
C165 100nF
C166 100nF
C167 100nF
C168 10uF
C169 10nF
C170 10nF
R141 47k
R142 1.2k
R143 1k
R144 1k
R145 1k
R146 1k
TODO:
– Level adjustment for speaker input
– Filter for analog supply voltage
– Decoupling capacitors, including −12V/+12V for Wave Table
Sheet: /AD1816 Audio Controller/
File: Audio.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 16/16