Processor

File: Processor.kicad_sch

Cache

File: Cache.kicad_sch

Local Bus IDE

File: VLB_IDE.kicad_sch

ISA

File: ISA.kicad_sch

Buffers

File: Buffers.kicad_sch

RTL8019AS Ethernet Controller

File: Ethernet.kicad_sch

Memory

File: Memory.kicad_sch

Keyboard and BIOS

File: Keyboard_BIOS.kicad_sch

AD1816 Audio Controller

File: Audio.kicad_sch

Chipset

File: Chipset.kicad_sch

TGUI9440 VGA Controller

File: TGUI9440_VGA.kicad_sch

Power

File: Power.kicad_sch

TGUI9440 VGA Memory

File: TGUI9440_Mem.kicad_sch

Pull-ups

File: Pull-ups.kicad_sch

Super I/O

File: Super_IO.kicad_sch

TODO:
- Add address decoder for DRAMS#
- Remove Ethernet boot ROM
- Add 3 pin header for CPU fan - switchable between 5V and 12V with a jumper
- DRAM - 2 or 4 sockets (2 double rank, or 2 double rank + 1 single rank)
- Check OWS#, is it ignored?
- Add decoupling/bypass capacitors

Check:
- P24T support
- Chipset power management signals, pins: 62, 156, 160
- (82C602) XD7, XD6 and XD4 strap options
- (82C602) XD4 strap - add 2.2k pull-down to enable RTC
- (82C602) Load capacitors for RTC crystal?
- 22 ohm x 2 resistor arrays in cache circuit - are they used?

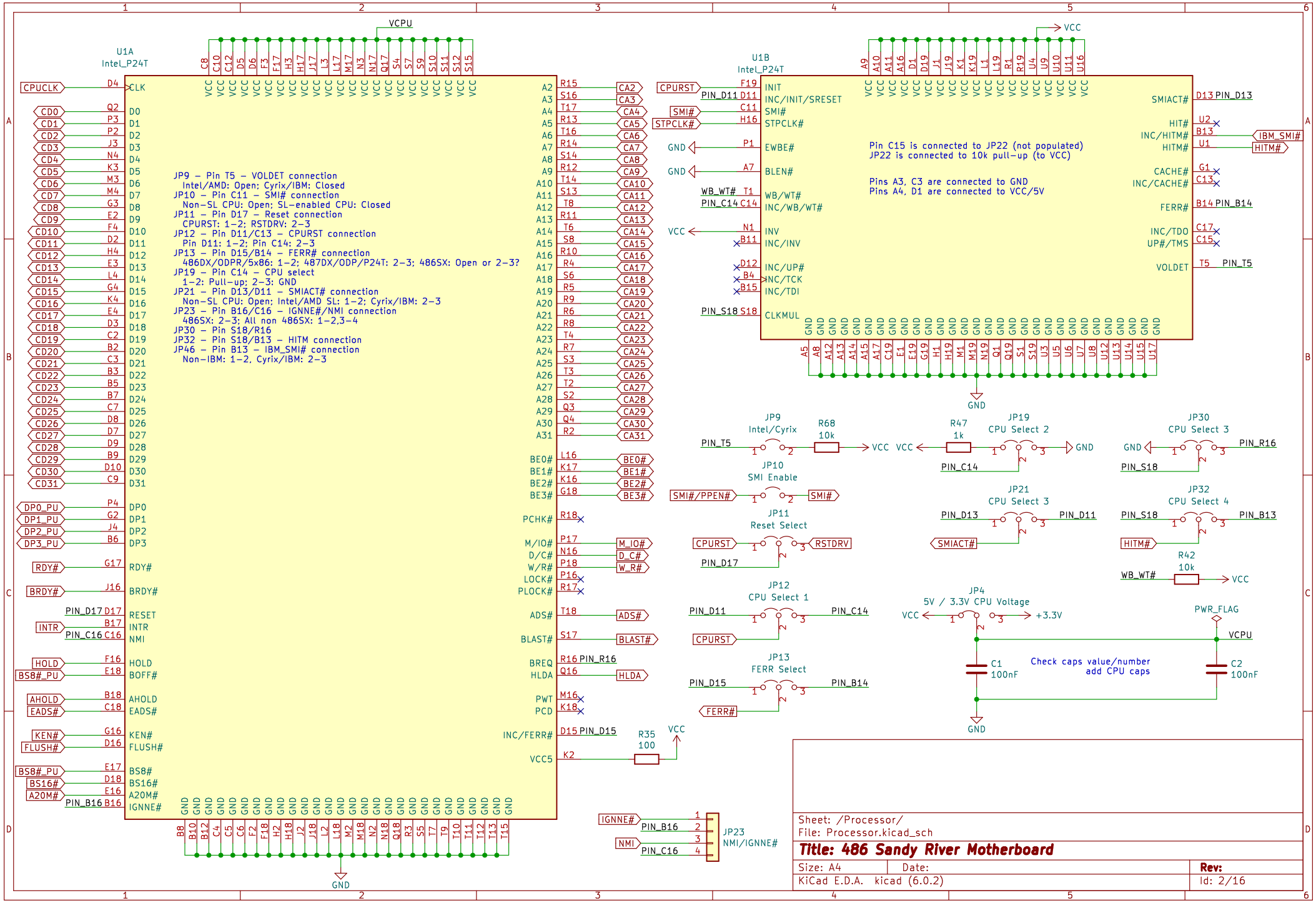
74xx Logic:
74F244 x 2 - DRAM address and control buffers?
74F138 - DACK decoder
74LS157 - Interrupt selector
7407 - Keyboard buffers; Reset circuit; BCLK buffer, anything else?
74F08(1) - Cache byte enable / chip select
74F08(2) - FLUSH# circuit; LDEV# circuit
74LS14 - Reset circuit, FLUSH# circuit
74F245 - CA[23:16] - LA[23:17],SA[19:16]

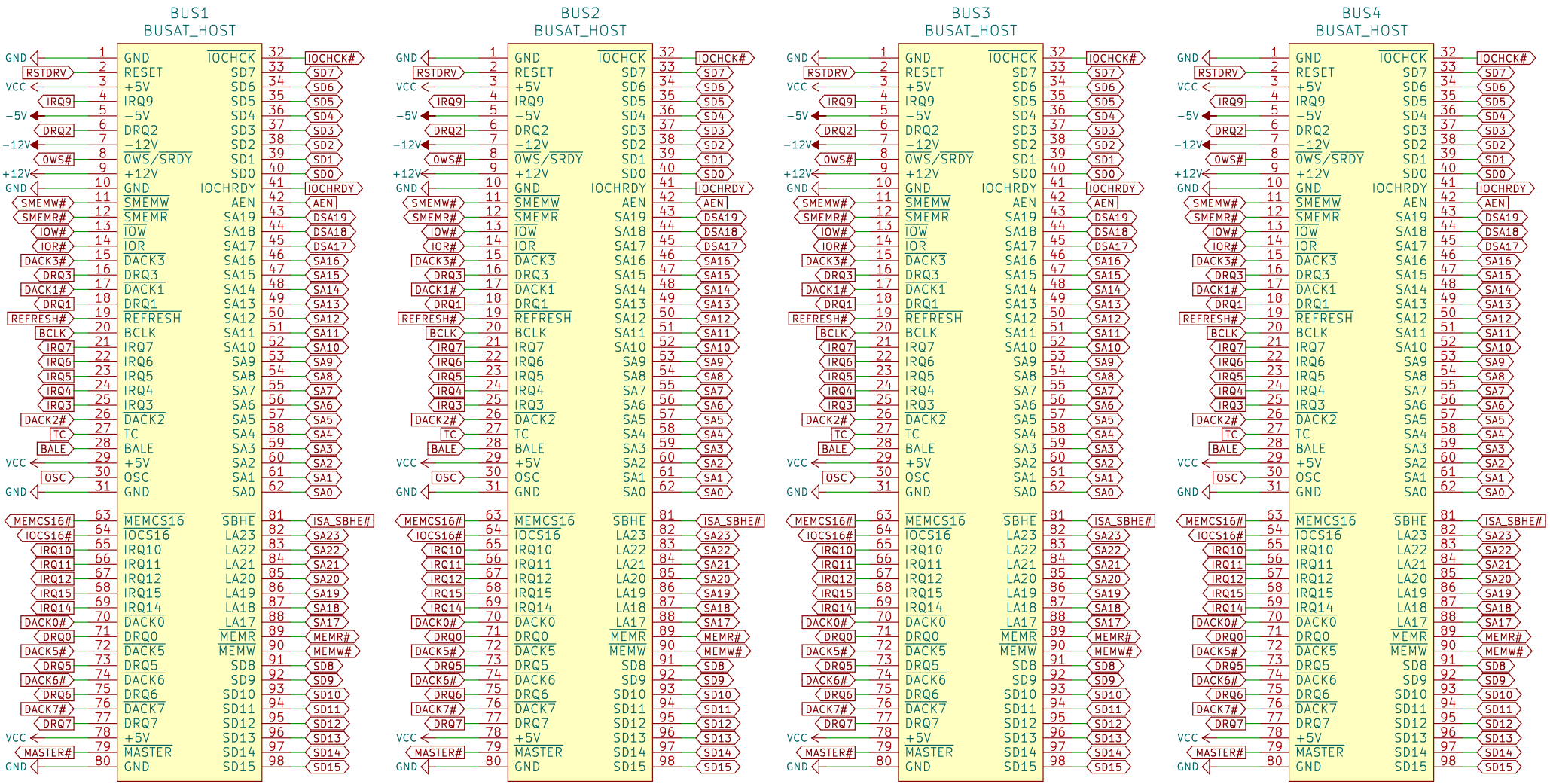
Checked:
- RTC crystal connection - what is the value of load capacitors?
- Cache data signals
- Cache control signals + cache configuration jumpers
- Cache address lines
- DRAM schematic
- ISA pull-ups
- Local bus pull-ups
- CPU configuration jumpers

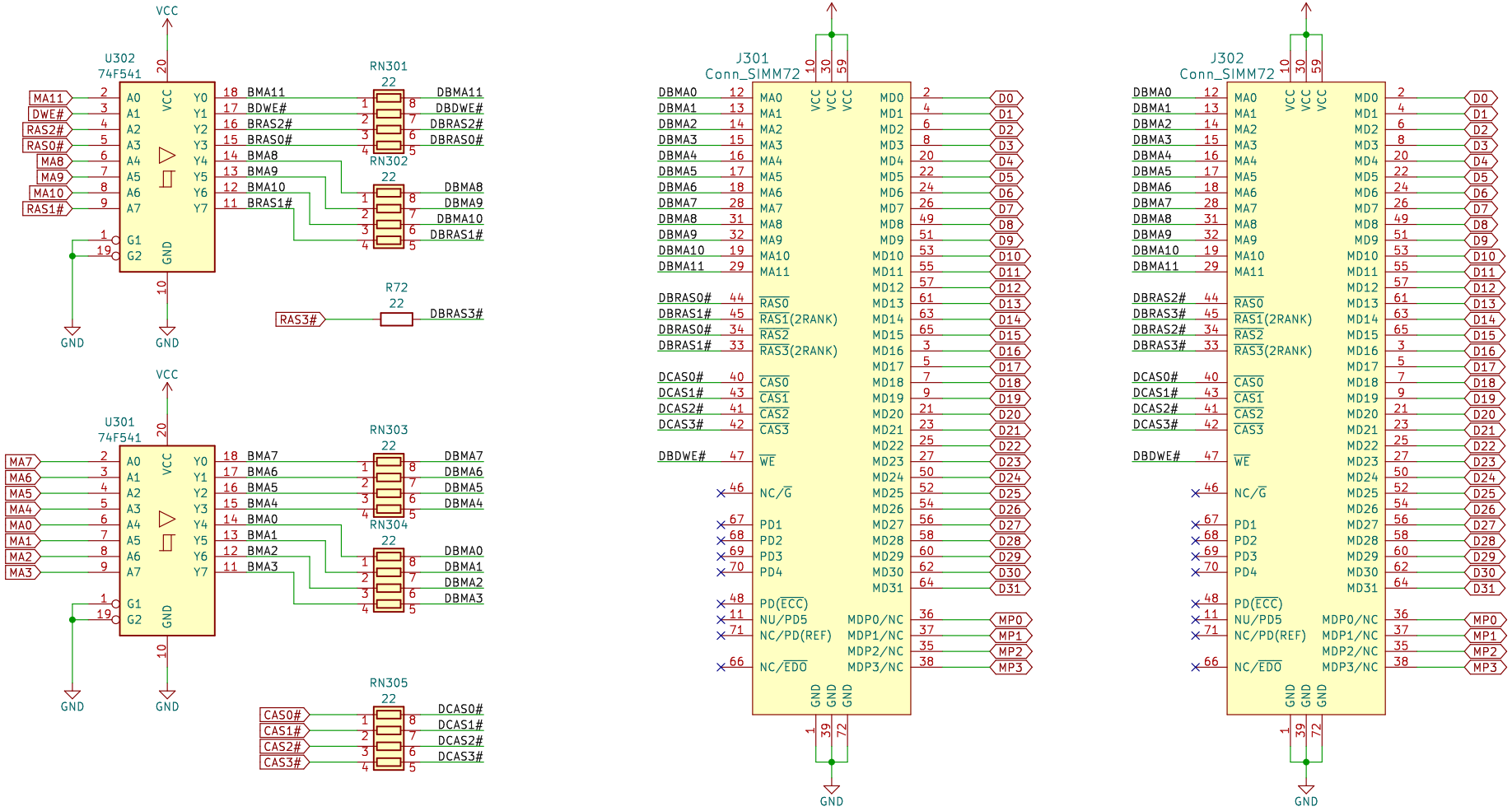
Sheet: /
File: mb486sr.kicad_sch

Title: 486 Sandy River Motherboard

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (6.0.2)		Id: 1/16


U1A
Intel_P24T
VCPU
JP9 – Pin T5 – VOLDET connection
Intel/AMD: Open; Cyrix/IBM: Closed
JP10 – Pin C11 – SMI# connection
Non-SL CPU: Open; SL-enabled CPU: Closed
JP11 – Pin D17 – Reset connection
CPURST: 1-2; RSTDRV: 2-3
JP12 – Pin D11/C13 – CPURST connection
Pin D11: 1-2; Pin C14: 2-3
JP13 – Pin D15/B14 – FERR# connection
486DX/ODPR/5x86: 1-2; 487DX/ODP/P24T: 2-3; 486SX: Open or 2-3?
JP19 – Pin C14 – CPU select
1-2: Pull-up; 2-3: GND
JP21 – Pin D13/D11 – SMIACT# connection
Non-SL CPU: Open; Intel/AMD SL: 1-2; Cyrix/IBM: 2-3
JP23 – Pin B16/C16 – IGNNE#/NMI connection
486SX: 2-3; All non 486SX: 1-2,3-4
JP30 – Pin S18/R16
JP32 – Pin S18/B13 – HITM connection
JP46 – Pin B13 – IBM_SMI# connection
Non-IBM: 1-2, Cyrix/IBM: 2-3
U1B
Intel_P24T
Pin C15 is connected to JP22 (not populated)
JP22 is connected to 10k pull-up (to VCC)
Pins A3, C3 are connected to GND
Pins A4, D1 are connected to VCC/5V
JP9
Intel/Cyrix
R68
10k
JP10
SMI Enable
JP11
Reset Select
JP12
CPU Select 1
JP13
FERR Select
R47
1k
JP19
CPU Select 2
JP21
CPU Select 3
JP30
CPU Select 3
JP32
CPU Select 4
R42
10k
JP4
5V / 3.3V CPU Voltage
PWR_FLAG
C1
100nF
C2
100nF
Check caps value/number
add CPU caps
R35
100
JP23
NMI/IGNNE#
Sheet: /Processor/
File: Processor.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 2/16

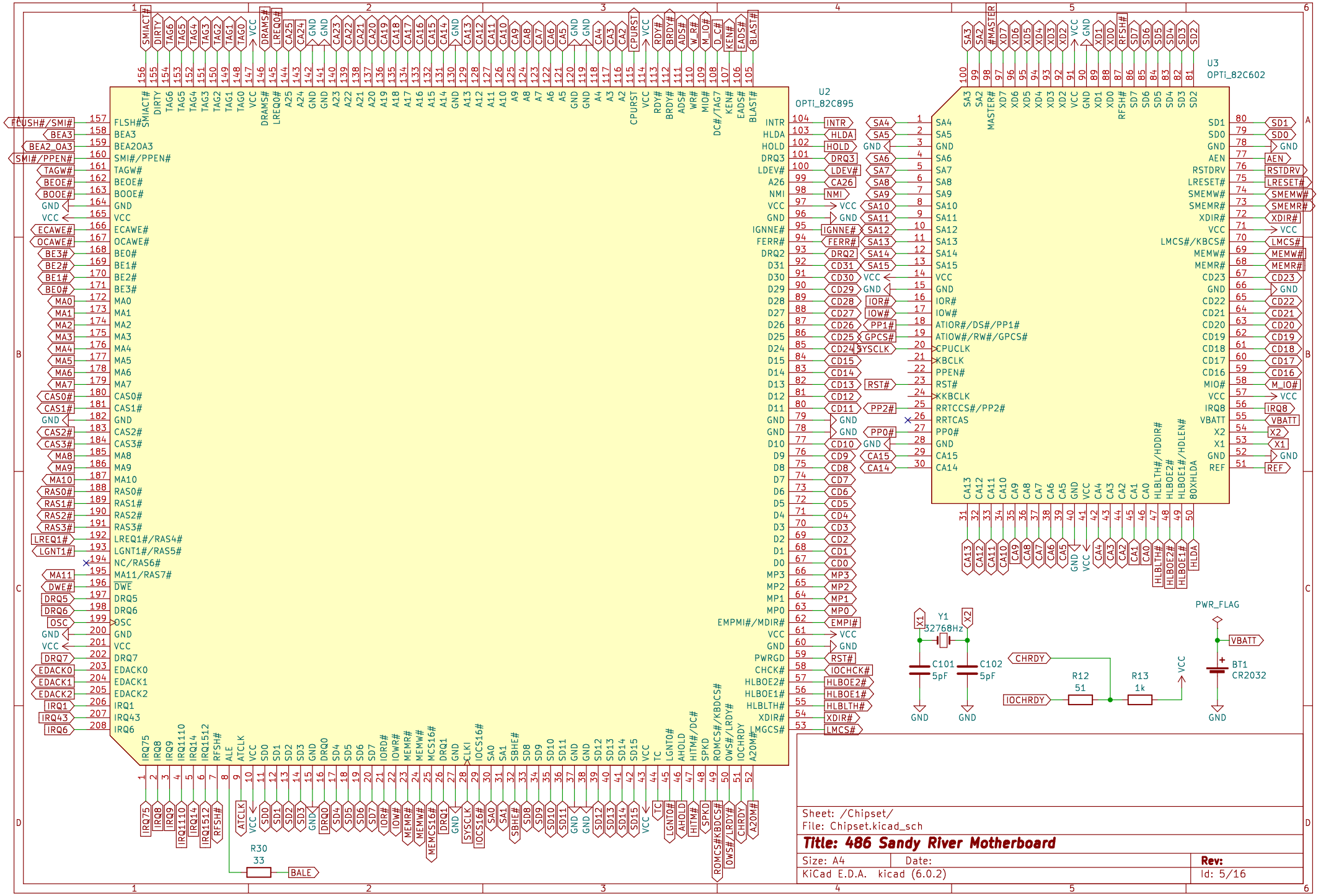

BUS1
BUSAT_HOST
BUS2
BUSAT_HOST
BUS3
BUSAT_HOST
BUS4
BUSAT_HOST
GND RESET +5V IRQ9 -5V DRQ2 -12V OWS/SRDY +12V GND SMEMW SMEMR IOW IOR DACK3 DRQ3 DACK1 DRQ1 REFRESH BCLK IRQ7 IRQ6 IRQ5 IRQ4 IRQ3 DACK2 TC BALE +5V OSC GND
IOCHCK SD7 SD6 SD5 SD4 SD3 SD2 SD1 SD0 IOCHRDY AEN SA19 SA18 SA17 SA16 SA15 SA14 SA13 SA12 SA11 SA10 SA9 SA8 SA7 SA6 SA5 SA4 SA3 SA2 SA1 SA0
MEMCS16 IOCS16 IRQ10 IRQ11 IRQ12 IRQ15 IRQ14 DACK0 DRQ0 DACK5 DRQ5 DACK6 DRQ6 DACK7 DRQ7 +5V MASTER GND
SBHE LA23 LA22 LA21 LA20 LA19 LA18 LA17 MEMR MEMW SD8 SD9 SD10 SD11 SD12 SD13 SD14 SD15
Sheet: /ISA/
File: ISA.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 3/16

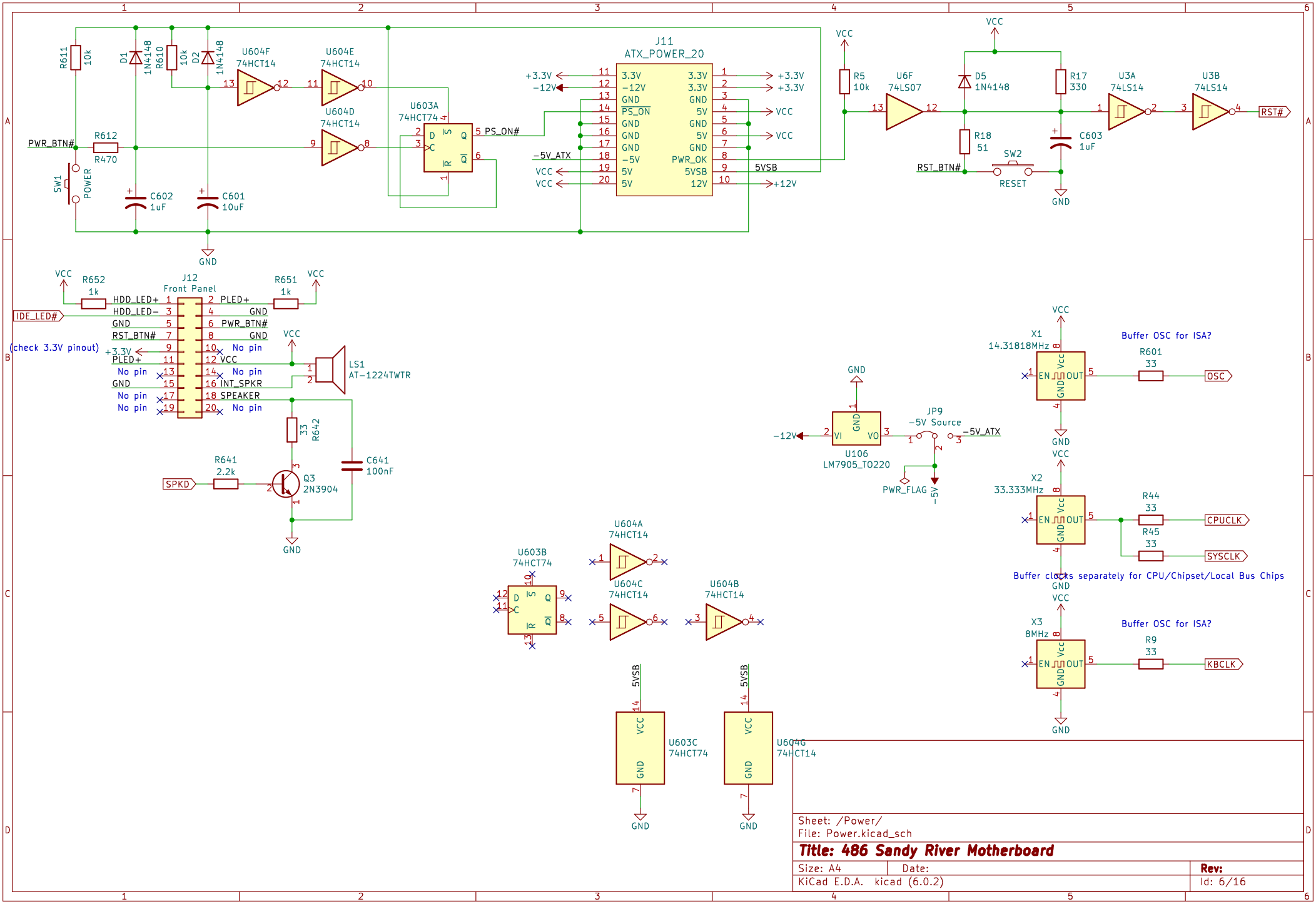


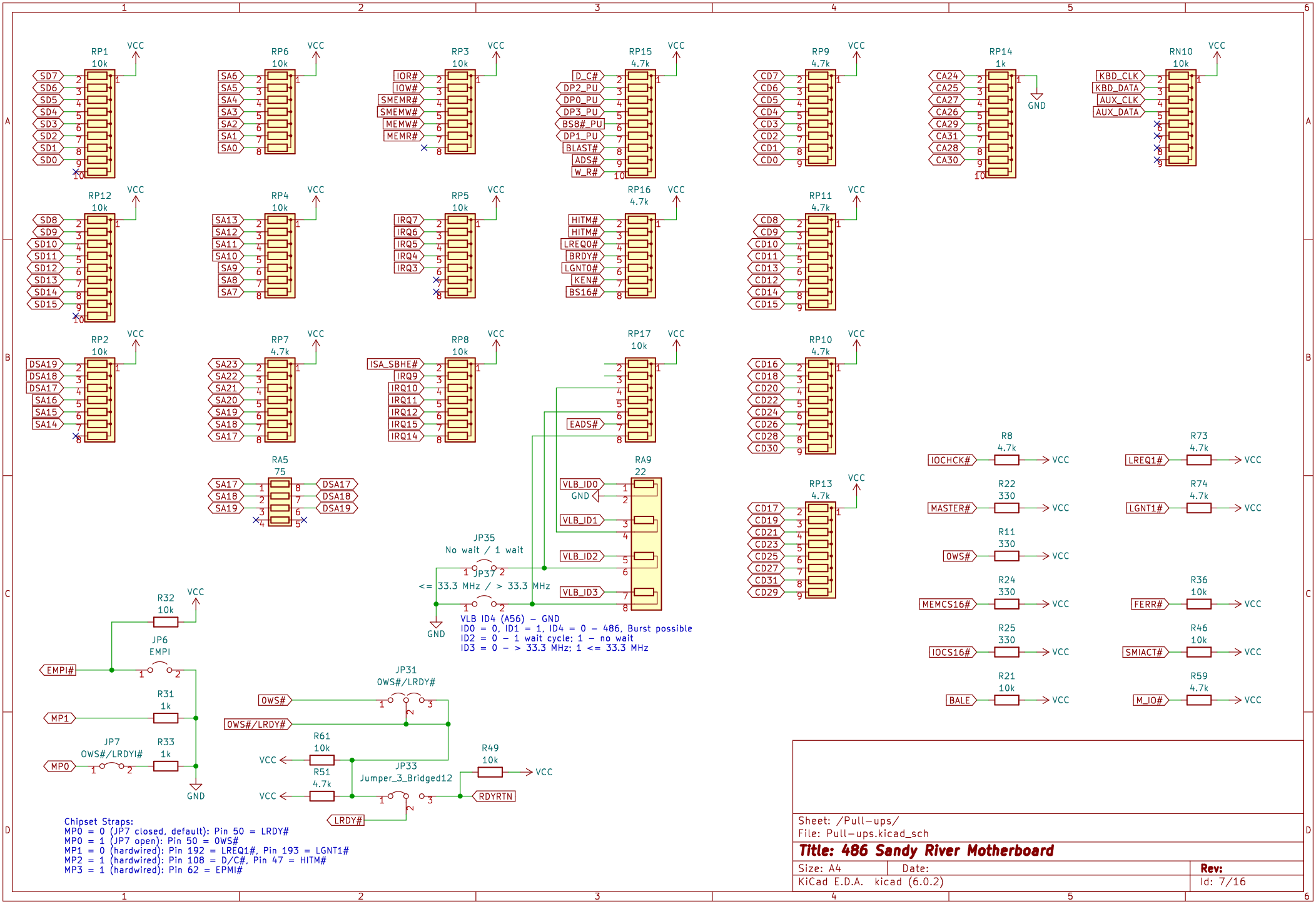
Sheet: /Memory/
File: Memory.kicad_sch

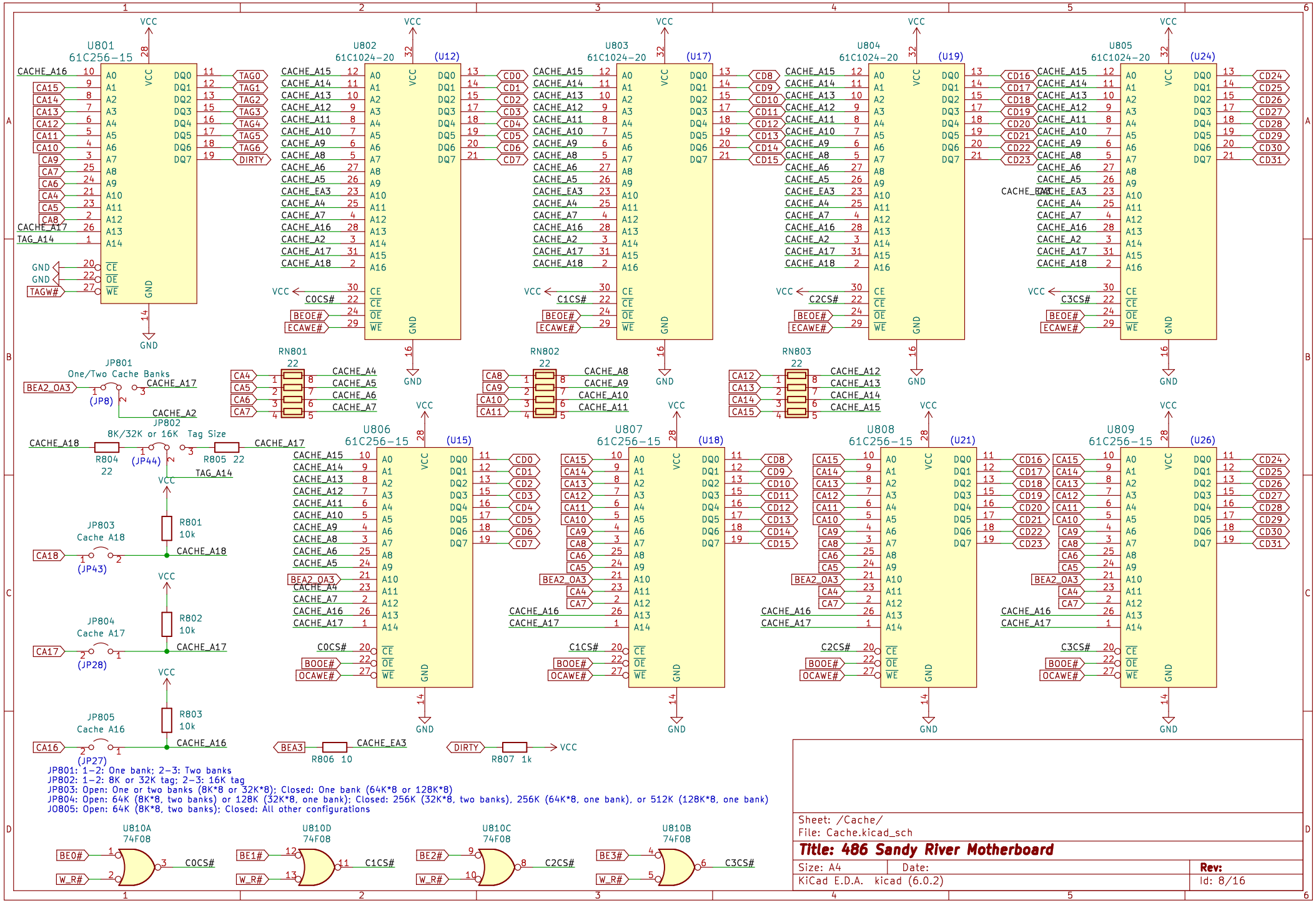
Title: 486 Sandy River Motherboard

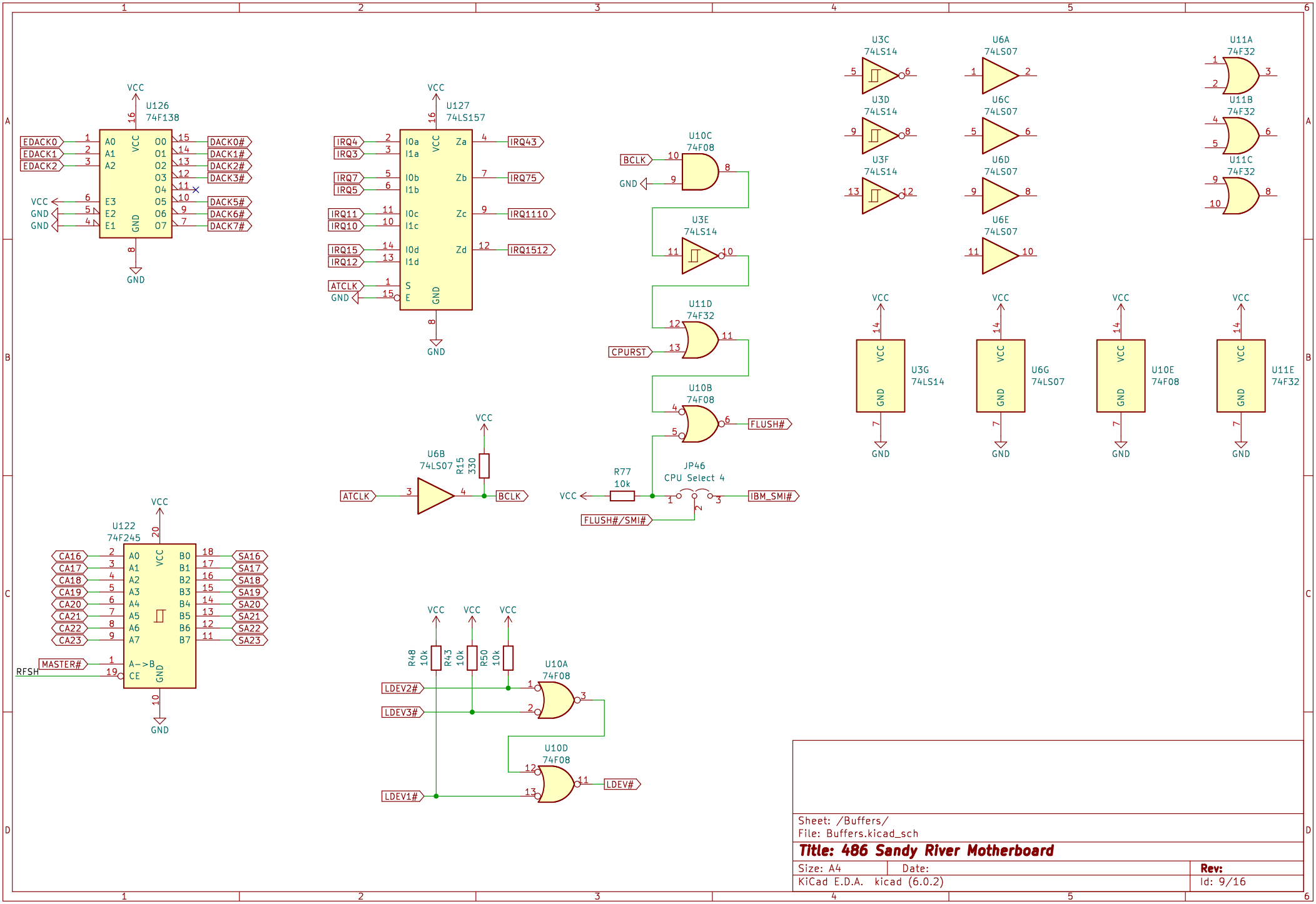
Size: A4	Date:	Rev:
KiCad E.D.A. kicad (6.0.2)		Id: 4/16


U2
OPTi_82C895
U3
OPTi_82C602
Y1
32768Hz
C101
5pF
C102
5pF
R30
33
BALE
R12
51
R13
1k
IOCHRDY
CHRDY
VCC
PWR_FLAG
BT1
CR2032
VBATT
GND
Sheet: /Chipset/
File: Chipset.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 5/16

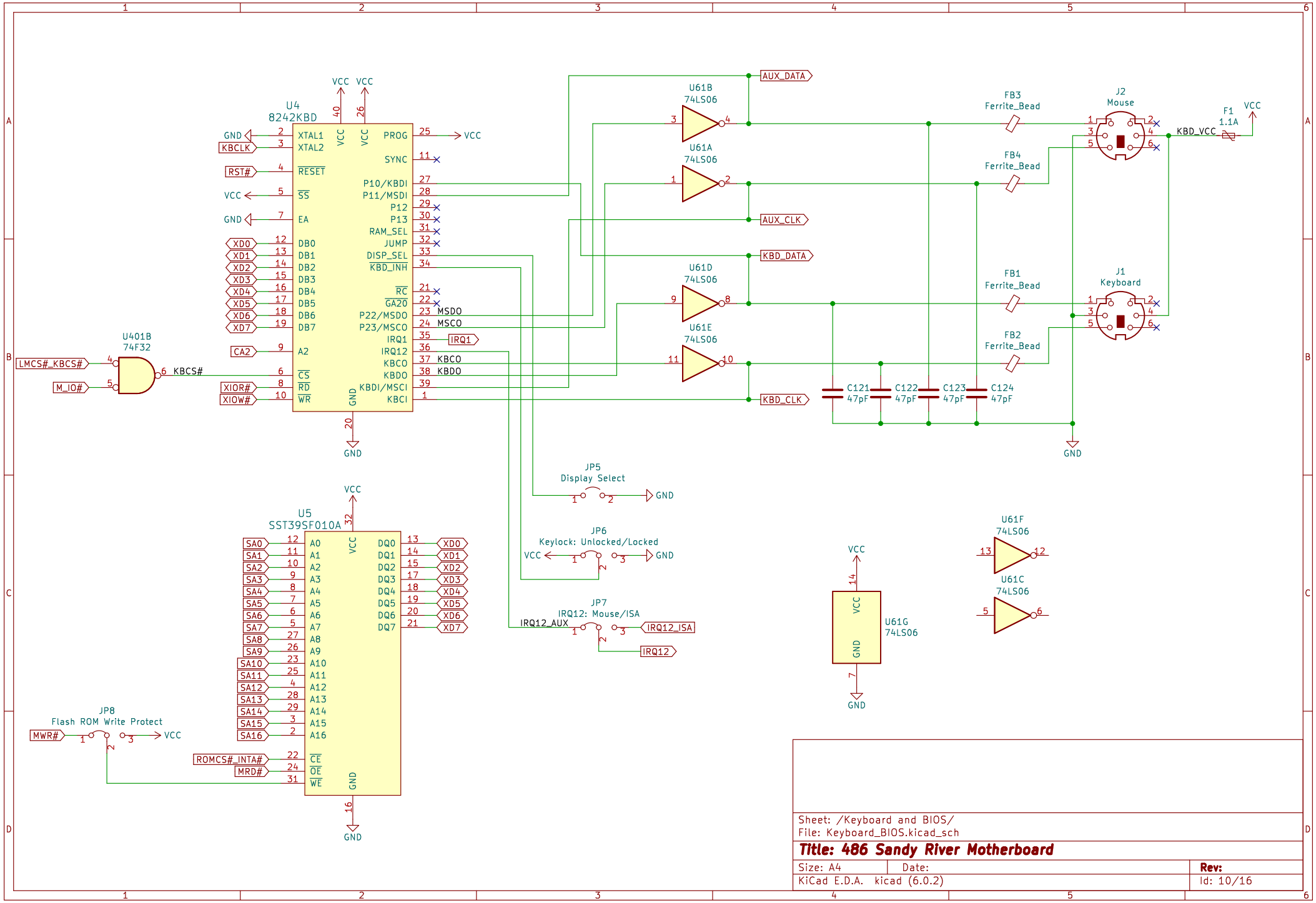

R611 10k
D1 1N4148
R610 10k
D2 1N4148
U604F 74HCT14
U604E 74HCT14
U604D 74HCT14
U603A 74HCT74
PS_ON#
PWR_BTN#
R612
R470
SW1 POWER
C602 1uF
C601 10uF
GND
J11 ATX_POWER_20
+3.3V
−12V
GND
PS_ON
5V
−5V
PWR_OK
5VSB
−5V_ATX
R5 10k
U6F 74LS07
D5 1N4148
R17 330
R18 51
SW2 RESET
RST_BTN#
C603 1uF
U3A 74LS14
U3B 74LS14
RST#
R652 1k
R651 1k
J12 Front Panel
HDD_LED+
HDD_LED−
RST_BTN#
PLED+
PWR_BTN#
INT_SPKR
SPEAKER
No pin
IDE_LED#
(check 3.3V pinout)
LS1 AT−1224TWTR
R642 33
R641 2.2k
Q3 2N3904
SPKD
C641 100nF
JP9 −5V Source
U106 LM7905_TO220
PWR_FLAG
X1 14.31818MHz
X2 33.333MHz
X3 8MHz
Buffer OSC for ISA?
R601 33
OSC
R44 33
R45 33
CPUCLK
SYSCLK
Buffer clocks separately for CPU/Chipset/Local Bus Chips
R9 33
KBCLK
U603B 74HCT74
U604A 74HCT14
U604C 74HCT14
U604B 74HCT14
U603C 74HCT74
U604G 74HCT14
Sheet: /Power/
File: Power.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 6/16

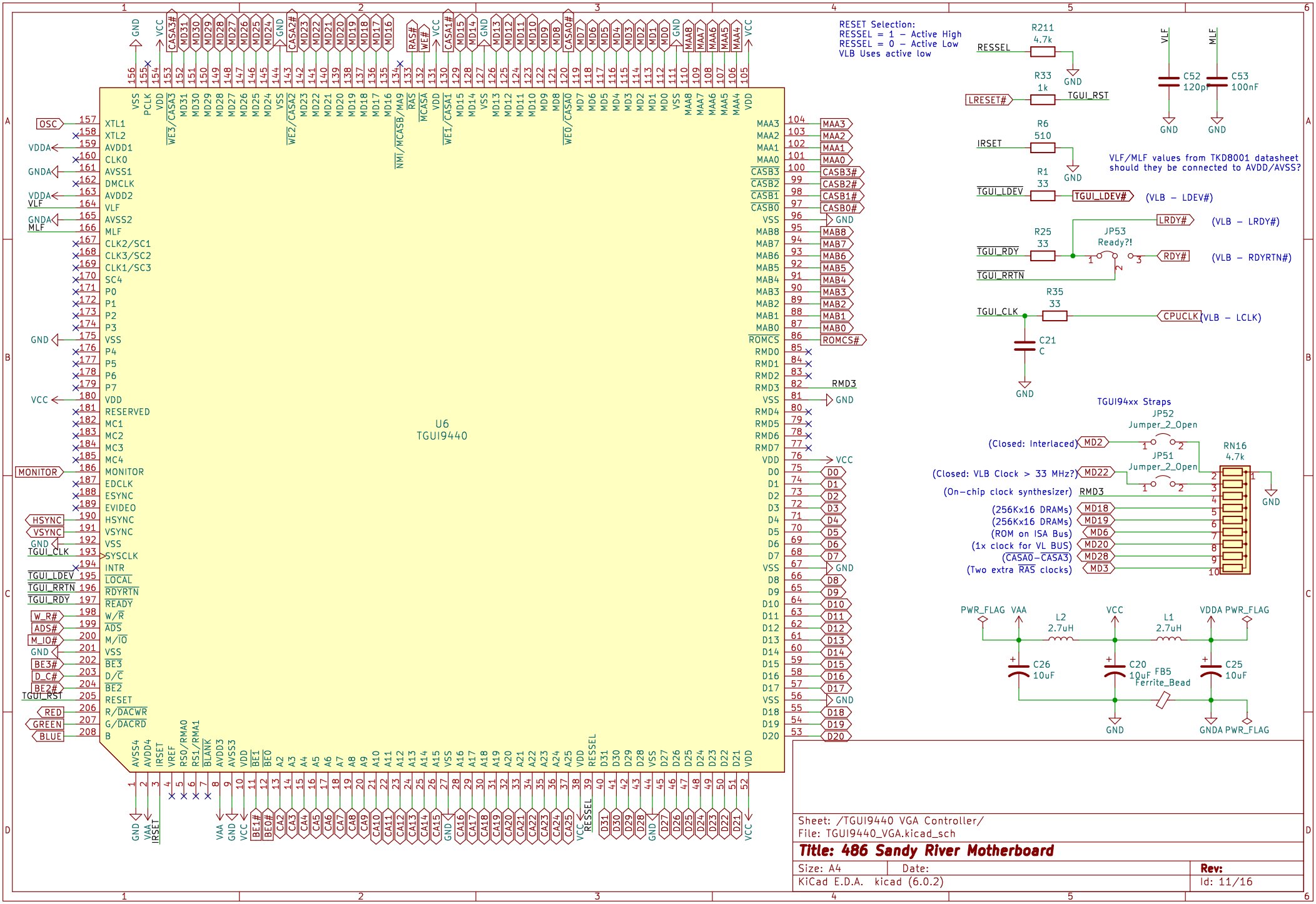

RP1
10k
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
VCC
RP6
10k
SA6
SA5
SA4
SA3
SA2
SA1
SA0
RP3
10k
IOR#
IOW#
SMEMR#
SMEMW#
MEMW#
MEMR#
RP15
4.7k
D_C#
DP2_PU
DP0_PU
DP3_PU
BS8#_PU
DP1_PU
BLAST#
ADS#
W_R#
RP9
4.7k
CD7
CD6
CD5
CD4
CD3
CD2
CD1
CD0
RP14
1k
CA24
CA25
CA27
CA26
CA29
CA31
CA28
CA30
GND
RN10
10k
KBD_CLK
KBD_DATA
AUX_CLK
AUX_DATA
RP12
10k
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
RP4
10k
SA13
SA12
SA11
SA10
SA9
SA8
SA7
RP5
10k
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
RP16
4.7k
HITM#
HITM#
LREQ0#
BRDY#
LGNT0#
KEN#
BS16#
RP11
4.7k
CD8
CD9
CD10
CD11
CD13
CD12
CD14
CD15
RP2
10k
DSA19
DSA18
DSA17
SA16
SA15
SA14
RP7
4.7k
SA23
SA22
SA21
SA20
SA19
SA18
SA17
RP8
10k
ISA_SBHE#
IRQ9
IRQ10
IRQ11
IRQ12
IRQ15
IRQ14
RP17
10k
EADS#
RP10
4.7k
CD16
CD18
CD20
CD22
CD24
CD26
CD28
CD30
RA5
75
SA17
SA18
SA19
DSA17
DSA18
DSA19
RA9
22
VLB_ID0
GND
VLB_ID1
VLB_ID2
VLB_ID3
RP13
4.7k
CD17
CD19
CD21
CD23
CD25
CD27
CD31
CD29
JP35
No wait / 1 wait
JP37
<= 33.3 MHz / > 33.3 MHz
GND
VLB ID4 (A56) – GND
ID0 = 0, ID1 = 1, ID4 = 0 – 486, Burst possible
ID2 = 0 – 1 wait cycle; 1 – no wait
ID3 = 0 – > 33.3 MHz; 1 <= 33.3 MHz
R8
4.7k
IOCHCK#
R22
330
MASTER#
R11
330
0WS#
R24
330
MEMCS16#
R25
330
IOCS16#
R21
10k
BALE
R73
4.7k
LREQ1#
R74
4.7k
LGNT1#
R36
10k
FERR#
R46
10k
SMIACT#
R59
4.7k
M_IO#
R32
10k
JP6
EMPI
EMPI#
R31
1k
MP1
JP7
OWS#/LRDYI#
R33
1k
MP0
GND
JP31
OWS#/LRDY#
OWS#
OWS#/LRDY#
R61
10k
R51
4.7k
JP33
Jumper_3_Bridged12
R49
10k
RDYRTN
LRDY#
Chipset Straps:
MP0 = 0 (JP7 closed, default): Pin 50 = LRDY#
MP0 = 1 (JP7 open): Pin 50 = 0WS#
MP1 = 0 (hardwired): Pin 192 = LREQ1#, Pin 193 = LGNT1#
MP2 = 1 (hardwired): Pin 108 = D/C#, Pin 47 = HITM#
MP3 = 1 (hardwired): Pin 62 = EPMI#
Sheet: /Pull-ups/
File: Pull-ups.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 7/16

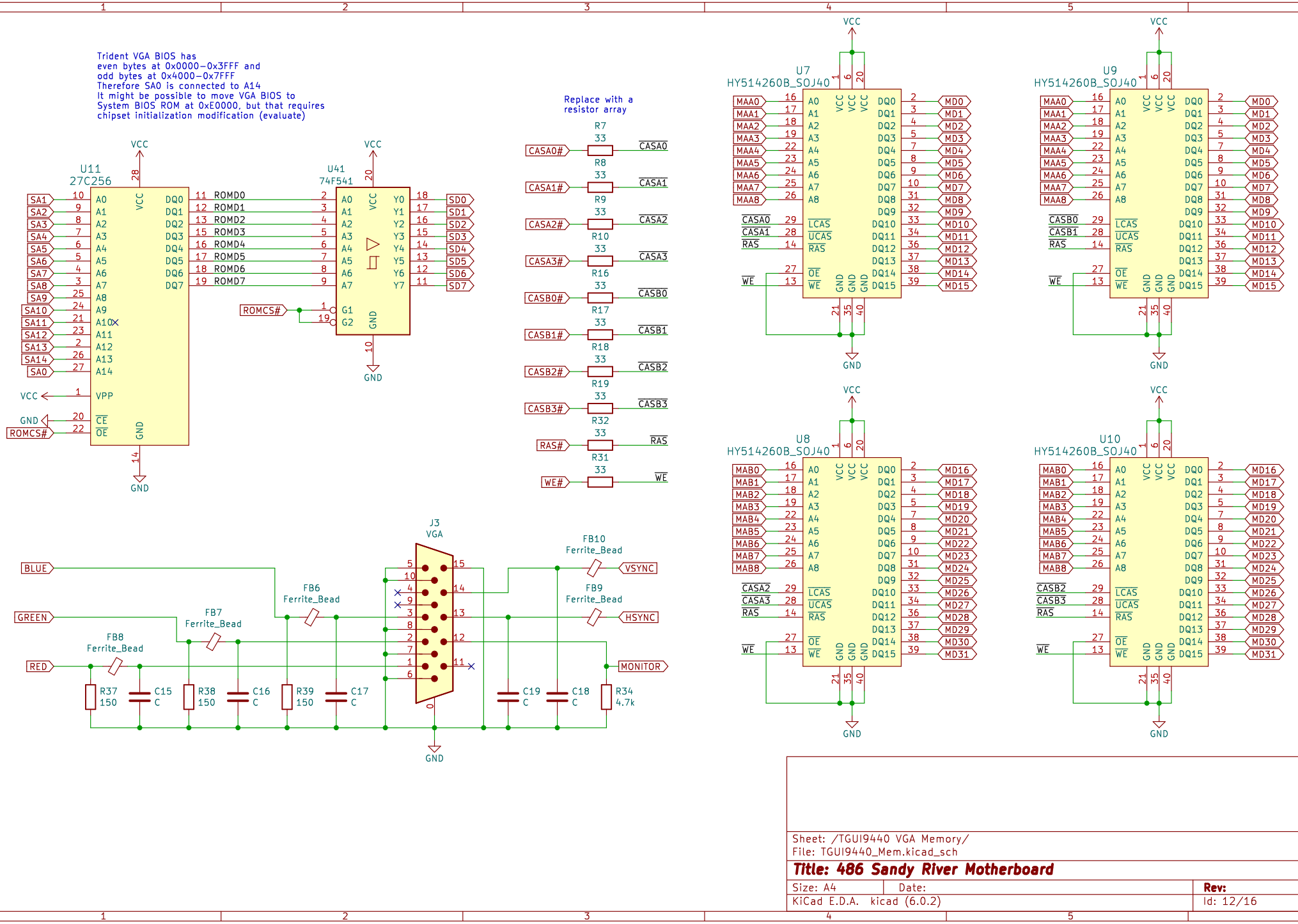

U801
61C256-15
U802
61C1024-20
(U12)
U803
61C1024-20
(U17)
U804
61C1024-20
(U19)
U805
61C1024-20
(U24)
U806
61C256-15
(U15)
U807
61C256-15
(U18)
U808
61C256-15
(U21)
U809
61C256-15
(U26)
JP801
One/Two Cache Banks
(JP8)
JP802
8K/32K or 16K Tag Size
(JP44)
JP803
Cache A18
(JP43)
JP804
Cache A17
(JP28)
JP805
Cache A16
(JP27)
RN801
RN802
RN803
R804 22
R805 22
R801 10k
R802 10k
R803 10k
R806 10
R807 1k
U810A
74F08
U810D
74F08
U810C
74F08
U810B
74F08
JP801: 1-2: One bank; 2-3: Two banks
JP802: 1-2: 8K or 32K tag; 2-3: 16K tag
JP803: Open: One or two banks (8K*8 or 32K*8); Closed: One bank (64K*8 or 128K*8)
JP804: Open: 64K (8K*8, two banks) or 128K (32K*8, one bank); Closed: 256K (32K*8, two banks), 256K (64K*8, one bank), or 512K (128K*8, one bank)
JO805: Open: 64K (8K*8, two banks); Closed: All other configurations
Sheet: /Cache/
File: Cache.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 8/16



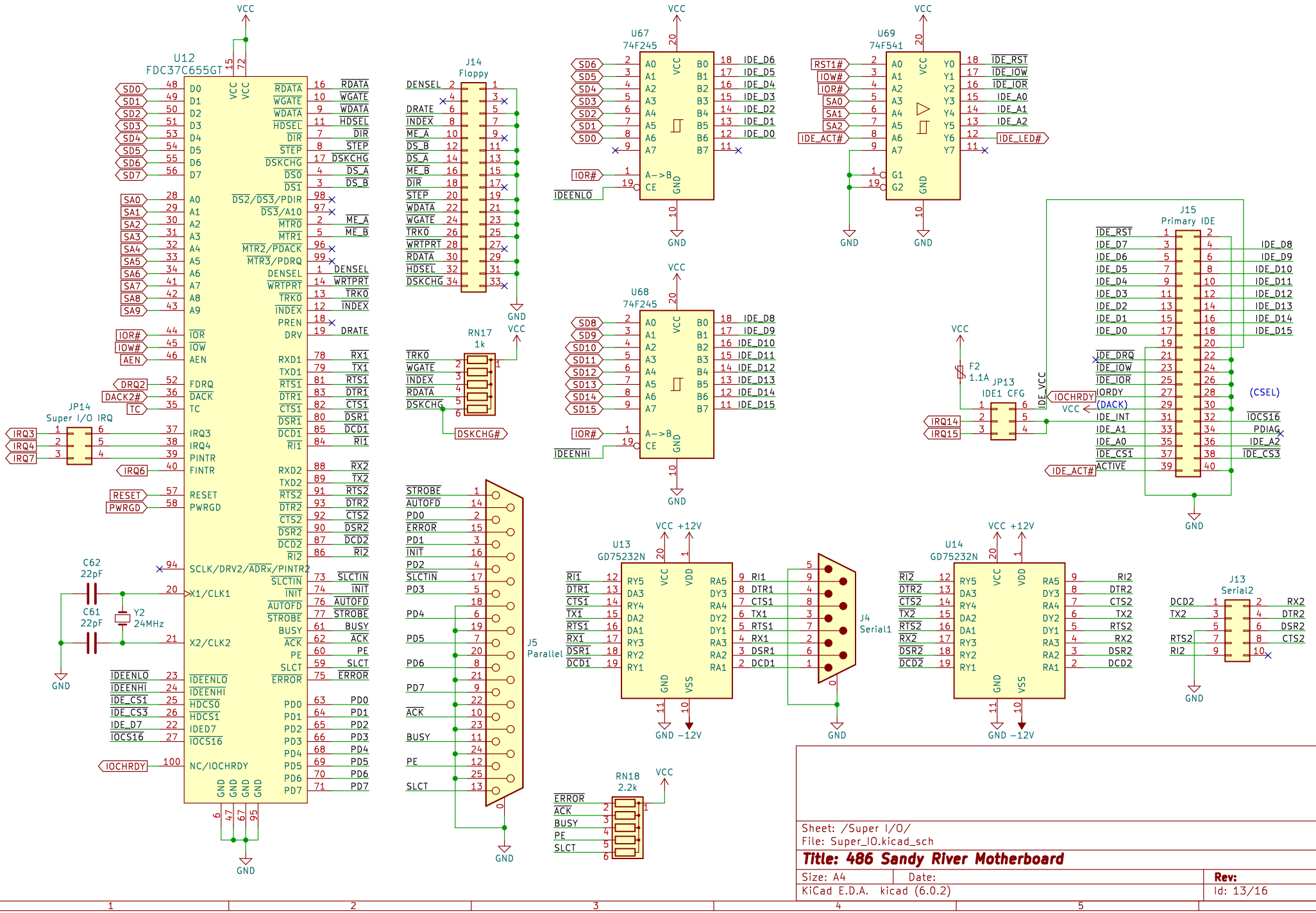
Sheet: /Buffers/		
File: Buffers.kicad_sch		
Title: 486 Sandy River Motherboard		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.2)		Id: 9/16

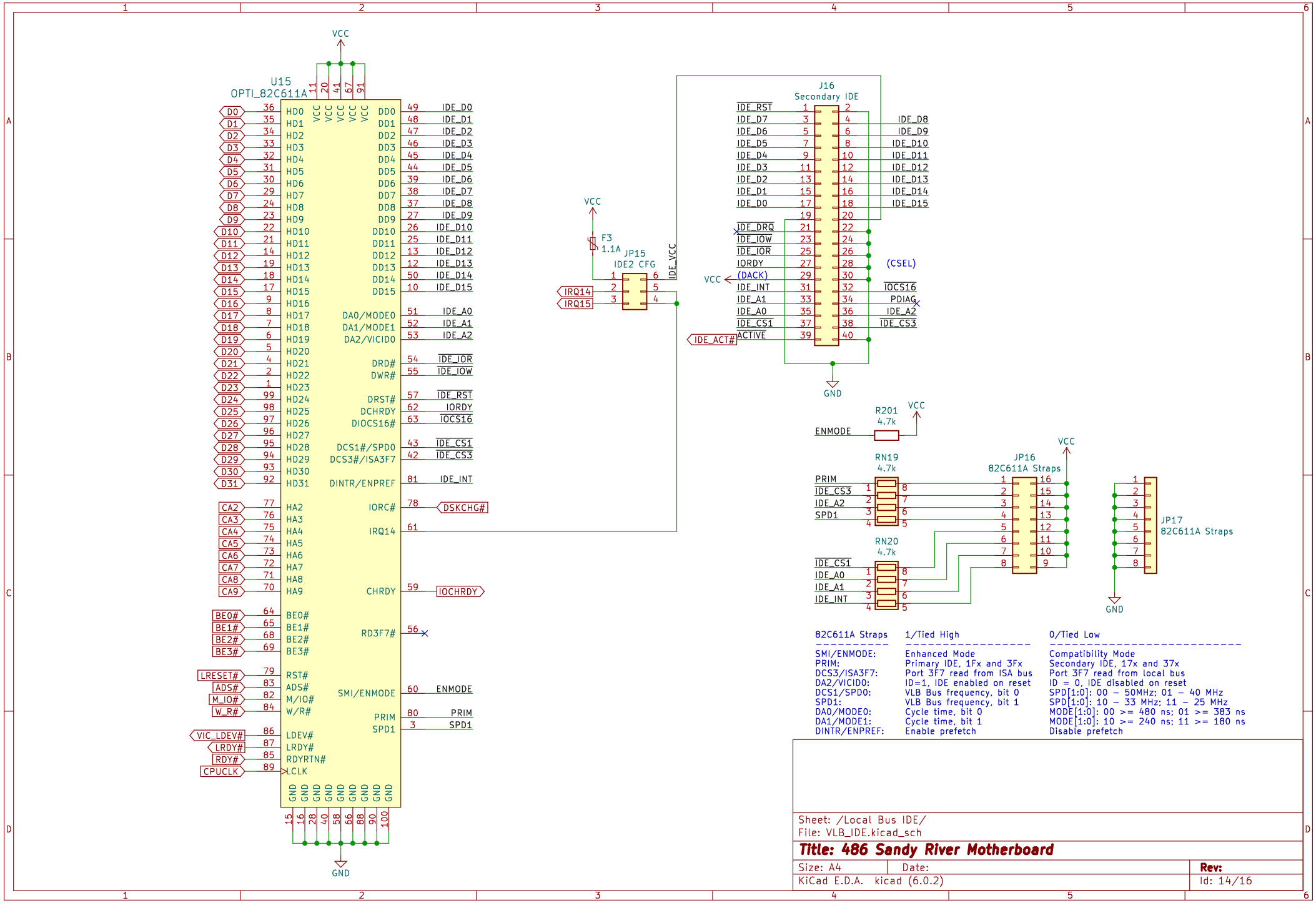

U4
8242KBD
U61B
74LS06
U61A
74LS06
U61D
74LS06
U61E
74LS06
U401B
74F32
U5
SST39SF010A
JP5
Display Select
JP6
Keylock: Unlocked/Locked
JP7
IRQ12: Mouse/ISA
JP8
Flash ROM Write Protect
J1
Keyboard
J2
Mouse
FB1
Ferrite_Bead
FB2
Ferrite_Bead
FB3
Ferrite_Bead
FB4
Ferrite_Bead
F1
1.1A
C121
47pF
C122
47pF
C123
47pF
C124
47pF
U61F
74LS06
U61C
74LS06
U61G
74LS06
AUX_DATA
AUX_CLK
KBD_DATA
KBD_CLK
KBD_VCC
IRQ1
IRQ12_AUX
IRQ12_ISA
IRQ12
KBCLK
RST#
LMCS#_KBCS#
M_IO#
KBCS#
XIOR#
XIOW#
MWR#
ROMCS#_INTA#
MRD#
MSDO
MSCO
KBCO
KBDO
VCC
GND
Sheet: /Keyboard and BIOS/
File: Keyboard_BIOS.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 10/16


U6
TGUI9440
RESET Selection:
RESSEL = 1 – Active High
RESSEL = 0 – Active Low
VLB Uses active low
R211 4.7k
R33 1k
R6 510
R1 33
R25 33
R35 33
C52 120pF
C53 100nF
C21 C
JP53 Ready?!
VLF/MLF values from TKD8001 datasheet should they be connected to AVDD/AVSS?
TGUI94xx Straps
JP52 Jumper_2_Open
JP51 Jumper_2_Open
RN16 4.7k
(Closed: Interlaced)
(Closed: VLB Clock > 33 MHz?)
(On–chip clock synthesizer)
(256Kx16 DRAMs)
(256Kx16 DRAMs)
(ROM on ISA Bus)
(1x clock for VL BUS)
(CASA0–CASA3)
(Two extra RAS clocks)
L2 2.7uH
L1 2.7uH
C26 10uF
C20 10uF
FB5 Ferrite_Bead
C25 10uF
Sheet: /TGUI9440 VGA Controller/
File: TGUI9440_VGA.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 11/16



Sheet: /TGUI9440 VGA Memory/	
File: TGUI9440_Mem.kicad_sch	
Title: 486 Sandy River Motherboard	
Size: A4	Date:
KiCad E.D.A. kicad (6.0.2)	Rev: Id: 12/16


U12
FDC37C655GT
U67
74F245
U68
74F245
U69
74F541
J14
Floppy
RN17
1k
RN18
2.2k
JP14
Super I/O IRQ
JP13
IDE1 CFG
F2
1.1A
J15
Primary IDE
C62
22pF
C61
22pF
Y2
24MHz
J5
Parallel
U13
GD75232N
U14
GD75232N
J4
Serial1
J13
Serial2
VCC
GND
VCC +12V
GND −12V
(CSEL)
Sheet: /Super I/O/
File: Super_IO.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 13/16

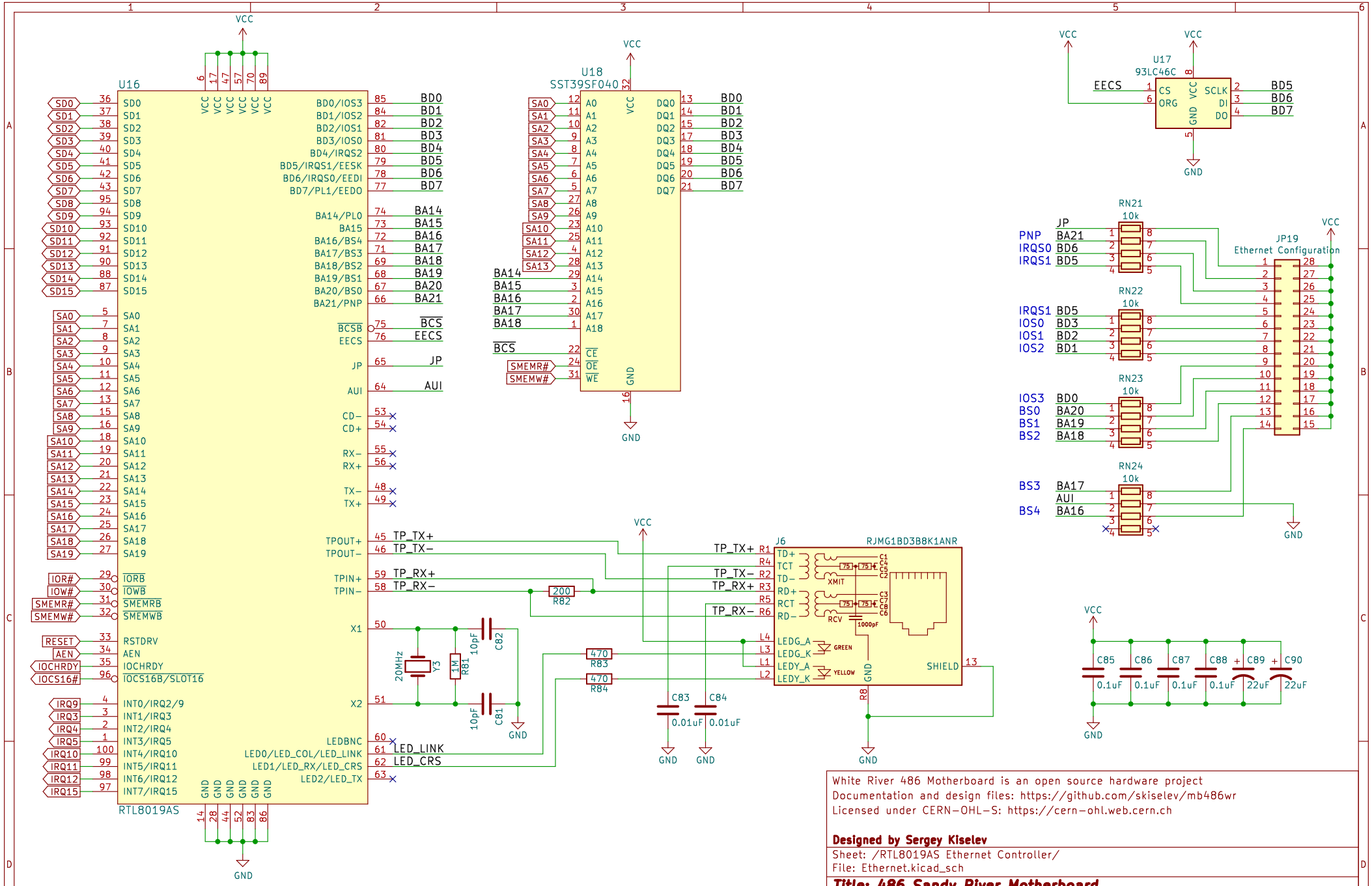


82C611A Straps	1/Tied High	0/Tied Low
SMI/ENMODE:	Enhanced Mode	Compatibility Mode
PRIM:	Primary IDE, 1Fx and 3Fx	Secondary IDE, 17x and 37x
DCS3/ISA3F7:	Port 3F7 read from ISA bus	Port 3F7 read from local bus
DA2/VICID0:	ID=1, IDE enabled on reset	ID = 0, IDE disabled on reset
DCS1/SPD0:	VLB Bus frequency, bit 0	SPD[1:0]: 00 – 50MHz; 01 – 40 MHz
SPD1:	VLB Bus frequency, bit 1	SPD[1:0]: 10 – 33 MHz; 11 – 25 MHz
DA0/MODE0:	Cycle time, bit 0	MODE[1:0]: 00 >= 480 ns; 01 >= 383 ns
DA1/MODE1:	Cycle time, bit 1	MODE[1:0]: 10 >= 240 ns; 11 >= 180 ns
DINTR/ENPREF:	Enable prefetch	Disable prefetch

Sheet: /Local Bus IDE/
File: VLB_IDE.kicad_sch

Title: 486 Sandy River Motherboard

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (6.0.2)		Id: 14/16



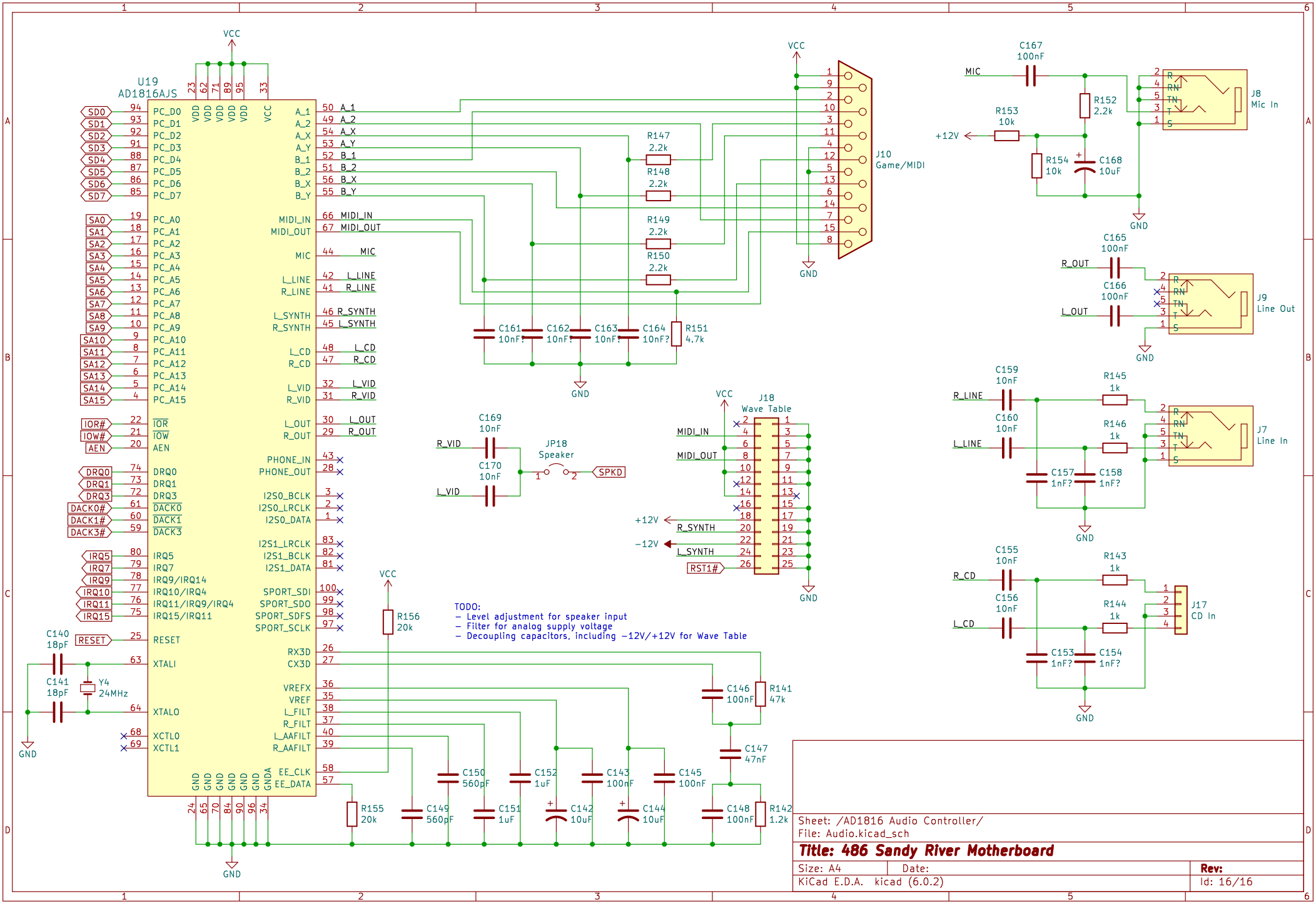
White River 486 Motherboard is an open source hardware project
Documentation and design files: https://github.com/skiselev/mb486wr
Licensed under CERN−OHL−S: https://cern−ohl.web.cern.ch

Designed by Sergey Kiselev

Sheet: /RTL8019AS Ethernet Controller/
File: Ethernet.kicad_sch

Title: 486 Sandy River Motherboard

Size: A4	Date: 2022−02−09	**Rev: 1.0**
KiCad E.D.A. kicad (6.0.2)		Id: 15/16


U19
AD1816AJS
VCC
GND
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
IOR#
IOW#
AEN
DRQ0
DRQ1
DRQ3
DACK0#
DACK1#
DACK3#
IRQ5
IRQ7
IRQ9
IRQ10
IRQ11
IRQ15
RESET
XTALI
XTALO
XCTL0
XCTL1
A_1
A_2
A_X
A_Y
B_1
B_2
B_X
B_Y
MIDI_IN
MIDI_OUT
MIC
L_LINE
R_LINE
L_SYNTH
R_SYNTH
L_CD
R_CD
L_VID
R_VID
L_OUT
R_OUT
PHONE_IN
PHONE_OUT
I2S0_BCLK
I2S0_LRCLK
I2S0_DATA
I2S1_LRCLK
I2S1_BCLK
I2S1_DATA
SPORT_SDI
SPORT_SDO
SPORT_SDFS
SPORT_SCLK
RX3D
CX3D
VREFX
VREF
L_FILT
R_FILT
L_AAFILT
R_AAFILT
EE_CLK
EE_DATA
J10
Game/MIDI
R147 2.2k
R148 2.2k
R149 2.2k
R150 2.2k
C161 10nF?
C162 10nF?
C163 10nF?
C164 10nF?
R151 4.7k
C167 100nF
MIC
R152 2.2k
R153 10k
+12V
R154 10k
C168 10uF
J8
Mic In
C165 100nF
R_OUT
C166 100nF
L_OUT
J9
Line Out
C159 10nF
R_LINE
R145 1k
C160 10nF
L_LINE
R146 1k
C157 1nF?
C158 1nF?
J7
Line In
C155 10nF
R_CD
R143 1k
C156 10nF
L_CD
R144 1k
C153 1nF?
C154 1nF?
J17
CD In
C169 10nF
R_VID
C170 10nF
L_VID
JP18
Speaker
SPKD
J18
Wave Table
MIDI_IN
MIDI_OUT
+12V
-12V
R_SYNTH
L_SYNTH
RST1#
R156 20k
R155 20k
C149 560pF
C150 560pF
C151 1uF
C152 1uF
C142 10uF
C143 100nF
C144 10uF
C145 100nF
C146 100nF
R141 47k
C147 47nF
C148 100nF
R142 1.2k
C140 18pF
C141 18pF
Y4
24MHz
TODO:
- Level adjustment for speaker input
- Filter for analog supply voltage
- Decoupling capacitors, including −12V/+12V for Wave Table
Sheet: /AD1816 Audio Controller/
File: Audio.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 16/16