Processor

File: Processor.kicad_sch

Cache

File: Cache.kicad_sch

Local Bus IDE

File: VLB_IDE.kicad_sch

ISA

File: ISA.kicad_sch

Buffers

File: Buffers.kicad_sch

RTL8019AS Ethernet Controller

File: Ethernet.kicad_sch

Memory

File: Memory.kicad_sch

Keyboard and BIOS

File: Keyboard_BIOS.kicad_sch

AD1816 Audio Controller

File: Audio.kicad_sch

Chipset

File: Chipset.kicad_sch

TGUI9440 VGA Controller

File: TGUI9440_VGA.kicad_sch

Decoupling Dapacitors

File: Decoup_caps.kicad_sch

Power

File: Power.kicad_sch

TGUI9440 VGA Memory

File: TGUI9440_Mem.kicad_sch

Pull-ups

File: Pull-ups.kicad_sch

Super I/O

File: Super_IO.kicad_sch

TODO - Schematic:
- Remove Ethernet boot ROM
- Add 3 pin header for CPU fan - switchable between 5V and 12V with a jumper
- DRAM - 2 or 4 sockets (2 double rank, or 2 double rank + 1 single rank)
- Check OWS#, is it ignored?
- Add decoupling/bypass capacitors
- RP17 - check unconnected pins
- U6/7407 - check unused gates
- U4, pin 22, PPEN# - check if it is indeed unconnected (seems to be that way)
- U4, pins 45, 46 (CA1, CA1) - check that they are connected to ISA SA1, SA0
- 3.3/3.45/4V CPU voltage regulator
- Check 22 ohm x 2 resistor arrays in cache circuit - are they used?
- Check chipset power management signals, pins: 62, 156, 160
- Check (82C602) load capacitors for RTC crystal?

TODO - PCB Layout:
- PQFP-208 - modify to be hand-soldering friendly
- Check headers footprints
- Check footprints for the inductors (VGA)

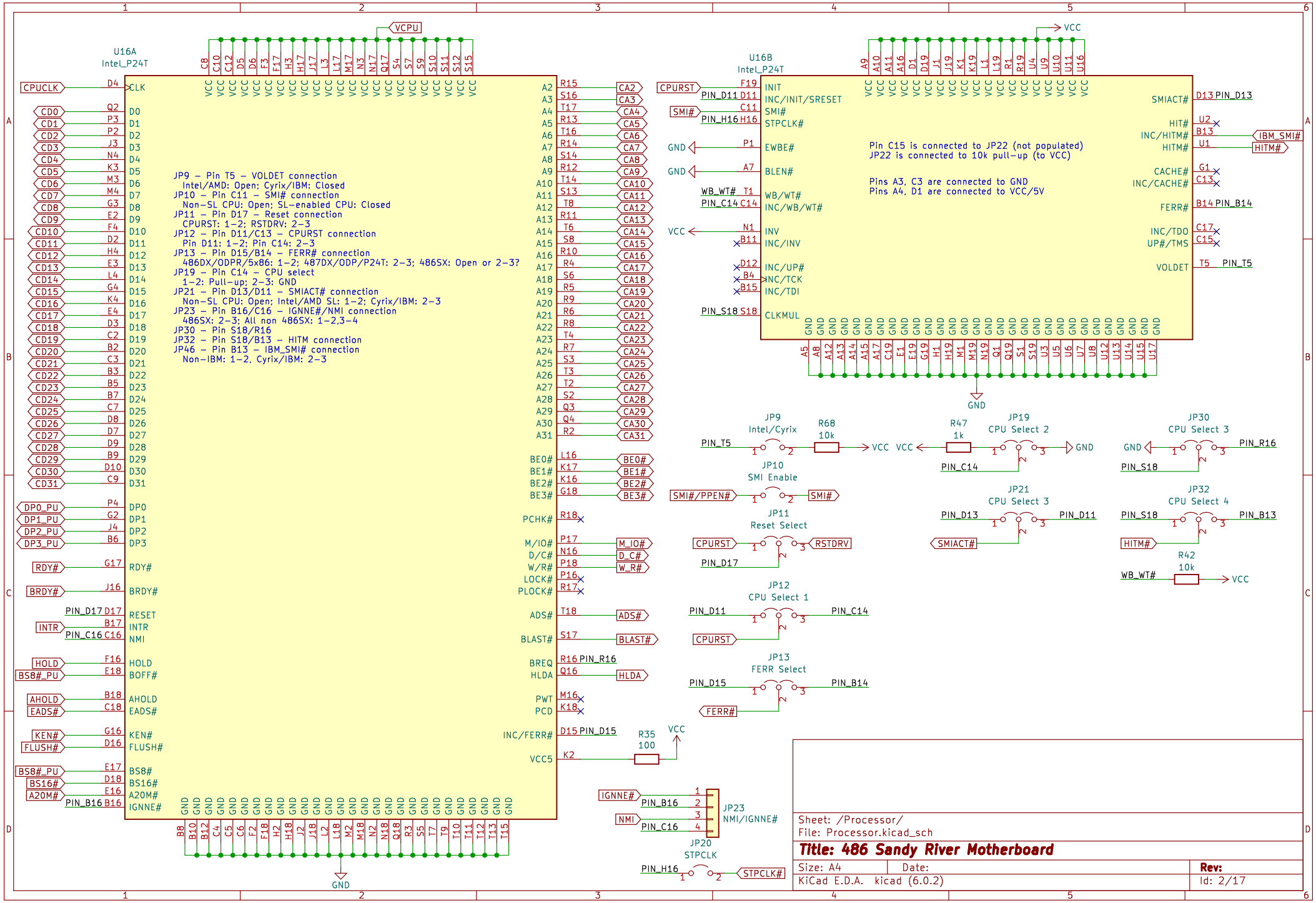
74xx Logic:
74F244 x 2 - DRAM address and control buffers?
74F138 - DACK decoder
74LS157 - Interrupt selector
7407 - Keyboard buffers; Reset circuit; BCLK buffer, anything else?
74F08(1) - Cache byte enable / chip select
74F08(2) - FLUSH# circuit; LDEV# circuit
74LS14 - Reset circuit, FLUSH# circuit
74F245 - CA[23:16] - LA[23:17],SA[19:16]

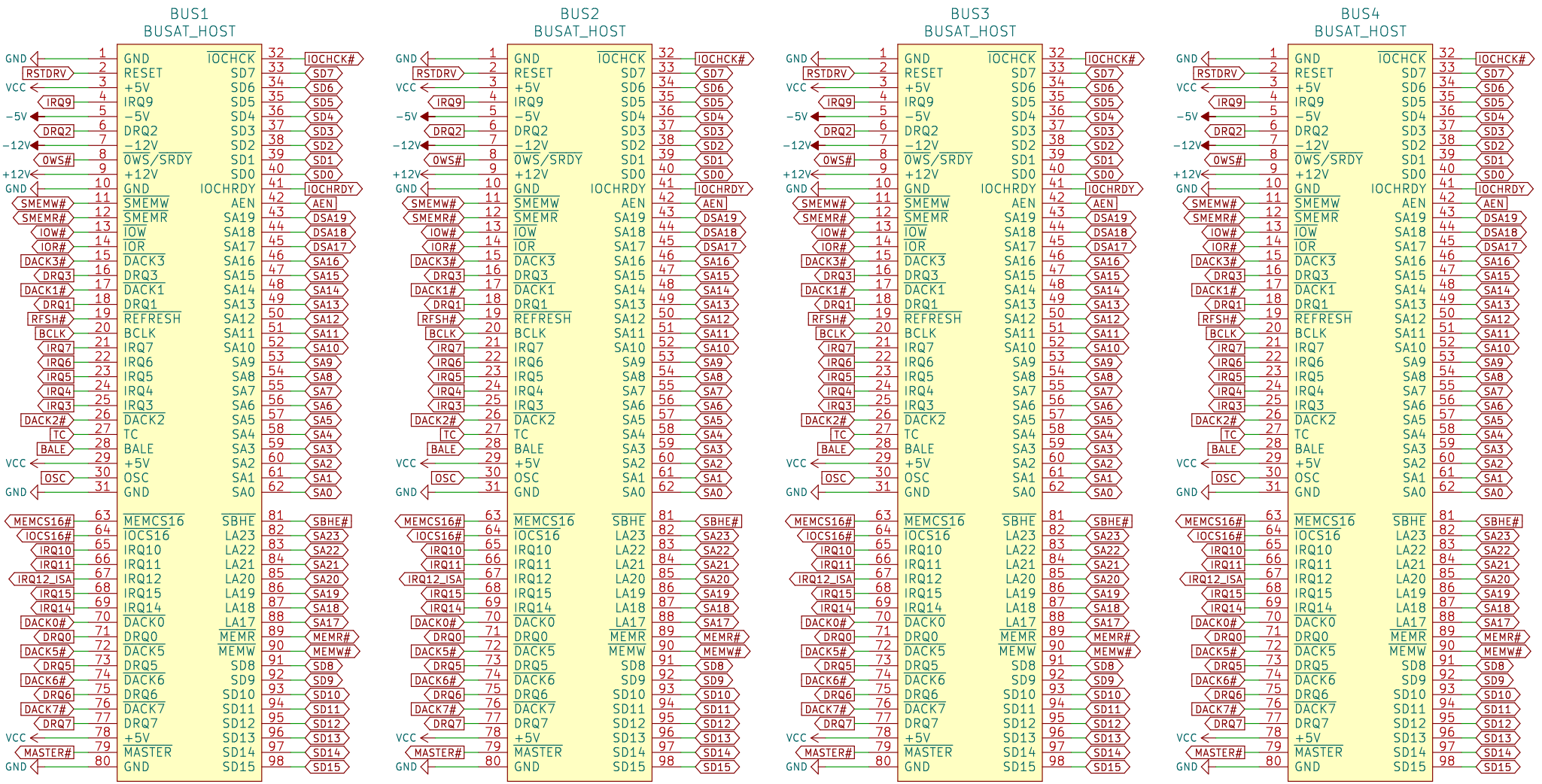
Checked:
- RTC crystal connection - what is the value of load capacitors?
- Cache data signals
- Cache control signals + cache configuration jumpers
- Cache address lines
- DRAM schematic
- ISA pull-ups
- Local bus pull-ups
- CPU configuration jumpers

Sheet: /
File: mb486sr.kicad_sch

Title: 486 Sandy River Motherboard

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (6.0.2)		Id: 1/17

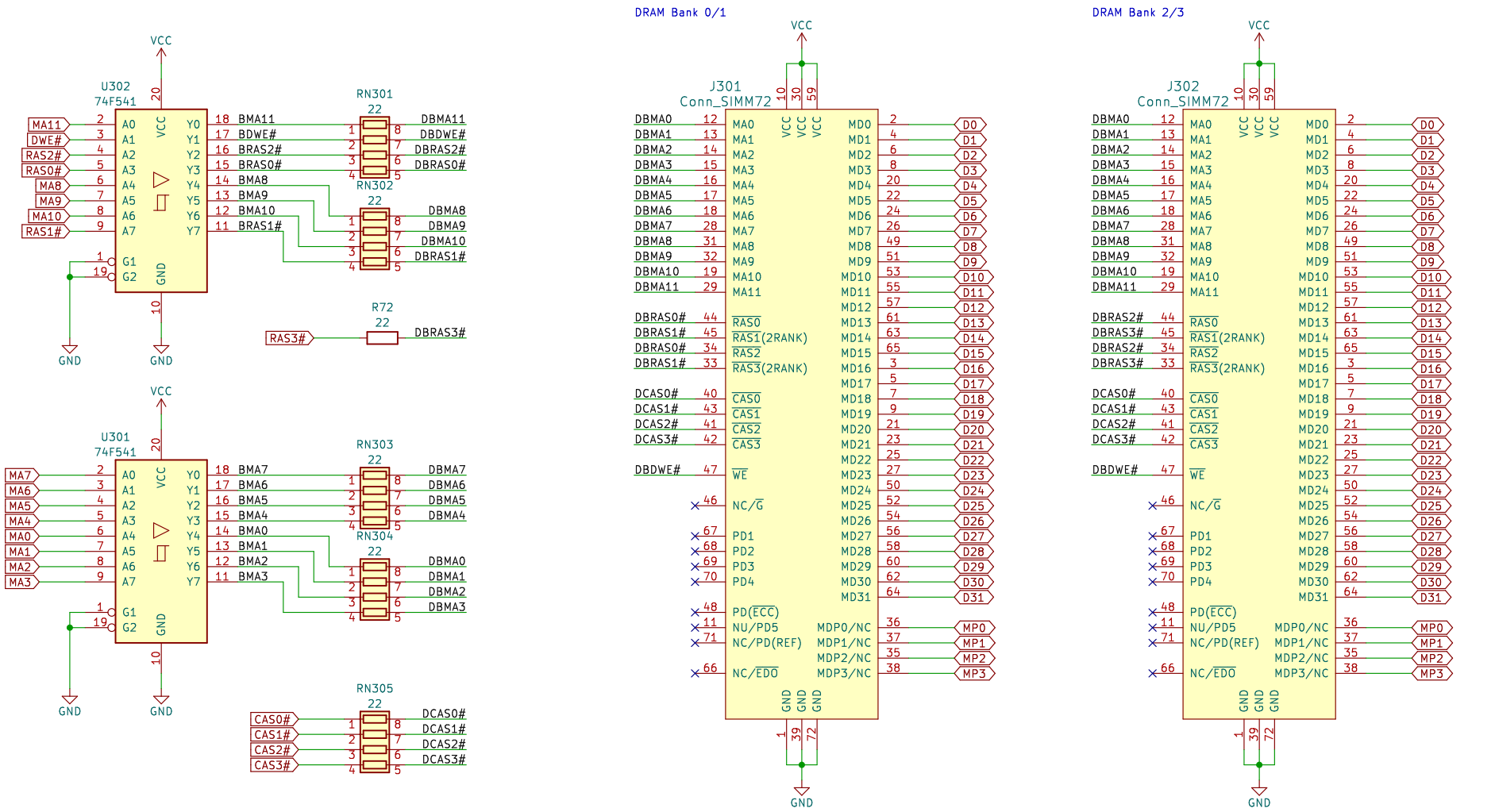

U16A
Intel_P24T
VCPU
CPUCLK
CLK
CD0
CD1
CD2
CD3
CD4
CD5
CD6
CD7
CD8
CD9
CD10
CD11
CD12
CD13
CD14
CD15
CD16
CD17
CD18
CD19
CD20
CD21
CD22
CD23
CD24
CD25
CD26
CD27
CD28
CD29
CD30
CD31
DP0_PU
DP1_PU
DP2_PU
DP3_PU
RDY#
BRDY#
RESET
INTR
NMI
HOLD
BOFF#
AHOLD
EADS#
KEN#
FLUSH#
BS8#
BS16#
A20M#
IGNNE#
JP9 – Pin T5 – VOLDET connection
Intel/AMD: Open; Cyrix/IBM: Closed
JP10 – Pin C11 – SMI# connection
Non-SL CPU: Open; SL-enabled CPU: Closed
JP11 – Pin D17 – Reset connection
CPURST: 1-2; RSTDRV: 2-3
JP12 – Pin D11/C13 – CPURST connection
Pin D11: 1-2; Pin C14: 2-3
JP13 – Pin D15/B14 – FERR# connection
486DX/ODPR/5x86: 1-2; 487DX/ODP/P24T: 2-3; 486SX: Open or 2-3?
JP19 – Pin C14 – CPU select
1-2: Pull-up; 2-3: GND
JP21 – Pin D13/D11 – SMIACT# connection
Non-SL CPU: Open; Intel/AMD SL: 1-2; Cyrix/IBM: 2-3
JP23 – Pin B16/C16 – IGNNE#/NMI connection
486SX: 2-3; All non 486SX: 1-2,3-4
JP30 – Pin S18/R16
JP32 – Pin S18/B13 – HITM connection
JP46 – Pin B13 – IBM_SMI# connection
Non-IBM: 1-2, Cyrix/IBM: 2-3
CA2
CA3
CA4
CA5
CA6
CA7
CA8
CA9
CA10
CA11
CA12
CA13
CA14
CA15
CA16
CA17
CA18
CA19
CA20
CA21
CA22
CA23
CA24
CA25
CA26
CA27
CA28
CA29
CA30
CA31
BE0#
BE1#
BE2#
BE3#
PCHK#
M_IO#
D_C#
W_R#
LOCK#
PLOCK#
ADS#
BLAST#
BREQ
HLDA
PWT
PCD
INC/FERR#
VCC5
R35
100
GND
U16B
Intel_P24T
CPURST
PIN_D11
SMI#
PIN_H16
EWBE#
BLEN#
WB_WT#
PIN_C14
WB/WT#
INC/WB/WT#
INV
INC/INV
INC/UP#
INC/TCK
INC/TDI
PIN_S18
CLKMUL
INIT
INC/INIT/SRESET
SMI#
STPCLK#
Pin C15 is connected to JP22 (not populated)
JP22 is connected to 10k pull-up (to VCC)
Pins A3, C3 are connected to GND
Pins A4, D1 are connected to VCC/5V
SMIACT#
PIN_D13
HIT#
INC/HITM#
HITM#
IBM_SMI#
CACHE#
INC/CACHE#
FERR#
PIN_B14
INC/TDO
UP#/TMS
VOLDET
PIN_T5
JP9
Intel/Cyrix
R68
10k
R47
1k
JP19
CPU Select 2
JP30
CPU Select 3
JP10
SMI Enable
SMI#/PPEN#
JP11
Reset Select
RSTDRV
JP21
CPU Select 3
JP32
CPU Select 4
JP12
CPU Select 1
JP13
FERR Select
R42
10k
JP23
NMI/IGNNE#
JP20
STPCLK
Sheet: /Processor/
File: Processor.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 2/17



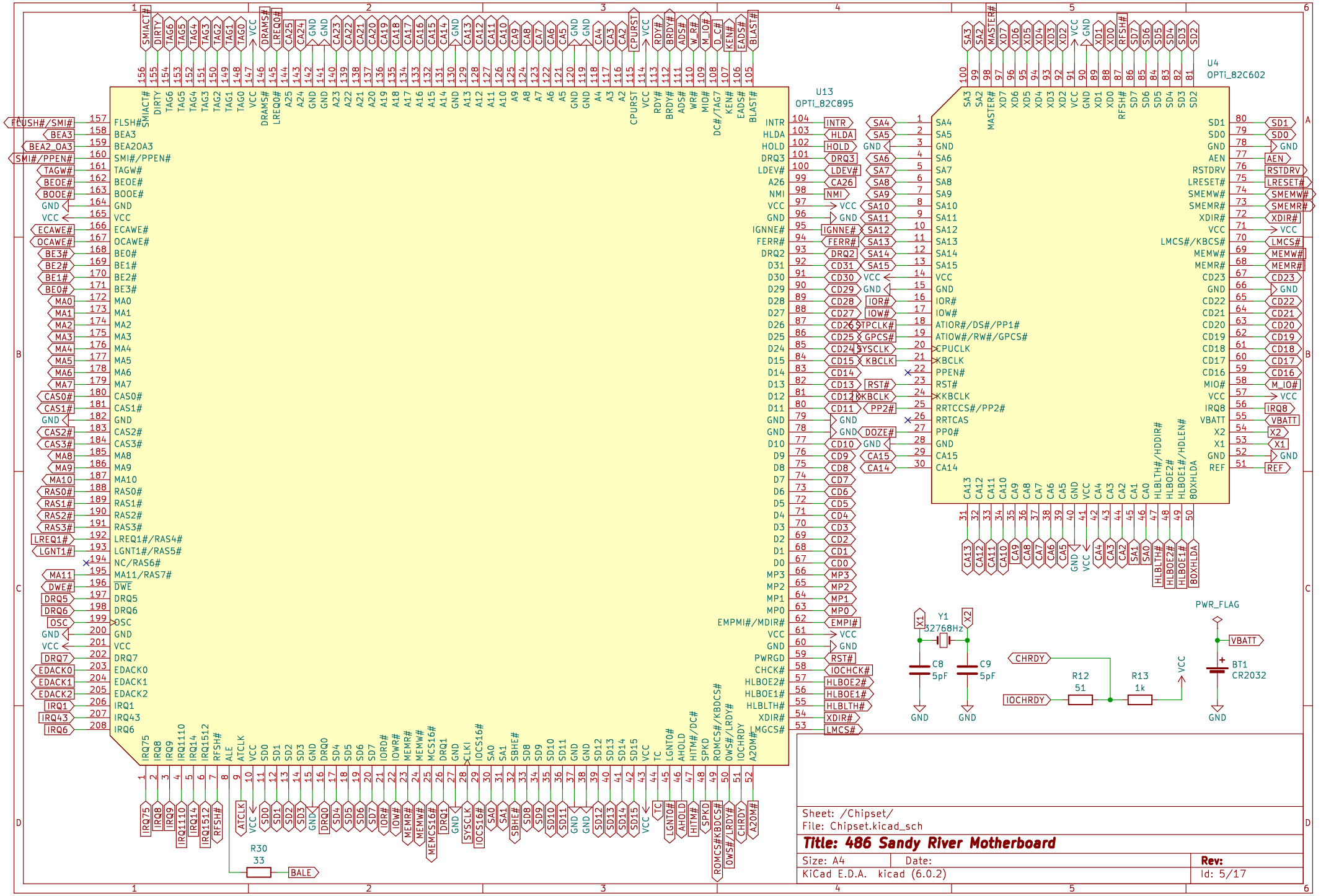
Sheet: /ISA/
File: ISA.kicad_sch

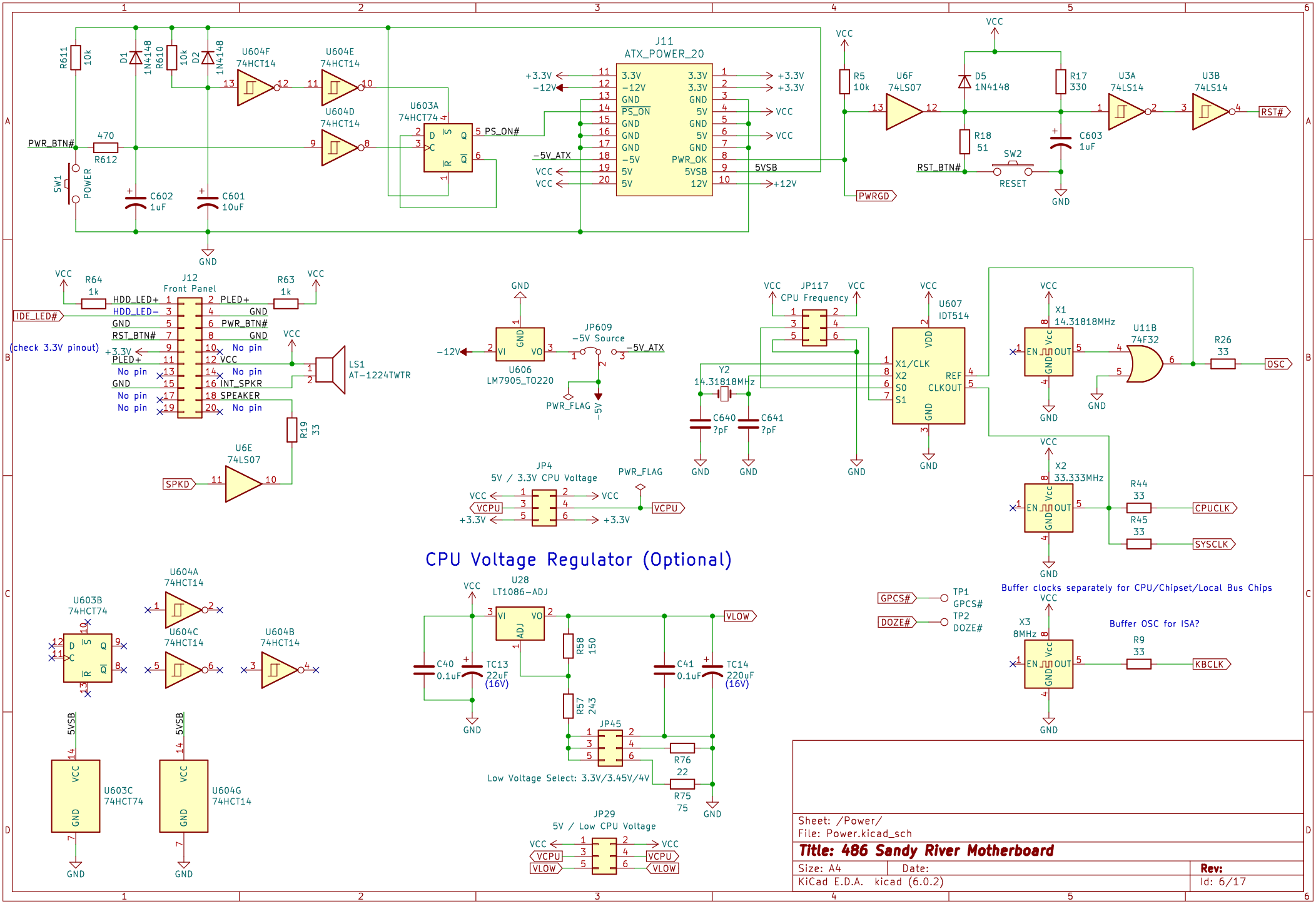
Title: 486 Sandy River Motherboard

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (6.0.2)		Id: 3/17



Sheet: /Memory/		
File: Memory.kicad_sch		
Title: 486 Sandy River Motherboard		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.2)		Id: 4/17

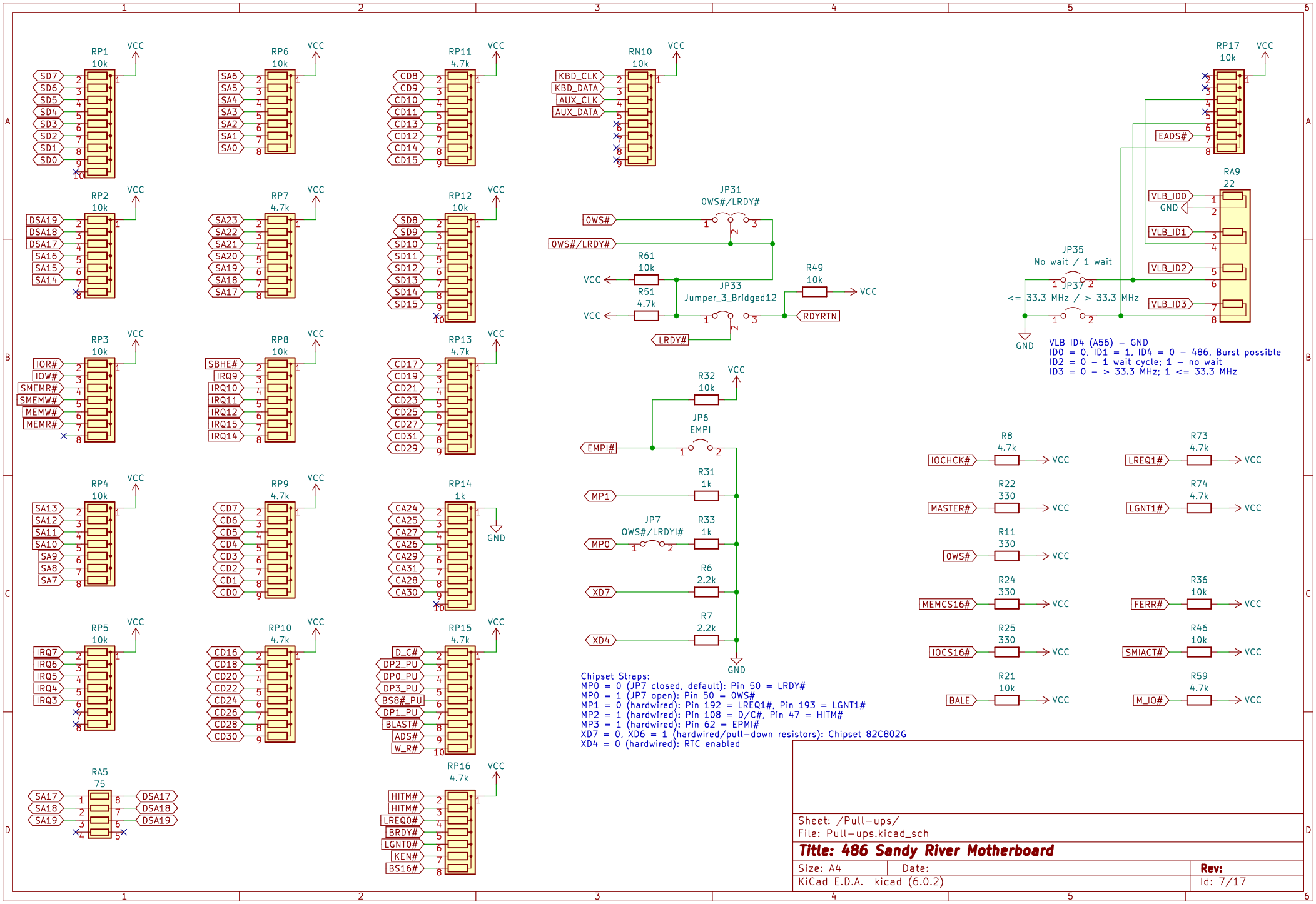

U13
OPTi_82C895
U4
OPTi_82C602
Y1
32768Hz
C8
5pF
C9
5pF
R30
33
BALE
R12
51
R13
1k
CHRDY
IOCHRDY
VCC
PWR_FLAG
VBATT
BT1
CR2032
GND
Sheet: /Chipset/
File: Chipset.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 5/17

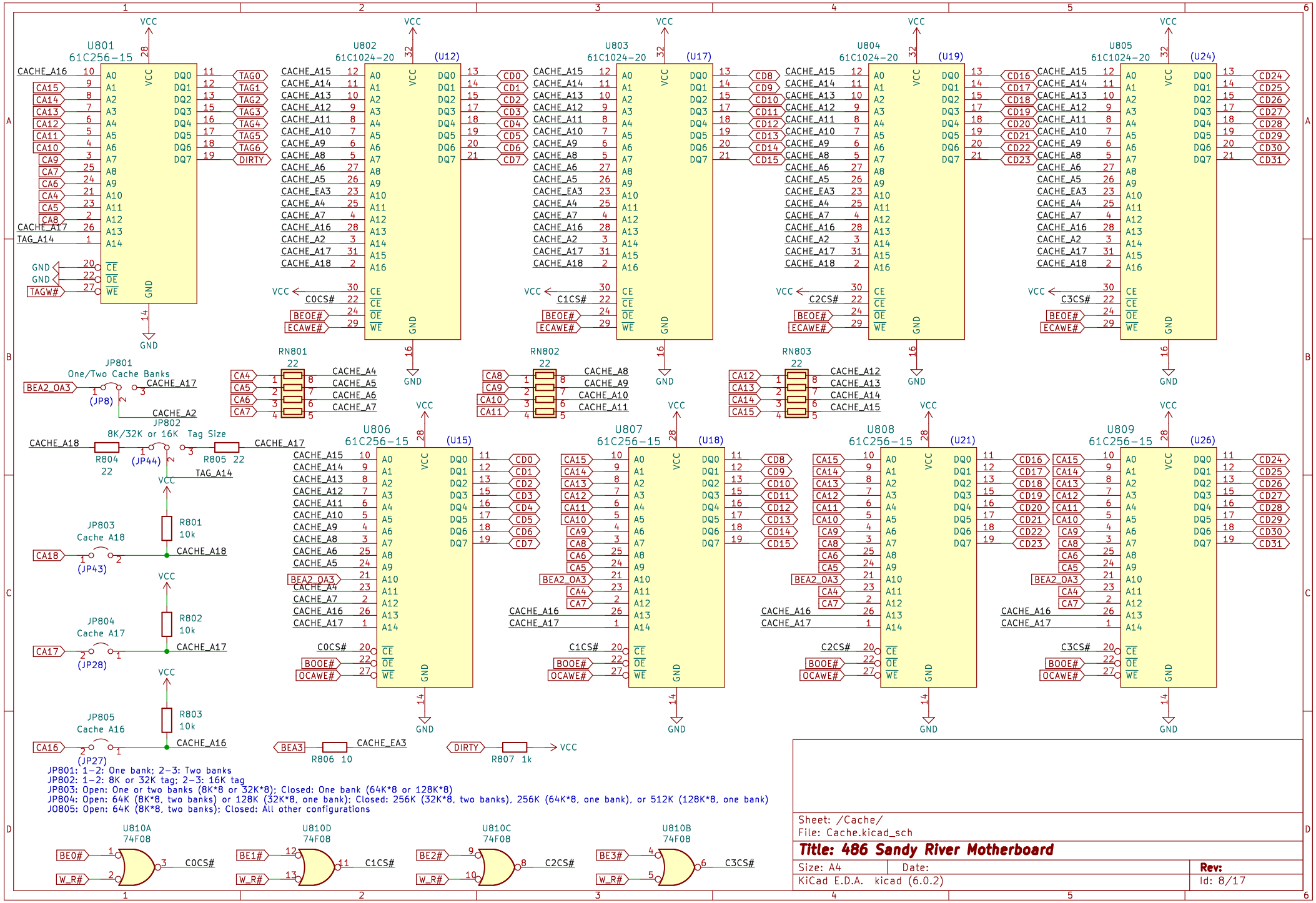


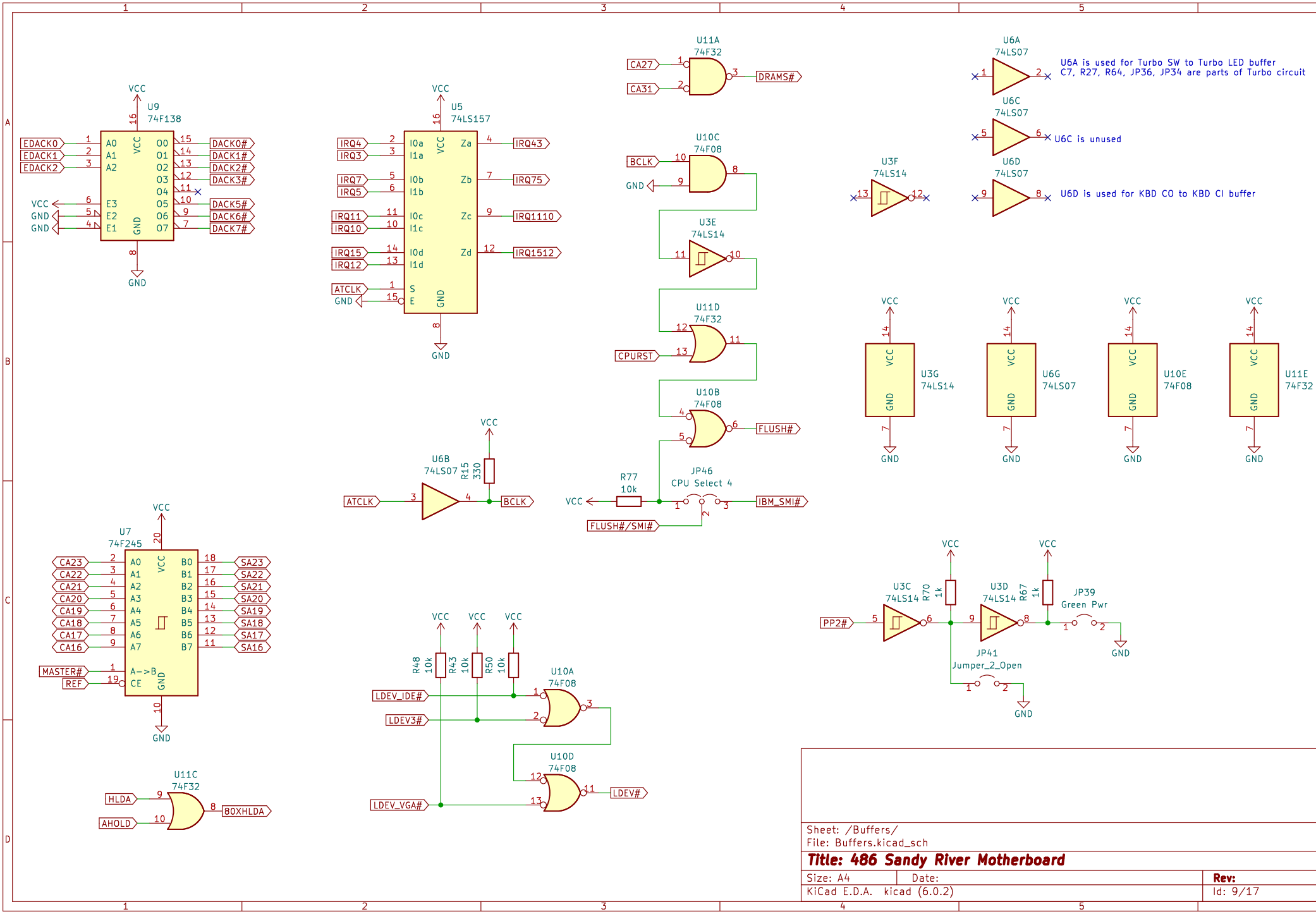
Sheet: /Power/
File: Power.kicad_sch

Title: 486 Sandy River Motherboard

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (6.0.2)		Id: 6/17


RP1
10k
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
VCC
RP6
10k
SA6
SA5
SA4
SA3
SA2
SA1
SA0
RP11
4.7k
CD8
CD9
CD10
CD11
CD13
CD12
CD14
CD15
RN10
10k
KBD_CLK
KBD_DATA
AUX_CLK
AUX_DATA
RP17
10k
EADS#
RA9
22
VLB_ID0
GND
VLB_ID1
VLB_ID2
VLB_ID3
JP35
No wait / 1 wait
JP37
<= 33.3 MHz / > 33.3 MHz
VLB ID4 (A56) - GND
ID0 = 0, ID1 = 1, ID4 = 0 - 486, Burst possible
ID2 = 0 - 1 wait cycle; 1 - no wait
ID3 = 0 - > 33.3 MHz; 1 <= 33.3 MHz
RP2
10k
DSA19
DSA18
DSA17
SA16
SA15
SA14
RP7
4.7k
SA23
SA22
SA21
SA20
SA19
SA18
SA17
RP12
10k
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
JP31
OWS#/LRDY#
OWS#
OWS#/LRDY#
R61
10k
R51
4.7k
JP33
Jumper_3_Bridged12
R49
10k
RDYRTN
LRDY#
RP3
10k
IOR#
IOW#
SMEMR#
SMEMW#
MEMW#
MEMR#
RP8
10k
SBHE#
IRQ9
IRQ10
IRQ11
IRQ12
IRQ15
IRQ14
RP13
4.7k
CD17
CD19
CD21
CD23
CD25
CD27
CD31
CD29
R32
10k
JP6
EMPI
EMPI#
R31
1k
MP1
JP7
OWS#/LRDYI#
MP0
R33
1k
R6
2.2k
XD7
R7
2.2k
XD4
GND
Chipset Straps:
MP0 = 0 (JP7 closed, default): Pin 50 = LRDY#
MP0 = 1 (JP7 open): Pin 50 = OWS#
MP1 = 0 (hardwired): Pin 192 = LREQ1#, Pin 193 = LGNT1#
MP2 = 1 (hardwired): Pin 108 = D/C#, Pin 47 = HITM#
MP3 = 1 (hardwired): Pin 62 = EPMI#
XD7 = 0, XD6 = 1 (hardwired/pull-down resistors): Chipset 82C802G
XD4 = 0 (hardwired): RTC enabled
RP4
10k
SA13
SA12
SA11
SA10
SA9
SA8
SA7
RP9
4.7k
CD7
CD6
CD5
CD4
CD3
CD2
CD1
CD0
RP14
1k
CA24
CA25
CA27
CA26
CA29
CA31
CA28
CA30
GND
R8
4.7k
IOCHCK#
R73
4.7k
LREQ1#
R22
330
MASTER#
R74
4.7k
LGNT1#
R11
330
OWS#
R24
330
MEMCS16#
R36
10k
FERR#
R25
330
IOCS16#
R46
10k
SMIACT#
R21
10k
BALE
R59
4.7k
M_IO#
RP5
10k
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
RP10
4.7k
CD16
CD18
CD20
CD22
CD24
CD26
CD28
CD30
RP15
4.7k
D_C#
DP2_PU
DP0_PU
DP3_PU
BS8#_PU
DP1_PU
BLAST#
ADS#
W_R#
RA5
75
SA17
SA18
SA19
DSA17
DSA18
DSA19
RP16
4.7k
HITM#
HITM#
LREQ0#
BRDY#
LGNT0#
KEN#
BS16#
Sheet: /Pull-ups/
File: Pull-ups.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 7/17

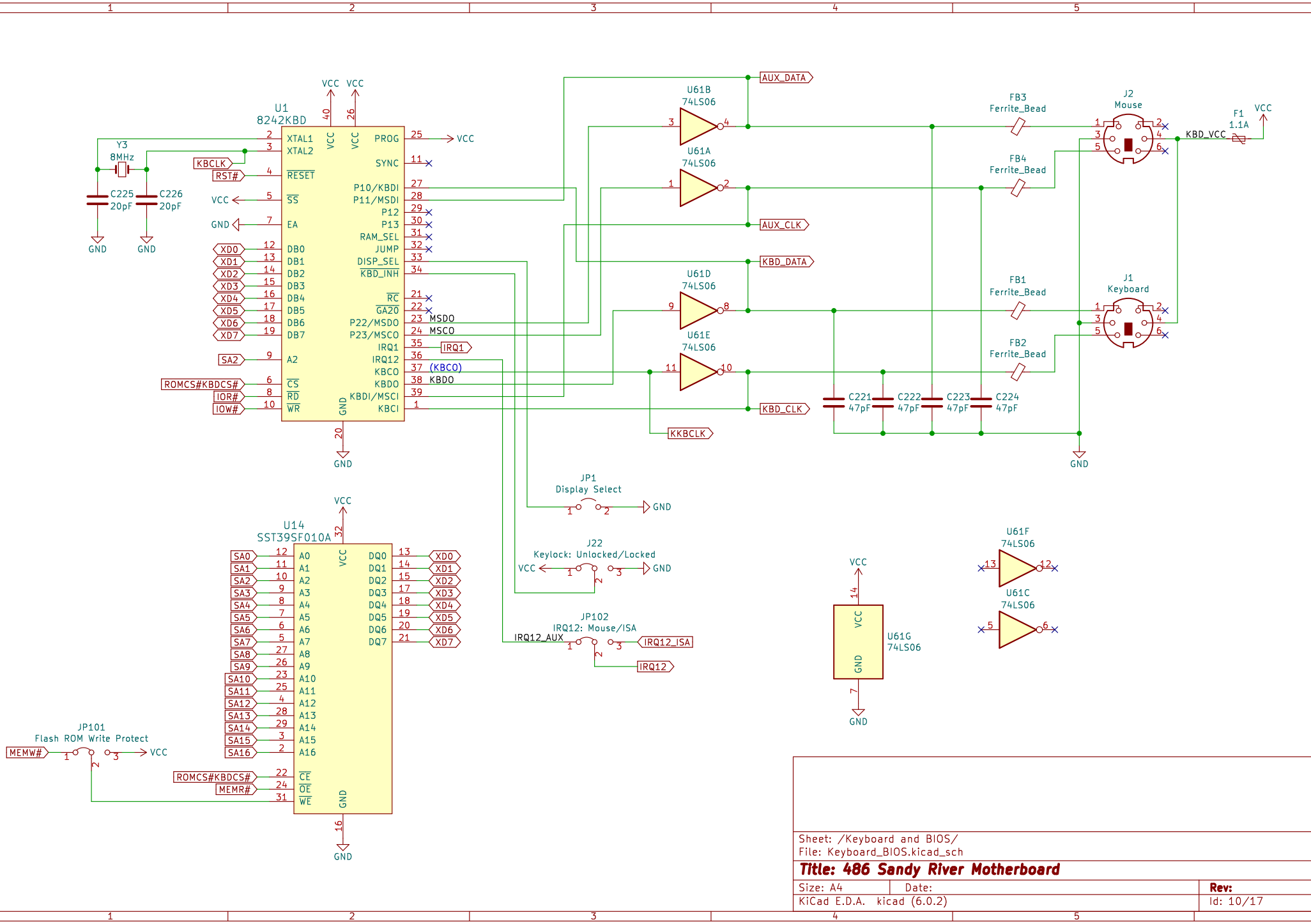

U801
61C256-15
U802
61C1024-20
(U12)
U803
61C1024-20
(U17)
U804
61C1024-20
(U19)
U805
61C1024-20
(U24)
U806
61C256-15
(U15)
U807
61C256-15
(U18)
U808
61C256-15
(U21)
U809
61C256-15
(U26)
VCC
GND
JP801
One/Two Cache Banks
(JP8)
JP802
8K/32K or 16K Tag Size
(JP44)
R804 22
R805 22
RN801 22
RN802 22
RN803 22
JP803
Cache A18
(JP43)
JP804
Cache A17
(JP28)
JP805
Cache A16
(JP27)
R801 10k
R802 10k
R803 10k
BEA3
R806 10
DIRTY
R807 1k
JP801: 1-2: One bank; 2-3: Two banks
JP802: 1-2: 8K or 32K tag; 2-3: 16K tag
JP803: Open: One or two banks (8K*8 or 32K*8); Closed: One bank (64K*8 or 128K*8)
JP804: Open: 64K (8K*8, two banks) or 128K (32K*8, one bank); Closed: 256K (32K*8, two banks), 256K (64K*8, one bank), or 512K (128K*8, one bank)
JO805: Open: 64K (8K*8, two banks); Closed: All other configurations
U810A
74F08
U810D
74F08
U810C
74F08
U810B
74F08
Sheet: /Cache/
File: Cache.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 8/17



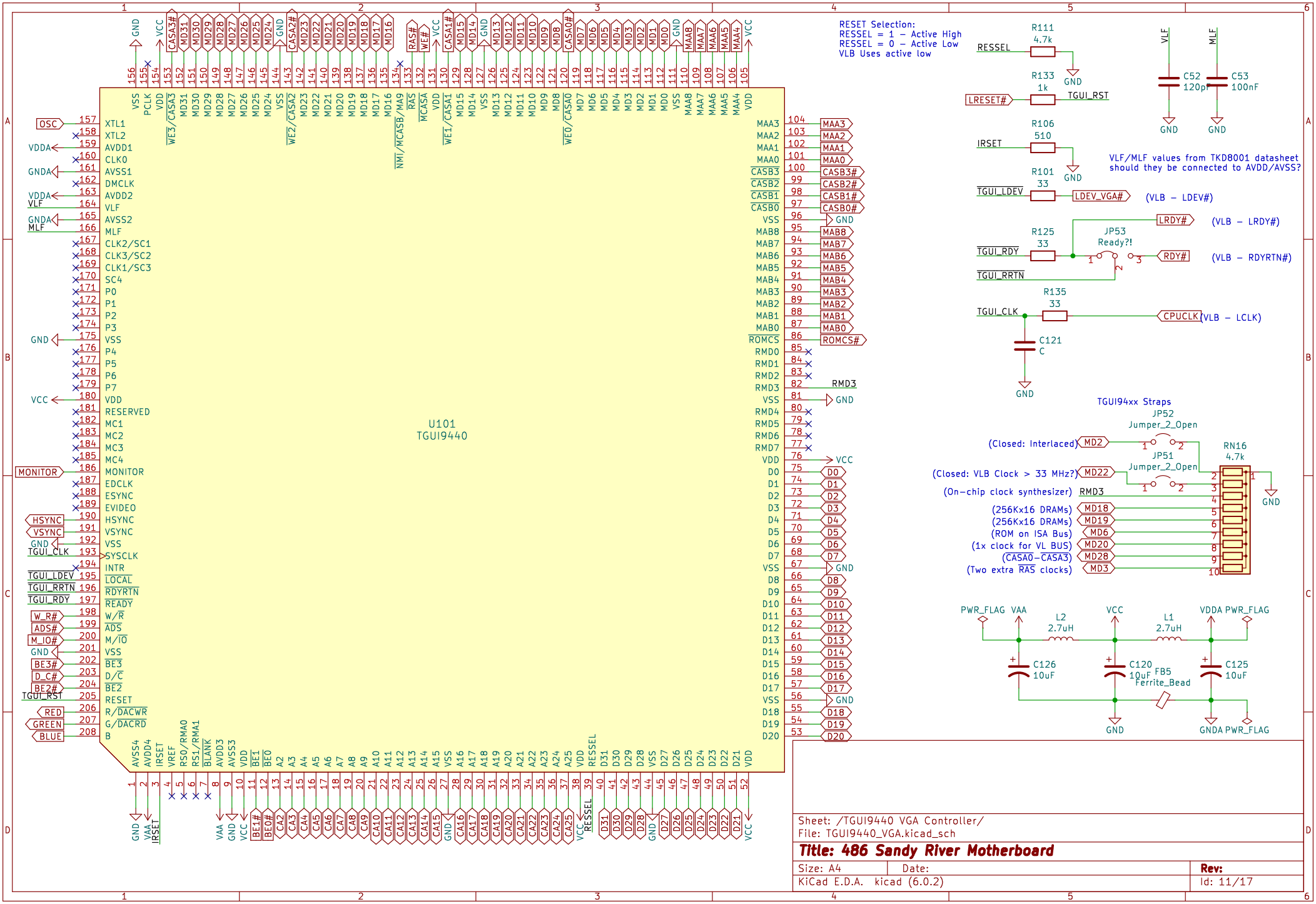
Sheet: /Buffers/
File: Buffers.kicad_sch

Title: 486 Sandy River Motherboard

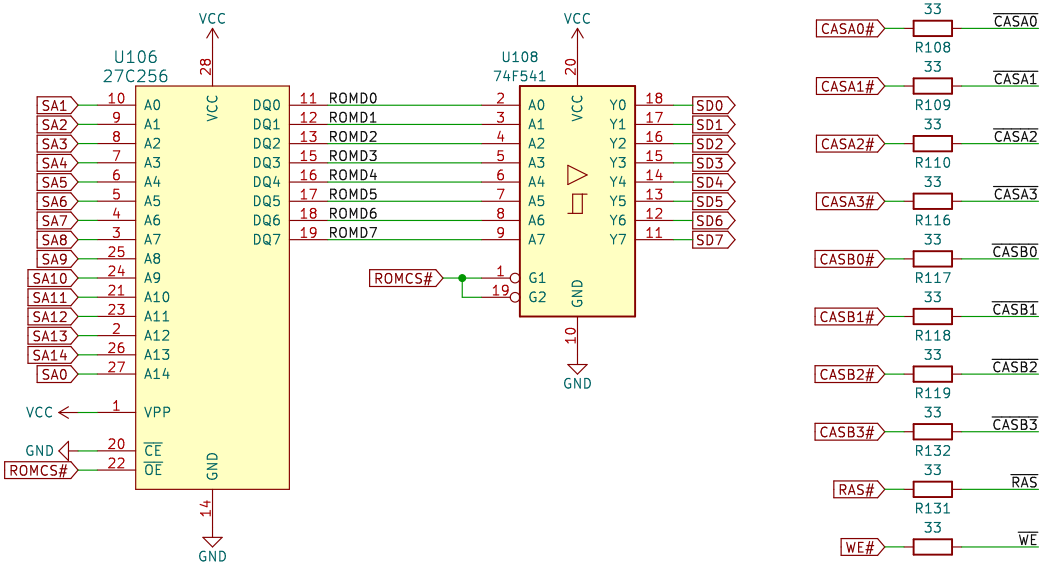
Size: A4	Date:	Rev:
KiCad E.D.A. kicad (6.0.2)		Id: 9/17



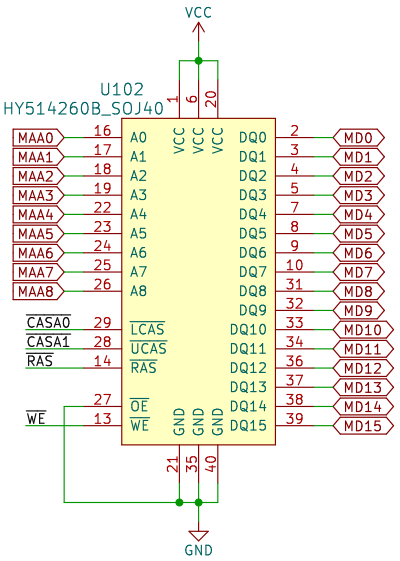
Sheet: /Keyboard and BIOS/		
File: Keyboard_BIOS.kicad_sch		
Title: 486 Sandy River Motherboard		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.2)		Id: 10/17

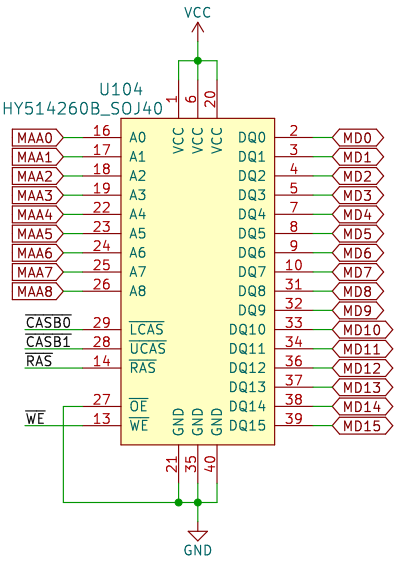

U101
TGUI9440
RESET Selection:
RESSEL = 1 – Active High
RESSEL = 0 – Active Low
VLB Uses active low
R111 4.7k
R133 1k
R106 510
R101 33
R125 33
R135 33
C52 120pF
C53 100nF
C121 C
JP53 Ready?!
VLF/MLF values from TKD8001 datasheet should they be connected to AVDD/AVSS?
(VLB – LDEV#)
(VLB – LRDY#)
(VLB – RDYRTN#)
(VLB – LCLK)
TGUI94xx Straps
JP52 Jumper_2_Open
JP51 Jumper_2_Open
RN16 4.7k
(Closed: Interlaced)
(Closed: VLB Clock > 33 MHz?)
(On–chip clock synthesizer)
(256Kx16 DRAMs)
(256Kx16 DRAMs)
(ROM on ISA Bus)
(1x clock for VL BUS)
(CASA0–CASA3)
(Two extra RAS clocks)
L2 2.7uH
L1 2.7uH
C126 10uF
C120 10uF
C125 10uF
FB5 Ferrite_Bead
PWR_FLAG
Sheet: /TGUI9440 VGA Controller/
File: TGUI9440_VGA.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 11/17

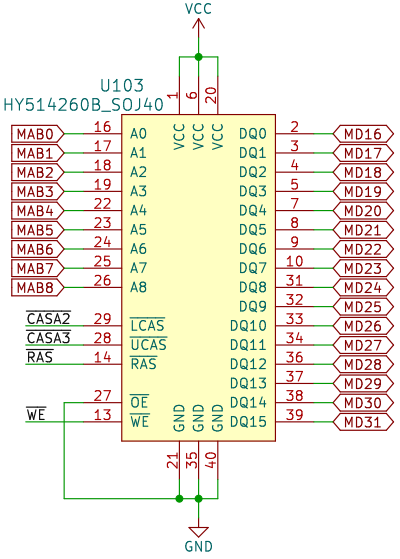
Trident VGA BIOS has
even bytes at 0x0000–0x3FFF and
odd bytes at 0x4000–0x7FFF
Therefore SA0 is connected to A14
It might be possible to move VGA BIOS to
System BIOS ROM at 0xE0000, but that requires
chipset initialization modification (evaluate)

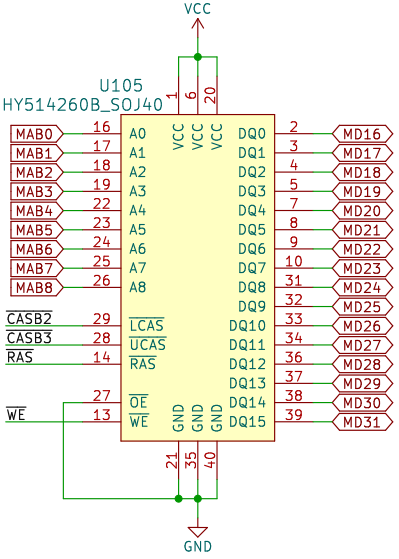


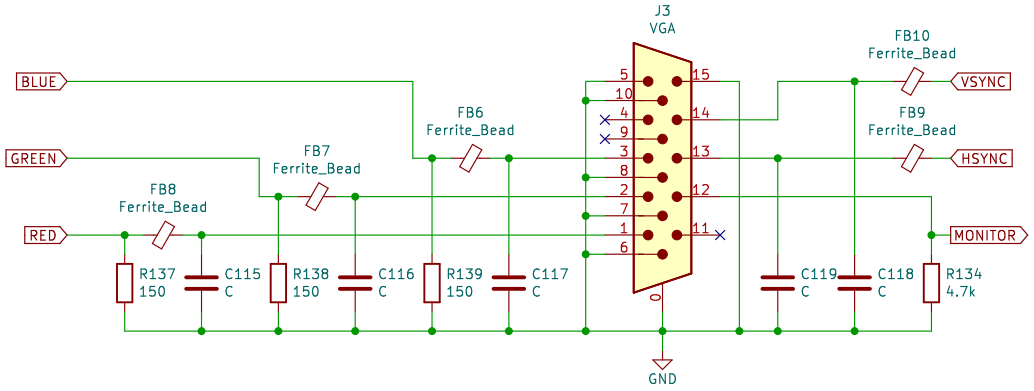
Replace with a
resistor array



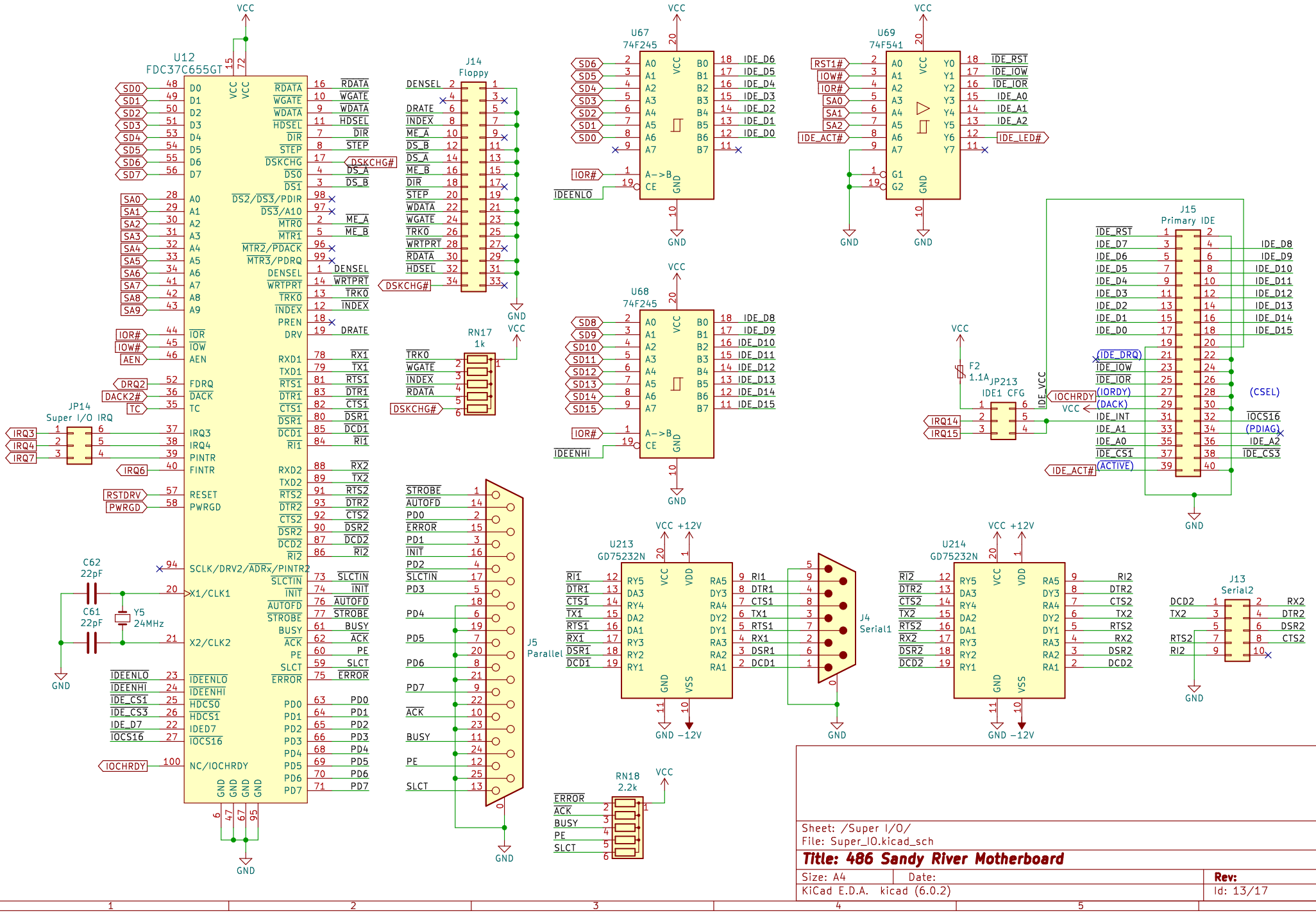


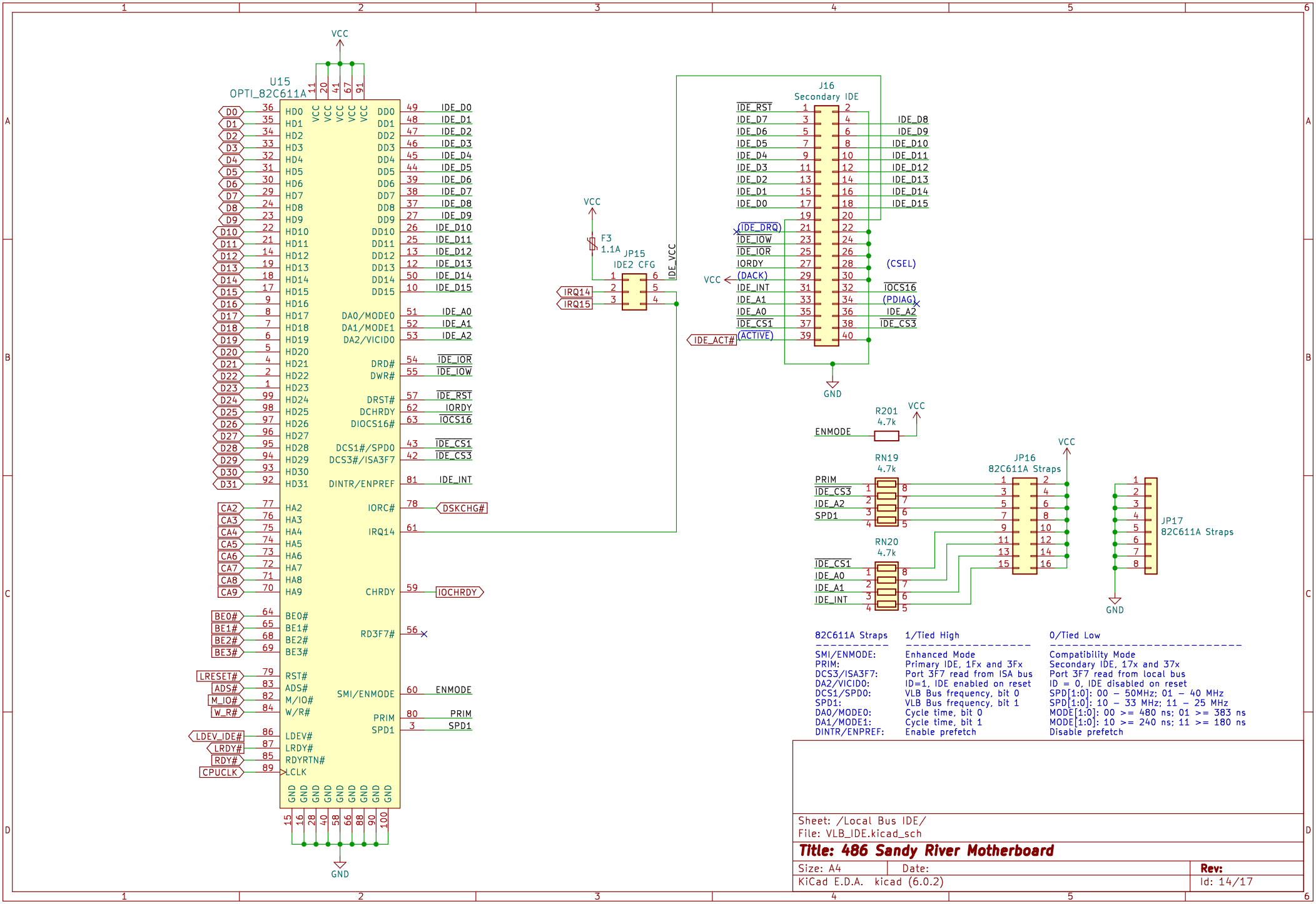






Sheet: /TGUI9440 VGA Memory/		
File: TGUI9440_Mem.kicad_sch		
Title: 486 Sandy River Motherboard		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.2)		Id: 12/17


U12
FDC37C655GT
U67
74F245
U68
74F245
U69
74F541
J14
Floppy
RN17
1k
RN18
2.2k
JP14
Super I/O IRQ
JP213
IDE1 CFG
F2
1.1A
J15
Primary IDE
C62
22pF
C61
22pF
Y5
24MHz
J5
Parallel
U213
GD75232N
U214
GD75232N
J4
Serial1
J13
Serial2
VCC
GND
VCC +12V
GND −12V
Sheet: /Super I/O/
File: Super_IO.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 13/17

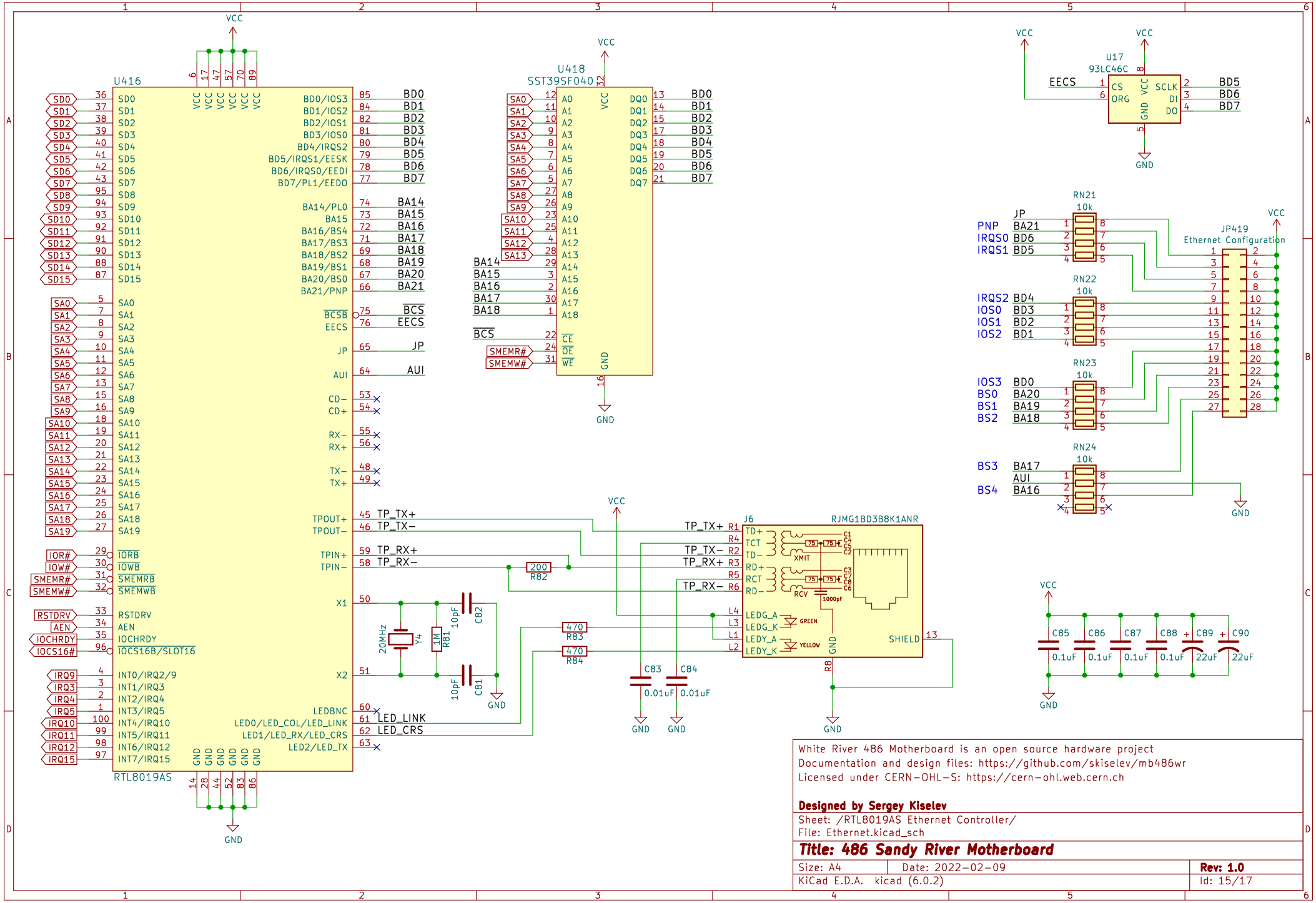


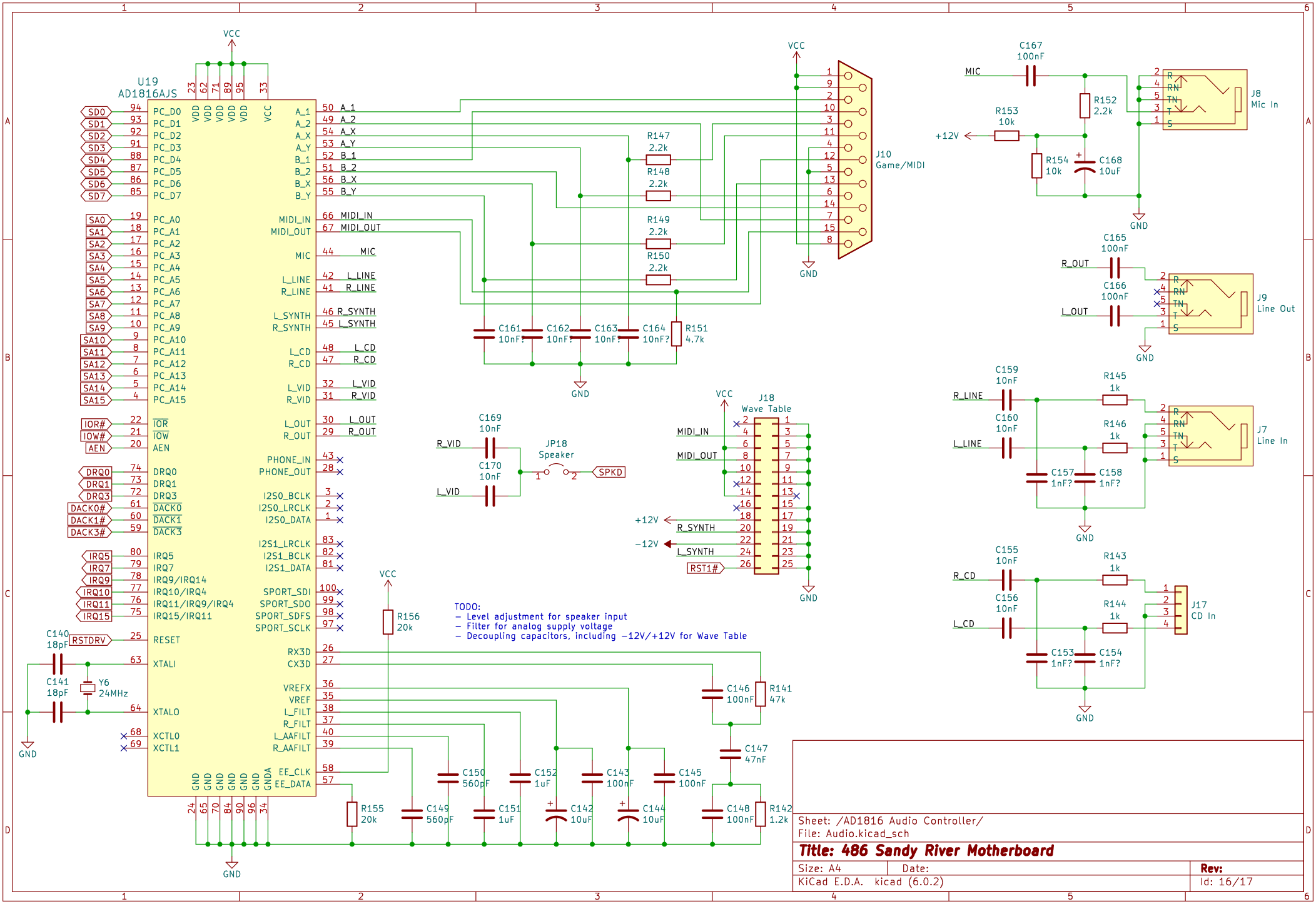
82C611A Straps	1/Tied High	0/Tied Low
SMI/ENMODE:	Enhanced Mode	Compatibility Mode
PRIM:	Primary IDE, 1Fx and 3Fx	Secondary IDE, 17x and 37x
DCS3/ISA3F7:	Port 3F7 read from ISA bus	Port 3F7 read from local bus
DA2/VICID0:	ID=1, IDE enabled on reset	ID = 0, IDE disabled on reset
DCS1/SPD0:	VLB Bus frequency, bit 0	SPD[1:0]: 00 – 50MHz; 01 – 40 MHz
SPD1:	VLB Bus frequency, bit 1	SPD[1:0]: 10 – 33 MHz; 11 – 25 MHz
DA0/MODE0:	Cycle time, bit 0	MODE[1:0]: 00 >= 480 ns; 01 >= 383 ns
DA1/MODE1:	Cycle time, bit 1	MODE[1:0]: 10 >= 240 ns; 11 >= 180 ns
DINTR/ENPREF:	Enable prefetch	Disable prefetch

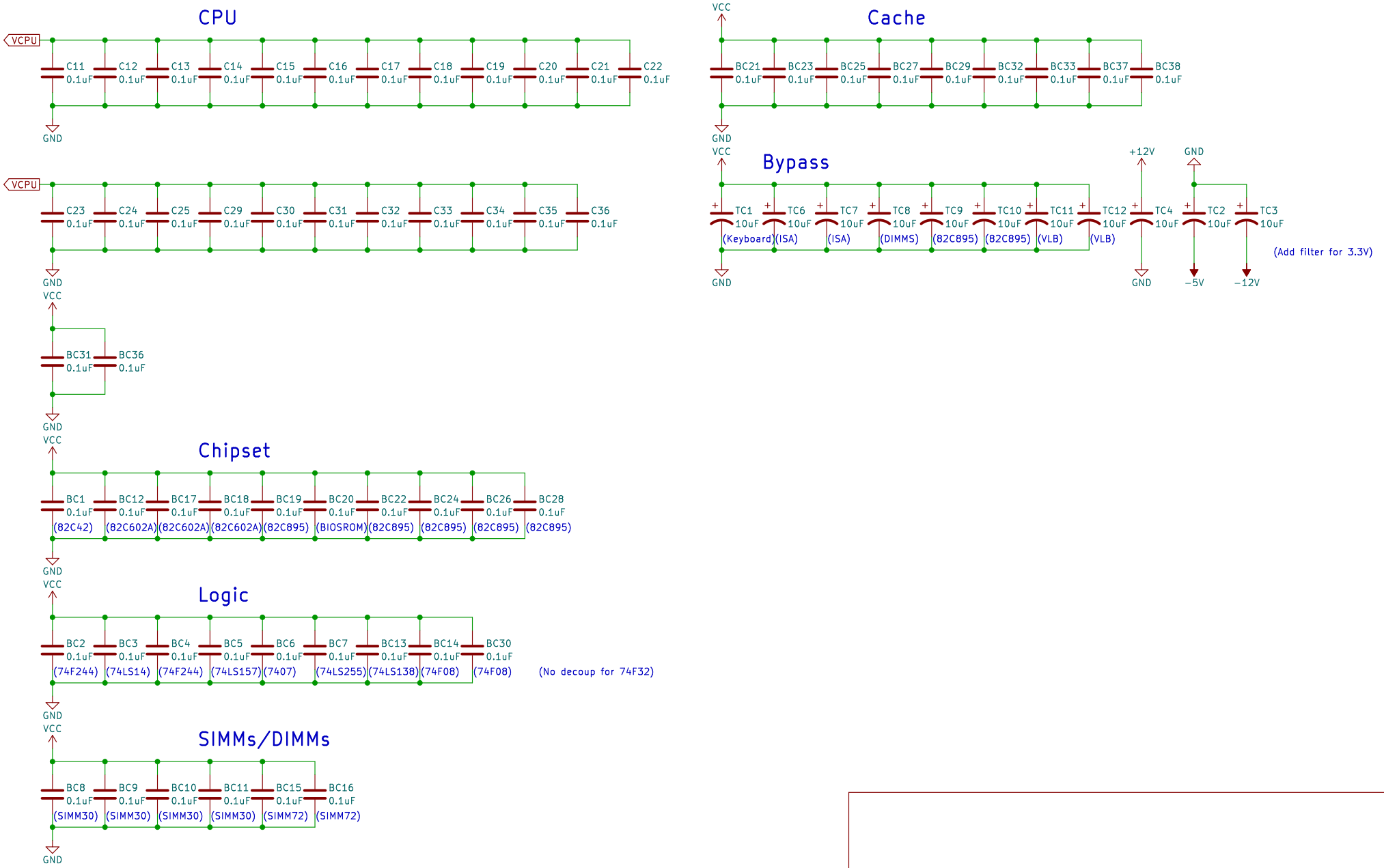
Sheet: /Local Bus IDE/
File: VLB_IDE.kicad_sch

Title: 486 Sandy River Motherboard

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (6.0.2)		Id: 14/17


U416
RTL8019AS
U418
SST39SF040
U17
93LC46C
JP419
Ethernet Configuration
RN21
RN22
RN23
RN24
10k
J6
RJMG1BD3B8K1ANR
VCC
GND
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BA14
BA15
BA16
BA17
BA18
BA19
BA20
BA21
BCS
EECS
JP
AUI
TP_TX+
TP_TX−
TP_RX+
TP_RX−
LED_LINK
LED_CRS
20MHz
Y4
SHIELD
XMIT
RCV
GREEN
YELLOW
White River 486 Motherboard is an open source hardware project
Documentation and design files: https://github.com/skiselev/mb486wr
Licensed under CERN−OHL−S: https://cern−ohl.web.cern.ch
Designed by Sergey Kiselev
Sheet: /RTL8019AS Ethernet Controller/
File: Ethernet.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date: 2022−02−09
Rev: 1.0
KiCad E.D.A. kicad (6.0.2)
Id: 15/17


U19
AD1816AJS
VCC
GND
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
IOR#
IOW#
AEN
DRQ0
DRQ1
DRQ3
DACK0#
DACK1#
DACK3#
IRQ5
IRQ7
IRQ9
IRQ10
IRQ11
IRQ15
RSTDRV
XTALI
XTALO
XCTL0
XCTL1
A_1
A_2
A_X
A_Y
B_1
B_2
B_X
B_Y
MIDI_IN
MIDI_OUT
MIC
L_LINE
R_LINE
R_SYNTH
L_SYNTH
L_CD
R_CD
L_VID
R_VID
L_OUT
R_OUT
PHONE_IN
PHONE_OUT
I2S0_BCLK
I2S0_LRCLK
I2S0_DATA
I2S1_LRCLK
I2S1_BCLK
I2S1_DATA
SPORT_SDI
SPORT_SDO
SPORT_SDFS
SPORT_SCLK
RX3D
CX3D
VREFX
VREF
L_FILT
R_FILT
L_AAFILT
R_AAFILT
EE_CLK
EE_DATA
J10
Game/MIDI
J8
Mic In
J9
Line Out
J7
Line In
J17
CD In
J18
Wave Table
JP18
Speaker
SPKD
RST1#
+12V
-12V
TODO:
– Level adjustment for speaker input
– Filter for analog supply voltage
– Decoupling capacitors, including −12V/+12V for Wave Table
Sheet: /AD1816 Audio Controller/
File: Audio.kicad_sch
Title: 486 Sandy River Motherboard
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (6.0.2)
Id: 16/17



Sheet: /Decoupling Dapacitors/
File: Decoup_caps.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.2)		Id: 17/17