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VHSIC Hardware Description Language Data Structures Computer Programming

What is the difference between structural, behavioural and data flow model in VHDL?

3 Answers



Harshul Mahendroo, studied at Modern Vidya Niketan Aravali Hills (2012) Answered Sep 13

Basically, Structural Modeling is the set of interconnected components. That is, it describes the structure (as in, the components that are visible in a structure). The visible components are instantiated in the declarative part of the architecture body while the declared components are instantiated with their respective interface ports in the statement part of the architecture body. Structural Modeling doesn't say anything about functionality.

The component instantiation statements are concurrent in nature. Thus, the order of these statements is not important.

Dataflow Modeling on the other side, includes declaration of a target signal using logical events occurring on the particular signal. Dataflow Modeling is primarily expressed using signal assignment statements. The structure of the entity in this can be easily deduced. In this case, a target signal is expressed using logical operations. The signal assignment statements are concurrent in nature, again the order in architecture body doesn't matter.

Whereas, Behavioral Modeling deals with the functionality of an entity. Here, the set of statements are executed sequentially in a specified order, mainly specified within a process statement. The process statement is itself a concurrent statement but inside it lies a set of statements which are all sequential in nature.

There is also another style of modeling, known as Mixed Modelling. This style of modeling possibly is the combination of any of the above mentioned modeling styles.

Each of these modeling method has a depth on its own. They are quite simple to understand yet get complex with increasing depth.

Feel free to ask if you have any doubts.:)

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| assign sum = ip1 ^ ip2; | | | |
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| endmodule | | | |
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| | ast complex and behavior of the logic | e is | |
| modeled. This is best for describing | sequentiai circuit. | | |
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| Rucha Deshmukh, studied Electr Pune Institute of Computer Techr Answered Dec 30 | onics and Telecommunication Engineerin nology (2018) | g at | |
| 1. Dataflow modelling uses Boolean | equations as design specifications. F | or eg. to | |
| design AND gate you use the equation | on y <= a & b; | | |
| Statements are executed concurrent | ly. | | |
| 2. Behavioural modelling executes s | tatements sequentially. | | |
| They are written inside a process sta | tement. Statements like if-else , swit | ch case, | |
| loops are part of behavioural model | ing. | | |
| Although we never use looping state difficult to implement on board. | ements while programming hardware | e as it is | |
| | | | |
| 3. Structural modelling uses logic di | agrams. | | |
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