VHSIC Hardware Description Language Data Structures Computer Programming

What is the difference between structural, behavioural and data flow model in VHDL?

3 Answers

Harshul Mahendroo, studied at Modern Vidya Niketan Aravali Hills (2012)
Answered Sep 13

Basically, Structural Modeling is the set of interconnected components. That is, it describes the structure (as in, the components that are visible in a structure). The visible components are instantiated in the declarative part of the architecture body while the declared components are instantiated with their respective interface ports in the statement part of the architecture body. Structural Modeling doesn't say anything about functionality.

The component instantiation statements are concurrent in nature. Thus, the order of these statements is not important.

Dataflow Modeling on the other side, includes declaration of a target signal using logical events occurring on the particular signal. Dataflow Modeling is primarily expressed using signal assignment statements. The structure of the entity in this can be easily deduced. In this case, a target signal is expressed using logical operations. The signal assignment statements are concurrent in nature, again the order in architecture body doesn't matter.

Whereas, Behavioral Modeling deals with the functionality of an entity. Here, the set of statements are executed sequentially in a specified order, mainly specified within a process statement. The process statement is itself a concurrent statement but inside it lies a set of statements which are all sequential in nature.

There is also another style of modeling, known as Mixed Modelling. This style of modeling possibly is the combination of any of the above mentioned modeling styles.

Each of these modeling method has a depth on its own. They are quite simple to understand yet get complex with increasing depth.
Feel free to ask if you have any doubts. :)

1.6k Views · View Upvoters

Related Questions More Answers Below

Related Questions

What is the difference between behavioral and structural code in VHDL?

What is primitive data structure?

What is the use of "linkage" port in VHDL?

What are the differences between B+Tree and B-Tree?

What is A flow chart for the VHDL design flow with explanation?

Features of data structures?

How do I model a memristor in VHDL? Is it possible?

What is the difference between creating a data structure and a class in Java?

What are the Applications of data structures?

What are data structures and why do we use them? What is their relationship with algorithms?

+ Ask New Question

flow with explanation?

Related Questions

What is the difference between behavioral and structural code in VHDL?

What is primitive data structure?

What is the use of "linkage" port in VHDL?

What are the differences between B+Tree and B-Tree?

What is A flow chart for the VHDL design flow with explanation?

Features of data structures?

How do I model a memristor in VHDL? Is it possible?

What is the difference between creating a data structure and a class in Java?

What are the Applications of data structures?

What are data structures and why do we use them? What is their relationship with algorithms?

+ Ask New Question

esign Systems

delling : Describing in terms of gates.

inbuilt gate in verilog and you have to

del you DUT in terms of equations. It's best

and its statement is concurrent in nature

2);

assign sum = ip1 ^ ip2;

assign carry = ip1 & ip2;

endmodule

Behavioral modelling : This is the least complex and behavior of the logic is modeled. This is best for describing sequential circuit.

828 Views · View Upvoters

Rucha Deshmukh, studied Electronics and Telecommunication Engineering at Pune Institute of Computer Technology (2018)

Answered Dec 30

1. Dataflow modelling uses Boolean equations as design specifications. For eg. to design AND gate you use the equation y <= a & b ;

Statements are executed concurrently.

2. Behavioural modelling executes statements sequentially.

They are written inside a process statement. Statements like if-else , switch case, loops are part of behavioural modelling.

Although we never use looping statements while programming hardware as it is difficult to implement on board.

3. Structural modelling uses logic diagrams.

n

Related Questions

What is the difference between behavioral and structural code in VHDL?

What is primitive data structure?

What is the use of "linkage" port in VHDL?

What are the differences between B+Tree and B-Tree?

What is A flow chart for the VHDL design flow with explanation?

Features of data structures?

How do I model a memristor in VHDL? Is it possible?

What is the difference between creating a data structure and a class in Java?

What are the Applications of data structures?

What are data structures and why do we use them? What is their relationship with algorithms?

t possible?

data structure and a class in Java?

es?

ıse them? What is their relationship with

e it in VHDL/RTL simulation?

ble and float data types?

ta type and data structure?

+ Ask New Question