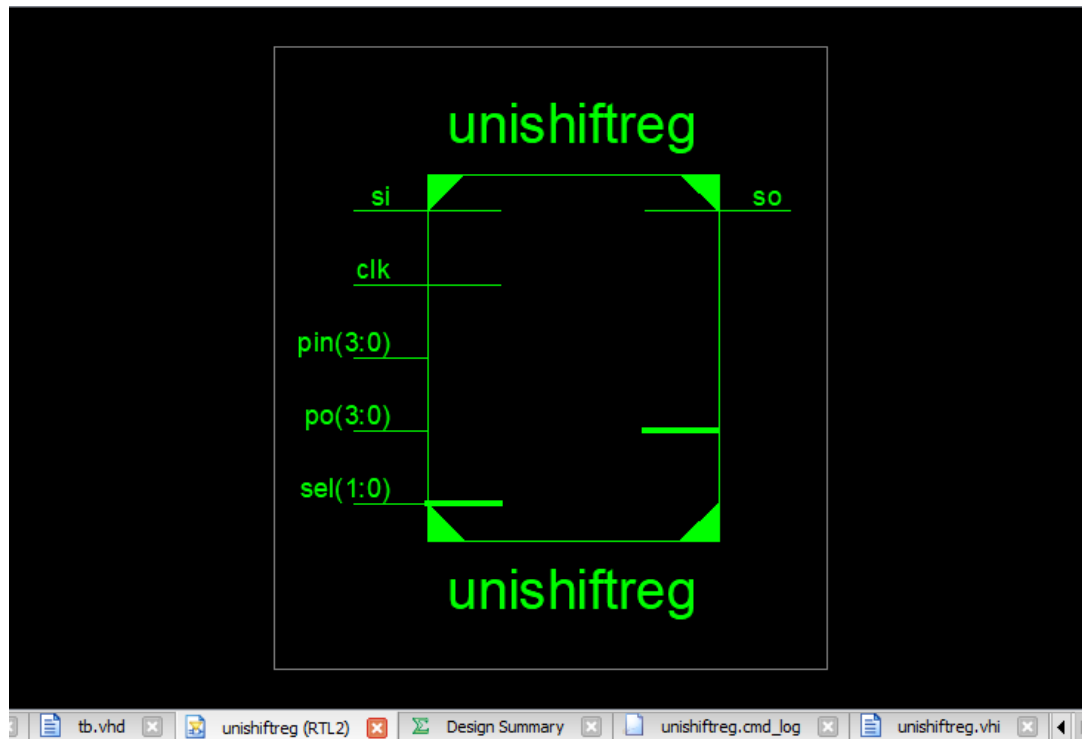


Name – Sujit Dhage Roll no = B43007

- ENTITY



- VHDL CODE:

-- Company:

-- Engineer:

--

-- Create Date: 09:32:53 09/13/2023

-- Design Name:

-- Module Name: C:/Users/Admin/Desktop/E41101/shiftreg/shiftreg.vhd

-- Project Name: shiftreg

-- Target Device:

-- Tool versions:

-- Description:

--

-- VHDL Test Bench Created by ISE for module: unishiftreg

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

-- Notes:

-- This testbench has been automatically generated using types std_logic and

-- std_logic_vector for the ports of the unit under test. Xilinx recommends

-- that these types always be used for the top-level I/O of a design in order

-- to guarantee that the testbench will bind correctly to the post-implementation

-- simulation model.

LIBRARY ieee;

USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--USE ieee.numeric_std.ALL;

ENTITY shiftreg IS

END shiftreg;

ARCHITECTURE behavior OF shiftreg IS

```

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT unishiftreg

PORT(

    si : IN    std_logic;

    clk : IN    std_logic;

    so : OUT    std_logic;

    pin : IN    std_logic_vector(3 downto 0);

    po : OUT    std_logic_vector(3 downto 0);

    sel : IN    std_logic_vector(1 downto 0)

);

END COMPONENT;

--Inputs

signal si : std_logic := '0';

signal clk : std_logic := '0';

signal pin : std_logic_vector(3 downto 0) := (others => '0');

signal sel : std_logic_vector(1 downto 0) := (others => '0');

--Outputs

signal so : std_logic;

signal po : std_logic_vector(3 downto 0);

-- Clock period definitions

constant clk_period : time := 10 ns;

BEGIN

    -- Instantiate the Unit Under Test (UUT)

    uut: unishiftreg PORT MAP (

        si => si,

```

```

        clk => clk,

        so => so,

        pin => pin,

        po => po,

        sel => sel

    );

-- Clock process definitions

clk_process :process

begin

    clk <= '0';

    wait for clk_period/2;

    clk <= '1';

    wait for clk_period/2;

end process;


-- Stimulus process

stim_proc: process

begin

    -- hold reset state for 100 ns.

    wait for 100 ns;

    wait for clk_period*10;

    -- insert stimulus here

    wait;

end process;

END;
```

- TESTBENCH

-- Company:

-- Engineer:

--

-- Create Date: 09:36:30 09/13/2023

-- Design Name:

-- Module Name: C:/Users/Admin/Desktop/E41101/shiftreg/tb.vhd

-- Project Name: shiftreg

-- Target Device:

-- Tool versions:

-- Description:

--

-- VHDL Test Bench Created by ISE for module: unishiftreg

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

-- Notes:

-- This testbench has been automatically generated using types std_logic and

-- std_logic_vector for the ports of the unit under test. Xilinx recommends

```
-- that these types always be used for the top-level I/O of a design in order
-- to guarantee that the testbench will bind correctly to the post-implementation
-- simulation model.
```

```
-----
```

```
LIBRARY ieee;
```

```
USE ieee.std_logic_1164.ALL;
```

```
-- Uncomment the following library declaration if using
```

```
-- arithmetic functions with Signed or Unsigned values
```

```
--USE ieee.numeric_std.ALL;
```

```
ENTITY tb IS
```

```
END tb;
```

```
ARCHITECTURE behavior OF tb IS
```

```
    -- Component Declaration for the Unit Under Test (UUT)
```

```
    COMPONENT unishftreg
```

```
    PORT(
```

```
        si : IN    std_logic;
```

```
        clk : IN   std_logic;
```

```
        so : OUT   std_logic;
```

```
        pin : IN   std_logic_vector(3 downto 0);
```

```
        po : OUT   std_logic_vector(3 downto 0);
```

```
        sel : IN   std_logic_vector(1 downto 0)
```

```
    );
```

```
    END COMPONENT;
```

```
--Inputs
```

```
signal si : std_logic := '0';  
  
signal clk : std_logic := '0';  
  
signal pin : std_logic_vector(3 downto 0) := (others => '0');  
  
signal sel : std_logic_vector(1 downto 0) := (others => '0');
```

```
--Outputs
```

```
signal so : std_logic;  
  
signal po : std_logic_vector(3 downto 0);
```

```
-- Clock period definitions
```

```
constant clk_period : time := 10 ns;
```

```
BEGIN
```

```
-- Instantiate the Unit Under Test (UUT)
```

```
uut: unishiftreg PORT MAP (
```

```
    si => si,
```

```
    clk => clk,
```

```
    so => so,
```

```
    pin => pin,
```

```
    po => po,
```

```
    sel => sel
```

```
);
```

```
-- Clock process definitions
```

```
clk_process :process
```

```
begin
```

```
    clk <= '0';
```

```
    wait for clk_period/2;
```

```
    clk <= '1';
```

```

        wait for clk_period/2;

end process;

-- Stimulus process

stim_proc: process

begin

    sel <= "00";

    si <= '1';

    wait for 100 ns;

    sel <= "01";

    si <= '1';

    wait for 100 ns;

    sel <= "10";

    pin <= "1010";

    wait for 100 ns;

    wait;

end process;

END;

```

- SYNTHESIS REPORT

Release 14.1 - xst P.15xf (nt64)

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--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.11 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.11 secs

--> Reading design: unishiftreg.prj

TABLE OF CONTENTS

- 1) Synthesis Options Summary
- 2) HDL Compilation
- 3) Design Hierarchy Analysis
- 4) HDL Analysis
- 5) HDL Synthesis
 - 5.1) HDL Synthesis Report
- 6) Advanced HDL Synthesis
 - 6.1) Advanced HDL Synthesis Report
- 7) Low Level Synthesis
- 8) Partition Report
- 9) Final Report
 - 9.1) Device utilization summary
 - 9.2) Partition Resource Summary
 - 9.3) TIMING REPORT

=====

* Synthesis Options Summary *

=====

---- Source Parameters

Input File Name : "unishiftreg.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "unishftreg"

Output Format : NGC

Target Device : xc3s400-5-pq208

---- Source Options

Top Module Name : unishftreg

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : Yes

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : Yes

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : Auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 8

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
Verilog 2001 : YES
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

=====

=====

* HDL Compilation *

=====

Compiling vhd file "C:/Users/Admin/Desktop/E41101/shiftreg/unishiftreg.vhd" in Library work.

Architecture behavioral of Entity unishiftreg is up to date.

=====

* Design Hierarchy Analysis *

=====

Analyzing hierarchy for entity <unishiftreg> in library <work> (architecture <behavioral>).

=====

* HDL Analysis *

=====

Analyzing Entity <unishiftreg> in library <work> (Architecture <behavioral>).

Entity <unishiftreg> analyzed. Unit <unishiftreg> generated.

=====

* HDL Synthesis *

=====

Performing bidirectional port resolution...

Synthesizing Unit <unishiftreg>.

Related source file is "C:/Users/Admin/Desktop/E41101/shiftreg/unishiftreg.vhd".

WARNING:Xst:647 - Input <pin> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

Found 1-bit register for signal <so>.

Found 4-bit register for signal <po>.

Found 4-bit register for signal <temp>.

Summary:

inferred 9 D-type flip-flop(s).

Unit <unishiftreg> synthesized.

=====

HDL Synthesis Report

Macro Statistics

# Registers	: 3
1-bit register	: 1
4-bit register	: 2

=====

=====

* Advanced HDL Synthesis *

=====

=====

Advanced HDL Synthesis Report

Macro Statistics

# Registers	: 9
Flip-Flops	: 9

=====

=====

* Low Level Synthesis *

=====

Optimizing unit <unishftreg> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block unishftreg, actual ratio is 0.

Final Macro Processing ...

=====

Final Register Report

Macro Statistics

# Registers	: 9
Flip-Flops	: 9

=====

=====

* Partition Report *

=====

Partition Implementation Status

No Partitions were found in this design.

=====

*

Final Report

*

=====

Final Results

RTL Top Level Output File Name : unishiftreg.ngr

Top Level Output File Name : unishiftreg

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

IOs : 13

Cell Usage :

BELS : 6

LUT2 : 2

LUT3 : 4

FlipFlops/Latches : 9

FD : 4

FDE : 5

Clock Buffers : 1

BUFGP : 1

IO Buffers : 8

IBUF : 3

OBUF : 5

=====

Device utilization summary:

Selected Device : 3s400pq208-5

Number of Slices:	5	out of	3584	0%
Number of Slice Flip Flops:	9	out of	7168	0%
Number of 4 input LUTs:	6	out of	7168	0%
Number of IOs:	13			
Number of bonded IOBs:	9	out of	141	6%
Number of GCLKs:	1	out of	8	12%

Partition Resource Summary:

No Partitions were found in this design.

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
clk	BUFGP	9

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Sped Grade: -5

Minimum period: 2.230ns (Maximum Frequency: 448.340MHz)

Minimum input arrival time before clock: 3.538ns

Maximum output required time after clock: 6.216ns

Maximum combinational path delay: No path found

Timing Detail:

All values displayed in nanoseconds (ns)

=====

Timing constraint: Default period analysis for Clock 'clk'

Clock period: 2.230ns (frequency: 448.340MHz)

Total number of paths / destination ports: 12 / 9

Delay: 2.230ns (Levels of Logic = 1)

Source: temp_3 (FF)

Destination: temp_2 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: temp_3 to temp_2

		Gate		Net
Cell:in->out	fanout	Delay	Delay	Logical Name (Net Name)

FD:C->Q	4	0.626	0.949	temp_3 (temp_3)
LUT3:I1->O	1	0.479	0.000	temp_mux0000<2>1 (temp_mux0000<2>)
FD:D		0.176		temp_2

Total 2.230ns (1.281ns logic, 0.949ns route)
(57.4% logic, 42.6% route)

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 15 / 9

Offset: 3.538ns (Levels of Logic = 2)

Source: sel<0> (PAD)

Destination: po_0 (FF)

Destination Clock: clk rising

Data Path: sel<0> to po_0

		Gate		Net
Cell:in->out	fanout	Delay	Delay	Logical Name (Net Name)
IBUF:I->O	2	0.715	1.040	sel_0_IBUF (sel_0_IBUF)
LUT2:I0->O	4	0.479	0.779	po_cmp_eq00001 (po_cmp_eq0000)
FDE:CE		0.524		po_0

Total 3.538ns (1.718ns logic, 1.820ns route)
(48.6% logic, 51.4% route)

=====
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 5 / 5

Offset: 6.216ns (Levels of Logic = 1)

Source: so (FF)

Destination: so (PAD)

Source Clock: clk rising

Data Path: so to so

		Gate		Net
Cell:in->out	fanout	Delay	Delay	Logical Name (Net Name)

FDE:C->Q	1	0.626	0.681	so (so_OBUF)
OBUF:I->O		4.909		so_OBUF (so)

Total		6.216ns (5.535ns logic, 0.681ns route)		
		(89.0% logic, 11.0% route)		

=====
Total REAL time to Xst completion: 4.00 secs

Total CPU time to Xst completion: 3.87 secs

-->

Total memory usage is 4493172 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 1 (0 filtered)

Number of infos : 0 (0 filtered)

- UCF FILE

NET "Clk" LOC = "P182";

NET "Rst" LOC = "P102";

NET "Mode(0)" LOC = "P93";

NET "Mode(1)" LOC = "P90";

NET "si" LOC = "P101";

NET "so" LOC = "p181";

NET "pin(0)" LOC = "P87";

NET "pin(1)" LOC = "P86";

NET "pin(2)" LOC = "P85";

NET "pin(3)" LOC = "P81";

NET "pin(4)" LOC = "P80";

NET "pin(5)" LOC = "P78";

NET "pin(6)" LOC = "P77";

NET "pin(7)" LOC = "P74";

NET "po(0)" LOC = "P162";

NET "po(1)" LOC = "P165";

NET "po(2)" LOC = "P166";

NET "po(3)" LOC = "P167";

NET "po(4)" LOC = "P168";

NET "po(5)" LOC = "P171";

NET "po(6)" LOC = "P172";

NET "po(7)" LOC = "P175";