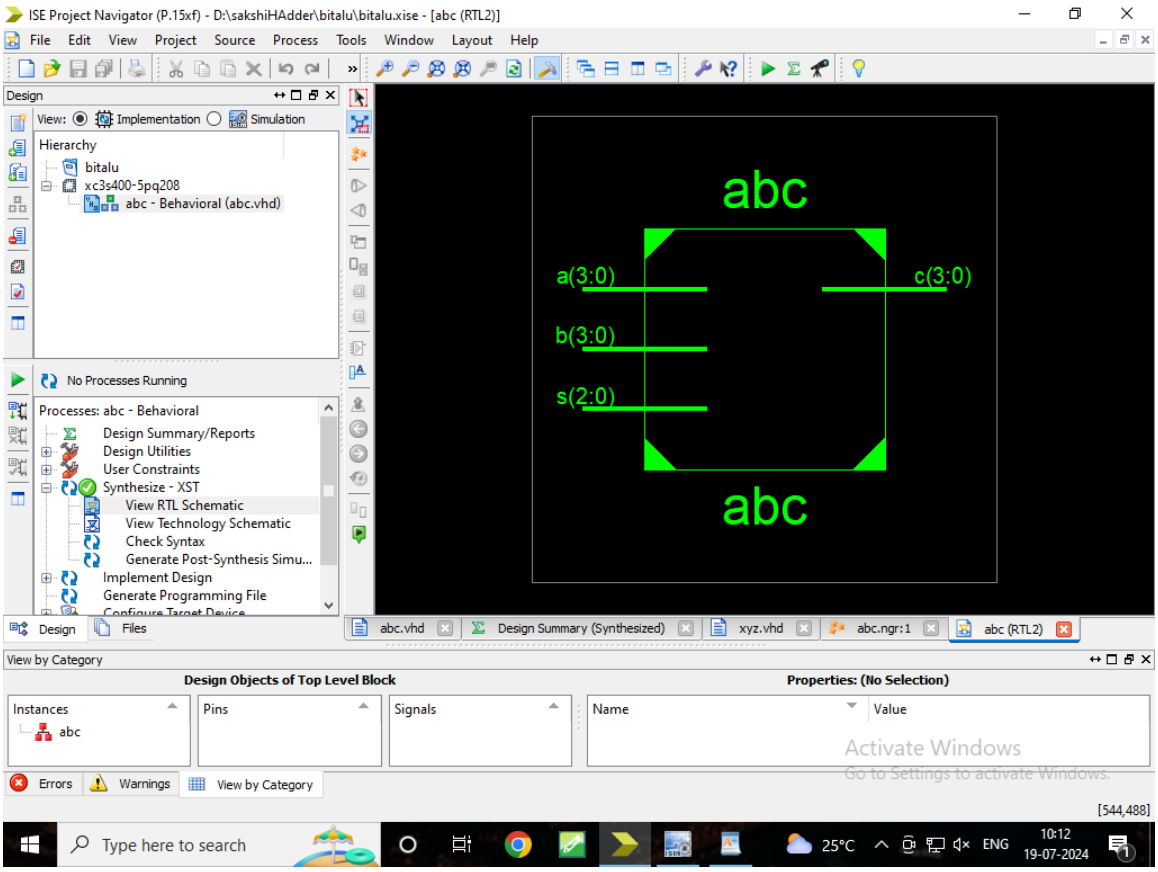
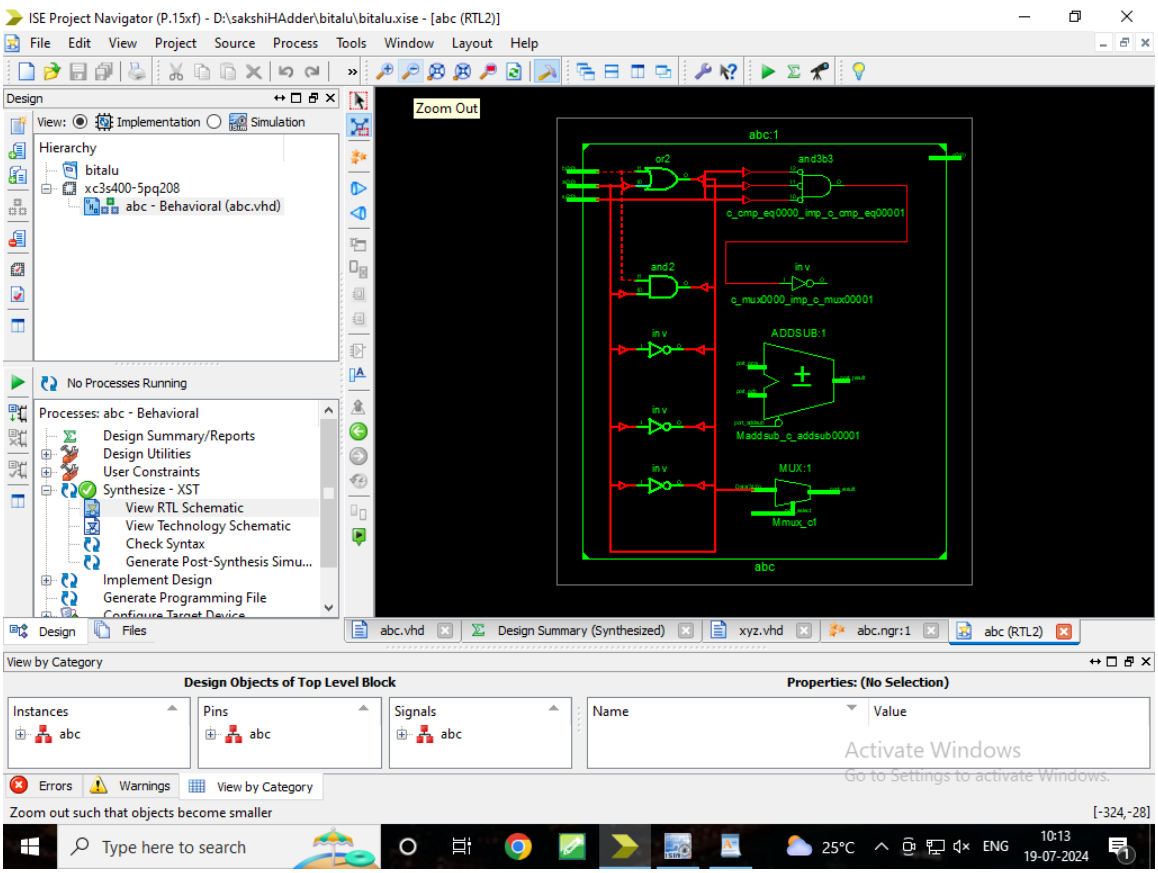
Name – Sujit Dhage Roll NO.=B43007

EXP 2 4-BIT ALU

```
ibrary IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;
use IEEE.STD_LOGIC_arith.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity abc is
	Port ( a : in    STD_LOGIC_VECTOR (3 downto 0);
		b : in    STD_LOGIC_VECTOR (3 downto 0);
		s : in    STD_LOGIC_VECTOR (2 downto 0);
		c : out    STD_LOGIC_VECTOR (3 downto 0));
end abc;
architecture Behavioral of abc is
begin
process (a,b,s)
begin
case s is
when "000" => c <=a+ b;
when "001" => c <=a - b;
when "010" => c <= a and b;
when "011" => c <= a or b;
```

```
when "100" => c <= a nand b;

when "101" => c <= a nor b;

when "110" => c <=    not a;

when "111" => c <= a;

when others => null;

end case;

end process;

end Behavioral;
```



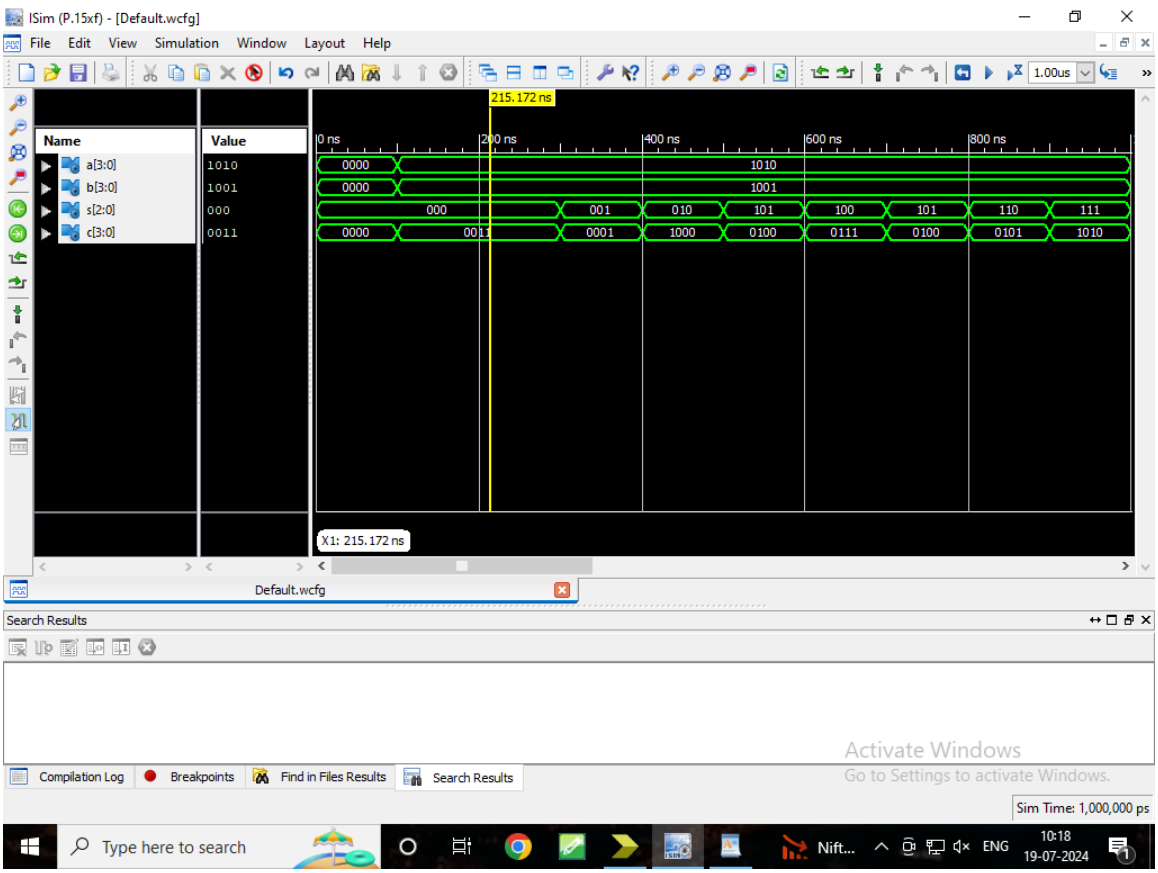



```
LIBRARY ieee;

USE ieee.std_logic_1164.ALL;

  -- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--USE ieee.numeric_std.ALL;


ENTITY xyz IS

END xyz;

  ARCHITECTURE behavior OF xyz IS


      -- Component Declaration for the Unit Under Test (UUT)


      COMPONENT abc
```

```
        PORT(
                a : IN    std_logic_vector(3 downto 0);
                b : IN    std_logic_vector(3 downto 0);
                s : IN    std_logic_vector(2 downto 0);
                c : OUT    std_logic_vector(3 downto 0));
END COMPONENT;
   --Inputs
     signal a : std_logic_vector(3 downto 0) := (others => '0');
     signal b : std_logic_vector(3 downto 0) := (others => '0');
     signal s : std_logic_vector(2 downto 0) := (others => '0');
--Outputs
       signal c : std_logic_vector(3 downto 0);
     -- No clocks detected in port list. Replace <clock> below with
     -- appropriate port name
 ---constant <clock>_period : time := 10 ns;
 BEGIN

          -- Instantiate the Unit Under Test (UUT)
     uut: abc PORT MAP (
                a => a,
                b => b,
                s => s,
                c => c      );
 -- Clock process definitions
--      <clock>_process :process
--      begin
--                      <clock> <= '0';
--                      wait for <clock>_period/2;
--                      <clock> <= '1';
```

```
--                      wait for <clock>_period/2;
--      end process;
    -- Stimulus process
      stim_proc: process
      begin
           -- hold reset state for 100 ns.
           wait for 100 ns;
a<="1010";
  b<="1001";
s<="000";
wait for 100 ns;

  a<="1010";
b<="1001";
s<="000";
  wait for 100 ns;
  a<="1010";
b<="1001";
s<="001";
  wait for 100 ns;
  a<="1010";
b<="1001";
s<="010";
  wait for 100 ns;
  a<="1010";
b<="1001";
s<="101";
  wait for 100 ns;
  a<="1010";
```

```
b<="1001";
s<="100";
  wait for 100 ns;
  a<="1010";
b<="1001";
s<="101";
  wait for 100 ns;
  a<="1010";
b<="1001";
s<="110";
  wait for 100 ns;
  a<="1010";
b<="1001";
s<="111";
  wait for 100 ns;
        --- wait for <clock>_period*10;
  -- insert stimulus here
wait;
end process;
END;
```



net a(3) loc=p96;

net a(2) loc=p97;

net a(1) loc=p100;

net a(0) loc=p101;

net b(3) loc=p90;

net b(2) loc=p93;

net b(1) loc=p94;

net b(0) loc=p95;

net s(2) loc=p85;

net s(1) loc=p86;

net s(0) loc=p87;

net c(3) loc=p167;

net c(2) loc=p166;

net c(1) loc=p165

net c(0) loc=p162;

Release 14.1 - xst P.15xf (nt64)

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.09 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.09 secs

--> Reading design: abc.prj

TABLE OF CONTENTS

```
=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "abc.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "abc"
Output Format                      : NGC
Target Device                      : xc3s400-5-pq208

---- Source Options
Top Module Name                    : abc
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Mux Style                          : Auto
Decoder Extraction                 : YES
Priority Encoder Extraction        : Yes
Shift Register Extraction          : YES
Logical Shifter Extraction         : YES
XOR Collapsing                     : YES
ROM Style                          : Auto
```

Mux Extraction : Yes

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : Auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 8

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Keep Hierarchy : No

Netlist Hierarchy : As Optimized

RTL Output : Yes

Global Optimization : All Clock Nets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

===

===

* HDL Compilation *

===

Compiling vhdl file "D:/sakshiHAdder/bitalu/abc.vhd" in Library work.

Entity <abc> compiled.

Entity <abc> (Architecture <behavioral>) compiled.

===

* Design Hierarchy Analysis *

===

Analyzing hierarchy for entity <abc> in library <work> (architecture <behavioral>).

===

* HDL Analysis *

===

Analyzing Entity <abc> in library <work> (Architecture <behavioral>).

Entity <abc> analyzed. Unit <abc> generated.

===

* HDL Synthesis *

===

Performing bidirectional port resolution...

Synthesizing Unit <abc>.

Related source file is "D:/sakshiHAdder/bitalu/abc.vhd".

Found 4-bit 8-to-1 multiplexer for signal <c>.

Found 4-bit addsub for signal <c$addsub0000>.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 4 Multiplexer(s).

Unit <abc> synthesized.

INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic operations in this design can share the same physical resources for reduced device utilization. For improved clock frequency you may try to disable resource sharing.

===

HDL Synthesis Report

Macro Statistics

Adders/Subtractors : 1

4-bit addsub : 1

Multiplexers : 1

4-bit 8-to-1 multiplexer : 1

===

===

* Advanced HDL Synthesis *

===

===

Advanced HDL Synthesis Report

Macro Statistics

Adders/Subtractors : 1

4-bit addsub : 1

Multiplexers : 1

4-bit 8-to-1 multiplexer : 1

===

```
=========================================================================
*                          Low Level Synthesis                          *
=========================================================================
Optimizing unit <abc> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block abc, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Found no macro

=========================================================================

=========================================================================
*                          Partition Report
*=========================================================================

Partition Implementation Status

-------------------------------

  No Partitions were found in this design.

-------------------------------

=========================================================================
*                          Final Report                                 *
=========================================================================
Final Results

RTL Top Level Output File Name          : abc.ngr

Top Level Output File Name              : abc

Output Format                           : NGC

Optimization Goal                       : Speed

Keep Hierarchy                          : No

Design Statistics

# IOs                                   : 15
```

Cell Usage :

BELS : 34

LUT2 : 5

LUT3 : 10

LUT4 : 6

MUXF5 : 9

MUXF6 : 4

IO Buffers : 15

IBUF : 11

OBUF : 4

===

Device utilization summary:

Selected Device : 3s400pq208-5

Number of Slices: 11 out of 3584 0%

Number of 4 input LUTs: 21 out of 7168 0%

Number of IOs: 15

Number of bonded IOBs: 15 out of 141 10%

Partition Resource Summary:

No Partitions were found in this design.

===

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -5

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 12.624ns

Timing Detail:

All values displayed in nanoseconds (ns)

==========

Timing constraint: Default path analysis

Total number of paths / destination ports: 87 / 4

Delay: 12.624ns (Levels of Logic = 8)

Source: s<0> (PAD)

Destination: c<3> (PAD)

Data Path: s<0> to c<3>

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	14	0.715	1.179	s_0_IBUF (s_0_IBUF)
LUT3:I1->O	3	0.479	0.771	c_mux00001 (c_mux00001)

MUXF5:S->O 2 0.540 1.040 Maddsub_c_addsub0000_cy<1>1_f5 (Maddsub_c_addsub0000_cy<1>)

LUT4:I0->O 1 0.479 0.740 Maddsub_c_addsub0000_xor<3>11_SW0 (N2)

LUT3:I2->O 1 0.479 0.000 Maddsub_c_addsub0000_xor<3>11 (c_addsub0000<3>)

MUXF5:I0->O 1 0.314 0.000 Mmux_c_4_f5_2 (Mmux_c_4_f53)

MUXF6:I0->O 1 0.298 0.681 Mmux_c_2_f6_2 (c_3_OBUF)

OBUF:I->O 4.909 c_3_OBUF (c<3>)

Total 12.624ns (8.213ns logic, 4.411ns route)

(65.1% logic, 34.9% route)

==========

Total REAL time to Xst completion: 4.00 secs

Total CPU time to Xst completion: 4.22 secs

-->

Total memory usage is 4493160 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 1 (0 filtered)