**FIFO**

library IEEE; use IEEE.STD\_LOGIC\_1164.ALL; use IEEE.STD\_LOGIC\_ARITH.ALL; use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating ---- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity FIFO is

|  |  |
| --- | --- |
| Port ( DI : in std\_logic\_vector(3 | downto 0); |
| DO : out std\_logic\_vector(3 | downto 0); |

RW : in std\_logic; FULL : out std\_logic; RS : in std\_logic; CLK : in std\_logic); end FIFO;

architecture Behavioral of FIFO is

begin

process(RS,CLK)

type memory is Array( 0 to

variablemem: memory;

|  |  |  |
| --- | --- | --- |
| variable r\_p:integer range 0 variable w\_p:integer range 0 variable overwrite :boolean; | to to | 3;3; |

begin if RS='1' then DO<="0000";

elsif(CLK'event and CLK='1') then if RW='1'then

if (overwrite=False OR w\_p/=r\_p) then mem (w\_p):=DI;

ifw\_p=3 then w\_p:=0 ; else

w\_p:=w\_p+1; overwrite:=False;

elseif RW='0' then

(overwrite=False OR w\_p/=r\_p) then

if (r\_p=3 ) then r\_p:=0 ;

of std\_logic\_vector(3 downto 0);

end if;

if DO<=mem(r\_p);

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to 3 )

overwrite:=true; else

r\_p:=r\_p+1;

end if; end if;

end if;

if

if overwrite=true then FULL<='1';

else

FULL<='0';

end if;

else FULL<='0';

end if;

end if; end process;

end Behavioral;

ENTITY SSSA\_vhd IS END SSSA\_vhd;

ARCHITECTURE behavior OF SSSA\_vhd IS

-- Component Declaration for the Unit Under Test (UUT) COMPONENT fifo

PORT(

DI : IN std\_logic\_vector(3 downto 0); RW : IN std\_logic;

RS : IN std\_logic; CLK : IN std\_logic;

DO : OUT std\_logic\_vector(3 downto 0);

FULL : OUT std\_logic );

END COMPONENT;

--Inputs

SIGNAL RS :std\_logic := '0';

SIGNAL CLK :std\_logic := '0';

SIGNAL DI :std\_logic\_vector(3 downto 0) := (others=>'0');

--Outputs

SIGNAL DO :std\_logic\_vector(3 downto 0); SIGNAL FULL :std\_logic;

constant

w\_p=r\_p then

CLK\_period : time := 10 ns;

SIGNAL RW :std\_logic := '0';

-

BEGIN

-- Instantiate the Unit Under Test (UUT) uut: fifo PORT MAP(

DI => DI,

DO => DO, RW => RW, FULL => FULL, RS => RS, CLK => CLK

); process begin

|  |  |
| --- | --- |
| CLK<='0' wait for CLK\_period/2; | ; |

CLK<='1'

wait for CLK\_period/2; end process;

tb : PROCESS BEGIN

RS<='1'; wait for 100 ns; RS<='0'; RW<='1'; DI<="0011";

-- Wait 100 ns for global reset to finish wait for 10 ns;

RW<='1'; DI<="0110";

-- Wait 100 ns for global reset to finish wait for 10 ns;

DI<="1100";

-- Wait 100 ns for global reset to finish wait for 10 ns;

RW<='1'; DI<="1001";

-- Wait 100 ns for global reset to finish wait for 10 ns;

-- Place stimulus here

RW<='0';

-- Wait 100 ns for global reset to finish wait for 10 ns;

RW<='0';

-- Wait 100 ns for global reset to finish wait for 10 ns;

RW<='0';

-- Wait 100 ns for global reset to finish wait for 10 ns;

WAIT FOR CLK\_period\*10;

wait; **-- will wait forever** END PROCESS;

END;

RW<='1';

A screenshot of a computer

Description automatically generated

A computer screen shot of a diagram

Description automatically generated

A screenshot of a computer

Description automatically generated

=========================================================================

\* Final Report \*

=========================================================================

Final Results

RTL Top Level Output File Name : fifo.ngr

Keep Hierarchy : NO

Design Statistics

# IOs : 12

Cell Usage :

# BELS : 2

# GND : 1

# VCC : 1

# FlipFlops/Latches : 26

# FDCE : 4

# FDE : 22

========================================================================= CPU : 5.92 / 8.26 s | Elapsed : 6.00 / 8.00 s

-->

Total memory usage is 122500 kilobytes

Number of errors : 0 ( 0 filtered) Number of warnings : 0 ( 0 filtered)

Number of infos : 0 ( 0 filtered)