# Resumé

## 1. PERSONAL INFORMATION

| Last (Family) Name | First | Middle | Prefix |
|---|---|---|---|
| NANDY | SOUMITRA | KUMAR | PROFESSOR |

Organization's Name

Indian Institute of Science, Bangalore 560012 INDIA – (an Indian Institution of Eminence)

Preferred Mailing Address

Department of Computational and Data Sciences, Indian Institute of Science, Bangalore 560012 INDIA

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| Bangalore | Karnataka | 560012 | INDIA |

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## 2. EDUCATION

| Degrees | Year | Educational Institution | Location |
|---|---|---|---|
| PhD, CSA | 1989 | Indian Institute of Science, Bangalore | INDIA |
| MSc (Engg.), CSA | 1987 | Indian Institute of Science, Bangalore | INDIA |
| B.E (Hons), ECE | 1980 | Indian Institute of Science, Bangalore | INDIA |
| BSc. (Hons), Physics | 1977 | Indian Institute of Technology, Kharagpur | INDIA |

## 3. PROFESSIONAL HISTORY

| From (year) to (year) | Name of Company | Position Held |
|---|---|---|
| **Aug 09 -- date** | Indian Institute of Science, Bangalore | Senior Professor (HAG) |
| **Jan 03 -- July 09** | Indian Institute of Science, Bangalore | Professor |
| **Jun 97--Dec 02**: | Indian Institute of Science, Bangalore | Associate Professor |
| **Jun 91--May 97**: | Indian Institute of Science, Bangalore | Assistant Professor |
| **Mar 90--Jun 91**: | Indian Institute of Science, Bangalore | Sr. Scientific Officer(II) |
| **Sept 87--Mar 90**: | Indian Institute of Science, Bangalore | Sr. Scientific Officer (I) |
| **Oct 82--Aug 87**: | Indian Institute of Science. Bangalore | Scientific Officer |
| **May 80--Oct 82**: | M/S. ORG Systems, Bangalore | Computer Engineer |

Prof. S. K. Nandy was instrumental in initiating research in LSI System Design at the Indian Institute of Science. He worked towards setting up a State-of-the-art laboratory for Computer Aided Design at the institute in 1983 with the assistance of the United Nations Development Programme and the Government of India. This laboratory has active collaborations with Massachusetts Institute of Technology, Cambridge, USA, Technical University of Delft, The Netherlands, Leiden Institute of Advanced Computer Science, The Netherlands, Tokyo University and Waseda University, Japan, KTH Royal Institute of Technology, Sweden, and RWTH Aachen University, Germany. Today, the laboratory is engaged in state-of-the-art research in Embedded Reconfigurable System on Chip architectures for next generation high performance computing on the edge and core.

Prof. Nandy is a Senior Professor in the Department of Computational and Data Sciences. Over the years, he has graduated 28 PhDs, 16 MSc.(Engg.) and over 100 Master's students who have worked for their theses in the laboratory. He has another 8 PhDs in progress. His current research addresses important issues in micro-architectural and compiler optimizations for power and performance in Chip Multiprocessors (CMPs) and Runtime Reconfigurable System on Chips (MP-SoCs). All his research target massively parallel architectures/platforms for accelerating computations for Next Generation Sequence Alignment, Numerical Linear Algebra, Real-time Face Recognition, Cognition Engines, and Molecular Dynamics. Prof. Nandy has over 180 research publications in International Journals and Proceedings of International Conferences that highlight his research contributions.

Prof. Nandy has brought in large research contracts/grants from leading industry such as Intel, Hewlett Packard, Philips Research, STMicroelectronics, Texas Instruments, Sun Microsystems, Boeing, and SAFRAN to carry out research in micro-architecture design, memory hierarchy design in CMPs and MP-SoCs, runtime reconfigurable architectures, and SoC platforms. He works closely with DRDO laboratories on projects of national interests.

Prof. Nandy is the founder of a technology incubation company Morphing Machines, Pvt. Ltd (URL: www.morphing.in) set up in partnership with the Indian Institute of Science. He holds the position of Honorary Chief Scientist at Morphing Machines. He co-founded ReneLife (URL: www.renelife.co.in), along with Prof. Debnath Pal, under the faculty entrepreneurship programme of the institute. ReneLife in engaged in developing hardware-software co-designed accelerated solutions for next generation sequencing for Life Sciences applications.

Prof. Nandy is a senior member of the IEEE. He has served as a member of Programme Committee of several IEEE International conferences, viz. ASP-DAC, HiPC, VLSI Design, DAC, SAMOS. He is a member of the faculty selection committee of the Indian Institute of Science, and other institutions in the country, and a consultant to numerous industries in the area of VLSI Design and Embedded Systems. He has been an examiner for several PhD theses from IITs, and other leading institutions within and outside the country.

## 4. PUBLICATIONS

**Journal Publications:**

1. Oscar Ferraz , Srinivasan Subramaniyan, Ramesh Chinthalaa, Joao Andrade, Joseph R. Cavallaro, Soumitra K. Nandy, Vitor Silva , Xinmiao Zhang, Madhura Purnaprajna , and Gabriel Falcao, **"A Survey on High-Throughput Non-Binary LDPC Decoders: ASIC, FPGA, and GPU Architectures"**, IEEE Communications Surveys & Tutorials, Volume: 24, Issue: 1, pp. 524 – 556, 2022

2. Farhad Merchant, Tarun Vatwani, Anupam Chattopadhyay, Soumyendu Raha, and S.K.Nandy, **"Efficient Realization of Householder Transform through Algorithm-Architecture Co-design for Acceleration of QR Factorization"**, IEEE Transactions on Parallel and Distributed Systems, February 2018.

3. Mohammadi, Mahnaz; Krishna, Akhil; S, Nalesh; Nandy, S, **"A Hardware Architecture for Radial Basis Function Neural Network Classifier"**, IEEE Transactions on Parallel and Distributed Systems, November 2017.

4. Farhad Merchant, Anupam Chattopadhyay, Soumyendu Raha, S.K.Nandy, and Ranjani Narayan, **"Accelerating BLAS and LAPACK via Efficient Floating Point Architecture Design"**, Parallel Processing Letters, World Scientific Publishing Company, September 2017.

5. Nalesh S, Kavitha Madhu, Saptarsi Das, S.K.Nandy, and Ranjani Narayan, **" Energy Aware Synthesis of Application Kernels through Composition of Data-paths on a CGRA"**, Integration, The VLSI journal, Elsevier, 2017.

6. Gopinath Mahale, Hamsika Mahale, S.K.Nandy, and Ranjani Narayan, **"REFRESH: REDEFINE for Face Recognition using SURE Homogeneous Cores"**, IEEE Transactions on Parallel and Distributed Systems, Vol. 27, pp. 3602-3616, 2016.

7. Arnab Biswas, and S. K. Nandy, **"Role based shared memory access control mechanisms in NoC based MP-SoC"**, Nano Communication Networks, March 2016, Elsevier.

8. Arnab Biswas, S. K. Nandy, and Ranjani Narayan, **"Router Attack towards NoC enabled MPSoC and Monitoring Countermeasures Against Such Threat"**, Circuits, Systems, and Signal Processing (CSSP): Volume 34, Issue 10 (2015), Page 3241-3290, Springer

9. Kala. S, Nalesh. S, S. K. Nandy, and Ranjani Narayan, **"Scalable and Energy Efficient, Dynamically Reconfigurable FFT Architecture"**, Journal of Low Power Electronics, Vol. 11, No. 3, September 2015, American Scientific Publishers

10. Saptarsi Das, Kavitha Madhu, Madhav Krishna, Nalesh S, Farhad Merchant, Adithya Pulli, S. K. Nandy, and Ranjani Narayan, **"A framework for post-silicon realization of arbitrary instruction extensions on reconfigurable data-paths"**, Journal of Systems Architecture, Elsevier, July 2014

11. Saptarsi Das, Ranjani Narayan, Soumitra Kumar Nandy, **"Accelerating Reduction for Enabling Fast Multiplication over Large Binary Fields",** Book Title: E-Business and Telecommunications, Book Subtitle: International Joint Conference, ICETE 2011, Seville, Spain, July 18-21, 2011, Revised Selected Papers, and Communications in Computer and Information Science Volume 314, 2012, pp 249-263 Springer.

12. Ganesh Garga, Saptarsi Das, S. K. Nandy, Ranjani Narayan, Chandan Haldar, Maheshkumar P. Jagtap, and Siba Prasad Dash "**A Flexible Crypto-system Based upon the REDEFINE Polymorphic ASIC Architecture",** Defence Science Journal, Vol. 62, No. 1, January 2012, pp. 30-36.

13. H. Sarojadevi and S. K. Nandy, "**Processor-Directed Cache Coherence Mechanism – A Performance Study",** International Journal on Computer Science and Engineering (IJCSE), Vol. 3 (2011) No. 9, pp. 3202-3206.

14. Ratna Krishnamoorthy, Saptarsi Das, Keshavan Varadarajan, Mythri Alle, Masahiro Fujita, S K Nandy and Ranjani Narayan, "**Data Flow Graph Partitioning Algorithms and Their Evaluations for Optimal Spatio-temporal Computation on a Coarse Grain Reconfigurable Architecture",** IPSJ Transactions on System LSI Design Methodology, Vol. 4 (2011) pp.193-209.

15. Gaurav Kumar Singh, Mythri Alle, Keshavan Varadarajan, S. K. Nandy and Ranjani Narayan, **"A Generic Graph-Oriented Mapping Strategy for a Honeycomb Topology", (**proceedings of the International Conference on Futuristic Computer Applications), International Journal of Computer Applications 1(21):91–98, February 2010.

16. Mythri Alle, Keshavan Varadarajan, Alexander Fell, Ramesh Reddy C, NimmyJoseph, Saptarsi Das, Prasenjit Biswas, Jugantor Chetia, Adarsh Rao, S K Nandy, and Ranjani Narayan, **"REDEFINE: Runtime Reconfigurable Polymorphic ASIC",** ACM Transactions on Embedded Computing Systems, Vol. 9, No. 2, Article 11, Publication date: September 2009.

17. Subhasis Banerjee, G. Surendra and S. K. Nandy, **"On the Effectiveness of Phase Based Regression Models to trade Power and Performance using Dynamic Processor Adaptation"**, Journal of Systems Architecture : the EUROMICRO journal, Vol. 54 , No. 8, 2008, pp. 797-815.

18. G. Surendra, S. Banerjee and S. K. Nandy, ``**Instruction Reuse in Spec, Media and Packet Processing Benchmarks - A Comparative Study of Power, Performance and Related Microarchitectural Optimizations''**, Special issue of the Journal of Embedded Computing on "Performance Analysis, Resource Optimization, Methodology and high level design tools for Embedded Systems", Vol. 2, No. 1, 2006, pp. 15-34.

19. H. Saroja Devi, S. K. Nandy, S. Balakrishnan, ``**On the Correctness of Program Execution when Cache Coherence is maintained Locally at Data Sharing Boundaries in Distributed Shared Memory Multiprocessors**'', International Journal of Parallel Programming, Vol. 32, No. 5, October 2004.

20. G. Surendra, S. Banerjee and S. K. Nandy, ``**On the Effectiveness of Flow Aggregation in Improving Instruction Reuse in Network Processing Applications''**, International Journal of Parallel Programming, Vol. 31, No. 6, December 2003, pp. 469-487.

21. Abhijit Lele, S K Nandy and D H J Epema, `` **Harmony- An Architecture for Providing Quality of Service in Mobile Computing Environments"**, Special Issue of the Journal of Interconnection Connection Networks (JOIN) on Mobile Computing, Vol. 1, No. 3(2000), pp. 217-266, World Scientific Publications.

22. S. Ramanathan, S. K. Nandy and V. Visvanathan, ``**Reconfigurable Filter Coprocessor Architecture for DSP Applications"**, The Journal of VLSI Signal Processing, Vol. 26, No. 3, October 2000, Kluwer Academic Publishers.

23. S. Ramanathan, V. Visvanathan and S. K. Nandy, ``**A Computational Engine for Multirate FIR Digital Filtering''**, Signal Processing, Vol. 79, No. 2, December 1999, Elsevier Science.

24. S. Ramanathan, V. Visvanathan and S. K. Nandy, ``**Synthesis of ASIPs for DSP Algorithms"**, INTEGRATION, the VLSI Journal, Vol. 28, No. 1, pp. 13-32, September 1999, Elesevier Science.

25. S. Ramanathan, V. Visvanathan and S. K. Nandy, ``**Architectural Synthesis of Computational Engines for Subband Adaptive Filtering"**, The Journal of VLSI Signal Processing - Systems for Signal, Image and Video Technology, Vol. 22, No. 3, pp. 173-195, September 1999, Kluwer Academic Publishers.

26. Vinod Menezes, S. K. Nandy, and Biswadip Mitra, ``**Signal Compression through Spatial Frequency based Motion Estimation"**, INTEGRATION, the VLSI journal, No. 22, 1997, Elsevier Science Publishers, pp. 115-135.

27. Debabrata Ghosh and S. K. Nandy**, ``Design and Realization of High Performance Wave-Pipelined 8 X 8-bit Multiplier in CMOS Technology"**, IEEE transactions on Very Large Scale Integration (VLSI) Systems, Vol. 3, No. 1, March 1995, pp. 36-48.

28. S. K. Nandy, ``**Geometrical Design Rule Check of VLSI layouts in Distributed Computing Environment"**, International Journal of Computer Aided VLSI Design: An International Journal of Custom-Chip Design, Simulation and Testing, Vol. 1, No. 2, 1994, Gordon and Breach Science Publishers pp. 127-154.

29. S. K. Nandy and R. B. Panwar, ``**Geometric Design Rule Check of VLSI layouts in Mesh Connected Processors"**, International Journal of Computer Aided VLSI Design: An International Journal of Custom-Chip Design, Simulation and Testing, Vol. 1, No. 2, 1994, Gordon and Breach Science Publishers, pp. 135-167.

30. Debabrata Ghosh and S. K. Nandy**, ``A 600-MHz Halfbit Level Pipelined Accumulator-Interleaved Multiplier Accumulator Core"**, VLSI SIGNAL PROCESSING VI, IEEE Signal Processing Society, pp. 498-506, 1993.

31. S. Balakrishnan and S. K. Nandy, ``**Quasi Dynamic Approach to Layout Compaction"**, Microprocessing and Microprogramming, Vol. 30, 1990, pp. 231-236 (North Holland Publications).

32. C. E. Prakash and S. K. Nandy, ``**VOXEL based Modeling and Rendering Irregular Solids"**, Microprocessing and Microprogramming, Vol. 30, 1990, pp. 341-346 (North Holland Publications).

33. S. K. Nandy, C. Sudha Madhuri, Anuradha. D, and Rajat Moona, ``**K-d tree based Gridless Maze Routing on Message Passing Multiprocessor System"**, Journal of the IETE (special issue on microelectronics), Vol. 36, Nos. 3 & 4, 1990.

34. G. Vidyamurthy and S. K. Nandy, ``**On the Reconfigurability of Hardware Accelerators for VLSI CAD tools"**, Journal of the IETE (special issue on microelectronics) Vol. 36, Nos. 3 & 4, 1990.

35. S. K. Nandy and L. M. Patnaik, ``**Algorithms for Incremental Compaction of Geometrical Layouts"**, Computer-Aided Design, Butterworth and Co. (Publishers) Ltd., Vol. 19, No.5, June 1987, pp. 257-265.

36. S. K. Nandy and L. M. Patnaik, ``**Linear Time Geometrical Design Rule Checker based on Quadtree representation of VLSI Mask Layouts"**, Computer-Aided Design, Butterworth & Co. (Publishers) Ltd., Vol. 18, No. 7, September 1986, pp. 380-388.

37. S. K. Nandy and L. M. Patnaik, ``**A Study of Placement Algorithms through Trial Interchange of Logic Modules"**, Computers-Aided Design, Butterworth & Co. (Publishers) Ltd., Vol. 17, No. 5, June 1985, pp 211-214.

**Refereed Conferences and Workshop Publications**

1. Ritika Singh, Shashank Vijaya Ranga, Swarali Patil, Madhava Krishna, Mitsu Mehta, Anoop Mysore Nataraja, S. K. Nandy, Ranjani Narayan, Chandan Haldar, François Neumann, Philippe Baufreton, "**Micro-Architectural support for High Availability of NoC based MP-SoC",** proceedings of the 38th IEEE/AIAA Digital Avionics Systems Conference, San Diego, USA, 2019.

2. Farhad Merchant, Tarun Vatwani, Anupam Chattopadhyay, Soumyendu Raha, S. K. Nandy and Ranjani Narayan, **"Achieving Efficient Realization of Kalman Filter on CGRA through Algorithm-Architecture Co-design",** 14th International Symposium on Applied Reconfigurable Computing (ARC 2018), 2-4 May 2018, Santorini, Greece.

3. Santhi Natarajan, Krishnakumar N, Debnath Pal and S. K. Nandy, **" ReneGENE-GI: Empowering Precision Genomics with FPGAs on HPCs",** 14th International Symposium on Applied Reconfigurable Computing (ARC 2018), 2-4 May 2018, Santorini, Greece.

4. Santhi Natarajan, Krishnakumar N, Anuchan H.V, Debnath Pal and S. K. Nandy, **" ReneGENE-Novo: Co-designed Algorithm-Architecture for Accelerated Preprocessing and Assembly of Genomic Short Reads",** 14th International Symposium on Applied Reconfigurable Computing (ARC 2018), 2-4 May 2018, Santorini, Greece.

5. Louis Sutter, Thanakorn Khamvilai, Philippe Monmousseau, John B. Mains, Eric Feron, Philippe Baufreton, Francois Neumann, Madhava Krishna, S. K. Nandy, Ranjani Narayan, Chandan Haldar, **"Experimental Allocation of Safety-Critical Applications on Reconfigurable Multi-Core Architecture"**, proceedings of the 37th IEEE/AIAA Digital Avionics Systems Conference, London, UK, 2018.

6. Ipsita Biswas Mahapatra, S K Nandy, Utkarsh Agarwal and Chandrashekhar Azad, **" Design space exploration of an execution-driven functional-simulation methodology",** proceedings of the 31st International Conference on VLSI Design, January 8-10, 2018 Pune, India.

7. Tom Guillaumet, Eric Feron, Philippe Baufreton,Francois Neumann,Kavitha Madhu, Madhava Krishna, S K Nandy, Chandan Haldar, Ranjani Narayan, **"Task allocation of safety-critical applications on reconfigurable multi-core architectures"**, proceedings of the 36th IEEE/AIAA Digital Avionics Systems Conference, St. Petersburg, Florida, USA, 2017.

8. Kavitha Madhu, Tarun Singla, S K Nandy, Ranjani Narayan, Philippe Beaufreton, François Neumann, **"REDEFINE - case for WCET friendly hardwar acceerators for real time applications",** International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES 2017), Seoul, South Korea.

9. Santhi Natarajan, Krishna Kumar N, Debnath Pal and S. K. Nandy, **" AccuRA: Accurate Alignment of Short Reads on Scalable Reconfigurable Accelerators",** proceedings of SAMOS XVI 2016, July 18-21, 2016, Samos, Greece.

10. Kavitha Madhu, Anuj Rao, Saptarsi Das, Madhava Krishna, S. K. Nandy, Ranjani Narayan, Anup Kini, Makesh Tarun, Preetam Shivaram, Nalesh S, **"Flexible Resource Allocation and Management for Application Graphs on ReNÉ MPSoC"**, Proceedings of 7th PARMA-DITAM workshop, co-located with HiPEAC 2016, 2016, Prague.

11. Saptarsi Das, Nalesh S, Kavitha Madhu, S. K. Nandy, Ranjani Narayan, **"RHyMe: REDEFINE HyperCell Multicore for Accelerating HPC Kernels"**, 29th International Conference on VLSI Design, 2016.

12. Ashish Pradhan and S.K.Nandy, **" An Energy Efficient Dynamically Reconfigurable QR Decomposition for Wireless MIMO Communication"**, Proceedings of the IEEE VLSI Design 2016, Bangalore, India, Jan 4-7, 2016.

13. Farhad Merchant, Nimash Choudhary, S K Nandy, Ranjani Narayan, **"Efficient Realization of Table Look-up based Double Precision Floating Point Arithmetic"**, Proceedings of the IEEE VLSI Design 2016, Bangalore, India, Jan 4-7, 2016.

14. Gopinath Mahale, Eshan Bhatia, S.K. Nandy, Ranjani Narayan, **" VOP: Architecture of a Processor for Vector Operations in On-line Learning of Neural Networks"**, Proceedings of the IEEE VLSI Design 2016, Bangalore, India, Jan 4-7, 2016.

15. Farhad Merchant, Tarun Vatwani, Anupam Chattopadhyay, Soumyendu Raha, S K Nandy, Ranjani Narayan, **"Achieving Efficient QR Factorization by Algorithm-Architecture Co-Design of Householder Transformation"**, Proceedings of the IEEE VLSI Design 2016, Bangalore, India, Jan 4-7, 2016.

16. Mahnaz Mohammadi, Rohit Ronge, S. K. Nandy, **"Performance Evaluation of Feed-Forward Backpropagation Neural Network for Classification on A Reconfigurable Hardware Architecture"**, 12th International Symposium on Applied Reconfigurable Computing, Rio de Janeiro, Brazil, March 2016

17. Nalesh S, Saptarsi Das, Kavitha Madhu, S. K. Nandy, **"Energy Aware Synthesis of Application Kernels expressed in Functional Languages on a Coarse Grained Composable Reconfigurable Array"**, Proceedings of the IEEE International Symposium on Nanoelectronic and Information Systems 2015, Indore.

18. Madhava Krishna , Nalesh S , Kavitha T Madhu , Saptarsi Das , Chandan Haldar, Ranjani Narayan, and S K Nandy, **"ReN´E: Combating Dark Silicon in Polymorphic Massively Parallel Processing Cores",** ICCAD 2015 Conference for Workshop on Efficient Computing in the Dark Silicon Era**,** ICCAD 2015 Conference for Workshop on Efficient Computing in the Dark Silicon Era, Austin, Texas, USA, Nov 5, 2015.

19. Nalesh S, Kavitha T Madhu**,** Saptarsi Das, S. K. Nandy and Ranjani Narayan**, "Composition of Data-paths on a CGRA for Energy Aware Synthesis of Functionally Specified Application Kernels"",** ICCAD 2015 Conference for Workshop on Efficient Computing in the Dark Silicon Era, Austin, Texas, USA, Nov 5, 2015.

20. Alexander Fell, S K Nandy and Ranjani Narayan, **" A Deterministic, Minimal Routing Algorithm for a Toroidal, Rectangular Honeycomb Topology Using a 2-tupled Relative Address"**, proceedings of the 28th IEEE International System on Chip Conference, Beijing, China, September 8-11, 2015.

21. Mahnaz Mohammadi, Rohit Ronge, Jayesh Ramesh Chandiramani, and Soumitra Nandy, **" An Accelerator for Classification using Radial BasisFunction Neural Network"**, proceedings of the 28th IEEE International System on Chip Conference, Beijing, China, September 8-11, 2015.

22. Ipsita Biswas Mahapatra, Santhi Natarajan, Nalesh S, S. K. Nandy, **"SIMAAH: RTL simulation accelerator for complex SoC's"**, Procedings of the IEEE International Conference on Electronics, Computing and Communication Technologies, 2015.

23. Kavitha T Madhu, Saptarsi Das, Nalesh S., S. K. Nandy and Ranjani Narayan, **" Compiling HPC kernels for the REDEFINE CGRA"**, proceedings of the 17th International Conference on High Performance Computing and Communications (HPCC 2015), New York, August 24-26, 2015.

24. Ramesh Chinthala, Amitava Datta, S. K. Nandy, **" Exploration of Cache Line Size for Sawtooth Compressed Row Storage based SpMV Multiplication"**, proceedings of the 13th Australasian Symposium on Parallel and Distributed Computing (AusPDC 2015), Sydney, January 27-30, 2015.

25. Farhad Merchant, Arka Maity, Mahesh Mahadurkar, Kapil Vatwi, Ishan Munje, Madhava Krishna, Nalesh S, Nandhini Gopalan, Soumyendu Raha, S. K. Nandy, Ranjani Narayan, **"Micro-architectural Enhancements in Distributed Memory CGRAs for LU and QR Factorizations"**, Proceedings of the IEEE VLSI Design 2015, Bangalore, India, Jan 3-7, 2015.

26. Gopinath Mahale, Hamsika Mahale, Arnav Goel, S.K.Nandy, S.Bhattacharya, Ranjani Narayan, **" Hardware Solution For Real-time Face Recognition"**, Proceedings of the IEEE VLSI Design 2015, Bangalore, India, Jan 3-7, 2015.

27. Mahnaz Mohammadi, Nitin Satpute, Rohit Ronge, Jayesh Ramesh Chandiramani, S. K. Nandy, Aamir Raihan,Tanmay Verma, Ranjani Narayan**,** and Sukumar Bhattacharya, **" A Flexible Scalable Hardware Architecture for Radial Basis Function Neural Networks"**, Proceedings of the IEEE VLSI Design 2015, Bangalore, India, Jan 3-7, 2015.

28. Gopinath Mahale, Hamsika Mahale, Rajesh Parimi, S.K. Nandy and Sukumar Bhattacharya, **" Hardware Architecture of Bi-Cubic Convolution Interpolation for Real-time Image Scaling"**, Proceedings of the International Conference on Field-Programmable Technolgy, Shanghai Dec 10-12, 2014.

29. Pavan Akulakrishna, J Lakshmi, S K Nandy, **" Efficient Storage of Big-Data for Real-Time GPS Applications"**, Proceedings of the IEEE International Conference on Big Data and Cloud Computing (BDCloud2014) Sydney, Australia Dec. 3-5, 2014.

30. Aakriti Gupta, J Lakshmi, S K Nandy, **" Real Time Routing in Road Networks"**, Proceedings of the IEEE International Conference on Big Data and Cloud Computing (BDCloud2014) Sydney, Australia Dec. 3-5, 2014.

31. Zoltán Endre Rákossy, Farhad Merchant, Axel Acosta Aponte, S. K. Nandy, Anupam Chattopadhyay, **"Scalable and Energy-Efficient Reconfigurable Accelerator for Column-Wise Givens Rotation",** 22nd IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) IEEE, 2014, Oct 6-8, 2014, Playa del Carmen, Mexico.

32. Kavitha Madhu, Saptarsi Das, Madhava Krishna, Nalesh S, S. K. Nandy, Ranjani Narayan, **"Synthesis of Instruction Extensions on HyperCell, a Reconfigurable Datapath",** proceedings of SAMOS XIV 2014, July 14-17, 2014, Samos, Greece.

33. Mahesh Mahadurkar, Farhad Merchant, Arka Maity, Kapil Vatwani, Munje, Nandhini Gopalan, S. K. Nandy, Ranjani Narayan, **"Co-Exploration of NLA kernels and Specification of Compute Elements in Distributed Memory CGRAs",** proceedings of SAMOS XIV 2014, July 14-17, 2014, Samos, Greece.

34. Zoltán Endre Rákossy, Farhad Merchant, Axel Acosta Aponte, S. K. Nandy, Anupam Chattopadhyay, **"Efficient and Scalable CGRA-based Implementation of Column-wise Givens Rotation",** proceedings of IEEE ASAP 2014, June 18-20, 2014, Zurich, Switzerland.

35. Farhad Merchant, Anupam Chattopadhyay, Ganesh Garga, S. K. Nandy, Ranjani Narayan, and Nandhini Gopalan, **" Efficient QR Decomposition Using Low Complexity Column-wise Givens Rotation (CGR)"**, proceedings of the IEEE VLSI Design, Jan 7-9, 2014, VLSI Design 2014, IIT Mumbai (Bombay).

36. Ankit Anand, Lakshmi J and S. K. Nandy, **"Virtual Machine Placement optimization supporting performance SLAs",** proceedings of the IEEE International Conference on Cloud Computing Technology and Science (CloudCom 2013), Dec 2-5, 2013, Bristol, UK.

37. Kala S, Nalesh S, S. K. Nandy, and Ranjani Narayan **" Design of a Low Power 64 point FFT Architecture for WLAN Applications**, proceedings of the 25th IEEE International Conference on Microelectronics, Dec 15 - 18, 2013, Beirut, Lebanon

38. Mohit Dhingra , J. Lakshmi , S. K. Nandy, Chiranjib Bhattacharyya , and K. Gopinath **" Elastic Resources Framework in IaaS, preserving performance SLAs "**, proceedings of the IEEE Sixth International Conference on Cloud Computing, June 28 2013-July 3 2013, Santa Clara, California, USA.

39. Abhijit Giri and S. K. Nandy, **"Optimal Pipeline Depth And Supply Voltage For Power-constrained Processors"**, proceedings of the 26th International Conference on VLSI Design, January 5-10, 2013 Pune, India.

40. Kala S, Nalesh S, Arka Maity_, S K Nandy and Ranjani Narayan, **"High Throughput, Low Latency, Memory Optimized 64K Point FFT Architecture Using Novel Radix-4 Butterfly Unit"**, proceedings of the 2013 IEEE International Symposium on Circuits and Systems, to be held in Beijing, China from 19-23 May, 2013.

41. M. Dhingra, J. Lakshmi, and S. K. Nandy, **"Resource usage monitoring in Clouds"**, proceedings of the ACM/IEEE 13th International Conference on Grid Computing (GRID), September 2012.

42. Saptarsi Das, Keshavan Varadarajan, Ganesh Garga, Rajdeep Mondal, Ranjani Narayan and S K Nandy, **"A Method for Flexible Reduction over Binary Fields using a Field Multiplier"**, In the proeedings of the Internation Conference on Security and Cryptography (SECRYPT '11), July 2011 (Best Paper Award).

43. Adarsha Rao, S. K. Nandy, Hristo Nikolov, and Ed F. Deprettere. **"USHA: Unified Software and Hardware Architecture for Video Decoding."** In *Proceedings of the 9th IEEE Symposium on Application Specific Processors,* SASP'11, pages 30–37, june 2011 (Best paper Award).

44. Ratna Krishnamoorthy, Keshavan Varadarajan, Masahiro Fujita, S. K. Nandy, Mythri Alle, and Ranjani Narayan, **"Dataflow Graph Partitioning for Optimal Spatio-Temporal Computation on a Coarse Grained Reconfigurable Architecture",** In 7th International Symposium on Applied Reconfigurable Computing (ARC 2011), March 2011.

45. Ratna Krishnamoorthy, Keshavan Varadarajan, Ganesh Garga, Mythri Alle, Ranjani Narayan, Masahiro Fujita and S K Nandy, **"Towards Minimizing Reconfiguration Overhead in Dynamically Reconfigurable Processors: REDEFINE as a case study**", proceedings of the International Conference on Compilers, Architecture and

Synthesis for Embedded Systems (CASES 2010), Scottsdale, Arizona, Oct 24-29, 2010.

46. Thambi Prashank, Prasadarao M, Keshavan Varadarajan, Avinaba Dutta, Mythri Alle, Nandy S.K and Ranjani Narayan**, "Enhancements for Variable N-point Streaming FFT/IFFT on REDEFINE, a Runtime Reconfigurable Architecture"**, proceedings of the SAMOS X: International Conference on Embedded Computer Systems: Architectures, MOdeling and Simulation to be held in Samos, Greece, July 19-22, 2010.

47. Prasenjit Biswas, Keshavan Varadarajan, Mythri Alle, S. K Nandy and Ranjani Narayan, **"Design space exploration of systolic realization of QR factorization on a runtime reconfigurable platform"**, SAMOS X: International Conference on Embedded Computer Systems: Architectures, MOdeling and Simulation to be held in Samos, Greece, July 19-22, 2010.

48. Prasenjit Biswas, Pramod P Udupa, Rajdeep Mondal, Keshavan Varadarajan, Mythri Alle, S. K Nandy and Ranjani Narayan, **"Accelerating Numerical Linear Algebra Kernels on a Scalable Run Time Reconfigurable Platform"**, Proceedings of IEEE Computer Society Annual Symposium on VLSI, Lixouri, Kefalonia, Greece, July 5-7, 2010.

49. J. Lakshmi and S. K. Nandy, **"Is I/O Virtualization Ready for End-to-End Application Performance?",** Proceedings of 17th International Conference on Advanced Computing and Communications 2009, Bangalore, India, December 14-17, 2009.

50. Hristo Nikolov, Adarsha Rao, Ed F. Deprettere, S. K. Nandy, and Ranjani Narayan. **"H.264 Decoder: A Design Style Comparison Case Study."** In *Proceedings of the 43rd Asilomar conference on Signals, systems and computers,* Asilomar'09, pages 236–242, 2009.

51. Alexander Fell, Prasenjit Biswas, Jugantor Chetia, S.K. Nandy, and Ranjani Narayan, "**Generic routing rules and a scalable access enhancement for the Network-on-Chip RECONNECT", (**proceedings of the SOCC 2009), SOC Conference, September 2009.

52. Alexander Fell, Mythri Alle, Keshavan Varadarajan, Prasenjit Biswas, Saptarsi Das, Jugantor Chetia, S. K. nandy and Ranjani Narayan, **"Streaming FFT on REDEFINE-v2: An Application-Architecture Design Space Exploration",** proceedings of the 2009 International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES 2009), Grenoble, France, October 2009.

53. Adarsha Rao, Mythri Alle, Sainath V, Reyaz Shaik, Rajashekhar Chowhan, Sravanthi Mantha, Sankaraiah, S K Nandy, and Ranjani Narayan, **"An Input Triggered Polymorphic ASIC for H.264 decoding"**, proceedings of ASAP 2009, Boston, USA.

54. Ganesh Garga, David Guevorkian, S.K Nandy, H.S Jamadagni, **"High-Throughput Flexible Constraint Length Viterbi Decoders on De Bruijn, Shuffle-Exchange andButterfly Connected Architectures"**, proceedings of the IX SAMOS Sysmposium 2009, Samos, Greece July 20-22, 2009.

55. A N Satrawala and S K Nandy, **"RETHROTTLE: Execution Throttling in the REDEFINE SoC Architecture"**, proceedings of the IX SAMOS Sysmposium 2009, Samos, Greece July 20-22, 2009.

56. Ritesh Rajore, S K Nandy, H S Jamadagni, **"Architecture of Run-time Reconfigurable Channel Decoder"**, proceedings of the International Conference on Communications (ICC), Dresden, Germany, June 2009.

57. Mythri Alle, Keshavan Varadarajan, Alexander Fell, S K Nandy, and Ranjani Narayan, **''Compiling Techniques for Coarse Grained Runtime Reconfigurable Architectures''**, proceedings of the 5th International Workshop on Applied Reconfigurable Computing, Karlsruhe, Germany, March 2009.

58. J. Lakshmi, and S. K. Nandy, "**I/O Device Virtualization in the multi-core era, a QoS perspective"**, Proceedings of the 1st International Workshop on Grids, Clouds and Virtualization, Geneve May 2009.

59. J. Lakshmi, and S. K. Nandy, "**Modeling Architecture-OS Interactions using Layered Queuing Network Models"**, Proceedings of HPC-Asia 2009, March 2009, Taiwan.

60. Adarsha Rao, Mythri Alle, S K Nandy and Ranjani Narayan, **"Architecture of a Polymorphic ASIC for interoperability across multi-mode H.264 decoders"**, proceedings of ASAP 2008, Leuven July 2008.

61. Mythri Alle, Keshavan Varadarajan**,** Ramesh Reddy C, Nimmy Joseph, Alexander Fell, Adarsha Rao, S K Nandy and Ranjani Narayan, "**Synthesis of Application Accelerators on Runtime Reconfigurable Hardware**",

proceedings of ASAP 2008, Leuven July 2008.

62. Nimmy Joseph, Ramesh Reddy C, Keshavan Varadarajan, Mythri Alle, Alexander Fell, S K Nandy, and Ranjani Narayan, "**RECONNECT: A NoC for polymorphic ASICs using a Low Overhead Single Cycle Router**", proceedings of Application-Specific Systems, Architectures and Processors (ASAP 2008), Leuven July 2008.

63. Ganesh Garga, Mythri Alle, Keshavan Varadarajan, S. K. Nandy and H. S. Jamadagni, "**Realizing a Flexible Constraint Length Viterbi Decoder for Software Radio on a de Bruijn interconnection network**", Proceedings of International Symposium on System-on-chip (SoC 2008), Tampere, Finland, Nov 2008.

64. Amar Nath S, Keshavan V, Mythri Alle, S. K. Nandy, and Ranjani Narayan, **"REDEFINE: Architecture of a SoC Fabric for Runtime Composition of Computation Structures"**, Proceedings of the International Conference on Field Programmable Logic and Applications, FPL 2007, Amsterdam, Aug 2007.

65. S. Banerjee, G. Surendra, S. K. Nandy, **"Program Phase directed Dynamic Cache Way Reconfiguration for Power Efficiency ",** Proceedings of the ASP-DAC 2007 Asia and South Pacific Design Automation Conference, Jan 24-26, 2007, Yokohama, Japan.

66. Mythri Alle, Jayanta Biswas and S. K. Nandy, *"***High Performance VLSI Implementation for H.264 Inter/Intra Prediction***"*, Proceedings of International Conference on Distributed on Consumer Electronics (ICCE), Las Vegas, USA, 2007.

67. Keshavan Varadarajan, S. K. Nandy, et al, **"Molecular Caches: A caching structure for dynamic creation of application-specific heterogeneous cache regions"**, Proceedings of the 39th Annual IEEE/ACM International Symposium on Microarchitecture, 2006 (MICRO-39). Orlando, USA, Dec 9-13, 2006.

68. Sandeep B Singh, Jayanta Biswas, and S K Nandy, **"A Cost Effective Pipelined Divider for Double Precision Floating Point Number"**, Proceedings of 17th International Conference on Application-specific Systems, Architectures and Processors (ASAP 2006), Colorado, USA, September 11-13, 2006.

69. Mythri Alle, Jayanta Biswas, and S K Nandy, **"High performance VLSI architecture design for H.264 CAVLC decoder"**, Proceedings of 17th International Conference on Application-specific Systems, Architectures and Processors (ASAP 2006), Colorado, USA, September 11-13, 2006.

70. Mythri Alle, Jayanta Biswas, and S K Nandy, **"Speed and Area Optimized Implementation of H.264 8 X 8 DCT Transform and Quantizer"**, Proceedings of 2006 International Conference on Distributed Multimedia Systems (DMS'2006), Grand Canyon, USA, August 30 – September 1, 2006.

71. K. Kalapriya, S.K. Nandy, and N.C. Narendra, **"A Framework for Measurement of End-To-End QoS Requirements in Loosely Coupled Systems"**, Proceedings of AINA-SOCNE Vienna, Austria, April 2006.

72. Jayanta Biswas and S. K. Nandy, **"Key Management and Distribution for secure overlay multicast for Mobile Ad Hoc Networks"**, Proceedings of IEEE International Conference on Communications (ICC2006), Istanbul, Turkey, Jun. 2006.

73. Umesh Bellur, S.K. Nandy, K.Kalapriya and N. C. Narendra, **"Functional and Architectural Adaptation in Pervasive Computing Environments"**, Proceedings of MPAC, Middleware 2005, Grenoble, France, Nov 2005.

74. K.C. Nainwal, J. Lakshmi, S. K. Nandy, Ranjani Narayan and K. Varadarajan, **"A Framework for QoS Adaptive Grid Meta Scheduling"**, Proceedings of HADIS 2005 (First International Workshop on High Availability of Distributed Systems), Copenhagen, Denmark, August 2005.

75. Bharath.N, Nagaraju Bussa, S.K.Nandy, **``Artificial Deadlock Detection in Process Networks for ECLIPSE''**, proceedings of the IEEE 16th International Conference on Application-specific Systems, Architectures and Processors (ASAP 2005), Samos, Greece July 23 to 25, 2005.

76. Jayanta Biswas and S. K. Nandy, **`` Efficient Overlay Network Management scheme for Wireless Networks''**, proceedings of IEEE WirelessCom 2005 (International Conference on Wireless Networks, Communications and Mobile Computing), Hawaii, USA, June 2005.

77. Jayanta Biswas and S. K. Nandy, **``Quality of Support for Multicasting over Mobile Ad-hoc Networks''**, WiQoS'05 in proceedings of IEEE WirelessCom 2005 (International Conference on Wireless Networks, Communications and Mobile Computing), Hawaii, USA, June 2005.

78. K. Kalapriya, S. K. Nandy: **"Throughput Driven, Highly Available Streaming Stored Playback Video Service over a Peer-to-Peer Network",** Proceedings of the International Conference on Advanced Information Networking and Applications (AINA), Taiwan, March 28-30, 2005.

79. Jayanta Biswas and S. K. Nandy, **''Application Layer Multicasting for Mobile Ad-Hoc Networks with Network Layer Support,''** Proceedings of 29th Annual IEEE Conference on Local Computer Networks (LCN), Tampa, Florida, USA, November, 2004.

80. Jayanta Biswas, Mukti Barai, and S. K. Nandy, **"Efficient Hybrid Multicast Routing Protocol for Ad-hoc Wireless Netwroks,''** Proceedings of 29th Annual IEEE Conference on Local Computer Networks (LCN), Tampa, Florida, USA, November, 2004.

81. Subhasis Banerjee, G. Surendra and S. K. Nandy, **``Exploiting Program Execution Phases to Trade Power and Performance for Media Workload''**, in the proceedings of the 47th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2004), Hiroshima, Japan, July 2004.

82. Bharath N and S. K. Nandy, **``A Runtime Mechanism for Artificial Deadlock Detection in Bounded Process Networks''**, in the proceedings of the 47th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2004), Hiroshima, Japan, July 2004.

83. K. Kalapriya, R. Venkatesh Babu and S. K. Nandy, **''Streaming Playback Video over a Peer-to-Peer Network''**, in the proceedings of the International Conference on Communications (ICC 2004), Paris, France, June 2004.

84. K. Kalapriya, S.K.Nandy, Deepti Srinivas, R. Uma Maheswari, V. Satish, **"An Architectural View of the Entities Required for Execution of Task in Pervasive Space",** 10th International Workshop on Future trends in Distributed Computing Systems, Suzhou, China, May 2004.

85. K. Kalapriya, S.K. Nandy, et al**, "A Framework for Resource Discovery in Pervasive Computing for Mobile Aware Task Execution",** in the proceedings of the ACM SIGMicro Computing Frontiers 2004, April 14-16, 2004, Ischia Italy.

86. G. Surendra, S. Banerjee, S. K. Nandy, **"Power-Performance Trade-off using Pipeline Delays"**, Proceedings of the ASP-DAC 2004) Asia and South Pacific Design Automation Conference, Jan 27-30, 2004, Yokohama, Japan

87. S. Banerjee, G. Surendra, S. Banerjee, S. K. Nandy, **"Exploiting Program Execution Phases to trade Power and Performance for Media Workload",** Proceedings of the ASP-DAC 2004 Asia and South Pacific Design Automation Conference, Jan 27-30, 2004, Yokohama, Japan.

88. K. Kalapriya, B. R. Raghucharan, Abhijit Lele and S. K. Nandy, **``Dynamic Traffic Profiling for Efficient Link Bandwidth Utilization in QoS Routing''** Proceedings of the 9th Asia-Pacific Conference on Communications, Penang, Malaysia, September 2003.

89. Pradeep H. Rao, S. K. Nandy an Satya Kiran, **"Simultaneous MultiStreaming for Complexity-Effective VLIW Architectures"**, Proceedings of the Advances in Computer System Architecture (ACSAC'2003), Japan, September 2003.

90. K. Kalapriya, B. R. Raghucharan, Abhijit Lele, and S. K. Nandy, **"Traffic Profiling for Efficient Network Resource Utilization"**, Proceedings of the 2003 International Conference on Internet Computing, June 23-26, 2003, Las Vegas, USA.

91. Pradeep H. Rao and S. K. Nandy, **"Evaluating Compiler Support for Complexity-Effective Network Processing",** Proceedings of the Workshop on Complexity Effective Design, held in conjunction with the 30th International Symposium on Computer Architecture (ISCA), San Diego, California, June 7-12, 2003.

92. Satya Kiran, Jayram M.N., Pradeep H. Rao, and S. K. Nandy**, "A Complexity Effective Communication Model for Behavioral Modeling of Signal Processing Applications"**, Proceedings of the 40th IEEE/ACM Design Automation Conference, Anaheim, CA USA, June 2003.

93. S. K. Nandy, G. Surendra, and Subhasis Banerjee, **"Architectural Trends for Streaming Applications: An SOC perspective"**, (invited paper) in the proceedings of the 11th Annual Symposium on System on a Chip, IEEE Bangalore section, Indian Institute of Science, Bangalore, November 22-23, 2002.

94. Manvi Agarwal, S. K. Nandy, Jos van Eijndhoven, and S. Balakrishnan, **"Multithreaded Architectural support for Speculative Trace Scheduling in VLIW Processors",** 15th Symposium on Integrated Circuits and System Design, September 9-14, 2002, Brazil.

95. H. Sarojadevi, S. K. Nandy, and S. Balakrishnan, **"Enforcing Cache Coherence at Data Sharing Boundaries without Global Control: A Hardware-Software Approach"**, Euro-Par 2002, August 27-30 2002, Paderborn, Germany.

96. Manvi Agarwal, S. K. Nandy, Jos van Eijndhoven, and S. Balakrishnan **"On the benefits of Speculative Trace Scheduling in VLIW Processors"**, Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA' 02), June 24-27, 2002, Las Vegas, USA.

97. Abhijit Lele and S. K. Nandy, ``**Design and Performance Evaluation of Reconfigurable Low Power Gigabit ATM Switch"**, Proceedings of the 6th IEEE Asia-Pacific Conference on Communications, Oct 30 - Nov 2, 2001, Seoul, Korea.

98. Abhijit Lele and S. K. Nandy, ``**Multiresolution Based Wavelet Modeling of Multiplexed VBR Traffic"**, Proceedings of the 6th IEEE Asia-Pacific Conference on Communications, Oct 30 - Nov 2, 2001, Seoul, Korea.

99. Arshad Ahmed, S. K. Nandy and Paul Sathya, ``**Content Adaptive Motion Estimation for Mobile Video Encoders"**, Proceedings of the IEEE International Symposium on Circuits and Systems May 6-9, 2001, Sydney, Australia.

100. Surendra, S. K. Nandy and Paul Sathya, ``**Redeem_RTL: A Software Tool for Customizing Soft Cells for Embedded Applications"**, Proceedings of the 14th International Conference on VLSI Design, Bangalore, India, January 4-7, 2001.

101. Abhijit Lele and S. K. Nandy, ``**Architecture of a Reconfigurable Low Power Gigabit ATM Switch"**, Proceedings of the 14th International Conference on VLSI Design, Bangalore, India, January 4-7, 2001.

102. Abhijit Lele and S. K. Nandy, ``**Multiresolution Based Wavelet Modeling of Multiplexed VBR Traffic"**, Proceedings of the 6th IEEE Asia-Pacific Conference on Communications, Oct 30 - Nov 2, 2000, Seoul, Korea.

103. Abhijit Lele and S. K. Nandy, ``**Design and Performance Evaluation of Reconfigurable Low Power Gigabit ATM Switch"**, Proceedings of the 6th IEEE Asia-Pacific Conference on Communications, Oct 30 - Nov 2, 2000, Seoul, Korea.

104. Abhijit Lele, S. K. Nandy and D. H. J. Epema, ``**Dynamic Channel Allocation for next Generation Wireless Networks"**, Proceedings of the International Conference on Software, Telecommunications and Computer Networks (SoftCOM 2000), October 10 -14, 2000, Croatia and Italy.

105. Abhijit Lele, S. K. Nandy and D.H.J. Epema, ``**Design Space Exploration for Providing QoS within the Harmony Framework"**, Proceedings of the International Conference on Multimedia and Expo 2000, July 31 - August 2, 2000, New York.

106. M. Srikanth Rao and S. K. Nandy, ``**Power Minimization using Control Generated Clocks"**, proceedings of the 37th ACM/IEEE Design Automation Conference (DAC), June 5 - 9, 2000, Los Angeles USA.

107. S. Balakrishnan and S. K. Nandy, ``**Performance Evaluation of Multithreaded Architectures for Media Processing Applications"**, proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS) May 28 - May 31, 2000, Geneva Switzerland.

108. M. Srikanth Rao and S. K. Nandy**,``Controller Redesign based Clock and Register Power Minimization"**, proceedings of the IEEE International Symposium on Circuits and Systems May 28 - May 31, 2000, Geneva Switzerland.

109. Abhijit Lele and S. K. Nandy, ``**HARMONY - A Framework for providing Quality of Service in Wireless Mobile Computing Environment"**, Proceedings of the 6th International Conference on High Performance Computing, December 17-20, 1999, Calcutta, India.

110. S. Balakrishnan and S. K. Nandy, ``**Multithreaded Architectures for Media Processing"**, proceedings of the 1st Workshop on Media, Processors and DSPs (MP-DSP) Haifa, Israel, November 15, 1999, held in Conjunction with

the 32nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), November 16-18, 1999.

111. Avinash Gautam, V. Visvanathan and S. K. Nandy, ``**Automatic Generation of Tree Multipliers using Placement-Driven Netlists"**, Proceedings of the International Conference on Computer Design (ICCD '99), October 10 - 13, 1999.

112. S. Ramanathan, V. Visvanathan and S.K. Nandy, ``**Synthesis of Configurable Architectures for DSP Algorithms"**, In the proceedings of the 12th International Conference on VLSI Design, Jan 7-10, 1999, Goa, India.

113. H. Saroja Devi and S. K. Nandy, ``**Obviating the need for Directory in Auto-invalidating Caches**", Proceedings of the 6th International Conference on Advanced Computing, December 14-16, Pune (India), 1998.

114. Abhijit Lele and S. K. Nandy, ``**Can QoS Guarantees be supported for live Video over ATM Networks?"**, Proceedings of GLOBECOM '98, Sydney, Australia, November 1998.

115. S. Ramanathan, V. Visvanathan and S.K. Nandy, ``**Architectural Synthesis of Low-Power Computational Engines for LMS Adaptive Filtering,"** Proceedings of the International Conference on Signal Processing Applications and Technology, Toronto, Canada, September 1998.

116. S. Balakrishnan and S. K. Nandy, ``**Arbitrary Precision Arithmetic-SIMD Style"**, proceedings of the 11th International Conference on VLSI Design, Chennai, India, January 4--7, 1998.

117. S. K. Nandy, S. Balakrishnan and Ed Deprettere, ``**SYMPHONY : A Scalable High Performance Architecture Framework for Media Applications"**, Proceedings of the 5th International Conference on Advanced Computing, December 15-17, Chennai, 1997.

118. S. Balakrishnan, S. K. Nandy, and Arjan van Gemund, ``**Modeling Multi-threaded Architectures in PAMELA for Real-time High Performance Applications"**, Proceedings of the 4th International Conference on High Performance Computing, Bangalore, India, December 18-21, 1997.

119. M. R. Karthikeyan and S. K. Nandy, ``**An Asynchronous Architecture for Digital Signal Processors"**, Proceedings of the European Design and Test Conference and Exhibition, Paris, March 17--20, 1997.

120. Vinod Menezes, S. K. Nandy, Biswadip Mitra, ``**Spatial Frequency based Motion Estimation for Image Sequence Compression"**, Proceedings of the 3rd International Conference on High Performance Computing, Trivandrum, India, December 19-22, 1996.

121. S. K. Nandy and S. Balakrishnan, ``**Modeling and Design of High Performance VLSI Processor Arrays"**, Conference on Emerging Microelectronics and Interconnection Technologies, EMIT '96, February 12 -- 16, 1996, Bangalore, India (Invited Paper).

122. S. K. Nandy, S. Balakrishnan, and Ranjani Narayan, ``**Concerting Processors for Domain Specific High Performance Architectures"**, Proceedings of the 2nd International Conference on High Performance Computing, New Delhi, India, Dec 27 - Dec 30, 1995.

123. S. K. Nandy and Ranjani Narayan, ``**An Incessantly Coherent Cache Scheme for Shared Memory Multi-threaded Systems"**, Proceedings of the First International Workshop on Parallel Processing, Bangalore, India, December 26--31, 1994, pp. 240-245. Also as LCS, CSG-Memo 356, Technical Report, Massachusetts Institute of Technology, September 15, 1994.

124. John Morris, S. K. Nandy et al, ``**Hermes: Communicating *T-NGs"**, LCS, CSG-Memo 358, Technical Report, Massachussetts Institute of Technology, June 1994,``LIMITED DISTRIBUTION".

125. B.S. Ang, D. Chiou, J.C. Hoe, X.-W. Shen, J. Morris, S.K. Nandy and M.J. Beckerle, ``**ACD Requirements"**, LCS, CSG-Memo 357, June 1994, ``LIMITED DISTRIBUTION".

126. A Giri, V. Visvanathan, S. K. Nandy, and S. K. Ghoshal, ``**High Speed Digital Filtering on SRAM-Based FPGAs"**, Proceedings of the seventh international conference on VLSI Design, January 5-8, 1994, Calcutta, India.

127. G. N. Rathna, S. K. Nandy and K. Parthasarathy, ``**A Methodology for Architecture Synthesis of Cascaded IIR Filters"**, Proceedings of the seventh international conference on VLSI Design, January 5-8, 1994, Calcutta, India.

128. Debabrata Ghosh, S. K. Nandy and K. Parthasarathy, ``**TWTXBB:A Low Latency, High Throughput Multiplier**

**Architecture using a New 4→2 Compressor"**, Proceedings of the seventh international conference on VLSI Design, January 5-8, 1994, Calcutta, India.

129. Debabrata Ghosh, Shamik Sural and S. K. Nandy, ``**A 600MHz Half-Bit Level Pipelined Multiplier Macrocell"**, Proceedings of the seventh international conference on VLSI Design, January 5-8, 1994, Calcutta, India.

130. Debabrata Ghosh and S. K. Nandy, ``**A 600-MHz Halfbit Level Pipelined Accumulator-Interleaved Multiplier Accumulator Core"**, 1993 IEEE Workshop on VLSI Signal Processing, October 20 - 22, Veldhoven, The Netherlands.

131. Debabarata Ghosh and S. K. Nandy, ``**A 400MHZ Wave-Pipelined 8X8-bit Multiplier in CMOS Technology"**, International Conference on Computer Design (ICCD'93), Cambridge, Massachusetts, USA, October 3-6, 1993.

132. S.K. Nandy, Ranjani Narayan, V. Visvanathan, P. Sadayappan, P. Chauhan, ``**A Parallel Progressive Refinement Image Rendering Algorithm on a Scalable Multi-threaded VLSI Processor Array"**, Proceedings of the 1993 International Conference on Parallel Processing, Illinois, August 1993.

133. Debabrata Ghosh, S. K. Nandy, P. Sadayappan and K. Parthasarathy, ``**Architectural Synthesis of Performance--Driven Multipliers with Accumulator Interleaving"**, proceedings of the 30th ACM/IEEE Design Automation Conference, Dallas, USA, June 1993.

134. Ranjani Narayan, S.K. Nandy, V. Rajaraman, P.K. Fangaria**,** ``**A Space and Time Efficient Global Memory Support on Multicomputer Systems"**, Proceedings of the IASTED International Conference on Modelling and Simulation, Pittsburgh during May 1993.

135. Debabrata Ghosh, S. K. Nandy, K. Parthasarathy and V. Visvanathan, ``**NPCPL : Normal Process Complementary Pass Transistor Logic for Low Latency, High Throughput Designs"**, Proceedings of the fifth international conference on VLSI Design (VLSI Design '93), Bombay, India, Jan 1993.

136. G. N. Ratna, M. K. Sridhar, K. Parthasarthy and S. K. Nandy, ``**Floating point processor with gate-array technology: A preliminary design"**, 3rd International Workshop on VLSI Design, 1990.

137. S. Balakrishnan and S. K. Nandy, ``**Quasi Dynamic Approach to Layout Compaction"**, EUROMICRO 90, Sixteenth Symposium on Microprocessing and Microprogramming, pp. 231-236.

138. C. E. Prakash and S. K. Nandy, ``**VOXEL based Modeling and Rendering Irregular Solids"**, EUROMICRO 90, Sixteenth Symposium on Microprocessing and Microprogramming, pp. 341-346.

139. S. K. Nandy, M. S. Kailasnath and Ranjani Narayan, ``**Parallel Logic Simulation in a Dataflow Oriented Multiprocessor System"**, Proceedings of the PARCOM 90, pp. 341-348.

140. N. B. Bhat and S. K. Nandy, ``**Special Purpose Architecture for Accelerating Bitmap DRC"**, Proceedings of the 26th ACM/IEEE Design Automation Conference, Las Vagas, 1989, pp. 674-677.

141. S. K. Nandy, Rajat Moona and S. Rajagopalan, ``**Linear Quadtree Algorithms on the Hypercube"**, Proceedings of the International Conference on Parallel Processing, vol. 3, pp. 227-229, 1988.

142. N. B. Bhat and S. K. Nandy, ``**New Algorithms for Hardware Acceleration of DRC"**, Proceedings of the 2nd International Workshop on VLSI Design, Bangalore, India, 1988, pp 382-413.

143. R. B. Panwar and S. K. Nandy, ``**Parallel Architecture for Boundary Following of Regions of an Image stored as a Linear Quadtree"**, Proceedings of the 26th Annual Allerton Conference, on Communication, control and Computing, September 1988.

144. M. K. Srinivas, S. K. Nandy and R. Moona, ``**Implementation Issues of a Two-Layer Block Router Based on Lee's Algorithm on Personal Computers"**, TENCON, August 1987, Seoul, Korea, pp. 774-778.

145. S. K. Nandy and I. V. Ramakrishnan, ``**Dual Quadtree representation for VLSI Designs"**, Proceedings of the 23rd ACM/IEEE Design Automation Conference, Las Vagas, July 1986, pp. 663-666.

146. S. K. Nandy and L. M. Patnaik, ``**Placement through Pairwise Interchange among Connected and Unconnected Logic Modules"**, Proceedings of the 23rd Annual Allerton Conference on Communications, Control and Computing, October 2-4, 1985, pp. 686- 687.

147. S. K. Nandy and L. M. Patnaik, ``**A Hybrid Technique for Placement of Logic Modules"**, Proceedings of the IEEE International Conference on Computers, Systems and Signal Processing, 1984, pp. 1460-1463.

## 5. OFFICES HELD, COMMITTEE MEMBERSHIPS

Technical Programme Committee member for IEEE conferences ASP-DAC, DAC, DATE, VLSI Design, HiPC, ADCOM, SAMOS

Served as session chair in ASP-DAC, HiPC, VLSI Design, MWSCAS, SAMOS

Invited to deliver Keynote and Plenary talks in International Conferences

Organized and served as a General Chair for the Asia and South Pacific International Conference on Embedded SoCs (ASPICES 2005) during July 5-8, 2005 in Bangalore, INDIA. This conference was held in co-operation with IEEE and ACS.

Executive Committee Member of "Advanced Communication and Computing Society (ACCS)". This is a society engaged in furthering awareness in High Performance Computing in India. He was also the program chair for ADCOM 2009, the annual conference on advanced computing hosted by ACCS.

Member, Information Technology Research Academy, Medialab Asia, MeitY

Member, Assessment Board for DRDO Scientists

Examiner for PhD theses from IITs (Delhi, Mumbai, Chennai, Indore, Hyderabad, and Kharagpur), Birla Institute of Technology and Science Pilani (Pilani, and Hyderabad) and Defense Institute of Advanced Technology, Pune

Senior Member, IEEE

## 6. PATENTS

1. Paul Sathya Chelladurai, Arshad Ahmed, Soumitra Kumar Nandy: Method for efficient low power motion estimation of a video frame sequence. STMicroelectronics November 2005: US 06968010
2. Paul Sathya Chelladurai, Arshad Ahmed, Soumitra Kumar Nandy: Method for efficient low power motion estimation of a video frame sequence. STMicroelectronics January 2003: US 20030012282-A1
3. Soumitra Kumar Nandy: A molecular cache for multi-core processor, Indian Patent Application No.1215/CHE/2006; Granted on 23.01.2013
4. Soumitra Kumar Nandy, Ranjani Narayan, Mythri Alle, Keshavan Vardarajan, Alexander Fell, Adarsha Rao, Ramesh Reddy, Nimmy Joseph: Method and system on chip (SoC) for adapting a runtime reconfigurable hardware to decode a video stream US Patent 8,891,614
5. Soumitra Kumar Nandy, R Narayan, M Alle, K Vardarajan, A Fell: Method and System on Chip (SoC) for Adapting a Reconfigurable Hardware for an Application in Runtime US Patent 20,150,309,808