Flybot FC

Design a compact STM32F7-based FPV flight controller intended for **reliable field use**: vibration, electrical noise, moisture/dust exposure, rough handling, and dense RF environments. Emphasis on **robust power + connectors + ESD/EMI + traceability**.

---

1) Form factor & mechanical

- **Mounting:** 30.5 × 30.5 mm, **M3** pattern (standard stack).
- **Board size:** ≤ 36 × 36 mm preferred.
- **Height:** keep components inside a typical FC stack envelope (goal ≤ 8–10 mm total, excluding connectors).
- **Connector retention:** all external connectors must be **positive-lock** (latch) OR reinforced (TH anchor + strain relief guidance).
- **Vibration resilience:** no tall unsupported parts; heavy components anchored; connector pads reinforced.

Deliverable: mechanical drawing (DXF/PDF) + keep-out zones + connector locations.

---

2) Core compute

- **MCU:** STM32F7 family (e.g., STM32F722/STM32F745 class), chosen for Betaflight or iNAV support.
- **Clocking:** stable HSE crystal; layout per ST recommendations.
- **Memory:** onboard flash per MCU; add external flash only if justified for logging.
- **Boot & recovery:** accessible boot mode and SWD pads (test pads acceptable).

Deliverable: MCU choice rationale + pin map aligned to Betaflight target conventions.

---

3) Sensors

IMU

- **Primary IMU:** 6-axis gyro/accel (modern, low-noise; exact part can be proposed by designer).
- **Secondary IMU footprint (optional but preferred):** alternate part footprint or second IMU (DNP option) for supply-chain resilience.
- **IMU power:** separate clean rail/filtering; local decoupling; guard/ground strategy.

Barometer (optional)

- Footprint + DNP option (for variants).

Deliverable: sensor placement strategy for vibration + EMI.

---

4) Power architecture

Inputs

- **VBAT input:** 2S–6S LiPo (7–26V nominal). (Designer can propose max rating e.g., 30–35V survivability.)
- **Protections required:**
    - **Reverse polarity** protection (ideal-diode MOSFET or equivalent).
    - **TVS diode** on VBAT sized realistically.
    - **Input filtering** (LC / ferrite strategy) for ESC noise.
    - **Inrush/plug transient consideration.**

Rails

- **5V rail:** ≥ 2.5A total (goal 3A) for RX, GPS, peripherals.
- **9V (or 10V) rail:** ≥ 2A for VTX (switchable if possible).

- **3.3V rail:** clean digital/sensor rail.
- **Brownout behavior:** design so brief sags don't cause MCU undefined states (supervisor/reset IC strongly preferred).

Monitoring

- **Voltage sense:** VBAT to ADC with proper scaling/filter.
- **Current sense:** onboard current sense input support (sensor + scaling) OR external sensor interface.

Deliverable: annotated power tree + protection calculations + estimated thermal dissipation.

---

5) Interfaces & I/O

RC / control

- **1× UART** dedicated for CRSF/ELRS.
- **1× UART** for GPS.
- **1× UART** spare for telemetry/peripheral.
- **CAN bus:** 1× CAN (preferred) for future ecosystem / UAVCAN devices.
- **I2C:** exposed for peripherals (mag, baro, etc.), with proper pullups and ESD consideration.

Motor/ESC

- **8× motor outputs** (PWM/DSHOT capable) with clean signal routing and ground reference.
- Support **bidirectional DSHOT** (layout + timer mapping).

USB

- USB-C preferred (or micro-USB if you must), with:

    - ESD protection
    - proper CC resistors if USB-C device port
    - robust mechanical anchoring

OSD / video

Pick one approach:

- **Digital-first:** skip analog OSD (lean build).
- **Analog support:** include OSD chip footprint (e.g., MAX7456-class) + video in/out pads.

Deliverable: pinout table + connector pin definitions.

---

6) EMI/ESD hardening requirements

- **ESD protection** on:
    - USB D+/D-
    - all external UART/I2C/CAN lines that leave the board via cable
- **EMI controls:**
    - continuous ground plane strategy
    - controlled return paths
    - separation between switching regulators and IMU
    - optional common-mode choke on USB if designer recommends

Deliverable: EMI/ESD protection map + layout notes.

---

7) Environmental protection

- **Conformal coating-ready** layout:
    - keep mask-defined boundaries
    - avoid trapped volumes under connectors
    - define “no-coat” zones (USB contact area, baro vent if used)
- Component selection preference: **industrial/automotive temp grades** where reasonable (esp. regulators, protection ICs).

Deliverable: coating plan + masking diagram.

---

8) DFM/DFT

- **Test pads** for:
    - VBAT, 5V, 9V, 3V3, GND
    - SWDIO/SWCLK/NRST
    - UART TX/RX
- Clear silkscreen labeling for orientation + major ports.
- BOM with alternates for key parts (IMU optional, regulators, TVS).

Deliverable: manufacturing notes + test procedure outline.

---

9) Documentation & handoff package (what the designer must deliver)

1. **Schematic** (PDF + source)
2. **PCB layout** (source) with stackup definition
3. **Gerbers + drill + pick&place + assembly drawing**
4. **BOM** with MPNs + alternates + lifecycle risk notes

5. **Power budget + thermal estimate**
6. **Betaflight target pin map** proposal (timers, UARTs, DSHOT mapping)
7. **Bring-up checklist** (first power, rails, USB, SWD, IMU comms)

---

10) Acceptance criteria

- Survives:
    - reverse polarity event (defined duration) without catastrophic damage
    - VBAT transient event (defined test) without failure
- Boots reliably:
    - after repeated plug cycles
    - under motor/ESC noise present (bench test with motors)
- Interfaces:
    - USB stable connection (no random disconnects)
    - IMU stable under vibration (basic vibration bench test or motor-induced vibration)
- Power rails:
    - 5V and 9V meet rated current without excessive temperature rise (define max ΔT target)