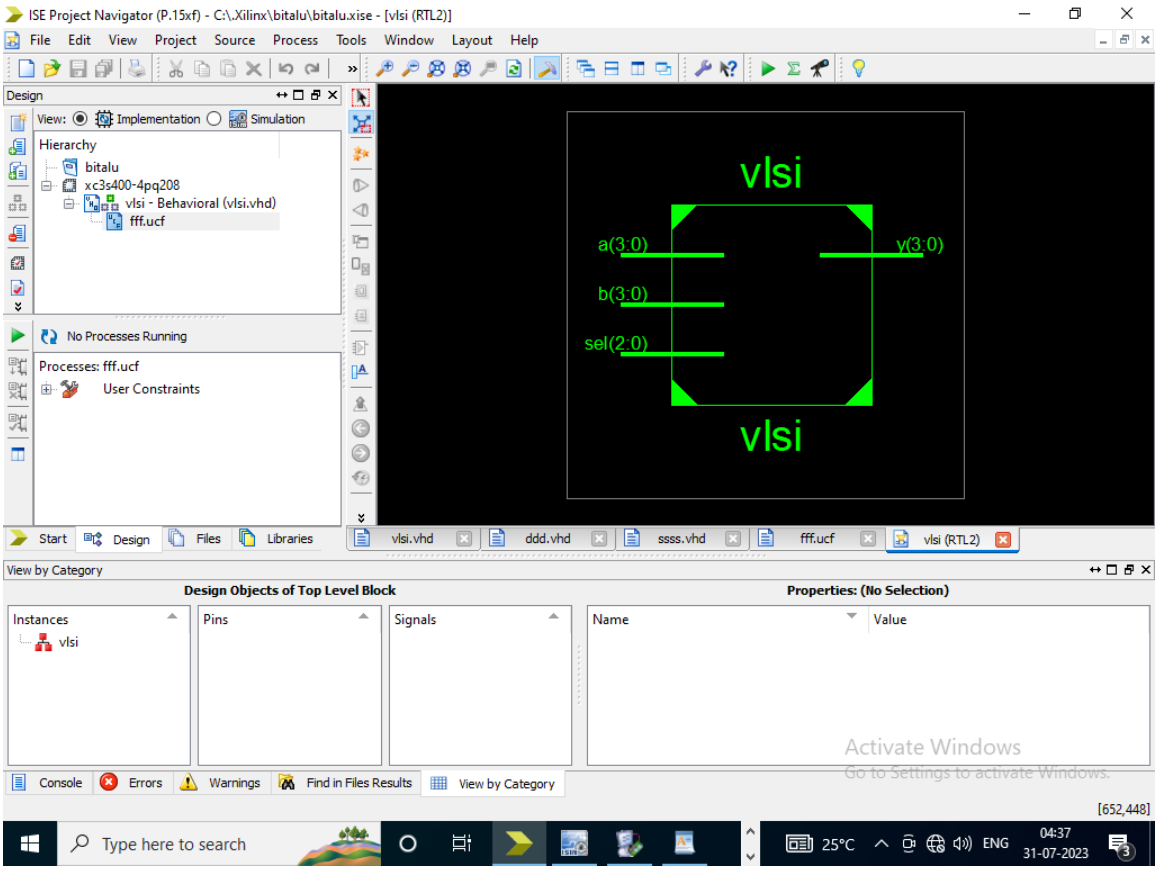
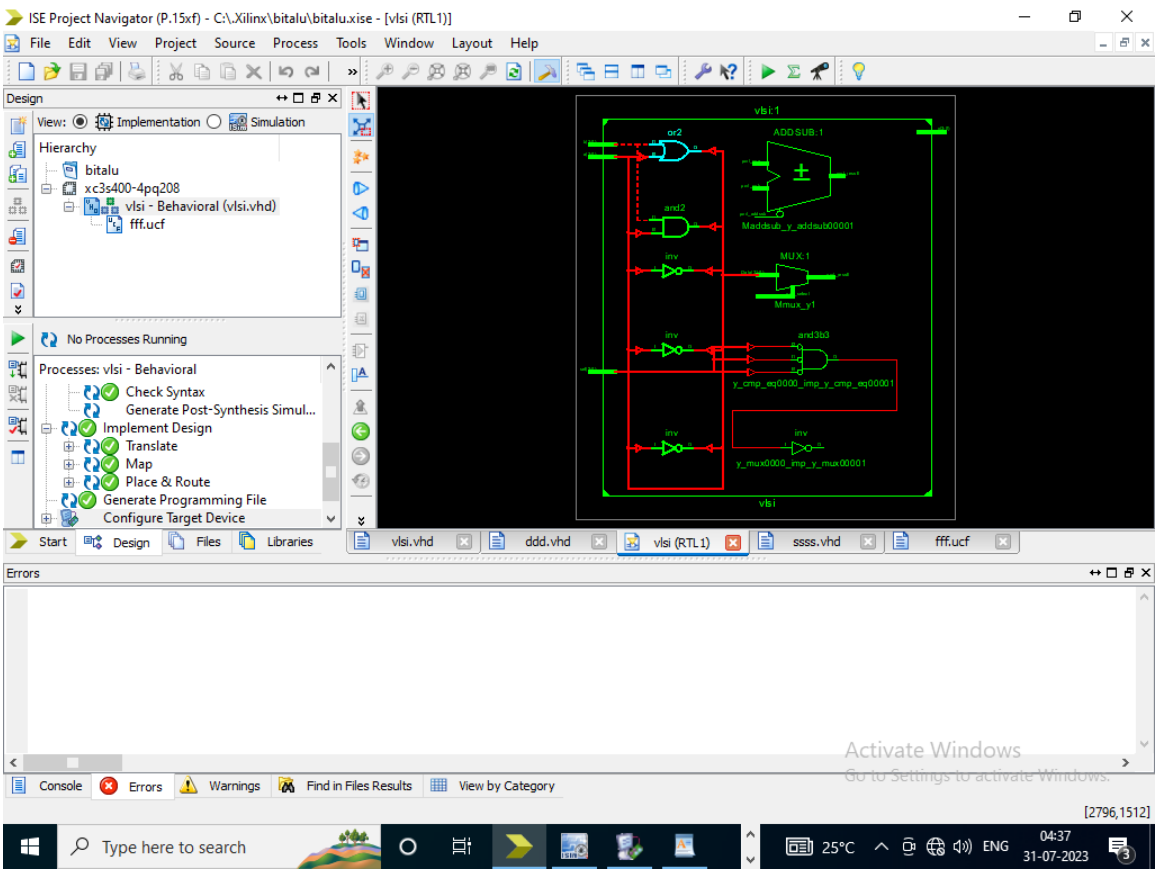
EXPERIMENT NO 2

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

use IEEE.STD_LOGIC_unsigned.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity vlsi is
    Port ( a : in    STD_LOGIC_VECTOR (3 downto 0);
           b : in    STD_LOGIC_VECTOR (3 downto 0);
           sel : in    STD_LOGIC_VECTOR (2 downto 0);
           y : out    STD_LOGIC_VECTOR (3 downto 0));
end vlsi;

architecture Behavioral of vlsi is
```

```
begin
process(a,b,sel)
begin
case sel is

when"000"=>y<=a+b;
when"001"=>y<=a-b;
when"010"=>y<=a and b;
when"011"=>y<=a or b;
when"100"=>y<=a nand b;
when"101"=>y<=a nor b;
when"110"=>y<=not a;
when"111"=>y<=a;
when others=>null;
end case;
end process;
end Behavioral;
```


ISE Project Navigator (P.15xf) - C:\.Xilinx\bitalu\bitalu.xise - [vlsi (RTL2)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
bitalu
xc3s400-4pq208
vlsi - Behavioral (vlsi.vhd)
fff.ucf
No Processes Running
Processes: fff.ucf
User Constraints
Start Design Files Libraries
vlsi
a(3:0)
b(3:0)
sel(2:0)
y(3:0)
vlsi
vlsi.vhd ddd.vhd ssss.vhd fff.ucf vlsi (RTL2)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
vlsi
Pins
Signals
Name
Value
Activate Windows
Go to Settings to activate Windows.
Console Errors Warnings Find in Files Results View by Category
[652,448]
Type here to search
25°C
ENG
04:37
31-07-2023




```
LIBRARY ieee;

USE ieee.std_logic_1164.ALL;


-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--USE ieee.numeric_std.ALL;


ENTITY ssss IS

END ssss;


ARCHITECTURE behavior OF ssss IS


    -- Component Declaration for the Unit Under Test (UUT)
```

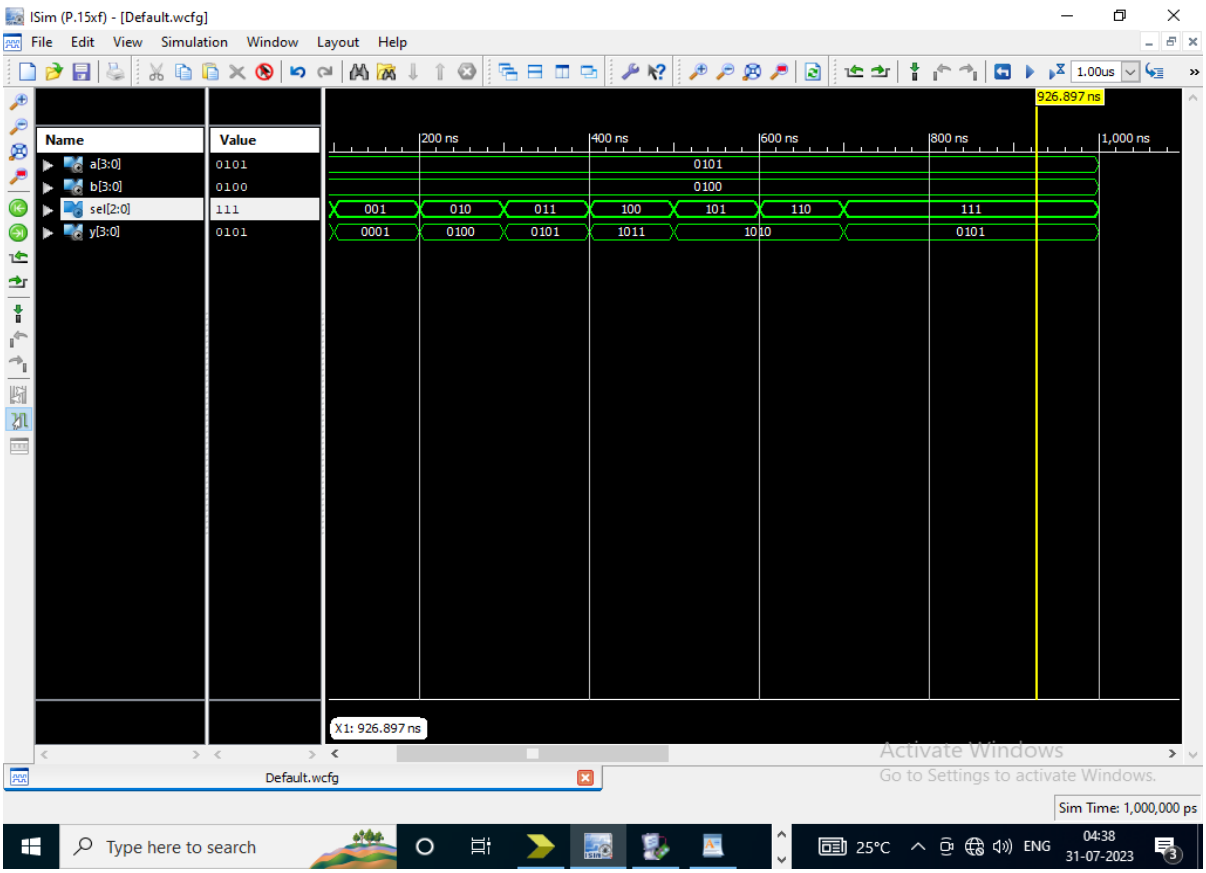
```
	COMPONENT vlsi
	PORT(
		a : IN	std_logic_vector(3 downto 0);
		b : IN	std_logic_vector(3 downto 0);
		sel : IN	std_logic_vector(2 downto 0);
		y : OUT	std_logic_vector(3 downto 0)
		);
	END COMPONENT;


	--Inputs
	signal a : std_logic_vector(3 downto 0) := (others => '0');
	signal b : std_logic_vector(3 downto 0) := (others => '0');
	signal sel : std_logic_vector(2 downto 0) := (others => '0');

		--Outputs
	signal y : std_logic_vector(3 downto 0);
	-- No clocks detected in port list. Replace <clock> below with
	-- appropriate port name

--	constant <clock>_period : time := 10 ns;

BEGIN

		-- Instantiate the Unit Under Test (UUT)
	uut: vlsi PORT MAP (
			a => a,
```

```
            b => b,
            sel => sel,
            y => y
        );

    -- Clock process definitions
--    <clock>_process :process
--    begin
--                <clock> <= '0';
--                wait for <clock>_period/2;
--                <clock> <= '1';
--                wait for <clock>_period/2;
--    end process;
--

    -- Stimulus process
    stim_proc: process
    begin
        a<="0101";
        b<="0100";
        sel<="000";

          -- hold reset state for 100 ns.
        wait for 100 ns;
        a<="0101";
        b<="0100";
        sel<="001";
```

```
        -- hold reset state for 100 ns.
        wait for 100 ns;
                a<="0101";
         b<="0100";
         sel<="010";


        -- hold reset state for 100 ns.
        wait for 100 ns;
a<="0101";
         b<="0100";
         sel<="011";


        -- hold reset state for 100 ns.
        wait for 100 ns;
                a<="0101";
         b<="0100";
         sel<="100";


        -- hold reset state for 100 ns.
        wait for 100 ns;
                a<="0101";
         b<="0100";
         sel<="101";
```

```
        -- hold reset state for 100 ns.
        wait for 100 ns;
a<="0101";
         b<="0100";
         sel<="110";

        -- hold reset state for 100 ns.
        wait for 100 ns;
                a<="0101";
         b<="0100";
         sel<="111";

        -- hold reset state for 100 ns.
        wait for 100 ns;

--          wait for <clock>_period*10;

        -- insert stimulus here

        wait;
```

```
    end process;

END;
```




```
net a(0) loc="p101";

net a(1) loc="p100";

net a(2) loc="p97";

net a(3) loc="p96";

net b(0) loc="p87";

net b(1) loc="p86";

net b(2) loc="p85";

net b(3) loc="p81";

net sel(0) loc="p78";
```

net sel(1) loc="p77";

net sel(2) loc="p74";

net y(0) loc="p168";

net y(1) loc="p171";

net y(2) loc="p172";

net y(3) loc="p175";

Release 14.1 - xst P.15xf (nt64)

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.11 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.11 secs

--> Reading design: vlsi.prj

TABLE OF CONTENTS

3) Design Hierarchy Analysis

4) HDL Analysis

5) HDL Synthesis

5.1) HDL Synthesis Report

6) Advanced HDL Synthesis

6.1) Advanced HDL Synthesis Report

7) Low Level Synthesis

8) Partition Report

9) Final Report

9.1) Device utilization summary

9.2) Partition Resource Summary

9.3) TIMING REPORT

===

* Synthesis Options Summary *

===

---- Source Parameters

Input File Name : "vlsi.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "vlsi"

Output Format : NGC

Target Device : xc3s400-4-pq208

---- Source Options

Top Module Name : vlsi

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : Yes

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : Yes

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : Auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 8

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

==========

==========

* HDL Compilation *

==========

Compiling vhdl file "C:/.Xilinx/bitalu/vlsi.vhd" in Library work.

Architecture behavioral of Entity vlsi is up to date.

==========

* Design Hierarchy Analysis *

==========

Analyzing hierarchy for entity <vlsi> in library <work> (architecture <behavioral>).

==========

* HDL Analysis *

==========

Analyzing Entity <vlsi> in library <work> (Architecture <behavioral>).

Entity <vlsi> analyzed. Unit <vlsi> generated.

===

* HDL Synthesis *

===

Performing bidirectional port resolution...

Synthesizing Unit <vlsi>.

    Related source file is "C:/.Xilinx/bitalu/vlsi.vhd".

    Found 4-bit 8-to-1 multiplexer for signal <y>.

    Found 4-bit addsub for signal <y$addsub0000>.

    Summary:

        inferred 1 Adder/Subtractor(s).

        inferred 4 Multiplexer(s).

Unit <vlsi> synthesized.

INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic operations in this design can share the same physical resources for reduced device utilization. For improved clock frequency you may try to disable resource sharing.

===

HDL Synthesis Report

Macro Statistics

Adders/Subtractors : 1

4-bit addsub : 1

Multiplexers : 1

4-bit 8-to-1 multiplexer : 1

==========

==========

* Advanced HDL Synthesis *

==========

==========

Advanced HDL Synthesis Report

Macro Statistics

Adders/Subtractors : 1

4-bit addsub : 1

Multiplexers : 1

4-bit 8-to-1 multiplexer : 1

==========

==========

* Low Level Synthesis *

==========

Optimizing unit <vlsi> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block vlsi, actual ratio is 0.

Final Macro Processing ...

==========

Final Register Report

Found no macro

==========

==========

* Partition Report *

==========

Partition Implementation Status

No Partitions were found in this design.

==========

* Final Report *

==========

Final Results

RTL Top Level Output File Name : vlsi.ngr

Top Level Output File Name : vlsi

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

IOs : 15

Cell Usage :

BELS : 34

LUT2 : 5

LUT3 : 10

LUT4 : 6

MUXF5 : 9

MUXF6 : 4

IO Buffers : 15

IBUF : 11

OBUF : 4

==========

Device utilization summary:

Selected Device : 3s400pq208-4

Number of Slices:	11	out of	3584	0%
Number of 4 input LUTs:	21	out of	7168	0%
Number of IOs:	15			
Number of bonded IOBs:	15	out of	141	10%

Partition Resource Summary:

No Partitions were found in this design.

==========

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -4

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 14.616ns

Timing Detail:

All values displayed in nanoseconds (ns)

==========

Timing constraint: Default path analysis

Total number of paths / destination ports: 87 / 4

Delay: 14.616ns (Levels of Logic = 8)

Source: sel<0> (PAD)

Destination: y<3> (PAD)

Data Path: sel<0> to y<3>

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	14	0.821	1.382	sel_0_IBUF (sel_0_IBUF)
LUT3:I1->O	3	0.551	0.907	y_mux00001 (y_mux00001)
MUXF5:S->O	2	0.621	1.216	Maddsub_y_addsub0000_cy<1>1_f5 (Maddsub_y_addsub0000_cy<1>)
LUT4:I0->O	1	0.551	0.869	Maddsub_y_addsub0000_xor<3>11_SW0 (N2)
LUT3:I2->O	1	0.551	0.000	Maddsub_y_addsub0000_xor<3>11 (y_addsub0000<3>)
MUXF5:I0->O	1	0.360	0.000	Mmux_y_4_f5_2 (Mmux_y_4_f53)
MUXF6:I0->O	1	0.342	0.801	Mmux_y_2_f6_2 (y_3_OBUF)
OBUF:I->O		5.644		y_3_OBUF (y<3>)
Total		14.616ns (9.441ns logic, 5.175ns route) (64.6% logic, 35.4% route)		

==========

Total REAL time to Xst completion: 4.00 secs

Total CPU time to Xst completion: 4.05 secs

-->

Total memory usage is 4493188 kilobytes

Number of errors : 0 (0 filtered)

Number of warnings : 0 (0 filtered)

Number of infos : 1 (0 filtered)

net a loc="p97";

net b loc="p100";

net cin loc="p101";

net s loc="p171";

net c loc="p168";