

EXPERIMENT NO:1

Half Adder

```
library IEEE;
```

```
use IEEE.STD_LOGIC_1164.ALL;
```

```
-- Uncomment the following library declaration if using
```

```
-- arithmetic functions with Signed or Unsigned values
```

```
--use IEEE.NUMERIC_STD.ALL;
```

```
-- Uncomment the following library declaration if instantiating
```

```
-- any Xilinx primitives in this code.
```

```
--library UNISIM;
```

```
--use UNISIM.VComponents.all;
```

```
entity adder is
```

```
    Port ( a : in  STD_LOGIC;
```

```
          b : in  STD_LOGIC;
```

```
          s : out  STD_LOGIC;
```

```
          c : out  STD_LOGIC);
```

```
end adder;
```

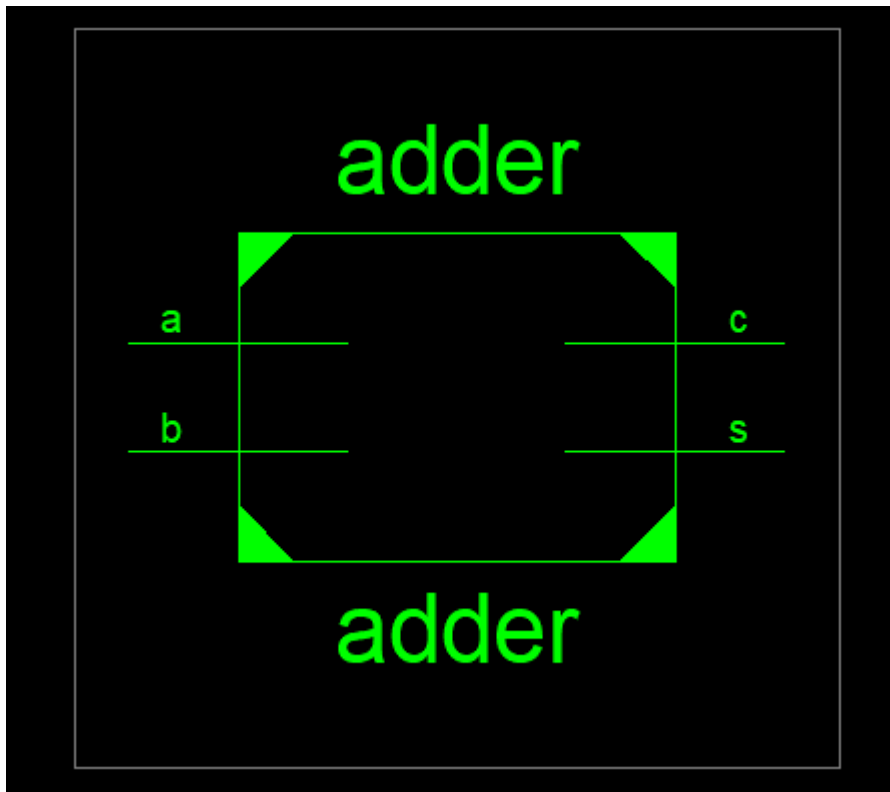
```
architecture Behavioral of adder is
```

```
begin
```

```
s<=a xor b;
```

```
c<=a and b;
```

```
end Behavioral;
```



```
LIBRARY ieee;
```

```
USE ieee.std_logic_1164.ALL;
```

```
-- Uncomment the following library declaration if using
```

```
-- arithmetic functions with Signed or Unsigned values
```

```
--USE ieee.numeric_std.ALL;
```

ENTITY hadder IS

END hadder;

ARCHITECTURE behavior OF hadder IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT adder

PORT(

a : IN std_logic;

b : IN std_logic;

s : OUT std_logic;

c : OUT std_logic

);

END COMPONENT;

--Inputs

signal a : std_logic := '0';

signal b : std_logic := '0';

--Outputs

signal s : std_logic;

signal c : std_logic;

```

-- No clocks detected in port list. Replace <clock> below with
-- appropriate port name

--constant <clock>_period : time := 10 ns;

BEGIN

    -- Instantiate the Unit Under Test (UUT)

    uut: adder PORT MAP (

        a => a,

        b => b,

        s => s,

        c => c

    );

    -- Clock process definitions

    -- <clock>_process :process

    -- begin

    --     <clock> <= '0';

    --     wait for <clock>_period/2;

    --     <clock> <= '1';

    --     wait for <clock>_period/2;

    -- end process;

    --

```

```
-- Stimulus process

stim_proc: process

begin

a<='0';

b<='0';

    -- hold reset state for 100 ns.

    wait for 100 ns;

a<='0';

b<='1';

    -- hold reset state for 100 ns.

    wait for 100 ns;

a<='1';

b<='0';

    -- hold reset state for 100 ns.

    wait for 100 ns;

a<='1';

b<='1';

    -- hold reset state for 100 ns.

    wait for 100 ns;

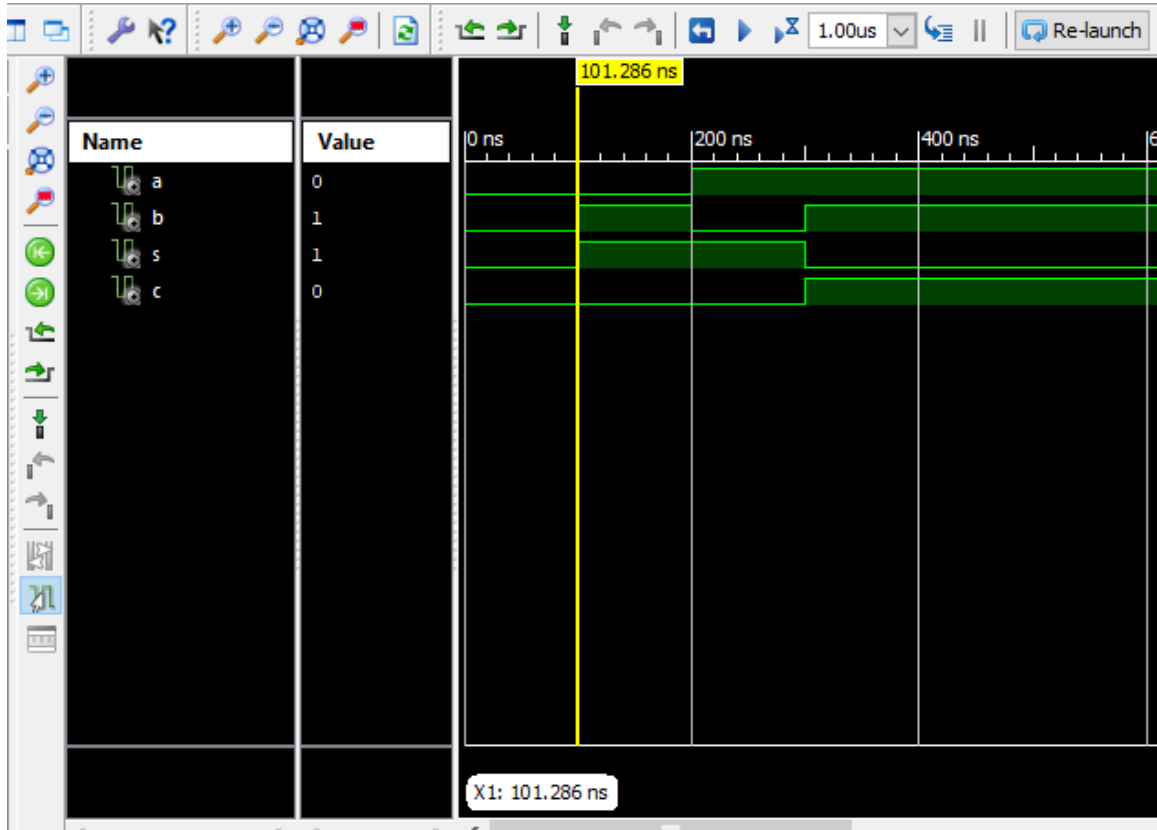
    --wait for <clock>_period*10;

    -- insert stimulus here

wait;
```

end process;

END;



Full Adder

```
library IEEE;
```

```
use IEEE.STD_LOGIC_1164.ALL;
```

```
-- Uncomment the following library declaration if using
```

```
-- arithmetic functions with Signed or Unsigned values
```

```
--use IEEE.NUMERIC_STD.ALL;
```

```
-- Uncomment the following library declaration if instantiating
```

```
-- any Xilinx primitives in this code.
```

```
--library UNISIM;
```

```
--use UNISIM.VComponents.all;
```

```
entity fulladder is
```

```
    Port ( x : in  STD_LOGIC;
```

```
           y : in  STD_LOGIC;
```

```
           z : in  STD_LOGIC;
```

```
           s : out STD_LOGIC;
```

```
           c : out STD_LOGIC);
```

```
end fulladder;
```

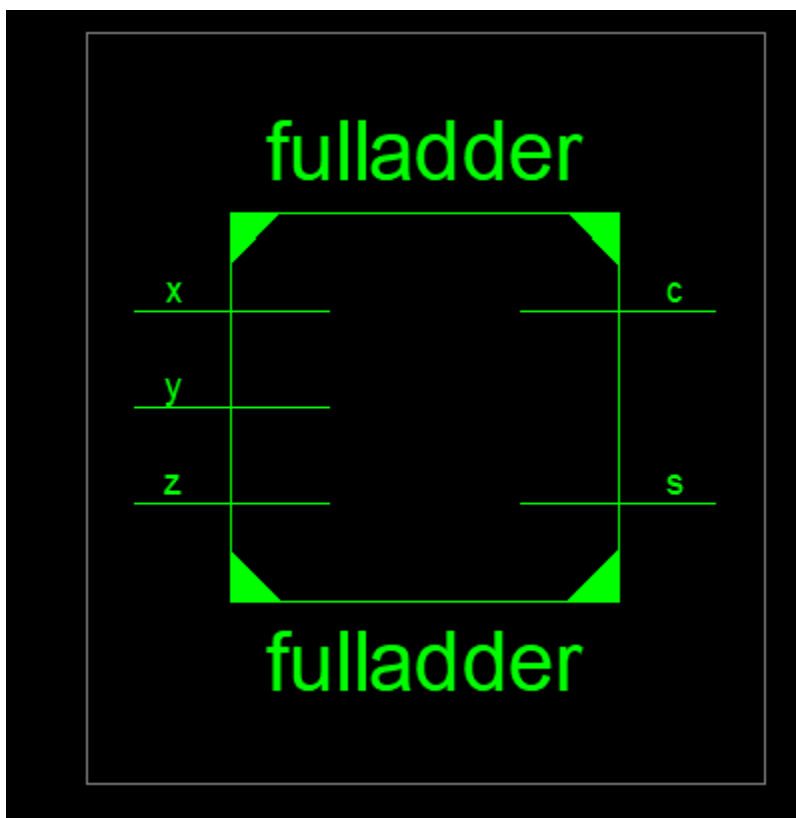
```
architecture Behavioral of fulladder is
```

```
begin
```

```
s<=(x xor y)xor z;
```

```
c<=((x xor y) and z) or (x and z);
```

```
end Behavioral;
```



```
LIBRARY ieee;
```

```
USE ieee.std_logic_1164.ALL;
```

```
-- Uncomment the following library declaration if using
```

```
-- arithmetic functions with Signed or Unsigned values
```



```
--USE ieee.numeric_std.ALL;
```

```
ENTITY fadder IS
```

```
END fadder;
```

```
ARCHITECTURE behavior OF fadder IS
```

```
    -- Component Declaration for the Unit Under Test (UUT)
```

```
    COMPONENT fulladder
```

```
    PORT(
```

```
        x : IN  std_logic;
```

```
        y : IN  std_logic;
```

```
        z : IN  std_logic;
```

```
        s : OUT std_logic;
```

```
        c : OUT std_logic
```

```
    );
```

```
END COMPONENT;
```

```
--Inputs
```

```
signal x : std_logic := '0';
```

```
signal y : std_logic := '0';
```

```
signal z : std_logic := '0';
```

```

        --Outputs

signal s : std_logic;

signal c : std_logic;

-- No clocks detected in port list. Replace <clock> below with
-- appropriate port name

--constant <clock>_period : time := 10 ns;

BEGIN

        -- Instantiate the Unit Under Test (UUT)

    uut: fulladder PORT MAP (

        x => x,

        y => y,

        z => z,

        s => s,

        c => c

    );

        -- Clock process definitions

    -- <clock>_process :process

    -- begin

    --         <clock> <= '0';

    --         wait for <clock>_period/2;

    --         <clock> <= '1';

```

```
--          wait for <clock>_period/2;

--    end process;

--
```

```
-- Stimulus process

stim_proc: process

begin

x<='0';

y<='0';

z<='0';

    -- hold reset state for 100 ns.

    wait for 100 ns;

x<='0';

y<='1';

z<='0';

    -- hold reset state for 100 ns.

    wait for 100 ns;

x<='0';

y<='0';

z<='1';

    -- hold reset state for 100 ns.

    wait for 100 ns;

x<='0';

y<='1';

z<='1';
```

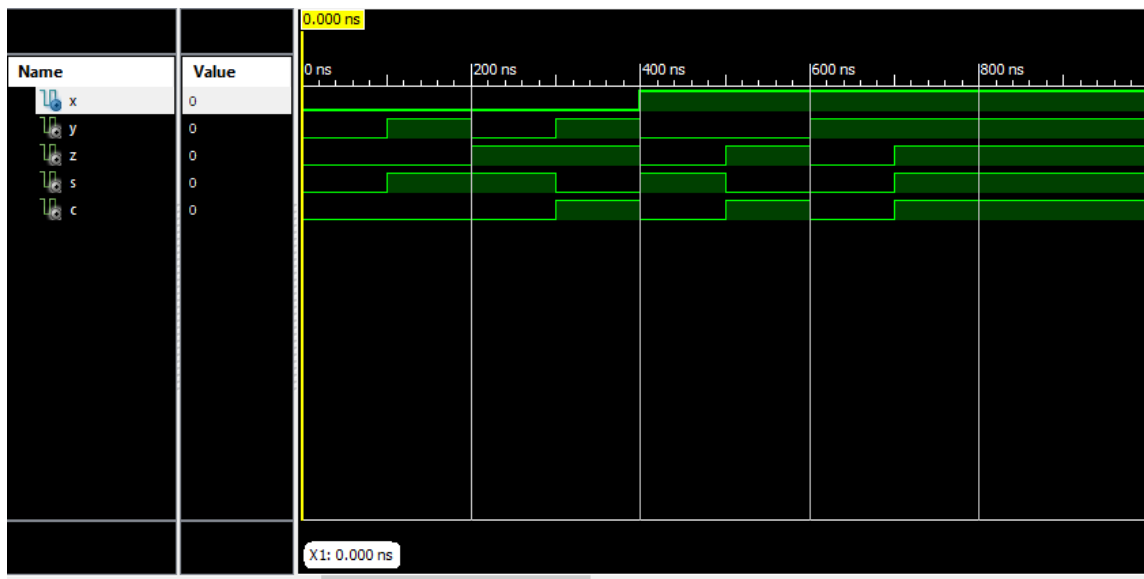
```
-- hold reset state for 100 ns.  
  
wait for 100 ns;  
  
x<='1';  
  
y<='0';  
  
z<='0';  
  
-- hold reset state for 100 ns.  
  
wait for 100 ns;  
  
x<='1';  
  
y<='0';  
  
z<='1';  
  
-- hold reset state for 100 ns.  
  
wait for 100 ns;  
  
x<='1';  
  
y<='1';  
  
z<='0';  
  
-- hold reset state for 100 ns.  
  
wait for 100 ns;  
  
x<='1';  
  
y<='1';  
  
z<='1';  
  
-- hold reset state for 100 ns.  
  
wait for 100 ns;  
  
  
--wait for <clock>_period*10;
```

-- insert stimulus here

wait;

end process;

END;



net "x" loc = "p101";

net "y" loc = "p100";

net "z" loc = "p97";

net "s" loc = "p171";

net "c" loc = "p172";

*

Final Report

*

=====

Final Results

RTL Top Level Output File Name : fulladder.ngr

Top Level Output File Name : fulladder

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

IOs : 5

Cell Usage :

BELS : 2

LUT3 : 2

IO Buffers : 5

IBUF : 3

OBUF : 2

=====

Device utilization summary:

Selected Device : 3s400pq208-4

Number of Slices:	1	out of	3584	0%
Number of 4 input LUTs:	2	out of	7168	0%
Number of IOs:	5			
Number of bonded IOBs:	5	out of	141	3%

Partition Resource Summary:

No Partitions were found in this design.

=====

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -4

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 9.033ns

Timing Detail:

All values displayed in nanoseconds (ns)

=====

Timing constraint: Default path analysis

Total number of paths / destination ports: 6 / 2

Delay: 9.033ns (Levels of Logic = 3)

Source: z (PAD)

Destination: c (PAD)

Data Path: z to c

		Gate		Net
Cell:in->out	fanout	Delay	Delay	Logical Name (Net Name)

IBUF:I->O	2	0.821	1.216	z_IBUF (z_IBUF)
LUT3:I0->O	1	0.551	0.801	c1 (c_OBUF)
OBUF:I->O		5.644		c_OBUF (c)

Total		9.033ns (7.016ns logic, 2.017ns route)		
		(77.7% logic, 22.3% route)		

=====

Total REAL time to Xst completion: 4.00 secs

Total CPU time to Xst completion: 3.66 secs

-->

Total memory usage is 4493176 kilobytes

Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)