

Stephen Oliver

Prof. Michel Fry

Computer Organization

2 February 2017

ASM Lab #3

PART 1:

The screenshot displays the ASMLab3_P1 - VisUAL interface. The left pane shows assembly code with line numbers 1 through 35. The right pane shows the state of registers R0 through R13, LR, and PC. The bottom status bar shows clock cycles and CSPR status bits.

Assembly Code (Left Pane):

```
1      ;Load    some starting values
2      MOVN    r0, #0      ;Max int
3      MOV     r1, #100
4      MOV     r2, #200
5
6      ;r3      = r1 + r2
7      ADD     r3, r1, r2
8
9      ;r4      = r1 + 1
10     ADD     r4, r1, #1
11
12     ;r4++
13     ADD     r4, r4, #1
14
15     ;load    some more values
16     MOV     r5, #50
17     MOV     r6, #200
18
19     ;r6      = r6 - r5
20     SUB     r6, r6, r5
21
22     ;r7      = r5 - r6
23     SUB     r7, r5, r6
24
25     ;r8      = r5 - 10
26     SUB     r8, r5, #10
27     ;SUB     r8, #10, r5 @Invalid! Immed value m
28
29     ;RSUB    reverses the order of the operands
30     ;r7      = r5 - r6 using RSUB
31     RSB     r7, r6, r5
32
33     ;r9      = 10 - r5
34     RSB     r9, r5, #10
35
```

Register Values (Right Pane):

Register	Value	Dec	Bin	Hex
R0	-1	Dec	Bin	Hex
R1	100	Dec	Bin	Hex
R2	200	Dec	Bin	Hex
R3	300	Dec	Bin	Hex
R4	102	Dec	Bin	Hex
R5	50	Dec	Bin	Hex
R6	150	Dec	Bin	Hex
R7	-100	Dec	Bin	Hex
R8	40	Dec	Bin	Hex
R9	-40	Dec	Bin	Hex
R10	0x0	Dec	Bin	Hex
R11	0x0	Dec	Bin	Hex
R12	0x0	Dec	Bin	Hex
R13	0xFF000000	Dec	Bin	Hex
LR	0x0	Dec	Bin	Hex
PC	0x38	Dec	Bin	Hex

Status Bar (Bottom):

Clock Cycles: Current Instruction: 1 Total: 13

CSPR Status Bits (NZCV): 0 0 0 0

PART 2.1:

ASMLab3_P2_1 - VisUAL

File Help

New Open Save Settings Tools Emulation Complete Line Issues 6 0 Execute Reset Step Backwards Step Forwards

Reset to continue editing code

1	MOV	r0, #32
2	ADD	r0, r0, #96
3	ADD	r0, r0, #128
4	ADD	r0, r0, #256
5	ADD	r0, r0, #512
6	ADD	r0, r0, #1024
7		

R0	2048	Dec	Bin	Hex
R1	0x0	Dec	Bin	Hex
R2	0x0	Dec	Bin	Hex
R3	0x0	Dec	Bin	Hex
R4	0x0	Dec	Bin	Hex
R5	0x0	Dec	Bin	Hex
R6	0x0	Dec	Bin	Hex
R7	0x0	Dec	Bin	Hex
R8	0x0	Dec	Bin	Hex
R9	0x0	Dec	Bin	Hex
R10	0x0	Dec	Bin	Hex
R11	0x0	Dec	Bin	Hex
R12	0x0	Dec	Bin	Hex
R13	0xFF000000	Dec	Bin	Hex
LR	0x0	Dec	Bin	Hex
PC	0x1C	Dec	Bin	Hex

Clock Cycles Current Instruction: 1 Total: 6

CSPR Status Bits (NZCV) 0 0 0 0

PART 2.2:

ASMLab3_P2_2 - [Unsaved] - VisUAL

File Help

New Open Save Settings Tools Emulation Complete Line 7 Issues 0 Execute Reset Step Backwards Step Forwards

Reset to continue editing code

1	MOV	r0, #2048
2	SUB	r0, r0, #1024
3	SUB	r0, r0, #512
4	SUB	r0, r0, #256
5	SUB	r0, r0, #128
6	SUB	r0, r0, #96
7	SUB	r0, r0, #32
8		

R0	0	Dec	Bin	Hex
R1	0x0	Dec	Bin	Hex
R2	0x0	Dec	Bin	Hex
R3	0x0	Dec	Bin	Hex
R4	0x0	Dec	Bin	Hex
R5	0x0	Dec	Bin	Hex
R6	0x0	Dec	Bin	Hex
R7	0x0	Dec	Bin	Hex
R8	0x0	Dec	Bin	Hex
R9	0x0	Dec	Bin	Hex
R10	0x0	Dec	Bin	Hex
R11	0x0	Dec	Bin	Hex
R12	0x0	Dec	Bin	Hex
R13	0xFF000000	Dec	Bin	Hex
LR	0x0	Dec	Bin	Hex
PC	0x20	Dec	Bin	Hex

Clock Cycles Current Instruction: 1 Total: 7

CSPR Status Bits (NZCV) 0 0 0 0

PART 3:

ASMLab3_P3 - VisUAL

File Help

New Open Save Settings Tools Emulation Complete Line 11 Issues 0 Execute Reset Step Backwards Step Forwards

Reset to continue editing code

1	MVN	r0, #0x80000000
2	MVN	r1, #0
3	MOV	r2, #0
4	MOV	r3, #0
5	MOV	r4, #0
6	MOV	r5, #0
7	ADD	r2, r0, #1
8	ADDS	r3, r0, #1
9	ADD	r4, r1, #1
10	ADDS	r5, r1, #1
11		

R0	2147483647	Dec	Bin	Hex
R1	-1	Dec	Bin	Hex
R2	-2147483648	Dec	Bin	Hex
R3	-2147483648	Dec	Bin	Hex
R4	0	Dec	Bin	Hex
R5	0	Dec	Bin	Hex
R6	0	Dec	Bin	Hex
R7	0x0	Dec	Bin	Hex
R8	0x0	Dec	Bin	Hex
R9	0x0	Dec	Bin	Hex
R10	0x0	Dec	Bin	Hex
R11	0x0	Dec	Bin	Hex
R12	0x0	Dec	Bin	Hex
R13	0xFF000000	Dec	Bin	Hex
LR	0x0	Dec	Bin	Hex
PC	0x2C	Dec	Bin	Hex

Clock Cycles Current Instruction: 1 Total: 10

CSPR Status Bits (NZCV) 0 1 1 0