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## ASM Lab 4

### PART 1:

The screenshot displays the ASM\_Lab4\_P1 - VisUAL emulator interface. The main window is divided into several sections:

- Top Bar:** Contains menu options (File, Help), a toolbar with buttons (New, Open, Save, Settings, Tools), and a status bar indicating "Emulation Complete" with line and issue counts (38, 0). Buttons for "Execute", "Reset", and "Step Backwards by one instruction" are also present.
- Assembly Code Editor:** Displays assembly code with line numbers 9 through 39. The code includes instructions like ASR, LSL, MOV, ROR, and TEQ, along with comments explaining the operations and register values.
- Register Window:** A table showing the current values of registers R0 through R13 and the Link Register (LR). The values are displayed in hexadecimal, decimal, and binary formats.
- Clock Cycles:** A section at the bottom showing the current instruction (1) and total instructions (22). It also displays the CSRR Status Bits (NZCV) as 1, 0, 1, 0.

**Assembly Code (Lines 9-39):**

```
9      ASR      r4, r3, #2 ;r4 = 0000 ... 0000 0000 010
10     ;
11     ;Shift    r3 by number of bits in r4 (4), result
12     LSL      r5, r3, r4 ;using register addressing i
13     ;
14     ;Right    rotate examples
15     MOV      r1, #0x12 ;r1 = 0000 0000 ... 0000 0001
16     ROR      r2, r1, #1 ;r2 = 0000 0000 ... 0000 000
17     ROR      r3, r2, #4 ;r3 = 1001 .... 0000 0000 00
18     ;
19     ;No       Rotate Left, instead rotate left x bits
20     MOV      r5, #0x12 ;r5 = 0x12
21     ;Rotate   r5 left 12 bits by ROR (32-12) = 20 bit
22     ROR      r6, r5, #20 ;r6 = 0x12000
23     ;
24     ;TEST     comparison opcodes and observe the CSP
25     MOV      r7, #3
26     MOV      r8, #3
27     MOV      r9, #-3
28     MVN      r10, #3 ;Complimented bit value of 3
29     ;CMP      and CMN examples
30     CMP      r7, r8 ;SUBTRACT same, so Zero flag set
31     CMP      r7, r9 ;SUBTRACT Not the same so no fla
32     CMN      r7, r8 ;ADD same, so no flag set
33     CMN      r7, r9 ;ADD Oposite sige, so Zero flag
34     ;TST      and TEQ examples, Pay attention to the
35     TST      r7, r8 ;BITWISE ANDS
36     TST      r7, r10 ;BITWISE ANDS
37     TEQ      r7, r8 ;BITWISE EORS
38     TEQ      r7, r10 ;BITWISE EORS
39
```

**Register Values:**

Register	Value (Hex)	Value (Dec)	Value (Bin)
R0	0x0	0	0
R1	0x12	18	1100
R2	0x9	9	1001
R3	0x90000000	2415919104	1001 0000 0000 0000 0000 0000 0000 0000
R4	0x19	25	10011
R5	0x12	18	1100
R6	0x12000	73728	1 0011 0000 0000 0000 0000 0000 0000
R7	0x3	3	11
R8	0x3	3	11
R9	0xFFFFFFF	268435455	1111 1111 1111 1111 1111 1111 1111 1111
R10	0xFFFFFFF	268435455	1111 1111 1111 1111 1111 1111 1111 1111
R11	0x0	0	0
R12	0x0	0	0
R13	0xFF000000	4294967040	1111 1111 1111 0000 0000 0000 0000 0000
LR	0x0	0	0

**Clock Cycles:** Current Instruction: 1 Total: 22

**CSRR Status Bits (NZCV):** 1 0 1 0

## PART 2.1:

ASM\_Lab4\_P2\_1 - VisUAL

File Help

New Open Save Settings Tools Emulation Complete Line 9 Issues 0 Execute Reset Step Backwards Step Forwards

Reset to continue editing code

1	MOV	r1, #1
2	LSL	r1, r1, #1
3	LSL	r1, r1, #1
4	LSL	r1, r1, #1
5	LSL	r1, r1, #1
6	LSL	r1, r1, #1
7	LSL	r1, r1, #1
8	LSL	r1, r1, #1
9	LSL	r1, r1, #1
10		

Shift

R0	0x0	Dec	Bin	Hex
R1	256	Dec	Bin	Hex
R2	0x0	Dec	Bin	Hex
R3	0x0	Dec	Bin	Hex
R4	0x0	Dec	Bin	Hex
R5	0x0	Dec	Bin	Hex
R6	0x0	Dec	Bin	Hex
R7	0x0	Dec	Bin	Hex
R8	0x0	Dec	Bin	Hex
R9	0x0	Dec	Bin	Hex
R10	0x0	Dec	Bin	Hex
R11	0x0	Dec	Bin	Hex
R12	0x0	Dec	Bin	Hex
R13	0xFF000000	Dec	Bin	Hex
LR	0x0	Dec	Bin	Hex

Clock Cycles Current Instruction: 1 Total: 9

CSPR Status Bits (NZCV) 0 0 0 0

## PART 2.2:

ASM\_Lab4\_P2\_2 - VisUAL

File Help

New Open Save Settings Tools Emulation Complete Line 9 Issues 0 Execute Reset Step Backwards Step Forwards

Reset to continue editing code

1	MOV	r1, #256
2	LSR	r1, r1, #1
3	LSR	r1, r1, #1
4	LSR	r1, r1, #1
5	LSR	r1, r1, #1
6	LSR	r1, r1, #1
7	LSR	r1, r1, #1
8	LSR	r1, r1, #1
9	LSR	r1, r1, #1
10		

Shift

R0	0x0	Dec	Bin	Hex
R1	1	Dec	Bin	Hex
R2	0x0	Dec	Bin	Hex
R3	0x0	Dec	Bin	Hex
R4	0x0	Dec	Bin	Hex
R5	0x0	Dec	Bin	Hex
R6	0x0	Dec	Bin	Hex
R7	0x0	Dec	Bin	Hex
R8	0x0	Dec	Bin	Hex
R9	0x0	Dec	Bin	Hex
R10	0x0	Dec	Bin	Hex
R11	0x0	Dec	Bin	Hex
R12	0x0	Dec	Bin	Hex
R13	0xFF000000	Dec	Bin	Hex
LR	0x0	Dec	Bin	Hex

Clock Cycles Current Instruction: 1 Total: 9

CSPR Status Bits (NZCV) 0 0 0 0