Stephen Oliver
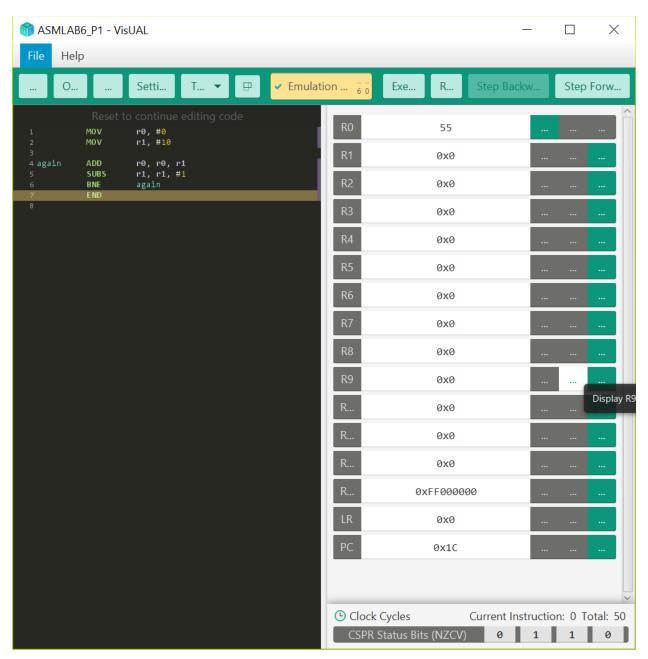
Professor Fry

Computer Organization

21 February 2017

<p style="text-align:center">ASM Lab 5/6</p>

PART 1::

PART 2::


```
          Reset to continue editing code
 1          MOV      r0, #3      ;r0 is current number
 2          MOV      r1, #0      ;r1 is count of number of
 3
 4 again    ADD      r1, r1, #1      ;increment number of
 5          ANDS     r7, r0, #1      ;test whether r0 is o
 6          BEQ      even
 7          ADD      r0, r0, r0, LSL #1  ;if odd, set r0
 8          ADD      r0, r0, #1
 9          B        again       ;and repeat (guaranteed r0
10 even     MOV      r0, r0, ASR #1 ;if even, set r0 = r0
11          SUBS     r7, r0, #1      ;and repeat if r0 !=
12          BNE      again
13 halt     END      ;stop computation
14
```

Register	Value			
R0	1	...	...	...
R1	7	...	...	...
R2	0x0	...	...	...
R3	0x0	...	...	...
R4	0x0	...	...	...
R5	0x0	...	...	...
R6	0x0	...	...	...
R7	0	...	...	...
R8	0x0	...	...	...
R9	0x0	...	...	...
R...	0x0	...	...	...
R...	0x0	...	...	...
R...	0x0	...	...	...
R...	0xFF000000	...	...	...
LR	0x0	...	...	...
PC	0x34	...	...	...

🕐 Clock Cycles   Current Instruction: 0 Total: 66

| CSPR Status Bits (NZCV) | 0 | 1 | 1 | 0 |