

We will be generating a 5-to-32 decoder hierarchically in Verilog. Please begin by generating a 2-to-4 decoder defined as follows:

module decoder2_4(in[1:0], out[3:0])

```
module decoder2_4(  
    input [1:0] in,  
    output [3:0] out  
);  
  
    reg [3:0] out;  
  
    always @(in) begin  
        case (in)  
            2'b00: out = 4'b0001;  
            2'b01: out = 4'b0010;  
            2'b10: out = 4'b0100;  
            2'b11: out = 4'b1000;  
        endcase  
    end  
  
endmodule
```