perplexity

We will be generating a 64-to-1 multiplexer hierarchically in Verilog. Please begin by generating a 2-to-1 multiplexer defined as follows:

module mux2_1(in1, in2, select, out)

```
module mux2_1(in1, in2, select, out);
    input in1, in2;
    input select;
    output out;

    assign out = select ? in2 : in1;

endmodule
```