perplexity

We will be generating a 5-to-32 decoder hierarchically in Verilog. Please begin by generating a 2-to-4 decoder defined as follows:

module decoder2_4(in[1:0], out[3:0])

```
module decoder2_4(
    input [1:0] in,
    output [3:0] out
);
    assign out[0] = ~in[1] & ~in[0];
    assign out[1] = ~in[1] & in[0];
    assign out[2] = in[1] & ~in[0];
    assign out[3] = in[1] & in[0];
endmodule
```