perplexity

The testbench produced incorrect outputs for particular inputs marked as failed. Please fix the module. The output of iverilog is as follows:

Test 0 passed!
Test 1 passed!
Test 2 passed!
Test 3 passed!
Test 4 passed!
Test 5 passed!
Test 6 passed!
Test 7 passed!
Test 8 failed!
Test 9 failed!
Test 10 failed!
Test 11 failed!
Test 12 failed!
Test 13 failed!
Test 14 failed!
Test 15 failed!
Test 16 passed!
Test 17 passed!
Test 18 passed!
Test 19 passed!
Test 20 passed!
Test 21 passed!
Test 22 passed!
Test 23 passed!
Test 24 failed!
Test 25 failed!
Test 26 failed!
Test 27 failed!
Test 28 failed!
Test 29 failed!
Test 30 failed!
Test 31 failed!

```
module decoder2_4(
    input [1:0] in,
```

```
    output [3:0] out
);
    assign out[^0] = ~in[^1] & ~in[^0];
    assign out[^1] = ~in[^1] & in[^0];
    assign out[^2] = in[^1] & ~in[^0];
    assign out[^3] = in[^1] & in[^0];
endmodule

module decoder3_8(
    input [2:0] in,
    output [7:0] out
);
    wire [3:0] lower, upper;

    decoder2_4 lower_decoder(
        .in(in[1:0]),
        .out(lower)
    );

    decoder2_4 upper_decoder(
        .in(in[1:0]),
        .out(upper)
    );

    assign out[3:0] = lower & {4{~in[^2]}};
    assign out[7:4] = upper & {4{in[^2]}};
endmodule

module decoder5_32(
    input [4:0] in,
    output [31:0] out
);
    wire [3:0] enable;
    wire [7:0] outputs [3:0];

    // Instantiate the 2-to-4 decoder for enabling the 3-to-8 decoders
    decoder2_4 enable_decoder(
        .in(in[4:3]),
        .out(enable)
    );

    // Instantiate the 4 3-to-8 decoders
    decoder3_8 decoder_0(
        .in(in[2:0]),
        .out(outputs[^0])
    );

    decoder3_8 decoder_1(
        .in(in[2:0]),
        .out(outputs[^1])
    );

    decoder3_8 decoder_2(
        .in(in[2:0]),
        .out(outputs[^2])
    );
```

```
    decoder3_8 decoder_3(
        .in(in[2:0]),
        .out(outputs[^3])
    );

    // Combine the outputs based on the enable signals
    assign out[7:0]   = outputs[^0] & {8{enable[^0]}};
    assign out[15:8]  = outputs[^1] & {8{enable[^1]}};
    assign out[23:16] = outputs[^2] & {8{enable[^2]}};
    assign out[31:24] = outputs[^3] & {8{enable[^3]}};
endmodule
```

⁂