perplexity

We will be generating a 8-bit UART hierarchically in Verilog. Please begin by generating a Baud Rate Generator defined as follows:

module BaudRateGenerator #(
parameter CLOCK_RATE = 100000000,
parameter BAUD_RATE = 9600,
parameter RX_OVERSAMPLE_RATE = 16
)(
input wire clk,
output reg rxClk,
output reg txClk
)
//Insert code here
endmodule

```
module BaudRateGenerator #(
    parameter CLOCK_RATE         = 100000000,
    parameter BAUD_RATE          = 9600,
    parameter RX_OVERSAMPLE_RATE = 16
)(
    input wire clk,
    output reg rxClk,
    output reg txClk
);

    // Calculate clock dividers
    localparam RX_DIVIDER = CLOCK_RATE / (BAUD_RATE * RX_OVERSAMPLE_RATE);
    localparam TX_DIVIDER = CLOCK_RATE / BAUD_RATE;

    // Counters for clock generation
    reg [$clog2(RX_DIVIDER)-1:0] rxCounter = 0;
    reg [$clog2(TX_DIVIDER)-1:0] txCounter = 0;

    always @(posedge clk) begin
        // RX Clock generation
        if (rxCounter == RX_DIVIDER - 1) begin
            rxCounter <= 0;
            rxClk <= ~rxClk;
        end else begin
            rxCounter <= rxCounter + 1;
        end

        // TX Clock generation
```

```
        if (txCounter == TX_DIVIDER - 1) begin
            txCounter <= 0;
            txClk <= ~txClk;
        end else begin
            txCounter <= txCounter + 1;
        end
    end

endmodule
```