

## We are generating a 64-to-1 multiplexer hierarchically in Verilog. We have generated 2-to-1 multiplexer defined as follows:

```
module mux2_1(in1, in2, select, out);  
input in1, in2;  
input select;  
output out;
```

```
    assign out = select ? in2 : in1;
```

```
endmodule
```

Please include the previous module(s) in your response and use them to hierarchically generate a 4-to-1 multiplexer defined as:

```
module mux4_1(in[3:0], select, out);  
//Insert code here  
endmodule
```

```
module mux2_1(in1, in2, select, out);  
    input in1, in2;  
    input select;  
    output out;
```

```
    assign out = select ? in2 : in1;
```

```
endmodule
```

```
module mux4_1(in, select, out);  
    input [3:0] in;  
    input [1:0] select;  
    output out;
```

```
    wire mux_out1, mux_out2;
```

```
    // First level of 2-to-1 multiplexers
```

```
    mux2_1 mux1 (.in1(in[0]), .in2(in[1]), .select(select[0]), .out(mux_out1));
```

```
    mux2_1 mux2 (.in1(in[2]), .in2(in[3]), .select(select[0]), .out(mux_out2));
```

```
    // Second level of 2-to-1 multiplexer
```

```
    mux2_1 mux3 (.in1(mux_out1), .in2(mux_out2), .select(select[1]), .out(out));
```

endmodule