perplexity

We are generating a 5-to-32 decoder hierarchically in Verilog. We have generated 2-to-4 decoder defined as follows:

```
module decoder2_4(
input [1:0] in,
output [3:0] out
);

reg [3:0] out;

always @(in) begin
case (in)
2'b00: out = 4'b0001;
2'b01: out = 4'b0010;
2'b10: out = 4'b0100;
2'b11: out = 4'b1000;
endcase
end

endmodule
```

Please include the previous module(s) in your response and use them to hierarchically generate a 3-to-8 decoder defined as:

```
module decoder3_8(in[2:0], out[7:0]);
//Insert code here
endmodule
```

```
module decoder2_4(
    input [1:0] in,
    output [3:0] out
);

  reg [3:0] out;

  always @(in) begin
    case (in)
      2'b00: out = 4'b0001;
      2'b01: out = 4'b0010;
      2'b10: out = 4'b0100;
      2'b11: out = 4'b1000;
    endcase
  end
```

```
endmodule

module decoder3_8(
    input [2:0] in,
    output [7:0] out
);

  wire [3:0] out_low;
  wire [3:0] out_high;

  decoder2_4 decoder_low (
    .in(in[1:0]),
    .out(out_low)
  );

  decoder2_4 decoder_high (
    .in(in[1:0]),
    .out(out_high)
  );

  assign out[3:0] = (in[2] == 0) ? out_low : 4'b0000;
  assign out[7:4] = (in[2] == 1) ? out_high : 4'b0000;

endmodule
```