

## The testbench failed to compile. Please fix the module. The output of iverilog is as follows:

error: out is not a valid l-value in decoder2\_4.  
out is declared here as wire.

The issue arises because you are trying to assign a value to an output declared as a wire inside an always block. In Verilog, wires cannot be assigned values within procedural blocks (like always or initial blocks); they can only be assigned using continuous assignments outside these blocks. However, if you declare the output as a reg, you can assign values to it inside procedural blocks. Here's how you can modify your module:

```
module decoder2_4(  
    input [1:0] in,  
    output reg [3:0] out  
);  
  
    always @(in) begin  
        case (in)  
            2'b00: out = 4'b0001;  
            2'b01: out = 4'b0010;  
            2'b10: out = 4'b0100;  
            2'b11: out = 4'b1000;  
            default: out = 4'b0000;  
        endcase  
    end  
  
endmodule
```

Alternatively, you can use continuous assignment if you prefer not to use procedural blocks:

```
module decoder2_4(  
    input [1:0] in,  
    output wire [3:0] out  
);  
  
    assign out[0] = ~in[1] & ~in[0];  
    assign out[1] = ~in[1] & in[0];  
    assign out[2] = in[1] & ~in[0];  
    assign out[3] = in[1] & in[0];  
  
endmodule
```

