perplexity

We will be generating a 64-to-1 multiplexer hierarchically in Verilog. Please begin by generating a 2-to-1 multiplexer defined as follows:

module mux2_1(in1, in2, select, out)

Here is a basic implementation of a 2-to-1 multiplexer in Verilog:

```
module mux2_1(
    input in1,
    input in2,
    input select,
    output out
);

    assign out = (select) ? in2 : in1;

endmodule
```

This module uses a ternary operator to select between `in1` and `in2` based on the `select` input. If `select` is high (1), `out` will be assigned the value of `in2`; otherwise, it will be assigned the value of `in1`.