perplexity

We will be generating a 8-bit UART hierarchically in Verilog. Please begin by generating a Baud Rate Generator defined as follows:

module BaudRateGenerator #(
parameter CLOCK_RATE = 100000000,
parameter BAUD_RATE = 9600,
parameter RX_OVERSAMPLE_RATE = 16
)(
input wire clk,
output reg rxClk,
output reg txClk
)
//Insert code here
endmodule

```
module BaudRateGenerator #(
    parameter CLOCK_RATE = 100000000,
    parameter BAUD_RATE = 9600,
    parameter RX_OVERSAMPLE_RATE = 16
)(
    input wire clk,
    output reg rxClk,
    output reg txClk
);

reg [31:0] rx_counter;
reg [31:0] tx_counter;
localparam RX_DIVISOR = CLOCK_RATE / (BAUD_RATE * RX_OVERSAMPLE_RATE);
localparam TX_DIVISOR = CLOCK_RATE / BAUD_RATE;


always @(posedge clk) begin
    rx_counter <= rx_counter + 1;
    if (rx_counter >= RX_DIVISOR) begin
        rxClk <= ~rxClk;
        rx_counter <= 0;
    end
end

always @(posedge clk) begin
    tx_counter <= tx_counter + 1;
    if (tx_counter >= TX_DIVISOR) begin
        txClk <= ~txClk;
```

```
        tx_counter <= 0;
    end
end

endmodule
```