perplexity

The testbench produced incorrect outputs for many of the shift values mentioned below. Please fix the module. The output of iverilog is as follows:

Time=0 sel=0 input=a5a5a5a5 shift= 1 output=00000001
Time=10000 sel=0 input=a5a5a5a5 shift= 8 output=000000a5
Time=20000 sel=0 input=a5a5a5a5 shift=16 output=0000a5a5
Time=30000 sel=1 input=a5a5a5a5 shift= 1 output=80000000
Time=40000 sel=1 input=a5a5a5a5 shift= 8 output=a5000000
Time=50000 sel=1 input=a5a5a5a5 shift=16 output=a5a50000
Time=60000 sel=1 input=a5a5a5a5 shift= 0 output=00000000
Time=70000 sel=1 input=a5a5a5a5 shift=31 output=4b4b4b4a

```
module barrel_shift_32_w_rotation_ctrl(
  input sel_left_or_right_rotate,
  input [31:0] inputData,
  input [4:0] shiftVal,
  output [31:0] outputData
);

  reg [31:0] shifted_data;

  always @* begin
    if (sel_left_or_right_rotate == 1'b1) begin // Right Rotate
      shifted_data = {inputData[shiftVal-1:0], inputData[31:shiftVal]};
    end else begin // Left Rotate
      shifted_data = {inputData[31-shiftVal:0], inputData[31:32-shiftVal]};
    end
  end

  assign outputData = shifted_data;

endmodule
```

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