Skanda Koppula

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Massachusetts Institute of Technology
Masters of Engineering, BSc, Computer Systems, MEng GPA: 5.0/5.0 *Sept. 2013 - Expected February 2018*

Relevant courses: Hardware Architecture for Deep Learning, Computer and Network Security, Compilers, Operating Systems, Computer Architecture, Bayesian Inference, Machine Learning

Projects

MIT Formula SAE Racecar Electronics Team *October 2015 - Present*

- Designed PCBs and wrote firmware for open-source automotive battery management system. Orchestrates battery dis/charging state, balancing, safety checks, charging algorithms. https://github.com/MITEVT/ltc-battery-controller
- Demonstrated a CNN-based controller for a driverless Formula racecar. Wrote simulator, real-time controller, and tested RL-based approaches. https://arxiv.org/abs/1708.02215

Power-Based Side-Channel Attack on ATMega328 *Nov. 2015*

- Demonstrated extraction of an AES key from an Arduino's flash memory from chip's power traces. Implemented the Correlation Power Analysis attack.

Work Experience

Google Search, Research Intern *June 2017 - September 2017*

- Developed new method to visualize memory of recurrent neural networks, improving interpretability of end-to-end speech recognition networks.
- Resulted in paper accepted 2018 IEEE Conference on Acoustics and Signal Processing.

Yahoo Login Abuse, Software Engineering Intern *June 2016 - Aug. 2016*

- Prototyped neural network to classify account registration and login events on Yahoo services as spam. Demonstrated a 6% improvement in classifier's equal error rate from prior system. Deployed a multi-threaded data feed service to pull data from Facebook ThreatExchange to update classifier.

Square Security, Software Engineering Intern *June 2015 - Aug. 2015*

- Developed service to collect memory core crashdumps from Square card readers, symbolifying the binary contents to a human-readable source error trace.

Research

MIT Energy Efficient Circuits Group *Sept. 2015 - Present*

- Developed memory-efficient convolutional network for speaker identification. 10x size reduction and >100x decrease in energy consumption. Built custom hardware design on FPGA to evaluate ternarized speaker verification network.
- Paper accepted 2018 IEEE Conference on Acoustics and Signal Processing.

Skills

Embedded Systems/Electronics: **C**, **x86 Assembly**, **Altium**, **Vivado HLS**, and **Bluespec Verilog**.
Misc: **Python**, **C++**, **Java**, **Scala**, **shell scripting**, **TensorFlow/pytorch**
Web Systems: **JAX-RS/Jetty**, **Rails/RSpec**, **Flask, Django**

Awards

Cisco Snort Security Scholarship Recipient 2017
2nd Place North American FSAE Lincoln Electric Racing Competition (Team) 2017
Analog Devices Research and Innovation Scholar Award 2016